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F. H. Eisen
Program Manager

R. Zucca
Principal Investigator

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The scope of this program is to demonstrate a 4K GaAs static RAM having very low power dissipation, 1 μW/bit in standby, and a short access time, 10 ns, to meet the requirements of the DARPA Advanced On-Board Signal Process (AOSP).

At the end of the previous program, a RAM cell capable of the required power dissipation had been developed and a 256-bit RAM had been demonstrated.

In the six-month period covered by this report, the processing of several lots of three-inch wafers with 256-bit RAMs (mask set RM3) was completed. Modifications to the Cermet deposition process for high value resistors were

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(20) required to adapt to the processing of 3-inch wafers, resulting in resistor uniformity that is good or better than the Cermet resistor uniformity formerly achieved for 1-inch wafers.

Testing of the 256-bit RAM has been completed. A total of 15 totally functional RAMs have been identified. The read access time was as low as 1 ns. "Write" operations could be performed with 2 ns "write" pulses.

A 1K RAM was designed, and the corresponding mask set was completed, except for final checking and placement of the circuits on the reticle. Small changes in cell design were made to achieve higher tolerance to threshold voltage variation and to leakage currents. The peripheral circuits were redesigned placing emphasis on achieving low-power dissipation compatible with the lower dissipation of the cells, and yet maintaining a fast access time.

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SUMMARY

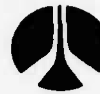
The scope of this program is to demonstrate a 4K GaAs static RAM having very low power dissipation, 1 μW/bit in standby, and short access time, 10 ns, to meet the requirements of the DARPA Advanced On-Board Signal Process (AOSP). High radiation tolerance (total dose and transient radiation) of GaAs circuits is also important for the AOSP application, and it will be evaluated and optimized within this program.

At the end of the previous program, a RAM cell capable of the required power dissipation had been developed, and a 256 bit RAM had been demonstrated. A Cermet resistor process was developed in order to provide the mega-ohm resistors required for the low power cells. In the final stage of the previous program, the fabrication of the 256 bit RAM was successfully implemented on 3-inch diameter GaAs wafers.

In the six-month period covered by this report the processing of several lots of three-inch wafers with 256 bit RAMs (mask set RM3) was completed. This process was affected by an early high rate of wafer breakage with an average loss of 23%. However, improvements in tooling at few critical steps have lowered the breakage rate to 18%, and further improvements are expected.

Processing was held up for some time due to difficulties with the Cermet deposition system. Poor adherence of the Cermet to the gold contacts, which occurred after the transition from 1-inch to 3-inch wafer processing, was resulting in poor resistor uniformity. With the implementation of a new deposition system the problem was corrected, and resistor standard deviations range now from 5 to 10% over 3-inch wafers. This uniformity is as good or better than the Cermet resistor uniformity formerly achieved for 1-inch wafers.

Testing of 256 bit RAM has been completed. A total of 15 totally functional RAMs have been identified, and a much larger number with a small number of failures were observed. The yield of functional RAMs is determined by design limitations on the peripheral circuits. Significant improvements are expected with the next design iteration.

 Rockwell International

Excellent results were obtained from access time measurements. The read access time was as low as 1 ns, with typical values of 5.5 ns. In "write" operations it was possible to routinely store data with 2 ns "write" pulses. Although the access time is conditioned to great extent by the peripheral circuits, these results indicate that the memory cell is capable of meeting not only the low-power requirements but also the high-speed (10 ns access time) specification.

Preliminary radiation experiments were carried out by exposing a wafer to a gamma dose of 10 Mrads. Measurements made before and after irradiation indicated that FET and diode parameters, with the exception of FET gate current and diode saturation current, generally exhibited only very small changes. The number of cell failures on individual RAM chips was found to be smaller after the radiation than before.

A 1K RAM was designed, and the corresponding mask set was completed, except for final checking and placement of the circuits on the reticle. The design of the 1K RAM included extensive simulation of all the circuits using the Spice program. Small changes in cell design were made to achieve higher tolerance to threshold voltage variation and to leakage currents. The changes consisted of lowering resistor values, lowering supply voltages, and increasing current levels. The peripheral circuits were redesigned placing emphasis on achieving low-power dissipation compatible with the low power dissipation of the cells, and yet maintaining a fast access time. This was accomplished by making extensive use of complementary drivers, and by including a switch that powers off most peripheral circuits when the chip is deselected. This 1K design can be expanded to 4K with only minor changes. The projected access time and standby power dissipation for a 4K RAM employing these circuits are 11 ns and 4.8 μW/bit, respectively. The latter represents the total chip power dissipation including the peripheral circuits and the power switch, divided by 4096, the number of memory cells.

1.0 INTRODUCTION

The development of a low-power radiation hard memory chip is motivated by the DARPA Advanced On-Board Signal Processor (AOSP) program. The goal of this program is to develop a flexible, multi-mission signal processor to fulfill the processing requirements of space based missions through the 1990's. The AOSP system specification translates into memory device specifications in the following manner. Long mission lifetimes (> 5 years) and space-based environmental conditions require a radiation hardened device technology capable of surviving total doses in excess of 10^6 rads. Power dissipations of 0.5 - 1 μW/bit are required due to the large memory sizes and limited power budget. The 4K memory design goals are summarized in Table 1-1.

Table 1-1
AOSP GaAs Memory Design Goals

Memory Type	Static Random Access-
Power Dissipation	1 μW/bit
Speed	$\tau_{access} < 10$ ns
Radiation Hardness	$> 10^6$ rad total dose
Storage Capacity	4096 bits/chip

The above requirements are very demanding. They represent a "speed power" product of < 10 fJ/bit.

In the previous GaAs static RAM development program, a low power RAM cell was designed and a 256 bit RAM was demonstrated. The final phase of the previous program provided an opportunity to begin processing 3-inch GaAs wafers. The implementation of the 3-inch wafer process was very successful.

In this report, the results from the first semester of a 21-month program designed to raise the complexity of the GaAs static RAM from 256 to 4K bits with the characteristics listed in Table 1-1 are discussed. In this

period, the characterization of the 256 bit RAM was completed, and a 1K RAM was designed. Process development work including improvements in the Cermet process for high value resistors is discussed in Section 2. The evaluation of the 256 bit RAM including a discussion on yield, performance, and radiation hardness is covered in Section 3. Finally, the design and predicted performance of the 1K RAM are discussed in Section 4.

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2.0 PROCESS DEVELOPMENT

During the past two quarters the main emphasis on RAM processing has been on Cermet resistors and device isolation. The final lots of RM3 wafers were completed during this time following equipment modifications for the Cermet resistor process. The resistor fabrication is now fairly well stabilized, with uniformity and resistivity parameters sufficiently controlled for 1K RAM designs. As to device isolation, work is continuing in identifying the near-surface conduction mechanism. Etching experiments have yielded results relating device isolation and EL2 distribution.

2.1 Cermet Resistor Process

Magnetron sputtering of Cermet films was initially intended to provide the uniformity as well as the correct sheet resistivity for 3-inch RAM wafers. Approximately half of the completed wafers do, in fact, have Cermet resistors deposited by magnetron sputtering, and have yielded fully functional 256 bit RAM arrays. One of the main problems associated with this technique, however, has been the lack of good uniformity of resistance values due primarily to contact problems of the Cermet to the second level metal lines. The differences between diode and magnetron sputtering appears to play a significant role in the adhesion of Cermet films, and as a result a new diode sputtering system was acquired and brought on-line specifically for Cermet processing. The new system is capable of utilizing three 8-inch sputtering targets, has a load lock system for high throughput, and is cryo-pumped for speed and cleanliness. By incorporating multiple targets with different ratios of Cr to SiO, a wide range of resistivities can be obtained. Table 2.1-1 shows resistor data obtained from several 3-inch RAM and test wafers. The resistor uniformity when using the new diode system is considerably better than that of the magnetron sputtered resistors, and at the same time can provide a wide range of resistivity values with relatively constant uniformity. As seen in Table 2.1-1, for example, the pull-down resistor varied from 7.9 MΩ to over 100 MΩ while uniformity values were maintained at approximately ± 10%.

Table 2.1-1
Cermet Resistance Data

Sample	System	Pull-down R	Pull-down σ	Pull-up R	Pull-up σ
RM3-131	Magnetron	80.3 MΩ	± 24%	48.0 MΩ	± 31%
RM3-134	Diode	67.7 MΩ	± 5%	30.8 MΩ	± 5%
RM3-1243	Diode	102.0 MΩ	± 10.2%	46.7 MΩ	± 10.3%
Test Wafer	Diode	7.9 MΩ	± 9.6%	3.8 MΩ	± 10.8%
Test Wafer	Diode	17.5 MΩ	± 8%	7.5 MΩ	± 9%

A check of the temperature coefficient of the resistance (TCR) was also done and compared to earlier data obtained with the magnetron system. For films with a bulk resistivity in the range of 80 - 100 Ω-cm, the TCR for the magnetron film was approximately 5000 ppm/°C while the corresponding value for the diode sputtered film is approximately 3000 ppm/°C. The diode films also exhibited less sensitivity to annealing conditions, and are thus more stable for post deposition processing.

The Cermet resistor process for the new 1K RAM mask set will follow that of previous RAM wafers; namely, sputter deposition of the Cermet film followed by ion milling for resistor definition. This process is identical to that of second level metal processing, and therefore, should be governed by the same yield limiting factors. The resistor pattern, however, is a very low density, and thus, factors such as resistor-to-resistor shorts should be non-existant when compared to the higher density second level metal lines. The Cermet resistivity value required for the RM4 mask set is 3.5 MΩ/□. Recent experiments utilizing the 80:20 wt% (SiO:Cr) target has shown that this value can be met, and thus Cermet processing for the 1K RAM design appears to be reasonably well stabilized.

2.2 Low Power RAM Isolation

Proton bombardment was employed on all wafers which yielded fully-functional RAM arrays, and work has continued in trying to identify the cause of

leakage currents when proton isolation is not used. The proposed model for the conduction mechanism has been based on the possibility of EL2 outdiffusing during the anneal, thus forming a p-type layer near the surface of the GaAs. Several workers[1,2] have reported on the outdiffusion of EL2, and in-house DLTS measurement have also indicated that EL2 outdiffuses to a certain extent. On the other hand, the possibility exists that contaminants which are on the surface of the GaAs prior to capping, are driven into the bulk material during anneal. Such contaminants might be carbon from wafer preparation, silicon from the capping process, or more likely, the existence of an excess arsenic layer on the surface of the GaAs.

A set of experiments was performed in an effort to investigate some of these possibilities. The first set was a series of arsenic implants intended to compensate for any outdiffusion of EL2. The result was that the leakage actually increased somewhat at the higher arsenic doses, and thus indicated that either EL2 was not outdiffusing, or that arsenic implantation was not a useful compensation technique. In another experiment, a test wafer was baked at 450°C prior to capping in an effort to drive any excess arsenic from the surface region. Isolation measurements showed no change in characteristics when compared to standard wafers. Thus, these tests as well as preliminary tests with p-type contacts were inconclusive in determining leakage mechanisms, and prompted further investigation into the substrate material itself.

The second set of experiments focused on etching through the dielectric material in a standard 3 mm isolation gap, and subsequent etching into the GaAs. The I-V characteristics of the gap were monitored as the etching proceeded. A typical I-V curve for an unetched isolation gap is shown in Fig. 2.2-1a. This characteristic, which was obtained following the Schottky metallization step, remained unchanged after removal of the SiO_2 and Si_3N_4 dielectric layers. However, as the GaAs was etched, an increase in the breakdown threshold voltage, which continued as the etch depth increased, was noted. A typical I-V result at a depth of 1300A is shown in Fig. 2.2-1b. A plot of threshold voltage vs etched depth is shown in Fig. 2.2-2. There appears to be two distinct regions which follow the relationship $V_B = Z^K$; where V_B is the breakdown voltage and Z is the etched depth. For etch depths less than ≈ 600A the exponent, K, is =

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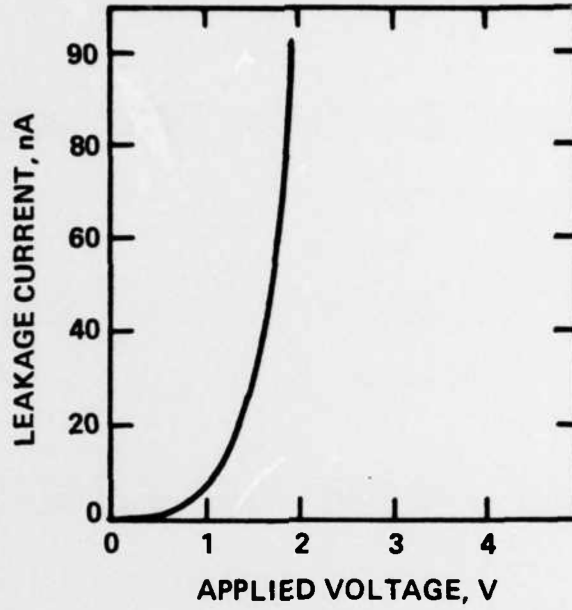
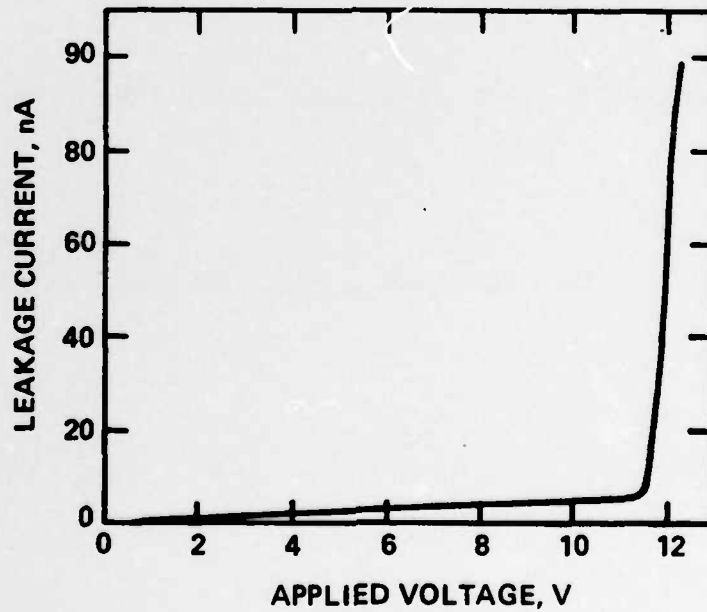


a) NO ETCHING



b) ETCH DEPTH = 1300Å

Fig. 2.2-1 Isolation characteristics showing the influence of GaAs etching.

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BREAKDOWN VOLTAGE (V)

50
40
30
20
10
9
8
7
6
5
4
3
2
1

100 200 500 1000 2000 3000

ETCH DEPTH (Å)

Fig. 2.2-2 3 μm isolation gap breakdown voltage as a function of etch depth into the GaAs.

0.53, while for depth greater than 600Å K = 1.9. This latter relationship agrees qualitatively with the EL2 trap distribution following anneal as reported in Ref. 1, where EL2 outdiffusion varies as Z^2. Thus, there appears to be a good correlation between the outdiffusion of EL2 and the breakdown voltage. The role of carbon and EL2 will be investigated in more detail in a third set of experiments currently under way. Wafers with different carbon and EL2 levels will be probed for isolation characteristics, and etching experiments will continue to be carried out in an effort to further characterize bulk parameters.

In addition to the isolation measurements which were made while etching the GaAs surface layer, a study of backgating effects was also performed. Fig. 2.2-3a shows a typical characteristic for a sample etched ≈ 1200Å. As the back-gate voltage, V_{BG}, is made more negative, the saturated source-drain current drops dramatically after reaching a certain threshold voltage. This threshold voltage can be shifted to higher negative values by continued substrate etching as shown in Fig. 2.2-3b. Thus, the relationship between substrate isolation and backgating effects holds true for etched samples in much the same manner as for proton isolated samples.

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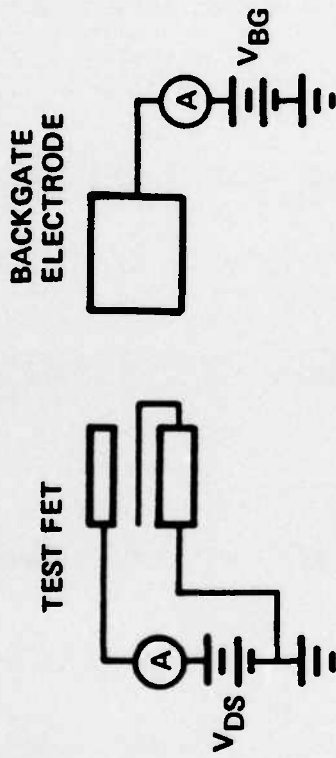
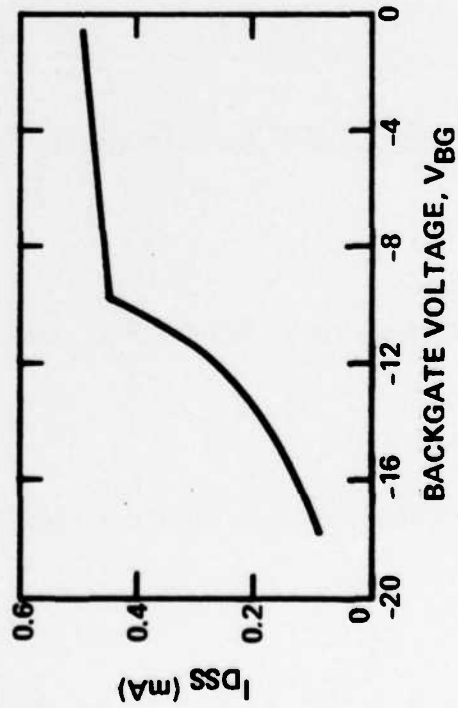
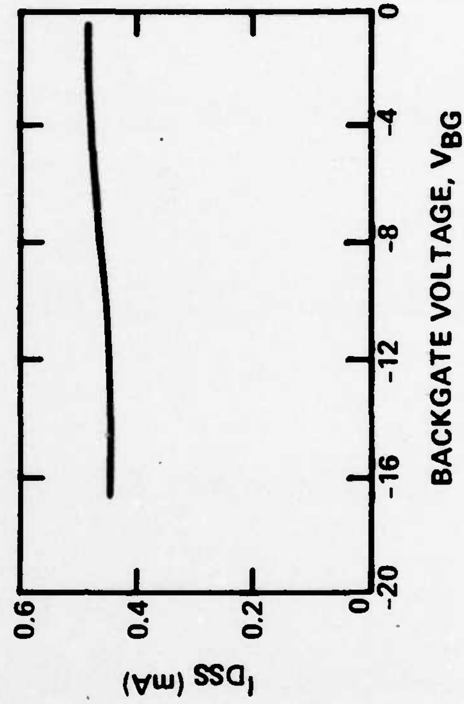




a) ETCH DEPTH = 1200Å



b) ETCH DEPTH = 2000Å

Fig. 2.2-3 Dependence of backgate threshold voltage on GaAs etch depth.

3.0 256-BIT RAM EVALUATION

The 256-bit RAMs discussed in this report were fabricated with mask set RM3. This is a slightly modified version of a previous mask set, RM2. The main changes were related to die organization and alignment marks for processing with a 10 X wafer stepper on 3-inch wafers. This was the first mask set on which the processing of 3-inch GaAs wafers was attempted. Mask sets RM3 contains a number of different versions of the 256-bit RAM, some with and some without peripheral circuits, plus a number of test structures consisting of portions of the peripheral circuits and single cells which had been extracted from the rest of the circuit for analysis. Most of the testing was concentrated on RAMs with peripheral circuits, and on the design version which provided the best chances of success following indications from measurements on test cells.

On mask set RM3, the design of the RAM cell was much more advanced than the design of the peripheral circuits. The design of the RAM cell had already undergone one iteration following extensive characterization. The peripheral circuits instead, were designed for the first time and just as a vehicle to address the memory array. No attempt had been made to attain low power dissipation in the peripheral circuits. This explains the apparent contradiction of having very low power memory cells controlled by relatively high power peripheral circuits. In the next iteration which is discussed in Section 4.0, the peripheral circuits have been redesigned so that their power dissipation is commensurate with the power dissipation of the memory cell array.

3.1 Review of the 256-Bit RAM Design

A photograph of the 256-bit GaAs static RAM is shown in Fig. 3.1-1. This memory chip was built using normally on MESFET devices, having a low threshold voltage, typically on the order of ≈ -0.5 V. A schematic of the cell is shown in Fig. 3.1-2. The cell consists of a pair of cross-coupled transistors. Since these are normally-on devices, level shifting is required, and it is provided by two forward bias diodes in each cross connection of the cell, and by connections of the FET gates to a negative power supply through pull-down resistors. The read operation is performed by an additional transistor larger

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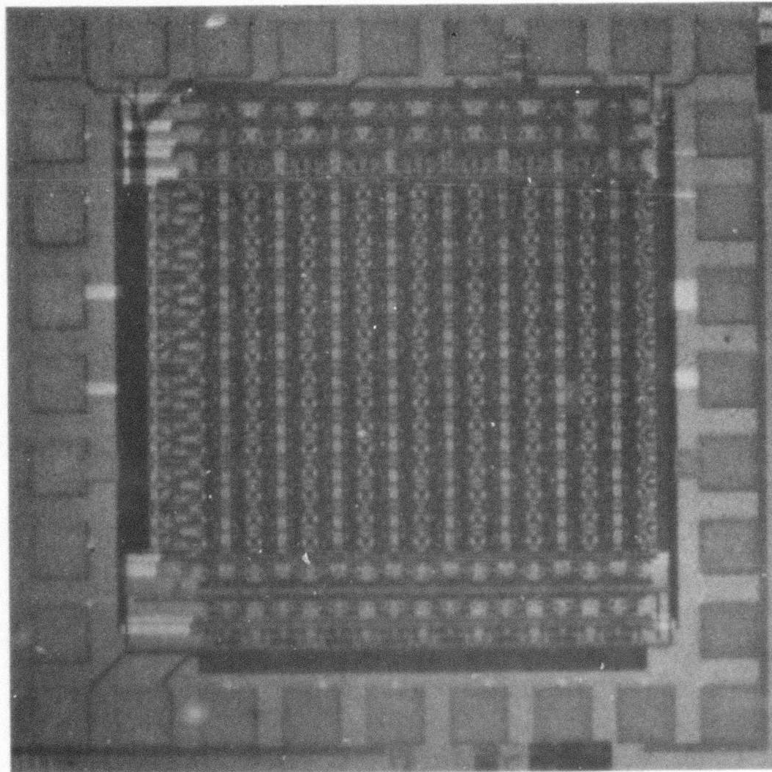

1.3 x 1.3 mm

Fig. 3.1-1 Photograph of a GaAs 256-bit static RAM.

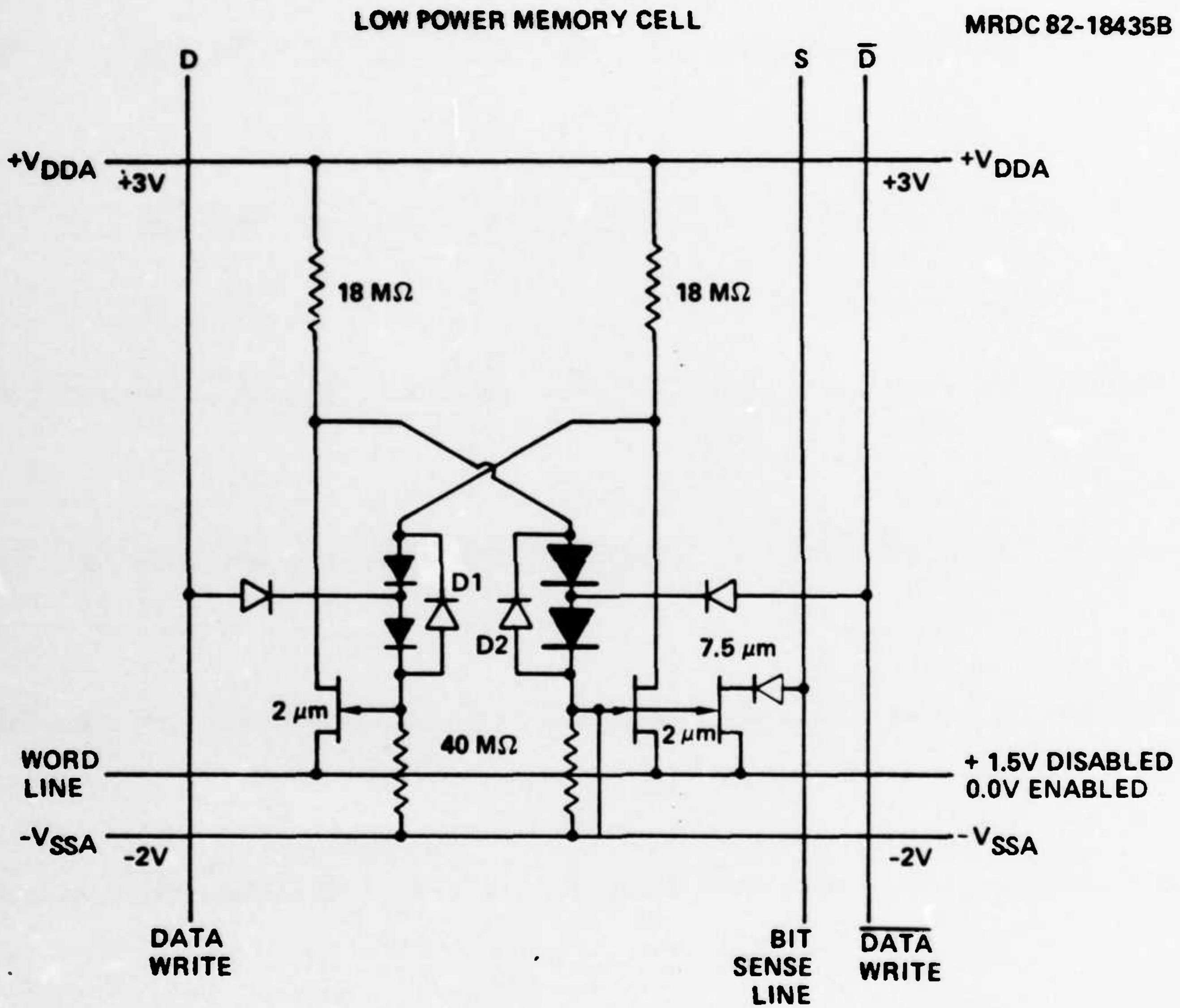

Fig. 3.1-2 Schematic of the cell used in the 256-bit GaAs static RAM.

than the latch transistor. When the word line is disabled this relatively large transistor consumes no power because its drain-to-source voltage is not sufficient to support any current. This transistor becomes active only when the word line is enabled when its voltage drops to 0 V. This scheme provides sufficient speed to meet the access time requirement, while allowing the two transistors in the cell to be very small, 2 μm wide. These transistors must be small to keep their current density as high as possible, and so reduce the effect of the subthreshold currents. A photograph of the cell is shown in Fig. 3.1-3. The dimensions are 51 × 39 microns.

A schematic of the peripheral circuit used with the 256-bit RAM is shown in Fig. 3.1-4. This is a fairly conventional circuit. The row and column address decoders require both the address and its complement. The complement could have been generated on chip by simple inverters, but then line drivers should have been provided. To simplify the design as much as possible, both the address and its complement were required as inputs.

The decoder circuit for the columns and rows are different from one another. The column decoder uses a NOR gate, while the row decoder makes use of a NAND operation performed by an SD^2FL gate having a complemented driver. This is a more advanced and a better power saving scheme than the one used for the column decoder. It was used only for the row decoder because it was experimental at the time it was designed. This design has been adopted for the 1K RAM (see Section 4.2).

Source follower drivers were used extensively in this design. They have excellent drive capability, but they consume too much power because they are always on. For this reason, they were replaced by complementary drivers in the design of the 1K RAM. Although complementary drivers are not as fast as source followers, they were adopted as a good tradeoff between speed and power dissipation.

3.2 Yield of 256-Bit RAMs

The functionality of the 256-bit static RAMs was tested using a lab microcomputer equipped with analog and digital outputs and inputs. The

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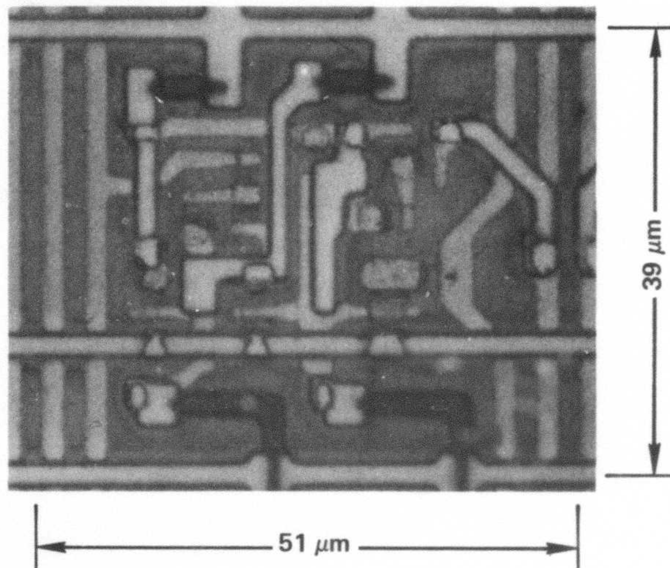


STANDBY POWER DISSIPATION	4 μW/BIT
ADDRESS ACCESS TIME	5.5 ns

Fig. 3.1-3 Photograph of a cell in the 256-bit GaAs static RAM.

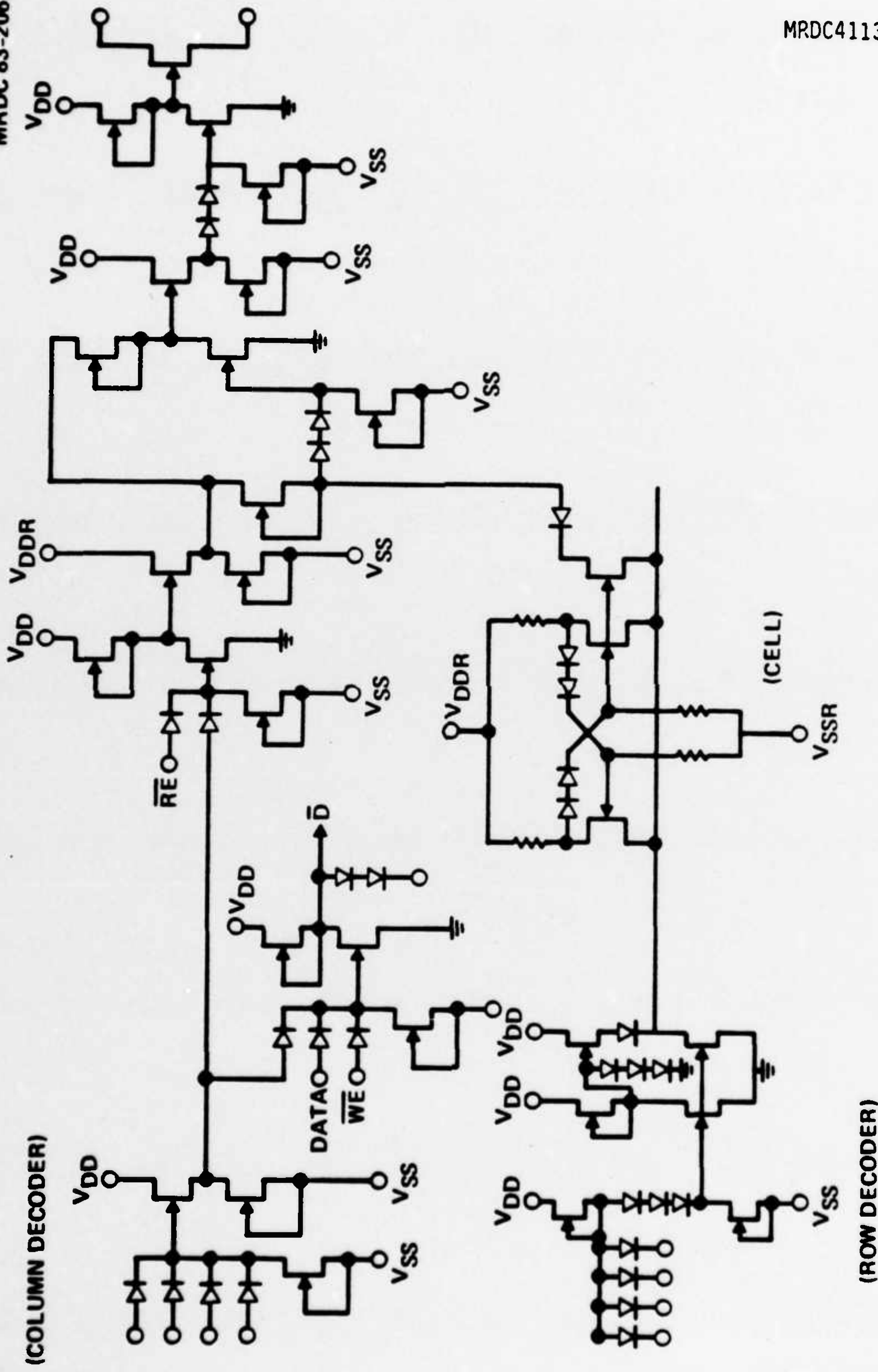


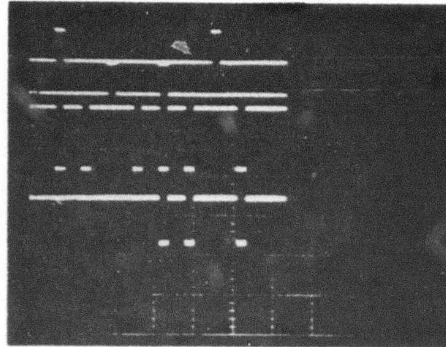
Fig. 3.1-4 Peripheral circuits for the 256-bit static RAM.

functionality tests were conducted at low speeds, limited by the lab microcomputer which was controlling the measurement. The test pattern used is illustrated in Fig. 3.2-1. The test procedure consists of write enabling one cell, writing a "one" in it, and disabling it. A "zero" is then written in a neighboring cell. After this is done, the original cell is enabled and read back to verify whether it held the "one" without being disturbed by the write operation in the neighboring cell. The process is then repeated writing a "zero" in the cell and a "one" in its neighbor. A cell was considered functional only if it passed both tests. In practice, this test pattern resembles very much a "walking one," and a "walking zero" pattern.

The yield of functional 256-bit static RAMs was measured on wafer. The results are summarized in Table 3.2-1 along with the average and standard deviation of threshold voltage for each wafer. The number of totally functional 256-bit RAMs is low. However, this yield is affected by the rather marginal operation of the peripheral circuits whose sensitivity to backgating was underestimated. Note the large number of failures in the range of 15 to 100. This number is larger than the number of failure for over 100 cells for most of the wafers. This anomaly is due to the large number of failures caused by the peripheral circuits, which occur by multiples of 16 cells, since the memory is arranged by a 16 × 16 array.

Table 3.2-1
Yield of 256-Bit Static RAMs

Wafer Number	Number of Cell Failures 0	1	2	3-14	15-100	>100	Testable Chips	Threshold Voltage Volts
51				2	5	10	8%	-0.71 ± 0.12
52	4	5	2	6	41	39	44%	-0.65 ± 0.11
54						11	5%	-0.67 ± 0.17
62	8	7	3	8	47	27	45%	-0.67 ± 0.12
63	1			7	24	6	17%	-0.74 ± 0.19
72			1		45	72	54%	-0.27 ± 0.10
101	2	5	8	12	62	12	84%	-0.48 ± 0.07



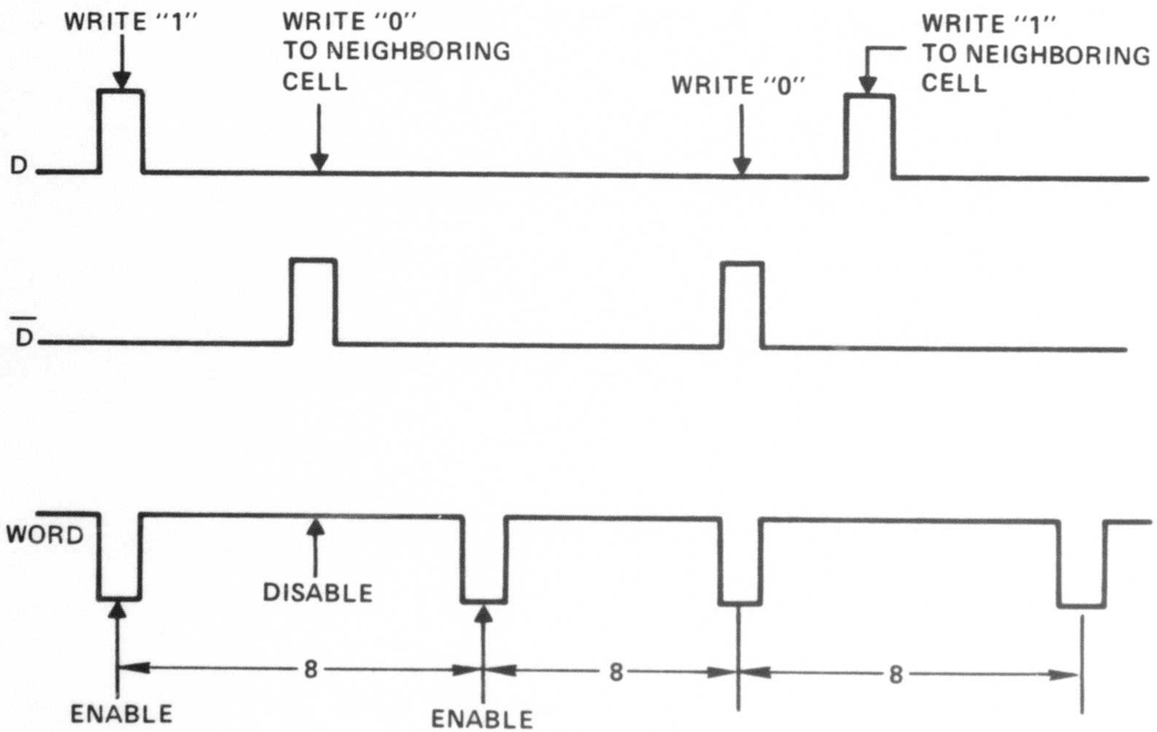


Fig. 3.2-1 Pattern used for testing the functionality of 256-bit static RAMs.

The column labeled testable chips in Table 3.2-1 indicate the percentage of chips which had no obvious failure, and on which it was worth conducting a functionality test. This column indicates a very large number of rejections. Mask set RM3, on which these RAMs were fabricated, was the first mask set used with a wafer stepper to process 3-inch GaAs wafers. The large number of losses was due to failures in the alignment, most of the time gross failures caused by lack of experience with the design of alignment marks. This problem has been corrected in subsequent mask sets.

In conclusion, the functionality tests show that the low power RAM cell can be successfully implemented into a RAM. Significant improvements in yield are expected from the next mask set on which the design of the peripheral circuits has been greatly improved. Several improvements in cell design to make them less sensitive to leakage should also be beneficial.

3.3 Access Time Measurements on 256-Bit RAMs

The access time was measured on individual cells at random, due to lack of instrumentation capable of automatically testing GaAs high speed RAMs at full speed. The methodology and the result of a read access time measurement is illustrated in Fig. 3.3-1. As shown on the top portion of this figure, the output is monitored continuously, and to do so the "read enable" line is constantly enabled. All the address lines are kept unchanged except for one bit which is toggled back and forth. At the start of a cycle, when the address is changed, the "write enable" line is turned on, and a "zero" is written in the cell, as confirmed by the output signal. The "write enable" line is then turned off, and the address is changed. When the address changes, the output also changes because a different cell is being read. Finally, the address is changed back to the original one, and the output follows the change of address displaying the zero that was stored in the cell. The access time is measured between the midpoint of the transition of the address and the midpoint of the transistion of the output. These two waveforms are displayed on an expanded scale on the lower part of Fig. 3.3-1. This example corresponds to a typical measurement which yields a read access time of 5.5 ns. Access times as low as 1 ns have been observed.

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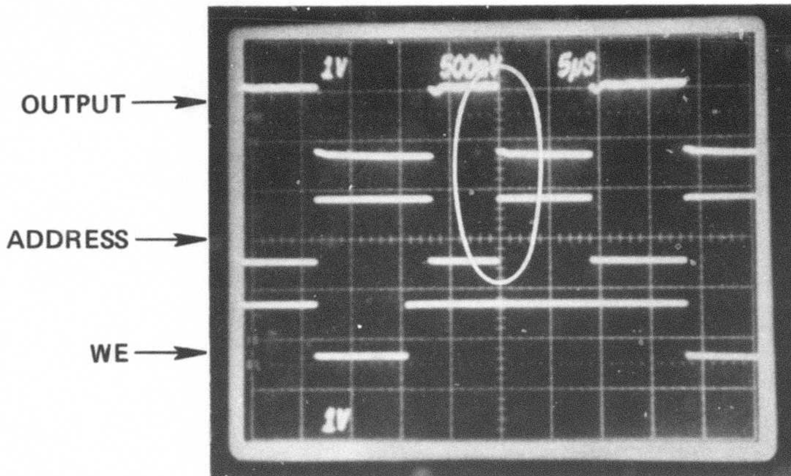

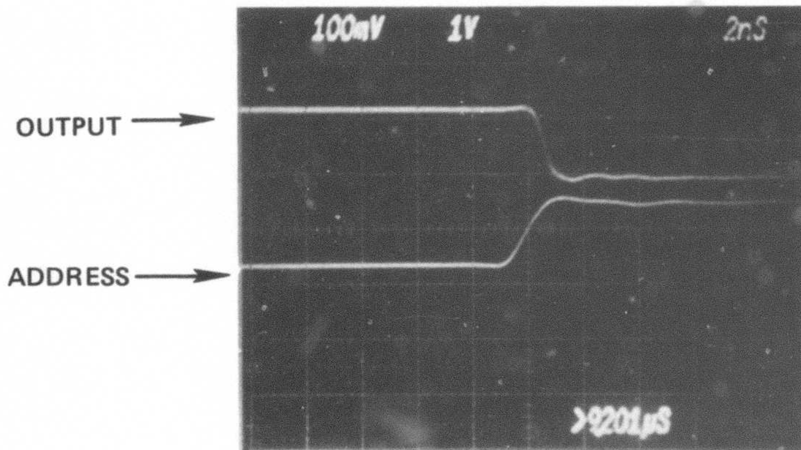

$\tau \simeq 1.0$ ns

Fig. 3.3-1 Read access time for the 256-bit static RAM.

As to the write operation, an important parameter is the minimum width of the write pulse required for the cell to store a bit. A "write" pulse width measurement is illustrated in Fig. 3.3-2. As with the access time measurement, the output is monitored continuously with the "read enable" line permanently on. The address is kept unchanged while the data input is switched periodically between "one" and "zero". The write enable line is turned on for a very short time in the second half of the data input cycle. As shown by the top trace in Fig. 3.3-2 the output changes whenever this "write enable" pulse is turned on showing that the pulse length is sufficient for the input data to be acquired by the cell. The experiment consists of shortening this write enable pulse, and determining at what length it becomes too short for the cell to latch in the new data. In this measurement the pulse was shortened to the minimum length allowed by the test equipment, 2 ns, without observing failures.

The result from the high speed measurements on the 256-bit RAM indicate that this chip is indeed capable of operating at high speed. This should not be surprising because the peripheral circuits used in this 256-bit version consume rather high power, and therefore they should be expected to operate at high speed. More significant is the observation that the low power RAM cell is indeed capable of operating at high speed. In particular, the ability of the cell to store a "one" or a "zero" with a very short (2ns) "write" pulse is very important, because it leaves 8 ns to the peripheral circuit for all the rest of the write operation. As a new low power version of the peripheral circuits was being designed (see Section 4.2) great effort had to be made to maintain the short access time while drastically lowering power consumption.

3.4 Radiation Experiment

Experiments were conducted to obtain preliminary information on the tolerance of the RAM cell to gamma radiation (total dose). Wafer No. 51 on Table 3.2-1 was exposed to a total gamma dose of 10^7 rads. Test device statistics and memory failure were evaluated before and after the irradiation.

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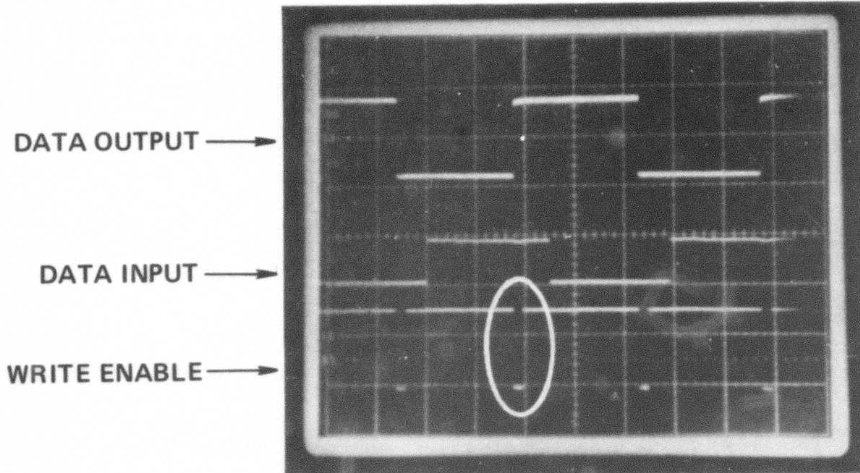

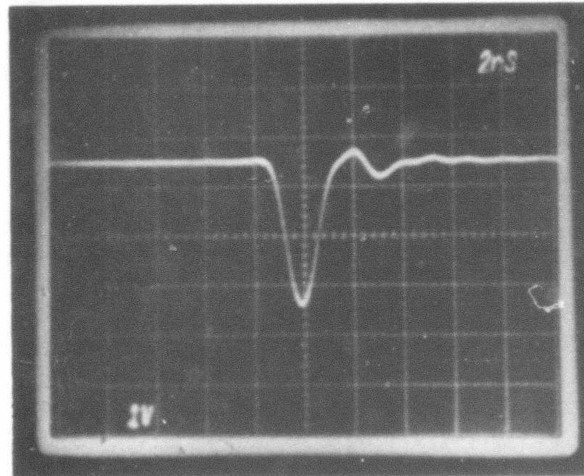

WRITE PULSE WIDTH < 2 ns

Fig. 3.3-2 Minimum "write" pulse width for the 256-bit static RAM.

The data in Table 3.4-1 represents statistical parameters of test FETs and diodes before and after irradiation. The statistical parameters were obtained from 396 FETs and 396 diodes in test cells distributed uniformly over the 3-inch diameter wafer. The data were acquired and analyzed by an automatic test system. The main conclusion from Table 3.4-1 is that the device characteristics experience no significant change after irradiation. This applies to the FET threshold voltage, -VP, saturation current, IDSS, saturation voltage, VSAT, etc. and to the diode ideality factor, NF, barrier height, VB, and series resistance, RS. The reverse saturation current of the diode, ISAT, shows a large change. However, I_{sat} is a very sensitive fitting parameter obtained from the forward characteristic of the diode. The diode characteristics are virtually unchanged as shown by the voltage corresponding to a current of 0.15 mA shown at the bottom of the diode tables.

The data in Table 3.4-2 show counts of cell failures before and after irradiation. As indicated in Table 3.2-1 this particular wafer had no fully functional RAMs. A rather surprising observation from the table is that the number of failures in each one of the chips tested tended to decrease rather than increase after irradiation. This is attributed to the rather marginal threshold voltage of the FET devices on this wafer. Therefore, even the very small shift shown in Table 3.4-2 (from 0.712 V - 0.696 V average) could help improving the yield of good cells.

The conclusions from this preliminary experiment is that no significant change is caused by a 10^7 rad gamma dose. More extensive experiments will be carried out on fully functional RAMs under bias. Total dose experiments on logic GaAs circuits done with and without bias have not shown any significant difference in the past. However, this will need to be verified on the low power RAM.

Table 3.4-1
Effect of a 10^7 Rad Gamma Dose on Device Statistics

	FET					Diode				
	Parameter	Unit	Average	SD	%	Parameter	Unit	Average	SD	%
	-VP	V	0.712	0.1110	15.5	ISAT	AMPS	7.0E-11	1.1427E-09	1630.8
	RS	OHMS	42.33	9.978	23.6	NF		1.106	0.212	19.2
	K	MMHO/V	5.614	0.799	14.2	RS	OHMS	462.1	142.7	30.9
					15.9	VB	V	0.902	0.083	9.2
Before 10^7 Rad	IDSS	MA	2.178	0.4151	19.1	VO.15MA	V	0.7[illegible]6	0.052	6.5
Radiaton	GD	MMHO	0.136	0.023	16.8					
	RON	OHMS	268.7	54.38	20.2					
	VSAT	V	0.949	0.083	8.7					
	IG	NA	44.57	497.3	1115.7					
	-VP	V	0.696	0.103	14.9	ISAT	AMPS	4.2830E-11	1468.5	
	RS	OHMS	41.67	8.782	21.1	NF		1.092	0.165	15.1
	K	MMHO/V	5.688	0.744	13.1	RS	OHMS	468.2	123.3	26.3
					15.2	VB	V	0.911	0.062	6.8
After 10^7 Rad	IDSS	MA	2.121	0.394	18.6	VO.15MA	V	0.798	0.042	5.2
Radiation	GD	MMHO	0.134	0.022	16.4					
	RON	OHMS	295.0	56.91	19.3					
	VSAT	V	1.001	0.081	8.1					
	IG	NA	92.60	763.5	824.5					

Table 3.4-2

Number of Failures in 256-Bit Static RAMs Before and After Gamma Irradiation with a 10^7 Rad Dose.

Chip #	Before	After
1	41	16
2	8	4
3	14	3
4	85	38
5	91	63
6	256	245
7	194	78
8	198	120
10	79	50

4.0 1K RAM DESIGN

Based on the experience from the 256-bit RAM (see Section 3.0), a new mask set (RM4) has been designed. The principal element on this mask set is a 1K static RAM. The cell design and layout used in the 256-bit RAM has been maintained based on the good results obtained. Only minor changes were made to make the cell more tolerant to leakage current. These changes are discussed in Section 4.1. The peripheral circuits were totally redesigned. An effort was made to design and lay out the peripheral circuits so that they can be used in a 4K RAM without major changes. Power dissipation was carefully trimmed while maintaining speeds compatible with the requirements of the program. A power switch was included to cut down power consumption when the chip is not addressed. This design of the peripheral circuits is discussed in Section 4.2.

The new mask set contains two almost identical versions of the 1K RAM (they differ only in the design and layout of the capacitors within the cell), and also a number of 256-bit RAMs. All the 256-bit RAMs are similar to the 1K RAM. The differences between versions lie on subtle changes in cell design for experimental purpose. The 256-bit RAM was chosen for this experimentation because it uses less wafer area. Test cells containing separate components of the peripheral circuits and individual RAM cells with all the identical nodes accessible to probes, are also included on the mask set, as well as small test areas for parametric characterization of devices and components.

The power switch was incorporated in all the designs. Its output is connected to a contact pad, which can be used to either monitor the operation of the switch or to override it with an external voltage.

4.1 RAM Cell Design

A schematic of the cell for the 1K RAM is shown in Fig. 4.1-1. When this schematic is compared with Fig. 3.1-2 which corresponds to the current 256-bit RAM, it becomes obvious that only minor changes were made. These changes consist of a) lowering the values of the pull-up and pull-down resistors;

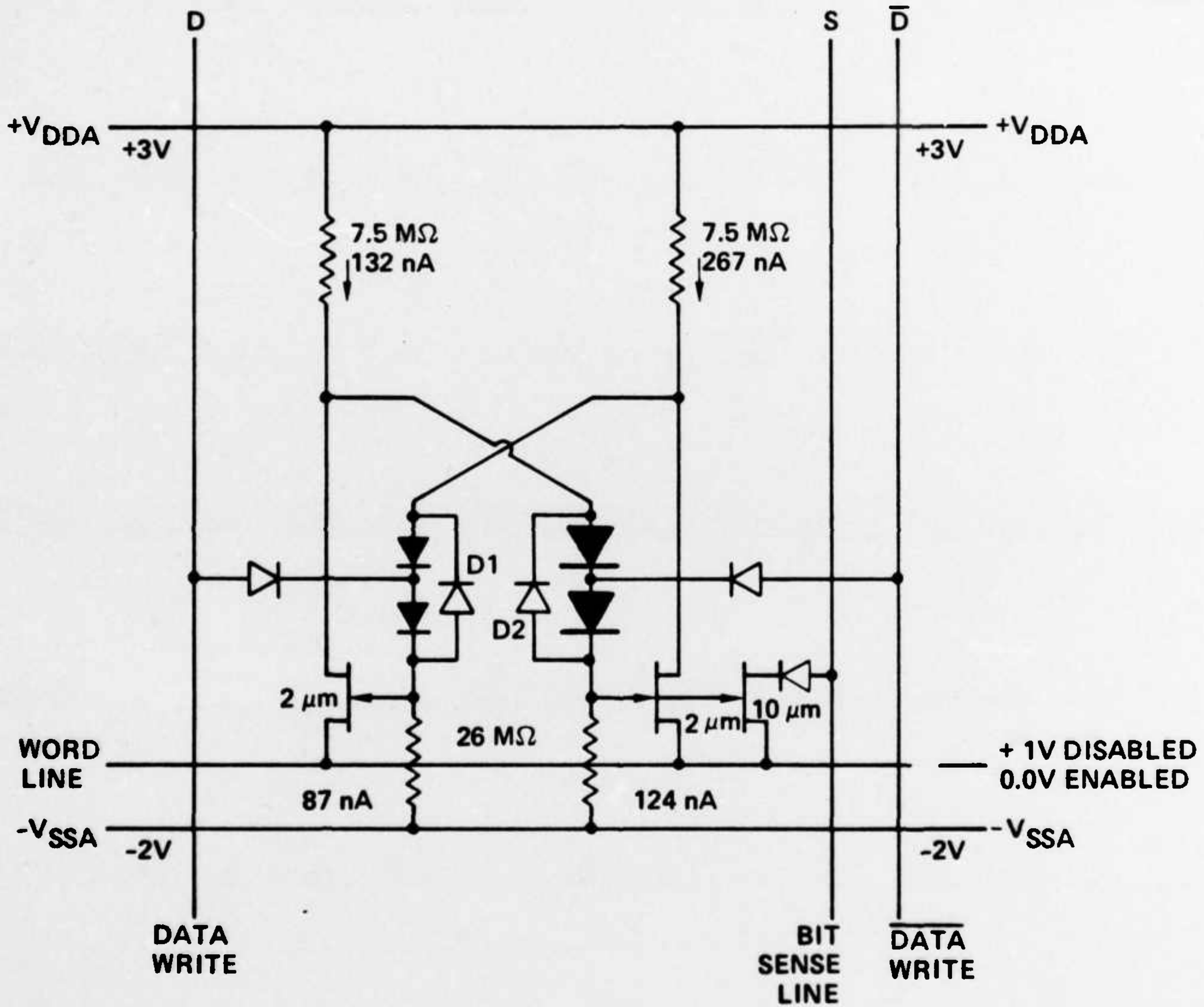

Fig. 4.1-1 Schematic of the cell for the 1K GaAs static RAM.

b) lowering the supply voltage values from +5 and -3 V to +3 and -2 V, c) lowering the voltage swing on the word line from 0 to 1.5 V down to 0 to 1 V; d) increasing the width of the output transistor from 7.5 to 10 μm. All these changes, except for the last one, were done with the purpose of lowering the voltage margins and increasing the current levels in order to reduce the sensitivity of the cell to leakage currents. By lowering bias voltages where currents were increased, it was possible to maintain the low power dissipation of the cell. As indicated in the estimate at the bottom of Fig. 4.1-1, the power dissipation per bit is 1.6 μW. The increased width of the output transistor from 7.5 to 10 μm is required because the bit sense line is longer on the 1K RAM than it is on the 256-bit RAM.

In summary, the changes made represent only minor deviations from the original design. The layout of the cell has remained virtually unchanged, except for minor adjustments to increase the distance between neighboring elements wherever the possibility of leakage was suspected. As a result of these layout changes the size of the cell was increased slightly from 51 × 39 μm to 54 × 43 μm. This design is rather conservative, and there is room for some size reduction at a later stage.

4.2 Peripheral Circuit Design

The organization of the 1K GaAs static RAM is shown on the block diagram in Fig. 4.2-1. From a system standpoint, this is a 1K × 1 RAM. The cells are arranged in a 16 × 64 array. A rectangular rather than square array was chosen because the row control circuits have a much lower power dissipation than the column control circuits. This is just one example of the tradeoff of power for speed done in this design.

The overall organization of the peripheral circuits is straightforward. Row and column address circuits receive the input addresses, generate true and complement values of these addresses, and drive the relatively long lines going to the row or column decoders. The row or column decoders (one per row and one per column) decode the address and control the corresponding row or column. The data write and read operations are also fairly conventional. The read operation

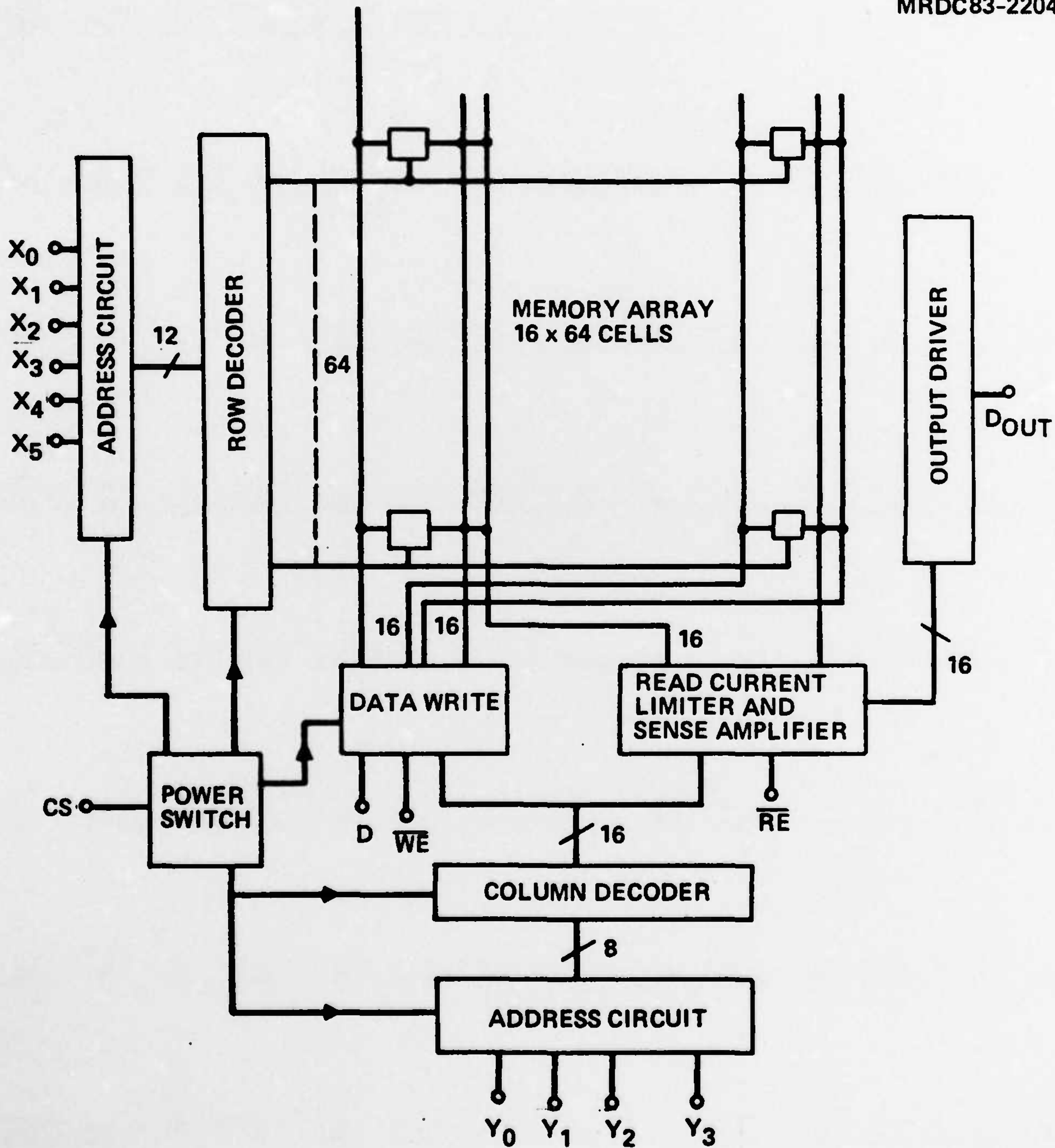

Fig. 4.2-1 Organization of the 1K GaAs static RAM.

is done without using a differential amplifier because it did not appear to be necessary in the 256-bit RAM.

As shown in Fig. 4.2-1 the power switch controls the positive supply voltage to most of the peripheral circuits. It does not perform an indiscriminate power down because a few transistors need to be left on. However, the amount of power dissipation left is minimal. A schematic of the power switch is shown in Fig. 4.2-2. It is a simple design where a switching transistor turns on or off the V_{CS} output. In order to be able to turn off the switching transistor, the gate is pulled down by the negative supply of the memory array.

As an example of the design of the peripheral circuits, Fig. 4.2-3, shows the schematic of the address circuit used for both the rows and the columns of the array. This circuit, one for each address bit, must be capable of generating the true address, B_0, and its complement, $\overline{B}_0$ with sufficient drive capability to drive the address line running all along the side of the array. The key components to achieve such drive capability with moderate power dissipation are complementary (push-pull) drivers, which resemble regular inverters, but have the active load pullup replaced by an active FET. In the circuit shown in Fig. 4.2-3, the true and complement values which are being generated are also used to drive the active pull-ups of the push-pull drivers so that the total number of components is kept to a minimum. In this circuit all the positive bias voltages are controlled by the power switch.

Although the complementary driver is very useful for saving power, and it is the only possible choice given the power requirements of this project, it is not ideal in terms of switching time. This is illustrated by the output of the SPICE simulation of this address circuit shown in Fig. 4.2-4 where the top trace represents the input to the address circuit, and the bottom traces represent the true and complement output of the address circuit. It is clear that the B_0 and $\overline{B}_0$ output are not completely symmetric. The rise time of the $\overline{B}_0$ is longer than the rise time of B_0 output. However, an overall acceptable compromise has been reached, with an address time of 1.6 ns which is within the time budget allocated to the address circuit. Similar power speed tradeoffs were

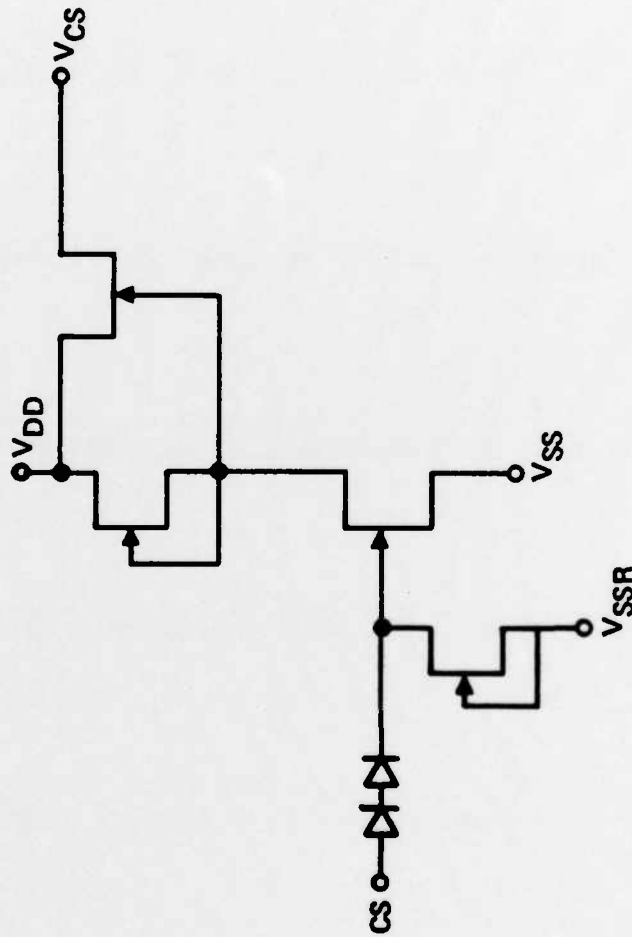

Fig. 4.2-2 Schematic of the power switch for the 1K GaAs static RAM.

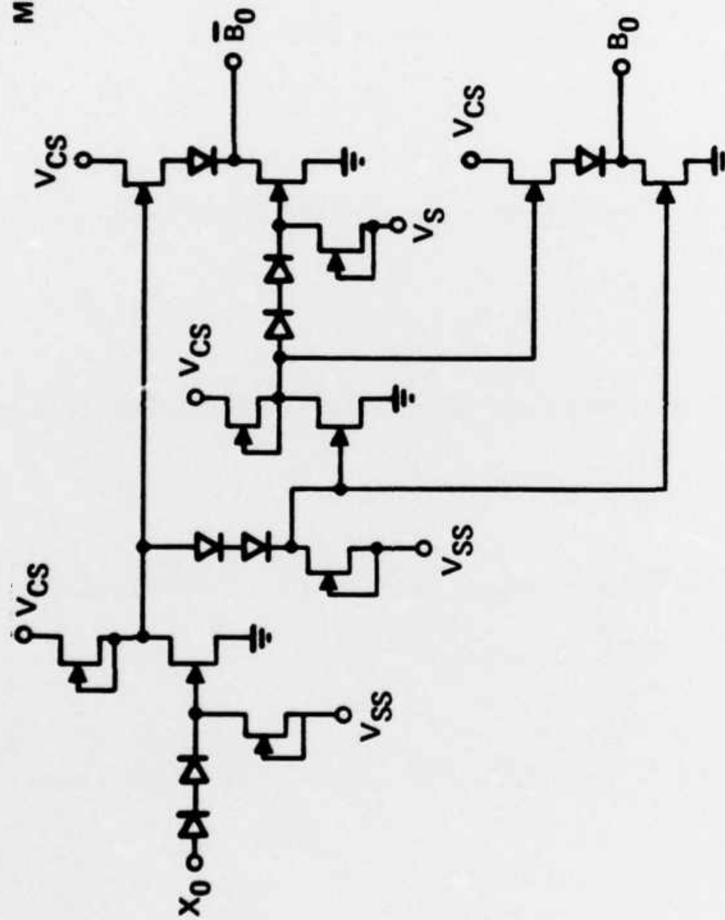

Fig. 4.2-3 Schematic of the address circuit for the 1K GaAs static RAM.

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Fig. 4.2-4 Results from a SPICE simulation of the address circuit.

made for every circuit in order to minimize power dissipation while still maintaining an acceptable speed.

The overall results of this design in terms of speed are summarized in Figs. 4.2-5 and 4.2-6 which show the timing diagrams for the "read" and "write" operations of the 1K RAM, respectively. The times indicated on these diagrams were determined by simulation. As shown in the diagrams, the read operation is performed in 5.5 ns, and the write operation takes place in 4.8 ns. This is better than the 10 ns allowed for the 4K RAM but a margin was left intentionally because the longer lines in the 4K RAM will increase the delay of some of the "read" and "write" operations. By allowing a margin on the 1K design it is possible to meet the 10 ns requirements on the 4K RAM without any major redesign of the circuits.

A detailed analysis of the power dissipation predicted for the 1K RAM is presented in Table 4.2-1. Here each component of the peripheral circuit is listed along with its power dissipation calculated with the chip selected (when the power switch is on) and deselected. The power dissipation of the memory array is based on the 1.6 μW/cell estimated on Fig. 4.1-1. The power switch causes a small addition to the total power consumption. The total power dissipation is 49 mW when the chip is selected, and 9.6 mW when the chip is deselected. If this total power dissipation is divided by 1K to calculate the average power dissipation, the corresponding figures are 47.6 μW/bit when the chip is selected and 9.3 μW/bit when the chip is deselected.

The power dissipation figures estimated do not meet the 1 μW/bit program requirement. However, some improvement will occur with the 4K design simply due to the more favorable ratio between the number of peripheral circuit components and the number of memory cells as the memory becomes larger. When this happens the number of peripheral circuits increases only with the square root of the number of memory cells. Therefore, a 4K static RAM, which has 4 times the number of memory cells of a 1K RAM, has only 2 times the number of peripheral circuit components of the 1K RAM.

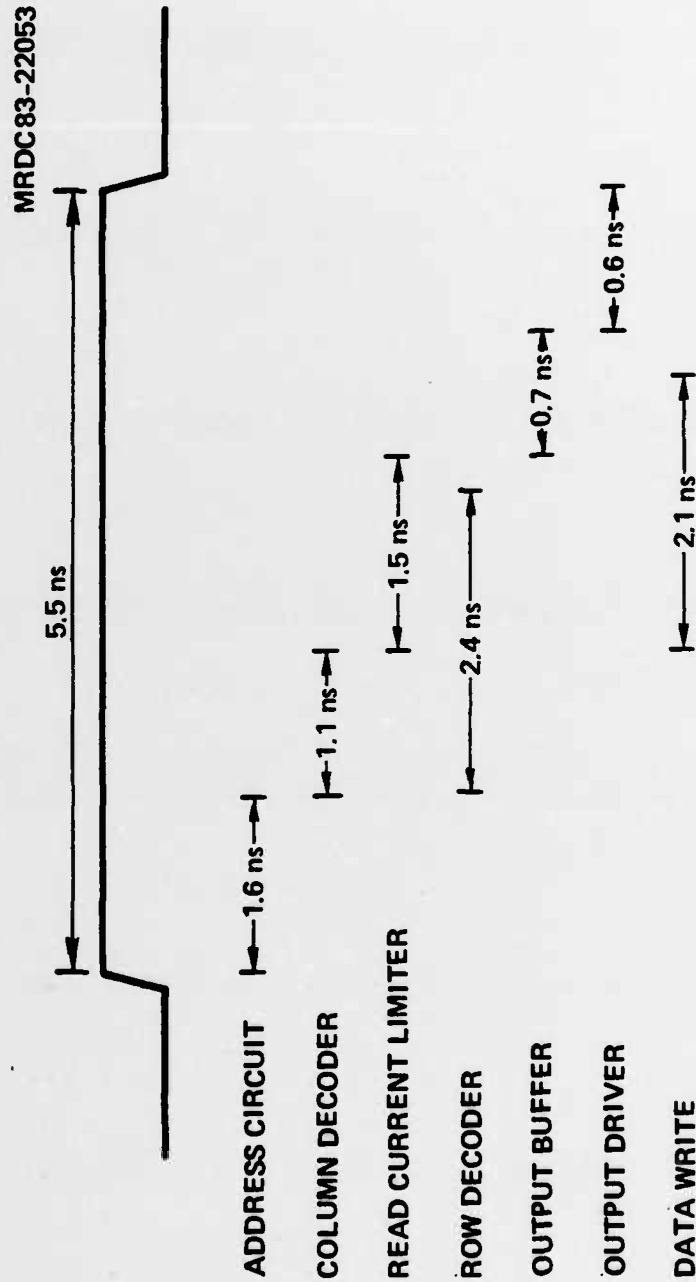

Fig. 4.2-5 Timing diagram for the read operation on the 1K GaAs static RAM.

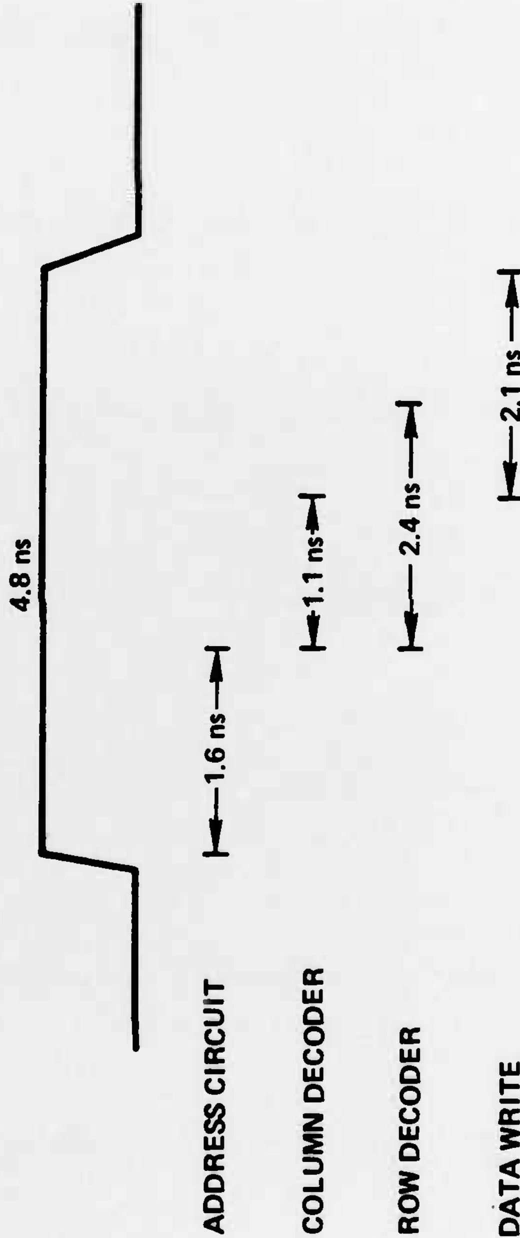

Fig. 4.2-6 Timing diagram for the write operation on the 1K GaAs static RAM.

Table 4.2-1

Estimated Power Dissipation for the 1K GaAs Static RAM

	Chip Selected			Chip Deselected
	Addressed	Not Addressed		
Address Circuit	1.66 mW × 10		16.60 mW	0.20 mW
Column Decoder	0.16 mW × 1	0.24 mW × 15	3.70 mW	2.00 mW
Read Current Limiter	0.44 mW × 1	0.16 mW × 15	2.90 mW	2.50 mW
Row Decoder	0.20 mW × 1	0.25 mW × 63	15.90 mW	0.40 mW
Data Write	0.51 mW × 1	0.44 mW × 15	7.10 mW	0.40 mW
Output Circuit	0.97 mW		0.97 mW	0.97 mW
Memory Array 1024 × 1.6 μW			1.60 mW	1.60 mW
Power Switch			0.02 mW	1.50 mW
Total Power Consumption			48.80 mW	9.57 mW
Power per Bit			47.60 μW	9.34 μW

In Table 4.2-2 some projections for the power dissipation and access time of a 4K RAM are presented. These projection are based on the assumption that no change is made in the memory cell and the peripheral circuits used for the 1K design. As shown on the lower lines, the access times are 11 ns for the "read" operation and 9.6 for the "write" operation. The power dissipation is 100 mW when the chip is selected, and 20 mW when the chip is deselected. When these numbers are divided by 4K, the size of the array, the power dissipation per bit becomes 24.4 μWt/bit when the chip is selected, and 4.8 μW/bit when the chip is deselected.

In summary, with the new design a major step was taken toward reaching the goals of the program. Once data from this design are obtained, further adjustment to the power dissipation will be possible.

Table 4.2-2

Projections on Power Dissipation and Access Time for a 4K GaAs Static RAM

	Chip Selected	Chip Deselected
Peripheral Circuit	93.4 mW	13.3 mW
Memory Array	6.5 mW	6.5 mW
Total Power	99.9 mW	20.0 mW
Power/Bit	24.4 μW	4.8 μW
Read Access Time	11.0 ns	
Write Access Time	9.6 ns	

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