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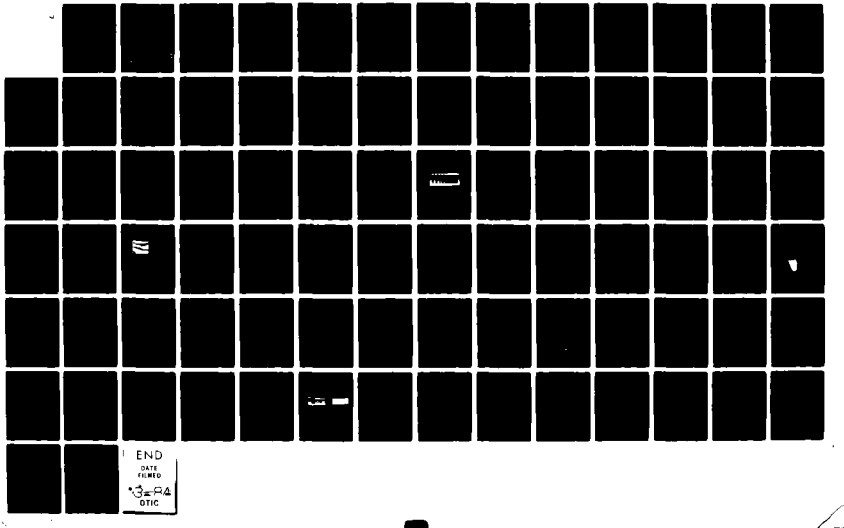

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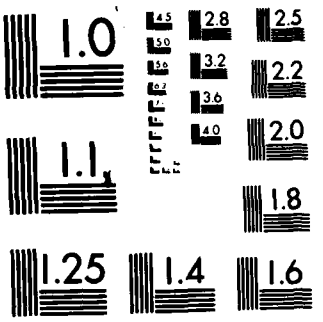

COMPUTER MODELING OF COMPLETE IC FABRICATION PROCESS

Final Report

by

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20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

Process and device modeling, especially in two-dimensions, for the complete IC fabrication process is reported. New understanding of oxidation and diffusion effects in silicon are reported and new computer tools and techniques are discussed. Device simulation is coupled to process modeling and new results for both short- and narrow-channel devices are reported. Non-planar device simulators, both poisson and two-carrier capabilities, have been developed. New techniques have been developed for parameter extraction and measurements.

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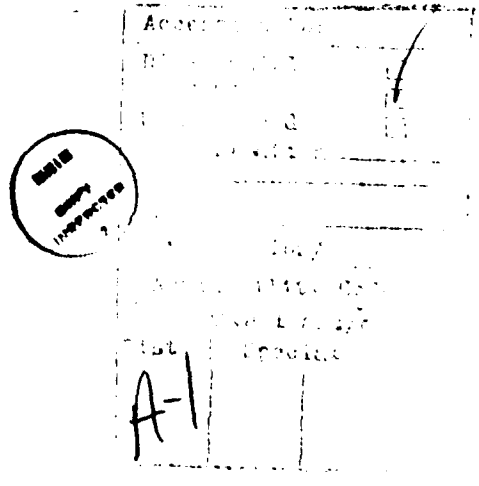
Abstract

Process and device modeling, especially in two-dimensions, for the complete IC fabrication process is reported. New understanding of oxidation and diffusion effects in silicon are reported and new computer tools and techniques are discussed. Device simulation is coupled to process modeling and new results for both short- and narrow-channel devices are reported. Non-planar device simulators, both poisson and two-carrier capabilities, have been developed. New techniques have been developed for parameter extraction and measurements.



1. Introduction

This research effort has addressed computer modeling of the complete IC fabrication process. At the beginning of this contract period the SUPREM II process simulator was coming into widespread industrial use. As a result of the present activities a complete set of two-dimensional process and device modeling tools has been developed and distributed. Applications of these tools include both fundamental studies of impurity diffusion and oxidation phenomena in two dimensions as well as device studies for scaled MOSFET technologies. A total of seven new PhD's have graduated under sponsorship of this contract as well as three Masters degrees have been granted. In the following sections specific proposed tasks and research accomplishments of this program are discussed. The discussion will be focused in two areas--fundamentals of technology modeling and tools to couple process and device modeling.

2. Fundamentals of Technology Modeling

In the proposal for this contract, impurity diffusion was cited as a critical dimension-limiting step in scaling MOSFET's for VLSI. Both the oxide isolation effects as well as scaling of the intrinsic shallow-junction FET were presented as fundamental concerns. The objectives cited in this subsection included:

1. Investigation of physical effects for impurity diffusion--especially oxidation enhancement and local oxidation effects.

2. Development of methods for two-dimensional analysis of these effects.

Accomplishments

Over the period of this contract several major advances were made both in understanding the kinetics of process models and in developing analysis methods to support the physical research as well as applications to device design. The accomplishments can be identified and classified in the following areas:

1. Bulk impurity diffusion and associated point-defect mechanisms [1]

2. Impurity diffusion mechanisms in polycrystalline silicon [2]

3. Hybrid algorithms for simulation of coupled oxidation-diffusion in two dimensions [3]

4. Kinetic models and algorithms for two-dimensional oxidation [4].

Each of these accomplishments will now be discussed along with the intermediate results which have been presented.

At the beginning of this contract we had reported new results concerning two-dimensional impurity diffusion [5]. These results are widely quoted as the first quantitative data giving lateral penetration of point defects which alter diffusivity. Moreover, others have developed analytic models for the phenomena based solely on this data [6]. Subsequent to this novel two dimensional work, extensive data was taken and published on the oxidation rate dependence of diffusivity in one dimension [7]. Simultaneously, careful examination of the ambient dependence of stacking fault growth and retrogrowth revealed a power law dependence on oxidation rate [8]. This analysis lead to the development of a comprehensive model for both growth/retrogrowth of stacking faults as well as impurity diffusion owing to the generation of interstitials at the silicon dioxide-silicon interface [1]. This work also opened the way for a further study of defect mechanisms in polysilicon.

During the course of this research it has become clear that diffusion phenomena in polycrystalline silicon shows fundamentally different properties than in the bulk. The study of arsenic diffusion in polysilicon by means of Rutherford backscattering provided the key evidence that both bulk and grain boundary diffusion occur simultaneously and can be clearly distinguished [9]. These results show clearly that grain boundary diffusion is four orders of magnitude higher than in the bulk. Subsequent work showed the effects of dopant segregation at the interfaces--both lateral boundaries as well as at the poly-bulk interface [2]. In a further study of grain boundary effects related to point defects, undoped polysilicon was used as a buffer layer to consume defects generated during oxidation. It was shown by means of marker layers in the bulk that for polysilicon thicknesses of about 5000A, the grain boundaries consume virtually all defects generated during oxidation [2]. The parameters for the grain boundary model were extracted based on use of two-dimensional process simulation [10].

Simultaneously with the polycrystalline diffusion modeling discussed above, a model for change in the poly grain structure itself was being developed [11]. The key feature of the model is a dopant dependent growth mechanism which accounts for enhanced growth in n-type doped layers [12]. The combined models for impurity diffusion and grain growth in polysilicon are now incorporated into the SUPREM III multilayer process simulator [13].

The problem of simultaneously modeling oxidation and diffusion in two dimensions has posed both experimental and numerical difficulties. In the course of this work, advances in both experimental techniques as well as in modeling have been achieved. The experimental effort used sidewall capacitance and breakdown properties of n+ regions near locally oxidized edges to characterize lateral boron diffusion in the presence of two-dimensional oxidation [3]. The modeling used was an extension of a purely analytic technique developed earlier [14]. By combining a set of analytic solutions for simultaneous oxidation and diffusion with numerical solutions for the case of a fixed boundary diffusion, a novel simulator was demonstrated [15]. The technique shows orders of magnitude speed improvement over purely numerical solutions and the technique has been applied in several device studies [10].

In the process of understanding the process models and their limitations for two-dimensional oxidation, a new approach is formulated. A novel reduced-grid solution to the Navier-Stokes hydrodynamics equation was used to model the creeping flow of the oxide during growth [16]. The numerical algorithm involved an extension of the boundary-value method developed for efficient device analysis [17]. An interaction between pressure and velocity is used subject to an artificial compressability condition to simplify the solution. This assumed decoupling is removed upon convergence of the algorithm. Using the oxide growth simulator, many properties of locally oxidized structures were investigated and understood. Simulated results and experiments clearly show the dependence of pad oxide and nitride layer thicknesses as well as etched surfaces on bird's beak shape and encroachment [18]. An extensive set of simulations and comparison with published stacking fault data showed the direct correlation of stress conditions during oxide growth with defect generation. In addition, a first order semi-

analytical formula was developed to model the stress-defect generation dependence [18]. The overall impact of this oxidation modeling effort is two-fold. First, the groundwork is now laid to develop a more robust coupled oxidation-diffusion solver. Second, the simulation tool can be used as the basis to go further in understanding the two-dimensional oxidation kinetics themselves [4]. In fact, both these topics are now being addressed in the follow-on contract.

3. Coupled Process and Device Modeling Tools

The scaling of devices for VLSI, especially MOSFET's requires the judicious trade-off of process variables and device dimensions. Short- and narrow-channel effects can be minimized or can become dominant depending on the design choices to be made. The proposed research objectives cited in this subsection of the proposal include:

1. The use of two-dimensional tools to characterize performance-limiting effects in MOS devices.

2. The investigation of new analysis methods to understand fundamental device limits--especially for short channel devices.

Beyond these two specific sets of tasks, it was projected that the coupling of process and device understanding and the unified model of MOSFET's would be of lasting value for VLSI development.

Accomplishments

During this contract an extraordinarily broad set of accomplishments were realized in the area of tool development and applications. In the area of analysis of MOS performance limits, processes at Stanford, Hewlett-Packard, and Texas Instruments were studied with uniformly good results. In the tool development area, two new process simulators were created as well as a new two-carrier device simulator. The analysis methods work produced several new results--both in terms of device characterization and parameter extraction. The list of highlight accomplishment includes:

1. Characterization and modeling of subthreshold and punchthrough limits of MOSFETs [19]

2. Modeling of narrow-width effects in MOSFETs [20] [21]

3. Process modeling for manufacturing including statistical effects [10]

4. Demonstration of a new hybrid analytical/numerical process simulator--"SUPRA" [10]

5. Demonstration of a new oxidation analysis tool--"SOAP" [23]

6. Demonstration of a new nonplanar device simulator including mobile carriers--"PISCES" [24]

7. Demonstration of an optimized extraction technique for model parameter determination--SUXES [25]

8. A new s-parameter characterization technique with applications to large- signal time-domain modeling [26]

9. A new time-domain concept for on-chip signal sampling via optical switches.

Over the contract period two major review articles were written on the subject of process modeling and they cover many of the topics outlined above [22] [27]. Nonetheless, each of the topics cited above is now briefly summarized.

During a previous contract we demonstrated that Poisson analysis can be used to understand performance limits of MOSFET's in subthreshold and punchthrough [28]. During this contract we released the "GEMINI" program [29] and used it further to understand the details of modeling conditions of weak inversion [19], [30]. The GEMINI tool is now used broadly in the industry and cited throughout the literature in this regard (i.e. see ref. [21]). In a follow-on investigation the use of Poisson analysis for narrow width effects [20] proved to be great value and industrial efforts at TI in this same direction have developed SPICE models based on the GEMINI tool [21].

In the area of two-dimensional process simulation, two major programs have been developed during this contract. The process simulator SUPRA was demonstrated [15] and has been broadly distributed in industry. As stated in the previous section, this tools has been used in several studies to understand physical limits such as boron lateral diffusion near local oxidation edges [3] and dopant diffusion in grain boundaries of polysilicon [10]. The SOAP program has provided a breakthrough in process modeling of

oxide growth [23]. Moreover, this program has leveraged fundamental studies of oxidation kinetics [4].

The further development of device simulation capabilities has focused on nonplanar analysis including mobile carriers. The PISCES program [24] has provided a powerful tool for both fundamental and applied studies. Effects such as mobility degredation due to surface scattering and bulk doping have been modeled physically with PISCES [24] [30]. In collaboration with Hewlett-Packard, the PISCES program is now being used to model GaAs MESFET's and to help design new processes. In the follow-on activities funded by ARO, the program has been extended to two-carriers and will be used for CMOS latch-up modeling as well as to model other bipolar effects.

The extraction of model parameter, both for process models as well as device models in SPICE, has been a troublesome area for engineers. Obtaining good model fits with realistic physical parameters can be troublesome and time consuming. The development of the SUXES program [25] has provided important leverage in overcoming these problems. The program has been used extensively for SPICE parameter extraction. More recently it has become clear that the approach is extremely attractive for both process and device modeling applications. SUXES is already being used for parameter extraction for complex process models including multiple species effects. Continued work with regard to device analysis and direct input into SPICE is an attractive extension of the work completed under this contract.

It was originally proposed that new methods for analysis of transient device effects would be developed. During this contract two new measurement techniques were developed as well as an extension of the one-dimensional transient device simulator "SEDAN" [31]. For very fast devices where the transit time is much shorter than typical pulses used in switching, it was found that by characterizing the device with s-parameters over a large signal bias range that accurate transient modeling could be achieved based on small signal parameters [26]. These results were tested for fast GaAs FET's in collaboration with Toshiba Corporation. Most recently a new time domain has been developed based on optical sampling switches. In collaboration with Los Alamos National Laboratory the

technique is now being tested with switches fabricated in bulk silicon. The effort will continue into the new contract period. This time domain tools should be most useful to characterize transient charge effects in MOSFETs. A final effort in time-domain simulation began as a follow-on to earlier work with SEDAN [32] Two novel applications have been realized:

1. The analysis of bipolar devices, particularly polysilicon emitter structures [33] and

2. The analysis of latchup phenomena [34]. This latter work in latchup will continue into the new contract. The two order-of-magnitude computational efficiency advantage of the approach over a fully two-dimensional analysis such as with PISCES makes it extremely attractive as an engineering tool.

Conclusions

The preceding two sections have outlined both fundamental advances in two-dimensional process modeling as well as new CAD tools developed over the past three years of the contract. Major accomplishments in both oxidation and diffusion studies have resulted in new understanding of these processes [1] [2] [4]. Moreover, new tools for process analysis--SUPRA and SOAP--have been developed and distributed [15] [23]. Studies both at Stanford and in industry have shown the relevance of coupled process and device simulation. The GEMINI and PISCES programs have been shown to be well suited to these purposes [19] [29] [24]. Parameter extraction capabilities as demonstrated with the SUXES program [25] have assisted in automated and accurate SPICE model fitting. Finally, new measurement techniques in the frequency and time domain have advanced the modeling art and provide the capabilities to gather useful data to understand device *limits* [35]. These measurement techniques now flank the analysis and modeling capabilities reported earlier [36] as well as new enhancements to the SEDAN program for transient device analysis [31].

As stated earlier, two major review papers outline many of these accomplishments as well as establishing the overall framework for process modeling [22] [27]. Appendix I gives the results presented in the 1981 invited paper [27] while Appendix II summarizes many of the more recent results given in the 1983 invited paper [22]. Of particular interest is Figure 20 of Appendix II along with the associated text. The figure reveals

the interrelationship of the CAD tools developed under ARO sponsorship both in this program as well as those at Berkeley and CMU.

It should be noted that this program has been exceptionally productive in communicating results as well as software to the industry. Appendix III shows the short course announcements for the annual research review at Stanford as well as the attendance lists of companies represented. Also listed in Appendix III are the current statistics on software distribution.

In conclusion, this research program has produced more than half-a-dozen highly skilled PhD's as well as several MS degrees. These individuals now work for companies . . as IBM, Bell Labs, HP, and AMD as well as the Air Force and academic institutio The output of both research and software is highly visible and well-received throug . the industry. The follow-on research program will extend many of the most p . g results discussed in this report.

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Process Modeling of Integrated Circuit Device Technology

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Invited Paper

Abstract—This paper reviews the field of computer-aided design as applied to process modeling of integrated circuit technology and devices. Device design applications for process modeling are considered for both bipolar and NMOS technologies. The kinetics of oxidation and impurity diffusion in silicon are discussed. The numerical solution of impurity diffusion is considered, including grid and time step constraints. New efforts in two-dimensional process modeling are briefly discussed along with test structure work needed for parameter estimation.

I. INTRODUCTION

THE MODELING of fabrication processes for integrated-circuit (IC) technology including the simulation of electrical device behavior is now as commonly used as circuit simulation. The purpose of this paper is to define the general topic of process simulation, review advances in the field and outline the frontiers as we now see them. The need for such modeling and simulation tools can be understood by examining the metal–oxide–semiconductor (MOS) transistor cross sections shown in Fig. 1. Fig. 1(a) shows typical MOS device dimensions circa 1970 and Fig. 1(b) shows those of the current state of the art. It can be seen that the vertical dimensions of oxide thickness and junction depth, for example, have been reduced substantially. More important is the shrinkage in spacing between the source and drain junction regions—called the effective channel length. It is this shrinkage in channel length that has resulted in the astronomical growth in transistor packing density. However, Fig. 2 shows the effect that scaling the effective channel length L_{eff} has on the threshold voltage V_{th}—the gate voltage needed to turn on the transistor. From the figure it is apparent that the threshold voltage changes with channel length. Moreover, the spread in measured values increases as dimensions are reduced. The control of both absolute value and statistical spread of parameters are major concerns for scaled-down devices. Because hundreds of thousands of devices of varying dimensions are being used on each very-large-scale integration (VLSI) chip, it is essential that parameter variation should be well understood and controlled. The solid line in Fig. 2 shows the simulated device threshold voltage as a function of device channel length. The agreement with experiment indicates that device simulation is a useful tool for understanding the distribution and control of device parameters.

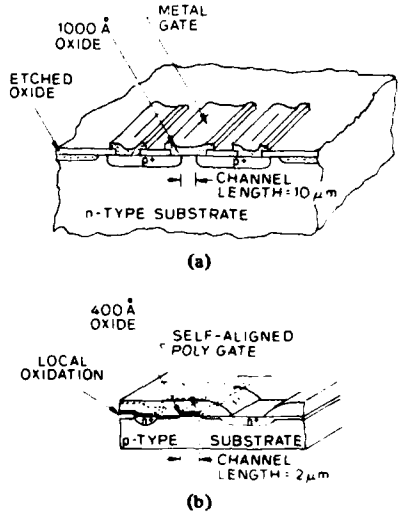

Fig. 1. Cross-section view of MOSFET devices as they have evolved from the 1960's to the present. (a) A p-channel metal gate device with 10-μm channel length circa 1970. (b) An n-channel silicon gate device with local oxidation used for isolation and a 2-μm effective channel length.

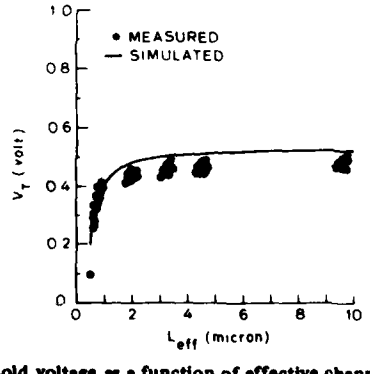

Fig. 2. Threshold voltage as a function of effective channel length for a NMOS process [59]. Both simulated and measured data show the dramatic sensitivity to variations in L_{eff}.

To understand the full implication of Fig. 2 it is necessary to turn to the schematic presentation of the fabrication sequence shown in Fig. 3. Shown in this figure are three aspects of the fabrication sequence used to create an MOS device: 1) a patterning mask is defined, 2) the gate region is etched,

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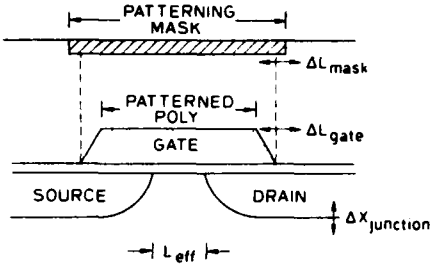


Fig. 3. Schematic cross-section of an NMOS transistor with variations in patterning mask (ΔL_{mask}), etched polysilicon gate (ΔL_{gate}) and diffused junction depth ($\Delta x_{junction}$) as shown. All contribute to the final effective electrical channel length.

and 3) the junction impurities are introduced into the silicon. Because all changes directly alter L_{eff}, and thus impact the electrical threshold parameter as shown in Fig. 2, it is apparent that an understanding of the various fabrication steps is crucial to predicting device performance. The modeling of the fabrication steps depicted in Fig. 3—as well as all others needed to create working IC devices—has come to be known as *process modeling*. The impact of process modeling is reflected primarily via its application in device modeling. The results shown in Fig. 2 reflect the essential coupling of process modeling and device analysis—that is, the underlying physical process variations control the observed electrical variations.

It is important to define the parameters involved in both process and device modeling. A simple statement of the problem suggests that there are 1) fundamental *physical constants* such as mobility and diffusivity, and 2) *process-controlled parameters* such as gate etch rate and source ion implantation dose. Unfortunately, the present understanding and modeling of these parameters is neither concise nor exact. First, the physical constants depend on fabrication conditions and device topologies. Second, the process parameters frequently depend on equipment and experimental conditions. Despite these obstacles, much progress has been made in quantifying both the physical constants and the parameters which depend on processing techniques. Both aspects of the parameters involved in process modeling and device simulation are discussed in subsequent sections.

As a final matter for consideration it is useful to define the *context* in which modeling and simulation are used. Device design is the dominant motivation for, and application of, process modeling and device simulation. There are a number of aspects of device design, including 1) physical constraints, 2) design tradeoffs, and 3) optimization of a given technology. The physical constraints involved in device design include both the fundamental constants and practical fabrication conditions. For example, the tradeoff between a surface channel or buried channel MOS device involves both the carrier mobility and the ion implantation used to create the channel region. Hence, at all times the designer wishes to determine the physical distribution of impurities and the implication of these impurities and applied bias conditions on the electrical device behavior. The tradeoffs of physical constraints with desired performance objectives constitute the design process. Design can frequently involve much trial and error; it is the objective of process modeling and device simulation to reduce the design time and simultaneously increase the success rate in achieving well-designed processes. The relative time and cost for simulation makes it highly useful since many fabrication runs and device topologies can be considered in the time it takes to create the first working device. The ability to make variations (or "run splits") is highly desirable both for optimizing designs and for targeting initial choices of experiments to be performed.

This paper traces the organization of the process modeling field. In Section II the understanding of process physics for electrical structures fabricated in the bulk silicon technology is reviewed. Section III describes the practical considerations in creating a process simulator to account for such effects. In Section IV the applications for process simulation in the context of a normal process design and control environment are discussed. In addition to the device engineering applications, it is clear that researchers with interests in material physics are using process simulation in developing their physical understanding. Section V opens the discussion of process modeling to a broader range of topics, including two-dimensional considerations. In Section VI the new modeling efforts in multidimensions are briefly introduced. Section VII gives a summary and conclusion.

II. Process Models for Dopant-Related Phenomenon

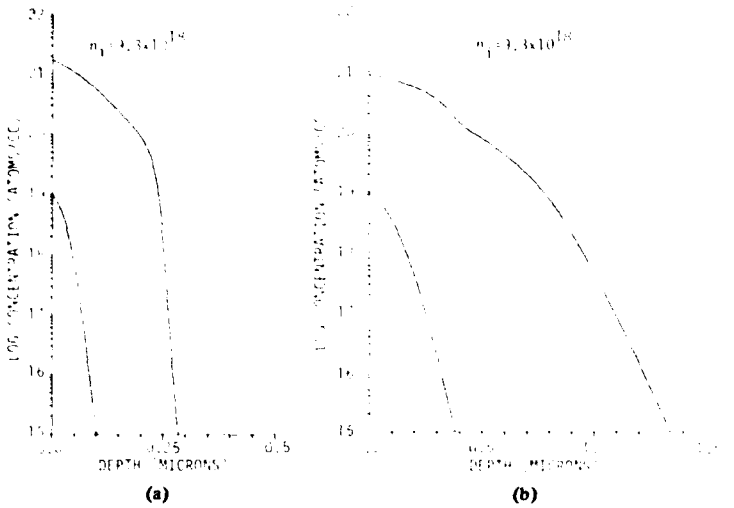
Oxidation and diffusion in silicon are the essential fabrication steps needed to form IC devices. Hence the study and modeling of these phenomenon date to the early days of transistor design [1]-[6]. Since that time there have been continued investigations, extensive collection of data and the development of models to represent the physical effects. Recent reviews give extensive documentation of the results [7]-[9]. In order to explain process simulation it is useful to review the basic features of modeling oxidation and diffusion—the key steps in IC fabrication technology.

The oxidation of silicon proceeds by diffusion of oxygen to the silicon interface where the oxidizing reaction occurs [4]. In the process of the reaction there is a motion of the interface by an amount Δx_{ox} and a swelling of the oxide layer by an amount $1/\alpha$, where α is the ratio in density between the silicon and silicon dioxide. The first-order model for oxidation predicts

$$x_{ox} \approx \frac{A}{2}\left[\sqrt{1+\frac{t+\tau}{A^2/4B}}-1\right] \tag{1}$$

where B/A and B are exponentially activated growth coefficients—the so-called linear and parabolic terms [5]. These coefficients, in addition to their temperature dependence, are dependent on parameters such as silicon crystalline orientation, substrate impurity concentration and ambient conditions [9]. From the perspective of process modeling, the moving boundary created by the oxidation requires careful consideration [10]. At present, the coupling of oxidation with other process physics can be stated as a deterministic set of independent boundary conditions at the respective interfaces. Hence there is no need to simultaneously solve for boundary motion along with diffusion. The decoupling of oxidation from diffusion provides substantial simplification from that of a free-boundary problem, a typical occurrence in many physical problems [11]. In Section III, the numerical means for simulating oxide growth are discussed.

The diffusion of impurities in silicon is directly correlated with the motion of point defects—vacancies and most probably interstitials as well [3], [7]. The motion of each impurity



(a) (b)

Fig. 4. Simulated profiles for (a) arsenic and (b) phosphorus impurities under both intrinsic and high concentration conditions. The intrinsic diffusion profiles match Gaussian analytical solutions. The high concentration profiles show effects of clustering (i.e., the dashed curve in (a) as given by (6)) and vacancy-enhanced diffusion (i.e., the "kink" effect in (b) as calculated using a modified form of (5)).

obeys a continuity equation subject to local dependence of the diffusivity on point defect concentrations and the electrostatic potential. The continuity equation for each impurity species in one dimension has the form

$$\frac{\partial C}{\partial t} = \frac{\partial}{\partial x}\left(D\frac{\partial C}{\partial x}\right) \pm \frac{q}{kT}\frac{\partial}{\partial x}\left(D\hat{C}\frac{\partial \phi}{\partial x}\right) \tag{2}$$

where C and $\hat{C}$ are the total and electrically active concentrations (the plus sign applies for acceptors and the minus sign for donors) and ϕ is the electrostatic potential given by

$$\phi = \frac{kT}{q}\ln\frac{n}{n_i} \tag{3}$$

where n and n_i are the actual and (at the diffusion temperature) intrinsic electron concentrations. Under conditions of high impurity concentrations, the diffusivity is substantially changed. The simplest formulation for the changed diffusivity is given by

$$D = D_i\left(\frac{1+\beta(n/n_i)}{1+\beta}\right) \tag{4a}$$

for donor impurities and

$$D = D_i\left(\frac{1+\beta(n_i/n)}{1+\beta}\right) \tag{4b}$$

for acceptors, where D_i is the intrinsic diffusivity and β is an empirical coefficient. There are more complicated formulations which consider the charge state of the point defects. For example, using a vacancy model [7] the diffusivity can be written as

$$D = D^0 + D^+\left(\frac{n_i}{n}\right) + D^-\left(\frac{n}{n_i}\right) + D^=\left(\frac{n}{n_i}\right)^2 \tag{5}$$

where the superscripts denote the charge state of the point defects associated with each contributing portion of diffusivity and the factors involving either n_i/n or n/n_i estimate the normalized equilibrium concentrations of each defect species. For the simplified forms given in (4), the empirical coefficients are given by $\beta = D^-/D^0$ for donors and $\beta = D^+/D^0$ for acceptors. Unfortunately, experimental results are not yet available to resolve the details of individual defect contributions to (5), although in the case of phosphorus the shape of the profile under high concentration conditions shows three distinct regions which have been interpreted using this model [7]. The determination of the exact point defect kinetics involved in impurity diffusion is a topic of extreme importance in the further development of process modeling.

Under conditions of high concentration there can be clustering and precipitation of impurities which result in electrical inactivity [12]–[14]. A typical example of this effect can be given for arsenic where the relationship between total and electrically active concentration is

$$C = \hat{C} + nk\hat{C}^n \tag{6}$$

where n is the number of atoms in a cluster and k is the equilibrium constant which is temperature dependent. Although it is possible to model this process dynamically [13], at present the data suggests this is not necessary for practical conditions. Mathematically, a dynamic model would require coupled continuity equations with an associated rate constant to describe the coupling between the two states. Although there is some data concerning these rates [13] the computational overhead of modeling two species and the associated restrictions concerning time steps for simulation do not warrant such model complexity. Hence, in present process simulators an equilibrium model such as that given by (6) is used.

To summarize the preceding discussion of impurity diffusion, Fig. 4 shows the simulated profiles for arsenic and phosphorus, each diffused for equivalent times under conditions of both low and high concentration. For the low

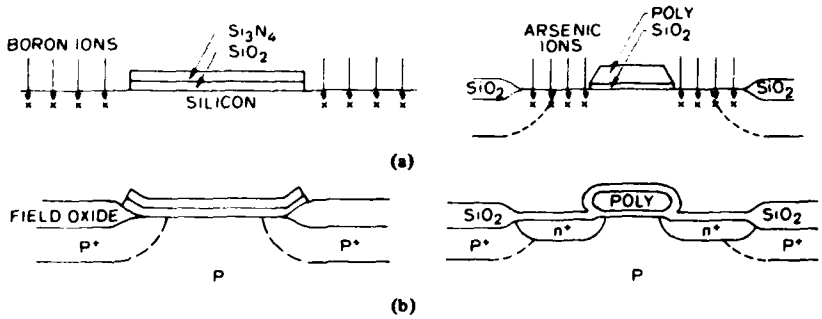


Fig. 5. Cross-section of an NMOS transistor during the fabrication sequence to illustrate the dominant role of oxidation and impurity redistribution including the two-dimensional effects of topography. (a) Implantation of boron and the local oxidation to isolate transistors. (b) Implantation of arsenic to form source and drain along with the additional topography changes due to oxidation.

concentration results, where the maximum concentration is less than n_i, the profile is nearly Gaussian in shape as would be expected from classical theory for constant diffusivity [4]. The high concentration profile for arsenic shows the effects of enhanced diffusivity and clustering. The specific details of the models used in these simulations are described elsewhere [15]. There are several recent discussions of process modeling including diffusivity, high concentration and clustering effects, as summarized in the preceding [16], [14].

The preceding discussion has emphasized the individual effects of oxidation and diffusion. In IC technology, where impurities are diffused during oxidation, the two effects are intimately coupled in device fabrication. In addition, there are frequently multiple layers of material involved in a practical device structure. For example, portions of the fabrication of an NMOS device are shown in Fig. 5 with schematic cross sections. The first step shown is the patterned ion-implantation of boron and subsequent local oxidation to form the so-called field regions which isolate the devices. The important aspects of these steps include masking properties of the silicon-nitride/silicon-dioxide layer (both for implantation and oxidation) and the oxidation/redistribution of boron during the field oxidation process itself. The second section in Fig. 5 shows the patterned polysilicon region which masks the source-drain ion implantation. Subsequent oxidation will change its thickness, doping concentration and topography. It is apparent that the oxidation of all silicon surfaces is a major factor in device technology. The consideration of two-dimensional effects for both patterning and oxidation/diffusion are considered in Section VI.

The presently accepted statement of the moving boundary problem for silicon oxidation involves a deterministic motion of the interface as described earlier. The impurities are redistributed in concert with this convective boundary motion via the thermodynamic segregation properties between the materials. There is a flux from material 1 to 2 given by

$$F_{1-2} = h\left(C_1 - \frac{C_2}{m_{1-2}}\right) \tag{7}$$

where F is the flux from region 1 to 2, h is a velocity which accounts for the equilibration rate of the segregation process and m is the segregation coefficient. This flux is then included as a boundary condition for the diffusion in each layer. The segregation properties of impurities in the silicon/silicon-dioxide system favor boron in the oxide and phosphorus and arsenic in the silicon [4]. The physics of this redistribution are still being studied and coefficients presently used for process modeling represent the results of data analysis based on equilibrium kinetics (i.e., h has a large value). The presence of multiple layers, such as the gate region shown in Fig. 5, requires the proper application of the diffusion equations in all regions with appropriate boundary fluxes used at each interface. The numerical implications and implementation of these equations are discussed in Section III.

As a final point with regard to the physics of moving boundaries for one-dimensional process simulation it is important to consider the models for deposition and etching. In principle, the models appear to have the same basic form as does oxidation of silicon. However, the kinetics of both chemical vapor deposition and plasma or reactive ion etching involve more complicated kinetics—even for first-order modeling. In the case of epitaxial deposition it has been demonstrated that the transient properties of both the silicon deposition and the dopant incorporation must be considered [17]-[19]. The modeling of one-dimensional etching to date has been of an empirical nature [20]. In addition, there are system dependencies including partial pressures and bias/loading effects. Nonetheless, it appears that kinetic models will soon be developed [21].

III. Computer Implementation

The computer implementation of process models for IC fabrication dates from the mid-1960's and is based on work at a number of industrial laboratories [22]-[24]. It was clear at that time that a numerical solution of the oxidation/diffusion problem, even in two dimensions [25], was not a major problem. The lack of suitable kinetic models, however, was a major obstacle—the emphasis on phosphorus-diffused bipolar technology at that time created a special problem due to the complicated diffusion characteristics of phosphorus. Another problem, probably as important as the lack of accurate kinetic models, was the need for an engineering-oriented tool that utilized the available process models. In the 1970's, circuit simulation became solidly established [26], providing a practical example for developments in related disciplines. As early as 1971, a process-oriented device simulator demonstrated the concepts of using a process description as a user input format [27]. Building on the previously reported

modeling approaches and experience from circuit simulation, process simulation has now become a useable engineering tool [28], [29].

In summary, the factors which have influenced the development of process simulation have been primarily the lack of both accurate kinetic models and a viable user interface. Numerical implementation, while it does not critically limit the development of process simulation, poses an interesting challenge in implementing kinetic models. Some of the choices made in implementing process models for oxidation and diffusion are reviewed later.

A. Numerical Versus Analytical Computer Solutions

In order to accurately model the processing of IC devices, numerical and analytical techniques have been considered [30], [31]. While analytical solutions exist for expressing an impurity profile using processing information, they are usually derived either from a simplified physical model or from a functional fit to empirical data. These approaches tend to be valid only for a restricted set of processing conditions. On the other hand, the analytical techniques provide excellent insight and efficiency–independent of their useability for complex kinetics or multistep processes. Numerical methods allow a more exact modeling of the physics involved during the various sequential processing steps. In addition, they tend to be more accurate and are applicable over a much wider range of processing conditions.

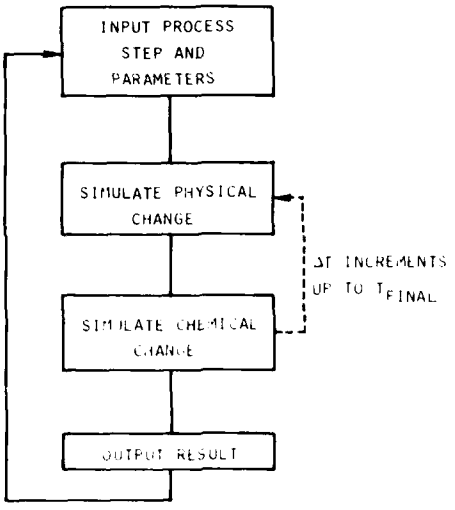
Impurity redistribution during thermal cycling is an important and useful example to consider in discussing the choice of either analytical or numerical solutions. For impurities whose peak impurity concentration is below n_i, the intrinsic carrier concentration at the diffusion temperature, simple analytical solutions fitting the impurity profiles to Gaussian or complementary error functions have been widely used [4]. At high concentration levels, greater than n_i, diffusivity becomes a function of distance as shown in Fig. 4(a). This invalidates a key assumption used in deriving these simple solutions. Several analytical approaches have been reported [32]-[34], based on polynomial curve fits to empirical data for arsenic or boron diffusion at high peak impurity concentrations. These models become inaccurate as the peak concentration approaches n_i because of model assumptions. In addition, no satisfactory analytical model exists for phosphorus profiles at high peak concentrations. The most serious shortcoming of the analytical solutions results from the fact that the physical characteristics of the system are changing in both time and space during the processing step. For example, boron diffusivity may be enhanced due to its own high concentration or self-induced electric fields. It may be substantially altered by the presence of significant concentrations of n-type impurities. In turn, the presence of boron in high concentrations may influence the diffusivity of other impurities or it can affect the oxidation rate of silicon.

The accuracy and generality obtained by using the more physical models which must be solved numerically is obtained at the expense of increasing complexity. The device cross section, whether it is one- or two-dimensional, must be discretized in space–represented as a collection of small cells. The processing time, for example, the time of an oxidation step, must also be discretized. This discretization of time and space allows the important assumption to be made that the concentrations of the various impurities present are constant over each individual cell during the time increment, as are the diffusivity and other physical parameters.

B. Numerical Implementation

Having explored briefly the comparison of numerical and analytical approaches to process modeling, this subsection gives a description of the numerical approach. It is necessary to create a spatial grid on which one solves for the concentration of impurities as a function of time. The grid spacing must be sufficiently dense so that all profile features are accurately represented. On the other hand, since numerical solutions can be time consuming, it is important not to use an excessive number of grid points for the solution. In a similar way, the increments of time used for process simulation must be short enough to not "step-over" important effects–thereby causing errors. But if the time increments are too small the simulation time becomes excessive. Moreover, for shallow profiles as used in VLSI devices, the proper control of time increments is reflected directly in junction depths which control, for example, simulated channel lengths in MOS devices. The time step constraints are especially important since the objectives of a simulator for complete process modeling require numerical solutions over many process steps and, frequently, long periods of time.

The schematic operation of process simulation is illustrated in Fig. 6(a). For each step in the sequence which describes integrated circuit fabrication–for example ion implantation followed by diffusion and oxidation–the physical and chemical changes in the one-dimensional slice are simulated on a spatial grid by means of incrementing time and solving the diffusion equations for all impurities. Time is advanced and the process is repeated until the final specified time for that step is completed. Then the next step is considered and the inner simulation loop is again activated. Fig. 6(b) shows a typical input specification for a three-step process used to create the so-called boron channel-stop profile under the field oxide which isolates neighboring devices. The first step is a boron ion implantation which takes no looping in time to simulate–simply a lookup table of values for the profile spatial distribution [35]. The subsequent oxidation steps each require inner simulation loops in discrete time as shown in Fig. 6(a). The input format of each step uses keywords to identify needed parameters and simulation control. For example, the MODEL card specifies the physical coefficients used to model diffusion and oxidation, while the STEP card gives the process dependent information such as times and temperatures. The physical change shown in Fig. 6(a) corresponds to added thickness of the oxide layer (see (1)). The chemical change is the redistribution of boron by thermal diffusion (see equation (2)) and segregation into the oxide (see (7)). These equations are evaluated at each time step and, in the case of the diffusion equation, all grid points are solved simultaneously by means of standard matrix inversion techniques [36]. Fig. 6(c) shows the impurity profiles of the boron in both the silicon and oxide at the end of each of the steps. Although the simulation grid is not shown, there is grid allocated both in the oxide and in the silicon. For the case of boron diffusion and segregation, a major fraction of the dopant ends up in the oxide. The interface plays a dominant role in this process–both physically and numerically. Let us consider the problem of grid allocation in a two-layer system including the effects of segregation. Following this discussion we will return to the



(a)

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TITLE   FIELD IMPLANT
GRID    DYSI=0.005, DPTH=0.5, YMAX=2.0
SUBS    ORNT=100, ELEM=B, CONCENTRATION=1.0E15

COMMENT REDEFINE WET OXIDATION COEFFICIENTS
MODEL   NAME=WET1, PRTE=7.0, PREA=0.78, PRES=0.92

COMMENT IMPLANT BORON AT 65KEV
STEP    TYPE=IMPLANT, ELEMENT=B, DOSE=5.0E12, AKEV=65

COMMENT OXIDIZE/DRIVE-IN
STEP    TYPE=OXIDIZE, TEMPERATURE=1000, TIME=10, MODL=DRY0
STEP    TYPE=OXIDIZE, TEMPERATURE=1000, TIME=73, MODL=WET1

END
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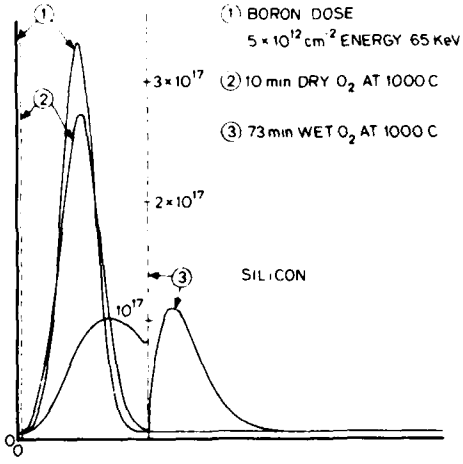
(b)



(c)

Fig. 6. The schematic representation of process simulation as a sequence of steps and an example. (a) Flowchart showing outer-looping on steps and time increments involving numerical simulation on a grid structure. (b) A typical input specification for a process sequence [15]. (c) Output plots of boron in the oxide and in the silicon for the steps listed in (b).

problem of diffusion including grid and time constraints as they affect the numerical simulation.

One implementation [15] of the spatial discretization of the silicon/silicon-dioxide structure for a one-dimensional process

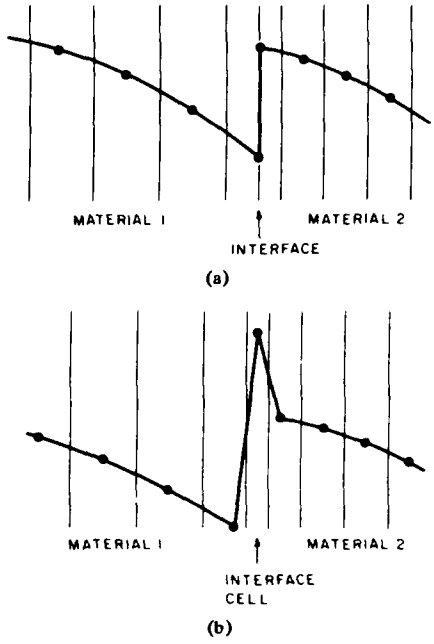


Fig. 7. Schematic representation of a spatial grid structures. (a) An abrupt interface model. (b) An interface of finite thickness.

simulation is shown in Fig. 7(a), where a section around an interface between two layers of material is shown. The thickness of the cells representing the materials on either side of the interface is shown to be constant within a particular layer. A nonuniform spacing may result if the two materials have different densities (i.e., silicon and silicon dioxide) in which case the movement of the interface will cause the grid on either side of the moving boundary to become nonuniform.

The flux of impurities across the interface is determined by the segregation flux as described in (7). When there is movement of the interface, an additional motion-induced flux

$$F = -v_{ox}(\alpha C_{I-1} - C_I) \tag{8}$$

is needed when the interface crosses a cell boundary to account for the relative expansion of the oxide layer due to the difference in density [10]. Although this approach is adequate for long diffusion times, recent experimental results have suggested that the preceding modeling of the interfacial region is insufficient [37]-[38]. The transition region from one material to another has a region of finite thickness that acts as a trap for the impurities present near the interface. To more accurately model the effects of the interface, a modified grid structure, shown in Fig. 7(b), replaces the abrupt interface with an interfacial cell of finite thickness. The motion-induced boundary flux is unaffected by this change, but the segregation flux across the abrupt boundary is replaced by two similar equations describing the flux across the boundaries of the interfacial cell. These two fluxes are

$$F_m = h\left(C_I - \frac{C_{I+1}}{m_m}\right) \tag{9a}$$

and

$$F_n = h\left(C_{I-1} - \frac{C_I}{m_n}\right) \tag{9b}$$

where F_m is the flux between the interface cell and the layer below it, F_n is the flux between the layer above and the interface cell, and m_m and m_n are the corresponding segregation coefficients. The effects modeled by the inclusion of this interfacial cell are most significant for the shallow junction depths and short diffusion times needed in VLSI technology. The thermal redistribution of impurities between the cells not at the interface is due to diffusive fluxes which are calculated using (2).

As mentioned in Section II, the oxidation of silicon to form silicon dioxide can be described by (1). However, this formulation assumes that the parabolic and linear growth rate coefficients B and B/A are constant over the duration of the oxidation step, an assumption that is not valid as the concentration in the silicon at the interface exceeds n_i. Thus (1) is recast in the incremental form

$$\Delta x_{ox} = \frac{1}{2}\left[-(2x_{ox} + A) + \sqrt{(2x_{ox} + A) + 4B\Delta t}\right] \quad (10)$$

and the values of B and B/A are recalculated at the beginning of each time increment Δt.

The spacing of the grid on which the physical system is simulated is of critical importance. The most obvious consideration in choosing the grid spacing involves the need to accurately represent the distribution of impurities. The accuracy of the physical representation is the most important consideration, but this choice also affects the accuracy of the numerical solution. Depending on the error terms of the numerical method used, the time step must decrease as the grid spacing decreases.

The constraints on both grid spacing and time increments are illustrated by the following example. For the diffusive fluxes, ignoring all second-order effects, the change in impurity doping in a volume changes with time in a manner described by Fick's second law

$$\frac{\partial C}{\partial t} = \frac{\partial}{\partial x}\left[D\frac{\partial C}{\partial x}\right]. \quad (11)$$

In order to solve this problem over the spatially discretized system, a matrix equation of the form

$$\frac{\partial \vec{C}}{\partial t} = A\vec{C} \quad (12)$$

is needed, where $\vec{C}$ is the concentration vector

$$\vec{C} = \begin{bmatrix} C_1 \\ C_2 \\ \cdot \\ \cdot \\ \cdot \\ C_{m-1} \\ C_m \end{bmatrix}.$$

The matrix A is defined as

$$A = \begin{pmatrix} A_{11} & A_{12} & \cdots & A_{1n} \\ A_{21} & A_{22} & \cdots & A_{2n} \\ \cdot & \cdot & & \cdot \\ \cdot & \cdot & & \cdot \\ \cdot & \cdot & & \cdot \\ A_{m1} & A_{m2} & \cdots & A_{mn} \end{pmatrix} \quad (14)$$

where

$$A_{ij} = \begin{cases} \dfrac{2D_{i-1}}{h_{i-1}(h_{i-1}+h_i)}, & j = i-1 \\ -\dfrac{2D_{i-1}}{h_{i-1}(h_{i-1}+h_i)} - \dfrac{2D_i}{h_i(h_{i-1}+h_i)}, & j = i \\ \dfrac{2D_i}{h_i(h_{i-1}+h_i)}, & j = i+1 \\ 0, & j < i-1 \text{ or } j > i+1. \end{cases} \quad (15)$$

D_i is the diffusion coefficient and h_i is the grid spacing between grid cells i and $i+1$.

From [36], the solution to (12) can be represented in terms of matrix exponentials (i.e., $e^A = \sum_{n=0}^{\infty}(1/n!)A^n$)

$$\vec{C}(t) = e^{At}\vec{C}(0) \quad (16)$$

where $\vec{C}(0)$ is the initial concentration vector. Define discrete times t_n, t_{n+1} such that $t_{n+1} = t_n + \Delta t$ and the concentration at each time step can be written

$$\begin{aligned} \vec{C}^n &= \vec{C}(t_n) \\ &= e^{At_n}\vec{C}(0) \end{aligned} \quad (17)$$

$$\begin{aligned} \vec{C}^{n+1} &= \vec{C}(t_{n+1}) \\ &= e^{At_{n+1}}\vec{C}(0) \\ &= e^{A\Delta t}e^{At_n}\vec{C}(0) \\ &= e^{A\Delta t}\vec{C}^n. \end{aligned} \quad (18)$$

Combining (17) and (18) yields

$$\vec{C}^{n+1} - \vec{C}^n = [I - e^{-A\Delta t}]\,\vec{C}^{n+1}. \quad (19)$$

Schemes yielding first- and second-order accuracy in time are obtained by using first- and second-order approximations, respectively, to $(I - e^{-A\Delta t})$ in (19)

For a first-order solution,

$$\begin{aligned} I - e^{-A\Delta t} &= I - \left[I - A\Delta t + \frac{1}{2}(A\Delta t)^2 - \frac{1}{6}(A\Delta t)^3 + \cdots\right] \\ &= A\Delta t + \epsilon_1(A\Delta t) \end{aligned} \quad (20)$$

where

$$\epsilon_1 < \frac{\Delta t}{2}\max_{1 \le i \le N}|A_{ii}|. \quad (21)$$

Ignoring the error term, equation (19) becomes

$$\vec{C}^{n+1} - \vec{C}^n = A\Delta t\vec{C}^{n+1}. \quad (22)$$

This can be rewritten as

$$\left(A - \frac{1}{\Delta t}I\right)\vec{C}^{n+1} = -\frac{1}{\Delta t}\vec{C}^n. \quad (23)$$

From (21), the maximum relative error at point i can be approximated by $|(\Delta t/2)A_{ii}|$. To keep the relative error below ϵ at each point, Δt should satisfy

$$\max_{1 \le i \le N}\left|\frac{\Delta t}{2}A_{ii}\right| < \epsilon \quad (24)$$

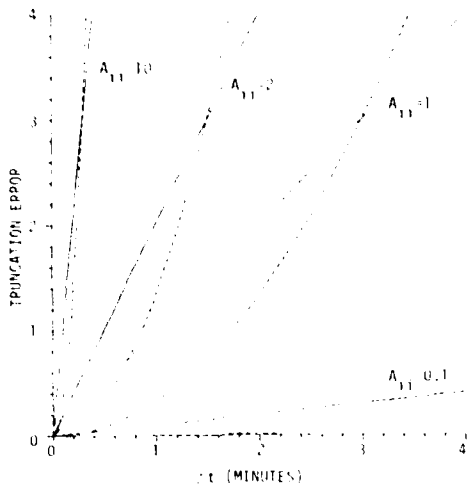


Fig. 8. Plot of truncation error versus Δt for both first- and second-order solution methods for several values of $\max/1 \leq i \leq N |A_{ii}|$. The solid line is for a first-order solution and the dashed line is for a second-order solution.

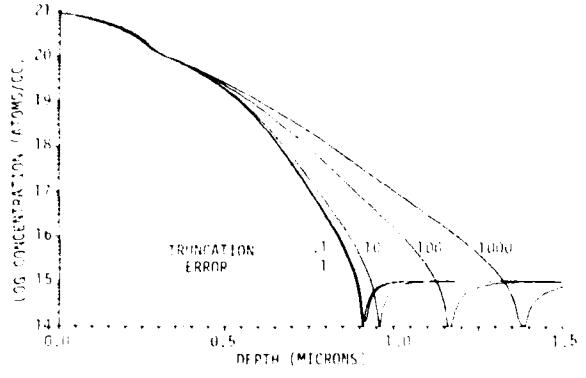


Fig. 9. Plot of several simulations of a phosphorus predeposition using different truncation error bounds.

which yields a limit on the time step of

$$\Delta t < \frac{2\epsilon}{\max\limits_{1 \leq i \leq N} |A_{ii}|}. \tag{25}$$

$|A_{ii}|$ is approximately $2D_i/h_i^2$ so

$$\Delta t_1 < \min_{1 \leq i \leq N} \left[\frac{h_i^2}{D_i}\right] \epsilon. \tag{26}$$

For a second-order solution

$$\Delta t_2 < \min_{1 \leq i \leq N} \left[\frac{h_i^2}{D_i}\right] \sqrt{3\epsilon}. \tag{27}$$

The significance of (26) and (27) can be seen in Figs. 8 and 9. Fig. 8 is a plot of the error term ϵ versus Δt for both first- and second-order solution methods and for several values of A_{ii}. Fig. 9 shows the results of a high temperature, high concentration deposition simulation using a first-order solution method for several values of ϵ. From Fig. 8 it can be seen that the size of the allowable error in the solution will have a significant effect on the total time to achieve a solution, and in the absence of other considerations will determine the order of the solution method used. The results of Fig. 9 indicate that truncation error bounds less than the cross-over value of $\epsilon = 3$ are needed, favoring the second-order solution method. The second-order method is also prefered due to consideration of overall accuracy and speed of convergence, but requires greater programming overhead and calculations per Δt. To stay within the $\epsilon = 1$ error bound shown in Fig. 9, several hundred Δt's were needed, even though the total time simulated was only 15 min. Because the number of iterations grow rapidly with greater accuracy of solution, care must be taken so as not to specify unnecessarily restrictive error bounds. The tradeoff of accuracy versus time of solution is emphasized here since most processing sequences have at least one step requiring an accuracy obtainable only through truncation error bounds less than 3. In fact, for today's VLSI structures, simulations using error bounds greater than 3 will result in erroneous device performance predictions.

To summarize this section, several final observations are helpful. Analytical techniques generally give good results for a minimal computational effort. However, when a range of sequential processing steps must be modeled, more physical models utilizing numerical techniques are required to achieve an accurate solution. The numerical solution technique used, the accuracy required, and the maximum acceptable time of solution, all affect the decisions made in designing and using a numerical process modeling program.

IV. Computer Process Simulation for Studying Physical Effects

The users of process modeling can be divided into two groups. One group contains process engineers who view modeling as a tool in the design and refinement of processing sequences. The other group uses process modeling to better understand the physics involved, which leads to better process models.

A major advantage of the numerical process simulation approach is that sequential processes can be modeled over a wide range of processing steps and conditions. It is this capability that brings process modeling out of the realm of research and allows it to be used as an engineering tool. The typical process involves a dozen or more processing steps, each of which depends on the preceding steps. To a process engineer, this ability to model a series of sequential processing steps is crucial.

One important consideration in designing a new process, or in modifying an existing one, is the calculation of sensitivities to fluctuations in the individual steps that are used. Because the final structure depends upon a linear sequence of steps, a minor variation in a step early in the process may be amplified during subsequent processing. For example, minor variations in processing temperature or implant energy can have a significant effect on the junction depth and oxide thickness. This is especially true in the state-of-the-art device processes that depend upon very shallow junctions and thin oxides. Identifying those steps in a process where fine control is needed to avoid unacceptable variations in device performance is a widely used application of process simulators.

The modeling of diffusion, oxidation, and segregation in the processing of semiconductor devices is complicated by many interacting physical mechanisms. Process modeling provides the capability to separate out the effects of various mecha-

nisms, and thereby provides an effective tool for understanding and development of physical models. It is indeed difficult to extract parameters from experimental data; however, the use of computer simulation in conjunction with experimental data, makes parameter determination more tractable [39].

To illustrate the leverage of simulation, consider the oxidation enhancement of diffusion (OED), where one has available only the initial and final oxide thickness and impurity profile, along with the processing conditions used. The factors that influence OED, the oxidation rate and the impurity fluxes, change significantly during the processing step. Extracting accurate values for the OED coefficients requires a large amount of experimental data. However, if a process simulator is used to model the coupled effects of oxidation and segregation, the OED coefficients can be determined more accurately and with far fewer experimental runs [39]. The interdependence of effects will become even more critical when extracting coefficients for models where the driving mechanisms are varying rapidly with time, as is typical for shallow junction, low temperature processes, and short process times.

The primary result when simulating a sequence of processing steps is the impurity distribution versus distance. When extracting data from a process, one usually obtains electrical characteristics rather than directly observing the impurity distribution. A common measurement is the sheet resistance R_S of a layer, defined as $R_S = \rho/x$, where ρ is the resistivity of the layer and x is its thickness. The sheet conductivity, which is the reciprocal of the sheet resistance, can be calculated from

$$G_S = \int_{x_1}^{x_2} q(\mu_n n + \mu_p p)\, dx \tag{28}$$

where n and p are the electron and hole concentrations and μ_n and μ_p are the mobilities of electrons and holes [40]. This expression can be simplified when considering a layer where either holes or electrons dominate, which is most often the case. For a p-type layer, such as a boron diffusion, equation (28) would simplify to

$$G_S = \int_{x_1}^{x_2} q\mu_p p\, dx. \tag{29}$$

This integral is complicated by the fact that the mobility μ_p is concentration dependent, as shown in Fig. 10(a), and, therefore, varies with distance. For certain impurity distributions, where approximations by Gaussian or certain other distributions are valid and where peak concentrations are such that an effective constant mobility can be assumed, analytical expressions exist for calculating the sheet resistance with acceptable accuracy. However, by using numerical integration techniques the sheet resistance of arbitrary layers can be easily determined. At present the primary limitation in accuracy of simulated sheet resistance calculations is the availability of reliable mobility data and models. Fig. 10(b) indicates the complex interaction of the concentration dependent mobility and the phosphorus diffusion model [41]. Both the simulated junction depth and sheet resistance are shown as a function of phosphorus surface concentration for a fixed deposition time at 850°C in a phosphine partial pressure [41]. As surface concentration increases up to n_i, the junction depth increases and the sheet resistance decreases. However, above

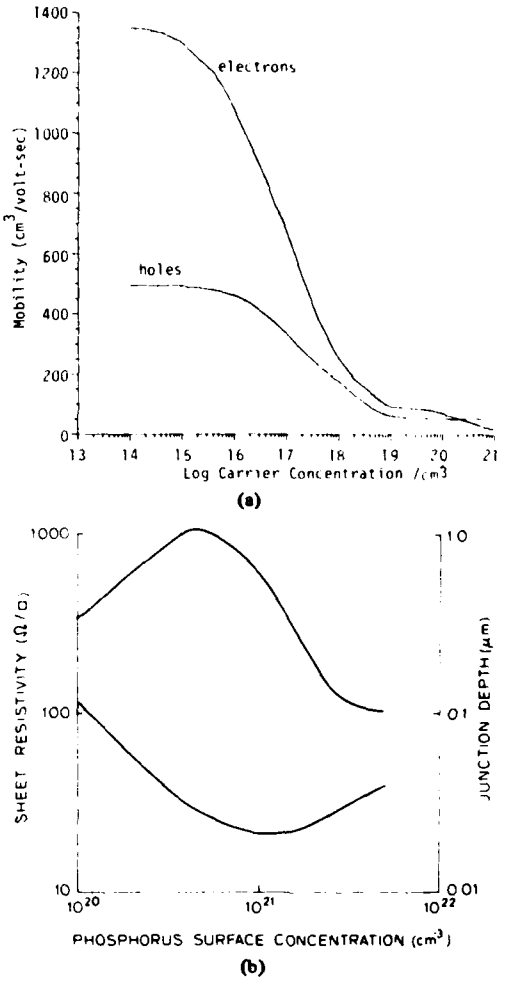


Fig. 10. (a) Plot of electron and hole mobilities in silicon versus impurity concentration. (b) Variations in junction depth and sheet resistance for a simulated phosphorus deposition at 850°C versus the surface concentration of phosphorus.

a concentration of about $1 \times 10^{21}/cm^3$, two effects become apparent. First, the mobility decreases rapidly as shown in Fig. 10(a). Second, the bandgap narrowing effects of the phosphorus model [7] become significant and the junction depth falls off. Both effects combine to give the results shown. This example clearly indicates the complexity of interaction of physical models and parameters such as mobility.

Sheet resistance is a valuable parameter in checking the status of the wafers while in process as well as determining aspects of the eventual device performance. The extraction of detailed impurity profile information requires much more time. For example, incremental sheet resistance measurements, where layers are sequentially removed, take several minutes per layer and the data becomes noisy for deep junctions and low concentrations [41]. On the other hand, spreading resistance is frequently used to obtain profiles, and data can be determined in less than an hour. In this case the data must be numerically corrected to obtain profile information [42]. Both incremental sheet resistance and spreading resistance, while useful are not routinely used in process control. The prediction and measurement of sheet resistance, on

the other hand, is invaluable. For this reason the capability to predict the sheet resistance and certain other electrical characteristics is an important addition to process modeling programs.

V. Device Applications for Complete Process Modeling

In the previous sections both the physical and numerical aspects of process modeling have been considered for the one-dimensional case—namely a vertical slice into the silicon wafer. Based on the availability of one-dimensional process simulation it is possible to consider a number of device applications. In this section a few of these applications are discussed in light of practical device structures. While the dominant emphasis to this point has been one-dimensional process effects, it will become clear from the examples that understanding the two-dimensional process effects is critical—especially for scaled-down MOS devices. In fact, this section will discuss MOS examples which motivate the further discussion of two-dimensional process modeling in Section VI.

A. Physical Dimension Control for Devices

For many applications, and as a practical matter of process control, the accurate knowledge of physical dimensions of devices is a major concern. In bipolar technology the epitaxial layer thickness and base width are two specific examples where dimensional control directly couples with electrical and process control factors. The modeling of these factors has been considered using analytical approximations [43], yet the advent of more accurate means to simulate impurity diffusion including the coupling of diffusing species now makes the correlation between process specification and resulting physically observable parameters a viable and valuable design tool. Fig. 11 shows the result of simulated and measured base-emitter profiles across a test wafer for a gas-phase predeposited phosphorus emitter bipolar process. In this case the process shows a rather extreme sensitivity to temperature gradients across the wafer because the deposition conditions are near a knee in the solid solubility curve [44]. Further investigation and experimentation revealed that ion-implanted emitters provide superior profile control as might be expected [45]. This basic approach has been demonstrated for other bipolar technologies [46]. Although bipolar technology has been scrutinized most carefully from the perspective of profile control, scaled MOS technologies have also become dominated by the need for strict dimensional control of impurities. For example, the double-diffused MOS (DMOS) technology, while not a contender per se for VLSI status, illustrates specifically the factors of junction depth and profile control as they affect device performance [47], [48]. In addition, as will be pointed out shortly, the source/drain junction depth of MOS devices directly impacts parameters such as threshold voltage and breakdown properties [49]. In a manner very similar to emitter junction depth control for bipolar, the control of shallow n^+ junctions as correlated to key process variables is a very important factor in NMOS design.

B. Process Dependence and Control of Electrical Parameters—One-Dimensional

There is a wealth of electrical parameters that can be controlled given an understanding of the one-dimensional impurity profiles. The most obvious parameters of concern to device designers include sheet resistance, junction capacitance, threshold voltage and gate capacitance for MOS devices. In addition to the parameters listed in the preceding, the dc components of current transport and recombination for bipolar devices are essential. Fig. 12 illustrates the physical relationship of the sheet resistance and junction capacitance to the doping profile for a double-diffused structure. The solution of Poisson's equation is used to determine depletion edges, both for zero bias and other conditions. This approach is sufficient to establish boundary conditions for either 1) integrating the active charge to obtain sheet resistance (perpendicular to the one-dimensional impurity slice, or 2) using total depletion layer width to extract capacitance.

In the case of MOS devices, the relationship of channel implant profile and threshold control has been carefully considered

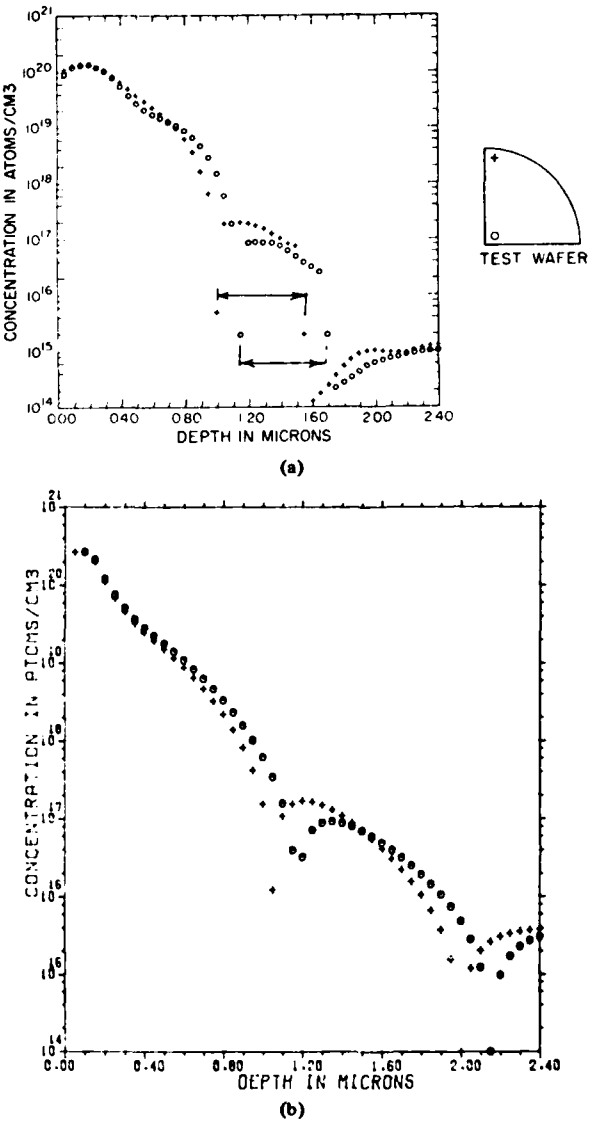


Fig. 11. Measured and simulated impurity profiles for a double-diffused phosphorus emitter bipolar process. (a) Corrected spreading resistance profiles across a quarter-wafer test chip. (b) Simulated profiles for the corresponding conditions and assumed process variations [44].

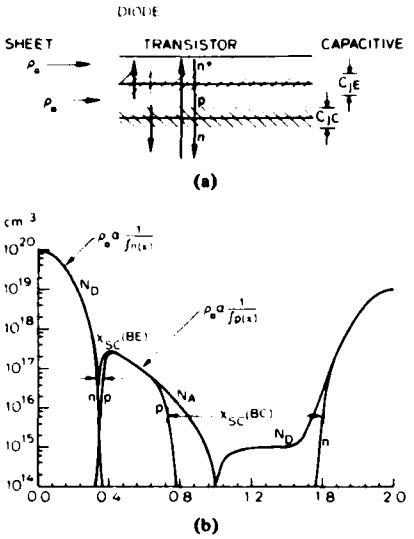


Fig. 12. Device parameters which can be obtained using one-dimensional process and device simulation. (a) Schematic view including: sheet resistance, junction capacitance, diode, and transistor transport currents. (b) One-dimensional profile with emphasis on the free-carrier profiles as they control sheet resistance and junction capacitance.

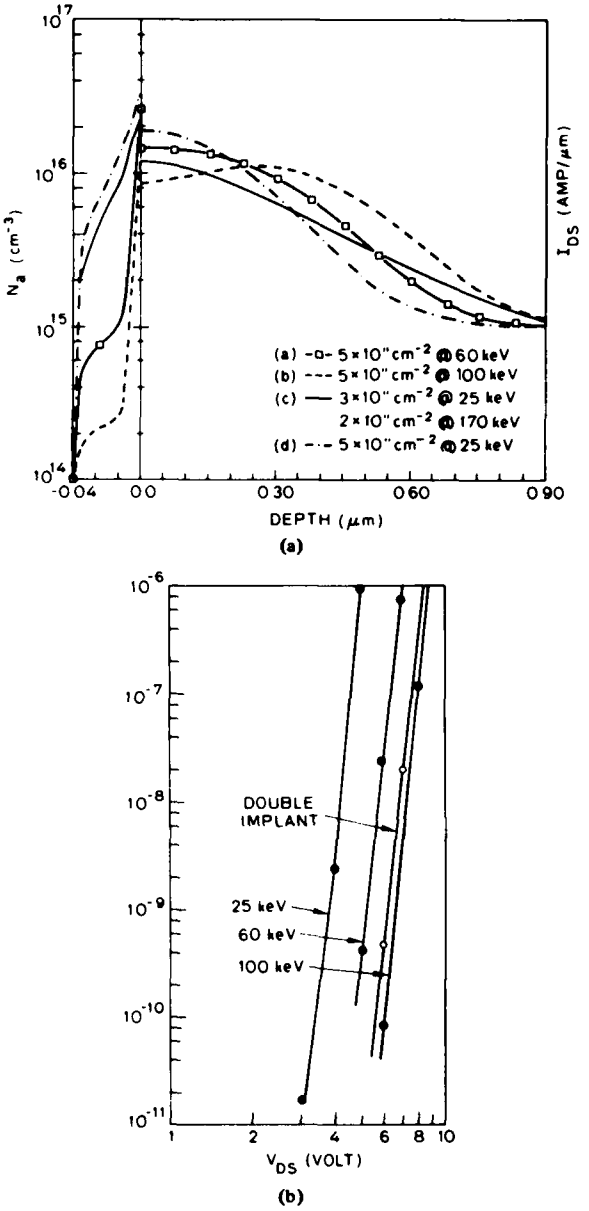


Fig. 13. Technology tradeoffs in choosing a channel implant for setting threshold in an NMOS device. (a) Several choices of implant dose and range conditions. (b) The resulting punchthrough curves of channel current with implant as a parameter.

[50]. The development of more complex channel doping schemes has continued and the need will be increased for tools to predict threshold sensitivities of more aggressive technology. Fig. 13 illustrates several implanted boron profiles used to obtain nominally the same threshold voltage. The primary difference between the approaches is the reduced subthreshold current obtained using the deeper implanted profile. Although the subthreshold characteristics involve two-dimensional effects, the clear dependence of electrical properties on the one-dimensional profile is an important aspect of the design process. In fact, the characterization of the boron profile using large geometry gate capacitance and MOS devices is a standard tool in process design.

As a final point, it should be reemphasized that many factors involving bipolar current transport can be characterized to first order based on one-dimensional approximations [51], [52]. As an important historical note it should be stated clearly that one-dimensional bipolar device analysis has been considered extensively [53]–[57]. Moreover, the direct coupling of process and device analysis was demonstrated using simplified analytical and numerical techniques [27]. Nonetheless, the process understanding and modeling during earlier investigations was not sufficiently accurate to match experimental results. Even now, the understanding of minority carrier and contact effects at a physical level limits our ability to model bipolar devices accurately. It is clear, however, that the coupling of one-dimensional process and device analysis for evaluation of transport and minority carrier currents in bipolar devices is a valuable tool in technology development [58].

C. MOS Device Parameters–The Two-Dimensional Modeling Frontier

As a final point for consideration, the problems of scaled-down MOS devices provide a focal point for applications of process modeling. As stated in Section I, the scaling of channel length causes two-dimensional effects to become dominant. The cross sections shown in Figs. 3 and 5 illustrate the role of topography in controlling the dimensions and lateral profile shapes in scaled NMOS. It is well known that the channel doping profile directly affects threshold voltage, subthreshold behavior and punchthrough [59]. The example given in Fig. 2 shows the role ot two-dimensional field effects on threshold. Namely, as the channel length becomes shorter, the two-dimensional field-effects from source and drain and their sensitivity to channel length dominate the threshold behavior.

The results presented in Fig. 13 have illustrated the profile effects on bulk punchthrough due to channel profile control. To illustrate the two-dimensional nature of profile sensitivities

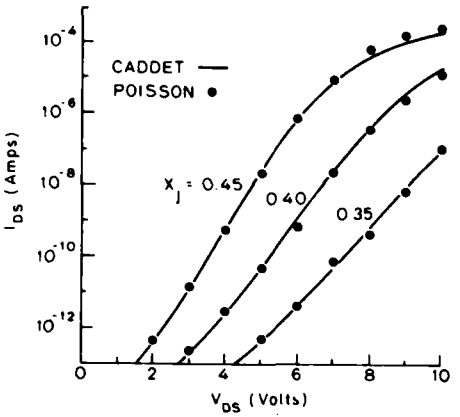


Fig. 14. Semilogarithmic plot of drain current versus drain voltage for a short-channel device under punchthrough conditions as a function of source-drain junction depth [59].

for punchthrough, Fig. 14 shows results of varying junction depth for a nominal one-micrometer channel length device. As stated in Fig. 3, the junction depth has a direct correlation with changes in effective channel length. The semilog plot of current versus voltage shows shifts of the order of hundreds of millivolts which correspond to order-of-magnitude shifts in current for a fixed gate voltage. These increased subthreshold currents are critical to the performance of dynamic circuits since storage is directly degraded by such leakage.

As a final illustration of impurity and topography sensitivities of scaled MOS devices, Fig. 15 shows the cross section, potential contours and calculated gate capacitance for a state-of-the-art NMOS device. It is clear from the device cross section and potential contours that it is impossible to describe the device adequately using a gradual channel approximation. Hence, the gate topology and junction profiles are intimately coupled to the device characteristics. As a result, the computed gate capacitance differs substantially from the idealized structure with a planar gate overlapping the source/drain regions. It is clear from this example that state-of-the-art MOS devices are highly two-dimensional and topography plays a dominant role in determining device characteristics. At this point it is appropriate to turn to the final section of this paper, the issues of multidimensional process modeling.

VI. Multidimensional Process Modeling

The preceding sections have placed emphasis on one-dimensional process modeling and application to device structures including highly two-dimensional field-effect devices. Indeed, the MOSFET threshold calculations involve Poisson solutions where the potential contour lines show that the classical gradual channel approximation is violated nearly everywhere. In addition to the two-dimensional device effects, the associated impurity profiles and topography of scaled-down devices are quickly becoming controlling factors. While it is feasible to extend one-dimensional process models to approximate some two-dimensional effects [59], [60], it is clear that for many general conditions of device fabrication, as reflected in Fig. 5, flexible and general tools for two-dimensional process modeling are required. The purpose of this section is to briefly review the status of two-dimensional modeling. The reader should be warned that this section in particular reflects an area which is rapidly changing.

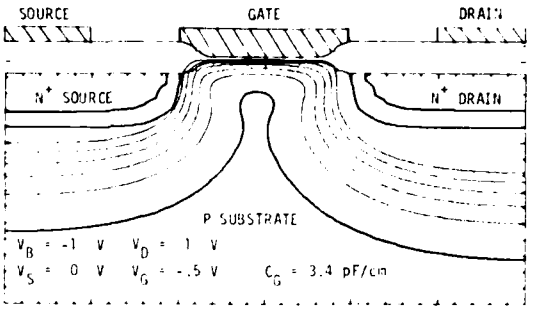


Fig. 15. Potential contours for an NMOS device, typical of that shown in Fig. 1(b), and the extracted gate capacitance using incremental bias solutions and integration of the depletion charge.

The device sections shown in Fig. 5 represent two aspects of two-dimensional process modeling—aside from the device analysis considerations discussed above. Topography and its modeling is essential for understanding a variety of fabrication limits including lithography, patterning, and step coverage. The advent of simulation tools in this area began in the late 1970's [61] and has quickly evolved into a major tool in process development—especially in the area of choosing equipment for lithography. Although it is beyond the scope of this paper to explore the variety of models and simulation techniques used for modeling topography, the reader is referred to several recent publications on this subject [62]–[64]. It is important to note the controlling influence of topography on both electrical and physical parameters of VLSI devices. One point to emphasize concerning topography modeling is the key algorithm used to model a moving interface. The string model represents a moving interface as a connected set of line segments (a "string"), which moves essentially as a Huygen wavefront throughout the process step—for all steps including development of photoresist, etching or deposition of layers and other steps which change topography. The beauty of this interface model is that it can be explicity moved to model a diversity of conditions, almost independently of the internal physics of the layer itself. However, redistribution within the layer or kinetics of interfaces are not explicitly handled by this approach at present.

We now turn to the more specific problems of modeling oxidation and impurity redistribution in two dimensions, as depicted in Fig. 5. Clearly the initial conditions for such a modeling problem are intimately related to topography. However, a more tightly coupled problem is involved because motion of the interface substantially affects the substrate redistribution of impurities. Moreover, the motion of the oxide interface depends strongly on both the interface doping and oxide shape. Although the effects of multispecies both in the oxide and in the bulk should be considered in the general case in fact there is no serious attempt reported to date where such an approach is being considered. The problems with such an approach are indeed much more complex than simply the number of variables—the understanding of two-dimensional kinetics is a totally new field. Figs. 16(a)–(c) show a number of recently reported methods for modeling the silicon/silicon-dioxide system in two dimensions. Each is now reviewed briefly.

Fig. 16(a) shows the conceptually simplest approach and also the most efficient method to model two-dimensional oxidation and impurity redistribution. Analytic solutions for low-concentration impurity redistribution under oxidizing conditions are well understood in one dimension [30], [65]

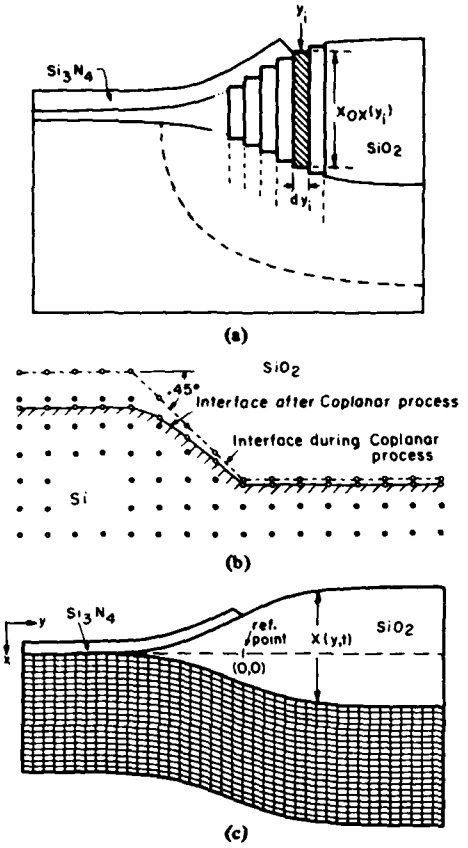


Fig. 16. Cross-sectional views of three representations for two-dimensional process modeling. (a) Analytic solutions have no grid but corrections for local oxidation are handled via superposition of slice-by-slice corrections [71]. (b) Numerical solution on a fixed substrate grid with analytical specification of oxidation and grid removal [67]. (c) Numerical solution on a transformed grid in the bulk where the interface is specified to be stationary [69].

and have been extended to two dimensions based on the superposition of infinitesimally thin vertical slices of impurity profiles and the subsequent redistribution under oxidizing conditions [31], [66]. The oxide correction is applied at each point x along the surface direction using basically a one-dimensional formulation for redistribution. In the analytical approach, as well as the numerical techniques which will be discussed next, the oxide shape and interface location is not simulated, but is instead specified based on measurements. For constant impurity diffusivity the analytic calculations agree well with numerically simulated results while computation time is nearly an order of magnitude less than for numerical simulation. It should be clearly pointed out that analytic solutions require no grid and directly calculate a final impurity distribution. On the other hand, the numerical techniques discussed later require allocation of grid points everywhere in space, and numerical computations with time increments sufficiently small so as to control the numerical errors.

Fig. 16(b) shows the grid used for a typical numerical simulation [67]. In this case a square grid is used and the interface between oxide and silicon is moved deterministically as discussed earlier. The grid motion is assumed to be vertical and diffusion in the oxide is neglected. The iterative solution method of Stone was used, similar to the case of device analysis [68]. There have been other numerical solutions of the more restrictive case of two-dimensional diffusion without a moving boundary [14], [16]. These last two numerical methods use a direct solution of the finite difference equations. The exact nature of the solution method is of less importance than the approximation of the oxide interface as being stationary with a fixed silicon spatial grid. These approaches are contrasted with the method discussed next.

Fig. 16(c) shows the transformed grid used to simulate local oxidation and impurity redistribution where the oxide-bulk interface is assumed to be stationary [69]. As discussed in all preceding methods, the oxide growth is a deterministic function based on experiments. The details of transformations and numerical methods are discussed elsewhere [69], [70]. The key difference between the approaches depicted in Figs. 16(b) and (c) is the added complexity in difference equations used for the transformation, whereas the interface specification becomes much easier. There is certainly great latitude to consider the most appropriate choice of analysis methods for two-dimensional process modeling.

In summary, the present status of two-dimensional process modeling is revealed schematically in Figs. 16(a)–(c). Both analytical and numerical techniques are actively being investigated, as are hybrid approaches [71]. It is too early to assess the impact of any particular methodology in the context of applications. However, it is useful to point out that two-dimensional profile determination is even more primitive than the simulation results discussed above. To conclude this section, a few experiments in two-dimensional profile measurement techniques are summarized.

The idea of test structures, especially for device modeling applications, is an old concept and IC manufacturers all use a variety of such devices. Many electrical test structures now can measure physical effect including layer-to-layer mask alignment [72] and doping effects in the bulk silicon [73], [74], to name just a few. Yet an even more specific set of test structures is now needed to characterize two-dimensional impurity profiles in a quantitative sense. A set of experiments which exploit threshold variations in the lateral dimension of narrow width (and long channel length) MOSFET's have been used to determine details of lateral surface profiles [66]. The technique was extended for a case where the narrow width controlling boron profile was moved by different mask distances away from the nitride LOCOS mask edge. Fig. 17(a) shows the cross section of the width dimension of such a patterned MOSFET with the channel dimension perpendicular to the paper. The Δx dimension was varied and the effective junction encroachment was measured electrically using the variable threshold method reported previously [75]. The rather surprising result shown in Fig. 17(b) is the fact that the boron diffusivity increases as the Δx dimension shrinks—bringing the local oxidation edge closer to the boron junction profile [75]. The result is consistent with independent physical measurements of junction depth as shown in Fig. 17(c). Here, a variable width nitride mask is used over a uniformly doped boron layer. Oxidation occurs between the masked regions, giving rise to the deeper junction depths as predicted based on oxidation-enhanced diffusion [76]. It is important to note that as the nitride pattern width shrinks, the enhancement under the nitride-covered regions increases, thereby indicating that indeed lateral effects of oxidation change junction depth. This is consistent with the results presented in Fig. 17(b). The overall impact of these results is

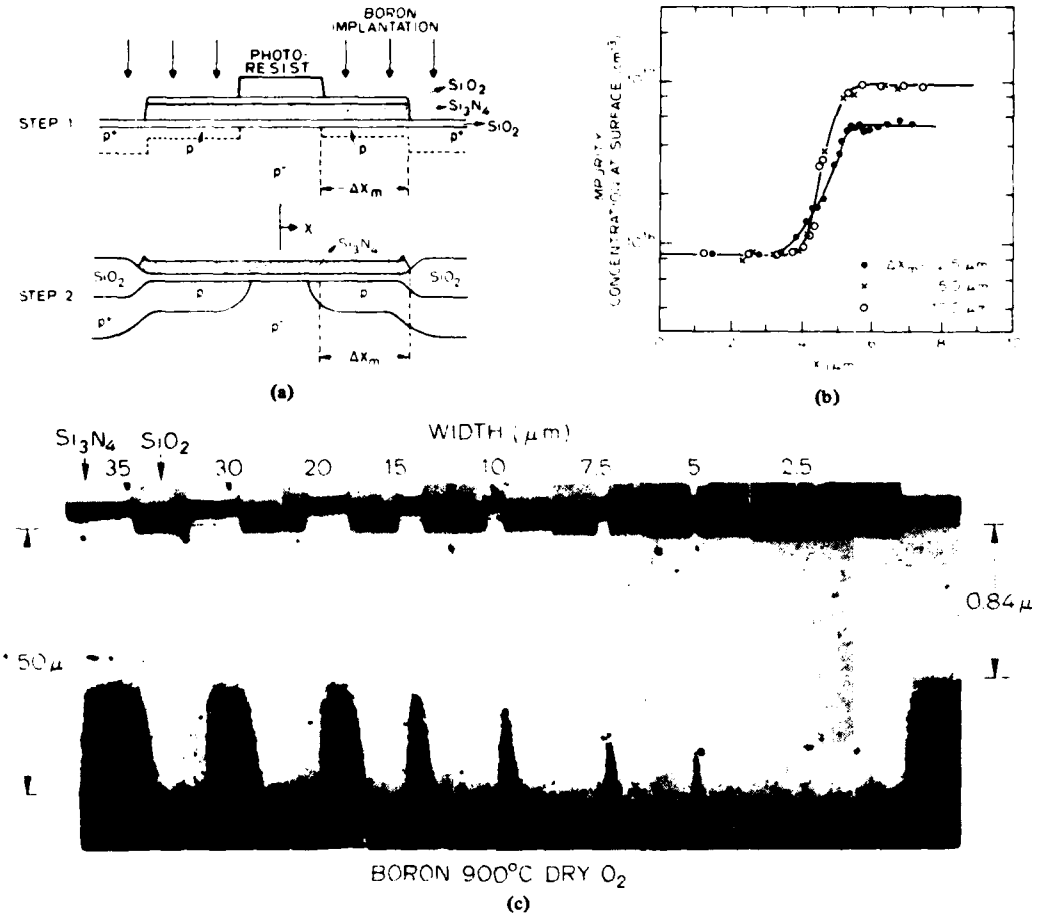


Fig. 17. Test structure results to confirm the lateral dependence of boron diffusion under local oxidation conditions [75]. (a) The cross-section of a narrow-width NMOS device and the Δx_m dimension is the separation between the boron implant edge and the local oxidation mask edge. (b) Extracted boron profiles as a function of lateral distance and using Δx_m as a parameter. (c) Stained junction depth for boron profiles both under a nitride mask and in a 100-μm oxidation window [76].

crucial from a device point of view. The characteristic dimension for these lateral effects is a few micrometers—yet this is exactly the dimension of current state-of-the-art VLSI devices. Hence, in fabricating and modeling device behavior, the detailed lateral profile effects must be carefully modeled and measured.

The preceding test structure approach uses threshold measurements which characterize surface profiles. A new set of results using junction capacitance and breakdown measurements of n^+ junctions near locally oxidized regions now reveals more explicit bulk effects of two-dimensional profiles on test structure results [71]. Fig. 18(a) shows the cross-section of a single finger of a junction capacitance structure which has been replicated many times laterally (with a 100-μm dimension into the paper) to form an array of junctions. Also shown on the plot are the depletion edges under breakdown conditions and the field lines with boxes denoting the actual breakdown points. Fig. 18(b) shows the one-dimensional slice of the impurity profile along the critical field line from Fig. 18(a). It is important to note that the breakdown point occurs when the depletion edge extends well past the region where the doping profile is linearly graded—thus invalidating simple analytic solutions of the problem. Fig. 18(c) shows the simulation and measurements of breakdown as a function of boron dose in the field region. The predicted and experimental curves show an excellent agreement. The results cannot be predicted based on simple theory owing to the complex bulk impurity profile. This particular example shows the power of coupling two-dimensional process and device simulators to compare with experimental results. Moreover, there is substantial interest in the coupling of computer tools and experiments from the practical perspective of device design.

VII. Conclusion

This paper has reviewed the field of process modeling of IC device technology. There has been considerable discussion and review of the motivation, including practical examples. A substantial portion of the paper considers one-dimensional process modeling. Both the physical and numerical aspects are discussed as are the applications. The vista of two-dimensional process modeling is now in sight and the field is moving rapidly. In a final set of comments, the growing role of test structures has been emphasized. The single most important conclusion of this paper involves a statement of need. As VLSI device dimensions shrink, the understanding and modeling of process kinetics

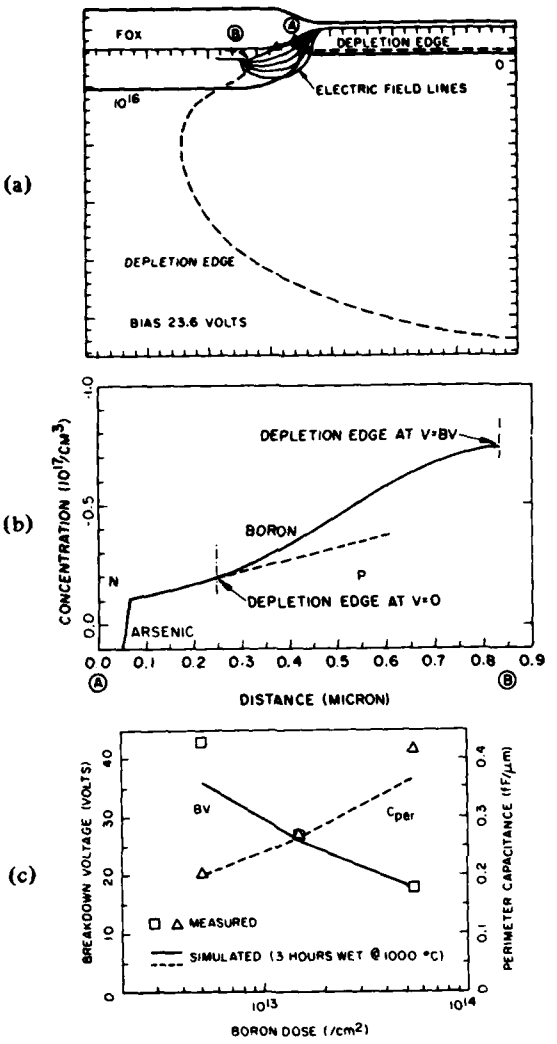


Fig. 18. Test structure results and two-dimensional simulations showing bulk impurity effects on breakdown voltage. (a) Cross-section of one finger of a breakdown test-structure [71] as modeled using both analytical and numerical techniques. (b) One-dimensional profile section near the field-oxide interface where breakdown occurs. (c) Breakdown voltage as a function of boron channel-stop implant dose, both measured and simulated.

become even more tightly coupled to two-dimensional device effects. The role of modeling in this area is growing and computer-aided-design tools are an essential media for both experimentation and application.

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Modeling of the Silicon Integrated-Circuit Design and Manufacturing Process

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Abstract—The evolution of process modeling is traced starting with bipolar technology in the 1960's through recent processing concerns for oxide-isolated MOS devices. The kinetics of diffusion and oxidation are used to illustrate both physical and numerical effects. The interaction of device effects with process modeling is discussed as well as the statistical implications of process variables. The nature of computer-aided design tools for process and device modeling are discussed. This includes tools that bridge gaps between technology and system design with potential application for manufacturing.

I. Introduction

THE FABRICATION and manufacturing of integrated silicon circuits has spawned a revolution equal in impact to that of the industrial revolution. This so-called information revolution differs substantially from the industrial revolution in its exploitation of computer-based technology in contrast to a technology focused primarily at mechanical advantage over the environment. On the other hand, the technology bases—steel and silicon—both require a sophisticated set of capital-intensive manufacturing techniques. The arsenal of silicon technology equipment in fact has a growing connection to metallurgy since the circuit design constraints which drive the technology are increasingly limited by interconnections—small metal lines; hence laser, ion, and other milling tools are now commonly used. However, the fact that active electronic elements are the primitive atoms of IC technology is the key driving force which separates this manufacturing endeavor from most other industrial technologies. It is the close interplay of the design of active transistor elements with the manufacturing technology which is the subject of this article.

Organization of the discussion which follows is intended both to chronicle the history and chart the future for IC manufacturing technology. The notion of process modeling will be introduced by means of examples related to bipolar transistor manufacturing. Next the features of MOS technology and the new concerns involved in modeling and manufacturing will be presented. Moving to the current issues of IC manufacturing technology, a discussion of state-of-the-art process kinetics will be given. Finally, the issues of CAD tools for both IC design and manufacturing will be summarized.

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II. Bipolar Technology and Process Modeling

The bipolar device technology dominated the decade of the 1960's while MOS technology was struggling with isolation and threshold control issues. Moreover, during this MSI era the off-chip drive capabilities of bipolar devices provided essential system leverage. From a production point of view the double-diffused technology dominated the high-speed market, with cut-off frequencies approaching 1 GHz. The desire to increase cut-off frequencies by shrinking base width led to a growing interest in emitter and base impurity profiles. During this period process models were developed in an effort to predict the process dependencies of double-diffused profiles [1]. Of special interest was the problem of push-out of the boron base impurity by heavily doped phosphorus emitters [2]. Although empirical models were developed and used [3], the dominant limitation of the modeling art arose from the lack of an adequate model for high-concentration coupled-species diffusion.

Fig. 1 shows the cross section of a typical double-diffused bipolar device along with one-dimensional impurity profiles in the emitter and base regions. A number of features of the device are apparent from the Fig. 1(b) and (c). First, the base-collector junction depth X_{BC} is different for the two regions. This indicates the fact that the boron diffusion is affected by the high-concentration phosphorus emitter. Second, the phosphorus profile exhibits a so-called "kink" in the high-concentration region of the profile. The implication of this kink on the resulting junction depths X_{BE} and X_{BC} as well as the base width X_B is of major importance in controlling electrical parameters of bipolar devices. Hence, the objective of process modeling is to provide basic understanding of the phenomena as well as engineering tools to assist in the design and process control during manufacturing. In the next few subsections the discussion will follow the evolution of one set of process models for bipolar device fabrication in order to demonstrate the tight interrelationship between the models and their application.

A. Models for Impurity Diffusion

The process of thermal diffusion of dopant impurities into a semiconductor is one of the key steps involved in creating integrated circuits. The dopant particles are charged and hence move by both diffusion and drift as

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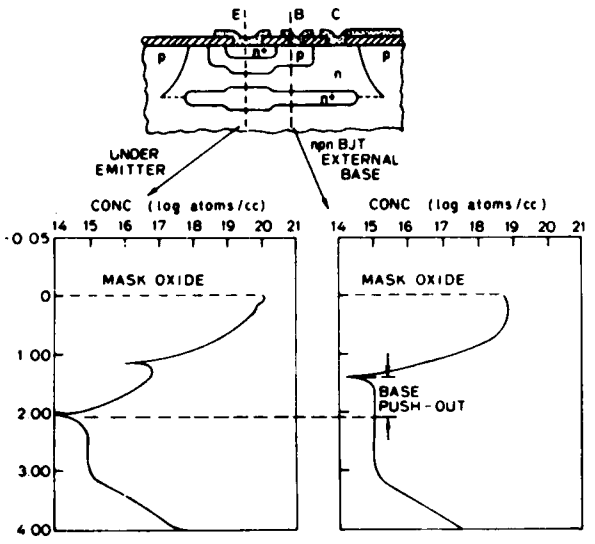


Fig. 1. Double-diffused bipolar transistor: (a) cross section, (b) impurity profile under the emitter, and (c) impurity profile under the base.

given by the flux equation for positively charged species

$$F(x) = -D\frac{\partial C}{dx} + \mu\mathcal{E}C \tag{1}$$

where D is the diffusivity, μ is the mobility, $\mathcal{E}$ is the electric field, and C is the concentration of active dopant impurities per cubic centimeter. The diffusivity and mobility obey the Einstein relationship so that

$$\frac{D}{\mu} = \frac{kT}{q} \tag{2}$$

where k is the Boltzmann constant and T is absolute temperature. The diffusivity is a thermally activated process so that its temperature dependence is of the form

$$D = D_0 e^{-E_a/kT} \tag{3}$$

where E_a is an activation energy—typically in the range of 3.4–3.6 eV [4]. The conservation of particles during the diffusion process dictates that their time rate of charge obeys the transport equation

$$\frac{\partial C}{\partial t} = -\frac{\partial F}{\partial x}. \tag{4}$$

It is the solution of this continuity equation for concentration versus both time and distance which is the basis for early process-modeling efforts. Two physical conditions are commonly used in the solution of (4): constant source and fixed dose impulse. Both boundary conditions are applied at $x = 0$.

The solution of the continuity equation for these two cases gives the following:

$$C(x,t) = C_s \operatorname{erfc}\left[\frac{x}{2\sqrt{Dt}}\right] \tag{5}$$

for the constant source value of surface concentration C_s,

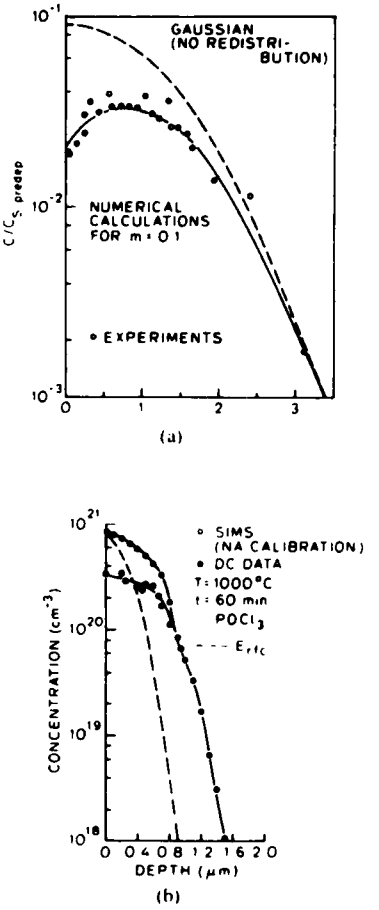


Fig. 2. Diffused impurity profiles: (a) boron [5] and (b) phosphorus [3].

and

$$C(x,t) = \frac{Q}{\sqrt{\pi Dt}} e^{-x^2/4Dt} \tag{6}$$

for the impulse dose Q per square centimeter.

The comparison of experiments with these two classical solutions—the complementary error-function and Gaussian forms—soon revealed that several physical effects altered the profiles substantially. For boron, although the diffusion process itself obeyed (1)–(4), the growth of an oxide layer at the surface during diffusion and the preference of the boron to be in silicon oxide rather than silicon give rise to the experimental results shown in Fig. 2(a) [5]. The segregation coefficient m is defined as follows:

$$m \equiv \frac{\text{Equilibrium impurity concentration in silicon}}{\text{Equilibrium impurity concentration in } SiO_2}. \tag{7}$$

Numerical solutions are typically required to properly correct for the impurity segregation; the best fit value of m is shown in Fig. 2(a). The figure also indicates that although the junction depth may well be predicted from (6), the peak concentration will be substantially incorrect. Since the total base doping and base width X_B will be determined by the surface concentration values, the difference between first-order models and experiment can be significant.

Fig. 2(b) shows the comparison between experiment [3] and (5) for a phosphorus diffusion. Clearly the results are not well represented by the complementary error function. Moreover, the two-region nature of the profile makes it difficult to use the equation even in an empirical sense for curve fitting since the sheet resistance will be controlled by the first portion of the profile whereas junction depth (hence X_B) will be determined by the profile tail. In order to provide even a qualitative agreement with experiment, a more complex set of diffusion kinetics are needed.

Although it is not the purpose of this article to consider diffusion theory in detail, the following discussion illustrates the level of sophistication required in order to provide suitable process models for IC technology. Three key aspects of the diffusion process can be illustrated for arsenic; similar phenomena also apply for phosphorus, boron, and other common dopants. First, the electrical carrier concentration affects the diffusion process. Second, diffusing species can change state and may become inactive [6] or alter the conditions which affect the other mechanisms [7]. Finally, the generation and consumption of point defects by the surface boundary alter impurity diffusion.

The carrier concentration effect on diffusivity can be represented in a general empirical form as [8], [9]

$$D = D + D^{-}\left(\frac{n_i}{n}\right) + D\left(\frac{n}{n_i}\right) + D^{=}\left(\frac{n}{n_i}\right)^2 \qquad (8)$$

where the various D's are superscripted to indicate components due to charge species, n_i is the intrinsic carrier concentration at the diffusion temperature, and n is the local concentration. To date the experimental evidence shows that for the p-type dopants (boron) the D_0 and D^{-} terms contribute whereas for n-type dopants such as phosphorus and arsenic, the D_0 and D terms dominate. Hence for arsenic the extrinsic diffusivity ($n \neq n_i$) can be represented by

$$D = D_0 + D\left(\frac{n}{n_i}\right). \qquad (9)$$

For n greater than n_i the second term dominates. Fig. 3(a) shows a comparison of calculated diffusion profiles assuming two different surface concentrations, one below n_i and the other substantially greater than n_i. Both calculations were made for the same time and temperature as indicated. From the figure it is clear that for increased n the diffusivity is enhanced substantially. Classical theory as given by equation (5) would yield a constant junction depth as reflected by the shallower profile.

At high concentrations, ($n \gg n_i$) the phenomena of clustering is hypothesized to remove arsenic from the diffusion process by forming energetically favorable collections of dopant. Current studies suggest that both solubility limits and electron concentrations affect clustering. One such equilibrium equation relating total number of atoms and active arsenic is given by [10]

$$C_T = C + mK_{eq}nC^m \qquad (10)$$

where C_T is the total concentration, C is the actively

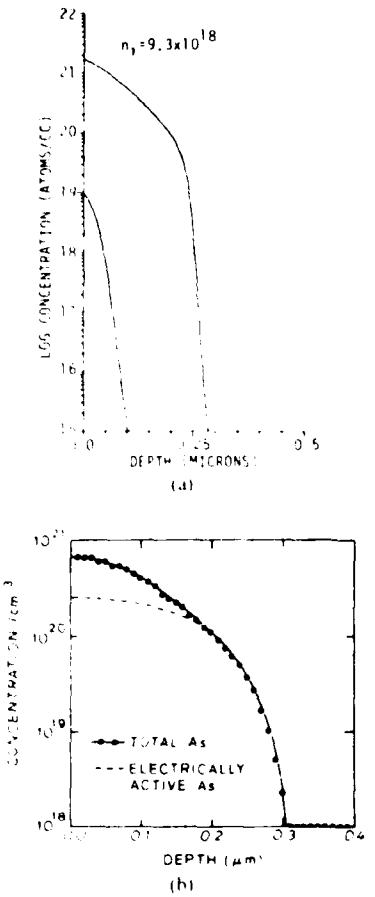


Fig. 3. High concentration diffusion effects: (a) numerical calculations based on (9) and (b) experimental results for arsenic [11].

diffusing dopant, m is the number of atoms per cluster, n is the electron concentration and K_{eq} is the equilibrium clustering coefficient. The results of the clustering are shown in Fig. 3(b) where the total arsenic, measured by Rutherford backscattering [11], as well as the electrically active portion of the profile are shown. The electrically active portion of the curve reflects a diffusion process given by (9) whereas the portion between the data and the dashed curve indicates the clustered portion given by (10). Although this discussion has been used to illustrate extrinsic diffusivity and clustering effects for arsenic, extrinsic diffusion phenomena are also observed for phosphorus and boron. Although recent reviews on the subject show phosphorus diffusion to be considerably more complex than the mechanisms considered earlier [7], an alternative approach considers phosphorus diffusivity to be controlled by the D_0 and $D^{=}$ components of (8) with another enhancement in diffusivity at lower concentrations owing to generation of extrinsic point defects [3]. This latter approach has the advantage of being practical from an engineering point of view and it has been used widely in computer programs for process simulation [12].

The final mechanism of primary importance in diffusion is surface generation and consumption of point defects.

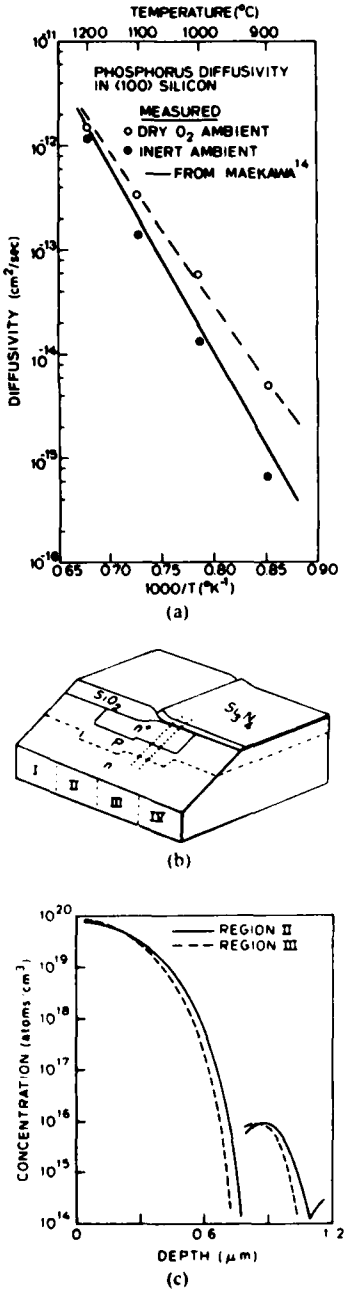


Fig. 4. Phosphorus diffusivity: (a) effect of oxidation enhancement (OED), (b) cross section of test structures, and (c) measured profiles with and without OED.

The oxidation of the silicon surface has been investigated as a generation source [13]. Fig. 4(a) shows the effect of oxidation on diffusivity of phosphorus in comparison to an inert surface condition. The semilog plot of diffusivity versus reciprocal of temperature shows that the difference between the boundary conditions is most pronounced at lower temperatures. This oxidation enhancement to diffusivity (OED) is experimentally determined to be related to the motion of the silicon dioxide interface. The difference in volumetric requirements for silicon in the SiO_2 and Si generate an excess of silicon determined by the oxidation rate according to the following empirical relationship [14]

$$\hat{C}_I = K_I \left(\frac{dX_{ox}}{dt} \right)^q \tag{11}$$

where $\hat{C}_I$ is the excess concentration of interstitial silicon, X_{ox} is the oxide thickness, K_I and q are empirical constants. The value for q is found to range between 0.4 and 0.6. The diffusivity enhancement is then written in terms of this excess concentration of interstitials as follows:

$$D = D^* + d_I \hat{C}_I \tag{12}$$

where D^* is the extrinsic diffusivity as discussed previously and d_I is a proportionality constant. Although the details of kinetic effects involved in oxidation-enhanced diffusion are a subject of great interest and investigation for their own sake, the implications for device fabrication are indeed important. The technology trends toward lower-temperature processing and high-pressure oxidation both directly affect the OED and hence junction depths and electrical parameters. Both phosphorus and boron show similar trends in OED effects. Fig. 4(b) shows the cross section of an experimental structure used to investigate both OED and coupled diffusion effects for boron and phosphorus [15]. In region III the phosphorus enhances the boron diffusion compared to region IV. In region II the surface is oxidized and, as can be seen in Fig. 4(c), both the boron and phosphorus diffusion is enhanced. Fig. 4(c) compares the spreading resistance profiles in regions II and III. A more extensive discussion of OED and other point-defect mechanisms involved in diffusion is given elsewhere [14].

In summary, the generation of point defects is a major effect in altering diffusion. Moreover, the use of local oxidation for both bipolar and MOS device isolation suggests there is a need to understand two-dimensional device implications as well as the one-dimensional surface kinetics.

B. Effects of Impurity Profiles on Bipolar Devices

The previous subsection has considered the phenomena involved in impurity diffusion and rudiments of the process models used to describe the one-dimensional impurity distributions. In this section the implications of these impurity profiles on device behavior are discussed. As stated at the beginning of this section, the tight processing tolerances in the vertical dimension for bipolar technology are responsible for advances in process modeling during the 1960's.

Both the dc and ac parameters for bipolar devices are tightly linked to impurity distributions. Junction capacitances are directly related to impurity profiles and the statistics of electrical variations with process sensitivities have been studied [16]. The dc parameters such as current gain and base transport current show the greatest sensitivity to process variations. Two physical factors account for this sensitivity and the increased difficulty in modeling the

electrical parameters directly from process models. First, the base width is extremely sensitive to the high-concentration emitter diffusion as well as the coupling of base and emitter profiles. As discussed in Subsection II-A, the complete set of kinetic effects in this regime of processing physics is indeed complex. Second, the base current, which directly affects current gain, is a function of both the emitter profile and minority-carrier recombination phenomena.

The problems associated with process modeling of the emitter profile have already been discussed. Considerations of minority-carrier effects in the emitter have resulted in improved models for carrier recombination as well as bandgap narrowing [17] which alter both the recombination and injected minority-carrier densities. Present trends in bipolar technology now emphasize polycrystalline emitter structures, both as a diffusion source [18] and to provide self-aligned contacts [19]. The exact role of this multilayer emitter is a current topic of investigation, and it appears that both interface phenomena [20] and impurity profile effects in the emitter [21] affect base current. Recent experimental evidence indicates that while the interface transport shows reproducible characteristics, the tight coupling of impurity diffusion and minority-carrier transport effects requires detailed knowledge of both in order to provide a first-principles model for base current [22]. In addition, recent efforts to model polysilicon diffusion effects have resulted in new simulation capabilities for multilayer systems [33].

While it has not yet been possible to model bipolar current gain directly from the specification of process variables, the modeling and characterization of the base transport has been a useful engineering tool. The well-known Moll-Ross relationship [23] defines the key variables involved in understanding the process sensitivities of the current transported between emitter and collector

$$I_{CE} = I_S\left(e^{qV_{BE}/kT} - e^{qV_{BC}/kT}\right) \tag{13a}$$

where

$$I_S = \frac{qAn_i^2}{\int_0^{X_B} N_A(x)\,D_n\,dx} \tag{13b}$$

and A is the emitter area, D_n is the electron diffusivity, $N_A(x)$ is the base doping profile, and X_B is the base width. It is clear from this equation that the integral quantity is the dominant process-dependent variable; it is controlled by both the impurity distribution $N_A(x)$ and its spatial extent X_B. During the 1970's it was found that the correlation of the pinched-base resistance[1] and I_S was an excellent means by which to monitor process control in bipolar device fabrication [24]. More recently, correlation of I_S directly with fabrication variables has shown the key role of both the integrated dopant concentration and subsequent thermal processing.

[1] The pinched base for an n-p-n bipolar device is the p-type resistance layer vertically bounded by emitter and collector n-type regions—essentially a JFET with emitter and collector as gate.

TABLE I
EFFECT OF EMITTER PREDEPOSITION TIME ON THE ELECTRICAL CHARACTERISTICS

Emitter Predeposition Time	Pinched Base Sheet Resistance	β_{max}	I_s	C_{JCO}
(min)			A	pF
31.35	11.4 K Ω	170	1.4×10^{-15}	.182
33	12.3 K	260	3.2×10^{-15}	.179
36.65	11.7 K	410	1.2×10^{-14}	.178

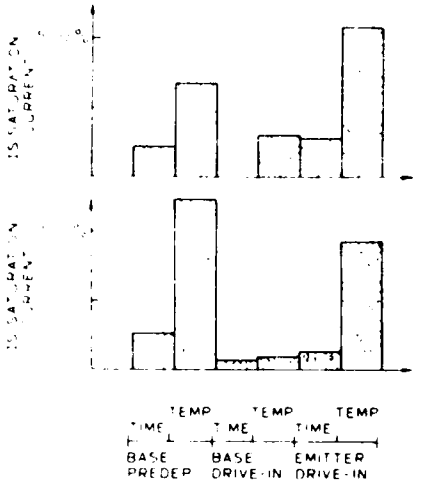


Fig. 5. Comparison of process sensitivities of saturation current for a bipolar device (top) chemical phosphorus source, (bottom) ion-implanted emitter.

A conventional double-diffused process using $POCl_3$ predeposition shows an extreme sensitivity of both I_s and current gain to predeposition time as indicated by the simulated results in Table I. By comparison, the base-collector zero bias capacitance, CJCO, shows no sensitivity to this emitter process variation. The tightly coupled emitter and base profiles do not substantially alter the base-collector junction gradient. In order to overcome these process sensitivities, ion implantation is used to accurately control the total dose of boron and phosphorus and to reduce sensitivities to subsequent thermal cycles. Fig. 5 compares the sensitivity of I_s to variations in time and temperature for the ion-implanted process compared to the "standard" chemically predeposited process. Both processes were designed to have similar vertical junction depths and maximum dc current gain. For variations of 1 min of time on all steps and 5 degrees in temperature, the resulting percentage variations in I_s are shown. Clearly the temperature for the base predeposition and emitter drive-in temperatures has the greatest impact—the ion-implanted process shows a five-fold reduction in sensitivity to the latter variation. In addition, the sensitivity to time variation is dramatically reduced for the ion-implanted process. As a final point, Fig. 6 compares the measured current gain versus collector current for the two processes. As can be

and

$$\tau = \frac{x_i^2 + Ax_i}{B}$$

for an initial oxide thickness of x_i.

The basic relationship given in (16) has proved to be an invaluable process model. A variety of ambient effects can be accounted for by changing the coefficients A or B. Dry oxidation, steam ambient, and even partial pressures of HCl have all been modeled in this way. Moreover, the change in dopant concentration in the silicon has been shown to affect oxidation rate, and this too can be accurately represented by changes in the appropriate coefficients. The following equations illustrate the nature of one such empirical formulation [31] which accounts for these doping-level-dependent kinetic effects

$$\frac{B}{A} = \left(\frac{B}{A}\right)\left[1 + \gamma(C - 1)\right] \tag{17}$$

where

$$C = \frac{1 + C_1\left(\frac{n}{n_i}\right) + C_2\left(\frac{n}{n_i}\right) + C_3\left(\frac{n}{n_i}\right)^2}{1 + C_1 + C_2 + C_3}$$

and

$$\gamma = 2.62 \times 10^{7} \exp\left(\frac{1.10\text{eV}}{kT}\right).$$

Hence, the linear growth rate term is directly affected by the concentration of vacancies, which is in turn controlled by carrier concentration—much as dopant diffusivity.

The scaling of MOS devices has resulted in three important trends related to oxidation effects. First, the growth of thin dielectrics for the gate region has become a critical factor. Second, growth of locally oxidized regions controls device spacings. Finally, the redistribution of impurities in all regions of the device—channel, junctions, and isolation regions—affect performance. Examples of advances in modeling in each of these areas are now presented.

The growth mechanisms for thin oxides is a topic of great interest, and a definitive first principles model is still to be developed; however, recent experiments involving *in situ* characterization of oxide thickness versus time have revealed new insight. Fig. 10 shows data of oxidation rate versus oxide thickness for two orientations of the silicon surface. In contrast to the thick oxide regime, the growth rates for thin oxides show sharp increases for short time and thin layers. The enhanced oxidation rate is clearly evident from Fig. 10. An extensive collection of data reveals that the oxidation rate can be adequately modeled using the following empirical formula [32]:

$$\frac{dx_{ox}}{dt} = \frac{B + k_1 e^{-x/L_1} + k_2 e^{-x/L_2}}{2x + A} \tag{18}$$

The first term is the conventional dependence as reflected in the differential form of (16). The second two exponential terms involve exponential decaying functions, dominant in the 20- and 200-A regimes of oxide growth, respectively. The pre-exponential coefficients show different Arrhenius plot behavior which may reveal information on the mechanisms responsible for both the ultra- and very-thin oxide growth mechanisms [32]. From a more practical viewpoint, a single exponential dependence using the spatial rather than time variable can be used to modify the B/A coefficient and give an excellent fit to data for oxides greater than 50 A. Combining the thin-oxide and heavy-doping effects in a single expression gives the following equation

$$\frac{B}{A} = \left(\frac{B}{A}\right)_i \left[1 + \gamma(C - 1)\right]\left[1 + k_1 e^{-x/L_1}\right] \tag{19}$$

where the heavy-doping term and thin-oxide terms are easily identified. The term loosely denoted as a product over the ith other effects suggests that partial pressure orientation, chlorine ambient effects—to mention only a few—must also be accounted for. A more complete discussion of the present understanding related to these other effects is presented elsewhere [4].

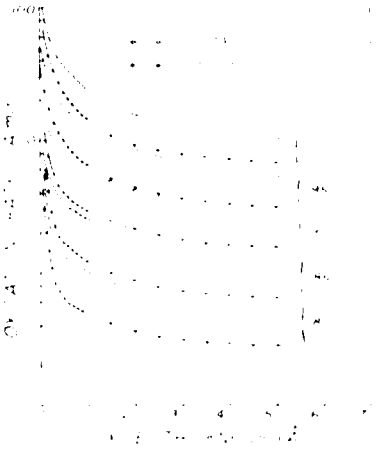


Fig. 10. Oxidation rate versus thickness for thin oxides [32].

As one can see from the previous discussion, the kinetics of oxidation are intimately tied to electrical activity in the substrate, ambient conditions, and even mechanisms within the layer itself. As stated at the beginning of this section, local oxidation (LOCOS) is a key component of modern MOS technology. Yet the growth of LOCOS results in still other kinetic effects beyond those described earlier. Fig. 11(a) shows the simulated cross section of a LOCOS structure during oxidation where the two-dimensional motion of the oxide elements is shown as well as the constraining nitride layer which exerts a normal stress. The arrows in the figure indicate oxide motion during growth. Note that because of the nitride stress, the oxide moves laterally out from the masking layer. Fig. 11(b) shows the measured cross section of the sample simulated from Fig. 11(a). The "bird's beak" and head are reflections of both the stress and flow as simulated. A full discussion of the two-dimensional kinetics is complicated. However, three key points should be mentioned. First, the concentration of oxidant C satisfies the two-dimensional Laplace equation

$$D\nabla^2 C = 0. \tag{20}$$

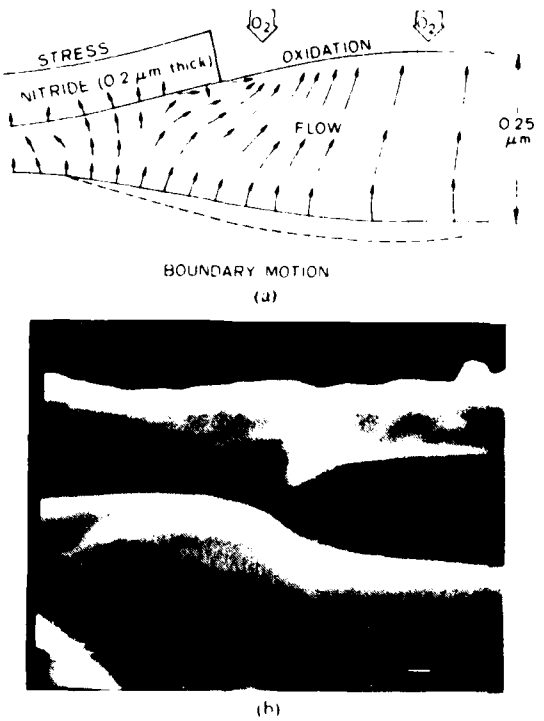


Fig. 11. Simulated and measured local oxidation cross sections: (a) numerical results showing key variables and (b) electron microscope picture.

Second, the oxide moves slowly and behaves as an incompressible fluid described by

$$\nabla \cdot V = 0 \tag{21}$$

where V is the velocity of oxide element.

Finally the boundary conditions involve both pressure and velocity and are mixed. The overall governing equation is a simplified form of the general Navier–Stokes hydrodynamic equation

$$\mu \nabla^2 V = \nabla P \tag{22}$$

where μ is the viscosity and P is the pressure. The velocity at the oxide–silicon interface is given by

$$V = (1 - \alpha) \frac{k_s C}{N} \hat{n} \tag{23}$$

where α is the volume ratio of consumed silicon to created oxide (0.473), k_s and N are given in (14c) and (15). The two-dimensional solution of (21) and (22) requires iterative numerical techniques and is discussed elsewhere [34]. The key point to emphasize is the fact that the LOCOS structure imposes a more complex physical set of constraints on the kinetic models than the one-dimensional case. Indeed, the trends in kinetic models for IC processes as discussed in Section IV indicate the overall importance of advances in this kinetic understanding and the need to push further in these models to keep pace with present and future device technology.

Having discussed both the basic one- and two-dimensional kinetic models of oxidation as well as selected features involved in second-order phenomena, let us next consider the electrical effects on MOS devices.

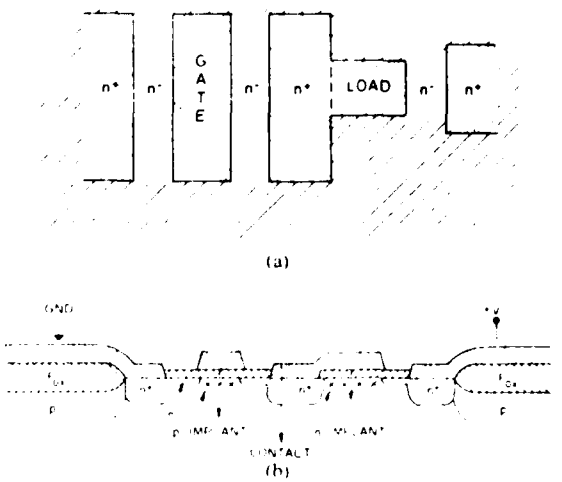


Fig. 12. NMOS Inverter (a) plan view and (b) technology cross section.

B. Effects of Oxidation and Lateral Diffusion on MOS Devices

The basic operation of the MOS device involves field effects imposed by electrodes on doped regions of the silicon. Hence the two- and even three-dimensional solution of Poisson's equation, using the correct oxide topography and selective dopings in the substrate, is essential in understanding both the devices and their sensitivities to fabrication technology. Fig. 12(a) shows the plan view of an NMOS inverter [35] and Fig. 12(b) shows the technology cross section of the enhancement and depletion devices as well as the nature of the LOCOS isolation regions. In the examples which follow, the sensitivity of several device parameters to the underlying process variables are discussed. In most of the cases the process variations lead to two-dimensional effects. Although limited success has been realized in test structures and other measurement tools for these effects [15], further technology development will dominantly use two-dimensional device simulations to correlate with electrical effects. The simulations most clearly show the dominant effects and in fact have facilitated initial attempts to extract process-related device parameters similar to the bipolar quantities such as I_s which have been discussed in Section II.

Fig. 13 shows the well-known curve of threshold sensitivity (simulated) with channel length along with experimental data. The spread in δL along the channel-length axis is the same at all channel lengths, but the resulting δV_T increases dramatically for shorter channel lengths. Fig. 14 shows simulated punchthrough threshold curves for the 1-μm channel length device. A variation of 10 percent in junction depth, for a fixed channel length, results in an order of magnitude change in current at a fixed V_{DS} [36]. Although the gate patterning is the dominant factor [37]

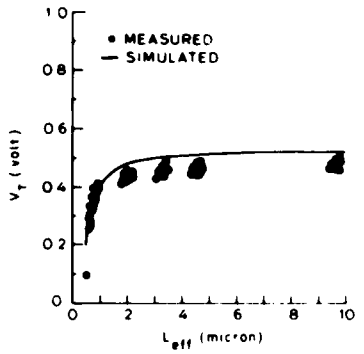


Fig. 13. Threshold voltage versus channel length.

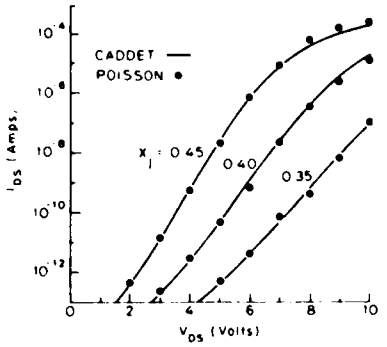


Fig. 14. Punchthrough current versus drain voltage for a nominal 1-μm channel length device.

affecting the short-channel variations in threshold, it is clear that vertical dimensions—directly changed by oxide etching and OED—have a substantial role at micrometer device dimensions. Both Figs. 13 and 14 show extreme sensitivities of electrical parameters to physical parameters for short-channel MOS devices.

Turning to the depletion load we can observe critical mask and process sensitivities for this narrow-width device [35]. Fig. 15(a) shows the impurity and LOCOS oxide profiles for a nominal masked 4-μm-wide depletion device. Also shown with dashed lines on the figure is the calculated depletion edge. The depletion edge reveals two facts: 1) the narrow-width threshold for this device is quite different from short-channel effects due to the shape of the lateral boron diffusion; and 2) the region of strong inversion is noticeably smaller than the masked 4-μm dimension due to both oxide and dopant encroachment. Fig. 15(b) shows the simulated bias dependence of available channel charge for the depletion device as a function of masked device width. While the extrapolated negative threshold shows minor variations, the slope for $\pm$1-μm variations is dramatic. The large change reflects the dominance of the LOCOS encroachment including diffusion especially for reduced widths. This example illustrates the need to develop new isolation methods for reduced-dimension devices. Moreover, the need for 2D oxidation and diffusion modeling has now become critical as we continue to reduce device dimensions.

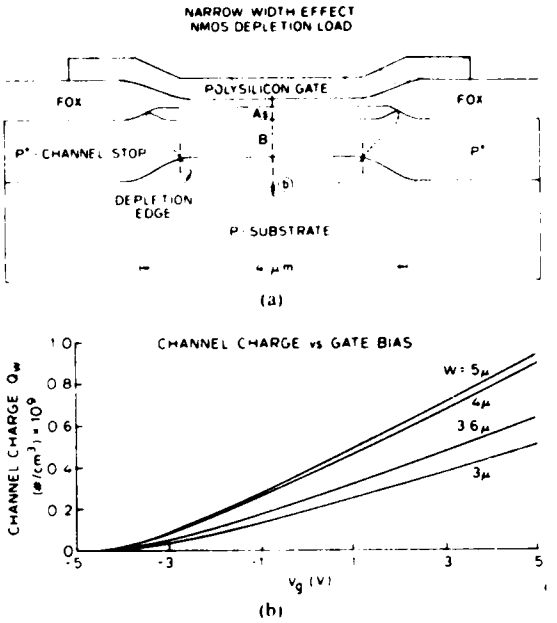


Fig. 15. NMOS depletion load: (a) technology cross section including depletion edge and (b) simulated channel charge versus bias.

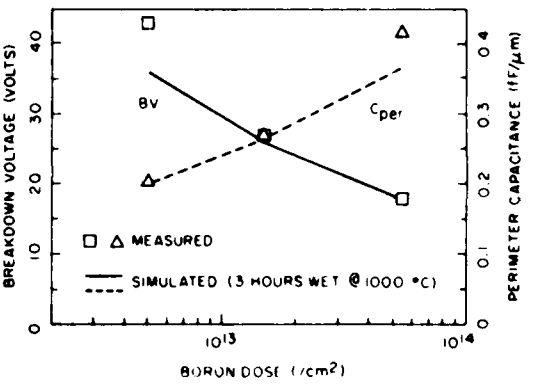


Fig. 16. Simulated and measured sensitivity of breakdown voltage and perimeter capacitance versus field implant dose.

As a final example in this section, consider the trade-offs to be made at the drain edge of the LOCOS region. Electrical factors include sidewall capacitance, breakdown, and leakage. From a structural point of view, the surface planarity and lateral bird's beak encroachment must be balanced with problems such as defect generation in the substrate. Fig. 16 shows the simulated and measured trade-offs to be considered in choosing boron dose in the field region [38]. The results show that over more than an order-of-magnitude change in dose, the capacitance can be reduced while continually increasing the breakdown. Obviously the field threshold must be factored into this analysis as well. Based on these experiments, the following empirical relationships are obtained:

$$BV \alpha (\text{dose})^{1/3} (X_{ox})^{0.75} \tag{24a}$$

$$C_{per} \alpha (\text{dose})^{+1/3} (X_{ox})^{0.75}. \tag{24b}$$

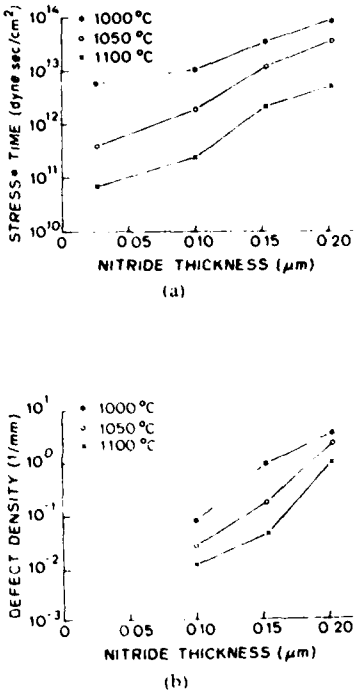


Fig. 17. Correlation between stress and defect density as a function of nitride thickness: (a) (stress) × (time) integral versus nitride thickness, and (b) measured defect densities.

These dependences are not immediately apparent from any first-order calculations [38]. However, the coupled 2D process and device analysis to be discussed in Section V clearly reveals these important design relationships. It should be emphasized, much as for the narrow-width depletion load, that the two-dimensional doping profile effects dominate the device performance.

While the previous example has emphasized the diffusive portion of the LOCOS step, the oxide growth itself plays a major role in determining circuit yields. In particular, the parameters such as pad oxide and nitride layer thickness used for the LOCOS directly affect defect generation. Recent simulations based on the model discussed in Subsection III-A reveal the correlation of calculated integral of stress and measured defect densities versus the nitride thickness as shown in Fig. 17. The trends show that factor-of-two changes in nitride thickness result in more than an order-of-magnitude increase in defects. Similarly, increased oxide-growth temperature reduces stress and defect generation [39]. This final example again illustrates the utility of modeling in the formulation of a design approach over a broad range of physical conditions.

IV. Trends in Processing Technology

The previous sections have presented an historic view of technology modeling. The phenomena of diffusion have been discussed, primarily from the perspective of bipolar technology. The modeling of oxidation has been driven by the MOS technology—especially the need for local oxidation to produce densely packed devices separated by oxide regions. These processing trends have illustrated the fundamental concerns and motivation for process modeling. The purpose of this section is to briefly provide a broader long-range perspective on the future trends of IC processing.

The equipment required to fabricate submicrometer-dimension devices has advanced rapidly over the past decade. In particular many new pieces of equipment have been demonstrated to anneal, deposit, and etch films for a variety of silicon-compatible materials. The technology objectives related to each of these process steps is now considered.

Annealing originally referred to a process step which produced a positive device effect, the activation of implanted impurities, or the final alloying of an ohmic contact, for example by modest cycles in temperature and ambient. The present technologies for laser, pulsed light, or other beam processing have resulted in well-controlled temperature transients. The materials effects are indeed profound, ranging from solid-phase epitaxy through nonequilibrium creation of silicide materials. In addition the controllable growth of silicon on insulators (SOI) is likely to eliminate the need for the sapphire substrate used in SOS. The opportunities to completely alter the nature of thermal processing in silicon technology seem vast indeed [40]. The trends toward lower processing temperatures and the use of materials which are sensitive to surface interface reactions favor the nonequilibrium approach. From a process-modeling point of view, these new technologies pose a substantial challenge. The radiation effects result in short time-scale events driven by sharp transients and extreme temperature gradients. The activation of point-defect mechanisms as well as intrinsic concentrations seem to be altered substantially by beam processing. In short, the new techniques for annealing involve highly nonequilibrium events which occur over very short time periods.

The use of deposited films in silicon technology has grown rapidly in the past few years. Low-pressure deposition techniques in particular have experienced a phenomenal growth. In addition to the common dielectric materials—silicon dioxide and silicon nitride—both silicon epitaxy [41] and contact metallization [42] are benefiting from new deposition techniques and equipment. Silicon epitaxy is an especially exciting area from the device point of view since many desirable device effects can be altered by epitaxy. Emitter efficiencies for up-operated bipolar devices can be improved and latchup sensitivities for CMOS reduced, for example. The key concern, however, has been the defect generation properties during growth, and control of thickness and electrical parameters. Trends show favorable progress toward better control of the parameters and defects, suggesting that the use of epitaxial layers is likely to increase in the future. In the area of metallization, the need to reduce contact resistance and control interdiffusion suggest that more versatile deposition techniques are needed. The use of deposited polysilicon layers for improved contact properties and reduced junction depths have been

discussed earlier in the context of polycrystalline bipolar emitter effects. The successful demonstration of selective CVD deposition of refractory metals [42] suggests one very positive trend in the direction to control MOS contact properties although vacuum-deposition techniques are likely to dominate for several years to come. As discussed shortly, the controlled etching of surfaces plays a key role in all IC processing, and certainly for metallization the interface properties are a factor of key concern in reliability and reproducibility. In the area of both metallization and dielectric materials, concerns with step coverage are crucial. For metal one must avoid openings due to thinning over steps while in the case of dielectrics it is essential to get good coverage over corners to increase breakdown and improve reliability. In summary, the role of deposition in lower-temperature processing is indeed important, and the need for process models in this area will continue to grow. Both dielectric and conducting layers are benefiting from new deposition techniques, especially those utilizing low-pressure equipment. Although it is too early to identify the leading approaches to selective deposition, the possibilities are quite attractive.

The final area suggested for special consideration is etching. The critical role of technology advances in this area cannot be overstated. The control of gate dimensions and edges for MOS is a direct result of etching. New oxide isolation techniques use careful control of steeply etched trenches [43]. Even for steps without specific spatial constraints, the end point detection of etching can be crucial to device reliability and defects created during subsequent thermal processing. Despite the critical dimension constraints of etching, both lateral and vertical, the kinetic effects involved are more complex than any other step in the fabrication process [44]. Fig. 18 shows the cross section of a hypothetical structure during an etching step and a few of the possible mechanisms involved in the etching which results in the observed convex-curved surface. The set of events can range from electronic and ionic bombardment of the surface to surface migration and desorption of reactants and products. Most etching techniques presently use several reactants including fluorine, chlorine, and oxygen as key active ingredients. For example, a typical etching process for silicon might involve $C_2F_6 + Cl_2$. There is a wide range of intermediate reactions occurring in the etching process as indicated in Fig. 18. Moreover, the role of bombardment and surface kinetics is not generally included in the normal rate equations. These "ambient" and surface effects will further complicate the kinetic picture. Since patterning is the dominant driving force in achieving smaller devices, it is this technology which is expected to undergo the greatest advances in equipment technology -- and hence be the most in need of improved process models. A further discussion of the device implications related to etching is given elsewhere [45].

In the previous discussion, I have emphasized annealing, deposition, and etching as key trends in processing technology. In particular, it is these areas in which new equipment

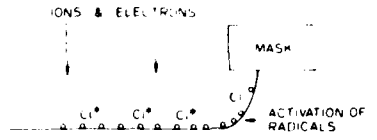


Fig. 18. Cross section of a wafer during etching and mechanisms and species involved in the kinetics

will shape the directions of device fabrication, and hence new process models will be needed to keep pace with process design and control. As pointed out in both Sections II and III, the statistics of device characteristics depend critically on some aspects of the fabrication process. In the examples cited above, the doping profile sensitivities for the bipolar base region and the controlling factors of channel length and source drain junction parameters for MOS have been demonstrated. Looking toward the next decade of IC technology, the lateral dimensional control of etched lines and electrical properties and integrity of thin layers will dominate process control concerns. In this spirit the trends related especially to deposition and etching will become more apparent. The use of recrystallization and special annealing techniques for multilayer interconnects and even active devices [46] is an area which is receiving increased attention. Moreover, the opportunities for innovative device structures in SOI will continue to be an exciting area for research [47]. In this field the concerns with the basic properties of oxides, interfaces and impurity diffusion again become first-order effects, much in the spirit discussed in Sections II and III.

Two areas of intense industrial activity and practical implication are lithography and multilayer metallization. The need to pattern fine lines prior to etching is crucial to the device scaling efforts. The issues involved in this area are substantially different from the silicon-based materials kinetics discussed here. The interested reader is thus referred to [48], [49]. Similarly, in the area of metallization for multiple levels of interconnect, the concerns move more into the fields of packaging and even organic chemistry than thermal processing which affects the silicon. Again, the reader is referred elsewhere [45].

A final overview of both the process modeling as well as new trends discussed in this section is presented in Table IV. The dominant process steps for which process modeling is currently an active field of endeavor are listed. The second and third columns describe both the mathematical tools and the limiting physical kinetics associated with the several process steps. The reader will recognize several physical models discussed in Sections II and III as well as more complex kinetics not discussed here. Selected references are included in the table to point the way for further study in these areas. The first three rows in Table III refer to implantation, diffusion, and oxidations—the key processes which are better established. Moreover, the manufacturing equipment and the process modeling tools are most advanced in these areas. Both etching and deposition represent the avant garde, in terms of both equipment and the need for more complete process modeling.

TABLE IV
RELATIONSHIP OF PROCESS STEPS, MODELS USED FOR SIMULATION, AND LIMITING PHYSICAL EFFECTS

PROCESS EFFECTS AND IMPLICATIONS			
Process Steps		Analysis Tools	Physical Limits
Ion Implantation		Distributions: Gaussian, Pearson...	Defects/Knock-ons
		Boltzmann Transport [4]	Transient Annealing [40]
		Monte Carlo [51]	
Diffusion		Fick's Law	Diffusivity
	"SUPREM" [12] "SUPRA" [38]	Multi-Stream Models [1] [7]	Precipitation; Transient Kinetics
Oxidation		Laplace + Surface Reaction	Surface Kinetics
	"SOAP" [34]	Hydrodynamics (Navier-Stokes) [52]	Stress/Flow
Etching	"SAMPLE" [50]	Huygen Waves [49]	Multi-Stream Kinetics [44]

V. CAD TOOLS FOR IC DESIGN AND MANUFACTURING

The previous sections have traced the evolution of process modeling beginning with bipolar concerns and moving to MOS devices and local oxidation effects. Now metallization, lithography, etching, and deposition will dominate IC processing through this decade. The development of process models have been an integral part of the fundamental understanding needed for control of manufacturing technology. The objective of this final section is to consider the computer-aided design (CAD) tools which have evolved in process modeling and to demonstrate their place in IC design and manufacturing.

For purposes of this discussion we limit our attention to the areas of technology, devices, and circuits. Fig. 19 shows parallel paths of development from a system point of view. The left path is that of the system design, ultimately leading to circuit design and IC layout for custom and semicustom blocks. The right path shows the technology-based leading to the working IC devices and design rules used by the circuit designers to create the actual cells and subsystems. Three major interfaces exist between the two paths. At the device and layout levels, the technologists and circuit designers communicate critical performance and layout information—dominantly through the mechanisms of device models for circuit simulation and the rules to create these devices. Hence model coefficients and layout rules are two key exchange formats for communication. We will not discuss layout further, although this topic and its ramifications for achieving greater system complexity on single IC chips is of major importance for VLSI [53]. The third interface is less formal than the previous two, but a critical one in the evolution of technology. This is the projection phase shown as an arrow coming from the last generation circuit and system design efforts. At this interface the projections must be made as to needed technology features—for example, analog capabilities in a digital technology—and the hopes and expectations of both the systems and technology groups must be enunciated and defined. This aspect of the design interface will have a

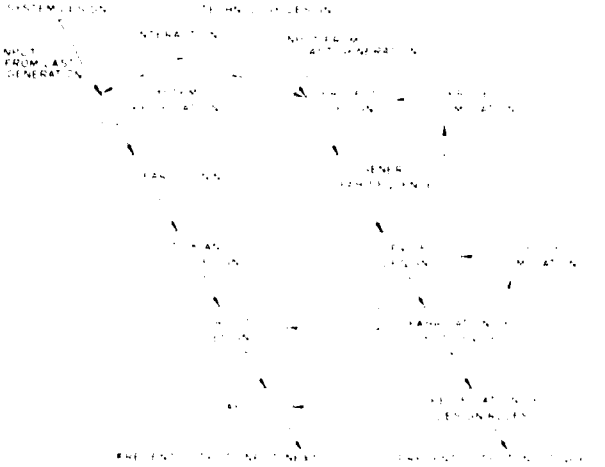


Fig. 19. Schematic of "system" and "technology" design processes and their interrelationships.

growing level of emphasis and importance with VLSI. There is a need to build cell libraries of substantial complexity, for example programmable ALU's and RAMs, and to scale them into new technologies and design rules. Moreover, the growing need to fully consider system-level factors such as hybrid and printed circuit interconnects, data conversion (A/D and D/A), and communication channels (busses and networks) suggests that chip technology will evolve in new directions. The choice to make on-chip hybrid technologies—for example, bipolar compatible MOS—will reflect a careful interchange across the system/technology interface.

We will define more narrowly the function of CAD for process design and manufacturing at the lower two interface levels shown in Fig. 19. Moreover, the dashed boxes shown as local feedback on the technology path (labeled "process" and "device") indicate that there are somewhat generic design steps involved in the development of technology. Fig. 20 shows a bottom-up slice of CAD at the process and device levels. The multifaceted equipment and process-models level shown at the bottom of the figure

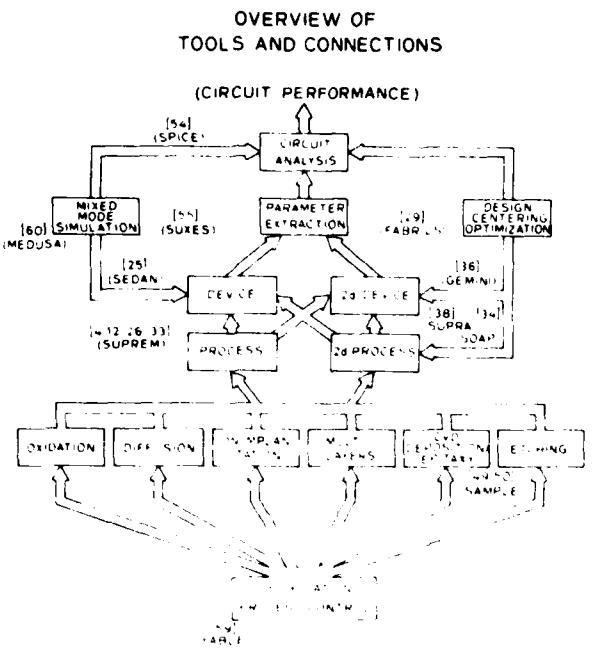


Fig. 20. Range of CAD tools and their interconnection in going from process specification through circuit design.

reflects the detailed considerations given in the previous sections. The incorporation of these process models into CAD programs, both one- and two-dimensional, provide the capability to simulate the effects of process steps such as oxidation and diffusion, and thereby "inspect" quantities such as junction depth and oxide thickness. Since it is time consuming and costly to fabricate IC's repeatedly during design, the simulation process is very efficient. Moreover, since measurement of physical parameters is difficult and often inaccurate, the use of simulation can be invaluable in providing feedback and cross-checking during both process development and manufacturing. Finally, the complexity of IC processing as reflected in all critical dimensions of submicrometer channel-length MOS devices requires careful design and process control over sequences of steps, not simply single oxidation or diffusion cycles. The predictive capabilities for process modeling CAD have grown rapidly and gained wide acceptance specifically because of the issues of process complexity and need for tight dimensional control.

Device modeling is the level just above process modeling in Fig. 20. Historically, these activities have been used extensively to understand fundamental limits of devices and predict performance. The successful evolution of process modeling—both one- and two-dimensional—now has established a basis for realistic and predictive device models. A number of the available tools at these various levels are included on the figure with appropriate literature references. The SUPREM program [12], [26], [4] is now the most mature of the process-modeling tools and is used extensively in process design. Industrial feedback suggests that there is a thousand-to-one cost savings in simulating a process step compared to laboratory cost. As we have demonstrated in Section III, the sensitivity of MOS devices to junction depths and oxide shape parameters such as oxide thickness and lateral extent for local oxidation plays a key, if not dominant, role in determining electrical characteristics. Hence, the availability of accurate process-modeling tools has laid the foundation for increased use and accuracy of device simulation.

The final levels of CAD tools shown in Fig. 20 are those for circuit simulation and device model parameter extraction. The circuit simulator SPICE [54] is shown as a specific tool because of its wide acceptance for more than a decade. The use of circuit simulation to evaluate performance is essential to the circuit designer if not also to the system designer. One can accurately determine speed limitations of gates and memory as well as off-chip current drive capabilities. Circuit simulation has replaced breadboarding at the chip level, primarily because of its demonstrated accuracy and speed compared to the inaccuracy and cost of breadboards.

A key limitation to simulation accuracy at the circuit level is device model parameters. The extraction capabilities shown in Fig. 20 primarily refer to extraction for prototype and production devices. Recent publications [55], [56], [37] have demonstrated efficient means to extract both single sets of parameters as well as statistically meaningful sets of parameters including critical correlations of parameters and physical effects. Sections II and III have shown the importance of such a statistical approach, especially for VLSI where the number of devices used and the distribution of their parameters limits design margins and performance. Fig. 20 also shows two alternative paths related to circuit simulation—mixed-mode simulation [60] and design centering of circuit parameters based on process and device inputs [29]. Each of these techniques tries to capture lower levels of detail in a form useful for circuit design. Mixed-mode simulation allows the direct embedding of device simulation in a circuit simulator environment. Design centering provides an environment to evaluate sensitivities of circuit parameters based on first-order analytic models for process and device effects.

The overall intent of Fig. 20 is to show an important coupling and synergism of process, device, and circuit CAD tools. While the present method for extracting circuit simulation model parameters relies heavily on measurements, the increasing use of the other tool sets will become dominant by the mid- to late 1980's. The reasoning parallels the motivation for process modeling itself—it will be faster and more accurate than experimentation, especially as process statistics become more significant. However, the concern with accuracy limitations of models and their coefficients will increasingly be pushed toward the processing end of the CAD tool chain. Limitations in device models related to resistances, capacitances, and even mobility each have an underlying set of technology variables such as impurity doses, junction depths, and oxide thicknesses. The factors-of-two change in device model parameters can increasingly be traced to these underlying

technology parameters as well as the associated lithography variations. Hence, Fig. 20 contains two messages. First, the range of CAD tools between process design and circuit simulation will be of growing importance. Second, the use of process and device simulation as local feedback, as shown in Fig. 19, are well established for process design and will grow quickly as manufacturing tools as well.

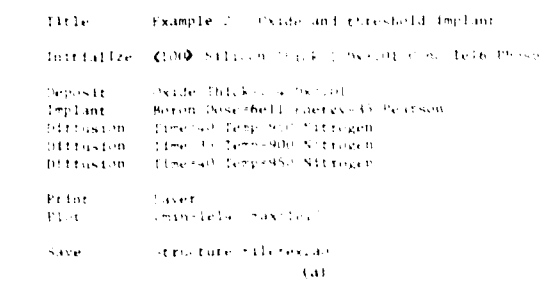
It is beyond the scope of this paper to consider in detail the analysis techniques or even the state-of-the-art features of one- and two-dimensional process- and device-analysis tools. The previous sections have demonstrated several examples with a suitable sampling of current technology-oriented device effects. Both short-channel narrow-width effects of local oxidation on parasitic devices as well as defect generation can now be modeled in two dimensions. Rather than project into the future concerning how far the evolution of process modeling CAD will advance, I would like to reflect on the potential for the modeling concepts and technology depicted in Figs. 19 and 20 to become an integral part of IC manufacturing. Implicit in the discussion is a firm belief that process models will keep pace with the rapid development of manufacturing equipment technology and device innovation.

There are four attributes of CAD for process and device modeling which are essential to its long-term success in IC manufacturing: accuracy, speed, friendliness, and system integrability. I will briefly discuss each of these. Accurate determination of process and device parameters is a critical factor for scalability and manufacturing of VLSI. The basic premise for success of CAD tools in this area is to predict the critical performance and process control variables with sufficient accuracy so that devices can be well designed and, more importantly, manufactured. Examples in Sections II and III show clearly this dual role of design and manufacturability.

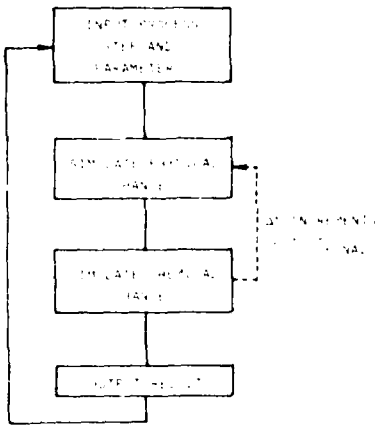
The factor of CAD tool speed has several implications. First, it is necessary that process and device designers get sufficient feedback quickly so that they reduce costs in the use of the fabrication facilities. Simulation obviously does not replace fabrication—it reduces the trial and error needed to converge to a stable process. Moreover, simulation allows the exploration of the process window and helps identify factors which can affect manufacturing and process control. A second factor related to speed is the growing possibility to use process models directly in the manufacturing environment—for example, as very sophisticated controllers for equipment. Although this aspect of simulation is only beginning to become practical, the prerequisite for its success is simulation speed in real time on the small computers used for process control. Finally, the growing complexity of process and device simulators, dictated by more complex kinetic models of physical processes, has caused a lag in available CPU cycles. The increased speed of next-generation computers has helped substantially. Nonetheless, there will be an ongoing effort in developing better algorithms to match the physics and yet provide real-time computations as suggested earlier.

The user interface for CAD tools, including process and device modeling, is a major factor in establishing broad usage in both engineering and manufacturing environments. In the area of process modeling the user input has evolved from text descriptions similar to SPICE-type syntax for device models. From the manufacturing point of view the text looks very similar to instructions used to control processing equipment. Fig. 21(a) shows one simple sequence of step specifications for an implantation and diffusion sequence. The internal program calculations used to solve for the resulting impurity distributions are shown schematically in Fig. 21(b). The physical changes refer to steps such as oxidation (16) and the chemical changes refer to diffusion (4). The discrete time solution of the respective partial differential equations results in the impurity profile shown in Fig. 21(c). Here the deposited oxide-layer thickness is shown as well as the impurity profile both in the oxide and into the silicon bulk. From the user interface point of view the pictures of profiles are extremely valuable, although more qualitative than quantitative. The transformation of impurity profiles into measurable quantities is the key step to get to the end result. For example, junction depth, sheet resistance, junction capacitance, and threshold voltage are typically desired user outputs. Fig. 21(d) shows one further post-processing capability for process simulation output. The profile from Fig. 21(c) has been converted into a plot of channel charge versus gate potential which can in turn be compared with measurements. From the viewpoint of manufacturing it will be increasingly important that such on-line monitoring of electrical as well physical outputs be generated so that feedback between results and design intent can be critically evaluated.

In the area of two-dimensional process and device simulation the user interface requires a different set of considerations. Here the topography is a dominant concern and text descriptions alone are not sufficient. Fig. 22 shows cross-sectional views of a portion of a CMOS device structure. Fig. 22(b) shows the cross section as viewed by the technologist when considering the trade-offs related to the boron implant and LOCOS steps. Fig. 22(c) shows the simulation grid used for 2D process modeling where high-concentration diffusion is to be modeled [57]. The discretization used to solve both the impurity diffusion and oxide interface effects place constraints on the most appropriate positioning of the grid. In addition, there are numerical analysis constraints implicit in the grid specification since the efficiency of the solution is affected by both the number of points and the form of their interconnection. For example, techniques such as line-relaxation (SLOR) or finite-difference (FD) methods each impose different constraints on the spacing of the grid [36]. The grid shown in Fig. 22(c) can also be used for device analysis of the physical structure shown in Fig. 22(a). As stated above, the physical as well as numerical constraints dictate how this grid must be refined or altered for the device modeling application. In this case, since electrical rather than impurity diffusion effects are involved, the grid must be altered in several regions. For example, the electronic analysis now



(a)



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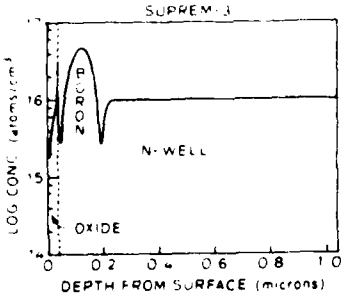

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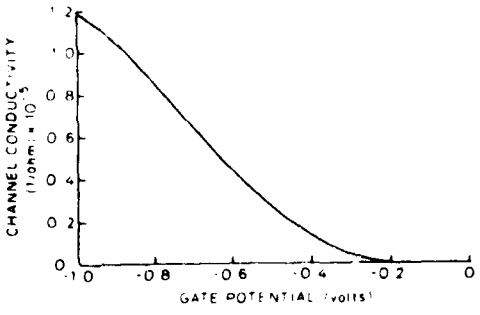
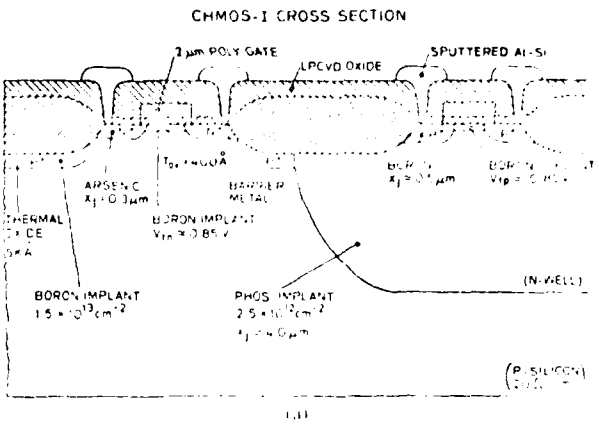
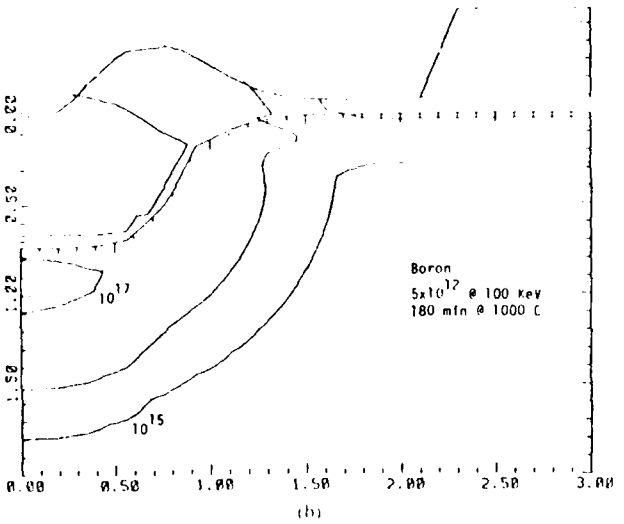


(d)

Fig. 21. User interface and underlying analysis for process simulation. (a) Input file. (b) schematic of computations performed. (c) output of impurity profile, and (d) computed channel charge versus bias.



(a)



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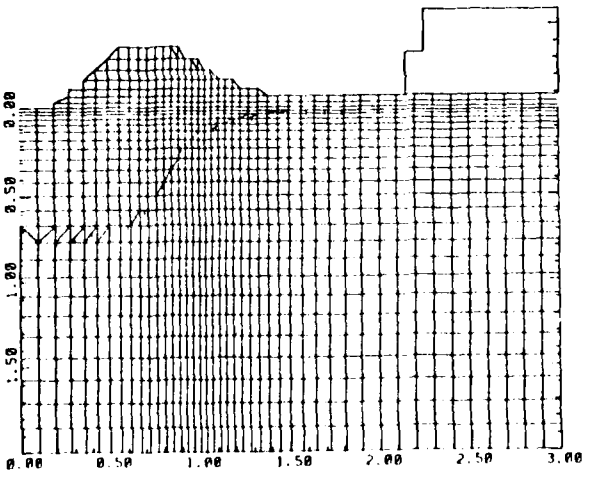

(c)

Fig. 22. CMOS cross section and analysis "windows". (a) complete inverter. (b) "window" for isolation analysis, and (c) numerical grid for device analysis.

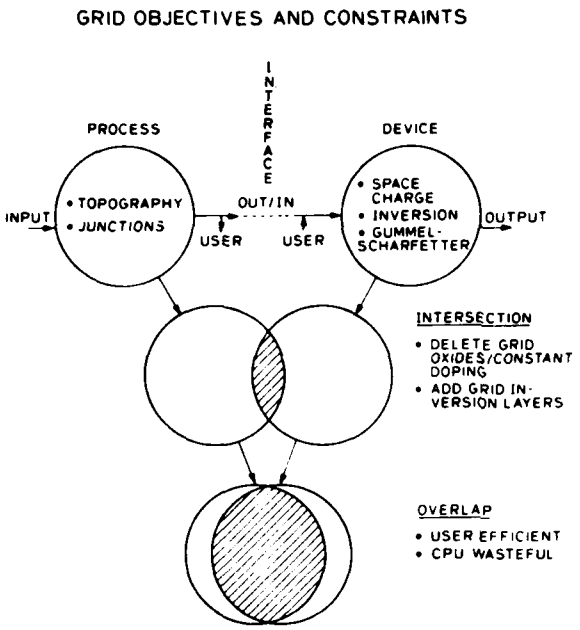

Fig. 23. Grid objectives and constraints for process and device analysis.

requires solution for depletion edges and carrier distribution which occur in regions physically quite separate from the regions of maximum concentration as shown in Fig. 22(b). The user interface problems associated with the systematic progression from Fig. 22(c) into device analysis is still an art rather than a science. Fig. 23 defines schematically the problems of grid definition and the associated physical constraints imposed by the process and device simulation. The user interfaces indicate required interaction. Recent research results indicate successful automation of parts of the process, and hence the ability to relieve the user of these time-consuming and error-prone steps [58]. The vertical sequence of choices in process and device-modeling grids indicate options at several levels. The physical constraints of the systems of equations—Fick's law contrasted with the Poisson and continuity equations—suggest the need for substantially different grids. The total merging of grids for both process and device modeling offers the user a great relief, but may excessively compromise the underlying numerical solvers. The choices to be made both at a user level and in the underlying algorithms will evolve rapidly over the next decade. Certainly automation of algorithms to increase numerical efficiency and simultaneously enhance the user interface are the preferred directions of evolution.

The final essential attribute of CAD tools for process and device modeling is system integrability. The meaning of this term can be discussed at three levels. These levels of integration have been implicitly defined in Figs. 19, 20, and 23—each indicating a lower level of interfacing and simultaneously a higher level of demands on performance and algorithms. The long-range wish is for an "Integrated CAD System"—a cradle-to-grave approach in the design, production, and testing of IC's. Certainly the need for CAD tools at all levels shown in the figures discussed throughout this section are crucial to the success of IC design and manufacturing. Extensive algorithmic research will produce the desired interfaces depicted in Fig. 23. The integration of the CAD tools shown in Fig. 20 will be driven by the increasingly tight manufacturing controls needed for scaled-down devices. Moreover, the device and interconnect models needed for SPICE will dictate increased use of process and device simulation to extract the current physical parameters and coefficients. Finally at the system level shown in Fig. 19, the need to manage and control production will mandate the high-level integration of process and device modeling CAD. Recent efforts to create CAD languages for IC manufacturing [59] suggest a very positive and far-sighted perspective on solutions to the system needs implied by Fig. 19. The needs to automate production-trained personnel, schedule equipment, and document procedures and results are all key ingredients of manufacturing system. Indeed, the CAD tools discussed in this article are one set of specific computer aids to be incorporated into such a manufacturing system of the future.

VI. Conclusion

The intent of this article is to put the details of process and device modeling in perspective, relative to the history and future of IC manufacturing. Since its inception, technology modeling has been used to understand the fundamental limits of process and device control. This paper has traced primarily the evolution of process models for impurity diffusion and oxidation. Examples for bipolar and MOS technologies have been given to show details of application to both device design and manufacturing control. In considering the future for process and device modeling two aspects have been emphasized. The trends in equipment technology for IC manufacturing will play a major role in dictating the need for further modeling work. Furthermore, the CAD tools for technology modeling fit into an overall system-design approach. This system must integrate individual CAD tools to meet the overall objectives of IC manufacturing.

Acknowledgment

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Stanford University Announces a Two-Day Program

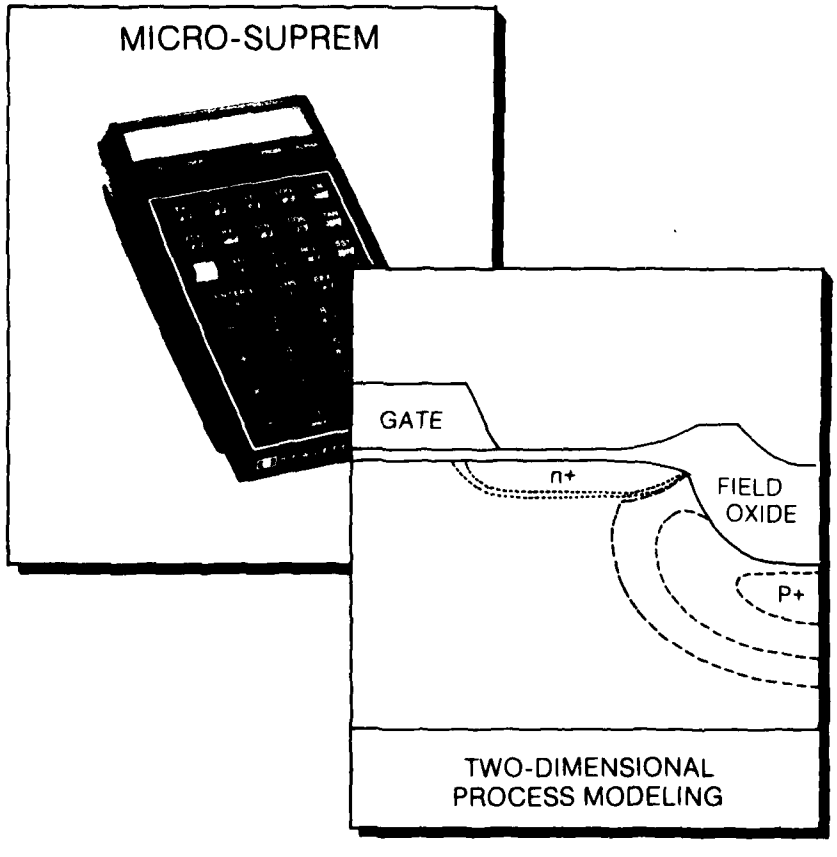
Computer-Aided Design of IC Fabrication Processes

Technology Modeling

Monday July 27, 1981

Process and Device Simulation

Tuesday July 28, 1981



Computer-Aided Design of IC Fabrication Processes

A two day program: July 27-28, 1981 Stanford, California

The modeling of fabrication processes for silicon integrated circuits is invaluable in developing VLSI. Device tolerances require tight control of all aspects of technology. This seminar series presents state of the art process modeling and simulation research efforts at Stanford. In addition to extensive discussions of oxidation, interfaces, polysilicon, and ion implantation, there will be a number of talks on process and device characterization. As illustrated by the cover, new process modeling tools will be discussed for the first time.

The meeting format will be a series of lectures as outlined in the program. Speakers will provide copies of foils. In addition, technical reports will be distributed which give an extended discussion of further background and details of the experiments, models and computer programs. The registration fee includes all course materials as well as lunches and dinner (July 27, 1981). The first day will involve primarily lectures and discussions of the materials aspects of technology modeling with substantial emphasis on specific experimental and model results. The second day will focus on more general aspects of simulation programs such as SUPREM, device simulation, and applications. A "forum" atmosphere will be encouraged to obtain specific user feedback. A number of specific applications and results (case studies) will be presented.

Location: Terman Auditorium, Stanford University, Stanford, California.

Fee: The fee for each day is $175 (including lecture notes, luncheon, and dinner July 27, 1981) or $300 for attending both days. Enrollment is limited, and advance enrollment is required.

Instructional Staff

GARY BRONNER, Research Assistant, Stanford University
DAVID CHIN, Research Assistant, Stanford University
LEE CHRISTEL, Research Assistant, Stanford University
BRUCE E. DEAL, Manager, Fairchild R&D, Palo Alto, California
ROBERT W. DUTTON, Professor, Stanford University
JAMES A. GREENFIELD, Research Assistant, Stanford University
STEPHEN E. HANSEN, Senior Scientific Programmer, Stanford University
CHARLES ROBERT HELMS, Adjunct Professor, Stanford University
THEODORE I. KAMINS, Member Technical Staff, Integrated Circuits Laboratory, Hewlett Packard, Palo Alto, California
MICHAEL R. KUMP, Research Assistant, Stanford University
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JAMES D. PLUMMER, Associate Professor, Stanford University
KRISHNA SARASWAT, Senior Research Associate, Stanford University
HANS STORK, Research Assistant, Stanford University
WILLIAM TILLER, Professor, Stanford University

Technology Modeling

Monday - July 27, 1981

8:00 a.m.	Registration	
8:30	Introduction and Status Report on SUPREM	Plummer, Dutton
9:30	Break	
9:50	High Pressure and HCl Oxidation	Deal
10:15	Thin Oxides: Growth Kinetics and Charge Characterization	Massoud
10:40	Atomic Level Modeling	Lever
11:00	Interface and Segregation Kinetics	Helms
11:30	Lunch	
1:00 p.m.	Modeling of Polysilicon Resistivity	Saraswat
1:55	Grain Growth, Diffusion, and Multilayer Properties of Polysilicon	Mei
2:05	Silicon Nitride Oxidation	Kamins
2:25	Break	
2:45	Point Defect Modeling Related to Oxidation	Tan
3:10	Characterization of Transient Processes	Bronner
3:30	Ion Implantation and Knock-ons	Christel
4:05	Micro SUPREM — a hand held version	Pfiester
5:30	Reception and Informal Discussion	
6:30	Dinner at the Faculty Club	

Process and Device Simulation

Tuesday - July 28, 1981

8:30 a.m.	The User's View of SUPREM	Hansen
9:15	Extraction of Electrical Parameters from SUPREM	Greenfield
10:00	Break	
10:20	Modeling of Dry Etching Technology	Mei
10:50	Two Dimensional Analytical Process Modeling	Chin
11:10	Two Dimensional Numerical Modeling of Diffusion	Kump
11:35	User Feedback†	Audience
12:00	Lunch	
1:30 p.m.	SEDAN II	Dutton
1:50	Review of GEMINI	Greenfield
2:10	Scaled Bipolar Structures	Stork
2:35	Break	
2:55	Device Parameter Extraction	Lefferts
3:25	Invited User Contributions and Wrap up†	

† Typical presentations include a few foils and five minutes of discussion.

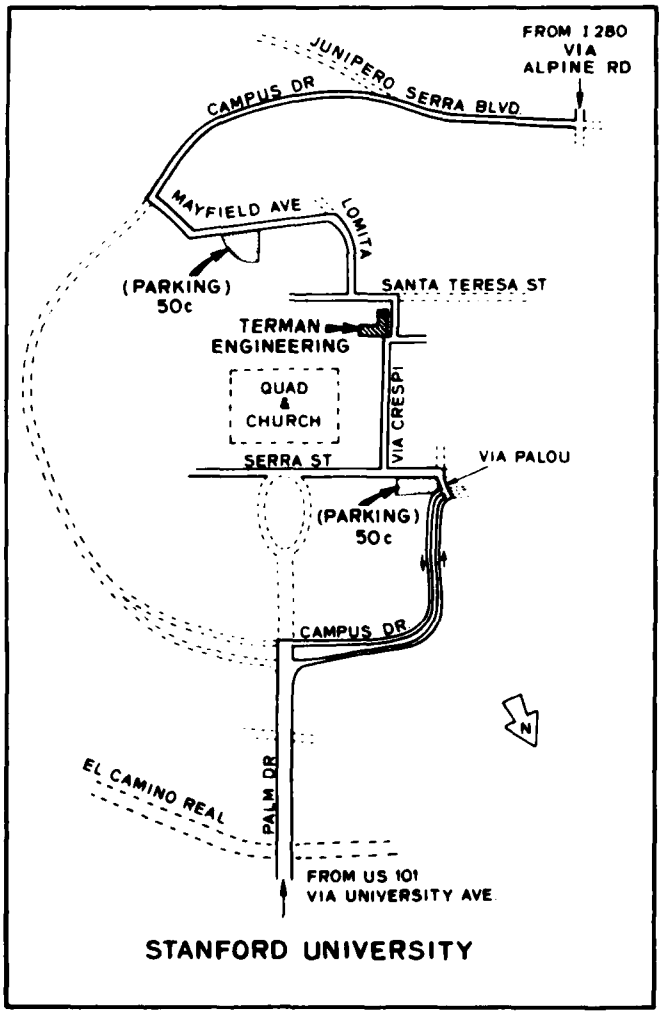
General Information

How to enroll: Enrollment is limited and advance enrollment is required. Enrollment may be made by individuals or companies. Upon request, a place in the program will be reserved for individuals who require time to obtain authorization.

To enroll: Please complete and return the form provided.

Refunds: If you enroll and then cannot attend, a refund, less $10 service charge, will be granted if requested in writing prior to the date of the program.

For further information: Write or call Stanford University Integrated Circuits Laboratory, c/o Robert Dutton, AEL Bldg., Stanford, California 94305; telephone (415) 497-1349.



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Computer-Aided Design of IC Fabrication Processes

A two-day program: July 27-28, 1981 Stanford, California

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248.	Tak Oki	Xerox - CIS	Both
249.	Noble Powell	GE - CIS	Both
250.	Reda Razouk	Fairchild	Both
251.	Dick Reynolds	DARPA	Both
252.	Sven Roosild	DARPA	Both
253.	Bill Sander	ARO	Both
254.	Sam Shichito	Texas Instruments-CIS	Both
255.	Fred Walczik	DEC - CIS	Both
256.	R. Wilkinson	TRW - CIS	Both

SPEAKERS

257. Gary Bronner
258. Lee Christel
259. Bruce E. Deal
260. Bob Dutton
261 Jim Greenfield
262. Steve Hansen
263. Bob Helms
264. Ted Kamins
265. Mike Kump
266. Bob Lefferts
267. Miin-Ron Lin
268. Hisham Massoud
269. Len Mei
270. Jim Pfiester
271. Jim Plummer
272. Krishna Saraswat
273. Hans Stork
274. Bill Tiller
275. Daeje Chin

STUDENTS

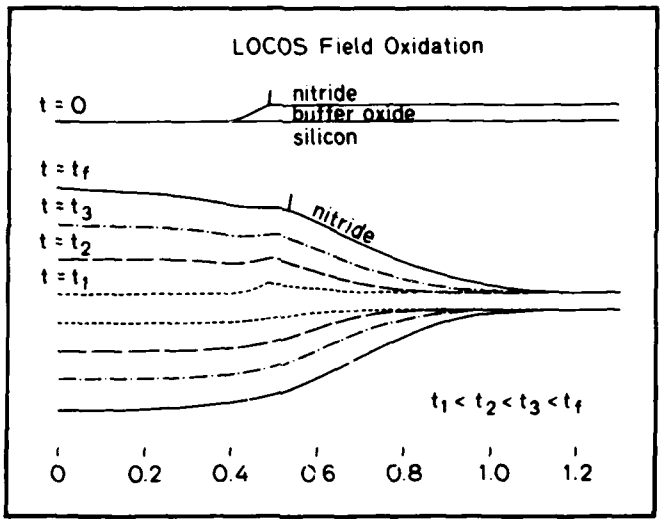
276. J. Shott
277 J. McVittie
278. D. Modlin
279. D. Harame
280. B. Swaminathan
281. Y. Ikawa
282. Bill Eisenstadt
283. M. Eldredge
284. Tatsumi Sumi
285. Hee Gook Lee
286. Charlie Ho
287. Akis Doganis

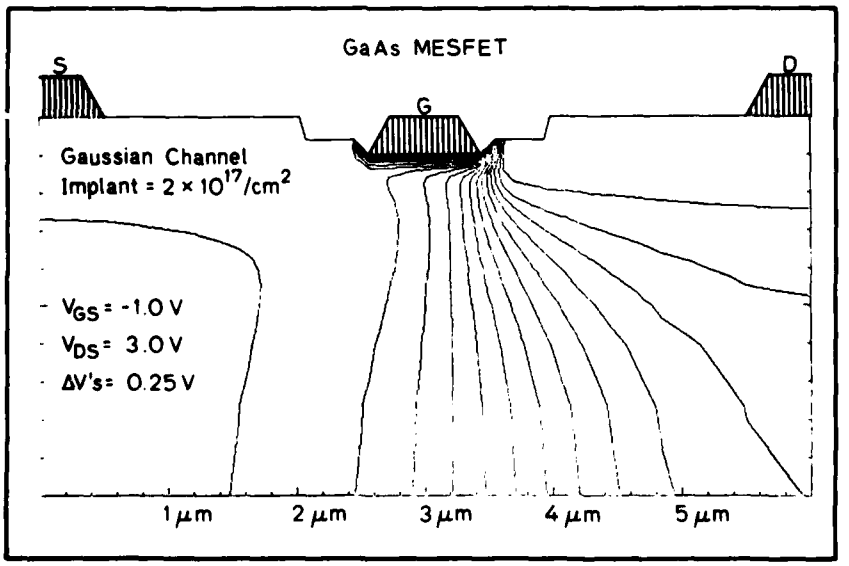
Stanford University Announces a Two-Day Program

Computer-Aided Design of IC Fabrication Processes

Technology Modeling
Wednesday August 18, 1982

Process and Device Simulation
Thursday August 19, 1982





Computer-Aided Design of IC Fabrication Processes

A two-day program:
August 18-19, 1982 Stanford, California

Over the past decade Stanford University has pioneered a fundamental research effort to understand and model integrated circuit (IC) technology. Once each year the Integrated Circuits Laboratory at Stanford presents a summary of recent findings, in the context of a short-course style discussion.

Over the past several years Stanford has developed a variety of process and device simulation programs which embody the results of fundamental research efforts and are finding increased use in process development and device design. At this year's conference new results in the simulation of two-dimensional oxidation and diffusion as well as the SUPREM-3 program are discussed. Novel applications of device modeling and flexible tools for device characterization are new areas where recent results will be presented.

The meeting format will consist of a series of lectures as outlined in the program. Speakers will provide copies of presented materials. In addition, there will be a distribution of technical reports which give an extended discussion of background information and details of the experiments, models, and computer programs. The first day will involve primarily lectures and discussions of the materials aspects of technology modeling with substantial emphasis on specific experimental and model results applicable to SUPREM-3. The second day will focus on more general aspects of process simulation, device simulation, and applications including a discussion of SUPRA. A "forum" atmosphere will be encouraged to obtain user feedback. A number of specific applications and results (case studies) will be presented. The registration fee provides for all course materials, as well as lunches and dinner (August 18, 1982).

Location: Annenberg Auditorium, Stanford University, Stanford, California.

Fee: The fee for each day is $190 (including lecture notes, luncheon, and dinner (August 18, 1982)) or $325 for attending both days. Enrollment is limited, and advance enrollment is required.

Instructional Staff

GARY BRONNER, Research Assistant, Stanford University
DAEJE CHIN, Research Assistant, Stanford University
LEE CHRISTEL, Research Associate, Stanford University
ROBERT W. DUTTON, Professor, Stanford University
WILLIAM R. EISENSTADT, Research Assistant, Stanford University
PAUL M. FAHEY, Research Assistant, Stanford University
SCOTT GOODWIN, Research Assistant, Stanford University
JAMES A. GREENFIELD, Research Associate, Stanford University
STEPHEN E. HANSEN, Senior Scientific Programmer, Stanford University
CHARLES ROBERT HELMS, Adjunct Professor, Stanford University
CHARLES P. HO, Research Associate, Stanford University
MICHAEL R. KUMP, Research Assistant, Stanford University
HISHAM MASSOUD, Research Assistant, Stanford University
DOUGLAS MODLIN, Research Assistant, Stanford University
THAO NGUYEN, Research Assistant, Stanford University
JAMES R. PFIESTER, Research Assistant, Stanford University
MARK R. PINTO, Research Assistant, Stanford University
JAMES D. PLUMMER, Associate Professor, Stanford University
CRAIG H. PRICE, Payload Development Engineer, US Air Force
REDA R. RAZOUK, Senior Member Research Staff, Fairchild R&D, Palo Alto, California
KRISHNA SARASWAT, Senior Research Associate, Stanford University
JOHN D. SHOTT, Senior Research Associate, Stanford University
BALAJI SWAMINATHAN, Research Assistant, Stanford University
DONALD E. WARD, Research Associate, Stanford University
ZHIPING YU, Research Assistant, Stanford University

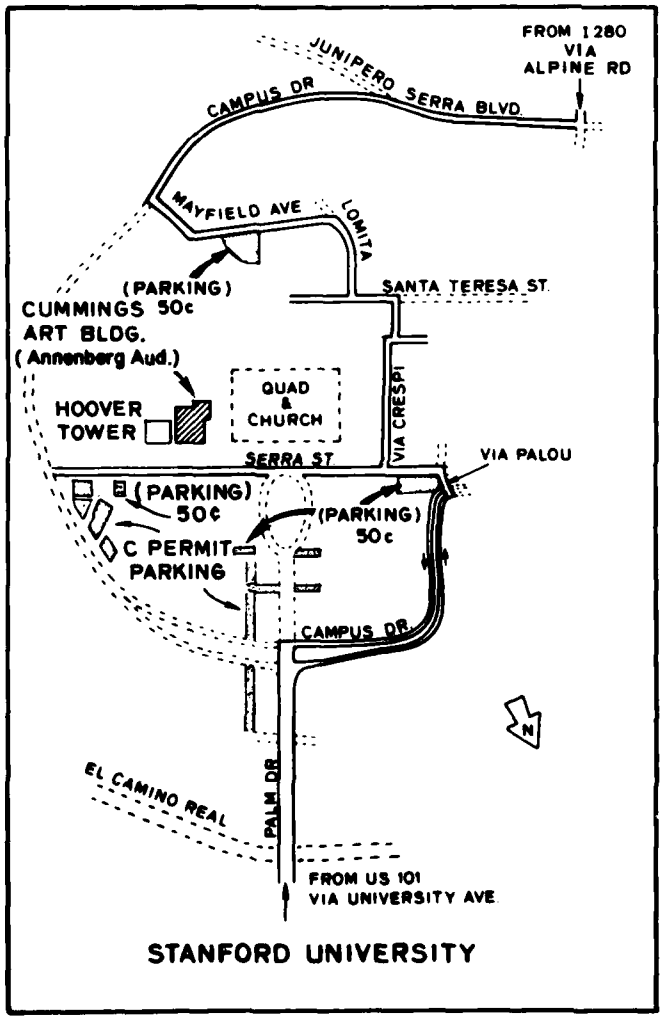
Technology Modeling
Wednesday August 18, 1982

8:00 am	Registration	
8:30	Introduction	Plummer
9:15	Thin Thermal Oxides	Massoud
9:35	High Pressure Oxides	Razouk
9:55	Break	
10:20	2D Oxidation Modeling	Chin
10:45	Enhanced Oxidation Techniques	Modlin
11:05	Interface Kinetics	Helms
11:25	Dopant Diffusion	Ho
11:55	Lunch	
1:00 p.m.	Ion Implantation	Christel
1:30	Diffusion in Polycrystalline Silicon	Swaminathan
1:50	Contacts and Interconnects	Saraswat
2:20	Gettering	Bronner
2:40	Break	
3:00	Diffusion Coefficient Extraction	Fahey
3:25	Electrical Parameters	Greenfield
3:45	Model Implementation in SUPREM	Dutton
4:30	Discussion and Questions	
5:30	Reception and Informal Discussion	
6:30	Dinner at the Holiday Inn	"Dinner Speaker"

Process and Device Simulation
Thursday August 19, 1982

8:30 am	Introduction	Dutton
9:10	SUPREM-3 Process Modeling	Hansen
9:35	Analysis of Multilayer Polycrystalline Structures	Yu
9:55	Interactive Device Design	Pfiester
10:15	Break	
10:40	Device Analysis for GaAs Technology	Price
11:10	Short Channel MOS Modeling	Nguyen
11:35	The Stanford IC Fabrication Facility	Shott
12:00	Lunch	
1:00 pm	2D Process Simulation	Kump
1:30	Isolation Region Structures	Goodwin
1:55	CMOS Latch-up Modeling	Pinto
2:20	Break	
2:40	Optimization Extraction of MOS Model Parameters	Ward
3:00	AC and Time Domain Characterization	Eisenstadt
3:30	Formal Discussion Solicited and Contributed User Feedback†	

†Please send proposed topics and sketches figures to be presented for discussion at the time of advanced registration.



General Information

How to enroll: Enrollment is limited and advance enrollment is required. Enrollment may be made by individuals or companies. A limited number of preferred-rate registrations for government employees will be accepted based on sponsor approval. Deadline for submission of enrollment forms, July 31, 1982.

To enroll: Please complete and return the form provided.

Refunds: If you enroll and then cannot attend, a refund will be granted if requested in writing prior to July 31, 1982.

For further information: Write or call Stanford University Integrated Circuits Laboratory, c/o Robert Dutton, AEL Building, Stanford, California 94305; telephones (415) 497-1349 and 497-4138.

(Enrollment is limited. Advance enrollment is required.)

If enrolling more than one person, please enclose a separate sheet to give name, affiliation, address, and telephone number for others.

Please mail to: Stanford University Integrated Circuits Laboratory, c/o Robert Dutton, AEL Building, Stanford, California 94305.

I enclose a check in the amount of $ _____ to cover _____ enrollment(s) in (check one):

☐ Technology Modeling August 18, 1982 $190
☐ Process and Device Simulation August 19, 1982 $190
☐ Both $325

Name _____
last *first* *middle*

Employed by _____

Company address _____

_____
city state zip

Daytime telephone and extension _____

Make check payable to STANFORD UNIVERSITY.

Stanford University
Integrated Circuits Laboratory
Stanford, California 94305

Computer-Aided Design of IC Fabrication Processes

A two-day program: August 18-19, 1982 Stanford, California

CAD of IC Fabrication Processes

August 18-19, 1982

Youssef S. Abedini	Fairchild	both
Martin A. Afromowitz	Univ. of Washington	both
Jeff Aguilera	Hewlett-Packard	8-19
Diane Ahrendt	Tektronix	both
H. Akiyama	Burns Research Corp.	both
John Altieri	IBM	both
Vince Alwin	RCA	both
David A. Angst	Digital Equipment Corp.	both
Lawrence Arledge	Texas Instruments	both
Wayne Armstrong	Westinghouse	both
Narain D. Arora	Digital Equipment Corp.	both
Jose I. Arreola	UTMC	both
Rolin K. Asatourian	Rockwell International	both
Warren C. Atwood	TRW	8-18
Ronny Bar-Gadda	Signetics	both
Uzi Y. Bar-Gadda	Advanced Micro Devices	both
Steve T. Bay	Nanometrics	8-18
Nabi Bayazit	Hewlett-Packard	both
Sam W. Beal	Texas Instruments Inc.	both
Israel Beinglass	IMP	8-18
James A. Benjamin	Eaton Corp.	both
Donald Bessler	ITT	both
Inderjit S. Bhatti	National Semiconductor	both
Mark S. Birrittella	Motorola Inc.	both
Matt Bonn	Intersil, Inc	8-19
Scott Bowden	IMP	8-19
Brian P. Brodfuehrer	Dept. of Defense	both
John Buchbach	Jet Propulsion Lab	both
L. L. Burns	Burns Research Corp.	both
Gregory N. Burton	Fairchild R&D	both
Thomas N. Casselman	Santa Barbara Research Center	both
Alex Cavalli	Tektronix, Inc.	both
Kit Cham	Hewlett-Packard	8-19
Phil Chan	Intel Corp.	8-19
Sudhir S. Chandratreya	Hewlett-Packard	both
J. J. Chang	Xerox Corp.	both
Yih-Jau Chang	STC Computer Research	both
Joseph P. Chapley	GTE Microcircuits	both
Kong-Chen Chen	Signetics Corp.	both
M. L. Chen	RCA	both
Henry Choe	Rockwell International	both
Cheuk Wah Chu	Tandem	8-19
Tom Clark	Analog Devices	both
Bill Cochran	Bell Labs	both
Barney M. Cohen	Advanced Micro Devices	both
Roy A. Colclaser	Univ. of New Mexico	both
John T. Collett	Newport Beach Research Center	both
Steven R. Collins	Raytheon Co.	both
Tom Collins	Tandem	both

Kwaku A. Danso	Synertek	8-18
Gary F. Derbenwick	Inmos Corp.	both
Ewald Detjens	STC Computer Research	8-19
T. J. Diesel	Hewlett-Packard	both
William G. Divens	Nanometrics	8-18
Norman L. Donovan	Siliconix	both
Edward C. Douglas	RCA	both
Dick Dowell	Hewlett-Packard	8-19
Michael P. Duane	Texas Instruments	both
Kamalesh Dwivedi	Mitel Corp.	both
Monir El-Diwnay	Fairchild	both
Moez M. Esmail	National Semiconductor	both
Chi-Yung Fu	Xerox	both
Julia S. Fu	Sandia National Labs	both
Isaura S. Gaeta	Fairchild	both
Raymond K.Gardner	Delco Electronics	both
Jean-Marie Gastineau	Matra Technology, Inc.	8-19
Philip J. Gerskovich	Cray Research, Inc.	both
Joseph R. Gigante	Westinghouse	both
Barrie Gilbert	Analog Devices	both
Henry Gildenbalt	General Electric	both
Linda Gonzalez	Data General Corp.	both
Diana L. Goodrich	General Dynamics	both
Ravender Goyal	National Semiconductor	8-19
Philip B. Grant	The Aerospace Corp.	both
Chris Groves	Mitel Corp.	both
Don Grubbs	IBM Corp.	both
Charles R. Hall	Westinghouse	both
Howard H. Hansen	IBM	both
Francis Harper	Western Digital	both
Kim G. Helliwell	Synertek	both
Ian Henderson	Texas Instruments	both
Luther Hendrix	Mostek	both
Steven J. Hillenius	Bell Labs	both
Robert H. Hobbs	United Technologies RC	both
Michael W. Hodel	Motorola Inc.	both
Fred Holmstrom	IBM Corp.	both
Kuo-Liang C. Hsi	Trilogy Systems	8-19
Peter Hsieh	STC Computer Research	8-19
Chung S. Hsu	Silicon Systems, Inc.	both
Sheng Teng Hsu	RCA	both
Cheng C. Hu	Inmos Corp.	both
Yaw-Wen Hu	Intel Corp.	both
Chin Huang	Unitrode	both
Alex C. Hui	LSI Logic Corp.	both
J. Inada	Burns Research Corp.	both
Weldon Jackson	Hewlett-Packard	8-19
David Jaffe	IBM	both
Saqib Jang	National Semiconductor	8-18
Prasad S. Jayasimha	IMP	8-19
Roy E. Jewell	Texas Instruments	both
Caroline Jones	Raytheon Co.	both
Edward Kelso	US Army Electronics	both

Ebrahim Khalily	Hewlett-Packard	8-19
Moiz B. Khambaty	IMP	8-19
Ronald W. Knepper	IBM	both
Daniel N. Koury Jr.	Motorola	both
Tom Krehbiel	Motorola	both
Joseph W. Ku	Fairchild	both
Gordon J. Kuhlmann	Rockwell International	both
Robert W. Lade	Eaton Corp.	both
Fang-Shi J. Lai	IBM	both
Pan-Wei Lai	Zilog, Inc.	both
Richard A. Laubhan	NCR Corp.	both
Duane G. Laurent	Mostek	both
W. W. Lee	Hughes Aircraft Co.	both
Robert B. Lefferts	Tektronix	both
Pat Leung	Aertech Industries	both
Michael P. Levis	Zilog, Inc.	both
Joseph Li	Data General Corp.	both
Sheau-suey Li	Data General Corp.	both
T. J. Lie	Burroughs Corp.	both
Albert M. Lin	Bell Labs	both
Ron A. Lindley	Burroughs Corp.	both
Bill Y.J. Liu	Fairchild	8-18
Michael S. Liu	Honeywell	both
Wei Jen Lo	Xerox	both
Kevin Look	Synertek	both
Steve W. Longcor	Advanced Micro Devices	both
Clifford D. Maldonado	Rockwell International	both
Lavi Malholtra	ISD	both
Gary Malloy	Hughes Aircraft Co.	8-18
Robert W. Manning	Inmos Corp.	both
Alan Marston	Hewlett-Packard	8-19
Herman L. Martin	EG&G Reticon	8-18
Russal A. Martin	Xerox	both
John B. Mason	GTE Microcircuits	both
Walter T. Matzen	Honeywell	both
Timothy K. McGuire	Bell Labs	both
Leighton McKeen	Burroughs Corp.	both
Paul G. McMullin	Westinghouse	both
Peter McNalli	National Semiconductor	both
Alwin E. Michel	IBM	both
Douglas G. Millward	Science Applications, Inc.	both
Robert D.Moore	Harris Corp.	both
Dick Motta	Zilog, Inc.	both
B. Nam	Burns Research Corp.	both
Matthew M. Nowak	Burroughs Corp.	both
S. Ochi	Burns Research Corp.	both
Sheng-Yueh Pai	Trilogy Systems	both
Olgierd A. Palusinski	Univ. of Arizona	both
Scott D. Pearson	IBM	both
B. Reddy Penumalli	Bell Labs	both
Dan W.Peters	Hewlett-Packard	both
Doug A. Pike	General Instrument Corp.	both
Jeff H. Pinter	Ford Aerospace	both

Richard C. Pinto	Rockwell International	both
Raymond Pong	Signetics	8-19
Sylvia Pressacco	Fairchild	8-18
Sunil Rahan	Intel	both
Muhit U. Rahman	Power Hybrids Inc.	8-18
Steve Ratner	Hewlett-Packard	both
Dan Reddy	Synertek	both
D. John Redman	Hewlett-Packard	both
Robert C. Rennick	Bell Labs	8-19
L. Howard Roberts	Matra Technology, Inc.	8-19
Lynette B. Roth	Hughes Research Labs	both
Jack L. Sachitano	Tektronix	both
Yoshio Sakai	Hitachi	both
Robert N. Sato	Hughes Aircraft	both
Robert Scheer	Intersil, Inc.	8-18
John Schmeising	Motorola, Inc.	both
Adele Schmitz	Hughes Research Labs	both
Marden H. Seavey	Digital Equipment Corp.	both
Jerold A. Seitchik	Texas Instruments	both
Nagib Sharif	Synertek	both
Steven C. Shatas	AG Associates	8-18
Jack Shiao	Tandem	both
Tadashi Shibata	Toshiba R&D Center	both
Mitsuo Shimizu	Canon USA	both
M. Shizukuishi	Burns Research Corp.	both
David M. Shupe	Bendix	both
Anil K. Singh	Rockwell International	both
Rama S. Singh	General Electric	both
John N. Skardon	Advanced Micro Devices	8-18
Michael P. Snowden	RCA	both
Joe Spear	BTU Engineering Corp.	both
Anthony Spielberg	IBM	both
John W. Stempeck	Polaroid Corp.	both
Edward P. Surowiec	General Electric	both
Bashir A. Syed	General Electric	both
C. T. Tarn	IBM	both
Marcel ter Beek	IMP	8-19
Timothy J. Thurgate	Intel	both
Robert E. Tremain	Xerox	8-19
Tom C. Trieu	Fairchild	both
Murray L. Trudel	Zilog, Inc.	both
Kuey Yeou Tsao	Gould, Inc.	both
Ben Tseng	Advanced Micro Devices	both
Ben Valdez	Hughes Aircraft Co.	both
Milton Vassell	GTE Labs	both
Kris B. Verma	Lockheed Corp.	both
John Walker	GTE Microcircuits	both
Perry Wallia	Synertek	both
Jeffrey Wang	Synertek	both
Shah Waqar	Trilogy Systems	8-19
Moe Wasserman	GTE Labs	both
Al Watkins	Raytheon Co.	both
Gene P. Weckler	EG&G Reticon	both

James C. Weaver	General Electric	both
Moo Y. Wen	IBM	both
K. R. Winrich	Santa Barbara Research Center	both
Thomas W. Woike	TRW	8-18
Evert A. Wolsheimer	Signetics	both
Henry C. Wong	Signetics	8-19
Joe Wong	Raytheon Co.	both
Richard C. Woodbury	Brigham Young Univ.	both
In-Nan Wu	Fairchild	both
Jeff Tse Yang	Memorex	both
Chingchi Yao	Advanced Micro Devices	both
Pak-Ho Yeung	Fairchild	both
Sewang Yoon	Power Hybrids	8-19
Swei-Yam Yu	Fairchild	both

speakers

Gary Bronner
Daeje Chin
Lee Christel
Robert W. Dutton
William R. Eisenstadt
Paul M. Fahey
Scott Goodwin
James A. Greenfield
Stephen E. Hansen
Charles Robert Helms
Charles P. Ho
Michael R. Kump
Hisham Massoud
James D. Meindl
Douglas Modlin
Thao Nguyen
James R. Pfiester
Mark R. Pinto
James D. Plummer
Craig H. Price
Reda R. Razouk
Krishna Saraswat
Siegfried Selberherr
John D. Shott
Balaji Swaminathan
Donald E. Ward
Zhiping Yu

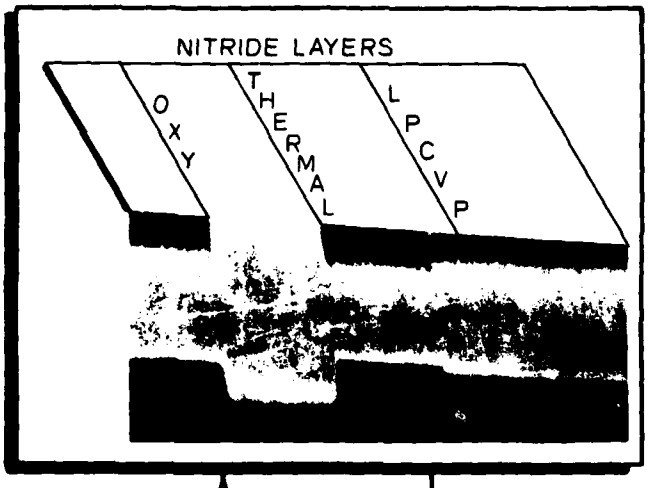
guests

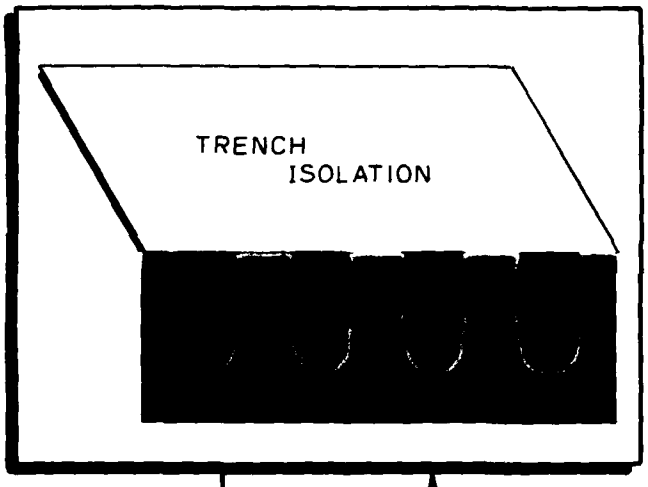
Tayo Akinwande
Dirk Bartelink
Bruce Cairns
Gary Chang
Bruce Deal
Jesus Del Alamo

Akis Doganis
Scott Dunham
Michael Eldredge
Martin Giles
David Harame
Esin Kutlu
Elliott Levinthal
Lanny Lewyn
Liang Lie
Frank Lin
Bill Loh
Paul Losleben
Jack Marshall
Sid Marshall
Jim McVittie
Gary Patton
Stan Perino
Nirmal Ratnakumar
Dick Reynolds
Fu-chia Shone
Tatsumi Sumi
Marc Taubenblatt
Bill Tiller
Jason Woo
Ernie Wood

Stanford University Announces a Three-Day Program

Computer-Aided Design and Manufacturing of Integrated Circuits





Silicon Technology and Process Models
Wednesday August 17, 1983

Model Implementation and Applications
Thursday August 18, 1983

Integrated Circuits Manufacturing Science
Friday August 19, 1983

Computer-Aided Design and Manufacturing of Integrated Circuits

A three-day program:
August 17-19, 1983 Stanford, California

Over the past decade Stanford University has pioneered a fundamental research effort to understand and model integrated circuit (IC) technology. Once each year the Integrated Circuits Laboratory at Stanford presents a summary of recent findings, in the context of a short-course style discussion. This year, for the first time, we have expanded the discussion to include new material on manufacturing science.

Stanford has developed a variety of process and device simulation programs which embody the results of fundamental research efforts and are of substantial value for process development and device design. At this year's conference new results and models for SUPREM 3 are discussed, especially in the areas of multilayer structures, implantation, oxidation and diffusion. The new oxidation analysis program SOAP is demonstrated as well as enhancements to SEDAN for polysilicon emitters and Schottky contacts. Applications of process and device modeling as well as the simulation tools are presented.

Within the least few years Stanford has established a manufacturing capability to fabricate IC's routinely for systems design on a fast-turn-around basis. In this manufacturing spirit we have expanded the program to discuss IC manufacturing science. Internally we are developing a new computer-aided system, FABLE, to assist in line management, documentation, training and a variety of other aspects of manufacturing. The scope of discussion will bridge the gap between device fabrication and process control issues and will include a number of representative industrial speakers.

The meeting format will consist of a series of lectures as outlined in the program. Speakers will provide copies of presented materials. In addition, there will be a distribution of technical reports which give an extended discussion of background information and details of the experiments, models, and computer programs. The first day will involve primarily lectures and discussions of the materials aspects of technology modeling with substantial emphasis on specific experimental and model results applicable to SUPREM 3. The second day will focus on more general aspects of process simulation, device simulation, and applications.

A "forum" atmosphere will be encouraged to obtain user feedback. A number of specific applications and results (case studies) will be presented. The third day will focus on the many issues involved in IC manufacturing science. Primarily industrial speakers will discuss key issues related to systems, equipment, and test structures to monitor and control IC production. The registration fee provides for all course materials, as well as lunches and dinner (August 17 and 18, 1983).

Location: Terman Auditorium, Stanford University, Stanford, California.

Fee: The fee for each day is $200 (including lecture notes, luncheon, and dinner (August 17 and 18, 1983) or $500 for attending three days. Enrollment is limited, and advance enrollment is required.

Instructional Staff

TAYO AKINWANDE, Research Assistant, Stanford University
DIMITRI A. ANTONIADIS, Associate Professor, MIT
WALTER BENZING, Director of Research, Applied Materials
JOE BERGER, Consultant in IC Development, Los Altos
JOHN C. BRAVMAN, Research Assistant, Stanford University
GARY B. BRONNER, Research Assistant, Stanford University
DAEJE CHIN, Research Assistant, Stanford University
CHRIS CLARK, Staff Engineer, Hewlett-Packard
SCOTT T. DUNHAM, Research Assistant, Stanford University
ROBERT W. DUTTON, Professor, Stanford University
PAUL M. FAHEY, Research Assistant, Stanford University
RICHARD FAIR, Vice President, Microelectronics Center North Carolina
MARTIN D. GILES, Research Assistant, Stanford University
JOHN GOLOVIN, President, Consilium, Palo Alto
SCOTT GOODWIN, Research Assistant, Stanford University
STEPHEN E. HANSEN, Senior Scientific Programmer, Stanford University
CHARLES ROBERT HELMS, Professor, Stanford University
CHARLES P. HO, Research Associate, Stanford University
MARK LAW, Staff Engineer, Hewlett-Packard Company
HISHAM Z. MASSOUD, Research Affiliate, Stanford University
JAMES McVITTIE, Senior Research Associate, Stanford University
MEHRDAD MOSLEHI, Research Assistant, Stanford University
WILLIAM G. OLDHAM, Professor, University of California, Berkeley
MIHIR PARIKH, Dept. Manager for Process Automation, Hewlett-Packard
DAVID PERLOFF, President, Prometrix, Sunnyvale
JAMES R. PFIESTER, Research Assistant, Stanford University
MARK R. PINTO, Research Assistant, Stanford University
JAMES D. PLUMMER, Professor, Stanford University
BRIAN K. REID, Assistant Professor, Stanford University
JERRY ROBINSON, Director of Manufacturing Operations, Zilog
ENRICO SANGIORGI, Research Associate, University of Bologna
KRISHNA SARASWAT, Senior Research Asociate, Stanford University
JOHN D. SHOTT, Senior Research Associate, Stanford University
WILLIAM TILLER, Professor, Stanford University
WILLIE J. YARBROUGH, Research Assistant, Stanford University
ZHIPING YU, Research Assistant, Stanford University

Silicon Technology and Process Models
Wednesday August 18, 1983

8:00 a.m.	Registration	
8:30	Introduction	Plummer
9:30	Thin Oxide Kinetics	Massoud
9:55	Oxide Charges	Akinwande
10:20	Enhanced Oxidation Kinetics	Tiller

10:45	Break	
11:15	Oxidant Transport in SiO_2	Helms
11:40	TEM Studies of Interface Morphology	Bravman
12:05	Thermal Nitridation of Silicon	Moslehi
12:30	Lunch	
1:30 p.m.	Extrinsic Diffusion	Fahey
2:00	Oxidation Enhanced Diffusion	Dunham
2:20	Polysilicon Modeling and Multilayer Structures	Ho
2:50	Transient Gettering Kinetics	Bronner
3:10	Break	
3:30	LPCVD Silicide Contacts	Saraswat
4:00	Multilayer Ion Implantation	Giles
4:20	Experimental Ion Implantation Profiles	Oldham
4:50	Discussion and Wrap-up	
5:30	Reception and Informal Discussion	
6:30	Cocktails	
7:30	Dinner	
8:30	Panel	

Implementation and Applications of Process and Device Models
Thursday August 18, 1983

8:30 a.m.	Introduction	Dutton
9:30	Status of SUPREM 3	Hansen
10:00	Transient Point Defect Modeling	Antoniadis
10:30	Break	
11:00	2D Oxidation Analysis Using SOAP	Chin
11:25	Isolation Structures Device Physics	Goodwin
11:50	Trench Isolation Technology	McVittie
12:15	Lunch	
1:30 p.m.	Development of CMOS Technology	Pfiester
1:55	Scaling of Junctions for CMOS	Fair
2:20	Analysis of CMOS Latch-up	Pinto
2:45	Break	
3:10	2D Device Analysis Using PISCES	Law
3:35	Analysis and Modeling of Polysilicon Emitters	Yu
3:55	Scottky Contact MOSFETs	Sangiorgi
4:15	Formal Discussion Solicited and Contributed User Feedback*	

*Please send proposed topics and sketches figures to be presented for discussion at the time of advanced registration

Integrated Circuits Manufacturing Science
Friday August 19, 1983

8:30 a.m.	Introduction	Shott
9:00	Integrated Approach to Manufacturing	Robinson
9:40	Wafer Management for Process Control	Golovin
10:20	Break	
10:45	Control in an IC Manufacturing System	Parikh
11:20	Test Structures for Yield Analysis	Perloff
11:55	Addressable Array Test Structures	Yarbrough
12:25	Lunch	
1:30 p.m.	FABLE A Language for Process Automation	Reid
2:10	Standards for Equipment Interfaces	Clare
2:40	Break	
3:00	Automated Wafer Handling	Berger
3:30	Interfaces and Equipment Reliability	Benzing

General Information

How to enroll: Enrollment is limited and advance enrollment is required. Enrollment may be made by individuals or companies. Preferred-rate registrations for government employees will be accepted based on sponsor approval. Deadline for submission of enrollment forms, August 5, 1983.

To enroll: Please complete and return the form provided.

Refunds: If you enroll and then cannot attend, a refund will be granted if requsted in writing prior to August 5, 1983.

Housing is available on the Stanford campus in student residences without private baths at reasonable rates. Campus recreational facilities are available for your use. For further information contact the Conference Office at 123 Encina Commons, Stanford, California 94305; telephone (415) 497-3126.

For further information: Write or call Stanford University Integrated Circuits Laboratory, c/o Robert W. Dutton, AEL Bldg., Stanford, California 94305; telephones (415) 497-1349 and 497-4138.

(Enrollment is limited. Advance enrollment is required)

I enclose a check in the amount of $_____ to cover ____ enrollment(s) in (check one)

☐ Silicon Technology August 17, 1983 ($200)

☐ Simulation and Application August 18, 1983 ($200)

☐ Manufacturing Science August 19, 1983 ($200)

☐ Entire Program August 17-19, 1983 ($500)

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Computer-Aided Design and Manufacturing of Integrated Circuits

A three-day program: August 17-19, 1983 Stanford, California

Stanford University
Integrated Circuits Laboratory
Stanford, California 94305

CAD OF IC FABRICATION PROCESSES
August 17-19, 1983

Larry D. Abe	TRW	8-19
John M. Acken	Sandia National Labs	8-18,19
H. Akiyama	Burns Research Corp.	3 days
Katie Alexander	Intel	8-17
John Altieri	IBM Corp.	3 days
T. Alvarez	Motorola	3 days
Kostas Amberiadis	RCA Labs	3 days
David Angst	Digital Equipment Corp.	3 days
Susanne Arney	Motorola	3 days
Sheldon Aronowitz	Fairchild	3 days
Rolin K. Asatorian	Rockwell International	3 days
Jimmy W. Baker	McDonnell Douglas Elect. Co.	3 days
Zaher Bardai	Acrian Inc.	3 days
Ronny Bar-Gadda	Signetics	3 days
Dean W. Barker	National Semiconductor	3 days
Allen R. Barlow	AMI	8-17,18
Dirk J. Bartelink	HP	3 days
Geoffrey D. Batchelder	Mostek	3 days
Nabi Y. Bayazit	HP	3 days
Donald W. Baylis	Fairchild	8-19
Allen F. Behle	Rockwell International	3 days
James A. Benjamin	Eaton Corp.	3 days
Inderjit S. Bhatti	National Semiconductor	3 days
Steve Bishop	NSA	8-17,18
Dale Blackwell	Mostek	3 days
Peter Blakey	General Motors Research Labs	3 days
Richard A. Blanchard	Siliconix	8-19
Nick Boruta	Synertek	3 days
Bob Bower	AMD	8-18
Joseph T. Boyd	Univ. of Cincinnati	3 days
Harold K. Brown	Intel	8-17,18
Rene Brown	Hughes Aircraft	3 days
Richard A. Bruce	Xerox	8-17,18
Nguyen D. Bui	AMD	8-17,18
Felixberto A. Buot	Sachs/Freeman Assoc., Inc.	3 days
Matthew S. Buynoski	National Semiconductor	8-17,18
Kit M. Cham	Hewlett-Packard	3 days
Nelson N. Chan	Intel Corp.	8-17,18
Ray Chan	Fairchild	3 days
Tung S. Chang	STC Computer Research	8-17,18
Joseph P. Chapley	GTE Microcircuits	3 days
Charles Chen	Synertek	8-18
Peter Chen	Fairchild	8-19
George Chi	GTE Microcircuits	3 days
Chang S. Choi	Tristar Semiconductor	8-17,18
H. Chun-Min	Data General	8-17
Steve Clark	Zilog	8-18
Ronald N. Clarke	TRW	3 days
William T. Cochran	Bell Telephone Labs	3 days
Brian Coffey	Philips Labs	3 days
Roy A. Colclaser	Univ. of New Mexico	3 days
Tom Collins	Tandem Computers	8-18
William P. Connors	McDonnell Douglas Elect. Co.	3 days
Richard G. Cosway	Motorola	8-17
William P. Cox	AMD	8-17
Peter Cuevas	Xicor	8-18
Shizue S. Davis	RCA Labs	3 days
Peter H. Decher	HP	8-18,19
Ewald Detjens	STC Computer Research	8-18

Akis Doganis	Xerox	3 days
Norman Donovan	Siliconix Inc.	3 days
James L. Dunkley	Silicon Systems	3 days
Eugene Y. Dyatlovitsky	Signetics Corp.	8-18
William R. Edwards	Burr-Brown Corp.	3 days
Badih El-Kareh	IBM Corp.	3 days
Abdel Eltoukhy	Fairchild	3 days
Nicholas E. English	Harris Semiconductor	8-19
Robert Fang	Data General	8-18
Don Ferris	Texas Instruments	8-17,18
Robert A. Flohr	Intel	8-19
Chao-Hsiang Fu	Integrated Device Tech.	3 days
Eric Fujishin	Zilog	8-18
Kuni Fukumuro	Synertek	8-18,19
Robert T. Garbs	Motorola	8-17,18
R. Keith Gardner	Delco Electronics	3 days
Michael Garner	Intel	8-17,18
Santoshi P. Gaur	IBM	3 days
Franklin Gonzalez	Harris Semiconductor	3 days
Bruce Gray	National Semiconductor	3 days
Chuck Green	Zilog	8-19
Chris K. Groves	Mitel Semiconductor, CANADA	3 days
Don Grubbs	IBM Corp.	3 days
Denny Gudea	Tylan Corp.	8-19
Esmat Z. Hamdy	Intel	3 days
Yu-Pin Han	Mostek	3 days
Harrison Haver	Motorola	3 days
Raymond A. Heald	Fairchild	8-18
Kim Helliwell	Synertek	8-18
Steven J. Hillenius	Bell Labs	3 days
Mark H. Ho	ITT	3 days
Robert H. Hobbs	United Tech. Research Center	8-17,18
Paul F. Hogan	Crane Naval Weapons SC	3 days
Ray Holzworth	Xicor	8-18
Paul J. Howell	Fairchild	3 days
Steve K. Hsia	Monolithic Memories	8-17,18
Cheng C. Hu	Inmos Corp.	3 days
Genda J. Hu	Xerox	8-17,18
John Huang	Intel	3 days
Ming-Der D. Huang	Signetics	8-17
Akira Ito	Harris Semiconductor	3 days
Weldon Jackson	HP	8-18
David Jaffe	IBM Research	3 days
Sheldon V. Jennings	TRW	3 days
David P. Jensen	National Semiconductor	3 days
Roy E. Jewell	Texas Instruments	8-17,18
Richard V. Johnson	Xerox	8-17,18
Walter H. Jopke	Control Data Corp.	3 days
Jon Kang	Zilog	8-18
Ashok Kapoor	Fairchild	3 days
Chris Kapral	GTE Lenkurt	3 days
Patrick N. Keating	Bendix Corp.	3 days
E.J. Kennedy	Union Carbide Corp.	3 days
Kevin W. Kiely	Logic Devices	8-18
Jung S. Kim	Gold Star Co.	3 days
Wen C. Ko	AMD	8-18
Tej Kohli	Siliconix	8-18
R. Kondo	Burns Research Corp.	3 days
Peter B. Kosel	Univ. of Cincinnati	3 days
Wei-Yi Ku	Signetics	8-17,18

Gordon Kuhlmann	Rockwell International	3 days
Robert W. Lade	Eaton Corp.	3 days
Paul H. Langer	Bell Labs	3 days
H. Peter D. Lanyon	Worcester Polytech. Ins.	3 days
Guillermo Lao	Xerox Corp.	3 days
Richard A. Laubhan	NCR Microelectronics	3 days
Duane G. Laurent	Mostek	8-17,18
James P. Lavine	Eastman Kodak Co.	3 days
Kwyro Lee	Gold Star Semiconductor	3 days
William W.Y. Lee	Hughes Aircraft Co.	3 days
Robert B. Lefferts	Tektronix, Inc.	3 days
Raymond T. Leung	Signetics Corp.	8-18
Eric K. Li	Fairchild	8-17,18
Joseph Li	Intersil	3 days
C. Y. Liu	IBM Corp.	3 days
Chun-Mai Liu	IMP	8-18
Dan Liu	Avantek	8-18
Albert Lo	Comdial	3 days
Michael J. Lo	Xerox	8-19
Stewart G. Logie	Synertek	8-17,18
Steven W. Longcor	AMD	8-18
Mike Lumsden	NSA	8-17,18
Senamjit Majumdar	Gould	8-19
Kenneth Mar	Hughes Aircraft	8-19
Jim Marolf	Zilog	8-17, 19
T. McCaffrey	IBM Corp.	3 days
David O. McGovern	Alternative Technologies	3 days
Leighton E. McKeen	Burroughs Corp.	3 days
Larry D. McMillan	Honeywell Inc.	3 days
Peter McNally	National Semiconductor	3 days
R.J. McReynolds	Burns Research Corp.	8-17
Jayant S. Mehia	AMD	3 days
Bob Meinke	HP	8-17,18
Paul Miller	Teletype Corp.	3 days
Mike Misheloff	VLSI Technology, Inc.	3 days
John L. Mohamed	Fairchild	8-19
Farrokh Mohammadi	ITT	3 days
Mohammad Mohaved-Ezazi	Xerox Corp.	8-18
Rick L. Mohler	IBM Corp.	3 days
Alan Moore	General Instrument	3 days
Tsou Morris	National Semiconductor	3 days
Brian Munt	Zilog	8-17
Paul Murray	IBM	3 days
B. Nam	Burns Research Corp.	3 days
David R. Newby	National Semiconductor	8-19
Edward D. Nowak	Synertek	8-18
Paul Nygaard	Hughes Aircraft	3 days
Soo-Young Oh	HP	8-18
Chris O'Kroley	Teletype Corp.	3 days
Richard F. Palys	Burroughs MCG	3 days
B. Reddy Penumalli	Bell Labs	3 days
Dan W. Peters	HP	8-17
Don Pettengill	AMD	8-18
Joe T. Pierce	National Semiconductor	3 days
Jeff H. Pinter	Ford Aerospace & Comm. Corp.	3 days
John Poksheva	Rockwell International	3 days
Robert G. Poulsen	Northern Telecom	8-19
Nader Radjy	AMD	8-18
Sunil Rahan	Intel	8-19
C.F. Rahim	Bell Labs	3 days

Subrahmaniam Rathnam	Mostek	3 days
Kola N. Ratnakumar	Precision Monolithics	8-18
Kothandaraman Ravindhran	GTE Labs	3 days
Ken J. Rebitz	Xicor	8-17
Thomas A. Reilly	Lafayette College	3 days
Llanda Richardson	Digital Equipment Corp.	3 days
Israel Rotstein	National Semiconductor	3 days
Klaus K. Schuegraf	Tylan Corp.	8-17
Jerold A. Seitchik	Texas Instruments	8-17,18
Albert M. Sekela	Honeywell Inc.	3 days
Majumdar Senajit	Gould Research Labs	8-19
Saleem A. Shaikh	AMD	3 days
Steven C. Shatas	AG Associates	8-17
Jack Shiao	Tandem Computers	8-18
M. Shizukuishi	Burns Research Corp.	3 days
Ying K. Shum	National Semiconductor	3 days
Rama S. Singh	General Electric Co.	3 days
Louis Sivo	AMD	8-17
John N. Skardon	AMD	8-19
Cezary Slaby	Northern Telecom, CANADA	3 days
Steven B. Southwick	Westinghouse	3 days
Gregorio Spadea	VLSI Tech., Inc.	3 days
Paolo Spadini	VLSI Tech., Inc.	3 days
Jacob Steigerwald	National Semiconductor	3 days
George Stickney	Motorola Inc.	3 days
Chien-Sheng Su	Intel Corp.	8-17
Kung-Yen Su	Signetics Corp.	8-18
Pin Su	RCA Co.	3 days
Yu Sun	AMD	8-19
Won G. Sunu	Gould, Inc.	3 days
C.T. Tarn	IBM Corp.	3 days
Richard C. Taylor	Synertek	8-19
Jay M. Tenenbaum	Fairchild	8-19
Robert E. Theriault	Northern Telecom, CANADA	3 days
Jack F. Thomas	Signetics Corp.	8-18
Mammen Thomas	AMD	8-17
P.S. Trammel	Signetics	8-17
Swe-Den Tsai	Monolithic Memories	8-17,18
Fu-Shiang Tseng	Fairchild	8-18
Huan-Chung H. Tseng	National Semiconductor	8-17,18
Kody Varahramyan	IBM Corp.	3 days
Kris Verma	Lockheed	3 days
Pete Vutz	Synertek	8-19
George Walker	Synertek	8-17,18
Perry C. Wallia	Synertek	8-17,18
Ching-Tai S. Wang	Delco Electronics	3 days
J.K. Wang	Hughes Aircraft	3 days
Moe S. Wasserman	GTE Labs	3 days
Douglas J. Welter	Motorola	8-19
Moo Wen	IBM Corp.	3 days
Richard K. Williams	Siliconix	8-17,18
William M. Wilson	Fairchild	3 days
Thomas W. Woike	TRW	8-17,18
Jerry J. Wolfe	IBM	3 days
Evert A. Wolsheimer	Signetics	8-18
E.G. Wright	Synertek	3 days
Jeff T. Yang	Memorex	3 days
Young U. Yu	FET Lab, Inc.	3 days
Michael Yung	Commodore MOS Technology	3 days
Peter M. Zeitzoff	Eastman Kodak Co.	3 days

GUESTS:

1. Charlotte Ludington
2. Edward Kelso
3. Bruce Deal
4. Dick Reynolds
5. Sven Roosild
6. Derek Webb
7. Reda Razouk
8. Fred Walczyk
9. Venson Shaw
10. C. S. Chang
11. Elizabeth Batson
12. Richard Pinto
13. Jacques Beauduoin

From NSA:

14. J. Crawford
15. M. Gould
16. B. Bandy
17. T. Smith
18. C. Putnam
19. J. Griffin
20. D. Kokalis

SPEAKERS:

1. Tayo Akinwande
2. Dimitri Antoniadis
3. Walter Benzing
4. Joe Berger
5. John Bravman
6. Gary Bronner
7. Daeje Chin
8. Chris Clare
9. Scott Dunham
10. Bob Dutton
11. Paul Fahey
12. Richard Fair
13. Martin Giles
14. John Golovin
15. Scott Goodwin
16. Stephen Hansen
17. Charles Helms
18. Charles Ho
19. Mark Law
20. Hisham Massoud
21. James McVittie
22. Mehrdad Moslehi
23. Andy Neurether
24. William Oldham
25. Harold Ossher
26. Mihir Parikh
27. David Perloff
28. James Pfiester
29. Mark Pinto
30. Jim Plummer
31. Jerry Robinson
32. Enrico Sangiorgi
33. Krishna Saraswat
34. John Shott
35. William Tiller
36. Willie Yarbrough
37. Zhiping Yu

Stanford University

Software Distribution

Purpose

To disseminate Stanford-developed computer software efficiently and broadly to potential users.

Background

The number of research projects involving computer software is steadily increasing. Mere publication in a research journal is often not adequate to transfer research methodologies and findings to other scientists or the public without the availability of the computer software used in the research.

A Software Distribution Center (SDC) has been established at Stanford University as a mechanism to distribute computer software efficiently to the largest number of potential users. The SDC relieves faculty and students of this often burdensome and distracting task, and also provides a focal point for individuals at other universities, in industry, in government and elsewhere who wish to access Stanford software.

The SDC provides no commercial services such as installation, maintenance, debugging, enhancements, training or support of any kind. The software is distributed on an "as is, with all defects" basis.

Software from Stanford is available on a three-tier schedule (see diagram). The first two tiers are accomplished by the SDC.

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The first tier of distribution is for non-commercial research use and is performed on a cost-recovery basis. The license granted is non-exclusive, non-transferable and for internal use only. Programs are provided at an estimated break-even price (factoring in the cost of reproduction, materials, postage and handling, and the estimated number of users), which allows the SDC to recoup its operating expenses. This type of distribution is generally made to academic colleagues, non-profit research institutions, and government agencies.

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The third tier of distribution is performed by private software companies which are granted a license from Stanford to develop the software and then to sublicense it to others. The commercial tier three distributor is able to provide the installation, maintenance, debugging, enhancements, training and support that the SDC cannot. In some cases, recipients of first or second tier distribution from the SDC may also become customers of the tier three distributors, desiring the more developed version and services provided.

Not all software programs are available from a tier three distributor. Some are currently distributed only on a tier one and/or tier two basis from the SDC. When a tier three licensee is sought, Stanford's Office of Technology Licensing considers such factors as:

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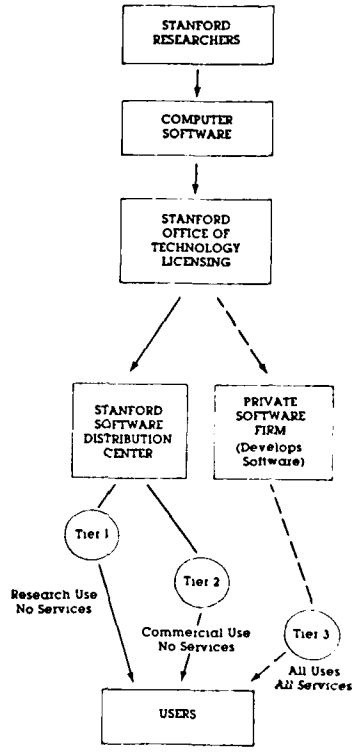
- —technological competence of the prospective licensee with respect to the particular software program
- —resources that are available to the prospective licensee for commitment to development, marketing and support

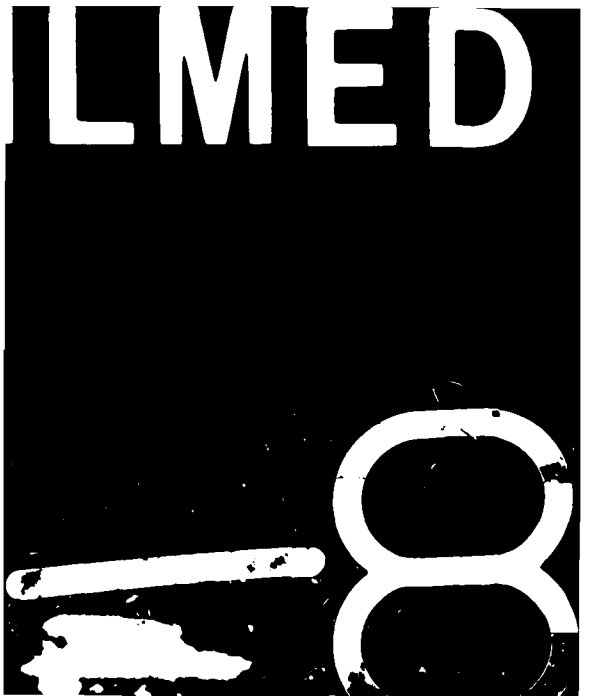
Administration of the SDC

The SDC is administered by the Office of Technology Licensing, 105 Encina Hall, Stanford University, Stanford, California 94305, (415) 497-0651, Telex 348402 STANFRD STNU.

The SDC staff looks forward to serving you and welcomes your inquiries.



	Tier 1	Tier 2	Tier 3
GEMINI	18	47	28
SEDAN	7	8	12
SOAP	0	4	0
SUPREM II	9	11	0
SUPREM III	21	36	54
SUPRA	9	28	42
SUXES	7	13	0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