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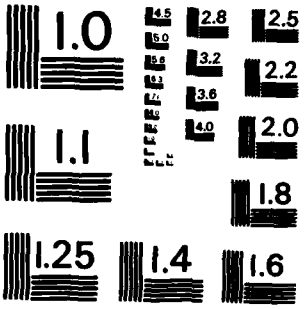

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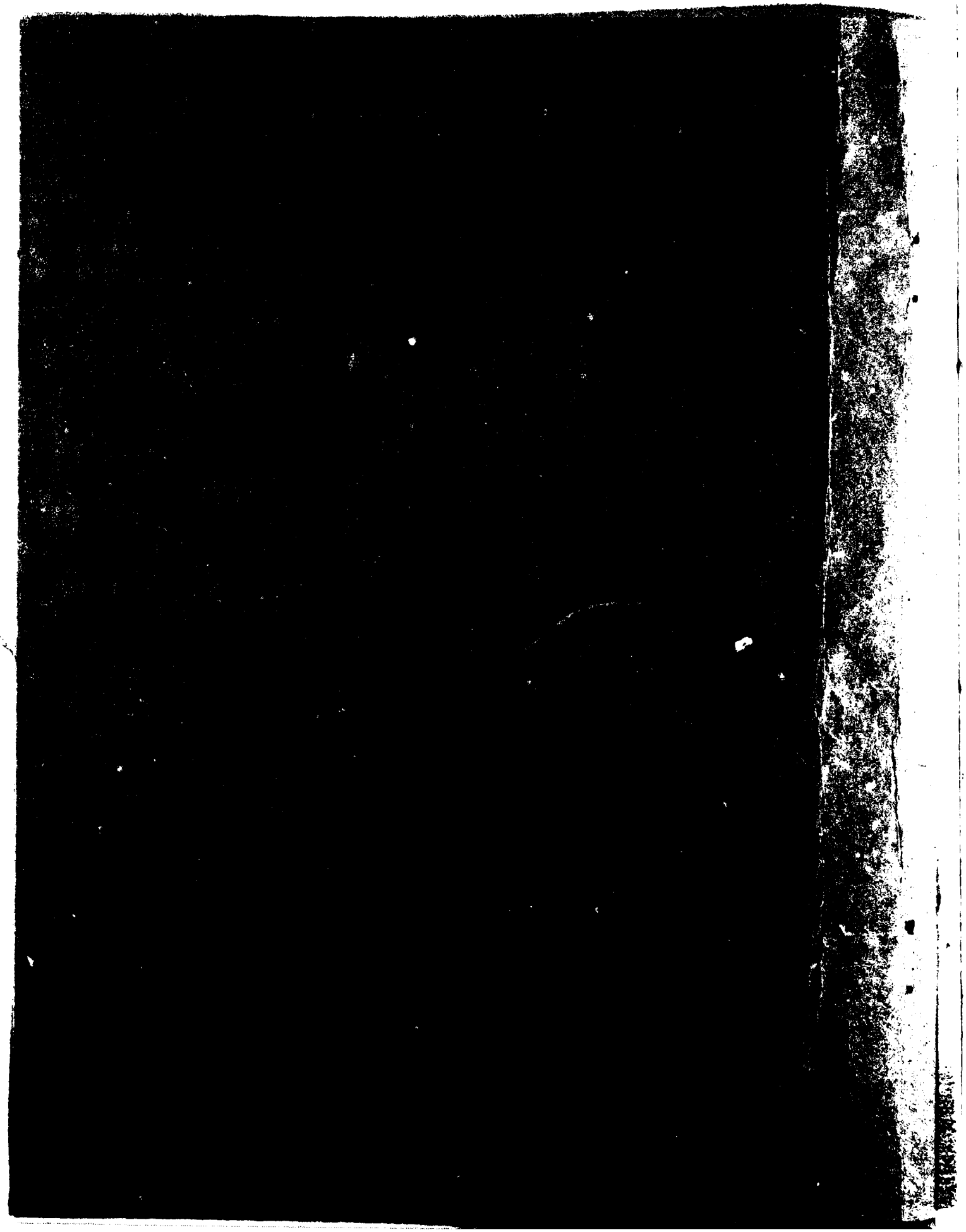

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20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

The report describes techniques for the continuous monitoring and control of phase and output power in active phased array modules. The output phase and power of the signal from the module are sensed by a simple six-port network using Schottky barrier detectors; the output voltage from these detectors is used in a control loop to provide correction signals to a phase shifter and attenuator. Two control schemes have been compared. One is a digital loop using a microprocessor and this achieves an overall (over)

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control accuracy of 0.1dB and 1°, but has the disadvantage of complexity and of a response time in the order of hundreds of milliseconds. The second is a completely analogue loop which has a response time of less than 100ns and can provide real-time phase correction during the output pulse from a module. Although the control accuracy is marginally worse with the analogue loop in these initial tests, it is expected that refinements in the continuation of this work will enable the same accuracy to be achieved in both digital and analogue loop techniques. The application of these techniques may be particularly important in future monolithic integrated circuit radar module design.

CONTENTS

1. INTRODUCTION

Basic active phased array module design concepts are now well advanced {1,2,3} and the technology is in a transition stage between hybrid construction and the use of monolithic GaAs chips as major functional blocks (low noise amplification, downconversion, phase and amplitude control, and microwave power generation). The need for low cost and mass production of phased array modules brings difficulties in maintaining tight tolerances on module output power and phase control. At the same time, system requirements for low sidelobe and adaptive antennas are presenting a need for much tighter tolerances than before. Current phase shifters frequently manage little better than 10^{o} rms error, which is obviously unacceptable in high resolution phase shifters (e.g. 6-bit shifters) currently under discussion.

One approach towards the achievement of very low phase and amplitude errors in active phased arrays is to place tight tolerances and a high degree of quality control on each component and assembly operation in an active array module. This is obviously incompatible with low cost.

Another approach, for which a case is made in the present work, is to not place tight tolerances on the module, but to measure continuously the output phase and power, a correction then being made dynamically for any deviations from desired values. Such an approach requires the module to have a voltage-controllable output power and phase, and a simple means for accurate phase and power measurement at the output as the sensor for the control loop (Fig. 1). Provided the sensor and control electronics are inexpensive, this approach offers the possibility of a low cost, high phase accuracy and high phase resolution array module. It is arguable that such a closed-loop control scheme is the only way to achieve the currently envisaged overall tolerances in array modules. It has already been shown that phase locked loop control of phase in active array modules can be achieved with the rapidity necessary (e.g. 100ns)

for most beam steering applications and the cancellation of temperature-induced phase drifts in active components {4,5}.

It is the aim of the present work to sample the r.f. output from a phased array module, either at the module or in the near field of its associated antenna, and to provide a closed loop control system capable of setting the output phase and power to within 1^{o} and 0.1dB of any desired prescribed values in a time of order 100ns.

The work therefore centres on the r.f. sensor, the control loop and the control element in the module.

2. R.F. SENSOR AND CONTROL LOOP FOR POWER AND PHASE MEASUREMENT

Most techniques for accurate phase and amplitude measurement at microwave frequency are expensive and complex. A commonly used instrument, which gives the accuracy required, is the network analyser in which downconversion of the r.f. signals to i.f. is first carried out and the measurements made at i.f. after careful calibration routines.

The use of two mixers, each in a linear region, one with a 90^{o} phase shift in the signal path, will provide amplitude and phase difference information between reference and module output signals (Fig. 2). This is the commonly used in-phase (I) and quadrature (Q) downconversion to baseband method employed in digital beamforming. There would be possibilities for the use of such a sensor in the present work, but the I and Q outputs also have d.c. offsets which are dependent on mixer balance and the mixer r.f. input signal drive levels. It was felt that great difficulty would be found in achieving the required phase and amplitude accuracy unless the system was complicated by prior downconversion of the r.f. signals to i.f. and then the I and Q outputs formed from i.f. mixers with their greater potential accuracy as phase detectors. Such a scheme would require a local

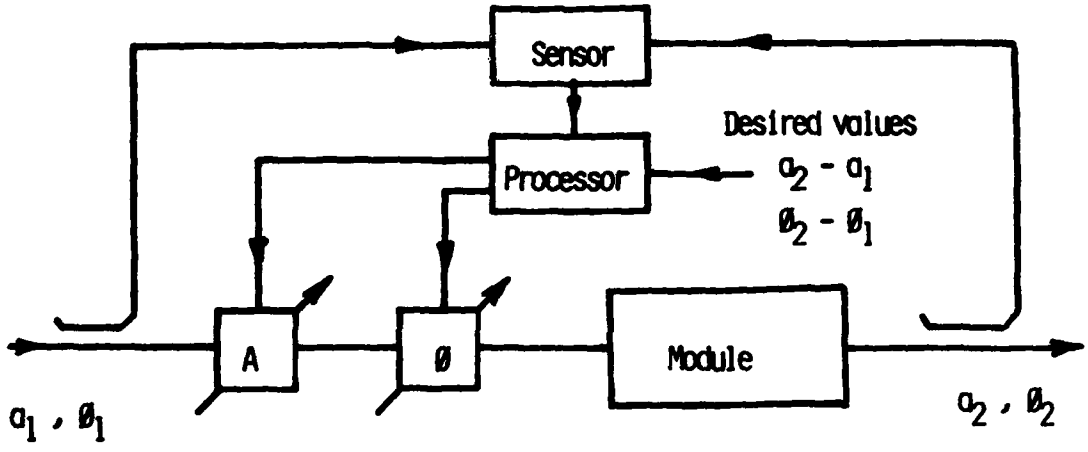

Fig.1: Amplitude and Phase Control Loop for an Active Array Module

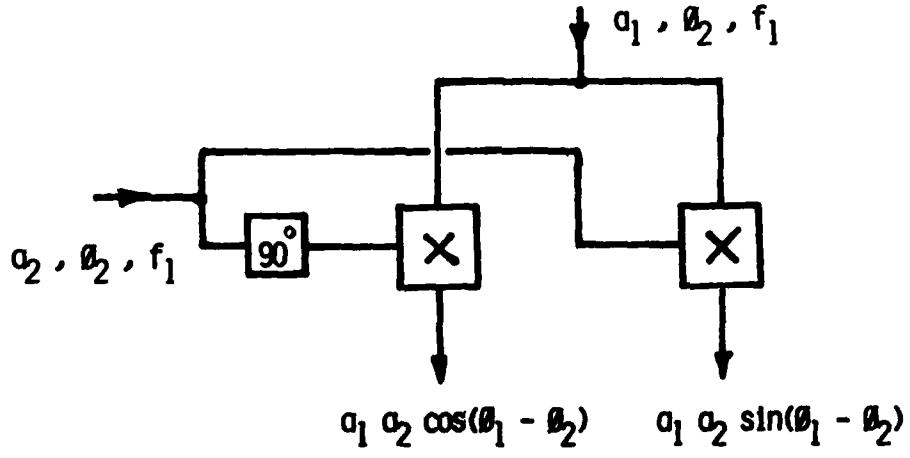

Fig.2: Amplitude and Phase Information from Two Mixers

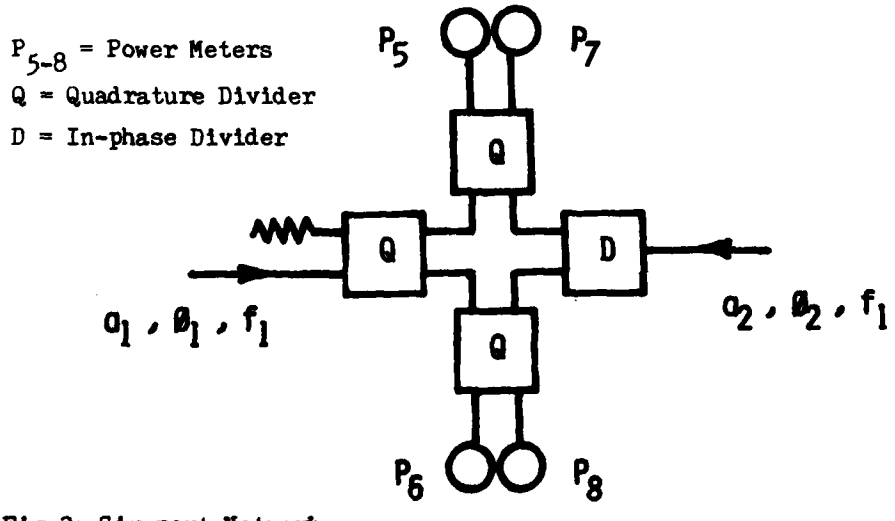

Fig.3: Six-port Network

oscillator in each module to track the r.f. output with a desired constant i.f. offset; this is in effect what a network analyser does, and this degree of complexity would be unwarranted in the present application.

The most attractive system, taking into account low component count and simplicity, is to use a six-port network as the phase and amplitude sensor. Such networks are attracting considerable attention at present because of their potential as low-cost network analysers at frequencies up to the mm-wave band {6,7,8,9}. A six-port network configured to measure the phase and amplitude difference between two signals is shown in Fig. 3. It consists of three quadrature 3dB hybrids and one in-phase 3dB divider. There are two signal input ports, r.f. power is measured at four ports, and one port is terminated in a matched load.

Each quadrature hybrid, if considered as an ideal device, provides an exactly 3dB split of input signals a_m and a_n into two orthogonal components as shown in Fig. 4. Likewise, an in-phase divider provides an exactly 3dB split with no phase difference between the components. The complete pattern of signal flow in the six-port network of Fig. 3 is shown in Fig. 5. The signals appearing at the four output ports are as follows:

$$\begin{aligned}
&\text{Port 5 :} \quad -j\left(\frac{a_1}{\sqrt{2}} + \frac{a_2}{\sqrt{2}}\right) \\
&\text{Port 6 :} \quad \frac{a_1}{\sqrt{2}} - j\frac{a_2}{\sqrt{2}} \\
&\text{Port 7 :} \quad \frac{a_2}{\sqrt{2}} - \frac{a_1}{\sqrt{2}} \\
&\text{Port 8 :} \quad \frac{a_2}{\sqrt{2}} - j\frac{a_1}{\sqrt{2}}
\end{aligned} \tag{1}$$

A square law detector placed at each of these ports will, therefore, provide an output voltage proportional to the square of the modulus of each of these signals. Voltages V_5, V_6, V_7 and V_8 will

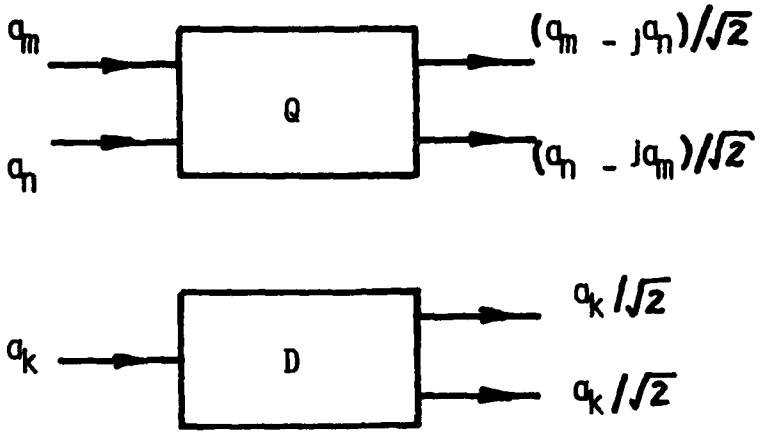

Fig.4: Amplitude and Phase Relationships for Dividers

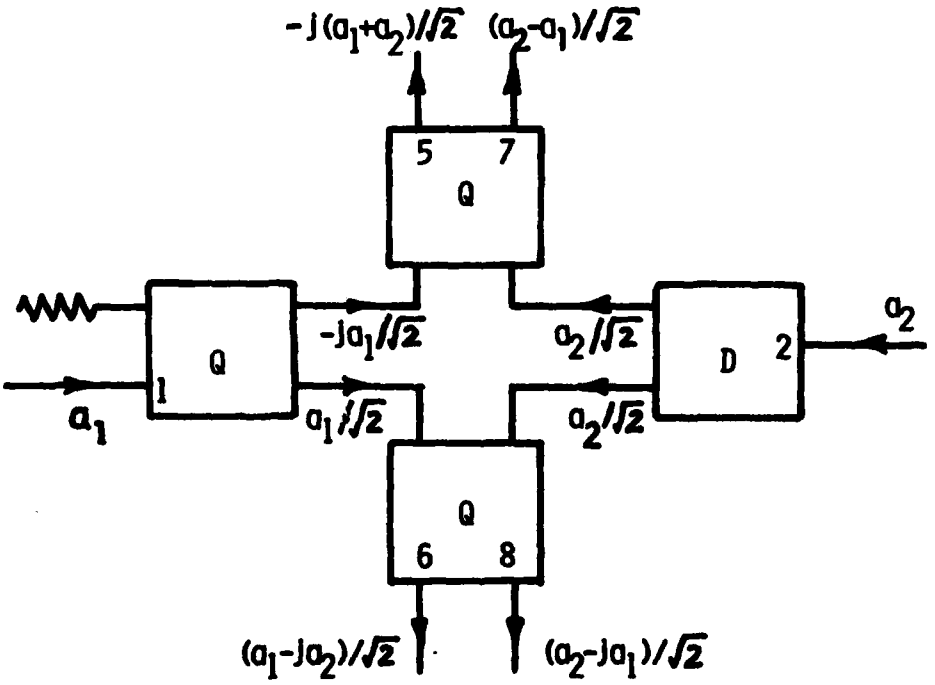

Fig.5: Signal Flow in the Six-port Network

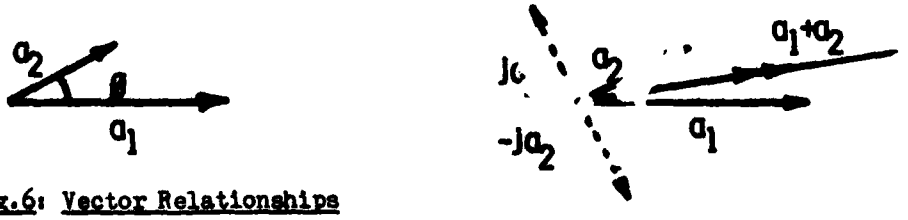

Fig.6: Vector Relationships

be obtained, where:

$$\begin{aligned} V_5 &= C\,|a_1 + a_2|^2 \\ V_6 &= C\,|a_1 - ja_2|^2 \\ V_7 &= C\,|a_2 - a_1|^2 \\ V_8 &= C\,|a_2 - ja_1|^2 \end{aligned} \qquad (2)$$

and it is assumed that the detector sensitivity $K_p (= 2R_oC)$, where R_o is the r.f. load, is the same for each detector. The various voltages may be expressed in terms of the amplitude and phase of the signals a_1 and a_2 by means of the cosine rule for the vector triangle involving a_1 and a_2, as shown in Fig. 6

$$\begin{aligned} V_5 &= C\,\left\{|a_1|^2 + |a_2|^2 + 2|a_1a_2|\cos\phi\right\} \\ V_6 &= C\,\left\{|a_1|^2 + |a_2|^2 + 2|a_1a_2|\sin\phi\right\} \\ V_7 &\quad C\,\left\{|a_1|^2 + |a_2|^2 - 2|a_1a_2|\cos\phi\right\} \\ V_8 &= C\,\left\{|a_1|^2 + |a_2|^2 - 2|a_1a_2|\sin\phi\right\} \end{aligned} \qquad (3)$$

where $\phi = \phi_2 - \phi_1$, the phase difference between the signals a_2 and a_1.

Thus $$V_5 - V_7 = 4C\,|a_1a_2|\cos\phi \qquad (4)$$

and $$V_6 - V_8 = 4C\,|a_1a_2|\sin\phi \qquad (5)$$

By elimination

$$|a_1a_2| = \frac{1}{4C}\left[(V_5 - V_7)^2 + (V_6 - V_8)^2\right]^{1/2} \qquad (6)$$

and $$\sin\phi = \frac{(V_6 - V_8)}{\left[(V_5 - V_7)^2 + (V_6 - V_8)^2\right]^{1/2}} \qquad (7)$$

$$\text{or } \cos\phi = \frac{(V_5 - V_7)}{\left[(V_5 - V_7)^2 + (V_6 - V_8)^2\right]^{1/2}} \qquad (8)$$

The conclusion from equations (6)-(8) is that if signal a_1 is the reference signal, measurements of V_5, V_6, V_7 and V_8, together with knowledge of the detector sensitivity K_p, will yield a value for the amplitude a_2 of the module output signal at the measurement point; measurement of V_5, V_6, V_7 and V_8 alone will yield a value of the module output phase with respect to the reference from either equation (7) or equation (8). Equation (7) will be more accurate around $\phi = 0$ or 180° and equation (8) will be more accurate around $\phi = 90^\circ$.

In order to obtain values for a_2 and ϕ, the various operations required on the measured voltages V_5, V_6, V_7 and V_8 can be carried out by analogue signal processing in circuits which have square law, square root, or sinusoidal characteristics. Such circuits, however, suffer from the usual deficiencies of analogue circuits, namely sensitivity of characteristics to variations in temperature and it is desirable that the processing operations should be kept to a minimum.

For a phase locked loop phase control system it is required that the phase detector should provide a null when the output phase and reference phase are identical. Such a phase detector characteristic, of sinusoidal form, may be simply obtained if the outputs $(V_5 - V_7)$ and $(V_6 - V_8)$ are summed through variable gain amplifiers or variable attenuators. This may be seen by inspection of equations (7) and (8) and the use of relationships:

$$\frac{1}{(1 + k^2)^{1/2}} \sin\phi + \frac{k}{(1 + k^2)^{1/2}} \cos\phi = \sin\left\{\phi + \arctan(k)\right\} \qquad (9)$$

$$\frac{1}{(1 + k^2)^{1/2}} \sin\phi + \frac{1}{(1 + k^2)^{1/2}} \cos\phi = \sin\left\{\phi + \arctan(1/k)\right\} \qquad (10)$$

Thus, by multiplying either the $\cos\phi$ or $\sin\phi$ outputs by factors within the range 1 down to a small value k, most easily accomplished

from a digital value of k as input to a multiplying digital-to-analogue convertor (MDAC), a sinusoidal phase detector characteristic with a null at a value of phase ϕ = -arctan or ϕ = -arctan ($^1/_k$) is obtained. If possible inversion of cos ϕ and sin ϕ outputs is also included, equivalent to negative values of k, unambiguous shifting of the phase detector null over the range $-\pi \leq \phi \leq \pi$ is obtained. Since the amplitude of the phase detector response is only important as regards the loop gain and not the phase accuracy, it is not necessary to calculate the denominators of equations (7) and (8).

A possible implementation of the phase control loop is shown in Fig. 7. For 1^o phase resolution, the value of k must cover the range $1.7 \times 10^{-2} \leq k \leq 1$, and thus 40dB gain control (e.g. 8-bit MDAC's) would be more than adequate.

This form of analogue processing, if implemented with low group delay amplifiers,would provide very fast phase correction. Although, in principle, full phase control over the range 0 - 2π could be provided by this means, there are good reasons why it is better to use the loop in a phase trimming operation rather than a phase setting operation. For the loop to control the full 2π phase range requires the voltage-controlled analogue phase shifter to cover more than 2π phase shift and appreciable control voltage output capability of the loop amplifier is required. A high loop gain is then required to reduce phase errors and this can bring instability problems; also, amplifier slew rate limitations with large voltage swings would reduce the speed of response.

The preferable scheme is therefore to make use of a conventional (e.g. pin diode) phase shifter as the main phase control. The most significant bits of the digital input phase code command are routed directly to this phase shifter. The analogue phase shifter driven by the phase sensing circuitry and the full number of bits of the input phase code then trims the phase to the exact value required, with an accuracy governed by the properties of the loop. The analogue phase shifter then only has to encompass a phase

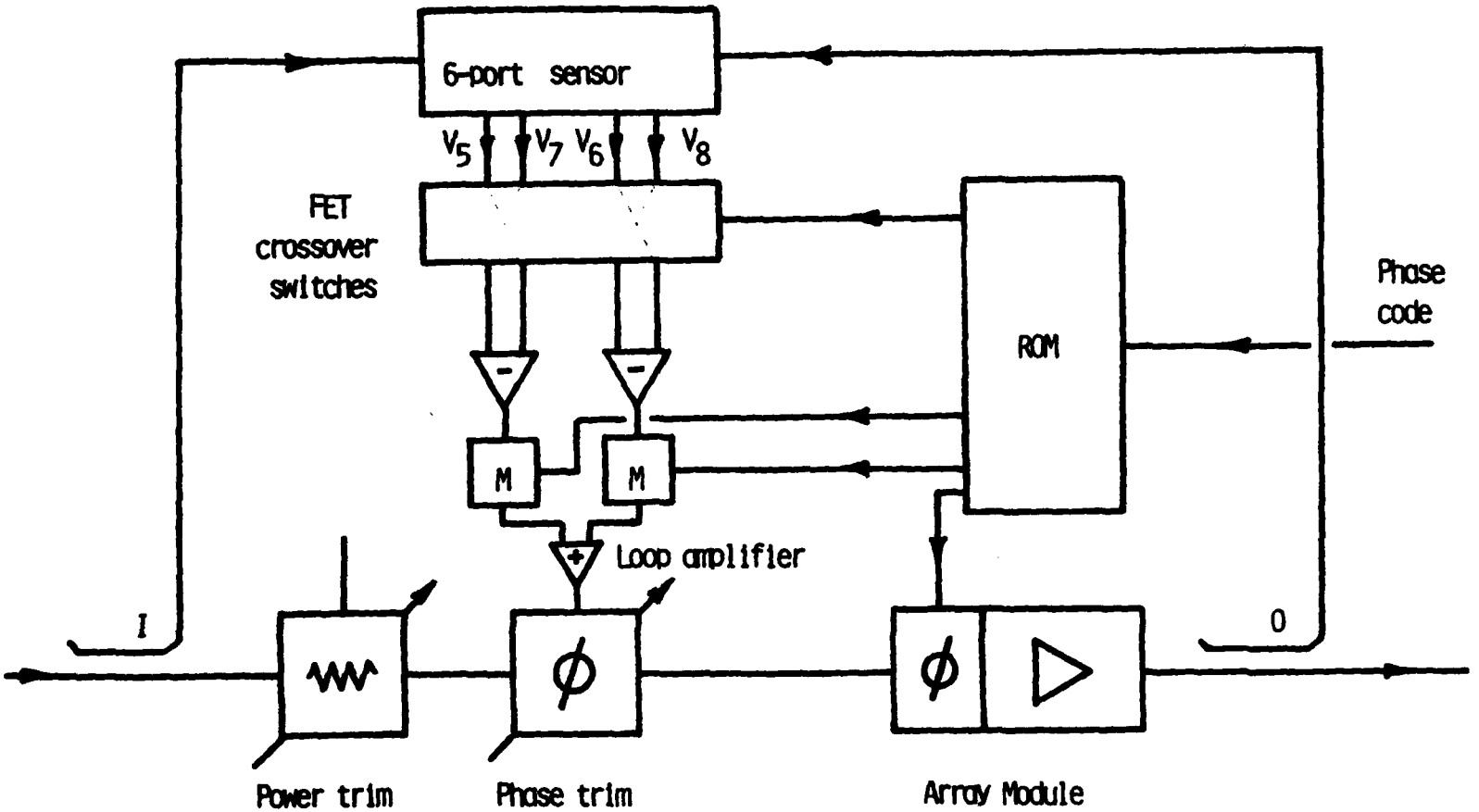

Fig.7: Schematic Diagram of the Phase Control Loop

M = Multiplying Digital-to-Analogue Convertor (MDAC)

control range of slightly greater than $2\pi/n$ where n is number of bits of control in the digital phase shifter. The scheme has the great advantage that a very crude, and therefore inexpensive, digital phase shifter may be used, the performance of which in terms of rms error and insertion phase variation from unit to unit would otherwise be unacceptable. Moreover, it would be unneccesary to provide more than 3 or 4 bits of control with the digital phase shifter, thereby minimising diode count and insertion loss. The control loop will provide the fine control, up to 8 bits if required. A simple feedback arrangement ensures that if the analogue phase shifter reaches either end of its control range, the digital phase shifter is incremented or decremented by 1 bit. The choice of the number of bits of control to be implemented with the digital phase shifter may be largely dependent on the range of control possible with the analogue phase shifter and also on factors such as amplifier slew rate, as mentioned before. However, in the case where fast real-time, possibly within-pulse, phase control is required, the range of the analogue phase shifter should encompass the range of likely "phase chirp" or dynamic phase variation. For example, in a power bipolar transistor, as a result of heat generation during the pulse, some 15^{o} - 20^{o} of phase change can occur {4}. In a multi-stage power amplifier, a capability of some 60^{o} analogue phase control would therefore be a sensible allocation.

This closed-loop phase control scheme has the additional application as a "retro-fit" to improve the accuracy of an existing digital phase shifter in a wide variety of systems.

In most cases, control of the signal amplitude, or equivalently the output power, is not as crucial as phase control, but if required fast amplitude correction could be achieved by a separate control loop which makes use of the relationship given in Equation 6. Under the assumption that a_1 represents the amplitude of the constant reference signal, the output power P_2 which is proportional to $|a_2|^2$ is simply represented by:

$$P_2 \propto \left[(V_5 - V_7)^2 + (V_6 - V_8)^2\right] \qquad (11)$$

The output power control loop would then be as shown in Fig. 8.

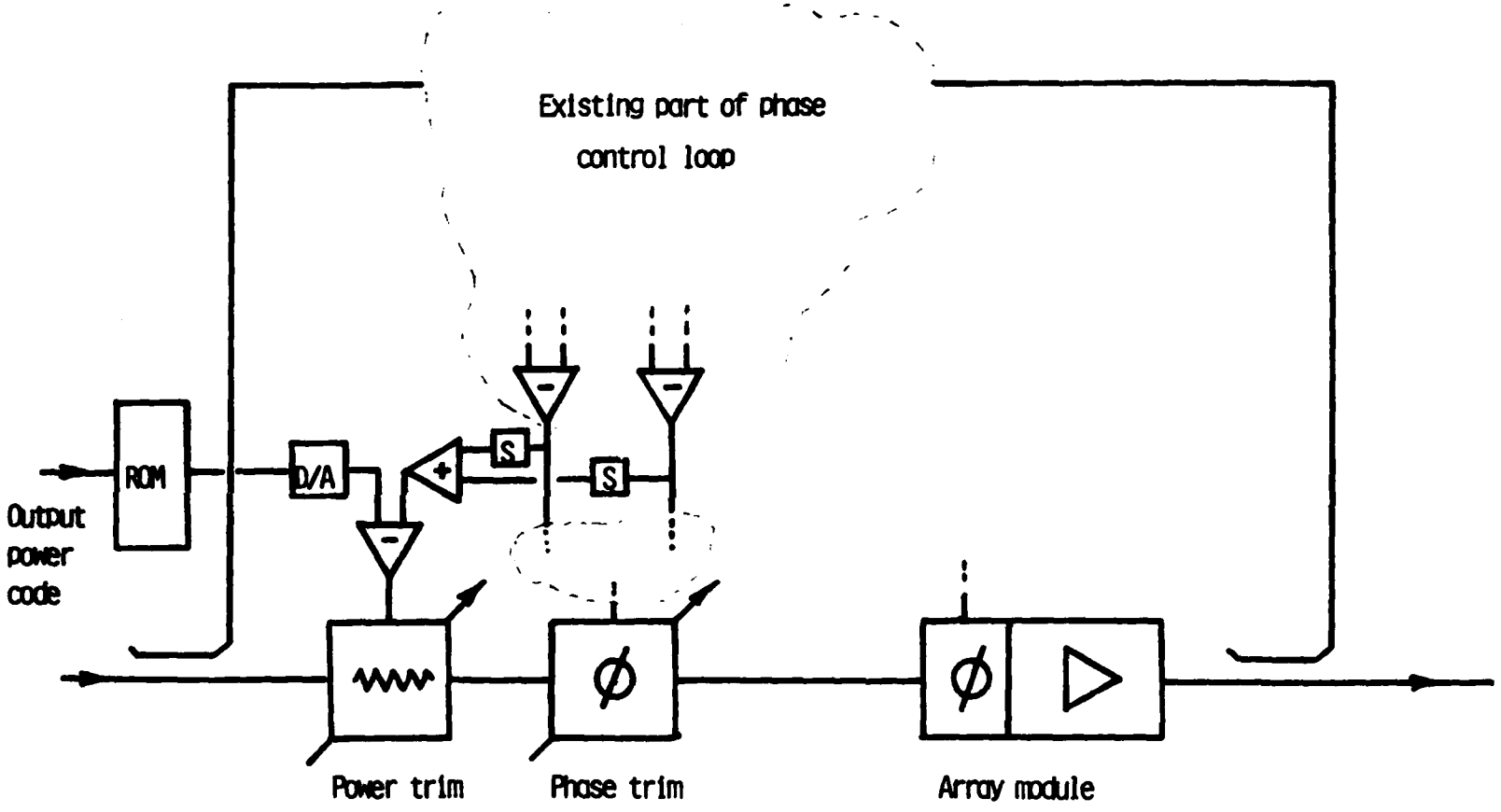

Fig.8: Schematic Diagram of the Output Power Control Loop

S = Analogue Circuit with Square-law Characteristic.

The required power is given as a digital input to the ROM, which then outputs through a D/A convertor an analogue voltage equal to the required value of $(V_5 - V_7)^2 + (V_6 - V_8)^2$, the constant of proportionality in Equation (11) being included as part of the calibration procedure. A differential amplifier with the D/A output and the actual measured value of $(V_5 - V_7)^2 + (V_6 - V_8)^2$ from the six-port network then provides the input for the voltage controlled attenuator governing the reference level input at the module.

The only alternative to analogue loop processing schemes for phase and output power control is to carry out all the operations digitally. A digital processing scheme would overcome any problems of drift or voltage offsets in analogue circuits, but at the penalty of being slow in operation. After digitisation of the measured voltages V_5, V_6, V_7 and V_8, the values of ϕ and a_2 can be calculated from Equations (6), (7) and (8) using a microprocessor; hardware based arithmetic, rather than software, would be used for the algebraic operations and a look-up table used for the sine and cosine conversions. From stored characteristics of the phase and amplitude control components in ROM, the appropriate control signals to the phase shifter and attenuator could be generated, as shown in Fig. 9.

In spite of the relatively slow response of a microprocessor-based system, involving a processing time of many milliseconds, this scheme facilitates development and testing of the logic which can later be implemented in a fast, dedicated hard-wired processor. In such a digital system, the effect of errors in the components (hybrids and divider) and variations in sensitivity between detectors may easily be compensated by input of information obtained in a simple calibration process, carried out on the six-port sensor and any other components used.

3. EFFECT OF ERRORS

3.1 Errors in the Six-Port Network

An assessment of errors is necessary to establish whether calibration routines are required and, if so, what form these must take.

The quadrature hybrids and in-phase divider cannot be perfect components and will in practice have amplitude and phase imbalance errors at the output. Certain definitions of these errors are used for commercially-available components {10}.

Insertion Loss (I.L.) - The net unrecoverable power in dB based on one-way transmission through the device.

Thus, for a quadrature hybrid:

$$I.L = 10 \log \left[\frac{P_I + P_Q}{P_{in}} \right]$$

where P_I = power output from in-phase coupled port

P_Q = " " " quadrature " "

P_{in} = total input power

Amplitude Imbalance (A.I.)- The difference in dB of the outputs with respect to the average output level.

Thus, for a quadrature hybrid, the amplitude imbalance at the quadrature port is:

$$A.I = 10 \log \left[\frac{2P_Q}{P_I + P_Q} \right]$$

Phase Imbalance ($\Delta\phi$) - The phase deviation from the ideal phase requirement (0° or 90°).

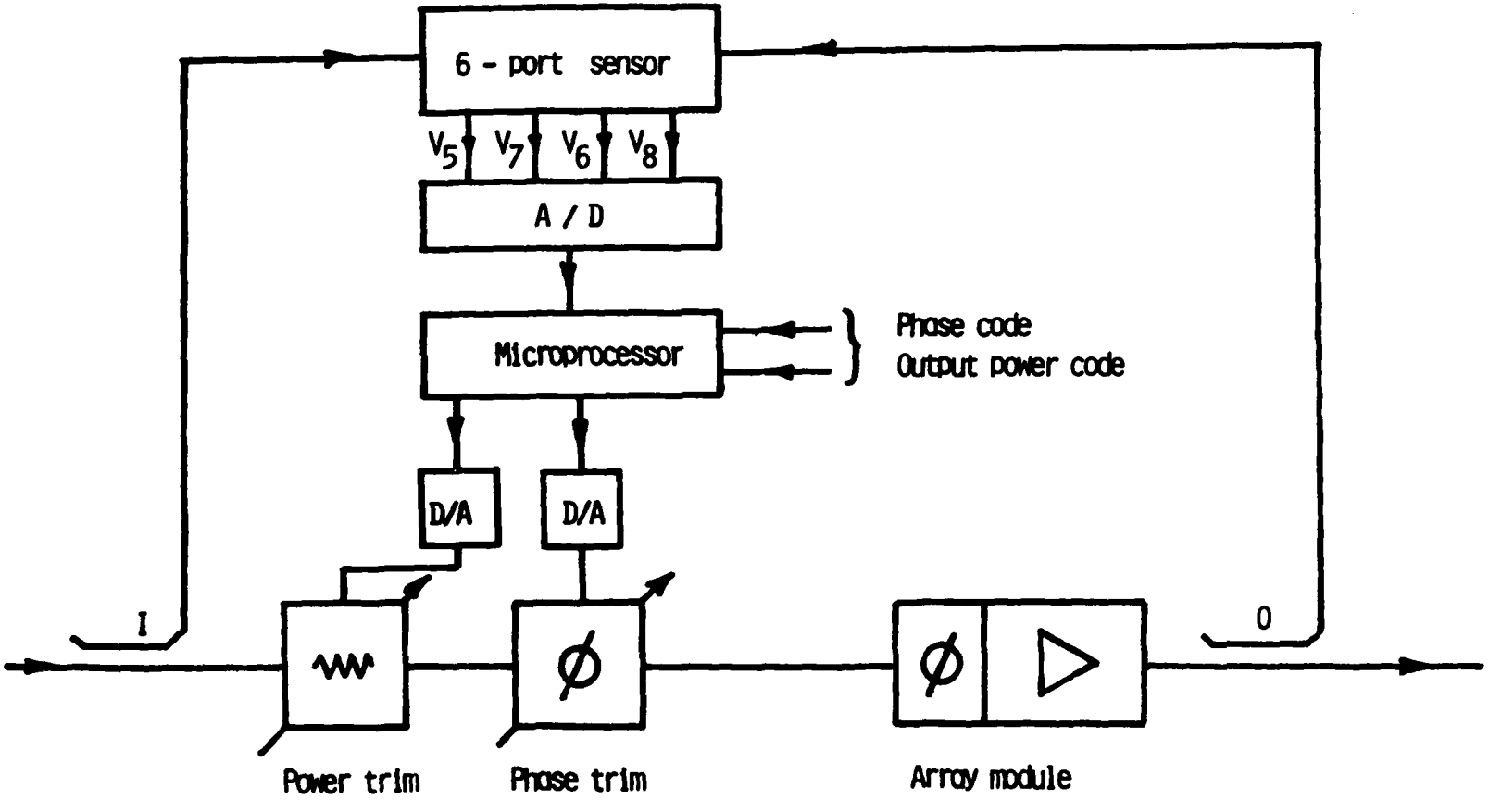

Fig.9: Schematic Diagram of Microprocessor-controlled Loop for Amplitude and Phase Correction

Commercially-available hybrids and in-phase dividers commonly achieve an amplitude imbalance of better than 0.5dB, a phase imbalance of better than 3^{o} and insertion loss of better than 0.5dB. Typically, such performance is maintained over at least a 10% bandwidth and in some cases may be possible over an octave or more.

By considering a defined amplitude and phase error at each of the output ports of the four dividers in the network of Fig. 3, the amplitude and phase of the signals appearing at ports 5 to 8 may be calculated. From these, through equations (6) - (8) the values of a_2 and ϕ may be calculated and then compared with the case where an error-free network is assumed. The calculations have been performed analytically for a couple of sets of error values, and then a computer program has been written to facilitate evaluation for a wide range of error combinations.

The results are summarised in Figs. 10 and 11. For three typical sets of errors in the dividers, Fig. 10 shows the variation of the error ε in the predicted value of the phase difference ϕ as a function of the value of ϕ over the 0^{o} to 360^{o} range. As might be expected, the peak error obtained is approximately the r.m.s. sum of the individual component errors in this case where the signals a_1 and a_2 have approximately equal magnitude. Fig. 11 shows the effect of a difference in magnitude, between a_1 and a_2 on the phase error. As might be expected, the phase error increases substantially as the difference in magnitude between a_1 and a_2 increases.

It is clear, therefore, that if the original accuracy requirement, namely 1^{o} and 0.1dB, for the system is to be achieved, some means for calibrating out errors will be necessary since it would not be expected that dividers and hybrids could in quantity be manufactured with significantly better tolerances than those currently available commercially.

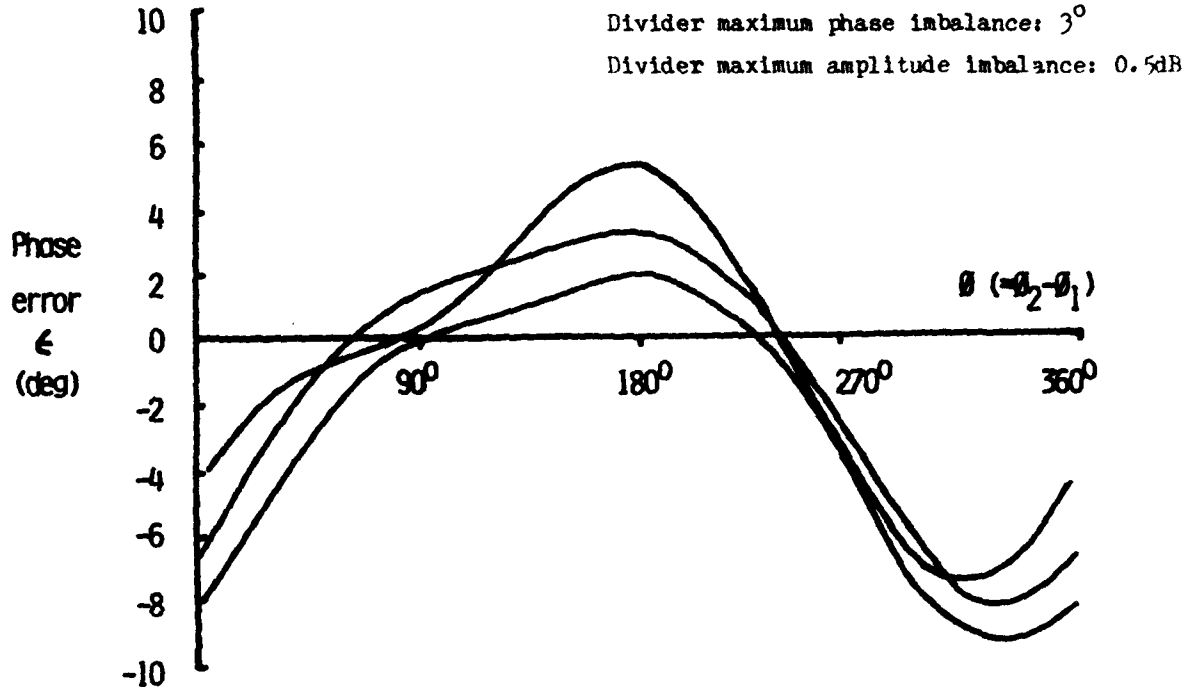

Fig.10: Phase Sensor Error as a Function of Input Signal Phase Difference
(curves show random choice of errors)

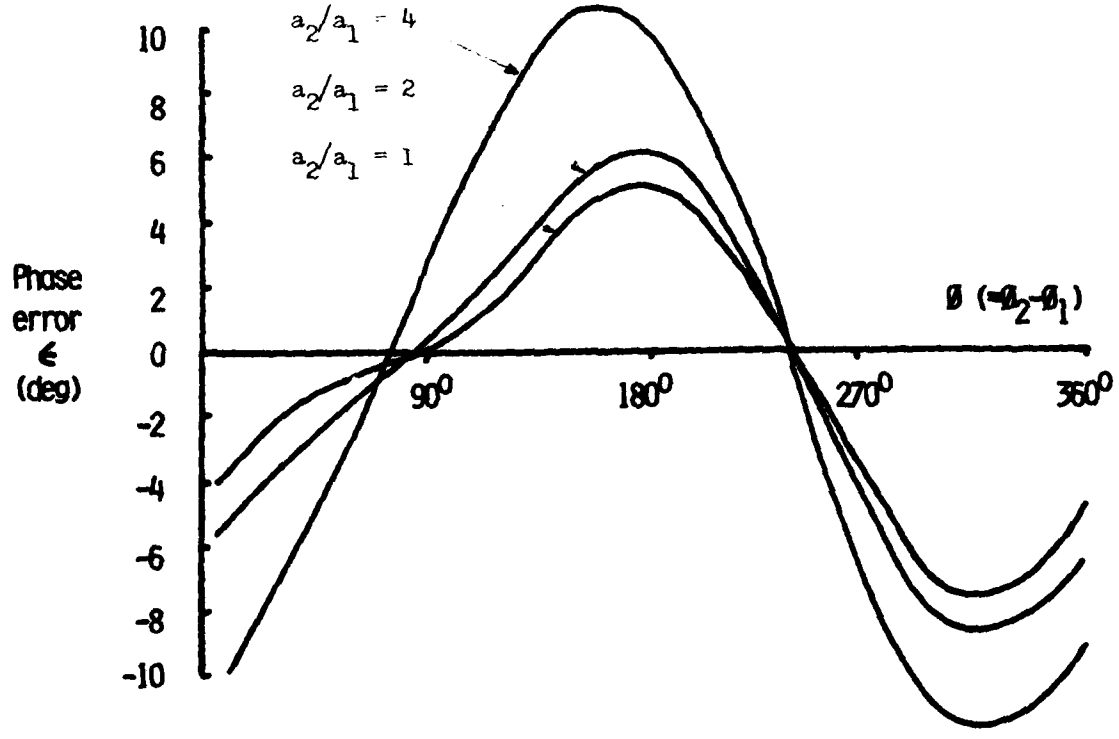

Fig.11: Effect of Input Signal Amplitude Difference on Sensor Phase Error

3.2 Errors in the Square-Law Detectors

A second source of error lies in the detectors. In the ideal case these were assumed to be exactly square-law and all diodes were assumed to have identical sensitivity. For most microwave measurement applications, a thermistor or bolometer is used as a microwave power sensor. Such devices, however, have a long thermal time constant (e.g. 100ms) and are therefore inapplicable in the present case. For fast measurements, the Schottky barrier diode (SBD) is the only satisfactory sensor that is in quantity production and relatively inexpensive.

The SBD exhibits a square law characteristic at very low power levels only (typically less than -20dBm) and the deviation from ideal square law behaviour depends very much on temperature. If a very wide dynamic range is required, it is important to know the exact detection law of the SBD above the -20dBm level. A general theoretical detection law for the SBD has been developed {11} and this takes into account the variation in the diode characteristics with temperature and d.c. bias. Temperature is a particularly important factor, since, in common with most semiconductor devices, the terminal characteristics vary appreciably with temperature.

The general equivalent circuit of an SBD is shown in Fig. 12. A shunt resistor R_1 of value approximately 50Ω is usually built in to the detector to improve the frequency response and VSWR; R_b and C_b are the equivalent circuit components representing the diode; R_p, L_p and C_p are the package equivalent circuit elements; R_L is the load resistance, V_b the d.c. bias voltage (if any) and C_o the capacitive loading on the output. Since $R_p \ll R_b$, $\omega L_p \ll R_b$ and $C_o \gg C_p$, C_b, the circuit may be simplified for all but very high frequencies to that shown in Fig. 13 where $C_1 = C_p + C_b$.

The value of R_b is usually expressed in the form of a current

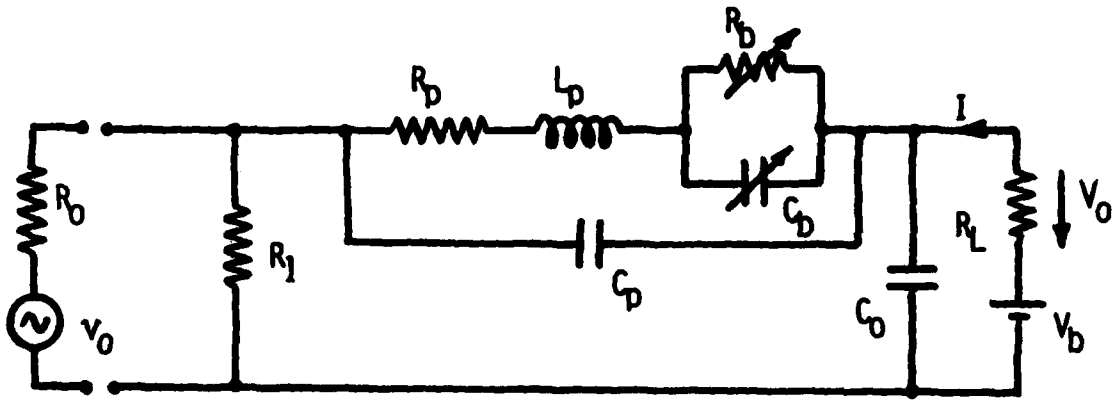

Fig.12: General Equivalent Circuit of a Schottky Barrier Detector (SBD)

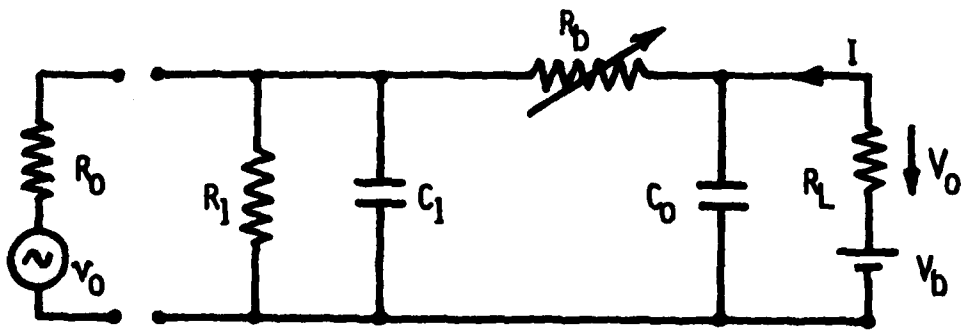

Fig.13: Simplified Equivalent Circuit

voltage law:

$$i = f(v) = I_s \exp\left[\frac{q\,v}{nkT} - 1\right] \tag{12}$$

where q is the electronic charge, k is Boltzmann's constant, T is the absolute temperature, n is the ideality factor and I_s is the reverse saturation current of the SBD.

A more accurate description of the law is, however:

$$i = f(v) = I_s \exp\left(\frac{q\,v}{nkT}\right)\left[1 - \exp\left(-\frac{q\,v}{kT}\right)\right] \tag{13}$$

The two relationships are identical if n = 1, and the difference between them is negligible if $v >> nkT/q$. For small signal levels, if n departs from unity, the difference can be important.

The quantities I_s and n are important parameters for the SBD. They can be expressed in terms of temperature and a set of constants a, b, c, d through:

$$I_s = aT^2 \exp\left(-b\,\frac{q}{kT}\right) \tag{14}$$

$$\frac{1}{n} = 1 - c\left(d - \frac{kT}{q}\right)^{-3/4} \tag{15}$$

Figs. 14 and 15 show the variation of I_s and n with temperature determined from measured i/v characteristics and the use of equation (13). Good agreement is found with the relationships of equations (14) and (15) using a best-fit determination of the constants a, b, c, d.

The voltage, v, appearing across the SBD consists of a d.c. component, V, and an a.c. component v_1 at the microwave frequency ω_1. To avoid added complexity in the present system, unbiased

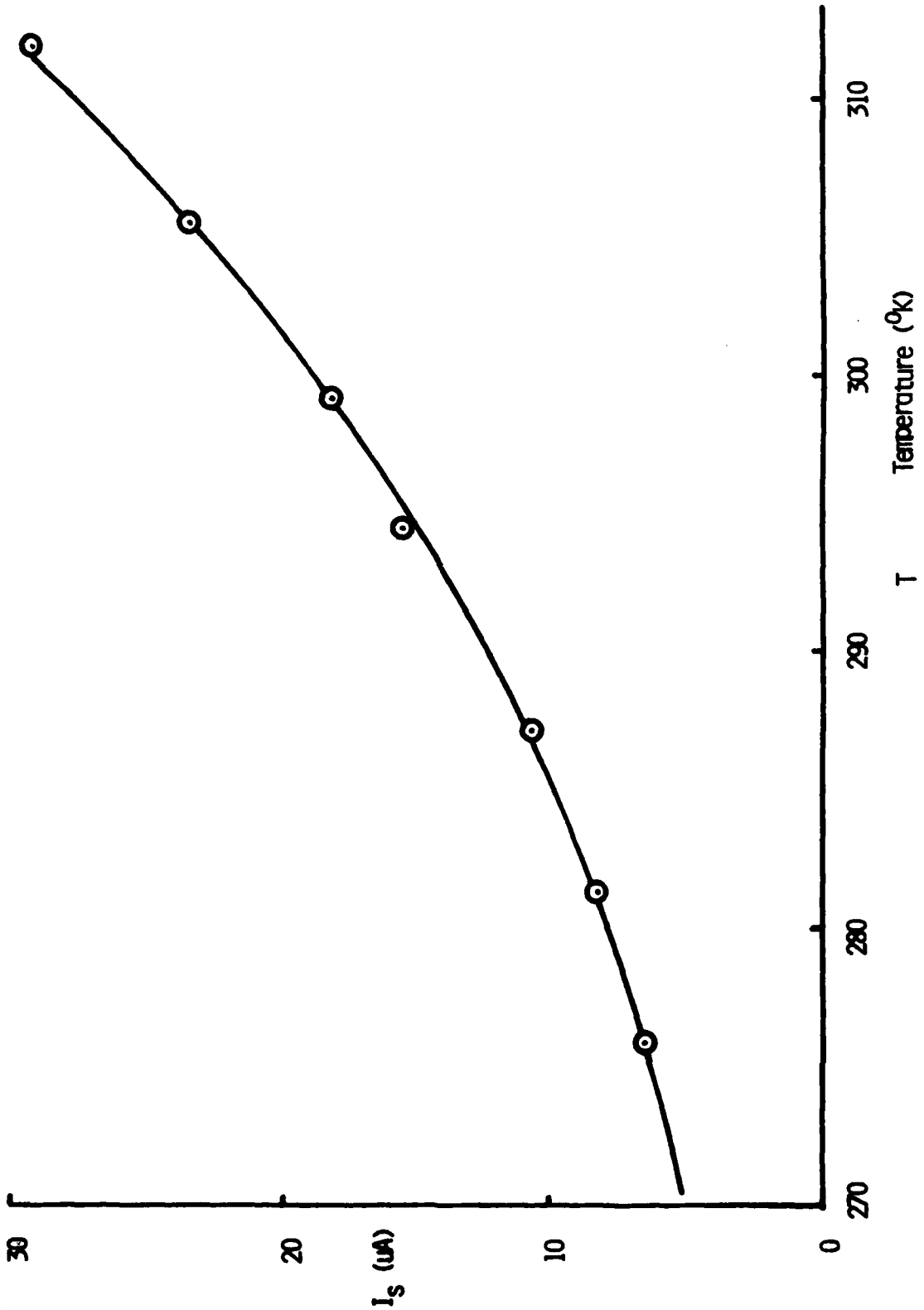

Fig.14: Variation of Reverse Saturation Current, I_s, with Temperature

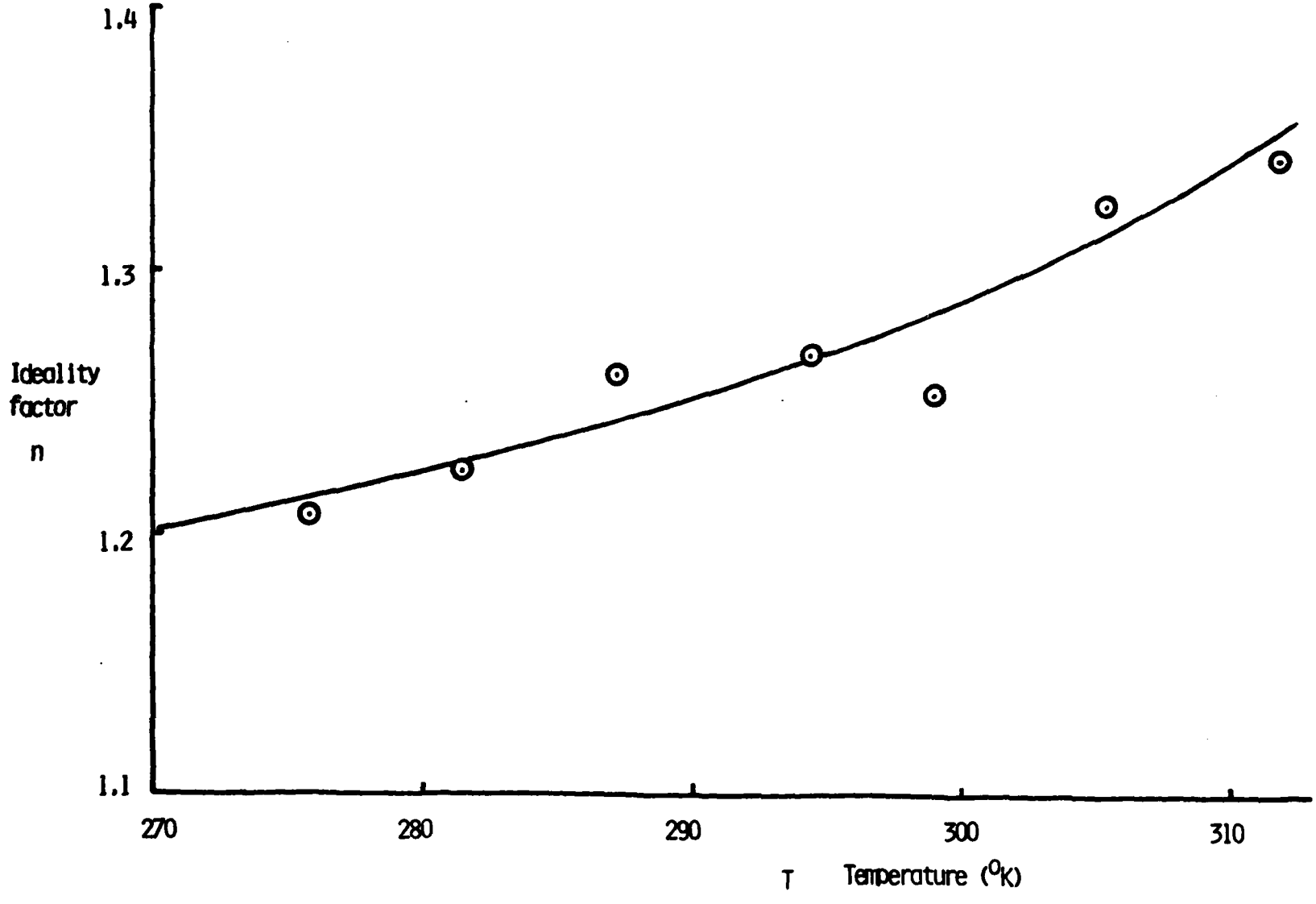

Fig.15: Variation of Ideality Factor, n, with Temperature

detectors will be considered. Thus, in Fig. 13:

$$v = V + v_1$$

$$= - I.R + Bv_o \cos(\omega_1 t - \theta) \qquad (16)$$

where $B = \left[1 + \frac{R_o}{R_1} + \frac{R_o}{R_b}^2 + (R_o \omega_1 C_1)^2 \right]^{1/2}$

$$\theta = \arctan \left(\frac{\omega_1 C_1}{\frac{1}{R_o} + \frac{1}{R_1} + \frac{1}{R_b}} \right) \quad \text{and} \quad R = R_L + \frac{R_o R_1}{R_o + R_1}$$

with R_o as the value to match the r.f. source (50Ω). From a substitution of equation (16) into equation (13), the d.c. component I of the current is obtained as:

$$I = I_s \exp\left(\frac{qV}{nkT}\right) I_o\left(\frac{qBv_o}{nkT}\right) - I_s \exp\left[\frac{(1-n)}{n}\frac{qV}{kT}\right] I_o\left[\frac{(n-1)}{n}\frac{qBv_o}{kT}\right] \qquad (17)$$

where $I_o(x)$ is the modified Bessel function of argument x. Since the d.c. output voltage $V_o = IR_L$, a general detector law may be obtained as a transcendental equation:

$$V_o = I_s R_L \left\{ \exp\left(\frac{-q\alpha V_o}{nkT}\right) I_o\left(\frac{qBv_o}{nkT}\right) - \exp\left[\frac{-(1-n)}{n} \cdot \frac{q}{kT} \alpha V_o\right] I_o\left[\frac{(n-1)}{n} \cdot \frac{qBv_o}{kT}\right] \right\} \qquad (18)$$

where $\alpha = 1 + \frac{R_o R_1}{R_L(R_o + R_1)}$

and the input microwave power P_{in} is related to v_o through

$$P_{in} = \frac{(Bv_o)^2}{2R_i} = \frac{B(1-B)v_o^2}{2R_o} \qquad (19)$$

since the input resistance of the detector at r.f. is given by

$$R_i = \frac{B}{1-B} \cdot R_o$$

Fig. 16 shows a comparison between the measured d.c. output voltage as a function of input r.f. power and the theoretical output voltage derived from equation (18). SBD detection law measurements were carried out to high accuracy by comparison with a standard barretter square law detector. A resolution of 0.001dB in the ratio of outputs between the SBD and the standard detector for equal input power in parallel channels was achieved, permitting an assessment of the deviation from square law behaviour of the SBD to much better than 1% accuracy.

Since equation (18) has been validated as regards good agreement with experimental results, it may therefore be used to determine the errors in the six-port measurement arising from non-ideal square law detector characteristics. Further analysis has shown that detector errors can also arise due to second harmonic content in the input signal. For many applications, a simple filter may be used to reduce the level of an second harmonic signal to negligible levels; the effect of harmonic signals are particularly serious if the input power to the detector is high. At 100μW input power level, a 1% second harmonic content would cause approximately 10% error in the d.c. output voltage from the detector.

Equation (18) may also be used to assess the variation of the detector characteristic with temperature. For low values of input microwave power (e.g. less than about 10μW), such that

$$x = \frac{qBv_o}{nkT} \leq 2, \text{ then } I_o(x) \simeq 1 + \frac{x^2}{4} + \frac{x^4}{64}$$

and a closed-form approximation to equations (18) and (19) may be

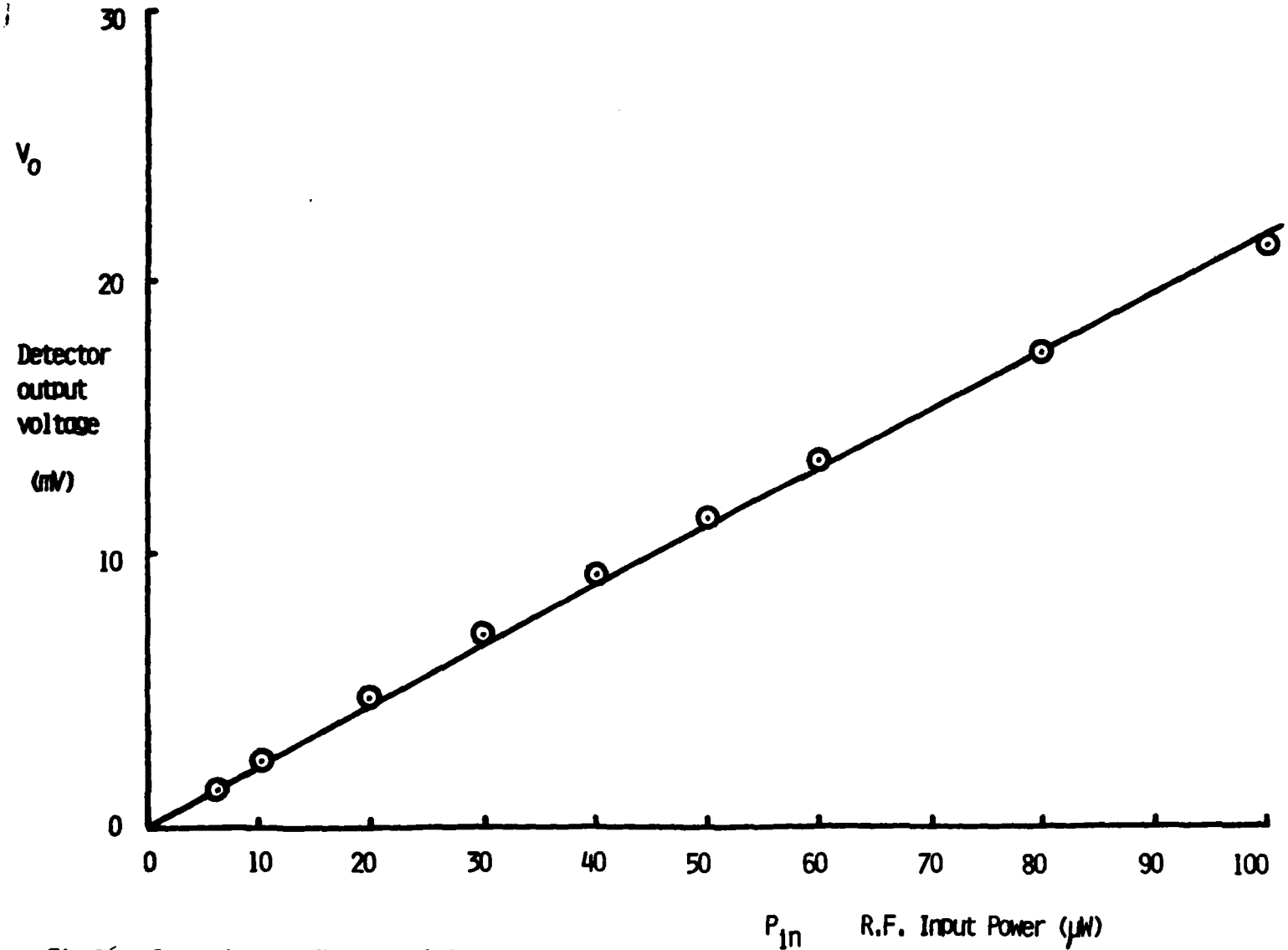

Fig.16: Comparison of Theory and Experiment for the SBD

obtained relating P_{in} and V_o

$$P_{in} = \frac{(n-1)^2 D - 1 + \left\{ \left[(n-1)^2 D - 1 \right]^2 - \left[1-(n-1)^4 D \right] \left(1 - \frac{V_o}{I_S R_L} D^{1/n} - D \right) \right\}^{1/2}}{\left[1 - (n-1)^4 D \right] R_o \left(\frac{q}{nkT} \right)^2 \frac{B}{4(1-B)}} \qquad (20)$$

with $D = \exp\left(\frac{qV_o}{nkT}\right)$

The calculated variation of detector sensitivity, K_p ($= V_o / P_{in}$) with temperature is shown in Fig. 17; this is obtained from equations (14), (15) and (20). It may be seen that there is a region of some 30K around 300K ambient, where the sensitivity changes by only a few percent. Outside this range, however, the sensitivity dependence on temperature is very severe.

It may be seen from equations (4), (5), (7) and (8) that a change in detector sensitivity, if uniform across all detectors in the six-port network, does not affect the accuracy of phase determination. Equation (11), however, shows that the measurement of power would be affected strongly by this change in detector sensitivity.

3.3 Control Loop Errors

A finite error always exists in control loops and this is a function of the loop gain, involving the sensitivities of the sensor, control elements and the gain of the loop amplifier.

Fig. 18 shows the system simplified for loop analysis. The following equations describe the loop:

$$V_d = -K_d (\phi_o - \phi_i - \phi_s) \qquad (21)$$

in which the negative sign, corresponding to the appropriate sense of slope at the phase detector zero crossing, is the stable condition. ϕ_o, ϕ_i and ϕ_s are the output phase, input reference phase and the required output phase respectively. K_d is the

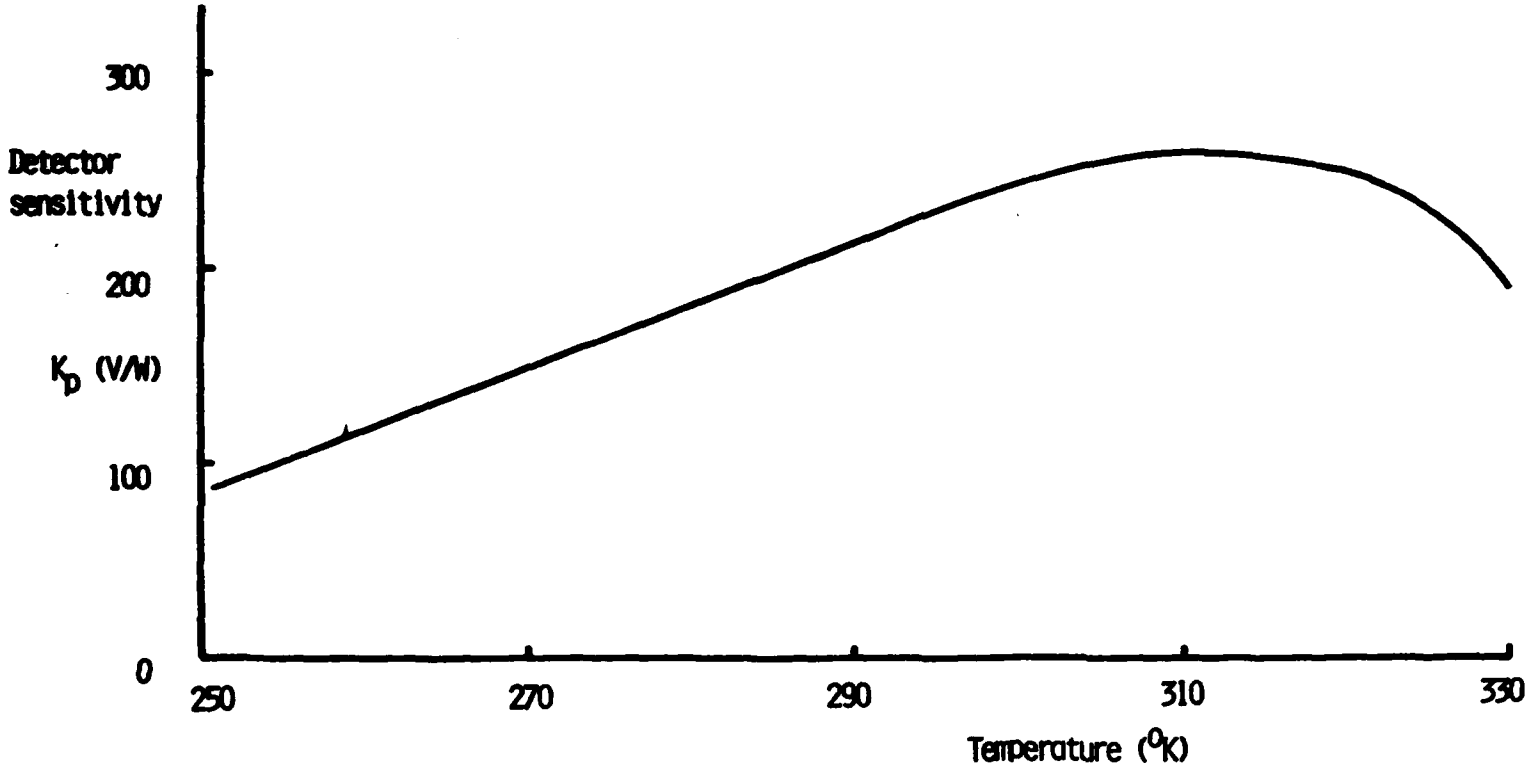

Fig.17: Theoretical Variation in SBD Sensitivity with Temperature

phase detector constant, which for small values of phase difference may be obtained from a small-angle linearisation of equation (5) and related to the detector sensitivity K_p in equation (2).

$$\phi_o = \phi_i + \phi_t + \phi_m \tag{22}$$

where ϕ_t is the phase shift introduced by the analogue phase trimmer and ϕ_m is the phase shift introduced by the module. The analogue phase shifter characteristic, K_ϕ, in radians per unit voltage then completes the loop parameters.

$$\phi_t = K_\phi K_a V_d \tag{23}$$

where K_a is the voltage gain of the d.c. coupled loop amplifier.

The closed-loop phase error ϕ_e then is given by:

$$\phi_e = \phi_o - \phi_i - \phi_s \tag{24}$$

From equations (21), (22) and (23):

$$\phi_o - \phi_i = - K_d K_a K_\phi (\phi_o - \phi_i - \phi_s) + \phi_m$$

$$\therefore \quad (\phi_o - \phi_i - \phi_s)(1 + K_d K_a K_\phi) + \phi_s = \phi_m$$

and then $$\phi_e = \frac{\phi_m - \phi_s}{1 + K_d K_a K_\phi} \tag{25}$$

To this must be added any error in the phase discriminator itself and therefore

$$\phi_e = \frac{\phi_m - \phi_s}{1 + K_d K_a K_\phi} + \text{(phase discriminator error)} \tag{26}$$

Taking some typical values : $K_d \simeq 1mV/rad$ (detectors in square law region; $P_{in} << 10\mu W$); $K_\phi \simeq 1rad/V$ (dual gate FET phase shifter {3, 12, 13, 14}); $\phi_m \simeq 22^o$ (maximum random error introduced by module and its associated digital phase shifter). It is then seen that a loop amplifier d.c. gain of 10^5 (100dB), which can be provided by a commercially available fast operational amplifier, can reduce the steady-state phase error by a factor of 100, to 0.2^o.

The conclusion from the loop analysis is that the steady-state phase error will be primarily governed by the phase discriminator error, namely by the constraints discussed earlier for the six-port network and the diode detectors.

4. EXPERIMENTAL WORK

Both the analogue and digital control techniques have been investigated through a series of initial experiments. Because of current interest in S-Band phased array modules within the Department, the frequency range 2.7 - 3.1 GHz was chosen for the investigations.

4.1 Digital Control Loop

The basis for the system, the overall form of which was given in Section 2 and Fig. 9, was a commercial single-board Z-80 microprocessor with 2.5 MHz clock rate and 16 K bytes of dynamic RAM. Because execution speed was not of prime importance in the system development, the program instructions were written in BASIC rather than in machine code.

The four Schottky diode power sensors (Type DA 3010) were sampled sequentially and the outputs, after buffering and amplification, multiplexed into a 12 bit A/D convertor. The convertor ran at a clock frequency of 1 MHz and used a quad slope integration method

to achieve conversion within a time of about 40mS.

The characteristics of each of the Schottky diode detectors were taken into account by prior calibration of each detector over the range of frequencies against a standard thermistor detector of better than 1% accuracy. All calibrations and subsequent experiments were carried out in the normal relatively constant laboratory temperature environment, so no account was taken of temperature variations.

Calibration of the six-port network characteristics was also carried out over the range of frequencies to an accuracy of approximately 1^{o} and 0.1dB, using a Hewlett Packard Microwave Analyser. The network itself, consisting of three quadrature hybrid Lange type {15,16,17} couplers and an in-phase Wilkinson divider was etched in microstrip form on a single 4" square piece of RT Duroid (0.025" thick, relative permittivity 2.33). Each 3dB coupler was fabricated as two 8.33dB couplers in series; though this increases the space involved, tolerances on the coupler dimensions are relaxed. The diodes were connected to the substrate via SMA connectors.

A commercial multi-stage varactor controlled analogue phase shifter was used as the phase control element. This provided a $0-2\pi$ range of phase control as a function of control voltage. The characteristics of this phase shifter, namely insertion phase as a function of frequency and control voltage were measured using the Network Analyser and again stored in the memory associated with the microprocessor.

The complete system was tested in the following way:

(a) an equiphase signal was injected into the two sampling ports of the system and a final calibration run carried out over the frequency range to take account of any line lengths and connector effects between components.

(b) the sampling ports of the system were connected either side of a known length of line and the analogue phase shifter in series. It was then verified, using the Network Analyser, that the phase shifter, under microprocessor control, corrected for the insertion phase of the length of line and that the phase difference between the sampling ports tracked, over the range of frequency, the required phase setting value taken as data input to the microprocessor.

The system accuracy was found to be close to the 1^{o} value taken in the initial specification. No attempt has yet been made to control amplitude (or equivalently the insertion gain or loss between the sampling ports), but this could be implemented by means of a digitally controlled attenuator.

The time taken for the system to adjust phase is long, typically of the order of 0.5s. An estimate of the phase correction time with a dedicated hardware system replacing the microprocessor is still of the order of tens of ms. Though the required accuracy can be achieved with this all-digital approach, it will be too slow for most real-time phase and amplitude correction applications.

4.2 Analogue Control Loop

This system follows the scheme outlined in Section 2 and Fig. 7. The same six-port network as described in Section 4.1 was used. The diode outputs after passing through FET switches and buffer amplifiers were subtracted in fast differential operational amplifiers (Plessey SL541) and multiplied by two 8-bit digital words in the multiplying digital-to-analogue convertors (DAC 0800). The weighted outputs were then added and amplified further in a fast operational amplifier (Plessey SL541) before driving the control input of a dual-gate FET phase shifter. The phase shifter characteristics are similar to those found by other authors {3,12,13,14}; they are non-linear and frequency dependent, but this non-linearity and frequency dependence only affects the loop gain and does not greatly influence the resulting phase

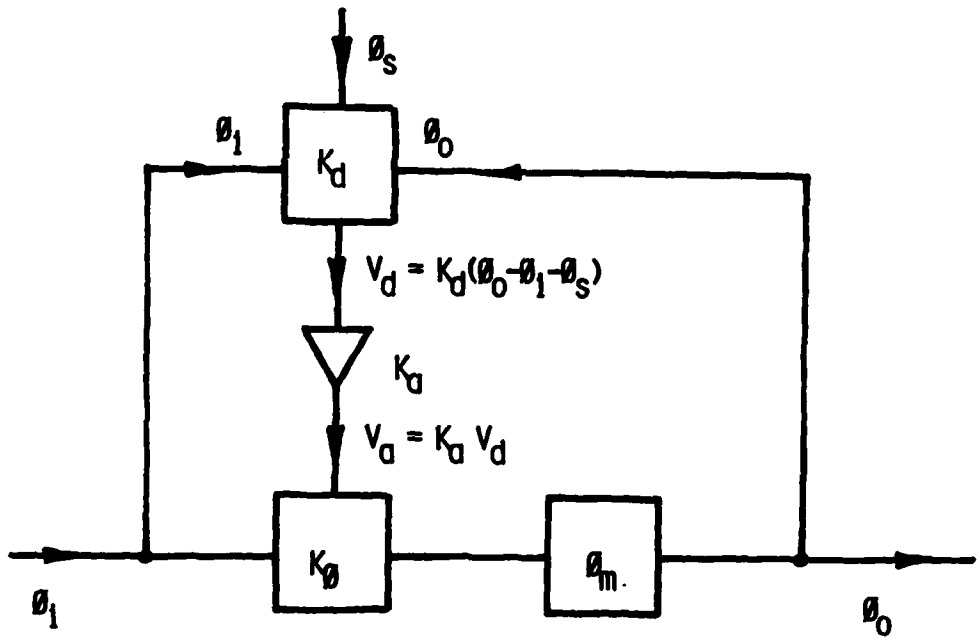

Fig.18: Schematic Diagram of the Phase Control Loop

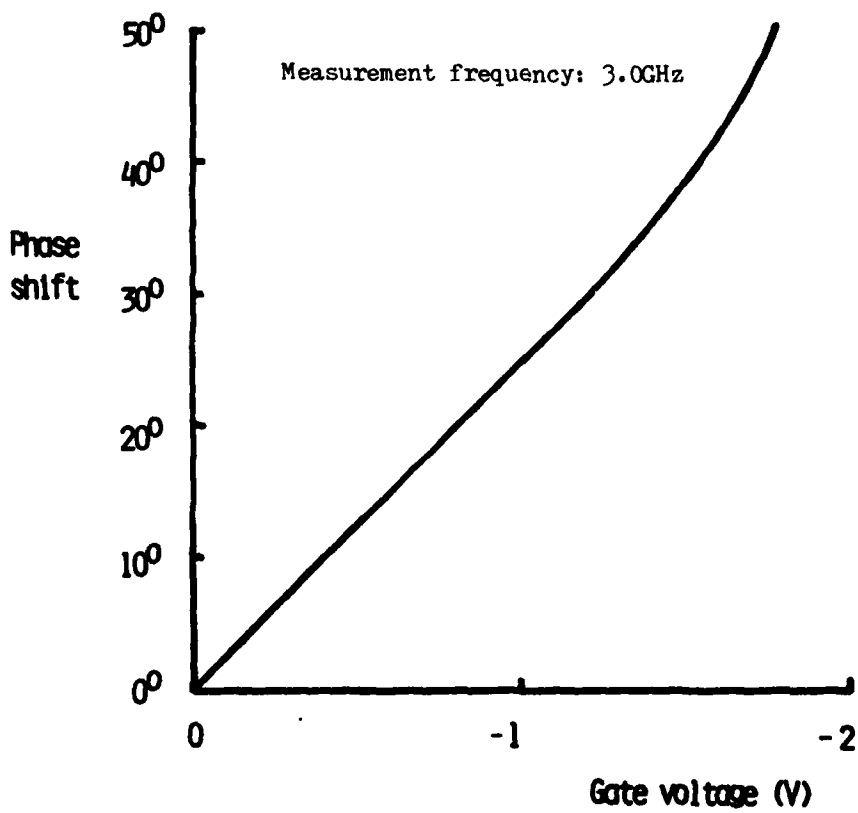

Fig.19: Phase Shift vs. Gate Voltage Characteristic for the Dual-gate FET Phase Shifter

error of the system. A typical measured phase shifter characteristic is shown in Fig.19.

The module to be controlled was an S-Band active phased array element with a 4-bit pin diode phase shifter. In open loop configuration, this phase shifter achieves some 10^{o} rms error and the array module itself shows some 30^{o} of phase variation during a pulse, associated with heating of the power bipolar transistors, if the maximum possible power output is used.

The system was first calibrated by the following procedure. The phase difference between the signals at input and output sampling points, which were approximately at the same power level, were monitored by a Network Analyser as well as being connected to the six-port network and control loop. A 6-bit phase control word was assumed as the input data format, giving phase specification to approximately 5^{o}. The most significant four bits were routed to the 4-bit phase shifter and, with the control loop disabled (phase trim setting at 0^{o}), the control word bit patterns for successive increments of approximately $22\frac{1}{2}^{o}$ over the range 0 360^{o} between I and O ports were found. An EPROM was then programmed to provide these control words to the phase shifter. This procedure takes account of the extra insertion phase introduced by the module. The full information of the 6-bit phase control word was decoded to provide the value of k and hence two multiplying factors of equations (9) and (10), required by the MDAC's. The null of the phase detector has then been set to the required phase.

Fig. 20 shows the performance of the system in open and closed-loop configurations. Fig. 20(a) shows the open-loop phase shift through the module during a 1 μs pulse. Approximately 30^{o} of phase shift is recorded. Fig. 20(b) shows closed loop control and it is seen that the phase is dynamically corrected in less than 200ns. The corrected phase value is within 2^{o} of that specified by the 6-bit phase word.

No attempt has so far been made to implement amplitude control, but this would be a relatively straightforward extension of the present techniques.

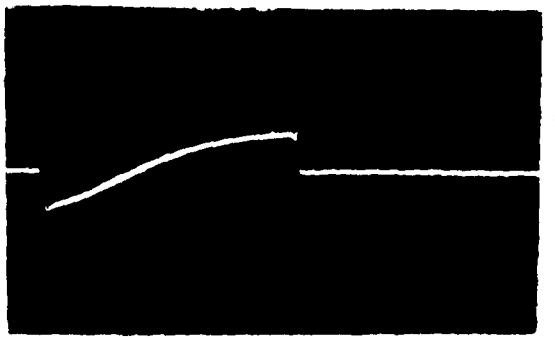

Fig.20a: Phase Shift during a 1μs pulse with Module Open-loop
(Maximum power output used to enhance phase shift)

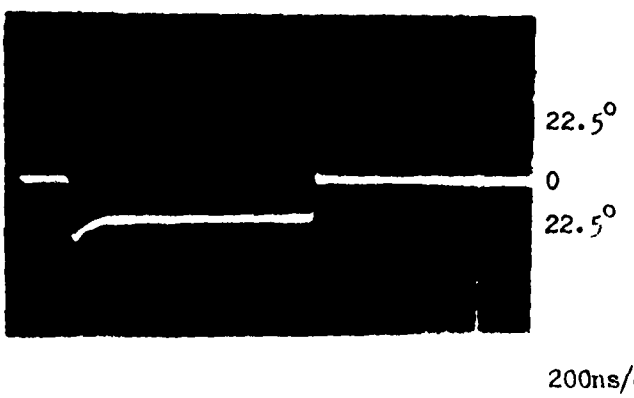

Fig.20b: Phase Shift during a 1μs pulse with Analogue Loop Control
(Phase command: $22\frac{1}{2}^{o}$)

These initial results show considerable promise. Though the 1^{o} phase accuracy cannot yet be guaranteed, it is likely that some simple calibration procedures to adjust the value of the multiplying factors into the MDAC's may achieve this. The earlier conclusions that the phase discriminator error would determine the overall error appear to be justified.

5. CONCLUSIONS

The work over this first one-year period has demonstrated the viability of closed-loop phase control to improve the accuracy of digital phase shifters or provide real-time, dynamic correction of output phase in active phased array modules.

A fully-digital control method satisfied the original design requirements, but is too slow for dynamic, within-pulse correction in active array modules.

The analogue loop approach is much simpler, with a relatively low component count, and is close to achieving the required accuracy.

6. FUTURE WORK

The work in the next one-year period (Feb 82-Feb 83) will concentrate on the following areas:

(a) accuracy improvement in the analogue loop scheme to achieve less than 1^{o} phase error.
(b) integration of the six-port sensor and beam lead Schottky diodes on a single microwave substrate less than 2" square.
(c) construction and test of the amplitude control loop.
(d) detailed performance measurements over a wide range of temperature and frequency.

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8. REFERENCES

{1} J.R. Forrest, J. Austin, A.A.de Salles and J.G.Schoenenberger.: "Design Considerations for Phased Array Modules", Final Technical Report, RADC-TR-80-354, Rome Air Development Center AFSC, Griffiss AFB, New York 13441 (Nov. 1980).

{2} J. Austin and J.R. Forrest.: "Design Concepts for Active Phased Array Modules", Proc. IEE, 127, Pt.F (CRSP), No. 4, pp. 290-300 (Aug. 1980).

{3} R.S. Pengelly.: "GaAs Monolithic Microwave Circuits for Phased Array Applications", Proc. IEE, 127, Pt. F(CRSP), No.4, pp. 301-311 (Aug. 1980).

{4} C.J. Ward, J.R. Forrest, P. Malamis, A.A.de Salles, M.E. Brinson and A.J. Parsons.: "High Phase Accuracy Active Phased Array Module for Multi-function Radars", Proc. IEEE MTT-S Symposium, Dallas, (June 1982).

{5} C.J. Ward.: "Delay Reduction Techniques in Phase-locked Loop Amplifiers", Electronics Letters, 17, No.7, pp. 253-255 (April 1981).

{6} C.A. Hoer.: "Using Six-port and Eight-port Junctions to Measure Active and Passive Circuit Parameters", National Bureau of Standards, Technical Note No. 673 (Sept. 1975).

{7} G.F. Engen.: "Determination of Microwave Phase and Amplitude from Power Measurements", IEEE Trans. IM-25, pp. 414-418, (Dec. 1976).

{8} A.L. Cullen, S.K. Judah and F. Nikravesh.: "Impedance Measurement using a Six-port Directional Coupler", Proc. IEE, 127, Pt. H(MOA), pp. 92-98 (1980).

{9} R.J. Collier.: "A Millimetre-wave Six-port Reflectometer using Image Guide", IEE Colloquium on Microwave Measurement (20 May 1981).

{10} Anaren Data Book and Catalogue.

{11} A.L. Cullen and T.Y. An.: "Microwave Characteristics of the Schottky Barrier Diode Power Sensor". To be published in Proc. IEE, 129, Pt. H(MOA) (1982).

{12} M. Kumar, R.J. Menna and H.C. Huang.: "Broad-band Active Phase Shifter using Dual-gate MESFET", IEEE Trans. MTT-29, No. 10, pp. 1098-1102 (Oct. 1981).

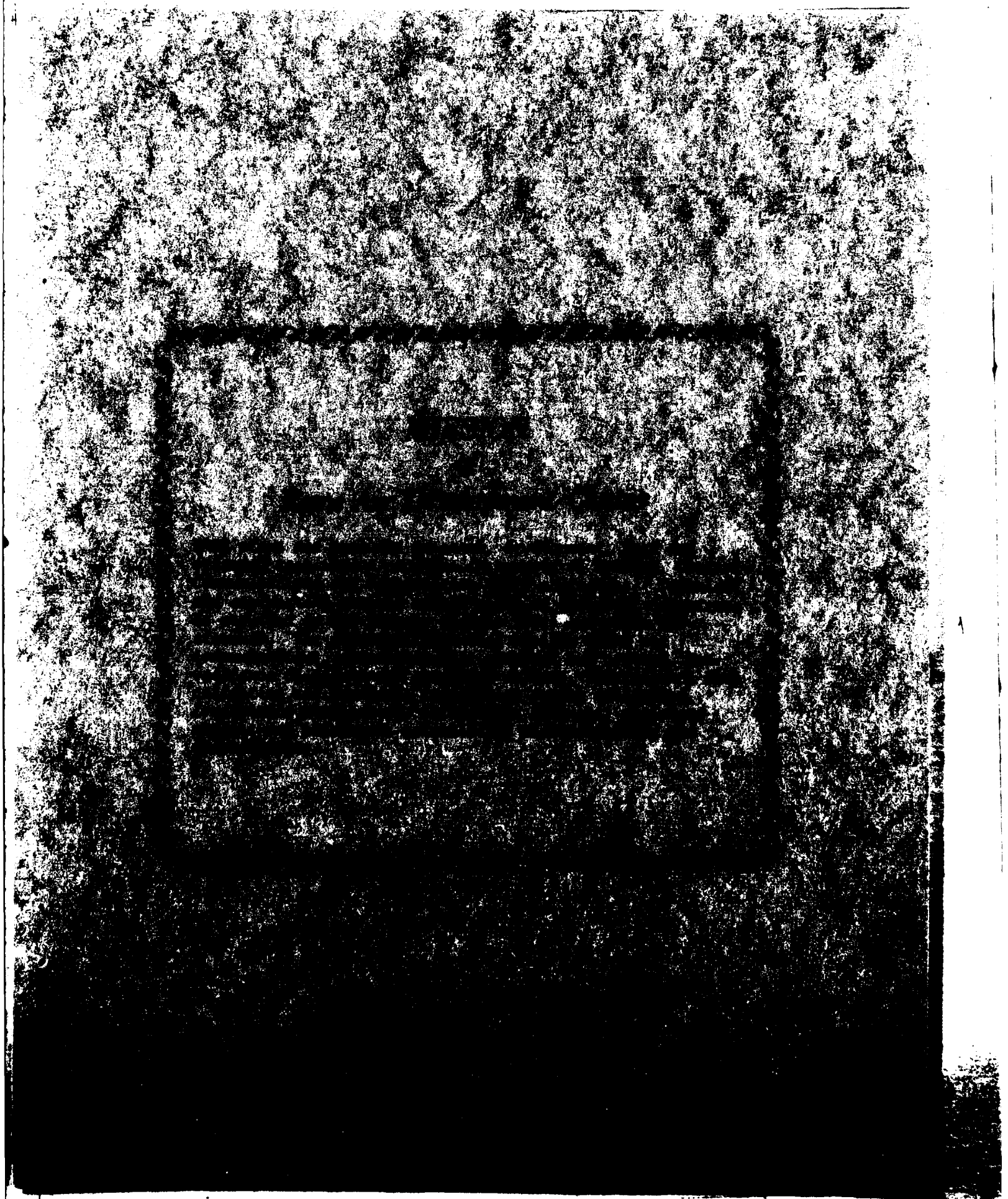
{13} C. Tsironis and P. Harrop.: "Dual-gate MESFET Phase Shifter with Gain at 12GHz", Electronics Letters, 16, No. 14, pp. 553-554 (July 1980).

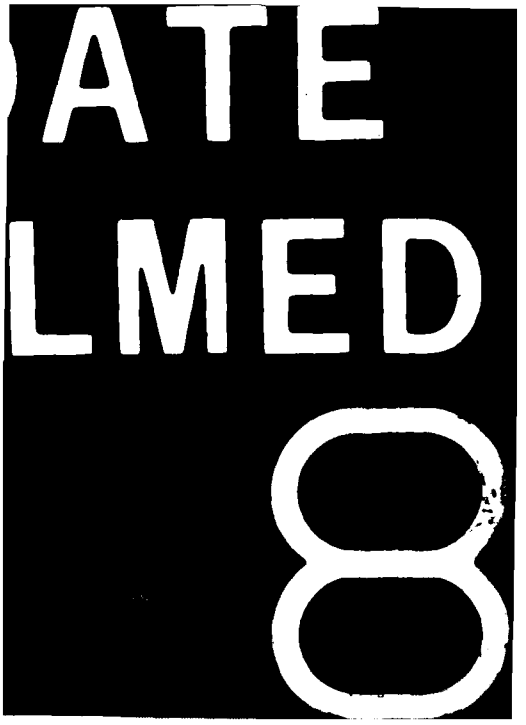
{14} R.S. Pengelly.: "Performance of Dual-gate GaAs MESFETs as Phase Shifters", IEEE Int. Solid State Circuits Conf. Digest, pp. 142-143, New York (1981).

{15} J. Lange.: "Interdigitated Stripline Quadrature Hybrid", IEEE Trans. MTT-17, No.12, pp. 1150-1151, (1969).

{16} S.J. Hewitt and R.S. Pengelly.: "Design Data for Interdigital Directional Couplers", Electronics Letters, 12, No.3, p.86 (Feb. 1976).

{17} W.P. Ou.: "Design Equations for an Interdigital Directional Coupler", IEEE Trans. MTT-23, pp. 253-255 (Feb. 1975).

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