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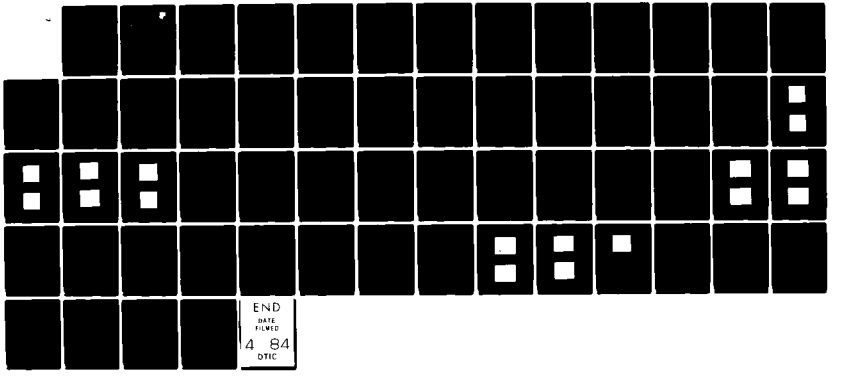

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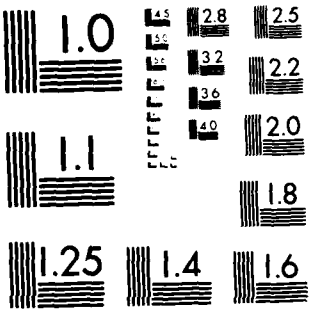

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AD A138648

RADC-TR-83-210
Final Technical Report
December 1983

SIGNAL PROCESSING CIRCUIT DEVELOPMENT

Northeastern University

B. L. Cochrun

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This report covers the design, fabrication and evaluation of three testbed modules: Linear imaging 256 element (LIRCCD), Area imaging 32 x 64 element (2DIRCCD) and a serial analog delay module (SADL).

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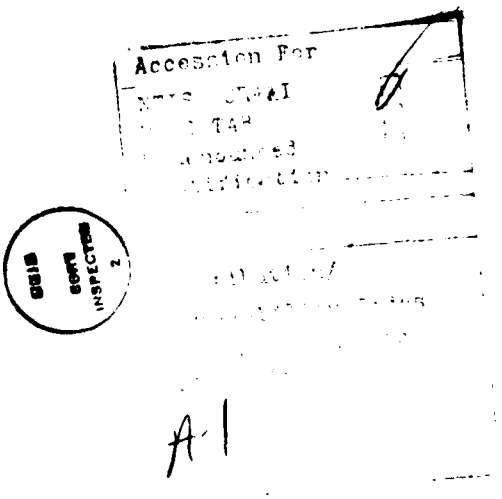
PREFACE

This technical report was prepared by Northeastern University, Boston, Massachusetts, under Contract No. F19628-80-C-0151. It describes work performed at the Dana Research Center, Electronics Research Laboratory from 1 May 1980 to 31 December 1982. The principal investigator was B. L. Cochrun.



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SECTION I

INTRODUCTION

This report covers the design and fabrication of three charge-coupled device test-bed modules, one module for each of the following devices:

(a) A 256 element Pt/Si Schottky diode linear imaging sensor.

(b) A 32 x 64 element Pt/Si Schottky diode IRCCD area imaging sensor.

(c) A 256 element serial analog delay line charge-coupled device.

All modules were to have the following common features:

(a) Operation from 115 Vac., 50-60 Hz input power

(b) Flexibility in terms of access to test points and variable bias voltages.

(c) Correlated-double-sampling (CDS) techniques to minimize noise and offsets where applicable.

(d) Double regulated power supplies where applicable.

(e) Packaging techniques to be compatible for use in TM500 type power modules.

SECTION II

LINEAR IMAGING 256 ELEMENT SENSOR TEST BED MODULE

A. Introduction

A simplified representation of the 256 element IRCCD chip is shown in Figure 2.0. CCD output shift registers A and B have common clock lines and identical input-output characteristics. The original impetus for the dual registers was to provide for differential output sensing for clock pickup cancellation. This testbed provides for clock pickup cancellation, as well as offsets, by means of correlated double sampling at the signal output.

Variable stare time for the IRCCD Schottky diode detectors is controlled by an external microprocessor. Two digital TTL level signals from the microprocessor, F_1 and F_2, are decoded by the system circuitry to give, on demand, four stare times $T_{ref}/2^n$ milliseconds, where n is an integer between 0 and 3. The system supplies start-convert (SC) and start packet (SP) signals to synchronize the video output with the signal processing program of the microprocessor.

The microprocessor requirements specify that the exact value of T_{ref} is not critical; however, the incremental changes are, i.e., either ½ or 2 for a decrease or increase respectively of stare time. A SP pulse is required for each T_{ref} interval. T_{ref} for this system was chosen as 100 milliseconds, thus requiring stare times of 12.5, 25, 50 and 100 milliseconds.

The entire electronic system, with the exception of the power supplies, is contained on a 9.5 x 4.5 inch PC board with a ground plane. Two systems were fabricated. The original design used a

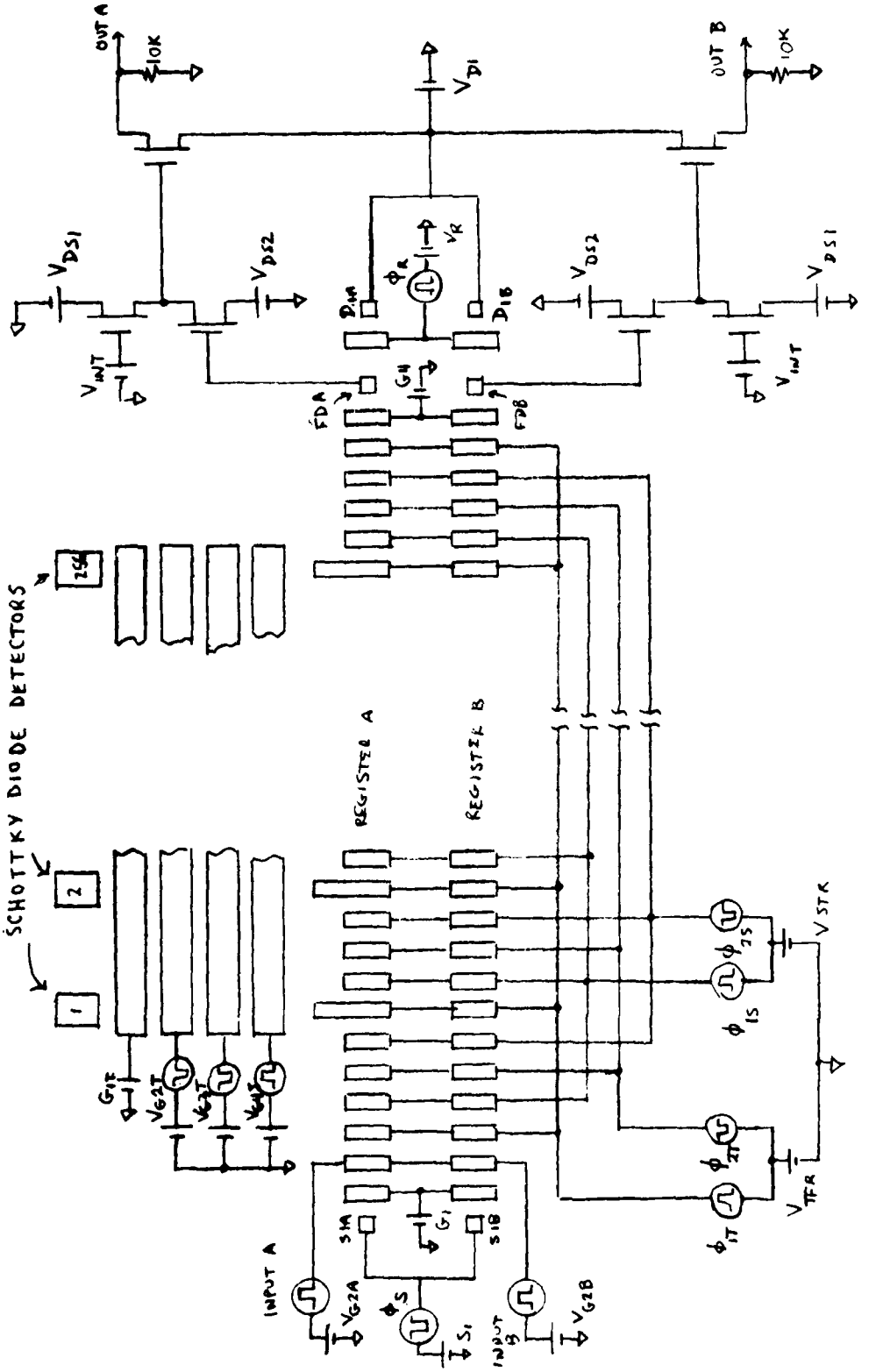


Figure 2.0 Representation of 256 element LIRCCD chip

2N74LS324 TTL VCO for the master clock (MCK). A second design incorporated a crystal oscillator as the MCK. The first design was intended for laboratory use with its benign environment. The second design was for operation in an all weather environment requiring a steel sealed container.

The physical layout of the two boards was dictated by convenient access to the bias adjustments. Consequently, the board layouts are physically different; however, the electronic operation of both is identical.

B. Clock Generation

The schematic representation of the LIRCCD chip in Figure 2.1 indicates the various clock signals and dc voltages required for operation. (A detailed description of the physical structure and operation of the chip may be found in Reference 1). Figure 2.1 illustrates the circuitry used to generate the TTL level signals $\overline{\Phi}_1$ and $\overline{\Phi}_2$ - the CCD gate clock voltages - $\overline{R}$ and $\overline{S}$ the reset and source clocks respectively. Figure 2.2 indicates the desired waveforms and the timing originating with the MCK.

In Figure 2.1 the frequency of the CK signal for counter 2N74161(1) is 166.65 KHz. This frequency was chosen on the basis of the minimum stare time of 12.5 milliseconds. The crystal MCK fundamental frequency is 333.3 MHz. Division by 2 to obtain the desired CK frequency is accomplished by means of the D type FF 2N7474(A). The 2N74LS324 VCO operates directly at 166.65 KHz. For timing purposes $\overline{CK}$, the direct output from either MCK is inverted to obtain CK the clock voltage for counter 2N74161(1). This counter's outputs Q_B and Q_C in conjunction

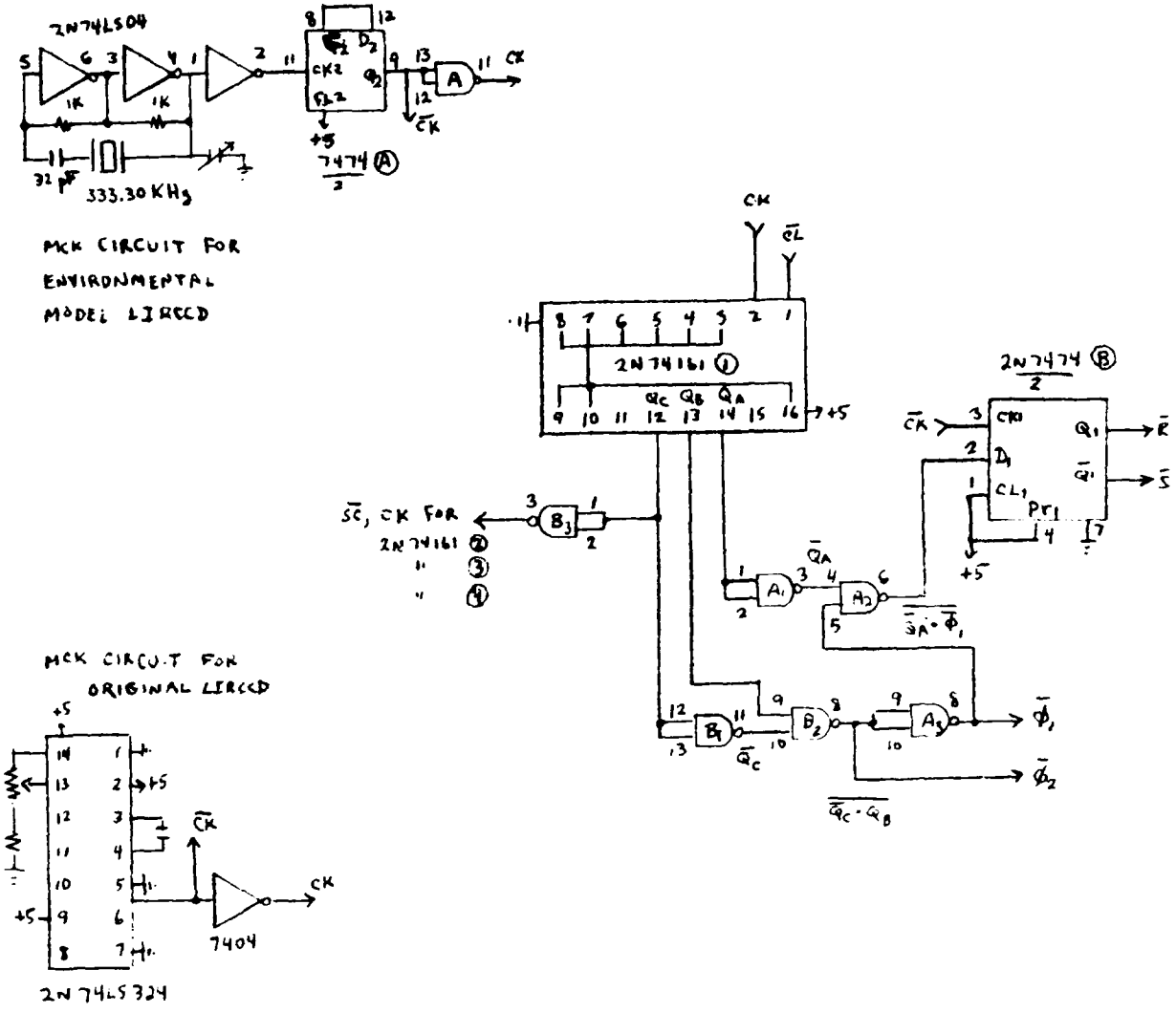


Figure 2.1 Circuitry for clock voltages $\bar{\phi}_1$, $\bar{\phi}_2$, $\bar{R}$ and $\bar{S}$ waveforms

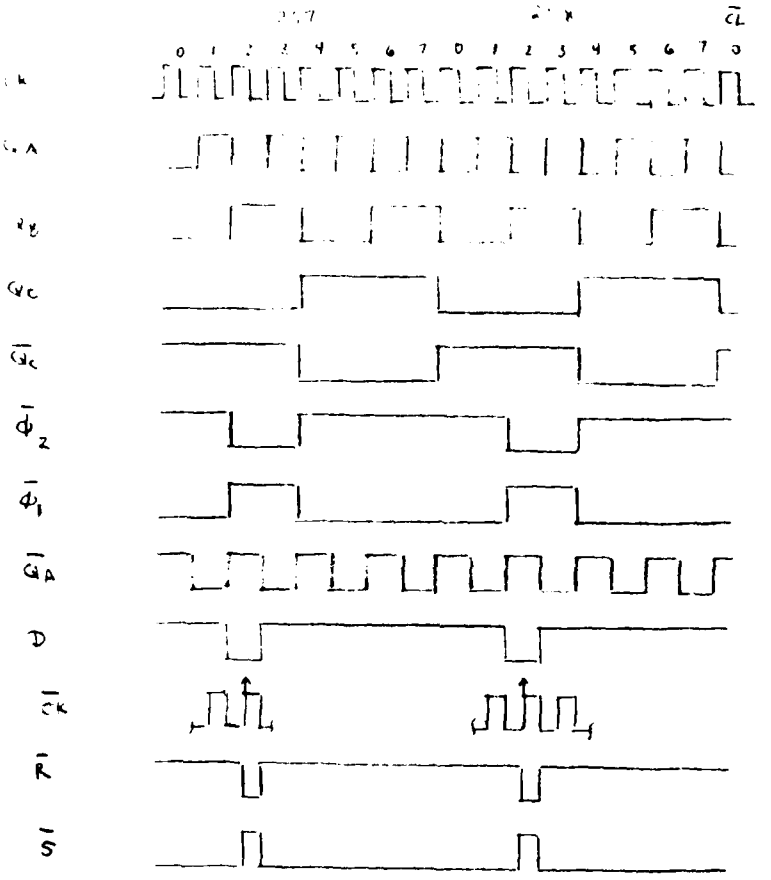


Figure 2.2 Timing diagram for $\overline{\emptyset}_1$, $\overline{\emptyset}_2$, $\overline{R}$ and $\overline{S}$ waveforms

with NAND gates B_1, B_2 and A_3 generate $\overline{\phi}_1$ and $\overline{\phi}_2$ at a clock rate of 20.83 KHz with pulse widths of 24 μseconds. As indicated in Figure 2.2, D_1 of the D type FF goes low with the coincidence of Q_A and $\overline{\phi}_1$. On the next rising edge of $\overline{CK}$, $\overline{R}$ is generated at the Q output and $\overline{S}$ at the $\overline{Q}$ output. NAND gate B_3 is used as an inverter to obtain the clock input for the synchronous counters (2) and (3) which are shown in Figures 2.3 and 2.5. A common clear signal, $\overline{CL}$ is used for counters 1 through 3 the circuitry for which is shown in Figures 2.3 and 2.5.

Figure 2.3 contains the remainder of the LIRCCD digital circuitry used to generate the transfer gate clock voltages $\overline{V_{G4T}}$ and $\overline{V_{G2T}}$ and control the stare time. Figure 2.4 illustrates the required waveforms and related timing. Figure 2.5 is a simplified circuit diagram, corresponding to Figure 2.3 which will be used to discuss the basic timing required to obtain the transfer gate voltages and the variable stare times.

Stare time is the time between successive parallel transfer gate pulses, $\overline{G_{4T}}$ and $\overline{G_{2T}}$, when the Schottky diode detectors are isolated from the serial CCD shift registers. At the end of the readout time a clear pulse $\overline{CL}$, is generated to reset the counters 1-3. This $\overline{CL}$ pulse width is made up of a BLANK pulse, a G_{4T} dummy pulse, both of which are adjustable and 1/2 cycle of $\overline{CK}$. $\overline{CL}$ width and the time for 258 cycles of CK are set for 12.5 milliseconds. The extra two counts, since there are 256 diodes, are necessitated by the physical structure of the chip. There is a two bit delay encountered when the output of Register A is direct coupled into the serial input of Register B. (See Figure 2.0 and Reference (1).)

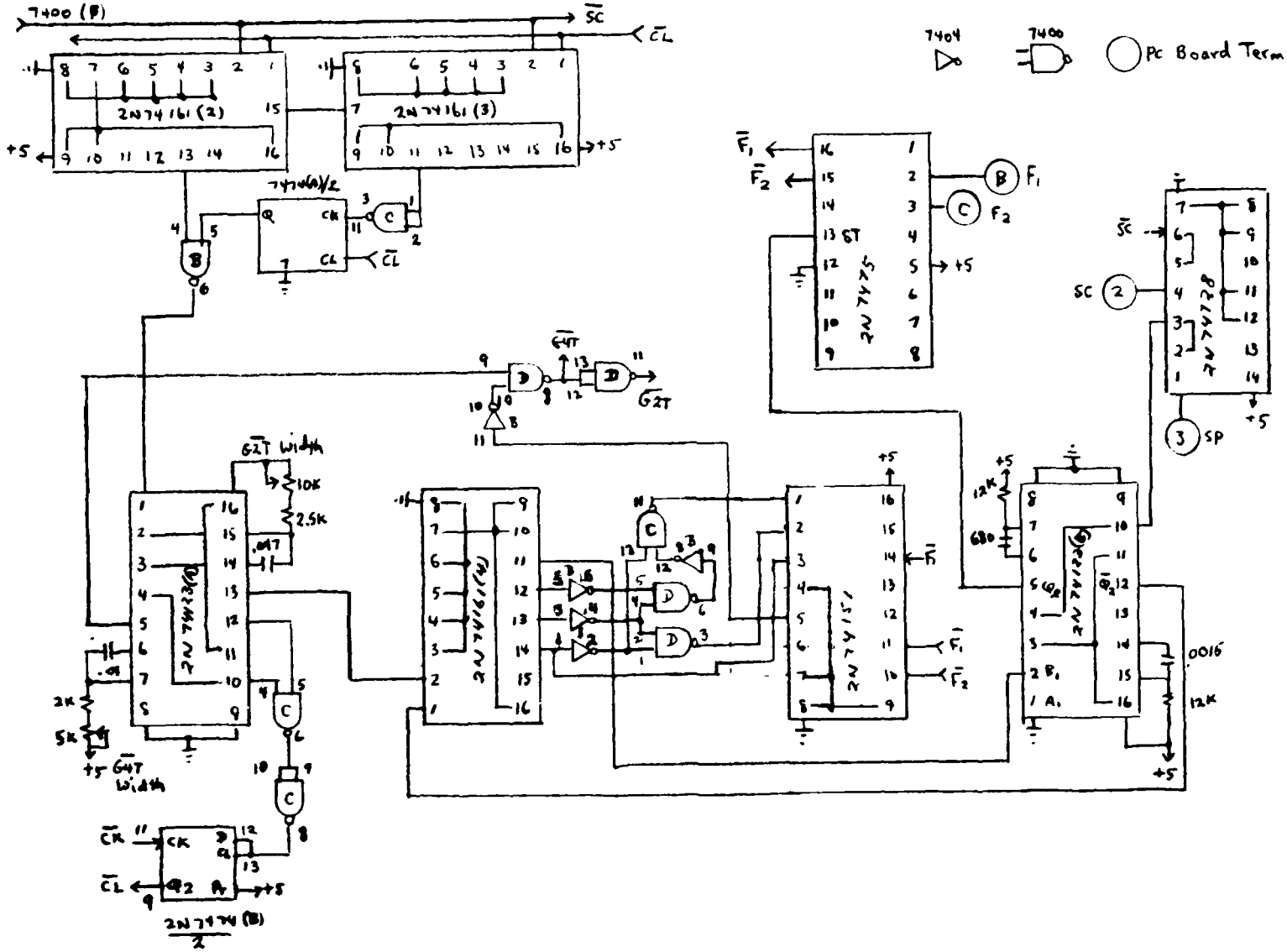


Figure 2.3 Circuitry for $\overline{G_{4T}}$, $\overline{G_{2T}}$ and variable stare time control

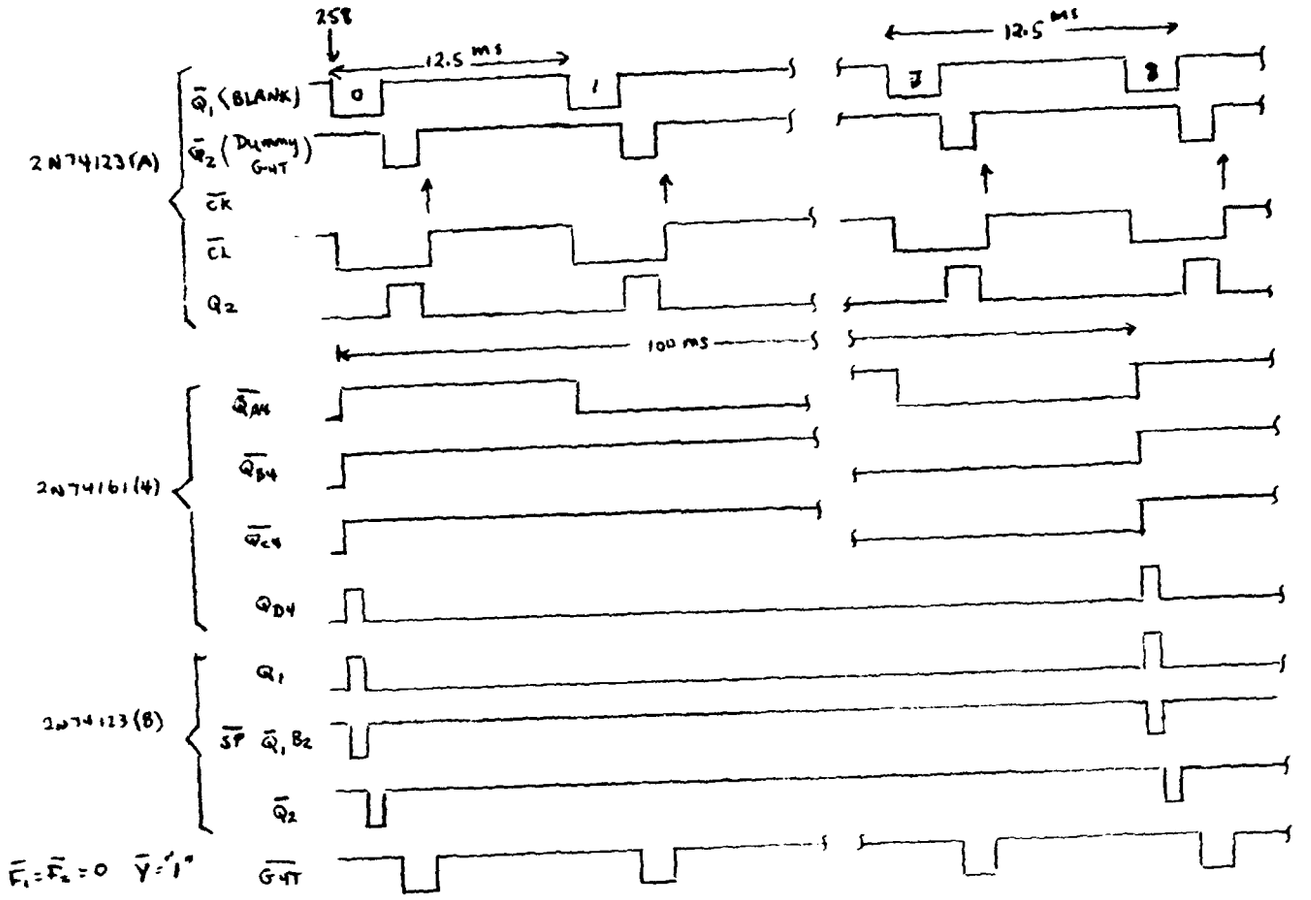
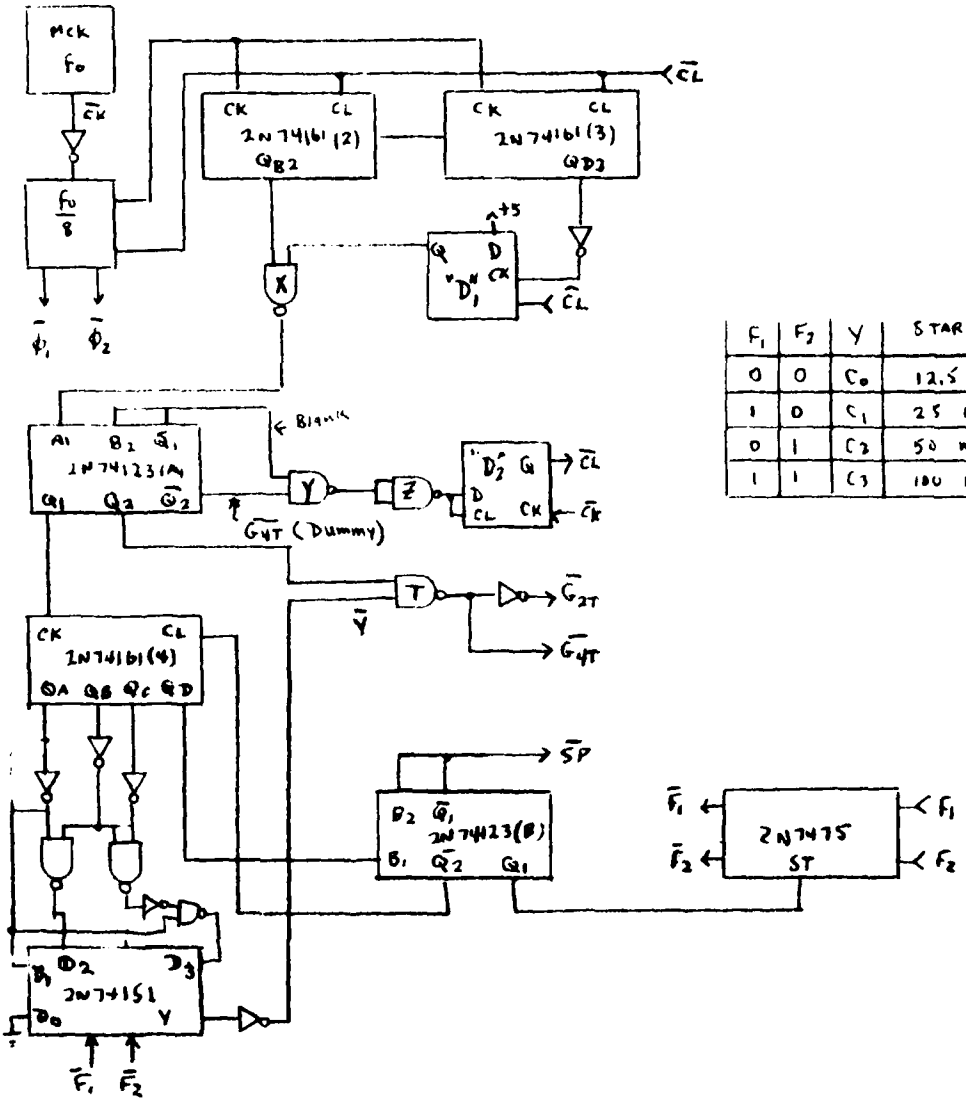


Figure 2.4 Timing diagrams for $\overline{G_{4T}}$, $\overline{G_{2T}}$ and SP waveforms



F_1	F_2	Y	STARE TIME
0	0	C_0	12.5 ms
1	0	C_1	25 MS
0	1	C_2	50 MS
1	1	C_3	100 MS

Figure 2.5 Simplified circuitry for $\overline{G_{4T}}$, $\overline{G_{2T}}$ and stare time control

In Figure 2.5 $\overline{CL}$ is initiated by the negative BLANK pulse obtained at the $\overline{Q}_1$ output of FF 2N74123 (A) when the A_1 input is triggered by the negative edge of the output from NAND gate (X). This negative edge results after the 258th. cycle of CK. The falling edge of Q_{D3} occurring at the end of the 256th. cycle, is inverted and clocks "D_1" output 0 high. Two cycles later Q_{B2} goes high driving the output of NAND gate (X) low.

$\overline{Q}_1$ of FF 2N74123 (A) is tied to B_2 so that $\overline{Q}_2$ is triggered by the termination of the BLANK pulse. The negative pulse at $\overline{Q}_2$, is adjustable and refered to as G_{4T} dummy since it is not the actual $\overline{G_{4T}}$ pulse used for transfer. Termination of the negative G_{4T} dummy pulse sets the D input of "D_2" high and on the next positive edge of $\overline{CK}$ the $\overline{CL}$ pulse is terminated and the next readout interval of 258 cycles of CK is initiated. Thus a time interval of 12.5 milliseconds is made up of the BLANK pulse width, the $\overline{Q}_2$ pulse width, 1/2 cycle of CK and 258 cycles of CK.

The actual $\overline{G_{4T}}$ pulse is obtained at the output of NAND gate (T). $\overline{G_{2T}}$, being the inverse of $\overline{G_{4T}}$, is obtained at the output of the following inverter. One input to NAND gate (T) is Q_2 of the FF 2N74123A. This positive pulse with the width of the G_{4T} dummy pulse will appear inverted at the output whenever the other input is high, i.e., when the inverted output $\overline{Y}$, of decoder 2N74151 is high.

$\overline{Y}$ output timing is a function of $\overline{F}_1$ and $\overline{F}_2$, the control inputs to the 2N74151 decoder, and the logic circuitry between the outputs and inputs of counter 2N74161(4) and the decoder respectively. CK for counter (4) is Q_1 of FF 74123(A). Thus counting is initiated on the leading edge of $\overline{CL}$. The rising edge of Q_{D4}, on the 8th. count of

$\overline{CL}$, is the B_1 input to FF 2N74123 (B). After 100 milliseconds a negative $\overline{SP}$ pulse is obtained at $\overline{Q}_1$ of FF (B). With $\overline{Q}_1$ tied to B_2 a negative clear pulse for counter (4) is obtained at $\overline{Q}_2$ upon termination of the $\overline{SP}$ pulse. Q_A, Q_B and Q_C of counter (4) are all low while the counter is being cleared and so only Q_D is affected.

The table shown in Figure 2.5 indicates the necessary control signals and Y output for the decoder for various stare times. When $\overline{F}_1 = 1$ and $\overline{F}_2 = 0$ the stare time should be 25 milliseconds. For these inputs to the decoder $\overline{Q}_A$ of counter (4) is one input to NAND gate (T). Every other transfer pulse is inhibited thereby yielding a 25 millisecond stare time. For a 50 millisecond stare time only three $\overline{G_{4T}}$ pulses are required for each 100 milliseconds. With $\overline{F}_1 = 0$ and $\overline{F}_2 = 1$, $Y = D_2 = \overline{\overline{Q}_A \cdot \overline{Q}_B}$ and $\overline{Y} = \overline{Q_A + Q_B}$ which results in the necessary positive input to NAND gate (T) at the beginning of the $\overline{SP}$ pulse and 50 milliseconds later. For a 100 millisecond stare time $\overline{Y} = \overline{\overline{Q}_A(Q_B + Q_C)}$ and only a single $\overline{G_{4T}}$ pulse is obtained for each $\overline{SP}$ pulse.

The $\overline{SP}$ is inverted by a buffer inverting driver amplifier 2N74128 to obtain the SP pulse for the μprocessor. (See Figure 2.3). Q_1 of FF 2N74123 (B), a positive pulse with the same width as $\overline{SP}$, is used to strobe a 2N7475 latch and prevent any change in stare time during the readout interval. The start convert,SC, pulses for the μprocessor are also obtained at the output of the 2N74128 driver as indicated in Figure 2.3.

Figure 2.6 contains the output amplifier stages which use DS0026's to obtain the clock voltages ϕ_1, ϕ_2, G_{2T}, G_{3T}, G_{4T}, R and S. (Also see Figure 2.0). The final data input incorporates a correlated-double-sampling technique which is illustrated in Figure 2.7. A detailed des-

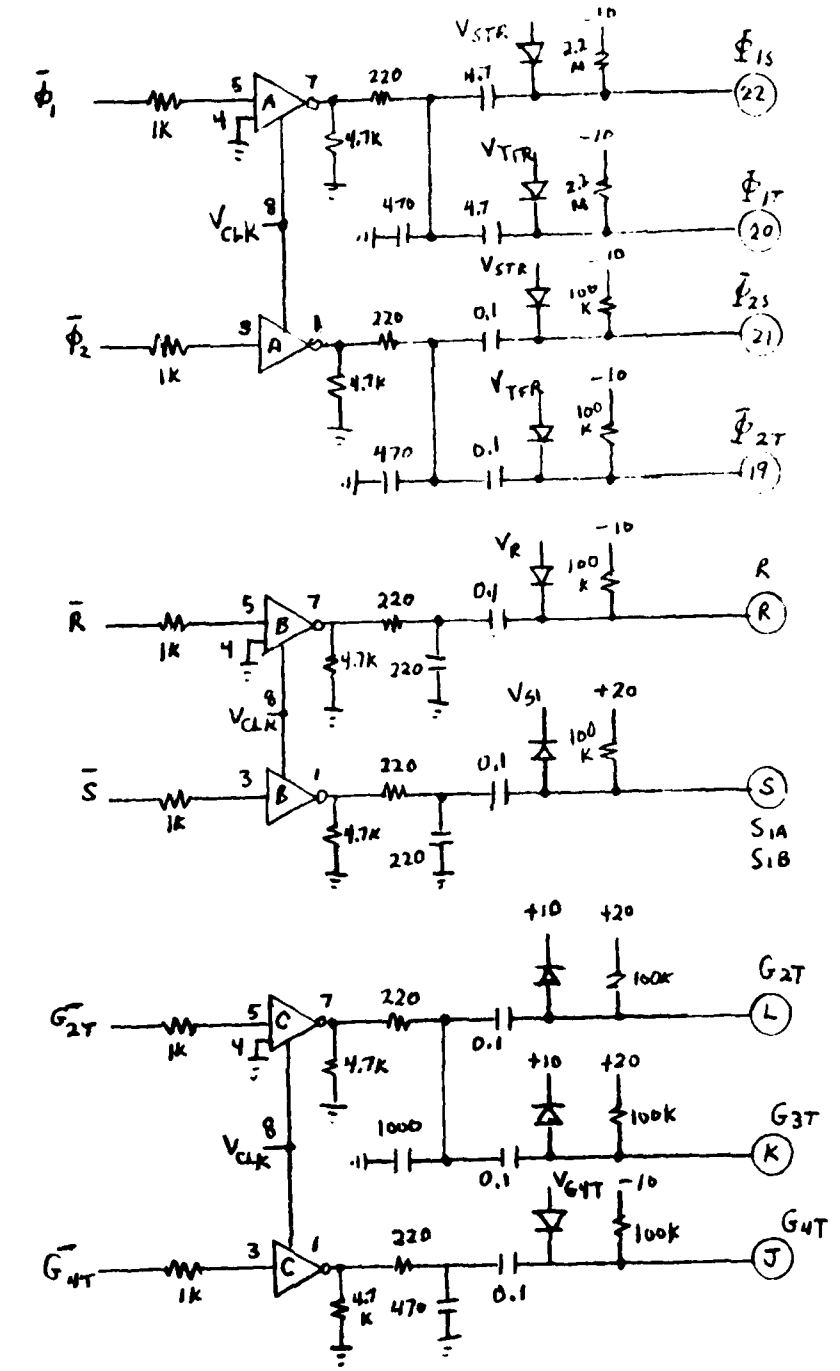


Figure 2.6 Output driver amplifier circuits for LIRCCD

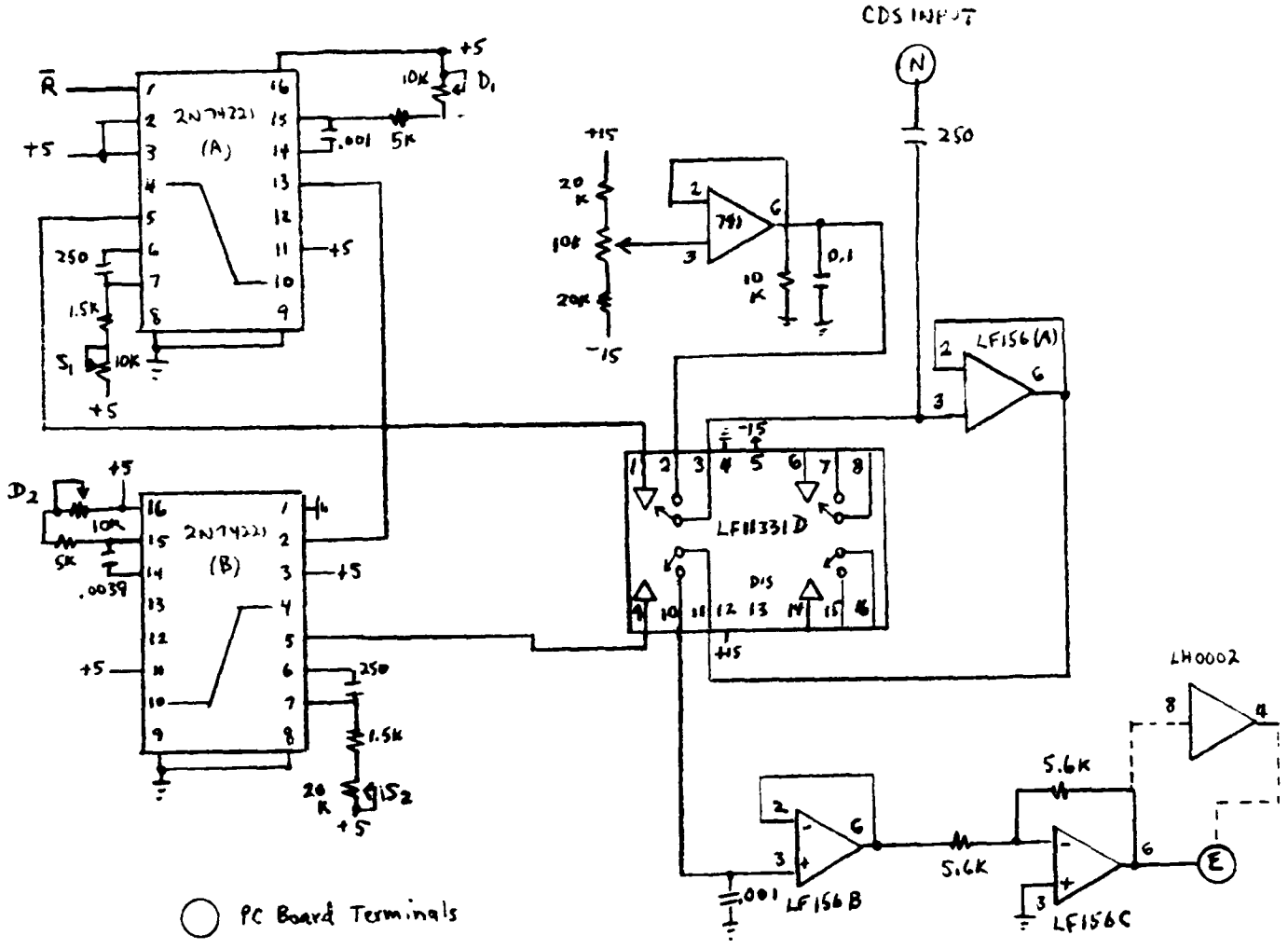


Figure 2.7 Correlated-double-sampling circuit

cription of the use of this approach to minimize offsets and noise can be found in Reference 2. Details of the variable bias supplies are shown in Figure 2.8. Connections to the R644 PC board plug are indicated in Figure 2.9.

Double regulation of the 25 volt, $\pm$ 15 and $\pm$ 10 volt bias supplies is illustrated in the power supply diagram of Figure 2.10. These voltages are obtained from an isolated shielded rack mountable housing.

C. Operating Waveforms

Waveforms for the operating system are shown in Figures 2.11 through 2.18. Figures 2.11 to 2.13 are the TTL clock voltages derived by the circuitry of Figures 2.1 and 2.3. Figures 2.14 to 2.17 are the output waveforms for the DS0026 driver stages shown in Figure 2.6. Figure 2.18 shows the CDS control waveforms D_1, S_1 (max), D_2 and S_2 (max).

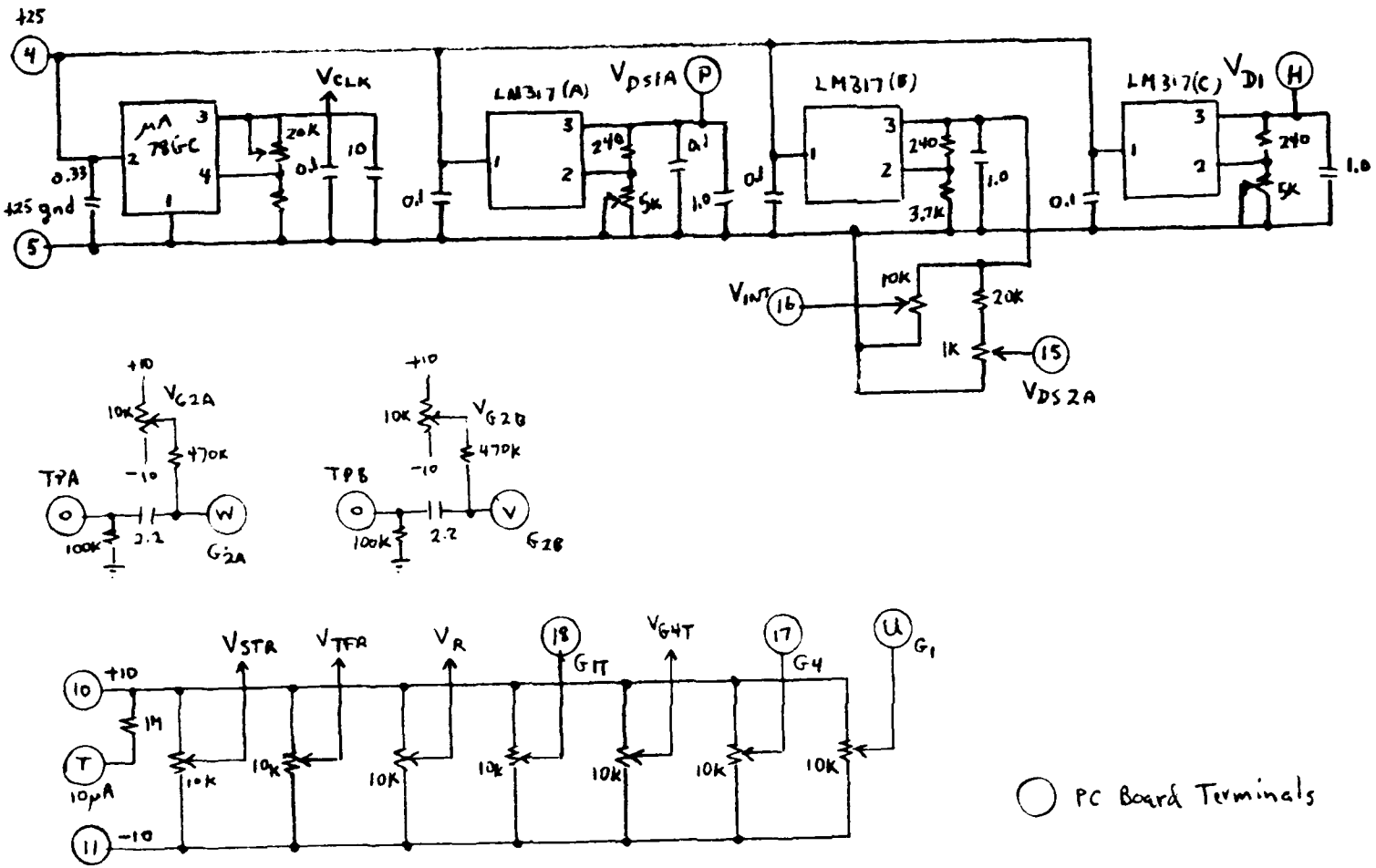


Figure 2.8 LIRCCD bias supplies

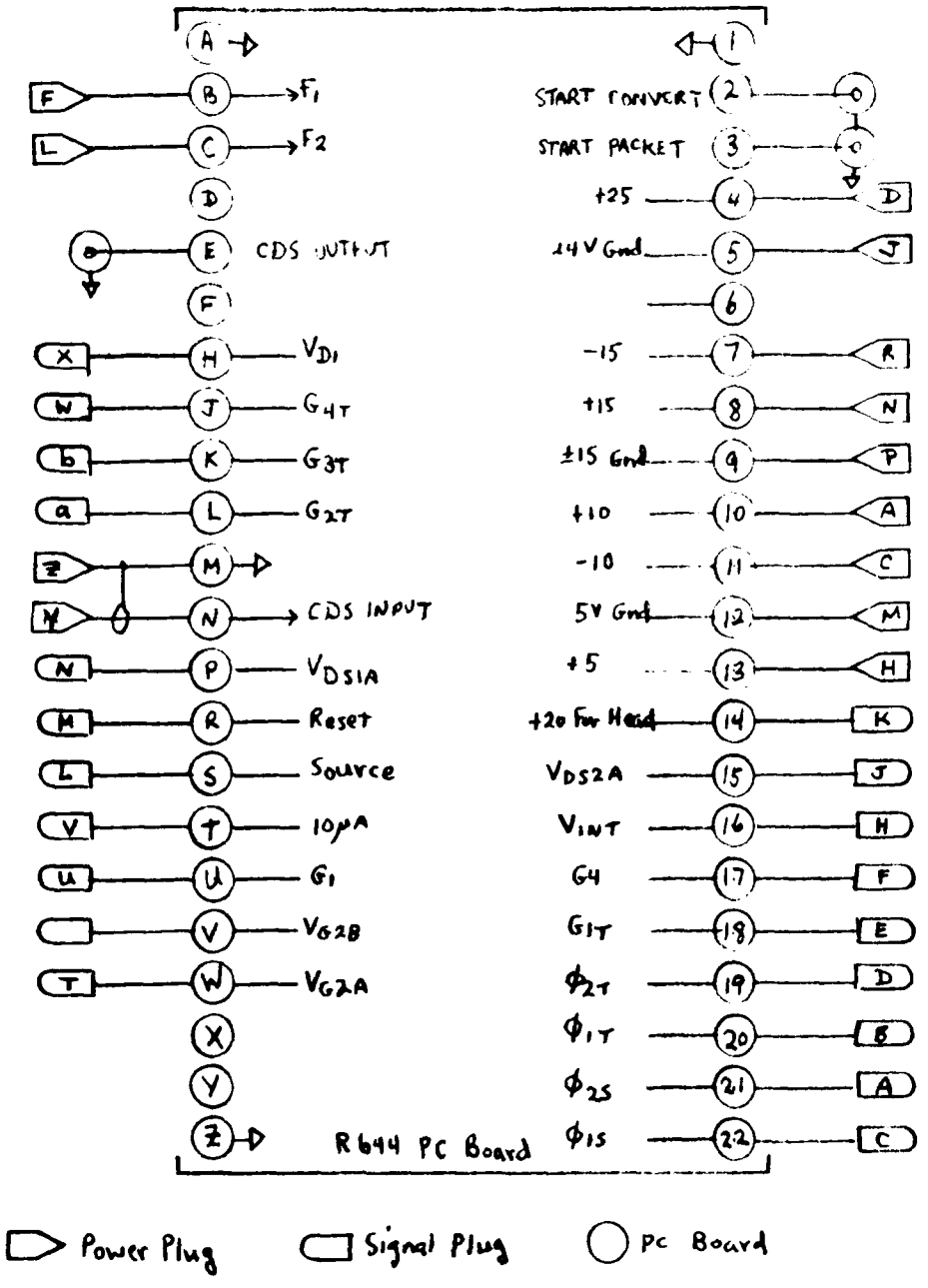


Figure 2.9 PC board wiring

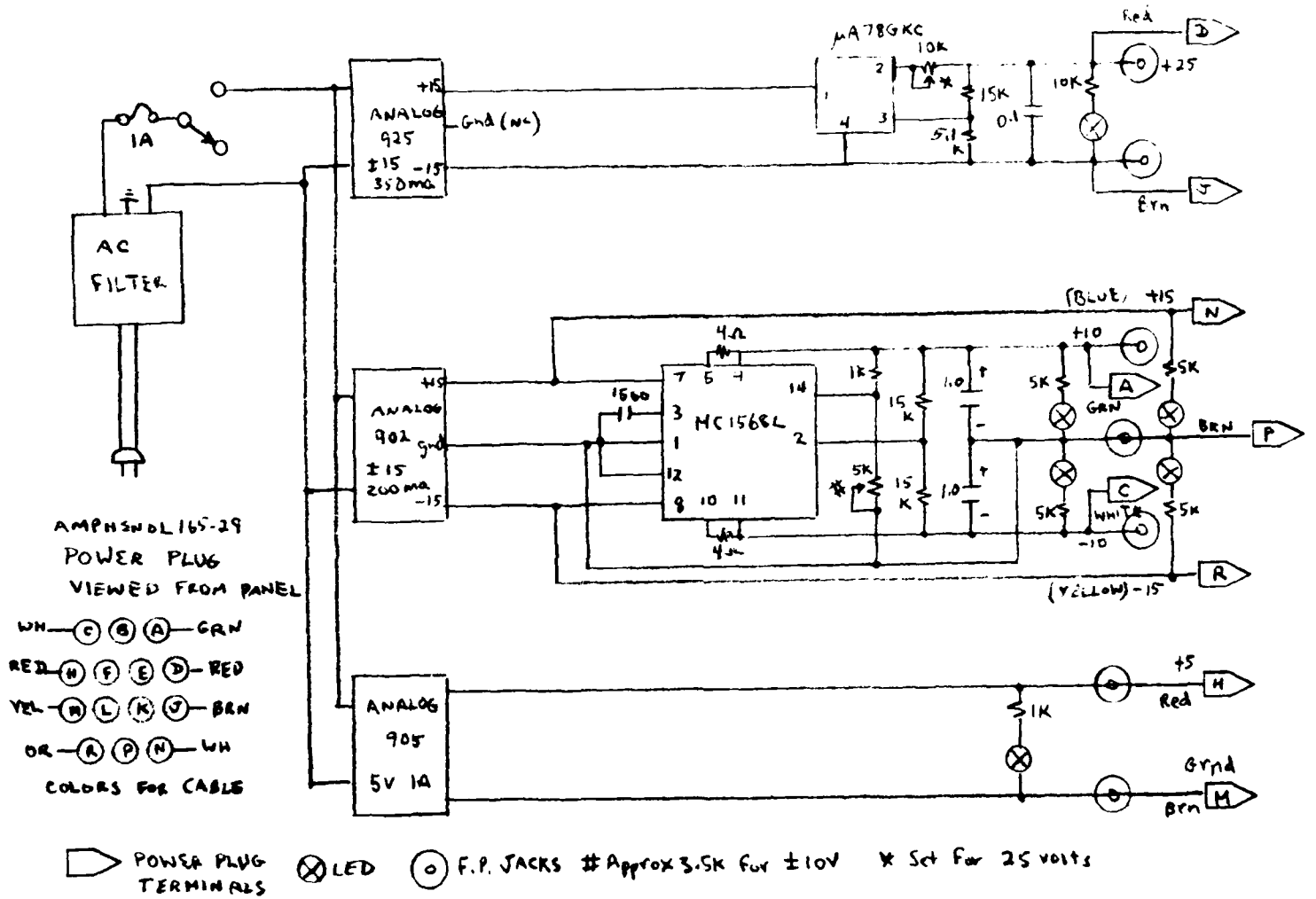


Figure 2.10 Power supply for LIRCCD

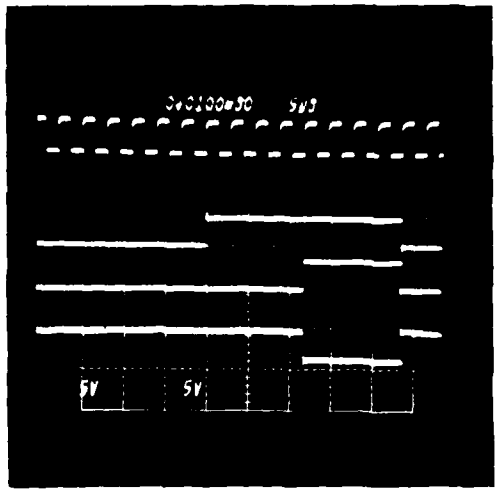


Figure 2.11 Operating waveforms, top to bottom, CK, $\overline{S}_C$, $\overline{\emptyset}_1$, $\overline{\emptyset}_2$.

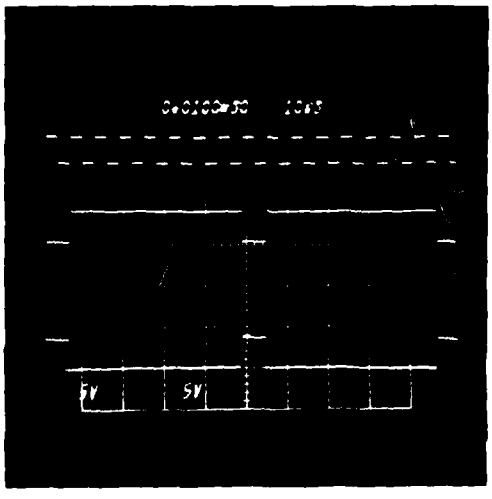


Figure 2.12 Operating waveforms, top to bottom, CK, $\overline{R}$, $\overline{S}$.

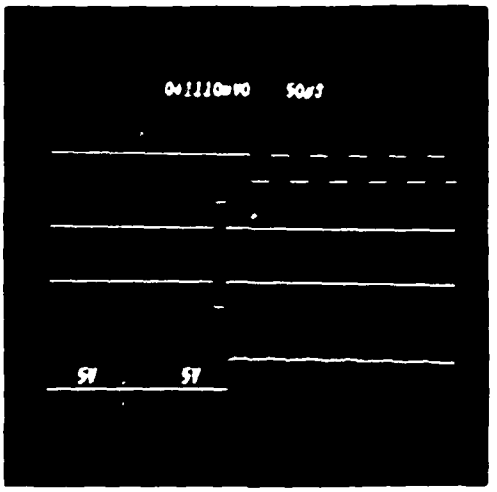


Figure 2.13 Operating waveforms, top to bottom, $\overline{S_C}$, $\overline{G_{2T}}$, $\overline{G_{4T}}$, $\overline{CL}$.

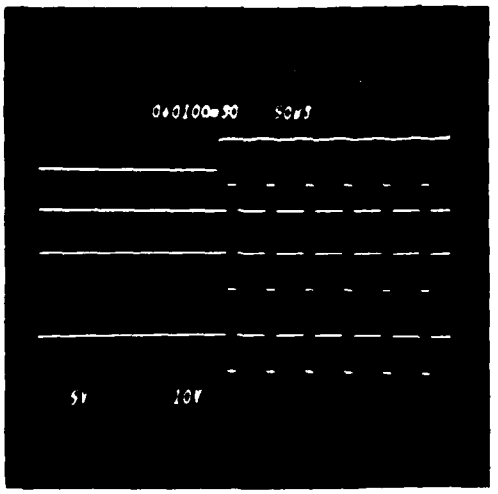


Figure 2.14 Operating waveforms, top to bottom, $\overline{CL}$, $\overline{\emptyset_1}$, $\emptyset_{1S}$, $\emptyset_{1T}$.

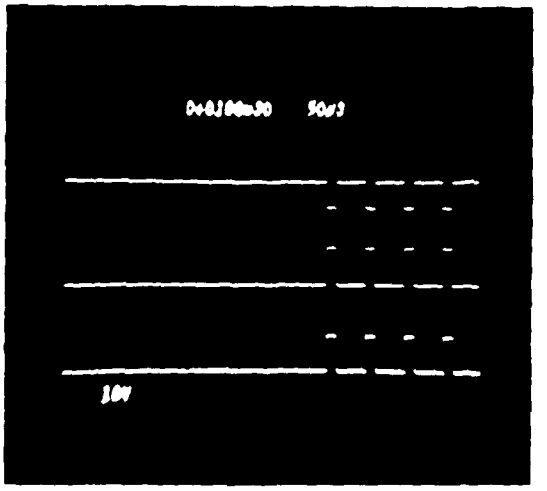


Figure 2.15 Operating waveforms, top to bottom, $\emptyset_2$, $\emptyset_{2S}$, $\emptyset_{2T}$.

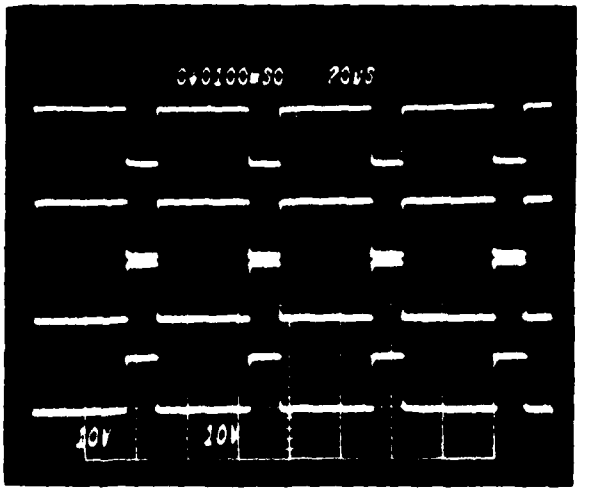


Figure 2.16 Operating waveforms, top to bottom, $\emptyset_{1S}$, $\emptyset_{1T}$, $\emptyset_{2S}$, $\emptyset_{2T}$.

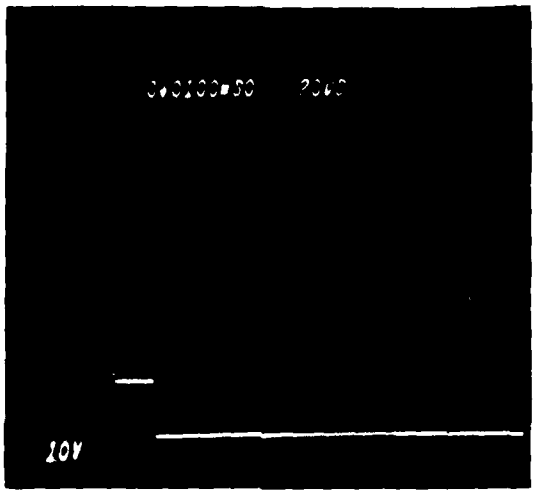


Figure 2.17 Operating waveforms, top to bottom, G_{2T}, G_{3T}, G_{4T}.

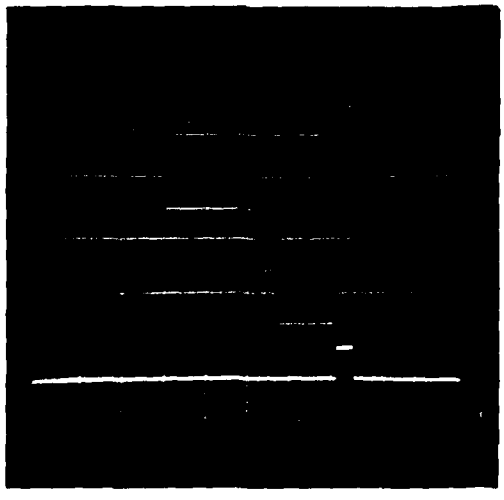


Figure 2.18 CDS control waveforms, top to bottom, D_1, S_1(max), D_2, S_2(max).

SECTION III

AREA IMAGING 32 X 64 ELEMENT 2DIRCCD TEST BED MODULE

A. Introduction

The area imaging 2DIRCCD chip structure consists of a 32 x 64 matrix of Schottky diode detectors formatted as 64 columns of 32 diodes/column. A simplified partial representation of the structure is shown in Figure 3.0. A column CCD shift register transports the charge from the diodes to a multiplexor CCD readout shift register. During the stare time the diodes are isolated from the column shift register by the diode transfer gates TA and TB. Clock voltages $\emptyset_{1SR}$ and $\emptyset_{2SR}$ transfers the charge in the column register to the multiplexer transfer gate TM which in turn clocks the charge from the column registers into the multiplexer shift register for readout by the clock voltages $\emptyset_{1M}$ and $\emptyset_{2M}$.

Other clock voltages required, but not indicated in Figure 3.0 are the fat zero inputs for each register, i.e., $\emptyset_{FZM}$ and $\emptyset_{FZSR}$ for improvement of transfer efficiency and the reset voltage $\emptyset_{RS}$ for the multiplex register.

B. Generation of Clock Waveforms

Two sets of clock waveforms are required. One, a group of slow clock voltages for the column shift registers and a second group of fast clock voltages for the multiplex output register. The fundamental basis for the clock frequencies is set by the specified stare time and the need for TV compatibility with respect to timing of the video output.

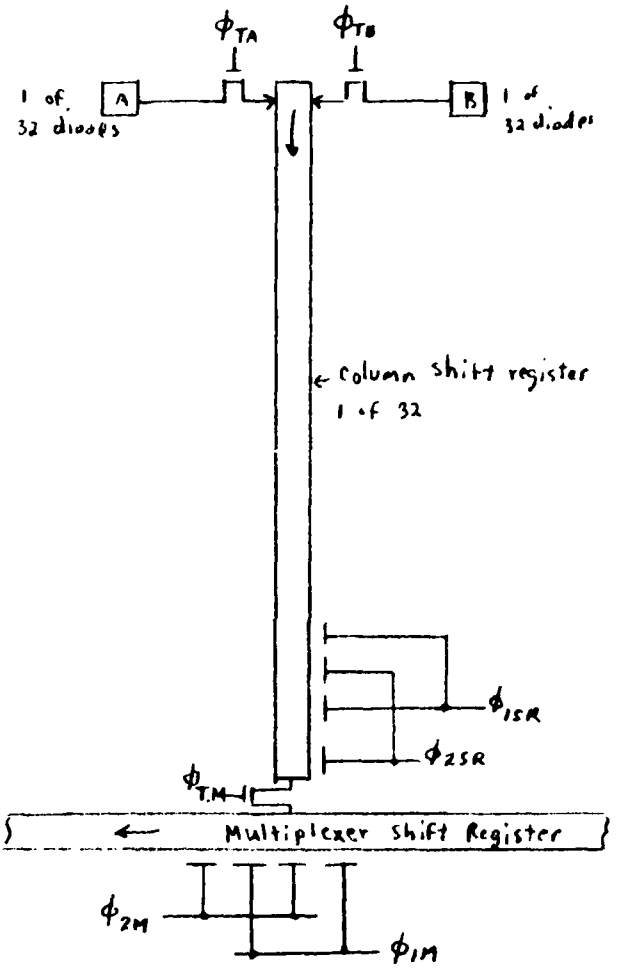


Figure 3.0 Simplified partial representation of 32 x 64 chip

Stare time is the interval between succeeding $\emptyset_{TA}$, or $\emptyset_{TB}$, pulses. All "A" diodes are transferred to the column shift resistor simultaneously by $\emptyset_{TA}$ and are read into the multiplexer by 32 $\emptyset_{TM}$ pulses. After each $\emptyset_{TM}$ pulse the 32 inputs to the multiplexer are read out by $\emptyset_{1M}$ and $\emptyset_{2M}$. The system specifications were for a frame rate of 1/60 or 16.666 milliseconds or 1/30 or 33 milliseconds.

On the basis of 16,666 milliseconds the desired frequency for the fast clocks is 245.8KHz and that for the slow clocks is 3.8KHz. The various clock waveforms and related timing is shown in Figure 3.1.

Figure 3.2 shows the circuitry for generating the fast clocks at 245.8KHz. The master clock is a crystal oscillator with a fundamental frequency of 3.9322MHz. Logic circuitry made up of 1/2 of the "D" type FF 2N7474 (A) and three 2N7400 NOR gates provides the inputs to counter 2N74193(A), either 3.9322MHz or 1.966MHz. The outputs from the counter are decoded by the 2N74154(A) 4-line to 16-line decoder and the timing and clock widths are controlled by the 16 outputs of the decoder.

Generation of $\bar{\emptyset}_{1M}$ is illustrated in the timing diagram of Figure 3.2a and the circuitry in Figure 3.2. The $\bar{\emptyset}_{1M}$ pulse is initiated by the first negative output from the decoder which is inverted to give a positive edge for CK pin 3 of 1/2 of 2N7474(B). The preset for 2N7474(B), pin 1 is held high until the 6th. negative pulse from the decoder terminates $\bar{\emptyset}_{1M}$ at Q, pin 5 of 2N7474(B). Since each output pulse from the decoder is .25μsec. the $\bar{\emptyset}_{1M}$ width is set at ≈1.6μsec. Since $T_{245.8} = 4\mu sec.$ this gives a duty cycle of ≈ 40% for $\bar{\emptyset}_{1M}$. $\bar{\emptyset}_{2M}$ is generated in the same manner using 1/2 7474(B) and the appropriate outputs from the decoder. Control of the rise time is provided by means of the two inverters 7400(B) which in turn are followed by the multiplex register gate driver dual amplifiers DS0026(A).

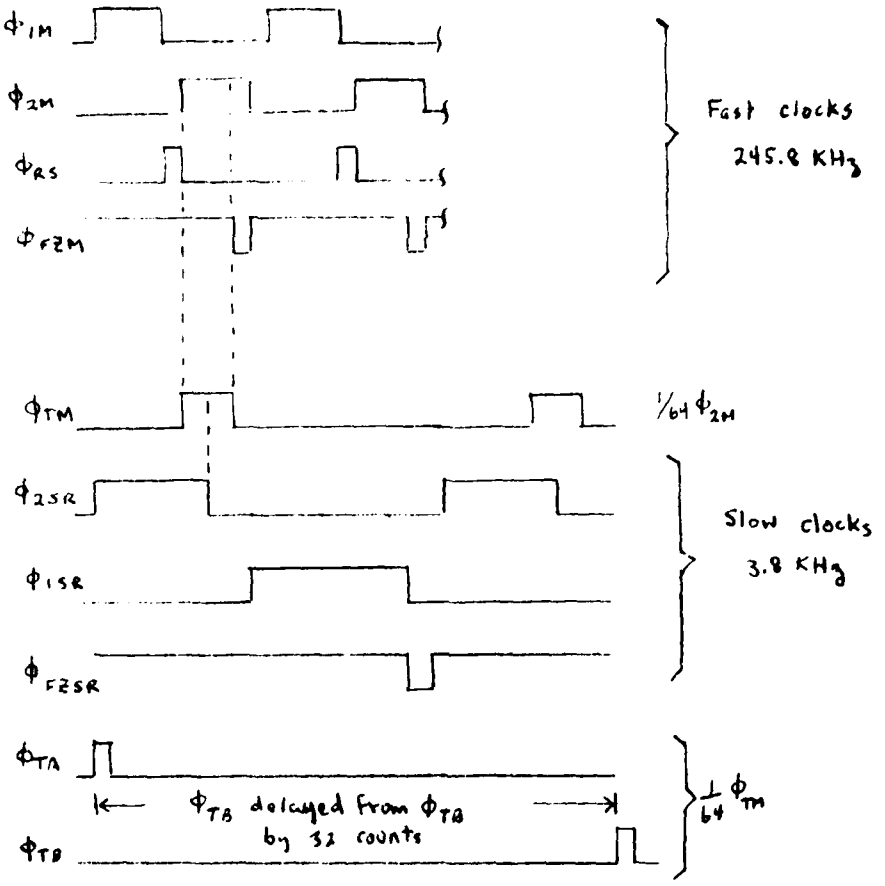


Figure 3.1 Clock and timing waveforms for 32 x 64 chip

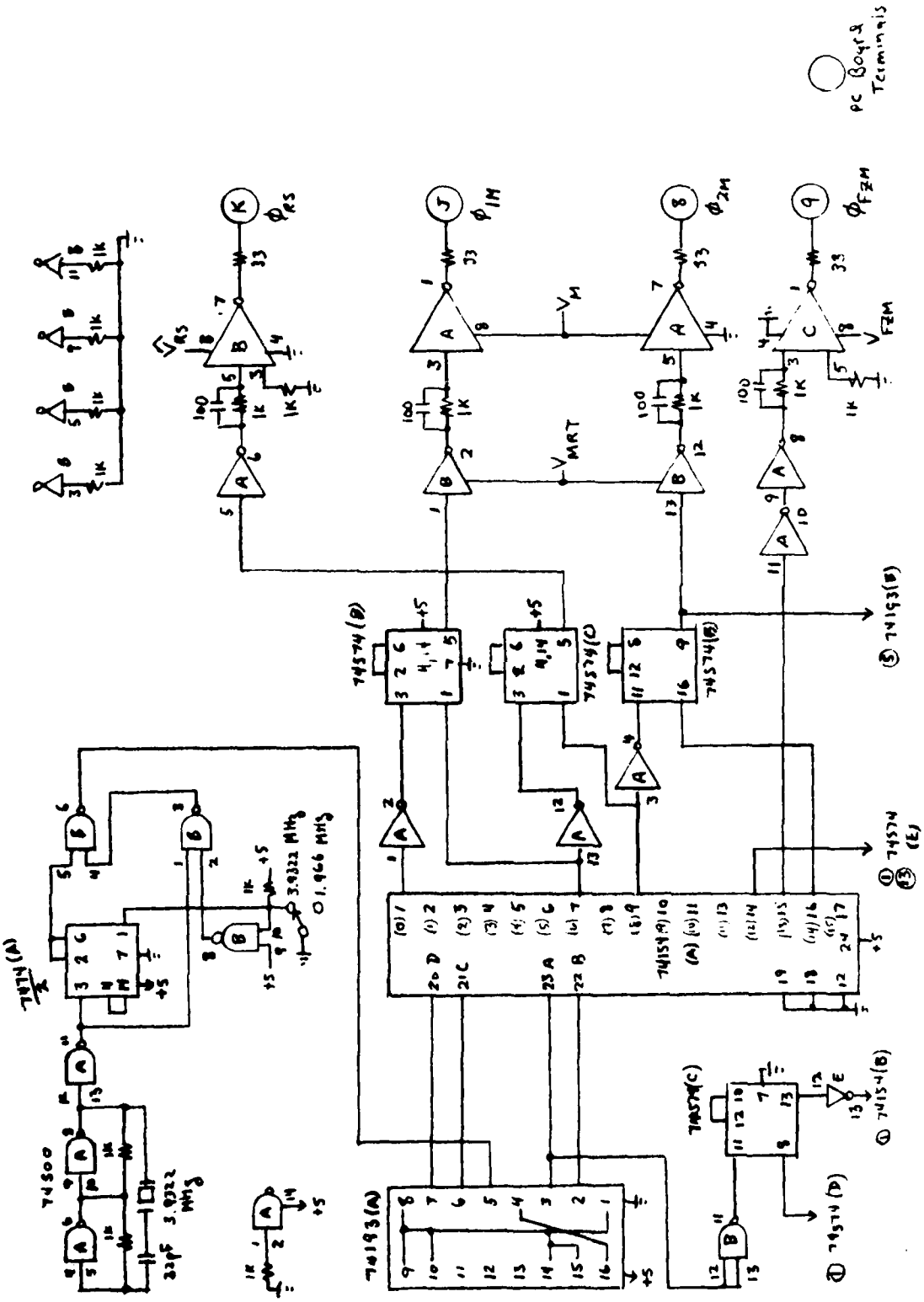


Figure 3.2 Clock circuitry for fast clocks

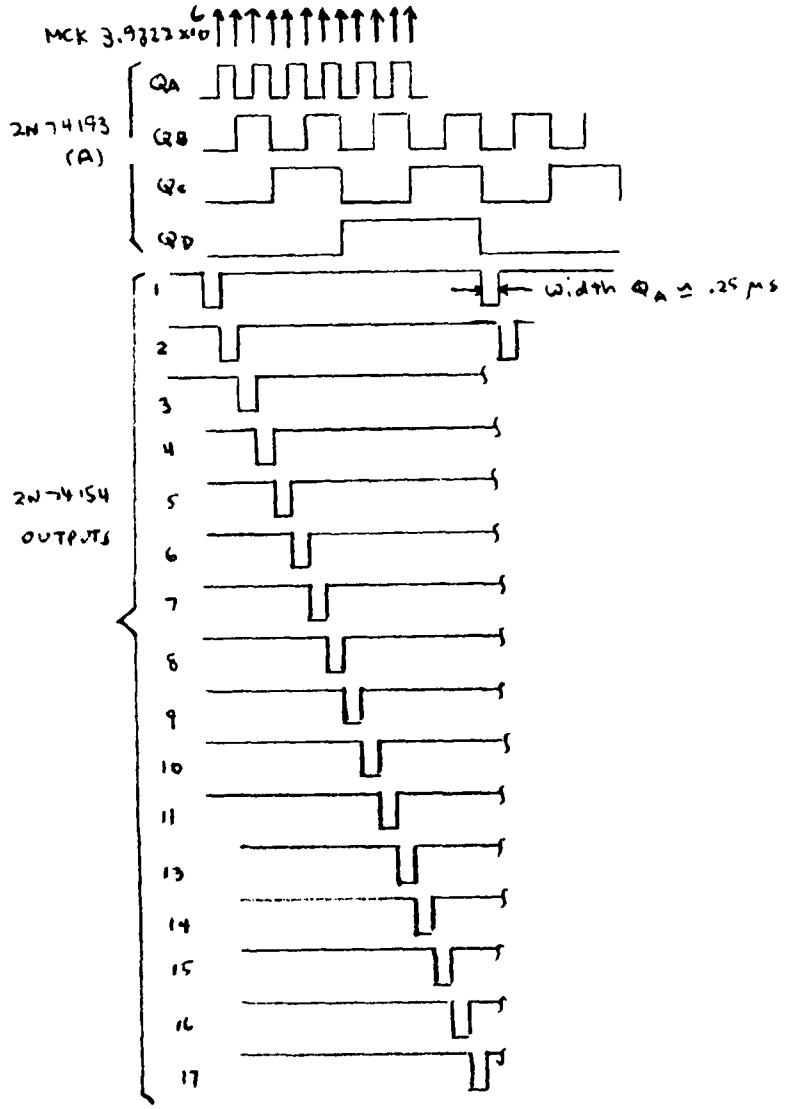


Figure 3.2a Timing diagram for 2N74154 decoder

Figure 3.3 shows the circuitry for generating the slow clocks at 3.8KHz. $\overline{\emptyset}_{TM}$ is 1/64 of $\overline{\emptyset}_{2M}$ and synchronizes $\overline{\emptyset}_{1SR}$ and $\overline{\emptyset}_{2SR}$. Counters 74193(B) and (C) provide the control inputs to decoder 2N74154(B). Timing and pulse widths for $\overline{\emptyset}_{1SR}$, $\overline{\emptyset}_{2SR}$ and $\overline{\emptyset}_{FZSR}$ are obtained by appropriate selection of the outputs from the decoder (B) in the same manner as discussed above for the fast clocks.

$\overline{\emptyset}_{TA}$ and $\overline{\emptyset}_{TB}$ are synchronized by $\overline{\emptyset}_{2SR}$ at a rate of $\overline{\emptyset}_{TM}/64$. Counters 74193 (D) and (E) provide their rates and allow for a 32 count delay between $\overline{\emptyset}_{TA}$ and $\overline{\emptyset}_{TB}$. A dual one-shot FF, 2N74221, provides for control of the gate widths of $\overline{\emptyset}_{TA}$ and $\overline{\emptyset}_{TB}$.

Control of rise time for $\overline{\emptyset}_{1SR}$ and $\overline{\emptyset}_{2SR}$ is provided by the two inverters 7404(D). Dual driver amplifiers provide the necessary clock amplitudes for the column register. Individual DS0026 drivers are used for the remaining clock outputs, $\emptyset_{FZSR}$, $\emptyset_{TM}$, $\emptyset_{TA}$ and $\emptyset_{TB}$.

Bias voltage circuitry is shown in Figure 3.4 Primary power is +24 and -12 volts for the output driver amplifiers and +5 volts for the TTL logic circuits. Three terminal regulators are used to control clock amplitudes. Emitter follower regulators are used to bias the output gates or the multiplex register with potentiometer control for the input gates of both registers.

C. Operating Waveforms

Figures 3.5 through 3.8 indicate the clock voltages and timing for the actual operating system. Figures 3.5 and 3.6 show the fast clock outputs and include $\emptyset_{TM}$. Figures 3.7 and 3.8 show the slow clock outputs and their timing with respect to $\emptyset_{TM}$. These waveforms correspond to a stare time of 16.66 milliseconds or with the MCK set at 3.9322MHz. Operation at 33 milliseconds gives the same waveforms at twice the time scale.

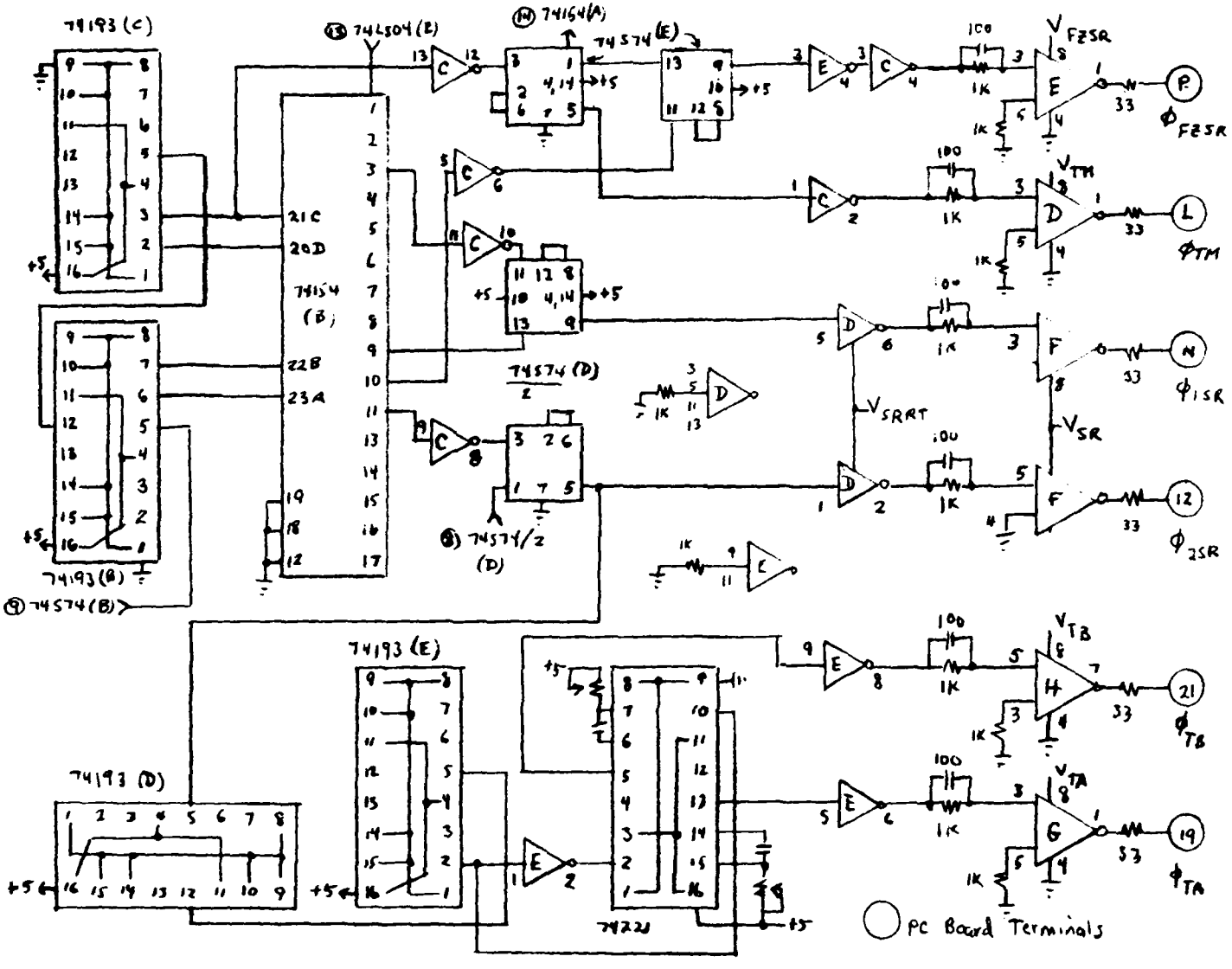


Figure 3.3 Clock circuitry for slow clocks

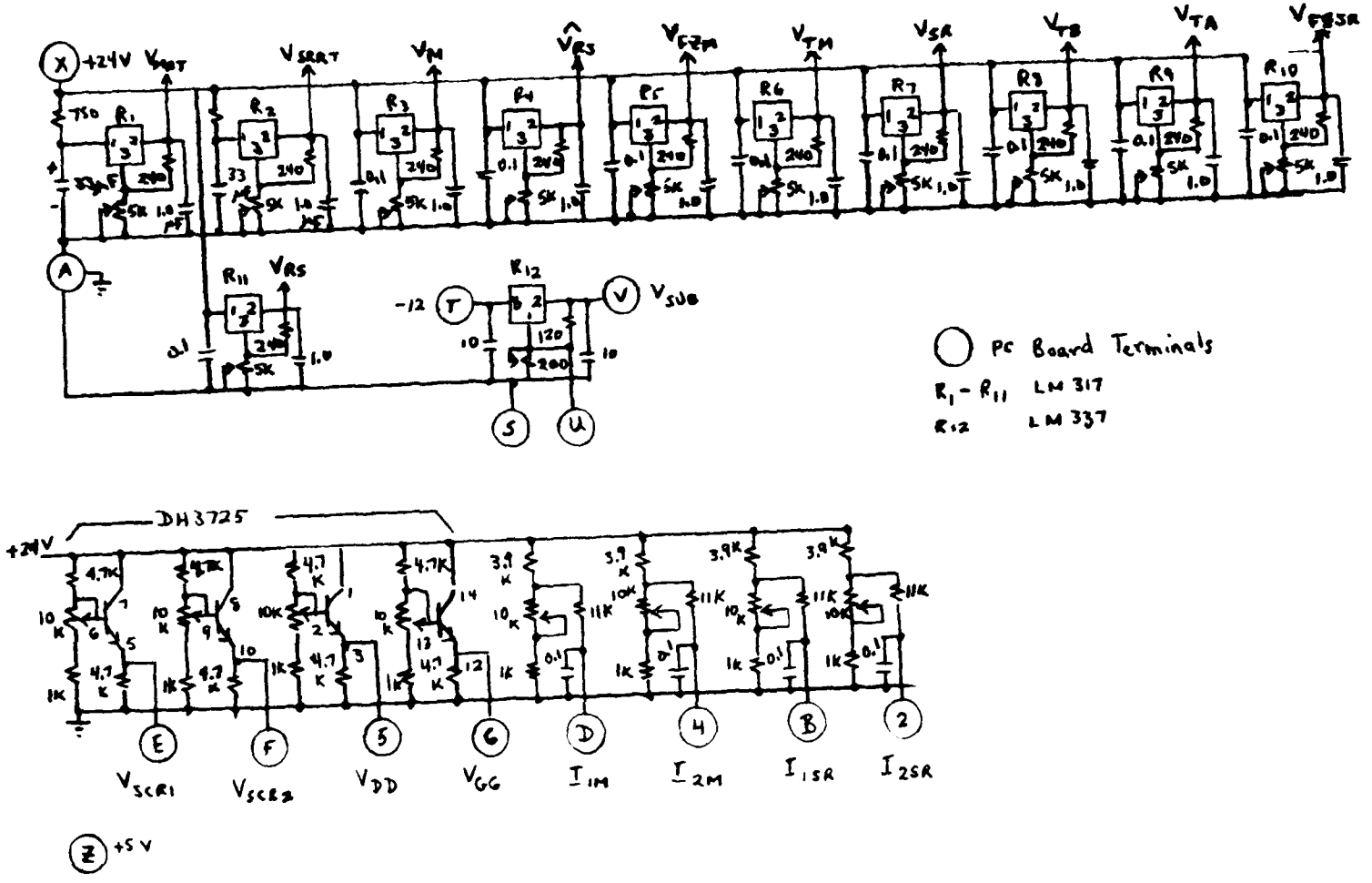


Figure 3.4 Bias circuits for 32 x 64 chip

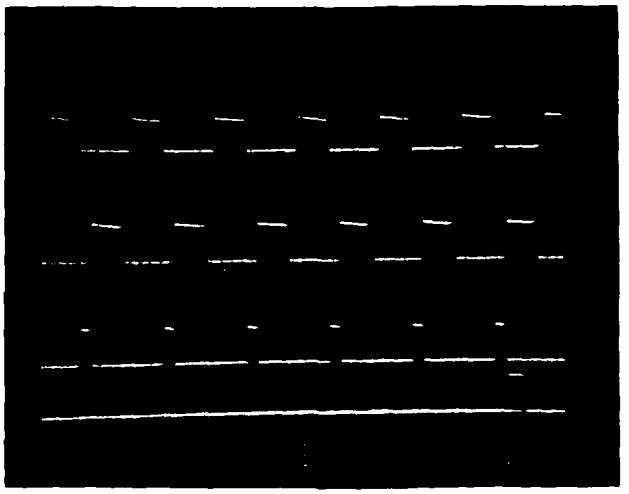


Figure 3.5 Operating waveforms, top to bottom, ϕ_{1M}, ϕ_{2M}, ϕ_{RS} and ϕ_{TM}.

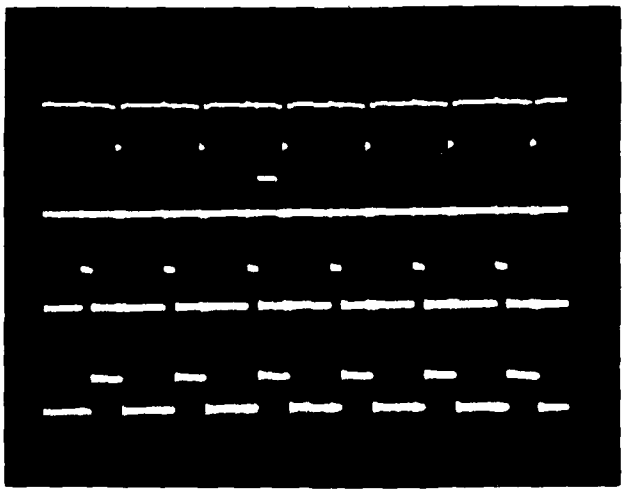


Figure 3.6 Operating waveforms, top to bottom, ϕ_{2M}, ϕ_{RS}, ϕ_{TM} and ϕ_{FZM}.

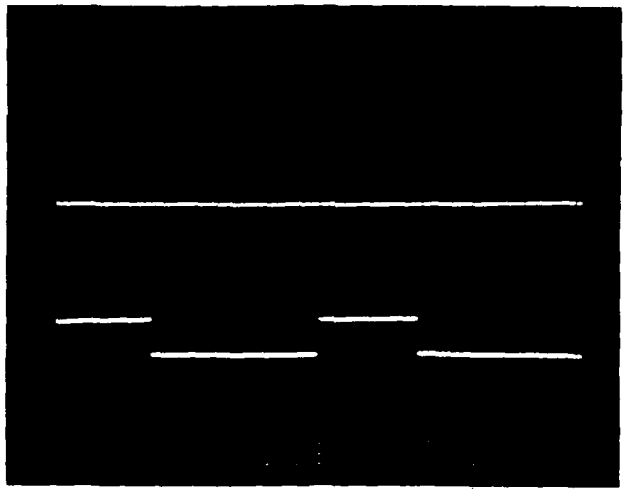


Figure 3.7 Operating waveforms, top $\emptyset_{TM}$, bottom $\emptyset_{2SR}$.

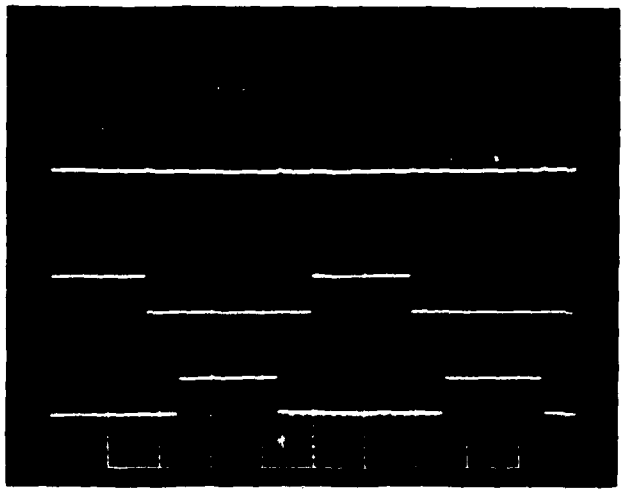


Figure 3.8 Operating waveforms, top to bottom, $\emptyset_{FZSR}$, $\emptyset_{2SR}$ and $\emptyset_{1SR}$.

SECTION IV

SERIAL ANALOG DELAY (SADL)

A. Introduction

The Serial Analog Delay Line (SADL) functions as a time-compressor/time-expander system. It utilizes the Fairchild CCD311 chip which is a 130/260 bit analog shift register with the capability of analog input sampling, delay and temporary storage of analog information. The SADL was designed to meet the following specifications:

(a) Maximum clock rate of 6 MHz.

(b) Maximum compression/expansion ratio of 6:1.

(c) Output blanked during reading time.

(d) Operation with internal or external clock at TTL levels.

(e) Read-in/read-out clock select internally derived.

(f) External input synch to begin operation.

(g) Dynamic range 50db minimum.

(h) Entire system compatible for TM500 power module.

B. CCD 311 Operation

A simplified diagram of the CCD 311 chip structure is shown in Figure 4.1a. As indicated it contains two 130 bit analog delay lines with a gated-charge detector preamplifier and a compensation amplifier common to both registers. The two lines may be multiplexed to double the sampling rate and thereby obtain an equivalent 260 bit delay line. Waveforms for multiplexed operation are shown in Figure 4.1b.

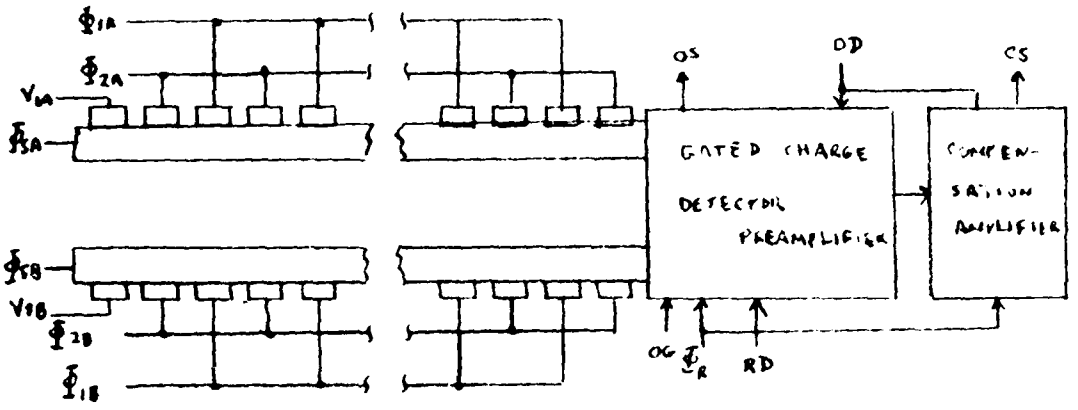


Figure 4.1a

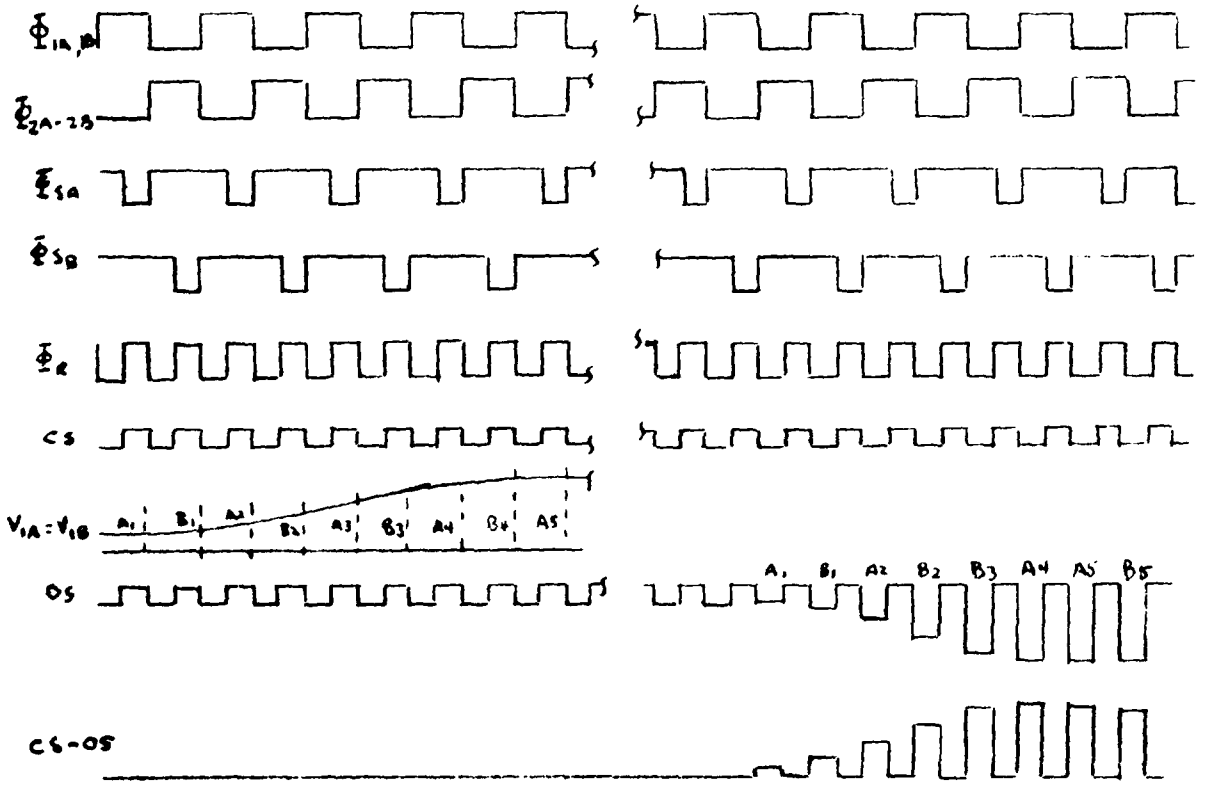


Figure 4.1b

CCD 311 simplified chip structure(a) and waveforms for multiplex operation(b)

With multiplex operation $\Phi_{1A} = \Phi_{1B}$ and $\Phi_{2A} = \Phi_{2B}$. The analog input is applied to both inputs V_{1A} and V_{1B}. Φ_{SA} and Φ_{SB} are the analog sample clocks for V_{1A} and V_{1B} respectively. Φ_R, the reset clock, must run at twice the rate of Φ_{1A} and Φ_{2A}.

Φ_R is internally coupled to the output to give the output signal OS from the on-chip preamplifier. The compensation amplifier provides the signal CS, at the Φ_R rate, so that an off-chip differential amplifier can be used to remove reset coupling from the video output, or CS-OS.

C. SADL Clock Generation

A simplified diagram of SADL clock circuitry is shown in Figure 4.2. The clock voltages Φ_R, Φ_1, Φ_2, Φ_{SA}, and Φ_{SB} correspond to those required for both read-in and read-out time intervals, i.e., the only variation is the difference in the rates. Consequently, the following discussion of the clock generation circuitry, while limited to the read-in interval, is applicable to either operation.

The MCK and MCK/6 outputs are inputs to the two-line to one-line decoder 2N74157. This is a quad decoder with 4 (Y) outputs controlled by a common SELECT logic level (S). With (S) low the (Y) output is /6 which is gated to the line driver SN74265(A) with complimentary outputs Φ_R and ϕ_R by means of NAND gate (A). Φ_R is converted from TTL level to Φ_R MOS level by driver amplifier D50026.

Φ_R is divided by 2 to obtain ϕR/2, the input to 2N74265(B) which gives the complimentary outputs Φ_1 and Φ_2. Φ_1 and Φ_2 are translated from TTL level to MOS level by DS0026(B), dual gate drivers, to obtain Φ_1 and Φ_2 which correspond to the clock voltages Φ_{1A} and Φ_{2A} in

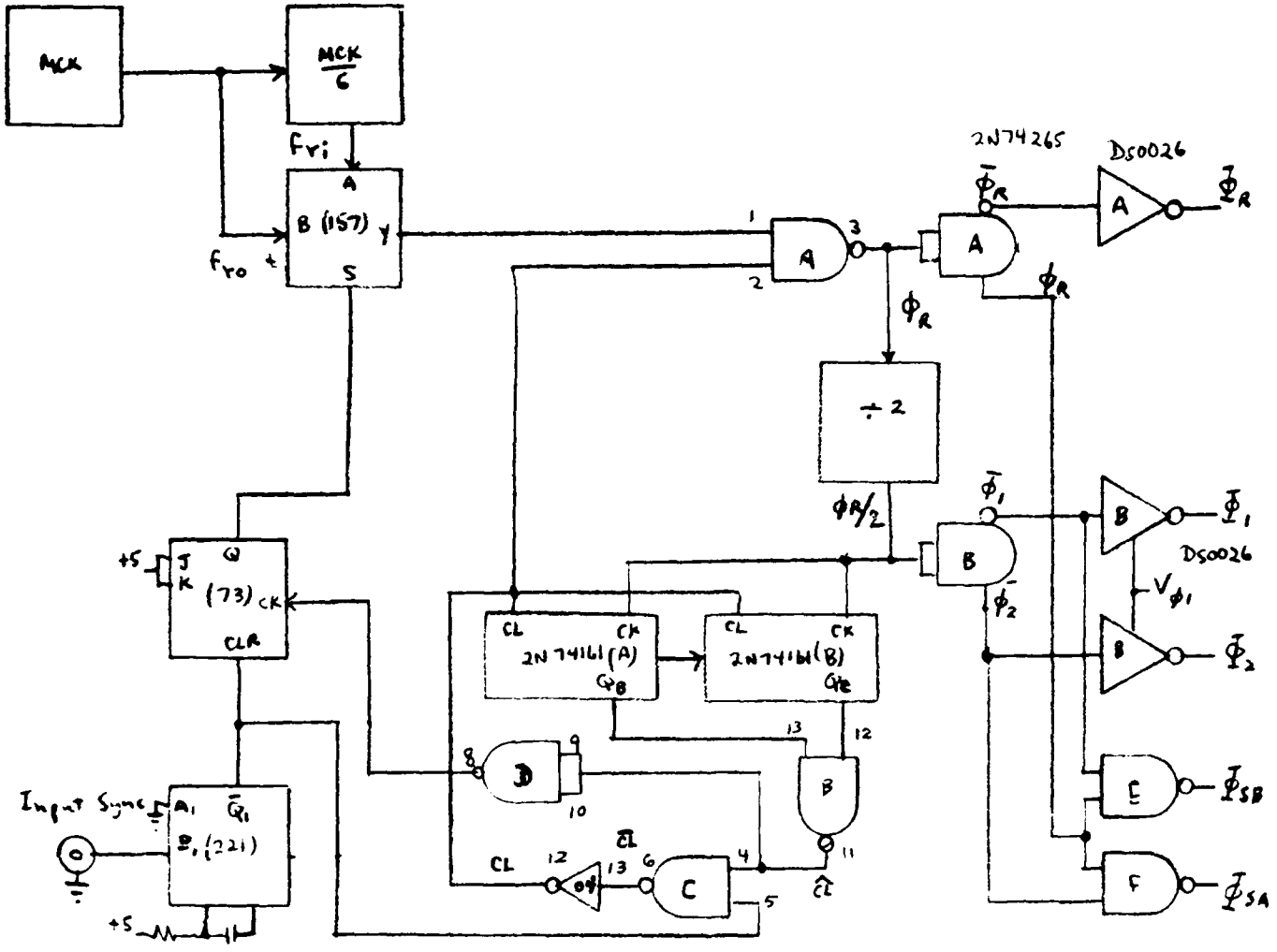


Figure 4.2 Simplified SADL clock circuitry

Figure 4.1b. The logic circuitry comprising NAND gate (E) and (F) with inputs $\overline{\Phi}_1$, $\overline{\Phi}_2$ and Φ_R generates the sample clock voltages $\overline{\Phi}_{SA}$ and Φ_{SB}.

The output of the divide by 2, $\Phi_R/2$ is the clock signal for the synchronous cascaded counters 2N74161 (A) and (B). After 130 cycles of $\Phi_R/2$ a $\hat{CL}$ pulse is obtained at the output of NAND gate (B). This input to NAND gate (C) coupled with other high input ($\overline{Q}_1$ of the one-shot FF 2N74221) gives $\overline{CL}$ as the input to inverter 7404. The output of the inverter then gives the desired clear pulse for the counters.

The purpose of NAND gate (C) and the JK FF 2N7473 is to allow for external synchronization and switching the output of the decoder at the end of the read-in time, and conversely at the end of the read-out time. With no external synch input signal $\overline{Q}_1$ of 2N74221 remains high which is the level of the CLR input for the 2N7473. $\hat{CL}$ is the CK input to the 2N7473. At the end of 130 counts the 7473 output Q toggles thereby changing the level of (S) of the decoder. The (Y) output is then connected to MCK to start the read-out time interval. One input to the NAND gate (A) is the counters CL signal level which is normally high. Consequently, the output of the decoder is gated through only when the counters are activated. If an external synch pulse occurs, the $\overline{Q}_1$ output is a negative pulse which synchronizes the start of the read-in time interval. During the duration of the $\overline{Q}_1$ negative pulse both counters and NAND gate (C) are disabled since the CL signal is low. Upon termination of the $\overline{Q}_1$ negative pulse (S) of the decoder is forced low by Q of the JK FF and the (Y) output is MCK/6. Simultaneously both counters and transmission NAND gate (C) are activated initiating the next read-in time interval.

Figures 4.3 and 4.4 are detailed diagrams of the total SADL system. Figure 4.3 shows the circuitry for MCK, MCK/6, $\overline{\Phi}_R$, Φ_R, $\overline{\Phi}_1$ and $\overline{\Phi}_2$. A 12 MHz crystal oscillator at TTL levels uses "D" FF $\frac{7474(C)}{2}$ to obtain MCK = 6 MHz at Pin 5. The combined logic circuitry of the "D" FF 7474(A) and the two NAND gates (A) is a divide by 1.5. Final division by 6 is accomplished by "D" FF (B) to obtain MCK/6.

Figure 4.4 contains the remainder of the clock generating circuitry for $\overline{\Phi}_{SA}$, $\overline{\Phi}_{SB}$, $\overline{\Phi}_{1A}$ and $\overline{\Phi}_{2A}$, bias circuitry for the CCD311, analog input circuitry and the video output circuits.

The outputs CS and OS from the CCD311 are buffered by emitter followers and capacitively coupled into the differential video amplifier μA733. This amplifier is a differential input-output configuration. The output from the μA733, CS-OS is coupled through an MOS switch, CD4053, to a discrete low impedance output emitter follower configuration capable of driving 50 ohms. The CD4053 switch is controlled by one section of the 74157 first used in Figures 4.2 and 4.3. Since Y output is controlled by the common (S) input, the switch will be closed during the read-out interval and open during the read-in interval.

D. Operating Waveforms

Waveforms for the operating SADL system are shown in Figures 4.5-4.9. Figure 4.5 indicates the CCD gate and sampling clock waveforms and the relative timing between the two. Figure 4.6 includes $\overline{\Phi}_R$ and Figure 4.7 is the same as Figure 4.6 on an expanded time scale. Figures 4.8 and 4.9 indicate the waveforms encountered for transition between the fast and slow clocks.

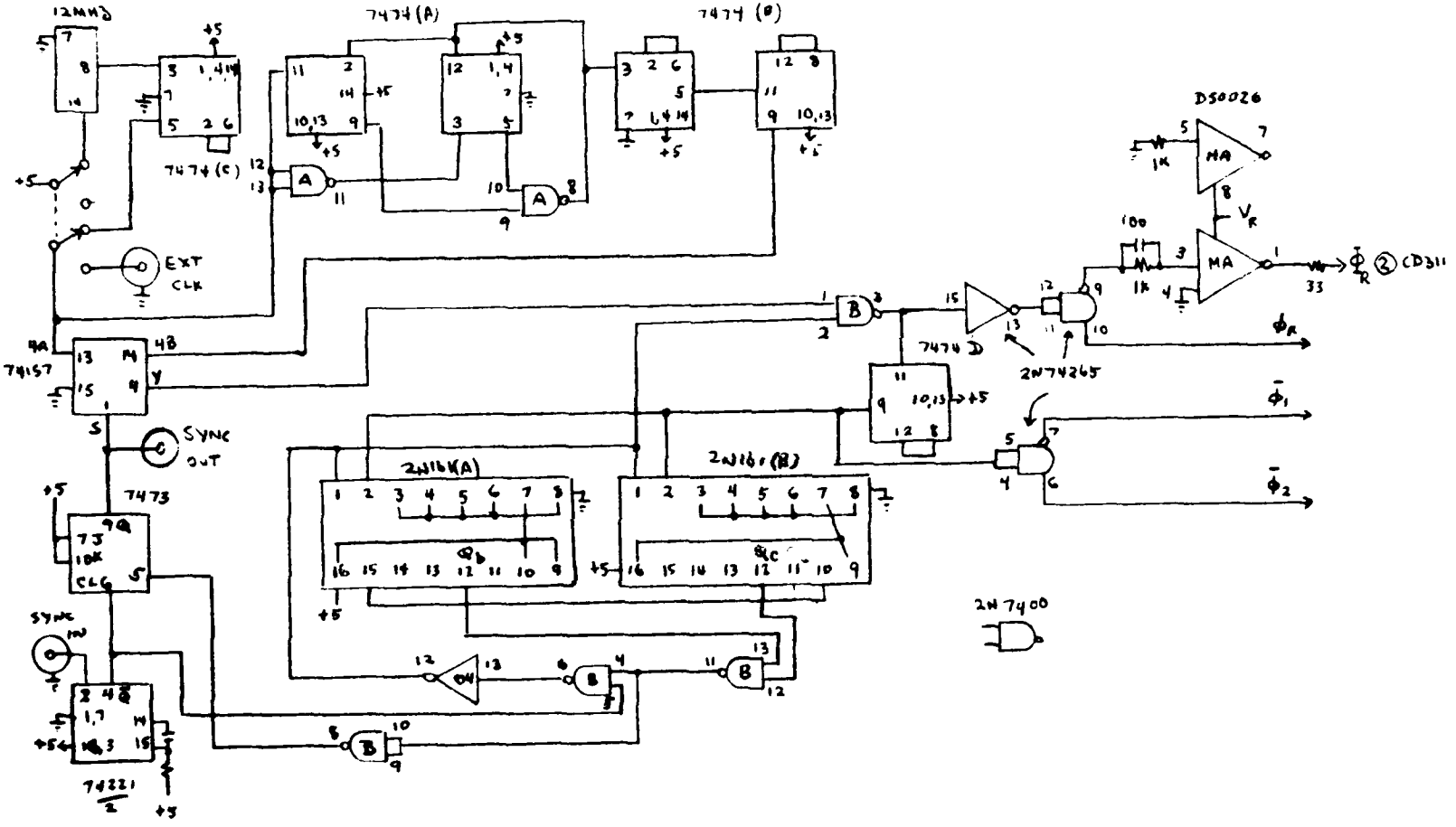


Figure 4.3 Detailed SADL clock circuitry for $\bar{\Phi}_R$, Φ_R, $\bar{\Phi}_1$ and $\bar{\Phi}_2$

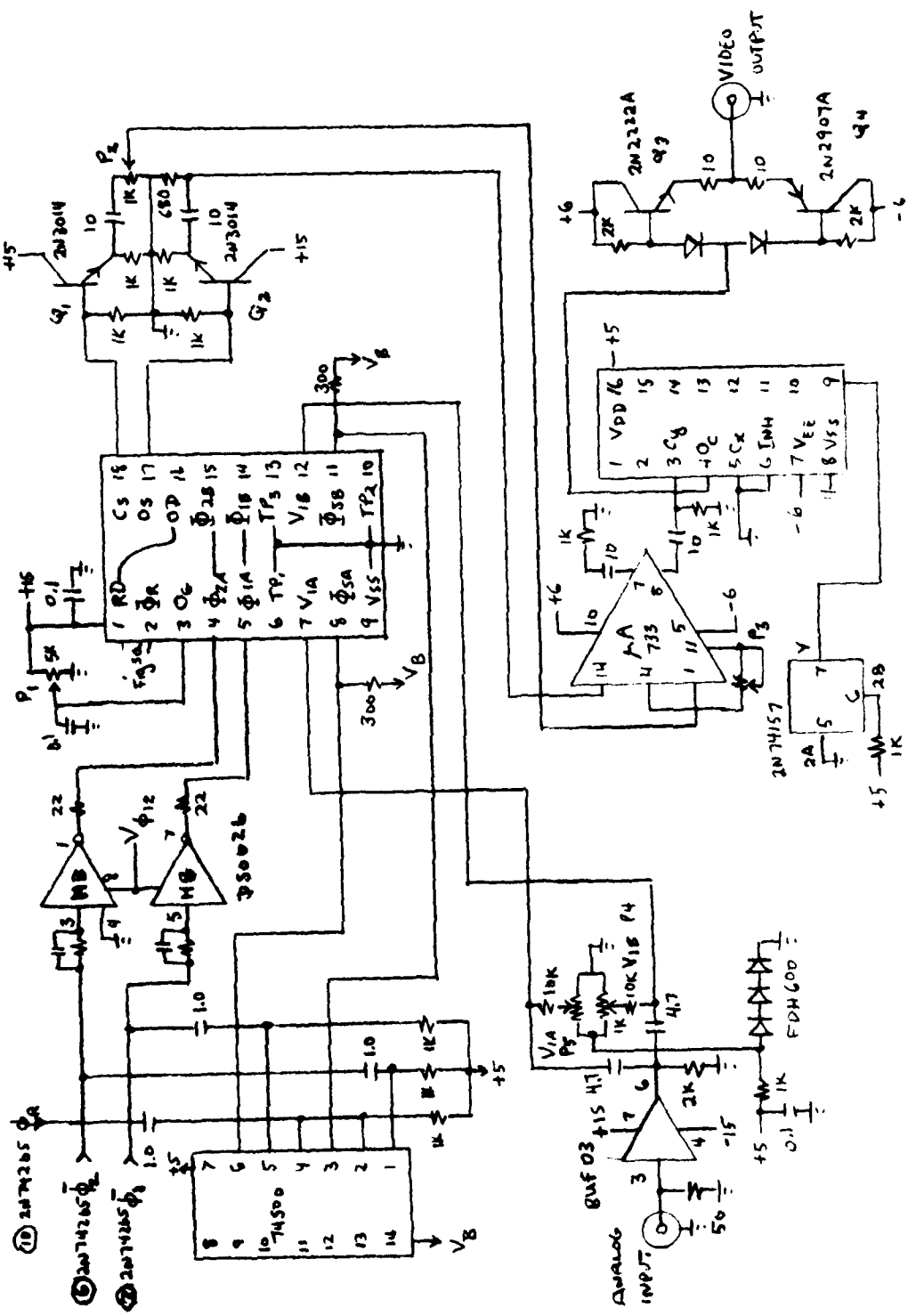


Figure 4.4 Detailed SADL clock circuitry for $\overline{\Phi}_{1A}$, $\overline{\Phi}_{2A}$, $\overline{\Phi}_{SA}$, $\overline{\Phi}_{SB}$

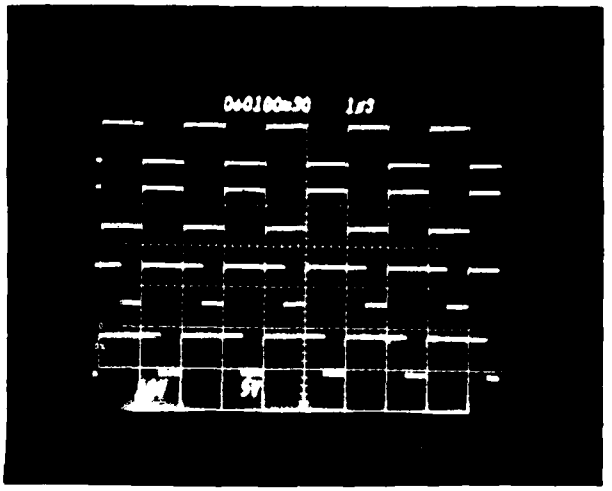


Figure 4.5 Operating waveforms, top to bottom, $\overline{\Phi}_{1A}$, $\overline{\Phi}_{2A}$, $\overline{\Phi}_{SA}$ and $\overline{\Phi}_{SB}$.

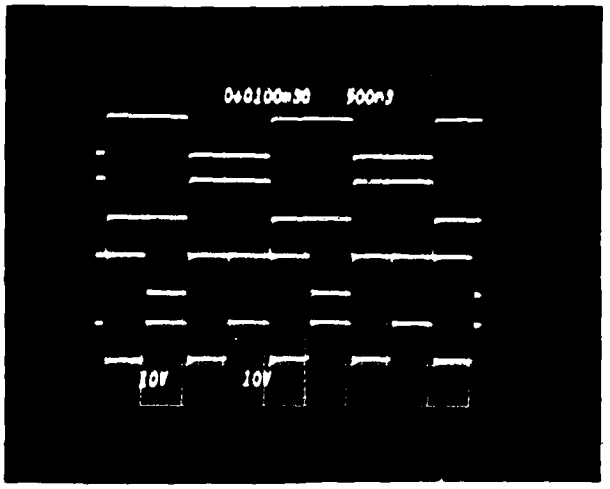


Figure 4.6 Operating waveforms, top to bottom, $\overline{\Phi}_{1A}$, $\overline{\Phi}_{2A}$, $\overline{\Phi}_{SA}$ and $\overline{\Phi}_{R}$.

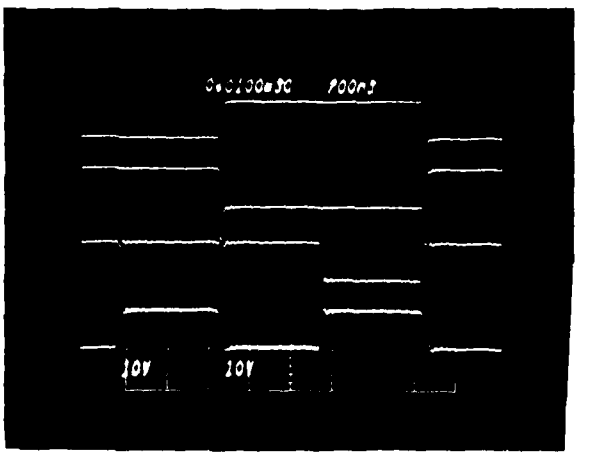


Figure 4.7 Operating waveforms, top to bottom, $\overline{\Phi}_{1A}$, $\overline{\Phi}_{2A}$, $\overline{\Phi}_{SA}$ and $\overline{\Phi}_{R}$.

Figure 4.8 Operating waveforms, transition from input to output cycle.

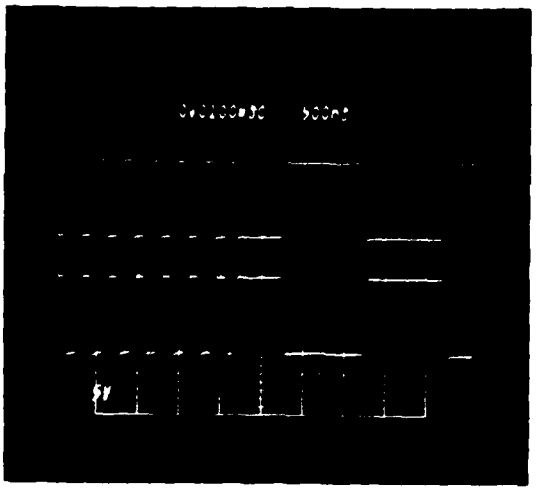


Figure 4.9 Operating waveforms, transition from output to input cycle.

E. SADL Fabrication

The SADL system was fabricated on a single board contained in a Tektonix single bin plug in unit used with a TM500 power module. Primary power from the TM500 module is used with an on-board regulating system to obtain $\pm$ 15 volts and + 5 volts. Double regulation for the $\pm$ 6 volts, used for the μA733 and the video output stage, is obtained using LM317 and LM337 regulators and the primary $\pm$ 15 volt supplies. Variable voltages for the Φ_{1A} - Φ_{2B} clock, Φ_R clock and Φ_{SA}, Φ_{SB} clock are obtained using LM317 regulators. The regulator circuits are shown in Figure 4.10. The board layout showing controls and placement of components is shown in Figure 4.11. Panel layout is in Figure 4.12.

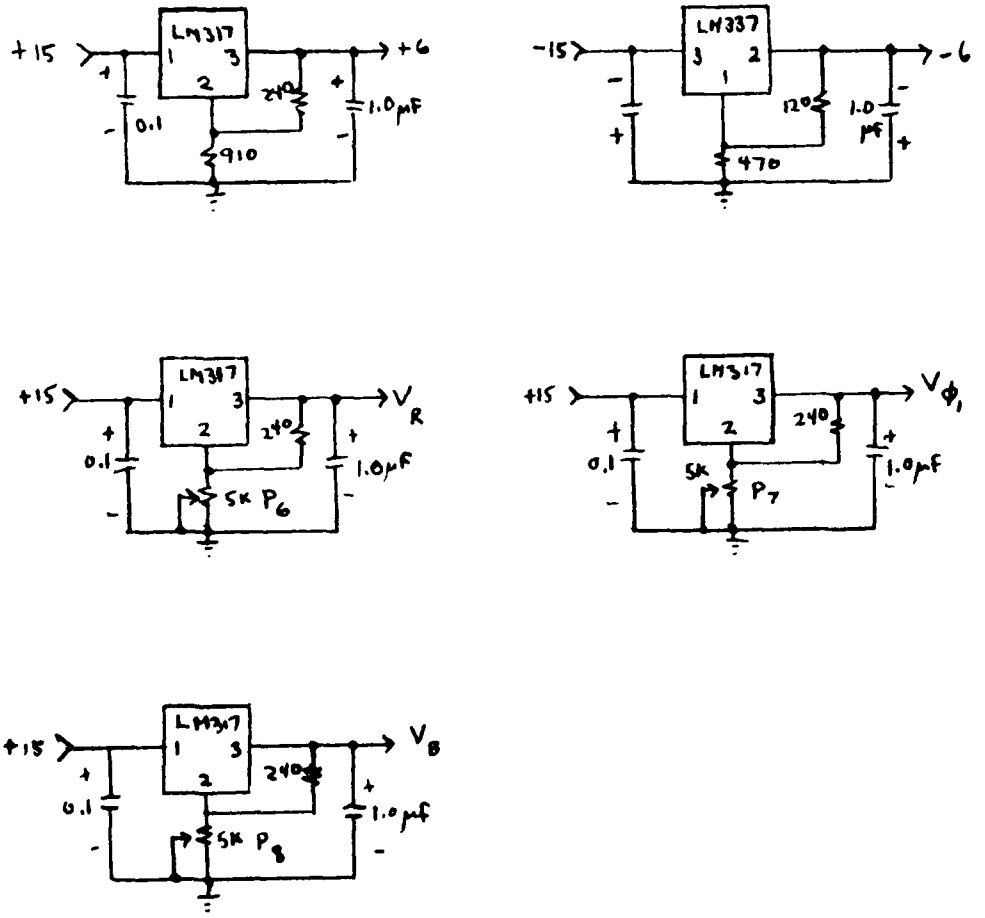


Figure 4.10 SADL bias regulator circuits

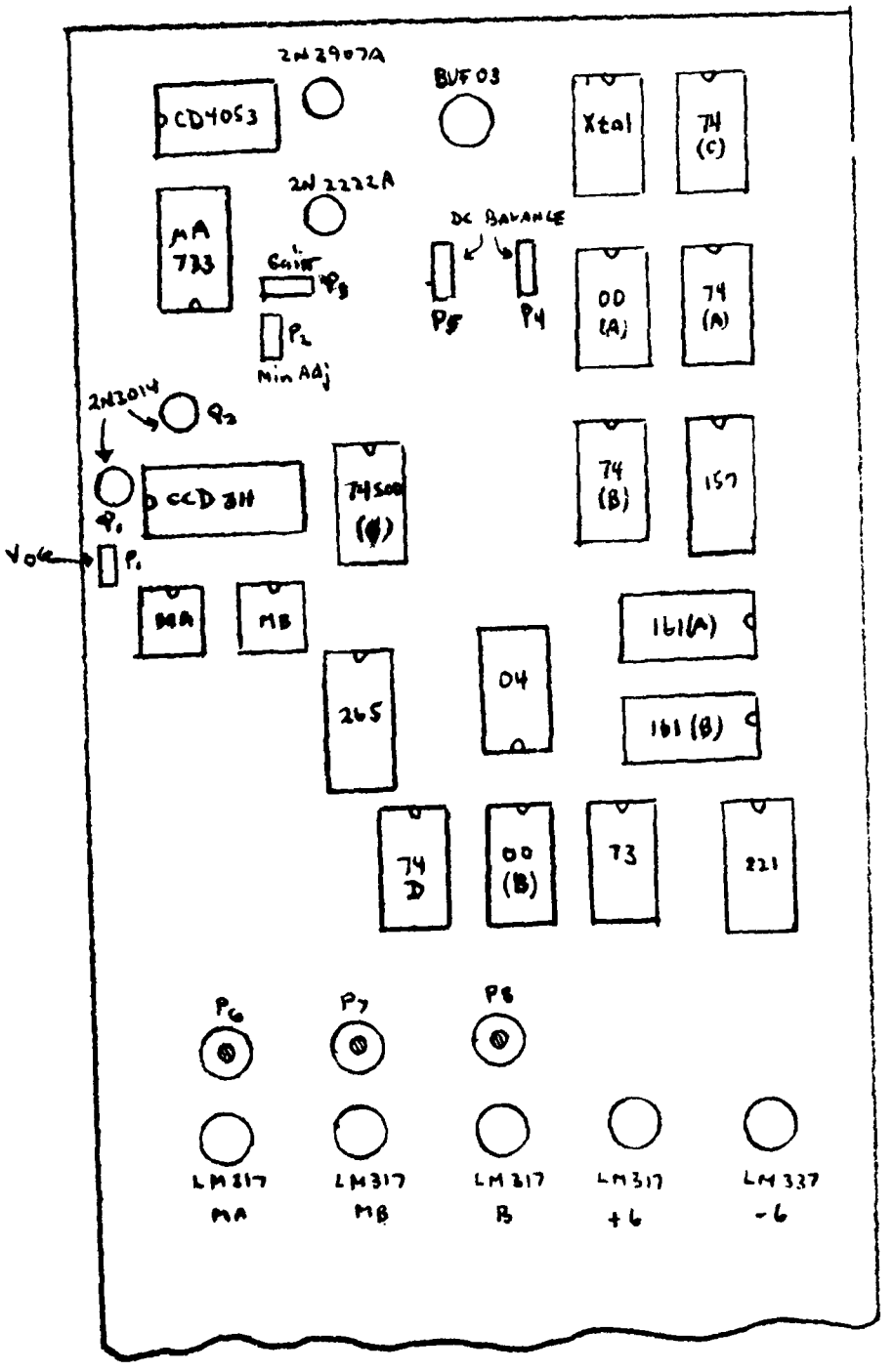


Figure 4.11 SADL board layout

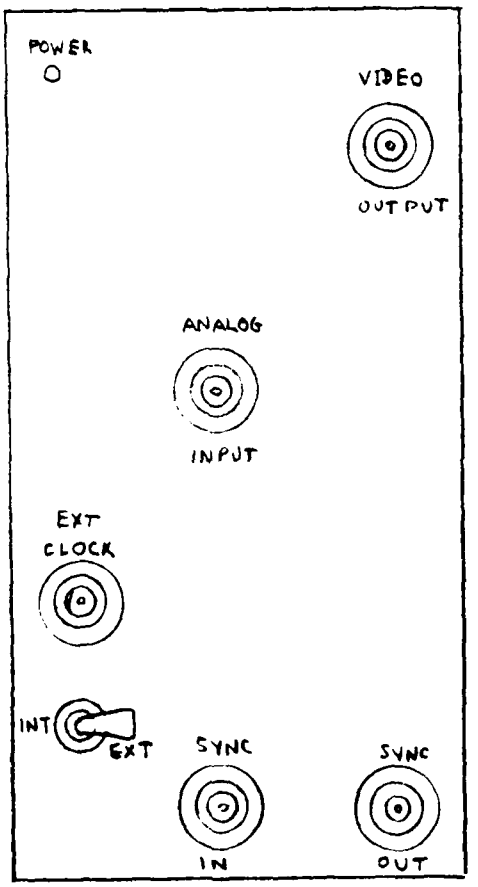


Figure 4.12 SADL panel layout

SECTION V

CONCLUSIONS

A. LIRCCD

This testbed module has been shown to function as designed and demonstrated the capability of using a μprocessor to control stare time on demand. Both models could be miniaturized even further by restricting the multi-turn potentiometers for only the critical variables. The environmental model will require long term evaluation under all possible weather conditions. If it proves necessary there is sufficient space in the sealed package to use a temperature controlled crystal oven for the crystal master oscillator.

B. 2DIRCCD

The 32 x 64 element test-bed module was found to function satisfactorily from the viewpoint of the given specifications. A definitive evaluation awaits the availability of operational chips.

C. SADL

The sampled analog delay line meets the given specifications. Some minor difficulties were encountered with clock feed through, but these appear to be resolvable by some fine tuning and additional filtering.

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2. Cochrun, B.L., "Signal Processing Circuit Development", Final Report, RADC-TR-80-260, September 1980.

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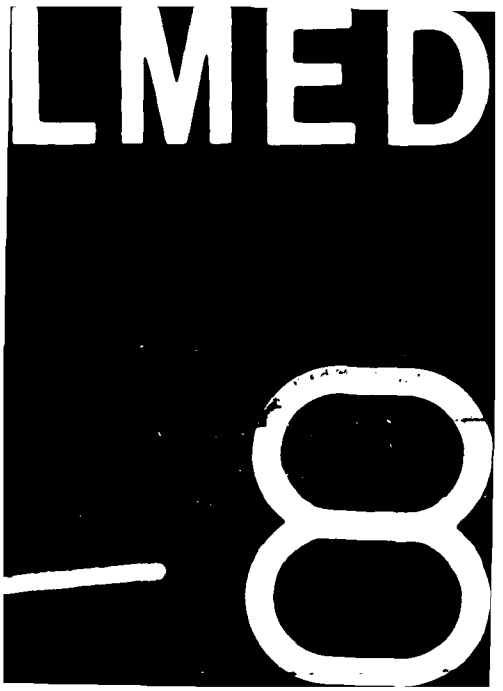
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