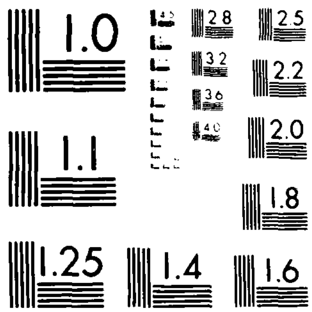
AD-A142 599 LOSSLESS SYMMETRIC TEM LINE IMPATT DIODE POWER COMBINERS(U) MICHIGAN UNIV ANN ARBOR ELECTRON PHYSICS LAB R ACTIS APR 84 TR-164 AFWAL-TR-84-1035 1/2

UNCLASSIFIED F33615-81-K-1429 F/G 9/5 NL



MICROCOPY RESOLUTION TEST CHART
NATIONAL BUREAU OF STANDARDS-1963-A

-(12)

AFWAL-TR-84-1035

LOSSLESS SYMMETRIC TEM LINE IMPATT DIODE POWER COMBINERS

One of a series of reports on Millimeter-Wave Circuit Analysis and Synthesis

R. Actis

Electron Physics Laboratory
Department of Electrical and Computer Engineering
The University of Michigan
Ann Arbor, Michigan 48109

AD-A142 599

April 1984

Interim Report for Period March 1, 1981-June 30, 1983

Approved for public release; distribution unlimited.

AVIONICS LABORATORY
AIR FORCE WRIGHT AERONAUTICAL LABORATORIES
AIR FORCE SYSTEMS COMMAND
WRIGHT-PATTERSON AIR FORCE BASE, OHIO 45433

NOTICE

When Government drawings, specifications, or other data are used for any purpose other than in connection with a definitely related Government procurement operation, the United States Government thereby incurs no responsibility nor any obligation whatsoever; and the fact that the government may have formulated, furnished, or in any way supplied the said drawings, specifications, or other data, is not to be regarded by implication or otherwise as in any manner licensing the holder or any other person or corporation, or conveying any rights or permission to manufacture use, or sell any patented invention that may in any way be related thereto.

This report has been reviewed by the Office of Public Affairs (ASD/PA) and is releasable to the National Technical Information Service (NTIS). At NTIS, it will be available to the general public, including foreign nations.

This technical report has been reviewed and is approved for publication.

Robert Blumgold
ROBERT BLUMGOLD
Project Engineer
Microwave Techniques & Applications Grp

Robert T. Kemerley
ROBERT T. KEMERLEY, Acting Chief
Microwave Techniques and Applications Grp
Microwave Technology Branch

FOR THE COMMANDER

Donald S. Rees
DONALD S. REES, Chief
Microwave Technology Branch
Avionics Laboratory

"If your address has changed, if you wish to be removed from our mailing list, or if the addressee is no longer employed by your organization please notify AFWAL/AADM, W-PAFB, OH 45433 to help us maintain a current mailing list."

Copies of this report should not be returned unless return is required by security considerations, contractual obligations, or notice on a specific document.

Unclassified

SECURITY CLASSIFICATION OF THIS PAGE (When Data Entered)

REPORT DOCUMENTATION PAGE		READ INSTRUCTIONS BEFORE COMPLETING FORM
1. REPORT NUMBER AFWAL-TR-84-1035	2. GOVT ACCESSION NO. AD-A142599	3. RECIPIENT'S CATALOG NUMBER
4. TITLE (and Subtitle) LOSSLESS SYMMETRIC TEM LINE IMPATT DIODE POWER COMBINERS		5. TYPE OF REPORT & PERIOD COVERED Interim Tech March 1, 1981-June 30, 1983
		6. PERFORMING ORG. REPORT NUMBER Tech. Report No. 164
7. AUTHOR(s) Robert Actis		8. CONTRACT OR GRANT NUMBER(s) F33615-81-K-1429
9. PERFORMING ORGANIZATION NAME AND ADDRESS Electron Physics Laboratory The University of Michigan Ann Arbor, MI 48109		10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS 20020392
11. CONTROLLING OFFICE NAME AND ADDRESS Avionics Laboratory (AFWAL/AADM-2) Air Force Wright Aeronautical Laboratories Wright-Patterson AFB, OH 45433		12. REPORT DATE April 1984
		13. NUMBER OF PAGES 147
14. MONITORING AGENCY NAME & ADDRESS(if different from Controlling Office)		15. SECURITY CLASS. (of this report) Unclassified
		15a. DECLASSIFICATION DOWNGRADING SCHEDULE N/C

16. DISTRIBUTION STATEMENT (of this Report)

Approved for public release; distribution unlimited.

17. DISTRIBUTION STATEMENT (of the abstract entered in Block 20, if different from Report)

18. SUPPLEMENTARY NOTES

19. KEY WORDS (Continue on reverse side if necessary and identify by block number)

Power combining
Negative-resistance devices
Lossless symmetric TEM line combining networks
IMPATT diodes
N-way resonant combiners

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

The results of an experimental investigation into a new approach to circuit-level power combining of negative-resistance devices are presented. The approach uses the properties of symmetric lossless TEM line combining networks together with the bandlimited characteristics of IMPATT diodes to achieve stable combiner designs having improved bandwidths over other approaches. The combining networks utilized in this investigation fall into the category of N-way nonresonant combiners which are often associated with various bandlimiting resistive stabilization techniques for suppressing non-power-producing

DD FORM 1 JAN 73 1473

Unclassified

SECURITY CLASSIFICATION OF THIS PAGE (When Data Entered)

20. (Contd.)

interactions among the devices. This combining design requires no such stabilizing scheme. Suppression of undesired odd modes is accomplished in lossless circuits by an appropriate combination of device and circuit which provides the necessary condition for a stable combiner.

An experimental realization of the simplest example of a lossless symmetric combiner design is presented in two different circuit mediums. A two-diode microstrip combiner and a two-diode coaxial combiner were developed to demonstrate the design principles. The combiners operated in a stable nonspurious amplifier configuration. A 3-dB bandwidth of 16 percent with 4.2 dB of gain was observed in 94 percent combining efficiency.

FOREWORD

This report describes the studies of lossless symmetric TEM line IMPATT diode power combiners carried out at the Electron Physics Laboratory, Department of Electrical and Computer Engineering, The University of Michigan, Ann Arbor, Michigan. The work was sponsored by the Air Force Systems Command, Avionics Laboratory, Wright-Patterson Air Force Base, Ohio under Contract No. F33615-81-K-1429.

The work reported herein was performed during the period March 1, 1981 to June 30, 1983 by Dr. Robert Actis. The report was released by the author in June 1983.

The author wishes to thank Professor D. F. Peterson, his dissertation chairman, for his encouragement and guidance as well as Professors G. I. Haddad and V. V. Liepa and Mr. J. R. East for their advice and support throughout the research effort. He would also like to thank Dr. D. C. Yang for help in fabricating the microstrip circuits and with the automated measurement system and Drs. R. K. Mains, P. A. Blakey, and J. C. Chen for many helpful discussions.

TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

Figure		Page
3.5	Smith Chart Plot of Impedance Data Obtained from a Short Circuit Termination at the Device Terminals. Data Corresponding to ℓ_2 Is Closest to Representing a Short Circuit in the Measurement Frequency Bandwidth and Establishes the Length from the Calibrated Measurement Reference Plane to the Device Terminals.	37
3.6	Large-Signal Automated Test Set.	38
3.7	First Generation Microstrip 50-Ω Test Circuit.	40
3.8	Reflection Coefficient of a Device Measured in a Coaxial Test Fixture Using a 6- to 50-Ω Impedance Transformer.	41
3.9	Electrical Equivalent of a Coaxial Test Circuit Useful for Establishing Impedance Level on Microstrip.	42
3.10	(a) Microstrip Circuit Fixture for Device Characterization and (b) Circuit Equivalent of Device Characterization Fixture.	44
3.11	Reflection Coefficient Magnitude of a Device Measured in the Microstrip Test Circuit of Fig. 3.10	45
3.12	Single-Diode Small-Signal Impedance Corresponding to Fig. 3.11. Data Is Normalized to 50 Ω and Rotated Through a Length of Transmission Line Functioning as the Quarter-Length Impedance Transformer.	47
3.13	Plot of Small-Signal Impedance Showing the Similarities of Four Candidate Microstrip-Combiner Diodes.	48
3.14	Single Device Microstrip Test Fixture with Bias Circuit.	49
3.15	(a) Top View of a Single Device Microstrip Test Circuit with Bias Circuit. (b) Bias Test Circuit.	51
3.16	Small-Signal Reflection Gain of a Device Measured in the Microstrip Test Circuit of Fig. 3.14	52

Figure		Page
3.17	Plot of Small-Signal Negative Impedance Associated with Fig. 3.16. The Data is Rotated Through a Length of Transmission Line and Normalized to 50 Ω. A Stable Combiner Design is Possible by Selecting a Circuit Impedance Z_c which Exhibits Impedance at 3.8 and 5.1 GHz as Shown.	[illegible]
3.18	Electrical Equivalent Circuit of Two-Diode Microstrip Combiner.	[illegible]
3.19	Illustration of Microstrip Combiner Test Fixture.	[illegible]
3.20	Two-Diode Microstrip Combiner Test Fixture.	[illegible]
3.21	Microstrip Circuit Board of the Two-Diode Microstrip Combiner Mounted on the Circuit Fixture.	[illegible]
3.22	Coaxial Line which Protrudes Through the Alumina Substrate to Form the Coaxial-to Planar Transition at the Combining Point.	[illegible]
3.23	Cross Section View of One-Half of the Two-Diode Microstrip Combiner Used in Characterizing Single Devices.	[illegible]
3.24	Reflection Gain of a Typical Diode as Measured in the Microstrip Combiner Circuit.	[illegible]
3.25	Individual Diode Small-Signal Impedance Curve for Three Different Bias Levels. Negative Impedance is Plotted and Normalized to 50 Ω. Data is Referenced to the Measurement Plane Shown in the Inset.	66
3.26	Large-Signal Device Characterization Results as Measured in the Two-Diode Combiner Circuit. Data Corresponds to 100 mA Bias Current Level.	68
3.27	Measured Added Power Data for a Microstrip Combiner Diode (100 mA Bias Current).	[illegible]
3.28	Small-Signal Reflection Gain of the Two-Diode Microstrip Combiner.	[illegible]
3.29	Measured Small-Signal Combiner Impedance for the Microstrip Combiner. Three Bias Current Levels are Shown. The Combining Port Load Impedance Z_L Is 50 Ω.	73

LIST OF SYMBOLS

a	Input power wave to a network.
b	Reflected power wave from a network.
E	Scattering coefficient associated with a measurement error network.
f	Frequency.
I	RF current.
ℓ	Length of transmission line.
N	Total number of devices.
P_{at}	Total combiner added power or generated power.
P_{gen}	Power generated by network/device. Identical to added power.
P_{in}	Input power injected into network.
P_{ref}	Reflected power from network/device.
Q	Quality factor.
R_d	Real part of device impedance, Z_d.
X_d	Imaginary part of device impedance, Z_d.
X_k	Combiner network eigenvectors.
Z	Impedance.
Z_c	Circuit impedance.
Z_d	Device impedance.
Z_L	Load impedance.
Z_m	Measured impedance.
Z_o	Characteristic impedance of transmission line.
$[Z_T]$	Combiner port termination matrix.
α	Constant defined in Chapter II.
β	Transmission line propagation constant.

Γ	Reflection coefficient.
η	Efficiency.
θ	Transmission line angle defined in Chapter II.
θ_c	Angle defined on Smith chart and associated with ω_c.
θ_m	Angle defined on Smith chart and associated with ω_m.
θ_T	Thermal resistance.
λ	Wavelength.
λ_k	Combiner network eigenvalues defined in Chapter II.
ω	Angular frequency.
ω_c	Angular frequency when device becomes active.
ω_m	Maximum angular frequency associated with active device.

CHAPTER I

INTRODUCTION AND OVERVIEW

This report presents the results of an experimental investigation regarding a new approach to circuit-level power combining of multiple negative-resistance devices. The proposed approach[1] makes use of radially symmetric lossless TEM line combining networks together with bandlimited negative-resistance devices to provide an improved, spurious-free design.

The combining networks studied are N-way nonresonant combiners which generally use bandlimiting resistive stabilization techniques to suppress undesirable interactions among devices. A unique feature of the new design is that no resistive stabilization technique is required. Suppression of the undesired device interactions is accomplished using lossless symmetric circuits by an appropriate "marriage" of device and circuit which provides the necessary conditions for stable combining.

This investigation is concerned with realizing combiners that make use of this approach to achieve stable combiners/amplifiers. Two combiners that have successfully demonstrated stable combining operation will be described. One design was developed in microstrip, and another was realized in a coaxial environment. Both combiners utilized two-IMPATT diodes in a symmetric circuit configuration. The appropriate circuit design to provide stable operation was obtained by determining the device properties of candidate combiner diodes in various test circuits, and then selecting a circuit which suppressed undesired device-circuit interactions. The performance of both combiners demonstrated nonspurious stable amplifier operation. A successful verification of the basic design approach was achieved.

1.1 Survey of Combining Techniques

The present state of microwave power combining techniques has recently been effectively summarized in various review articles.[2-4] Essentially, circuit-level power combining techniques can be classified into two basic categories: (1) "corporate" or "serial" combiners, which successively combine increasing levels of power; and (2) "N-way"combiners in which RF power from multiple devices is combined in a single step. The N-way combiners can be further sub-categorized into resonant and nonresonant structures. The waveguide combiner of Kurokawa and Magalhaes[5] and the circular cavity combiner of Harp and Stover[6] are examples of resonant structures. The Wilkenson N-way combiner[7] and Rucker's five-way combiner[8] are examples of nonresonant N-way combiners.

Each of the combining schemes mentioned has advantages and associated limitations. Corporate or serial combiners have inherent isolation among devices thereby eliminating non-power-producing interactions while providing broadband performance. However, substantial circuit losses can decrease combining efficiency in these structures. Resonant N-way combiners usually require some form of selective stabilization resistors to suppress undesired interactions among devices. In addition, the high-Q nature of the cavity circuitry usually leads to narrowband operation. These combiners do, however, have higher combining efficiencies since power generated has a more direct path to the output. Nonresonant

N-way structures provide larger amplifier bandwidths with a corresponding increase in the mode suppression problem.

The combining circuits considered in this report can be classified as N-way nonresonant TEM transmission line networks. Figure 1.1 illustrates where these combining structures are placed in the overall hierarchy. These combiners offer a new approach to N-way nonresonant combiner design in that the suppression of undesired combiner instabilities is accomplished without bandlimiting resistive stabilization techniques. The mode suppression problem is handled in lossless circuits by an appropriate selection of device and circuit which provides the necessary conditions for a stable combiner.

1.2 Outline of Experimental Investigation

The goal of this study is an experimental verification of a new approach to circuit-level power combining in which lossless TEM line combining networks are used with bandlimited IMPATT devices to realize stable combiners. The purpose of the designs realized in this investigation is not to achieve high power capability but rather to demonstrate a technique for realizing stable combiner/amplifier networks. In Chapter II of this report a summary of the theory pertaining to lossless N-way IMPATT diode power combiners is presented. An in-depth analysis of these types of combining structures is documented in a report by Peterson and Haddad.[10] These aspects of analysis relevant to the impedance description of the experimental combiner are reviewed for reference. The summary includes a

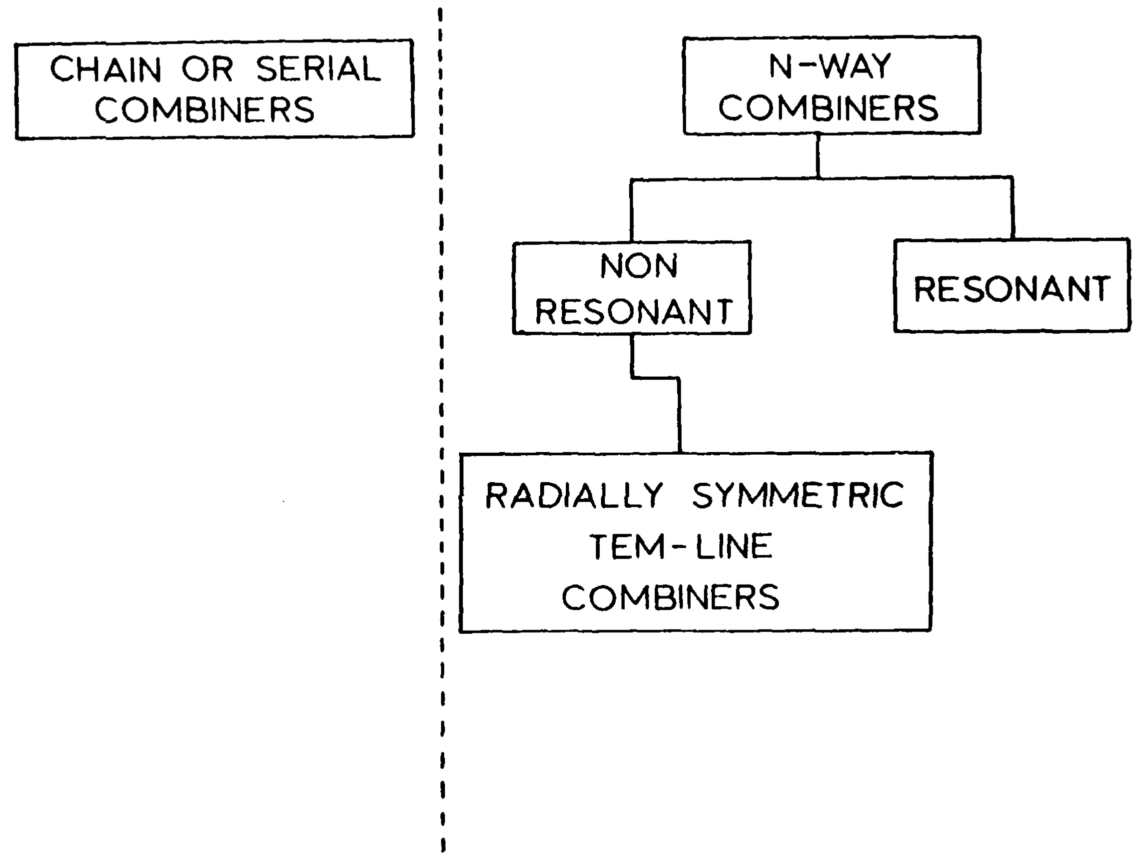


FIG. 1.1 BASIC CATEGORIES OF CIRCUIT-LEVEL POWER COMBINING TECHNIQUES. RADIALLY SYMMETRIC TEM LINE COMBINERS ARE A SUBCATEGORY OF N-WAY NONRESONANT STRUCTURES.

description of the general combiner network along with a detailed discussion of the undesired interactions that can occur among active devices in combiners of this type. Stability constraints imposed on the combiner circuitry are described which insure stable combiner operation while providing adequate design flexibility.

A description of the various diode test circuits used to characterize and select appropriate devices is given in Chapter III. The measurement test set is briefly described, and device characterization results are presented. Section 3.2 details the design and construction of a two-diode microstrip example that successfully verifies the lossless approach to IMPATT diode power combining. Characterization results of single and two-diode operation are presented for both small- and large-signal drive levels. Section 3.3 provides a further example of a lossless combiner design. In this case a coaxial circuit design provides the power summing function. Descriptions of single- and multiple-diode circuits are presented along with characterization results.

The last section of this report includes conclusions on the work and suggests some ideas for further work.

CHAPTER II

THEORY OF LOSSLESS N-WAY SYMMETRICAL IMPATT DIODE POWER COMBINERS

2.1 Combiner Network Description

A generalized network which can be used to combine RF power from multiple negative-resistance devices is illustrated in Fig. 2.1. The combiner structure is an N + 1 port network. N-ports are provided to accommodate the active device terminations while one port functions as the "combining port" providing common excitation and combined RF power output. This port is labeled as the zeroth port in Fig. 2.1 and is terminated in a load impedance of Z_L. The matrix description of the combiner circuit and the active device terminations will be used to establish the combiner network properties and operation. Moreoever, the circuit conditions for realizing a stable lossless combiner design using IMPATT devices will be described.

Each of the N-device ports is terminated with an active negative-resistance device. In this investigation, IMPATT diodes are used as the active device terminations. Each active device can be associated with an impedance describing function, $Z_d(\omega,|I|)$, which is a function of angular frequency ω and RF current amplitude $|I|$. The impedance describing function of each of the N-devices, along with the load impedance terminating the combining port, can be represented in a diagonal termination matrix given by

$$[Z_T] = \mathrm{diag}\{Z_L(\omega), Z_{d1}(\omega,|I_1|) \ldots Z_{dN}(\omega,|I_N|)\} \quad . \quad (2.1)$$

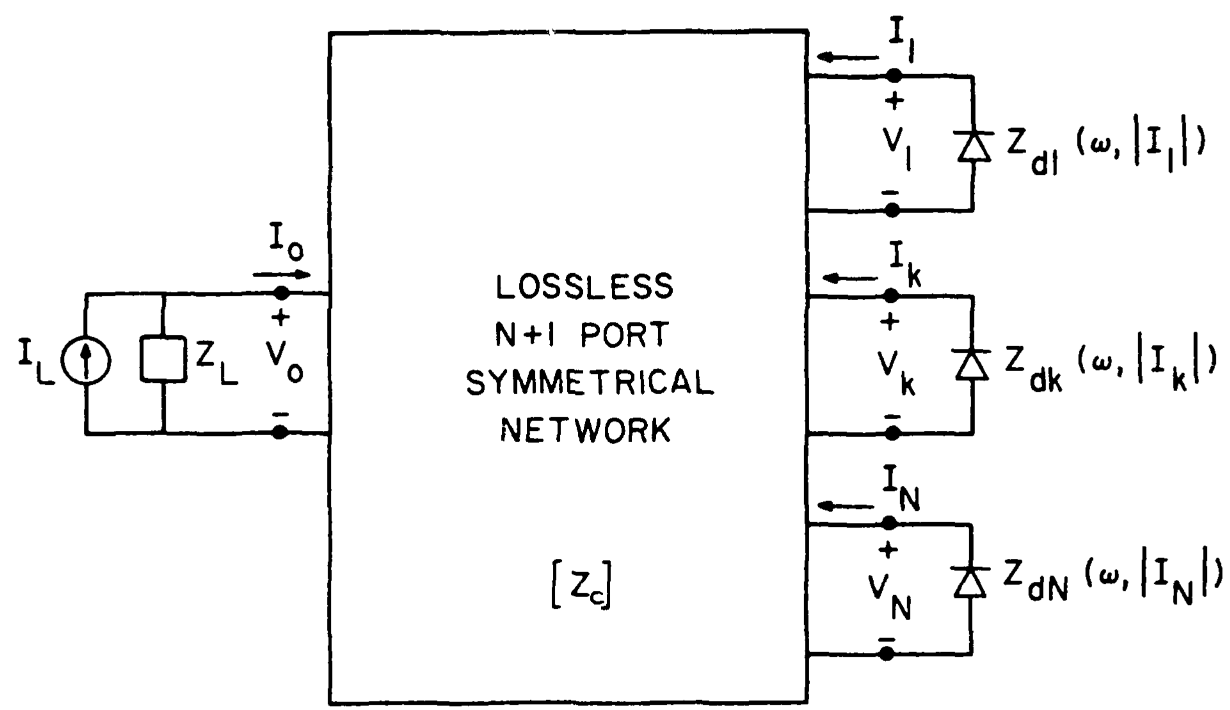


FIG. 2.1 GENERAL COMBINER NETWORK DEFINITION.

The combiner circuit is a symmetric arrangement of TEM transmission lines, connecting active negative-resistance devices to a central combining point. As part of the combiner network, the circuit can be described by an impedance matrix $[Z_c]$ given by

$$[Z_c] = \begin{bmatrix} Z_{od} & Z_{od} \cdots\cdots Z_{od} \\ Z_{od} & \\ \cdot & \\ \cdot & [Z] \\ \cdot & \\ Z_{od} & \end{bmatrix} ,$$

where $[Z]$ is an $N \times N$ matrix with elements Z_{mn} $(m,n = 1$ to $N)$ which are associated with only the combiner device ports (i.e., 1 to N). The symmetry properties and reciprocity of the combiner circuit are reflected in $[Z]$ which has the properties of a "circulant" matrix, that is, any row of $[Z]$ is a "rolled" version of any other row.[1] The elements of the matrix $[Z_c]$ represent the impedances of the combiner circuit looking in from the various device ports and the combining port accordingly.

2.2 Non-Power-Producing Interactions in Multiple Device Networks

When combining multiple devices in a single circuit, there exists the potential for non-power-producing interactions (combiner odd modes) among the devices being combined. These interactions which result in combiner instabilities can be viewed as network modes of oscillation that result in no fundamental RF power output. The stability of these modes of oscillation is a requirement for nonspurious, stable combiner performance.

The condition of oscillation for the general combiner network can be written as

$$([Z_c] + [Z_T])\vec{I} = \vec{0} \quad , \qquad (2.3)$$

where $[Z_c]$ and $[Z_T]$ are the circuit impedance matrix and termination matrix, respectively. $\vec{0}$ is the null vector and $\vec{I}$ is a vector of port RF circuits given by

$$\vec{I} = \begin{bmatrix} I_0 \\ I_1 \\ \cdot \\ \cdot \\ \cdot \\ I_N \end{bmatrix} \quad , \qquad (2.4)$$

At this point, it becomes appropriate to examine the load conditions at the combining port of the combiner (zeroth port) to eliminate terms in the network description involving the combining port. The combining port current I_0 can be expressed as

$$I_0 = - \frac{Z_{0p}}{Z_L + Z_{00}} \sum_{k=1}^{N} I_k \quad . \qquad (2.5)$$

With the use of Eq. 2.5 to absorb the combining port impedance terms in $[Z_c]$ and $[Z_T]$, the oscillation condition for odd-mode stability becomes

$$([Z'] + [Z_T'])\vec{I}' = \vec{0}' \quad , \qquad (2.6)$$

where the primed quantities are associated with ports 1 through N and the elements of $[Z']$ are given by

$$Z'_{mn} = Z_{mn} - \frac{Z^2_{0d}}{Z_{00} + Z_L} \quad . \qquad (2.7)$$

The termination matrix is now given by

$$[Z'_T] = \mathrm{diag}\{Z_{d1}(\omega,|I_1|) \;.....\; Z_{dN}(\omega,|I_N|)\} \quad . \qquad (2.8)$$

The symmetry and reciprocity properties of the combiner circuit, which were reflected in the matrix [Z], are retained in [Z']. The nontrivial solutions of Eq. 2.6 represent the modes of oscillation for the combiner network. Some of these oscillation modes (odd modes) will be seen to provide no fundamental frequency RF power at the combining point. Only one oscillation mode (even mode) will contribute to RF power output. The conditions required to suppress the undesired odd modes of oscillation can be determined by examining the circuit conditions associated with solutions to the oscillation condition.

The nontrivial solutions to Eq. 2.6 can be examined as an eigenvalue problem. The eigenvectors $\vec{X}_i$ and the associated eigenvalues λ_i for the circulant circuit matrix [Z'] are obtained from[1,9]

$$[Z']\vec{X}_k = \lambda_k \vec{X}_x \qquad (2.9)$$

and are given by

$$\vec{X}_k = \frac{1}{\sqrt{N}} \begin{bmatrix} 1 \\ e^{jk\alpha} \\ e^{j2k\alpha} \\ \vdots \\ e^{j(N-1)k\alpha} \end{bmatrix} \qquad (2.10)$$

and

$$\lambda_k = \sum_{n=1}^{N} Z'_{mn} e^{jk\alpha(n-1)} \quad , \quad \text{any } m \quad , \tag{2.11}$$

where k = 0 to (N − 1) and $\alpha = 2\pi/N$. An example of the circuit eigenvalues and eigenvectors for a three-device combiner is given in Appendix A.

The zeroth eigenvector $\vec{X}_0$ and its corresponding eigenvalue λ_0 can be associated with the desired even mode. When excited, this mode produces RF current at the combining point with the proper phase so that fundamental RF power may be extracted. The other eigenvectors $\vec{X}_k$ and corresponding eigenvalues λ_k can be associated with the undesired odd modes that result in RF currents at the combining point having destructive phase relationships that prohibit fundamental RF power extraction. The even-mode eigenvalue can be rewritten using Eqs. 2.7 and 2.11 as

$$\lambda_0 = -\frac{N Z_{0d}^2}{Z_{00} + Z_L} + \sum_{n=1}^{N} Z_{mn} \quad , \quad \text{any } m \quad . \tag{2.12}$$

The odd-mode eigenvalue can also be rewritten as

$$\lambda_k = \sum_{n=1}^{N} Z_{mn} e^{jk\alpha(n-1)} \quad , \quad \text{any } m \quad , \tag{2.13}$$

where k = 1 to (N − 1). When Eqs. 2.9 and 2.6 are compared, the oscillation condition becomes

$$-[Z'_T] = \lambda_k [I] \tag{2.14}$$

for $\vec{I}' = \sqrt{N} I_n \vec{X}_k$, where $1 \leq n \leq N$ and [I] is the identity matrix.

Figure 2.2 illustrates an interpretation for a three-diode combiner of the constructive and destructive phase relationship of the RF current at the combining point. Clearly the only desired mode for RF power output is the zeroth mode which corresponds to λ_o and $\vec{X}_o$. All other modes produce no fundamental RF power output.

The combiner eigenvalues have an important interpretation resulting from examination of Eq. 2.14. λ_k is the circuit impedance,[1] and under the assumption that all devices used in the combiner circuit are identical, Eq. 2.14 can be written as

$$- Z_{dn}(j\omega,|I_n|) = - Z_d(j\omega,|I|) = \lambda_k(j\omega) \quad , \qquad (2.15)$$

where $1 \leq n \leq N$. A stable solution to the zeroth mode, which is the fundamental RF power producing mode, would be required for RF power output,

$$- Z_d(\omega,I) = \lambda_o(j\omega) \quad . \qquad (2.16)$$

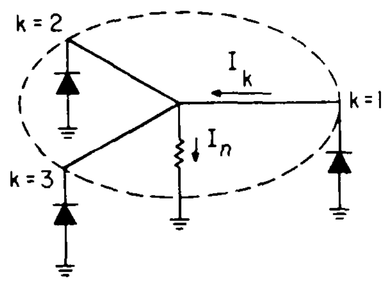
Equation 16 implies that for the even mode to be excited, a circuit impedance of λ_o at a frequency ω and RF current amplitude I would have to be realized. Any solution of the other λ_k gives

$$\sum_{k=1}^{N} I_k = 0$$

in Eq. 2.5, resulting in no RF power output. Therefore, a combiner design, free from odd-mode instabilities requires that the circuit-device interaction

$$- Z_d(j\omega,I) = \lambda_k(j\omega) \quad , \quad k = 1 \text{ to } (N - 1) \qquad (2.17)$$

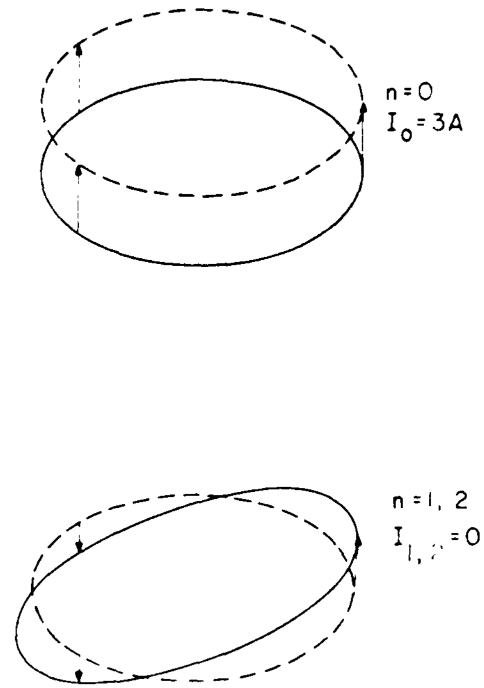
be prevented from occurring.



$$I_n = \sum_{k=1}^{3} I_k$$

$$I_n = A \sum_{k=1}^{3} e^{j2\pi/3kn}$$

$n = 0, 1, 2$



MODES OF OSCILLATION

[illegible]

Because of the inherent nonlinear nature of the devices and the possibility of nonidentical devices, additional modes other than those mentioned here are possible. However, results reported in the literature[1,9,10] have found these modes to be very unlikely because they require highly unusual device-circuit conditions to exist. The use of devices that are nearly identical appear to preclude the possibility of other modes from occurring.[10]

2.3 Lossless TEM Transmission Line Combiners

The general theory of combining networks that employ radial-symmetric circuits will now be applied to lossless combining networks that utilize IMPATT devices in TEM line circuits. Figure 2.[illegible] illustrates the typical features of these combining networks. The network is essentially an array of active IMPATT diodes, arranged symmetrically around a central "hub" or combining point. Each device is connected to the combining point via a section of TEM transmission line, and provides an active termination to that transmission line over a band of frequencies. The lossless nature of these combining networks requires that the system eigenvalues previously mentioned be imaginary (λ_k for k = 1 to (N − 1)), since all the Z_{mn} terms of the circuit matrix are imaginary. Therefore, in the case of the odd modes, all the power supplied into the combiner network is returned. The combining point behaves as a virtual short circuit as far as the combiner is concerned. A stable combiner design is one that can provide suitable terminations to the active devices to prevent any odd modes from occurring.

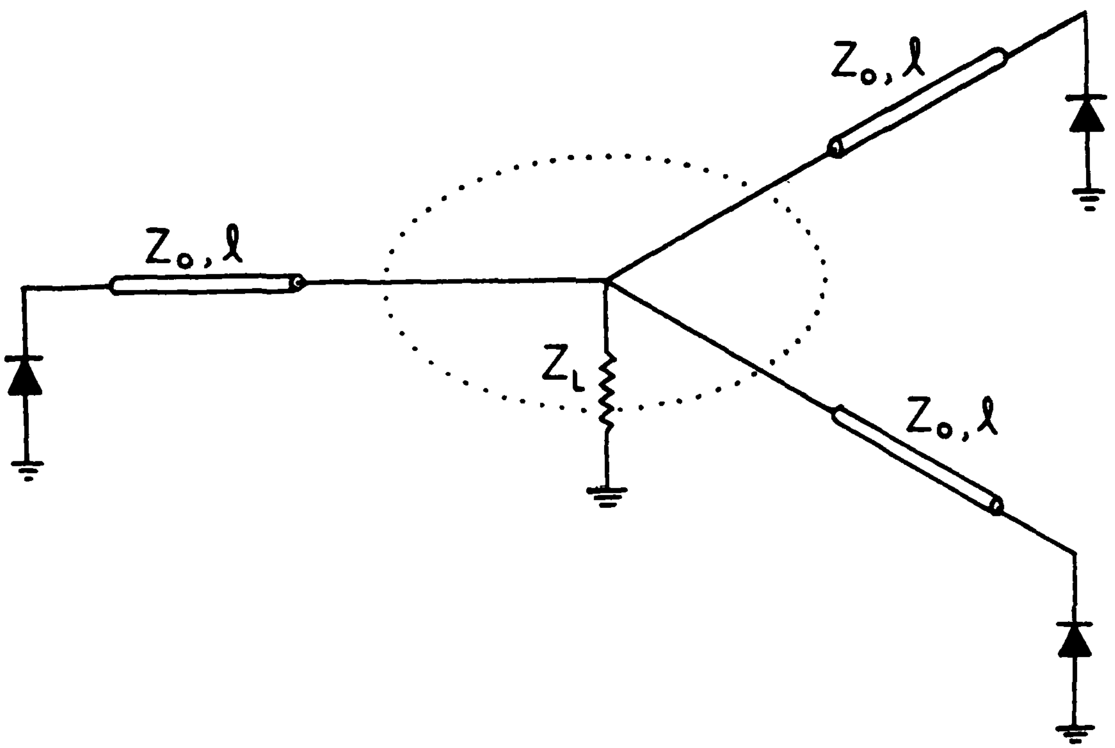


FIG. 2.3 GENERAL RADIAL SYMMETRIC TEM LINE COMBINING STRUCTURE.

A combiner circuit design can be realized by the use of IMPATT devices with dispersionless sections of TEM transmission lines. The bandlimited negative-resistance nature of IMPATT diodes may be used with combining lines of characteristic impedance Z_o and length ℓ to provide a stable design with only even-mode operation.

The combiner network of Fig. 2.3 is assumed to exhibit the symmetry properties of a circulant network; the relationship between port 1 and port 2 is identical to the relationship between port 1 and any other device port. That is, all Z_{1k} (for k = 2 to N) are the same. Furthermore, all Z_{kk} (for k = 1 to N) are also identical due to symmetry. Therefore, the circuit eigenvalues given by[9]

$$\lambda_k = Z_{11} + Z_{12}\, e^{jk(2\pi/N)} + Z_{13}\, e^{jk(2)(2\pi/N)} + \ldots \qquad (2.18)$$

become degenerate and

$$\lambda_1 = \lambda_2 = \lambda_3 = \ldots \lambda_{(N-1)} \quad . \qquad (2.19)$$

With all λ_k (k = 1 to N - 1) being identical, the odd-mode eigenvalues reduce to

$$\lambda_k = jZ_o \tan \beta\ell \qquad (2.20)$$

for k = 1 to (N - 1) and where $\beta = 2\pi/\lambda$ is the propagation coefficient and ℓ is the length of a transmission line. The eigenvalue associated with the even mode is given by

$$\lambda_o = Z_o \frac{NZ_L + jZ_o \tan \beta\ell}{Z_o + jNZ_L \tan \beta\ell} \quad , \qquad (2.21)$$

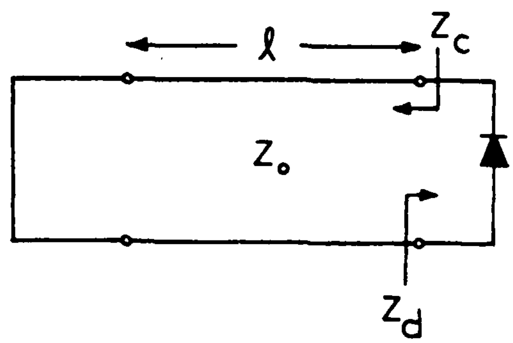
where Z_o is the characteristic impedance of each combining TEM transmission line and Z_L is the load impedance at the combining port. Straightforward equivalent circuits can be associated with the even- and odd-mode circuit eigenvalues. λ_o represents the input impedance of a section of dispersionless TEM transmission line of length ℓ and characteristic impedance Z_o terminated in an effective load impedance of NZ_L (N = total number of devices combined). The odd-mode eigenvalue, λ_k (k = 1 to N - 1), represents a section of TEM line terminated in a short circuit.

The odd- and even-mode equivalent circuits shown in Fig. 2.4 specify the circuit conditions required to control the particular circuit interactions. Clearly for a stable combiner design the odd-mode equivalent circuit situation must be prevented from occurring. A combiner design that provides odd-mode stability requires that there be no stable solution to the oscillation condition,

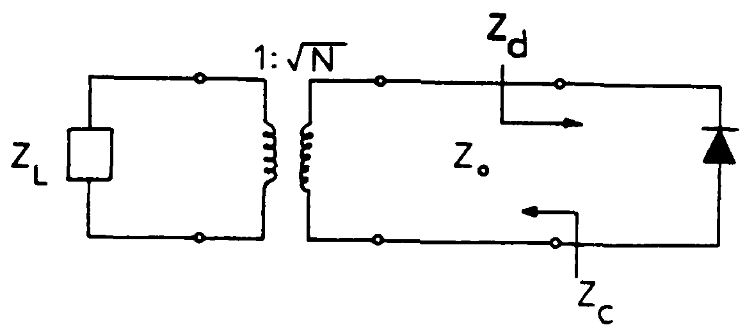
$$Z_d(j\omega,I) + jZ_o \tan \beta\ell = 0 \qquad (2.22)$$

for a given frequency ω and RF current amplitude I. This constraint can be met by the use of identical IMPATT devices having a band-limited negative resistance. Solutions to Eq. 2.22 need only be considered over a limited band of frequencies.

A typical admittance plane plot of an IMPATT device is shown in Fig. 2.5. The bandlimited active region is clearly evident. At small signal, the diode becomes active near the diode "avalanche" frequency, reaches a maximum negative conductance, and becomes passive again at some frequency determined by the device carrier transit time. Large-signal contours and constant-frequency contours



ODD MODE EQUIVALENT CIRCUIT



EVEN MODE EQUIVALENT CIRCUIT

FIG. 2.4 ODD- AND EVEN-MODE EQUIVALENT CIRCUITS ASSOCIATED WITH THE NORMAL MODES OF OSCILLATION FOR THE COMBINER SYSTEM.

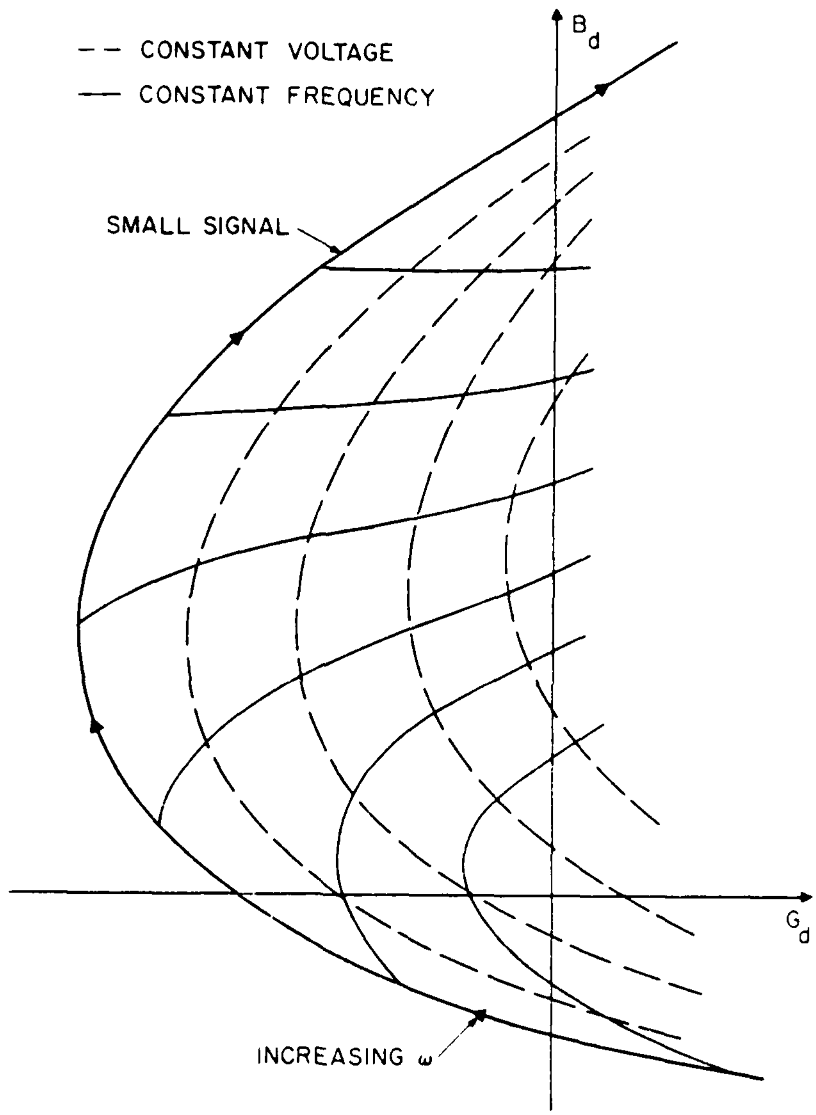


FIG. 2.5 A TYPICAL ADMITTANCE PLANE PLOT OF THE NONLINEAR PROPERTIES OF AN IMPATT DIODE.

are also indicated. An important subtlety of Fig. 2.5 is that at lower frequencies a passive device admittance at small-signal levels can become active for certain drive levels and frequencies. This point must be kept in mind in choosing an appropriate combiner circuit (TEM combining line length and characteristic impedance) to avoid solutions to Eq. 2.22.

Solutions of Eq. 2.22 can be rewritten as

$$R_d(j\omega, I) = 0 \tag{2.23a}$$

and

$$X_d(j\omega, I) = -Z_o \tan \beta\ell \quad . \tag{2.23b}$$

For an undesired device-circuit interaction to occur, Eq. 2.23b must be satisfied when $R_d(j\omega, I) = 0$ for a particular frequency and RF current amplitude.

2.4 Circuit Constraints for Combiner Stability

The combiner circuit design for only even-mode operation is more easily specified if the negative diode impedance and the circuit impedance for the odd-mode equivalent circuit are plotted on the same Smith chart as illustrated in Fig. 2.6. In this figure, the device curve (negative of the diode impedance) is plotted for a typical IMPATT diode in the inverted reflection coefficient plane (impedances associated with active devices are plotted inside the Smith chart and those impedances corresponding to passive devices are plotted outside the chart). Examination of Fig. 2.6 indicates that the diode becomes active at a frequency ω_c near the diode avalanche frequency, passes through a point of maximum reflection gain, and becomes passive again at the frequency ω_m. The circuit

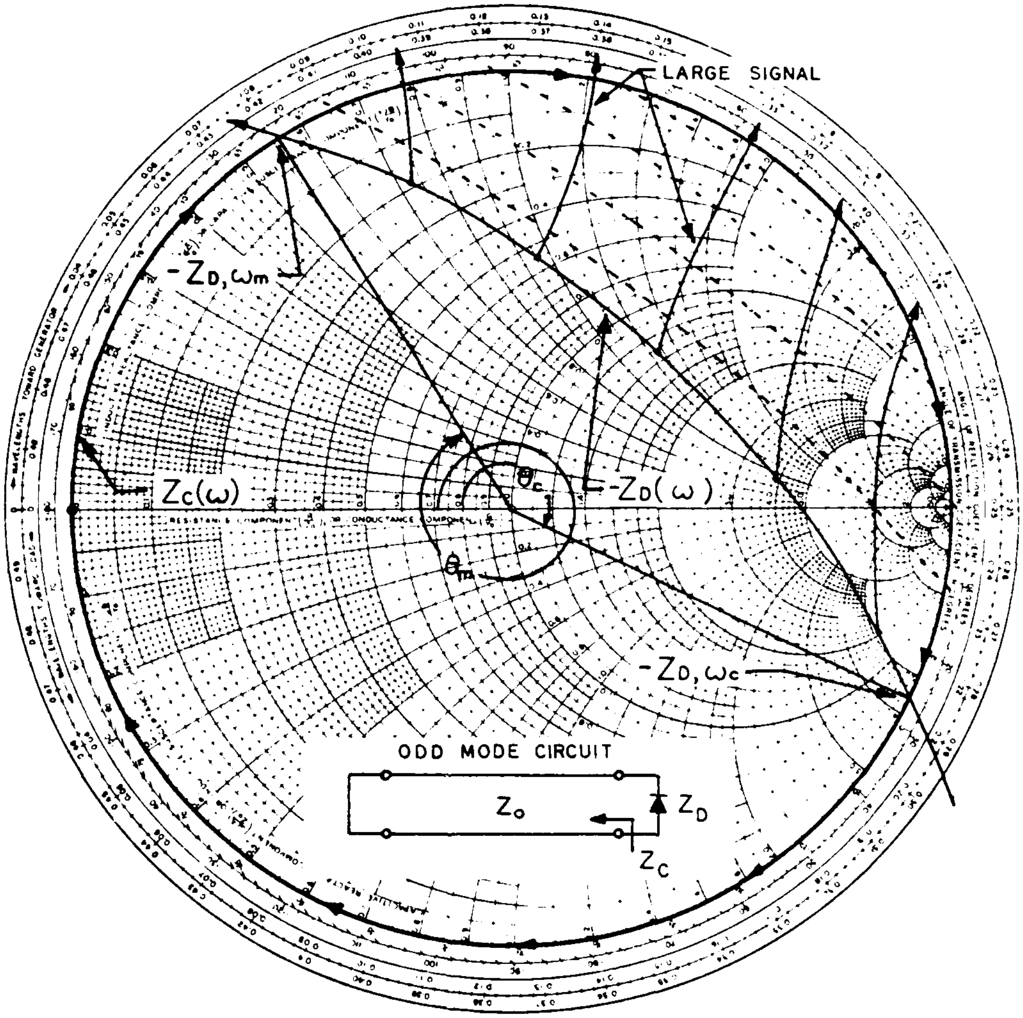


FIG. 2.6 SMITH CHART VISUA[illegible] [illegible] THE [illegible]-M[illegible] [illegible]
CRITERIA. THE ANGLES θ_m AND θ_c [illegible]
STRAINTS [illegible] [illegible]-M[illegible].

curve Z_c represents impedance vs. frequency of the odd-mode equivalent circuit (impedance of a short-circuited section of dispersionless TEM transmission line). In order for the combiner to provide odd-mode stability over the active bandwidth of the IMPATT device, a circuit design must be selected such that no intersection will occur between the circuit curve and the device curve (small- and large-signal) at a given frequency and RF amplitude. While the device is active this graphical constraint has the interpretation of avoiding the oscillation condition of Eq. 2.5.

The choice of circuit that provides combiner odd-mode stability is constrained by

$$- X_d(\omega_c) \geqq Z_o \tan \beta\ell \qquad (2.24a)$$

and

$$- X_d(\omega_m) \geqq Z_o \tan \beta\ell \quad , \qquad (2.24b)$$

where $X_d(\omega)$ is the reactive portion of the diode impedance when the real part of the diode impedance $R_d(\omega)$ is identically zero; and Z_o and ℓ are the characteristic impedance and line length of the lossless TEM combining transmission line, respectively. β is the wave propagation constant.

The requirement for combiner stability, indicated by Eq. 2.24, can best be presented if angles are associated with impedances on the Smith chart of Fig. 2.6. For odd-mode stability, the circuit appears as a short-circuited length of TEM transmission line. On a Smith chart, this translates to an impedance vs. frequency contour which begins at $Z = 0$ and proceeds along the outside perimeter of the Smith chart in a clockwise fashion, where the angle of the circuit normalized impedance $\theta(\omega) = 2\beta\ell$ is referenced as indicated in Fig. 2.6. Stability, therefore, can be achieved under the conditions

$$\theta(\omega_c) \doteq \arg(-\overline{X}_c) \tag{2.25a}$$

and

$$\theta(\omega_m) \doteq \arg(-\overline{X}_m) \quad , \tag{2.25b}$$

where $\overline{X}_c$ and $\overline{X}_m$ are the normalized diode reactances at ω_c and ω_m, respectively, under the condition that $R_d(\omega) = 0$; and they are defined as

$$\overline{X}_c = \overline{X}_d(\omega_c) = \frac{X_d(\omega_c)}{Z_o} \tag{2.26}$$

and

$$\overline{X}_m = \overline{X}_d(\omega_m) = \frac{X_d(\omega_m)}{Z_o} \quad . \tag{2.27}$$

The terms $\arg\{-\overline{X}(\omega_c)\}$ and $\arg\{-\overline{X}(\omega_m)\}$ are ambiguous as given. An appropriate reference to the angle $\theta(\omega)$ as shown in Fig. 2.6 is required. With the proper referencing, the conditions for combiner stability become

$$\theta(\omega_c) \doteq \pi - 2\tan^{-1}\left\{-\frac{1}{\overline{X}_d(\omega_c)}\right\} \tag{2.28a}$$

and

$$\theta(\omega_m) \doteq 2\pi + 2\tan^{-1}\{-\overline{X}_d(\omega_m)\} \quad , \tag{2.28b}$$

where $\tan^{-1}$ is given by its principle value which lies in the first or fourth quadrant. Other solutions to Eq. 2.24 are possible.[10] However, those solutions require longer TEM combining line lengths which in reality are often impractical.

The stability constraints of Eq. 2.28 specify the selection of the combiner circuit. The TEM combining line length ℓ determines the impedance angles $\theta(\omega_c)$ and $\theta(\omega_m)$. The selected normalization impedance Z_o scales the values of $\overline{X}_d(\omega_c)$ and $\overline{X}_d(\omega_m)$. The combination of line length and normalization impedance (characteristic impedance of combining line) that satisfies Eq. 2.28 suppresses circuit-device interactions that result in odd-mode instabilities. Diodes must, however, have $\omega_m/\omega_c \cong 2$ to satisfy the stability criteria[1] of Eq. 2.28.

The greatest flexibility for a stable combiner design is obtained by using the variables

$$\rho = \frac{X_d(\omega_c)}{X_d(\omega_m)} \tag{2.29}$$

and

$$\alpha = \frac{\omega_m}{\omega_c} \quad . \tag{2.30}$$

To manipulate the stability constraints of Eq. 2.28 to

$$\theta(\omega_c) \gtrapprox \pi - 2 \tan^{-1} \left[- \frac{1}{\rho\overline{X}_d(\omega_m)}\right] \tag{2.31}$$

and

$$\alpha \tan^{-1} \left[\frac{1}{\rho\overline{X}_d(\omega_m)}\right] + \tan^{-1} [\overline{X}_d(\omega_m)] + \frac{\pi}{2} (\alpha - 2) \lessapprox 0 \quad , \tag{2.32}$$

dispersionless lines are assumed and $\theta(\omega_m) = \alpha\theta(\omega_c)$. Equations 2.31 and 2.32 provide the criteria for choosing the combiner circuit. For a device with a given α and ρ, the equality in Eq. 2.32 can be used to find a maximum value of $\overline{X}_m$ from which a value of normalization impedance or characteristic impedance $Z_o = |Z_d(\omega_m)|/|\bar{X}_d(\omega_m)|$ can be determined. The inequality in Eq. 2.31 then determines the angle $\theta(\omega_c) = 2\beta(\omega_c)\ell$ from which the appropriate TEM combining line length ℓ is found. Generally, considerable flexibility in combiner circuit design can be obtained with devices having $\omega_m/\omega_c < 2$ because of the usually large stability margin provided by such devices.

2.5 Even-Mode Design Considerations

The constraints placed on the TEM combining line length and characteristic impedance specify a design providing odd-mode stability. It is useful, however, to consider the combiner as an even-mode oscillator or amplifier. The combiner circuit utilizes identical devices arranged in a radial-symmetric configuration around a central combining point. In view of this fact, each diode impedance is presented at the combining point through a length of TEM transmission line. This rotated impedance appears in parallel with $N - 1$ other identical diode impedances, which have also been rotated through similar TEM combining lines. Practical considerations should be given to obtaining a reasonable total impedance value at the combining point. Moreover, a desirable situation would be to obtain an impedance that is real (reactance equal to zero) at the design frequency and still fall within the odd-mode stability constraints. The nature of IMPATT impedances and the TEM line lengths required for odd-mode stability can often allow the real impedance condition to be achieved making the realization of a desired load impedance straightforward.

The even-mode equivalent circuit was shown in Fig. 2.4b and reflects the properties of an impedance transformer. Therefore, to achieve realistic load impedances at the combining point consideration must be given to the number of devices being combined (aside from physical congestion limitations). It is desirable to have the optimum power impedance point rotate through the TEM combining line to a real value, facilitating the design of the combiner as an amplifier or oscillator.

The choice of combining line length ℓ and characteristic impedance Z_o to give a real axis mapping and still provide odd-mode stability can often be achieved for devices with $\omega_m/\omega_c < 2$. An example will be presented to illustrate the technique. Figure 2.7 shows the impedance characteristics of an X-band IMPATT device experimentally determined.[10] The diode was biased at a current of 150 mA with a voltage of approximately 66 V. The optimum power normalized impedance occurs at frequency ω_o = 9.6 GHz and is given as

$$- \overline{Z}_{od} = \frac{- R_{do} - jX_{do}}{Z_o} = 0.02 + j0.47 \text{ [illegible]} \quad . \qquad \text{(2.[illegible])}$$

In order to rotate $- \overline{Z}_{do}$ to a real axis value (with a normalized impedance greater than unity) at the combining point, $- \overline{Z}_{do}$ must map through an angle $\theta_o = 2\beta(\omega_o)\ell = 4.014$ rad. This angle corresponds to a TEM line length equivalent to ℓ = [illegible] λ_o as read from the Smith chart, where λ_o is the wavelength at frequency ω_o. The question that must now be considered is if this particular value of TEM line length satisfies the stability constraint of Eq. 2.28a. This may be checked graphically by using

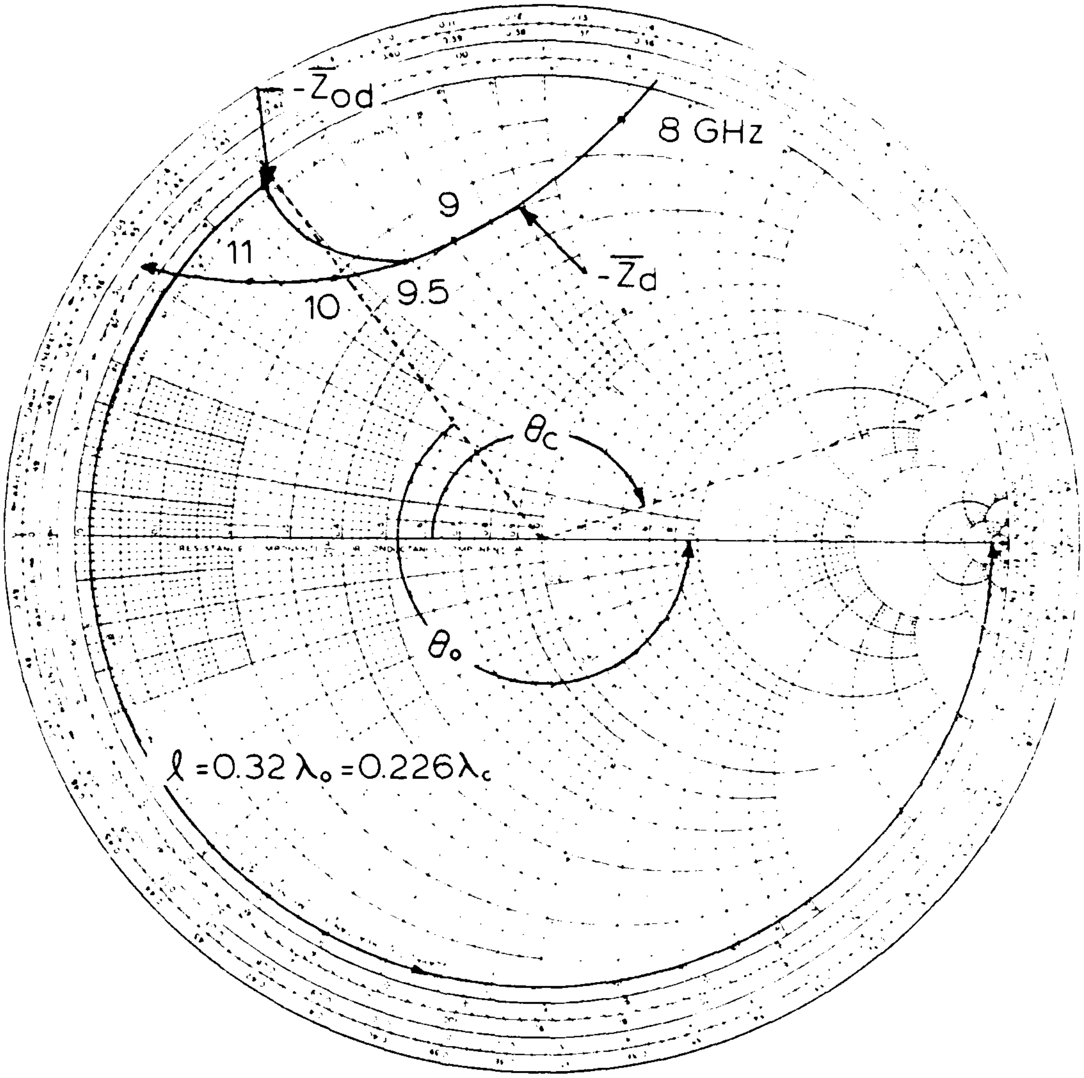


FIG. 2.7 EXPERIMENTALLY DETERMINED DEVICE CURVE ILLUSTRATING A GRAPHICAL TECHNIQUE FOR REALIZING A REAL IMPEDANCE AT THE COMBINING POINT.

$$\lambda_o = \frac{f_c}{f_o} \lambda_c \quad , \tag{2.34}$$

which assumes dispersionless lines. The TEM combining line length can now be expressed as $\ell = 0.226\ \lambda_c$, where $f_c = 6.7$ GHz has been assumed. The angle $\theta_c = 2\beta(\omega_o)\ell = 2.84$ rad and referenced as shown clearly satisfies Eq. 2.28a for odd-mode stability. In this example, a normalization impedance of $Z_o = 35\ \Omega$ was chosen. The large stability margin supplied by this IMPATT device provides both odd-mode stability and a real axis map for the optimum power impedance.

CHAPTER III

DEVICE CHARACTERIZATION AND COMBINER REALIZATION

The selection of IMPATT devices with appropriate negative-resistance characteristics is paramount for the realization of a stable lossless TEM line combiner. Candidate diodes must exhibit certain measured characteristics: (1) the devices must have a limited phase variation over their active bandwidths, otherwise odd-mode combiner instabilities can result; (2) the devices must have suitable impedance levels with respect to the embedding circuit, which insures adequate reflection gain for diode measurement; and (3) the devices must be nearly identical in their active region.

The device characteristics, as measured, depend largely on the test circuit in which the diode is measured. Therefore, a device may require testing in various circuits to determine the most desirable circuit to transform the device properties. In this investigation candidate IMPATT devices were characterized in various microstrip test fixtures to satisfy the required measured characteristics mentioned above. In this way not only were suitable combiner devices selected, but the combiner circuit characteristics were established.

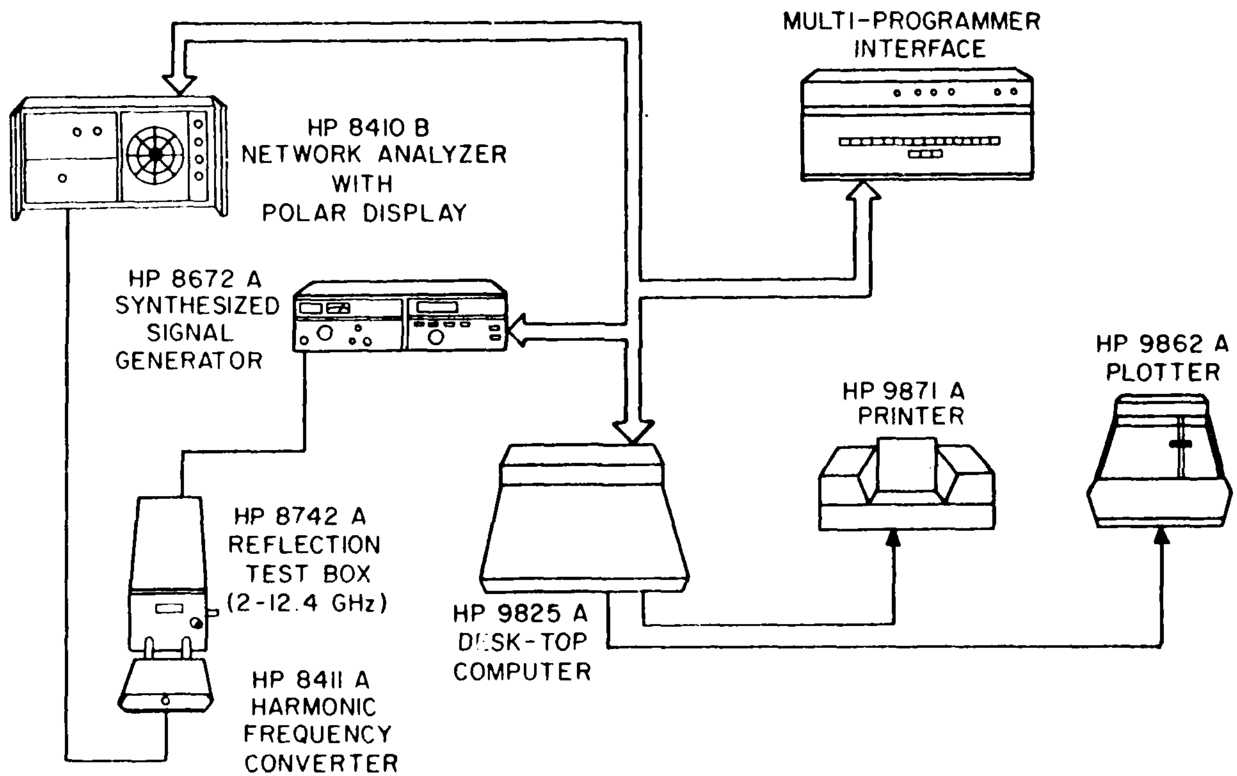
In this chapter the various test circuits used to select appropriate devices and determine a suitable combiner circuit are presented. The measurement of device characteristics, including the measurement test set and characterization procedure is discussed and the results presented.

The devices available for use in this study were Si double-drift IMPATT diodes manufactured by Hewlett-Packard.[11] Originally designed as pulsed power sources at X-band and Ku-band, these packaged devices were operated in a CW mode at lower current levels in this investigation. The goal here was not to obtain high power levels but to demonstrate the combining technique. A summary of the typical diode parameters of the devices used in this study is given in Appendix C.

3.1 Basic Experiment Test Set and Measurement Technique

A semi-automated microwave measurement system shown in Fig. 3.1 was used to measure and process impedance data obtained from various devices and networks in order to determine and realize a suitable combiner design. The measurement system is comprised of a microwave network analyzer, a synthesized signal generator, and a reflection test box, all of which are interconnected through a system multiprogrammer interface and interface computer bus (HP-IB). A Hewlett-Packard 9825-A desktop computer, with its support software, functioned as the measurement system controller providing communication and data transfer from the measurement hardward to the computer memory and to output peripherals. This system is designed to provide a fast and accurate method to collect, process, and present measured impedance data from a device/network under test.

An extensive collection of measurement software previously written in HPL (Hewlett-Packard Language) has been developed for this measurement system for control of the various hardware


MULTI-PROGRAMMER
INTERFACE
HP 8410 B
NETWORK ANALYZER
WITH
POLAR DISPLAY
HP 8672 A
SYNTHESIZED
SIGNAL
GENERATOR
HP 9871 A
PRINTER
HP 9862 A
PLOTTER
HP 8742 A
REFLECTION
TEST BOX
(2-12.4 GHz)
HP 9825 A
DESK-TOP
COMPUTER
HP 8411 A
HARMONIC
FREQUENCY
CONVERTER

components. In addition, the software provides the necessary data processing to correct errors in the measured data caused by an imperfect test set. Once a measurement is completed and the data corrected, various output formats can be selected to present the results. Typically, and the method most frequently used in this study, Smith chart plots of normalized impedance vs. frequency of active device/networks are used.

The complete measurement system of Fig. 3.1 is almost totally automated. The operator is required to initialize frequency limits and stepsize, and to manually change standard load terminations during a system calibration procedure. The system then responds by making calibrated, swept frequency measurements of the reflection coefficients for a device under test. The system software uses the standard one-port reflection measurement error model shown in Fig. 3.2 in calibrating the test set and provides error corrected data. An abbreviated flowchart of the one-port measurement and calibration procedure is shown in Fig. 3.3. The operation and hardware integration of the semi-automated microwave measurement system are well known and documented in the references.[12-17] The reader is referred to those references for a more in-depth discussion of the system and its limitations.

3.1.1 Measurement Reference Plane. The error-corrected reflection coefficient data obtained from the device/network under test is usually referenced to a specified measurement plane of the measurement test set. This reference plane is initially established at the test port of the reflection test box as indicated in Fig. 3.4. The impedance measured at this plane, Z_m, is in general not

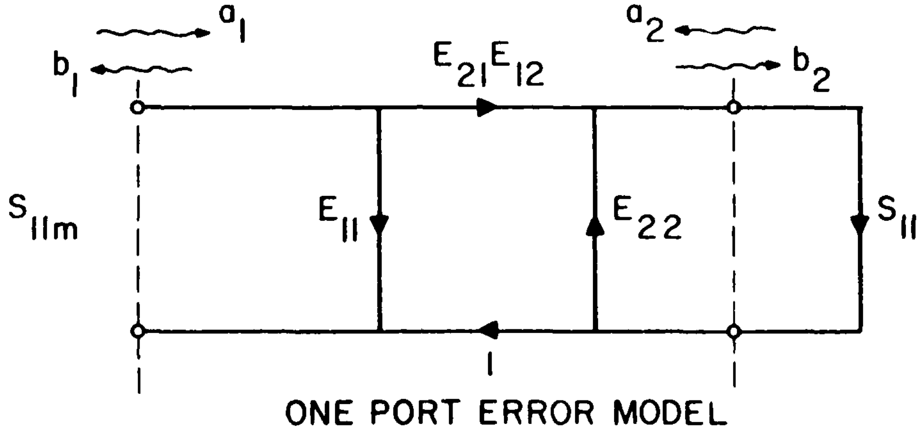


FIG. 3.2 ONE PORT ERROR MODEL USED IN THE REFLECTION COEFFICIENT MEASUREMENT ERROR-CORRECTING ROUTINE.

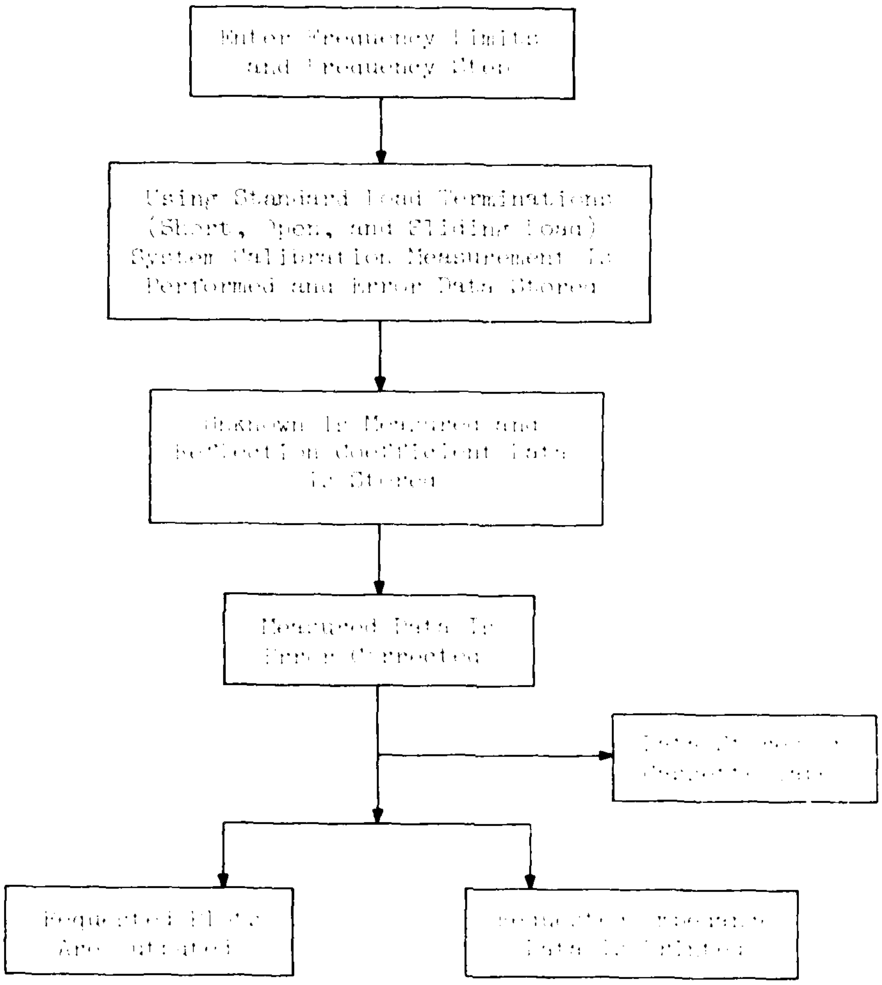
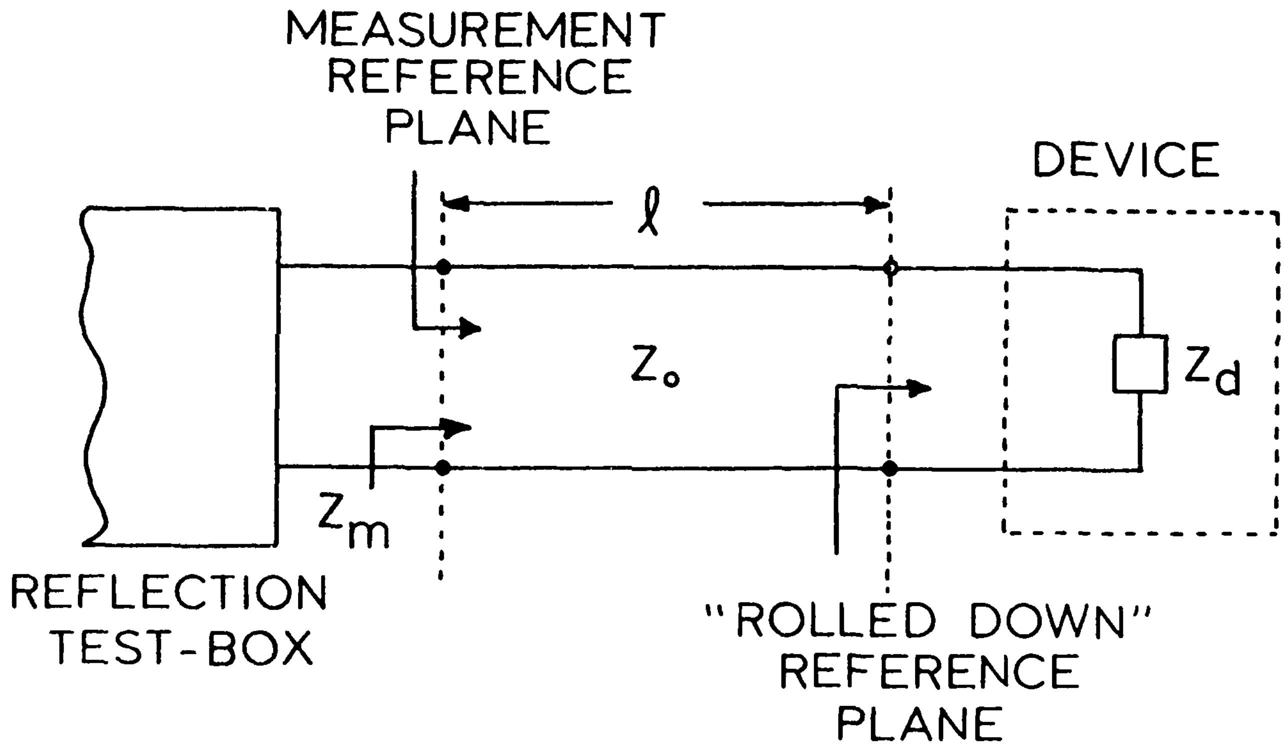


FIG. 3.3 FLOW CHART OF THE ONE-PORT REFLECTION COEFFICIENT MEASUREMENT PROGRAM USED WITH THE SEMI-AUTOMATED MICROWAVE SYSTEM.


MEASUREMENT
REFERENCE
PLANE
DEVICE
ℓ
Z_o
Z_d
Z_m
REFLECTION
TEST-BOX
"ROLLED DOWN"
REFERENCE
PLANE

the desired impedance of the device/network under test since it is rotated through a section of transmission line (characteristic impedance Z_o and length ℓ) connecting the measurement port with the combiner output port. The more useful impedance Z_d must be determined by either physically adding line length to the measurement port (i.e., line stretcher in the reflection test box) or by mathematically "rolling down" the reference plane using the expression

$$Z_d = Z_o \frac{Z_m - jZ_o \tan \beta\ell}{Z_o - jZ_m \tan \beta\ell} , \qquad (3.1)$$

which rotates Z_m to Z_d as shown in Fig. 3.4. In this investigation the mathematical approach was used. Length ℓ of the connecting TEM line is determined by replacing Z_d with a short-circuit termination and measuring this load over the desired measurement frequency band. The TEM line length is selected for use in Fig. 3.1 to position the error-corrected "rolled down" impedance [illegible] short-circuit impedance point on the Smith chart as shown [illegible]. [illegible] choice of ℓ that minimizes the spread [illegible] on the chart over the measurement frequency [illegible] line length. This establishes the [illegible] device/network terminals.

3.1.2 Note on Large-Signal [illegible]

measurements were necessary [illegible] of Fig. 3.1 was modified to [illegible] power meter. An available [illegible] synthesized signal generator [illegible] indicated [illegible] software control of frequency and input [illegible].

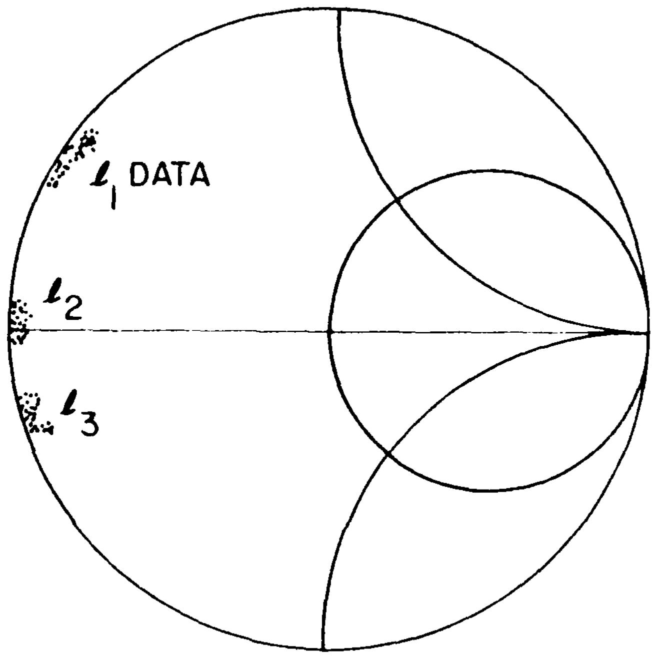


FIG. 3.6 SMITH CHART PLOT OF IMPEDANCE DATA OBTAINED FROM A SHORT CIRCUIT TERMINATION AT THE DEVICE TERMINALS. DATA CORRESPONDING TO ℓ_2 IS CLOSEST TO REPRESENTING A SHORT CIRCUIT IN THE MEASUREMENT FREQUENCY BANDWIDTH AND ESTABLISHES THE LENGTH FROM THE CALIBRATED MEASUREMENT REFERENCE PLANE TO THE DEVICE TERMINALS.

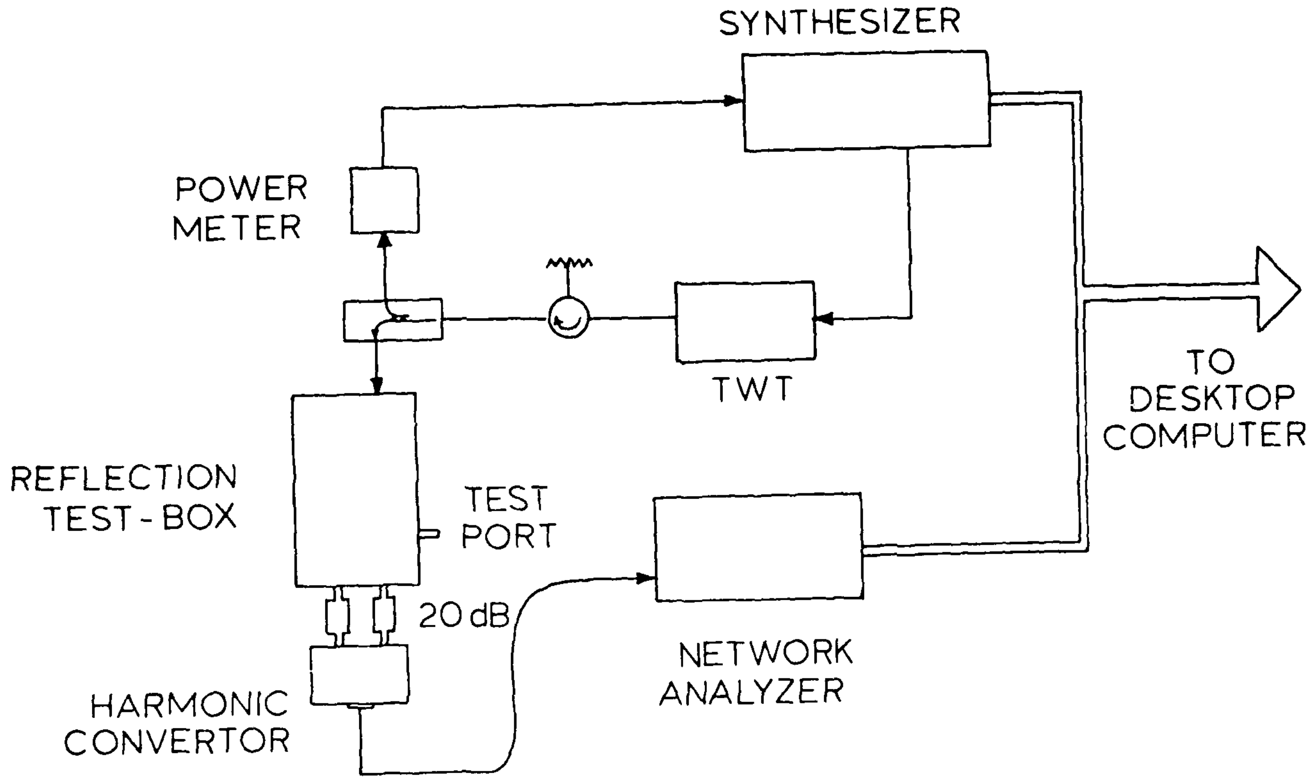


FIG. 3.[illegible] [illegible] AUTOMATED TEST SET.

3.2 Microstrip Experimental Combiner

3.2.1 Single-Device Test Circuits and Characterization Results.

Candidate combiner devices were initially characterized in the 50-Ω microstrip test circuit shown in Fig. 3.7. A section of 50-Ω micro-strip line was fabricated on 0.025 in. alumina substrate, which in turn was epoxied onto a gold-plated, brass test fixture assembly. Gold wire (0.0007 in diameter) was thermocompression bonded from the device to one end of the 50-Ω microstrip top conductor. An RF connector was connected to the other end. DC bias was provided with a bias tee included in the measurement test set. This circuit did not provide correct impedance levels to the diode. Some form of impedance matching network would be required.

The correct impedance level was determined by using an available IMPATT diode coaxial test circuit. This test circuit had an interchangeable two-section quarter-wavelength transformer which was useful in optimizing the circuit impedance level. Suitable negative-resistance levels were obtained with a transformer that transformed 50 Ω to approximately 6 Ω. Figure 3.8 illustrates typical reflection gains measured as a function of frequency for different bias currents.

The electrical equivalent of the coaxial test circuit is shown in Fig. 3.9. Although useful in establishing impedance levels in microstrip, the electrical length of the two-section transformer is prohibitive for a combiner design. The large phase variation associated with the coaxial-circuit transformer would likely lead to device-circuit instabilities. Consequently, a single-section impedance transformer designed to operate near the frequency of

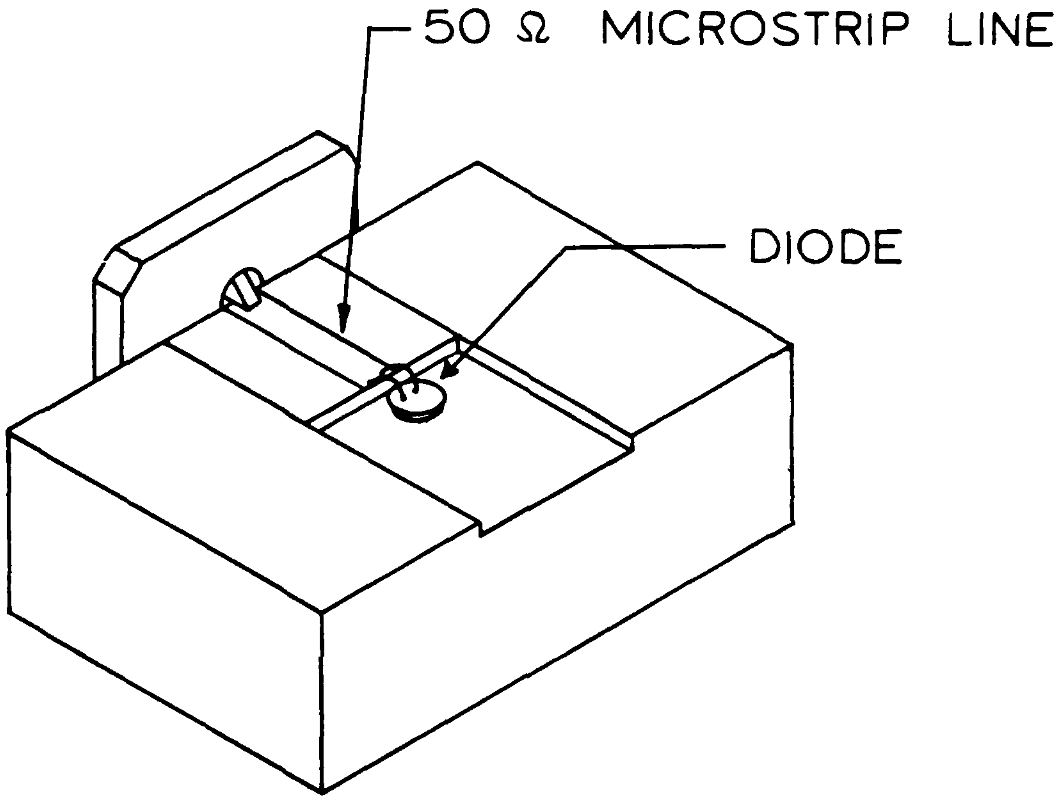


FIG. 3.7 FIRST GENERATION MICROSTRIP 50-Ω TEST CIRCUIT.

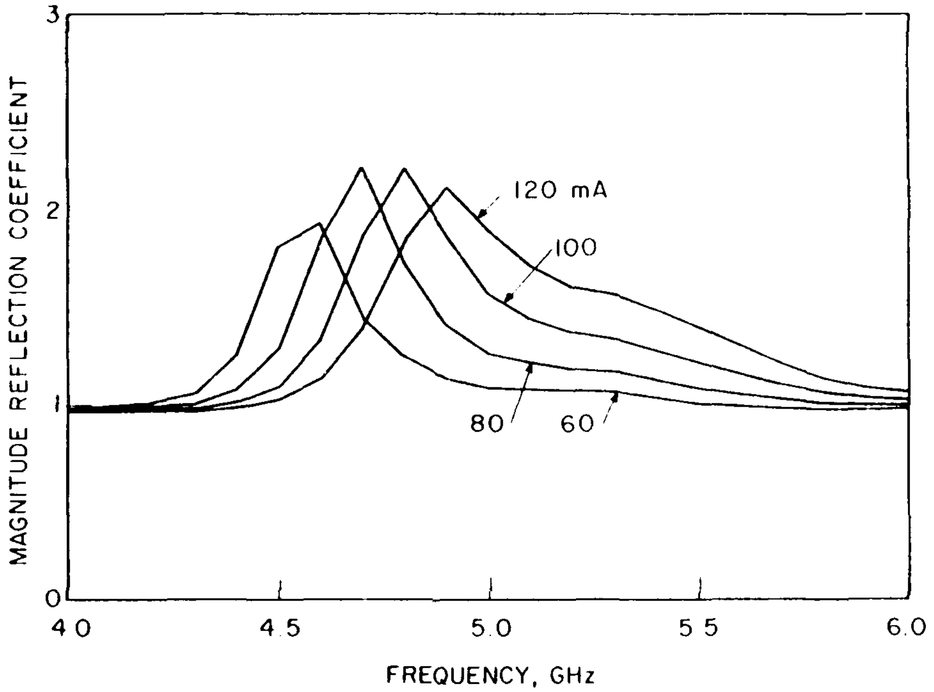


FIG. 3.8 REFLECTION COEFFICIENT OF A DEVICE MEASURED IN A COAXIAL TEST FIXTURE USING A 6- TO 50-Ω IMPEDANCE TRANSFORMER.

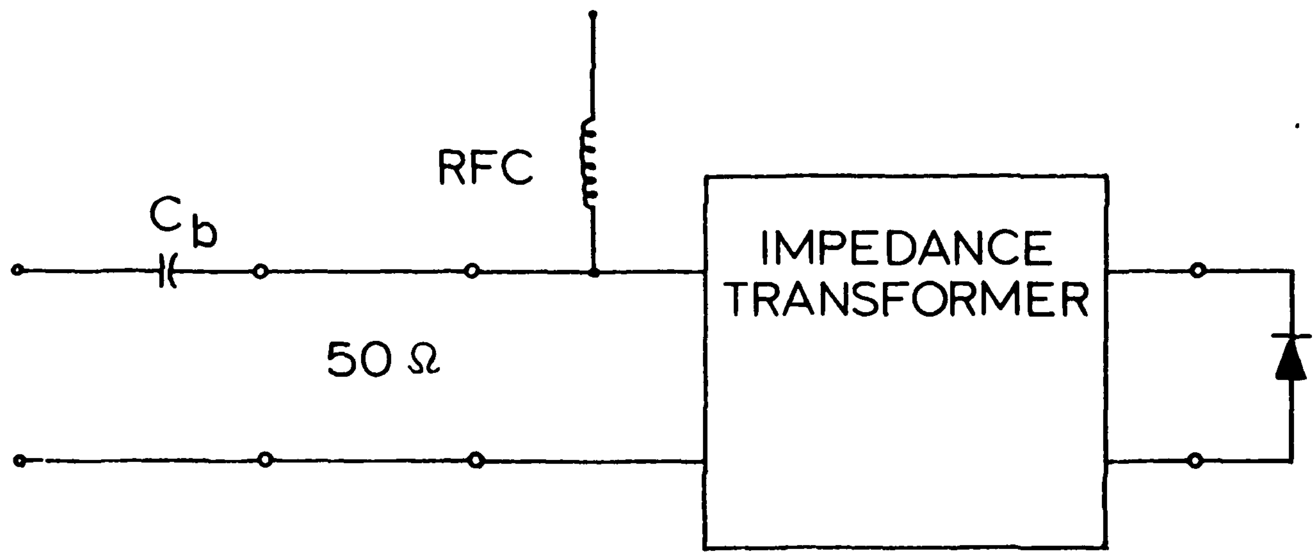


FIG. 3.9 ELECTRICAL EQUIVALENT OF A COAXIAL TEST CIRCUIT USEFUL FOR ESTABLISHING IMPEDANCE LEVEL ON MICROSTRIP.

peak small-signal gain in Fig. 3.8 was incorporated into the modified microstrip circuit board shown in Fig. 3.10.

The circuit board of Fig. 3.10 differs from the previous microstrip test circuit by the inclusion of a section of 18-Ω transmission line which improves the matching of the 50-Ω circuit to the device. No attempt was made to optimize the negative-resistance level or bandwidth. Only a suitable active device region was of concern. As described in the measurement test set section of this report, impedance data is referenced to a prescribed plane on the test circuit. The position of such a reference location is established using a short circuit at the plane of interest. In the case of the circuit board of Fig. 3.10, a 50-Ω section of microstrip line identical in length to that of Fig. 3.10a was fabricated and epoxied onto a similar test fixture. The end of this 50-Ω line was then bonded to the gold-plated assembly fixture with a minimum length of wire. This established a reasonable short circuit at the measurement plane. This technique works well with lines that are of the same width. Abrupt changes in the characteristic impedance of microstrip lines introduce significant capacitive discontinuities to prevent such a procedure from being used. For this reason, the measured impedance data was referenced to the terminals of the impedance transformer and not the IMPATT device. A combiner design is nevertheless still possible at this reference plane.

Figure 3.11 illustates the measured reflection coefficient data of a typical combiner device as measured in the microstrip test circuit of Fig. 3.10. The data is plotted as a function of frequency for different bias currents. The impedance transforming network has

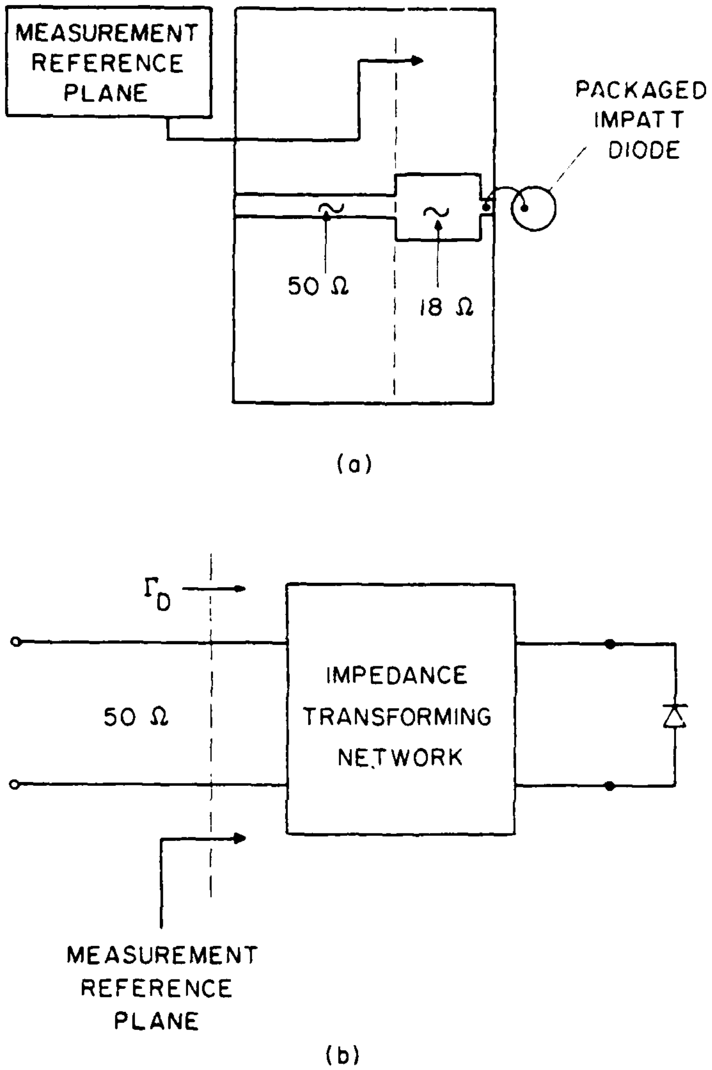


FIG. 3.10 (a) MICROSTRIP CIRCUIT FIXTURE FOR DEVICE CHARACTERIZATION AND (b) CIRCUIT EQUIVALENT OF DEVICE CHARACTERIZATION FIXTURE.

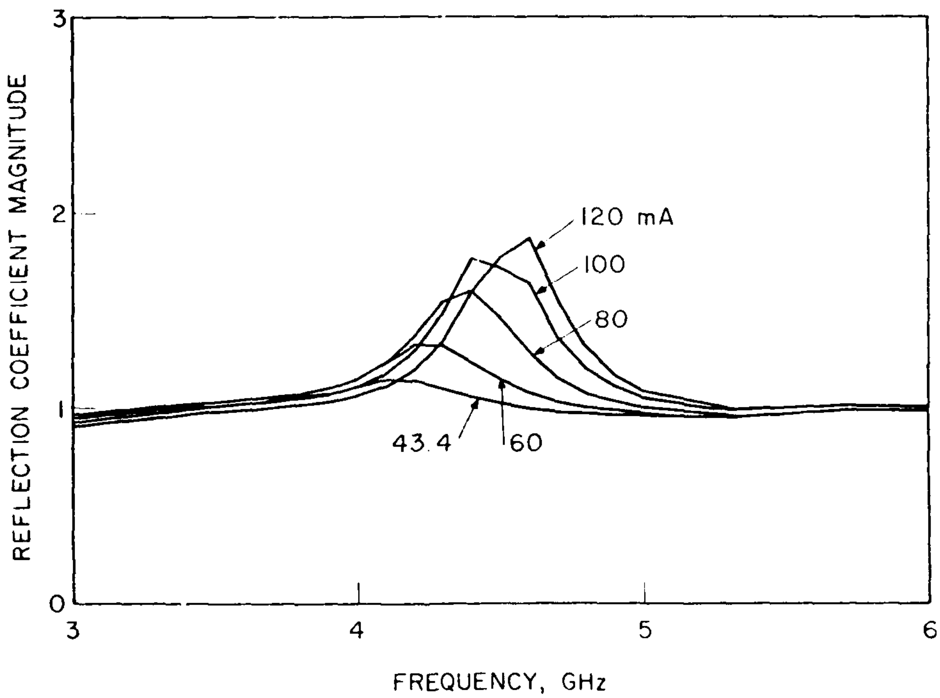


FIG. 3.11 REFLECTION COEFFICIENT MAGNITUDE OF A DEVICE MEASURED IN THE MICROSTRIP TEST CIRCUIT OF FIG. 3.1[illegible].

provided an improved match from the 50-Ω circuit impedance to the IMPATT impedance. This then provided a suitable level of measured reflection gain. No attempt was made to further optimize the impedance match since the goal was to achieve impedance levels suitable for the combiner design. High levels of reflection gain were not required.

A plot of the negative device impedance as measured at the reference plane shown in Fig. 3.10b and normalized to 50 Ω is illustrated on the Smith chart of Fig. 3.12. The impedances associated with the active device are mapped inside the chart. The data shown is for current bias levels of 100 and 120 mA. Although there is a large amount of phase variation over the device active bandwidth, there is enough stability margin for a stable combiner design. For these characteristics, the circuit impedance for odd-mode stability must lie inside the diode impedance locus as shown. This can be achieved with a short length of 50-Ω line from the combining point.

One drawback of the test circuit is that it does not supply bias to the IMPATT device. The final combiner design will require bias circuits for each device as a bias tee cannot be used. A biasing circuit on the fixture assembly must be included before using the test circuit to select the most identical IMPATT devices. As indicated in Fig. 3.13, diodes 21, 22 and 36 appear very similar and two were selected for use in the combiner.

A microstrip test circuit with a bias circuit incorporated onto the fixture assembly was developed and is shown in Fig. 3.14. The bias circuit consists of a length of 0.001 in diameter gold wire, one-quarter wavelength long at the frequency of interest, which is wound around a glass post, forming an RF choke (RFC).

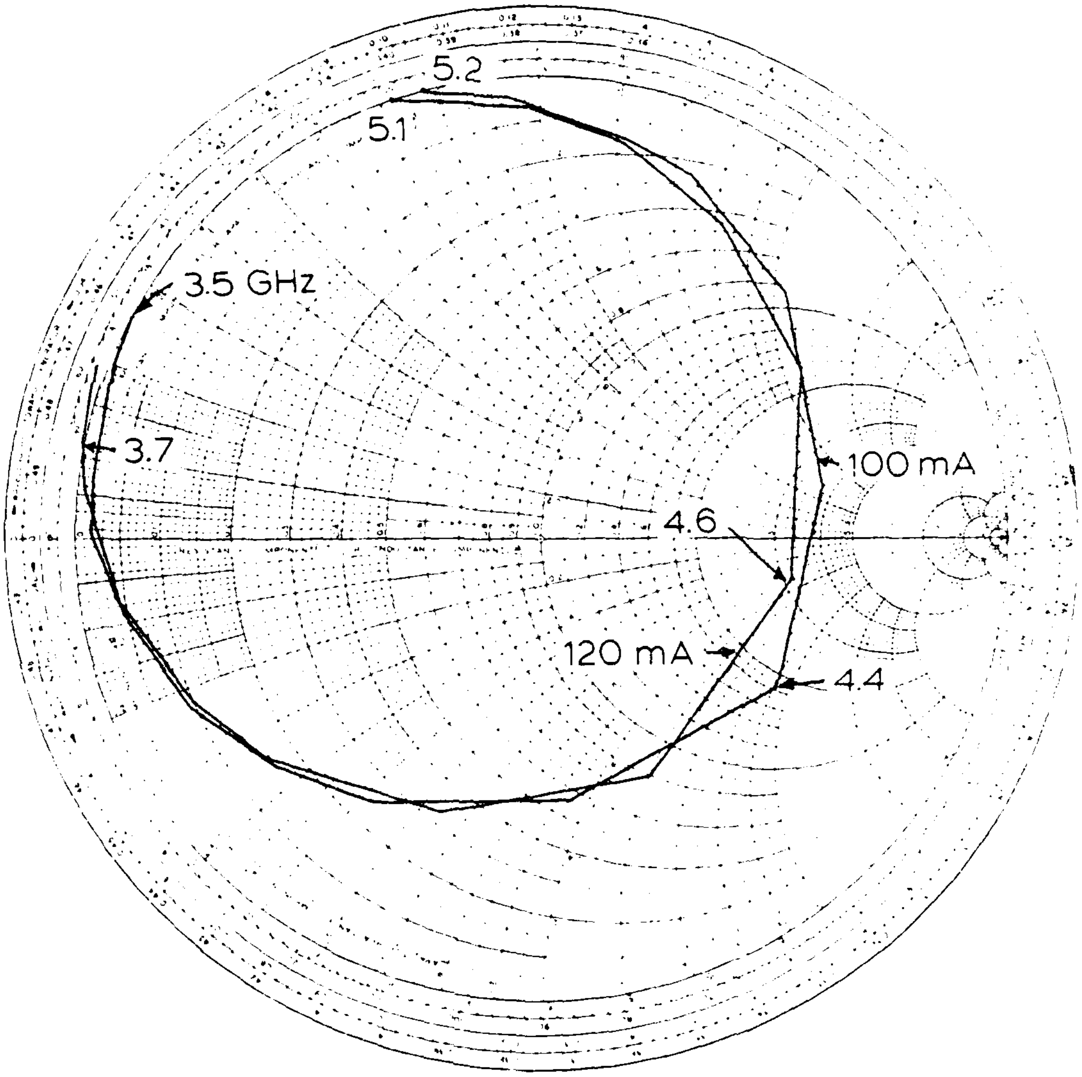


FIG. [illegible] [illegible]

FIG. [illegible] [illegible]

A [illegible] TRANSMISSION LINE [illegible]

[illegible] IMPEDANCE [illegible].

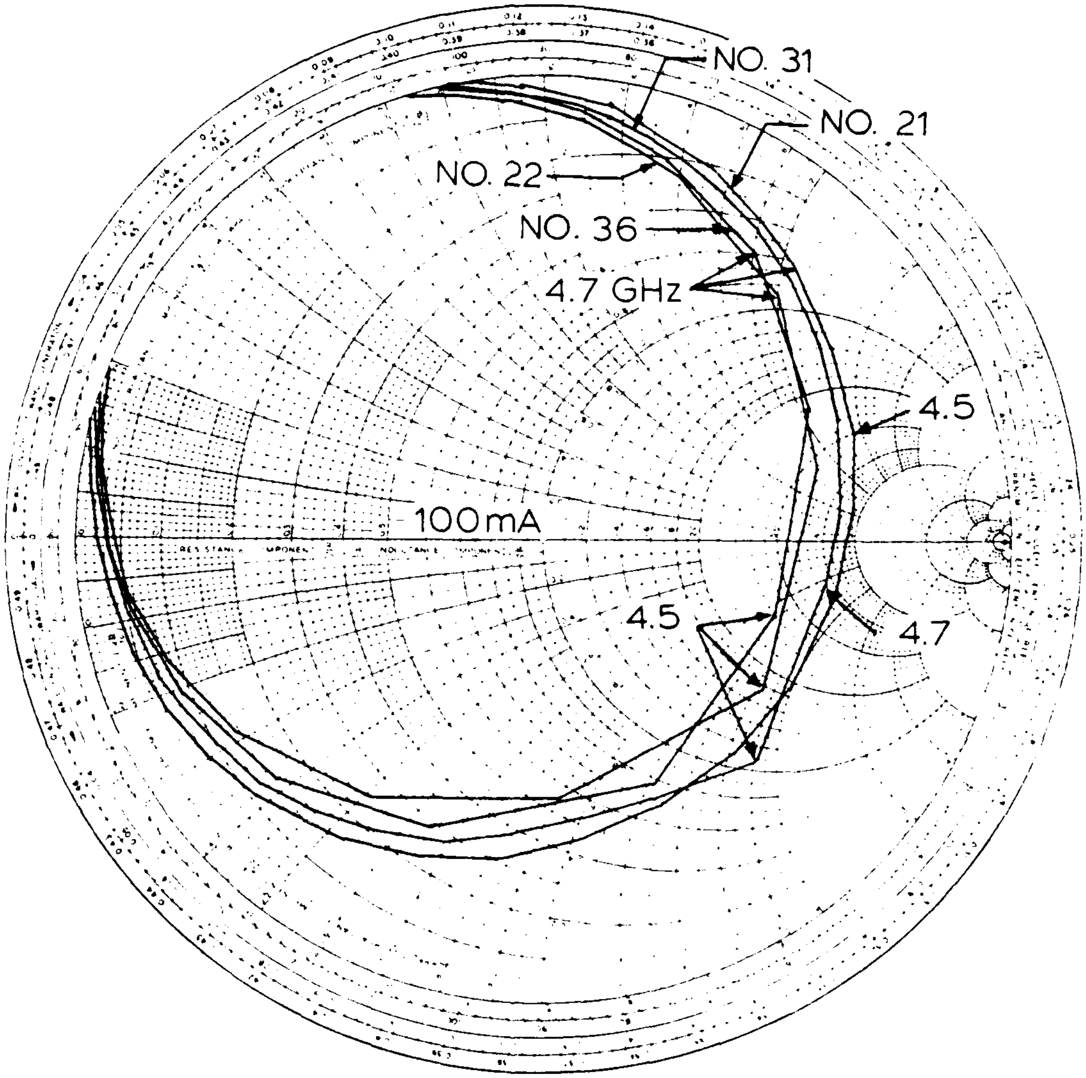
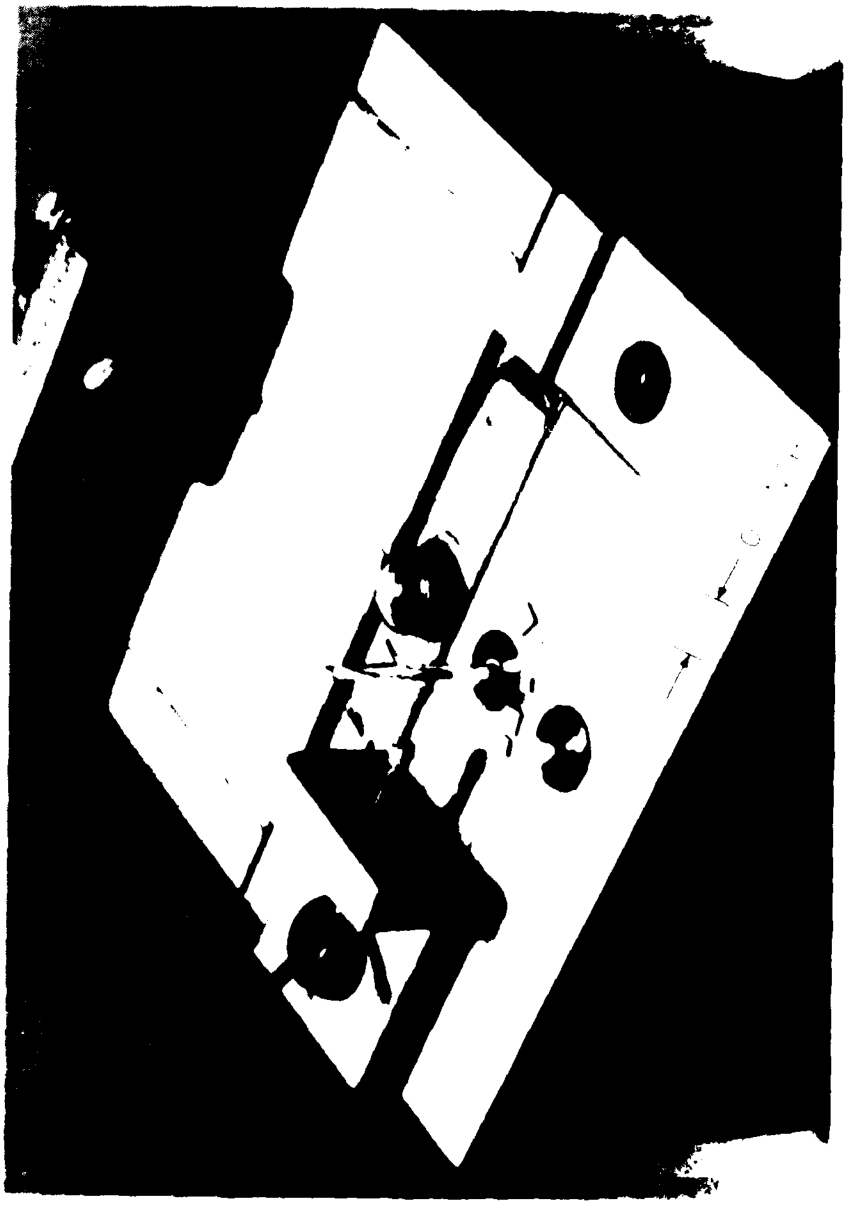


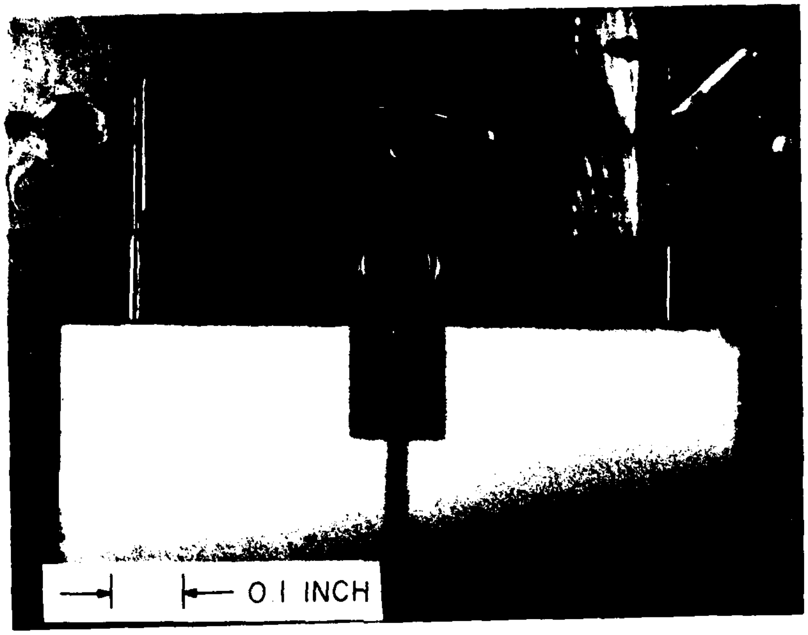
FIG. [illegible] SMALL-SIGNAL IMPEDANCE [illegible]

[illegible]

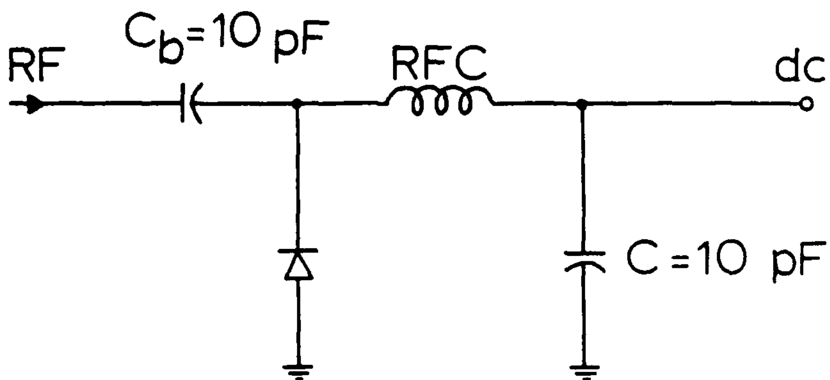


One end of the RFC is bonded to the device and the other end is bonded to an offset chip capacitor which is in turn connected to a dc feedthrough providing the required bias to the device. An additional offset capacitor is provided in series between the IMPATT device and RF connector for dc isolation of the measurement port. Such bias circuits have been very useful for the MIC circuits developed in this investigation, providing 30 to 40 dB of isolation. There is flexibility in the choice of offset capacitances. The rule of thumb followed in this study is to provide a low reactive value for the series isolation capacitance (at operating center frequency) as well as the by-pass capacitance forming the LC-combination on the bias port. A resonant LC-combination in the bias circuit at the subharmonic frequency is needed to eliminate this form of instability. If no subharmonic problems are evident, a suitable choice of by-pass capacitances can improve the impedance transformation of a device in the test circuit. Figure 3.15 shows the test fixture circuit board and its electrical equivalent circuit. Different by-pass capacitors were used to determine the most suitable value for the bias circuit. Another feature of the test fixture is the ease by which a device can be exchanged. Each IMPATT diode is soldered into metal cylinders which are held securely in the fixture assembly by machine screws. The entire assembly is made up of different sections to accommodate any modifications required in device or bias networks.

Figure [illegible] illustrates a typical result of reflection gain for a device measured as a function of frequency and bias current in the test circuit of Fig. 3.14. Typically peak [illegible]



(a)



(b)

FIG. 3.15 (a) TOP VIEW OF A SINGLE DEVICE MICROSTRIP TEST CIRCUIT WITH BIAS CIRCUIT. (b) BIAS TEST CIRCUIT.

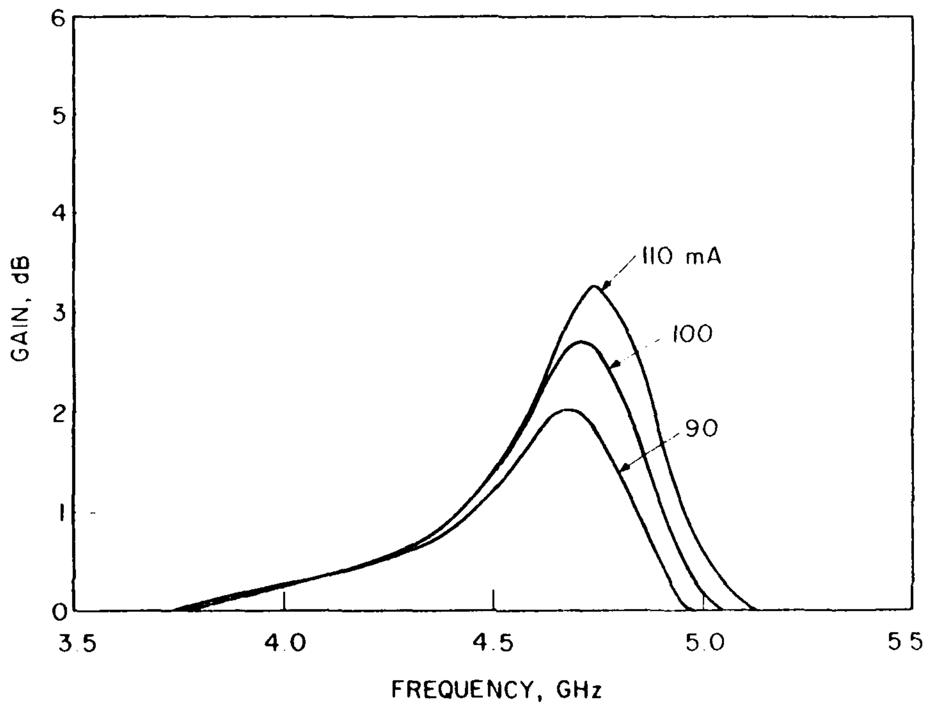


FIG. 3.16 SMALL-SIGNAL REFLECTION GAIN OF A DEVICE MEASURED IN THE MICROSTRIP TEST CIRCUIT OF FIG. 3.14.

of 2.5 to 3.5 dB were obtained at approximately 4.8 GHz. The negative impedance data associated with Fig. 3.16 is shown in Fig. 3.17 normalized to 50 Ω. Only minor differences in active bandwidth and reflection gain are apparent when the bias circuit is present.

Based on the measured results of several devices, a design for a two-diode microstrip combiner was developed. With reference to Fig. 3.17, two-diodes can provide a stable combiner design by using a length of line to place the circuit curve in the passive region of the diode curve over the active bandwidth. The circuit requirements are (for odd-mode stability)

$$|\overline{X_c(3.8\ \mathrm{GHz})}| \geq 0.5 \tag{3.2}$$

and

$$|\overline{X_c(5.1\ \mathrm{GHz})}| \leq 1.6 \ . \tag{3.3}$$

These conditions prevent the device-circuit interaction that may lead to odd-mode instabilities.

The conditions specified by Eqs. 3.2 and 3.3 can be satisfied by a length of transmission line in addition to the λ/4- transformer specified earlier in Fig. 3.5 or an appropriate lumped inductance element. Since the final combiner design is a planar microstrip structure, connection of the combining port is easily achieved with suitably chosen inductive bond wires.

A length of gold bonding wire can be considered as a lumped inductance of value,[18]

$$L = [illegible] \left[\ln\left(\frac{4\ell}{d}\right) - 1 \right] , \tag{3.4}$$

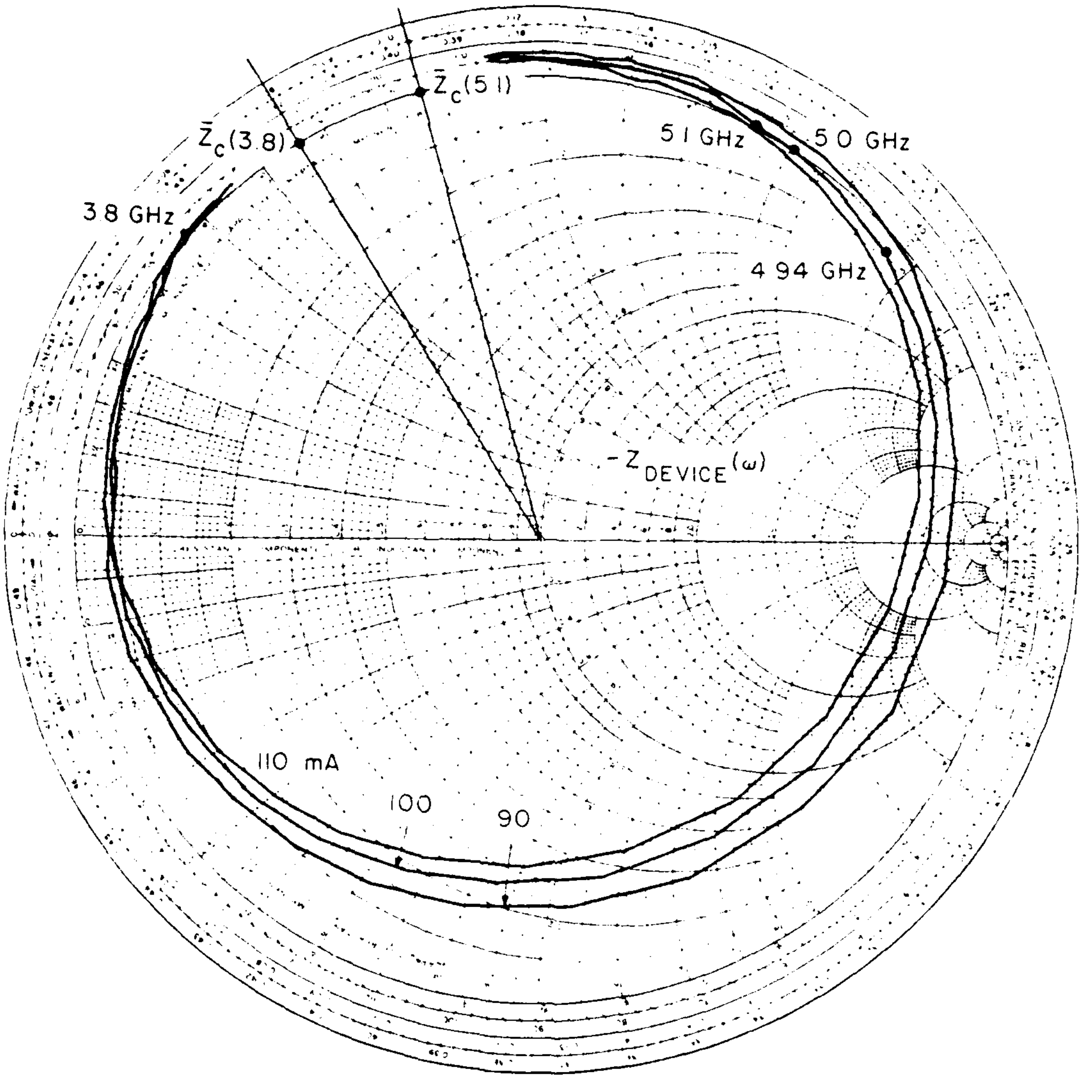


FIG. 3.17 PLOT OF SMALL-SIGNAL NEGATIVE IMPEDANCE ASSOCIATED WITH FIG. 3.16. THE DATA IS ROTATED THROUGH A LENGTH OF TRANS-MISSION LINE AND NORMALIZED TO 50 [illegible]. [illegible] DESIGN IS POSSIBLE BY SELECTING A CIRCUIT IMPEDANCE Z_c WHICH EXHIBITS IMPEDANCES AT 3.8 AND [illegible] GHz AS SHOWN.

where d is the diameter of bonding wire in inches, ℓ is the length of bonding wire in inches, and L is the lumped inductance value in nH. Using a length of 0.007 in diameter wire, .0[illegible] in length, results in an equivalent inductance L = 1.[illegible] nH. At the active diode frequency limits, this inductance corresponds to normalized circuit reactances of 0.56 and 0.76 as shown in Fig. 3.17. Clearly a stable combiner design as outlined from the device characterization results obtained in the latest microstrip test circuit is possible.

3.2.2 Two-Diode Microstrip Combiner Test Circuit. A two-diode microstrip TEM line combiner was designed and constructed based on results from individual IMPATT device measurements conducted on devices in various microstrip test circuits. The implemented design is shown schematically in Fig. 3.18. The simple two-way symmetry of the circuit is clearly evident. Two independent device bias circuits are incorporated into the design to provide separate bias current control for the devices. In addition, two microstrip impedance transforming networks are utilized to improve the circuit-device impedance match. A 50-Ω load is used at the combining point for the combiner load impedance.

The physical realization of the combiner design is shown in Figs. 3.19, 3.20 and 3.21. Each figure illustrates a slightly different feature of the entire combiner test-fixture assembly which consists of three parts: (1) the microstrip circuit board, (2) the dc bias port circuits, and (3) the combining port used for common excitation and RF power output. Each of the three parts of the combiner will be described in detail.

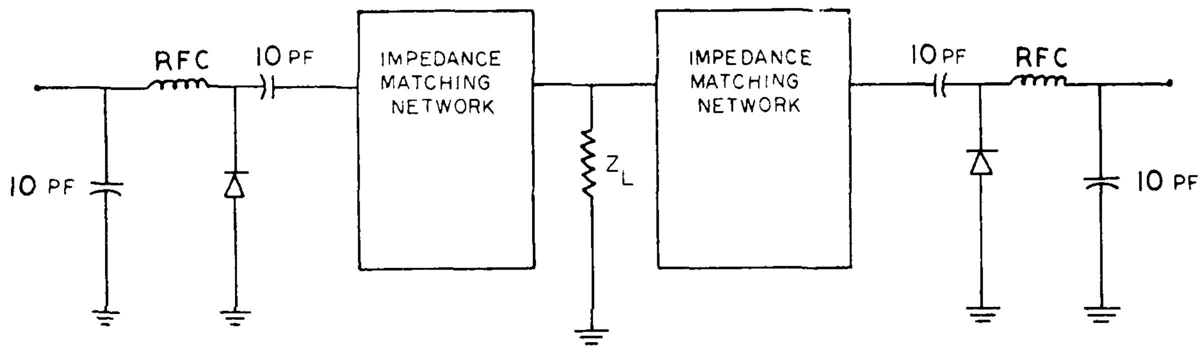


FIG. 3.18 ELECTRICAL [illegible]

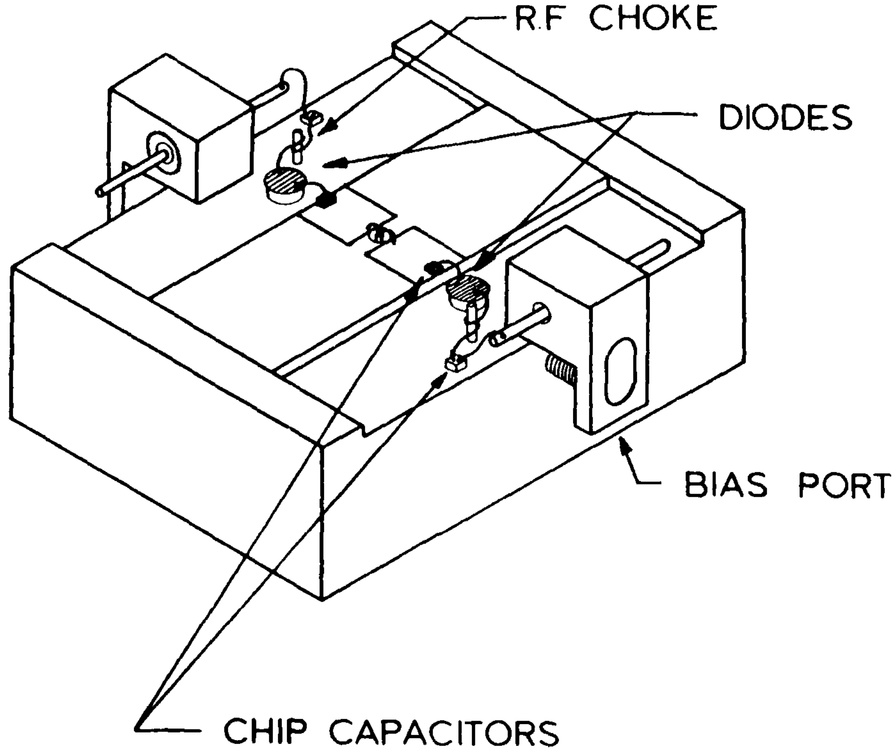
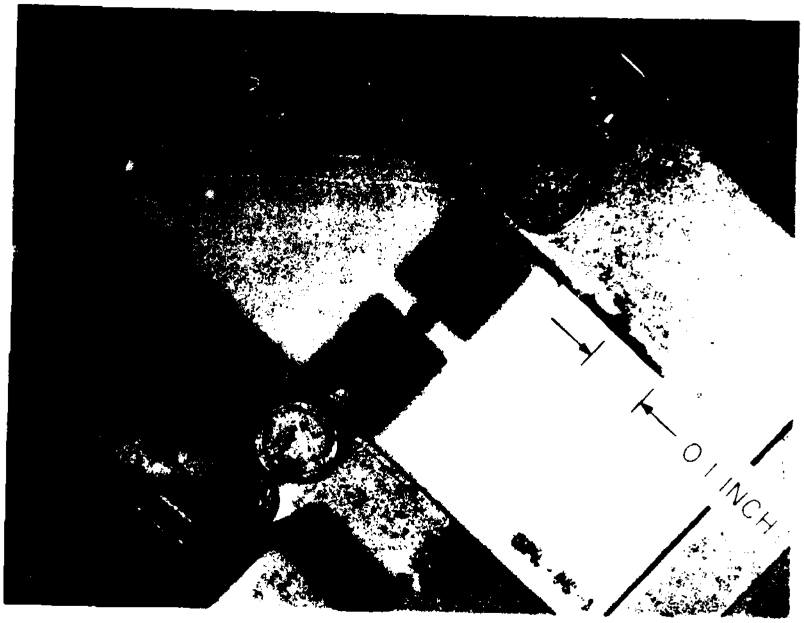


FIG. 3.19 ILLUSTRATION OF MICROSTRIP COMBINER TEST FIXTURE.

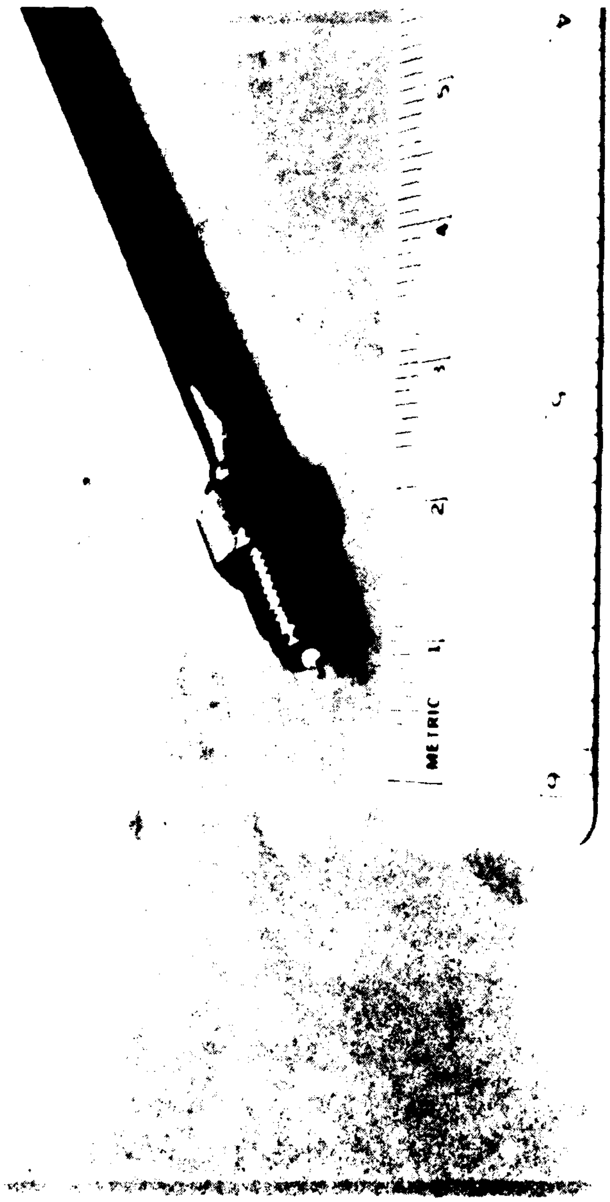

0.1 INCH

The microstrip circuit board contains the combining lines providing the appropriate terminations to the individual IMPATT devices. The board consists of 0.025 in thick alumina with a 0.030 in diameter holed placed in its center. An ultrasonic impact drill was required to drill the hole in the alumina board. Arranged on opposite sides of the center hole, two low-impedance sections of microstrip lines function as combining lines connecting the devices to common points for RF power output. Moreover, these microstrip sections function as impedance transformers providing an improved impedance match between the 50-Ω impedance at the combiner port and the low impedance of the packaged IMPATT devices. The design of these combining lines is identical to that used on the single-device microstrip test circuits described earlier. The circuit was duplicated on the two-diode combiner circuit as shown in Figs. 3.20 and 3.21.

The combiner design utilizes two independent bias sources to supply current-controlled bias to each IMPATT device. The use of independent supplies circumvents potential problems of thermal runaway and current stealing that can occur by using a single power supply. However, the two-supply design requires dc isolation between the two devices. This requirement is handled by the incorporation of two bias port circuits on the combiner test fixture. Each of the bias circuits include the same RF chokes and by-pass [illegible] capacitors as were used on the earlier microstrip test circuits. The bias circuits isolate each device from dc and provide a means of effectively supplying dc current to each device while blocking RF. Ceramic "feed throughs" facilitate the [illegible] to this test fixture, and provide an extra measure of strength to the entire assembly.

The combiner combining port is realized on the planar topology of microstrip by the use of a planar-to-coaxial transition. A small hole drilled in the alumina microstrip board provides a via for the center conductor of a coaxial transmission line to protrude through the microstrip planar surface forming a post. Silver contact epoxy is then used to anchor the midpoint of a length of 0.0007 in diameter gold bond wire onto this post. The other two ends of this wire are thermocompression bonded to the ends of each microstrip combining line. Figure 3.21 illustrates the top view of the microstrip board which clearly shows the transition required to realize the common combining point (a summary of this microstrip circuit board fabrication can be found in Appendix B.) Figure 3.22 illustrates the panel mount coaxial connector used as the combining port line. The panel mount is screwed into the combiner test fixture from underneath.

The two IMPATT devices are secured into the combiner test fixture by soldering them into cylindrical copper heat sinks, then fastening these firmly into prescribed cylindrical holes in the fixture assembly by means of machine screws. In this way, a suitable heat sink was provided by air cooling the combiner fixture. An additional restriction was found regarding the device bias current. The bias current upper limit was 160 mA. Surpassing this value resulted in bond wires melting and device burnout.


METRIC

<u>3.2.3 Single Device Characterization in the Two-Diode Combiner Test Fixture</u>. The nature of the coaxial-to-planar transition used on the two-diode combiner circuit is different from the single diode microstrip circuits. Consequently, additional device characterization measurements were carried out on the IMPATT devices using one-half of the combiner test fixture as shown in Fig. 3.23. The bond wire, connected to only one combining line, allows measurement of a single device in a circuit more suitable for predicting two-diode combiner performance.

Figure 3.24 illustrates the small-signal reflection gain of a typical device as measured in the two-diode combiner test fixture. Data for three different bias currents are shown with bandwidth 4.65 to 4.95 GHz. Peak small-signal gain at [illegible] mA bias current is 3.7 dB.

Using a short-circuit cap, a measurement reference plane was established at the combiner combining point and impedance data referenced to this point was obtained for individual IMPATT devices in the two-diode combiner test fixture. The data corresponding to Fig. 3.24 is plotted, normalized to 50 Ω on a Smith chart in Fig. 3.25. The diode curves of Fig. 3.25 represent small-signal data for three different bias current levels. The active device bandwidth is from approximately 4.6 to 4.9 GHz. The inset of Fig. 3.25 establishes the measurement reference plane for this data. In order for an odd-mode instability to occur, one of the device curves shown would have to intersect the short-circuit impedance point on the Smith chart. The narrow bandwidth of these IMPATT devices prohibits this intersection.

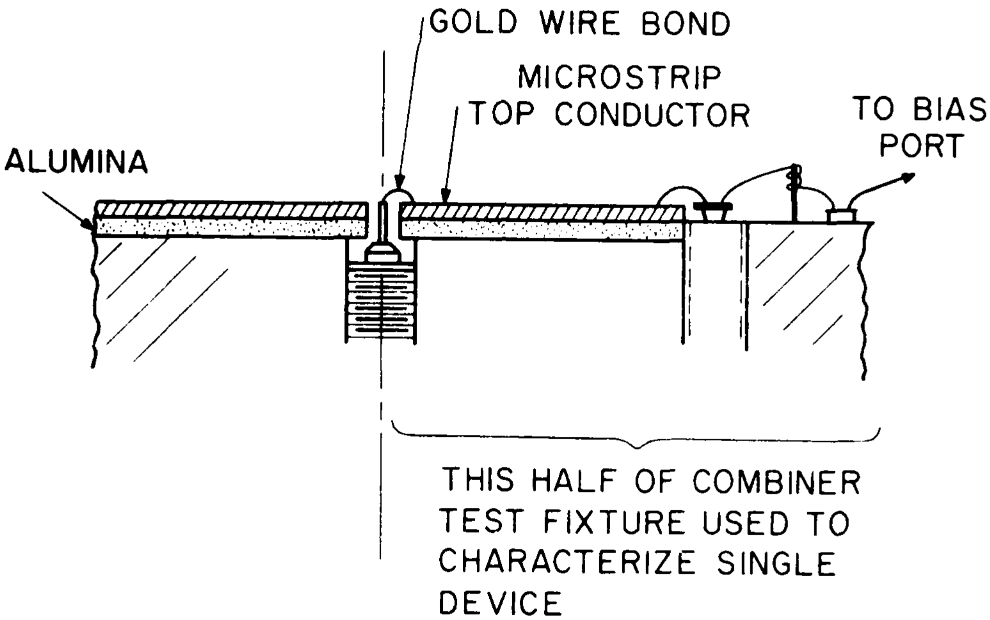


FIG. [illegible] CROSS SECTION VIEW OF ONE-HALF OF THE TWO-DIODE MICROSTRIP COMBINER USED IN CHARACTERIZING SINGLE DEVICES.

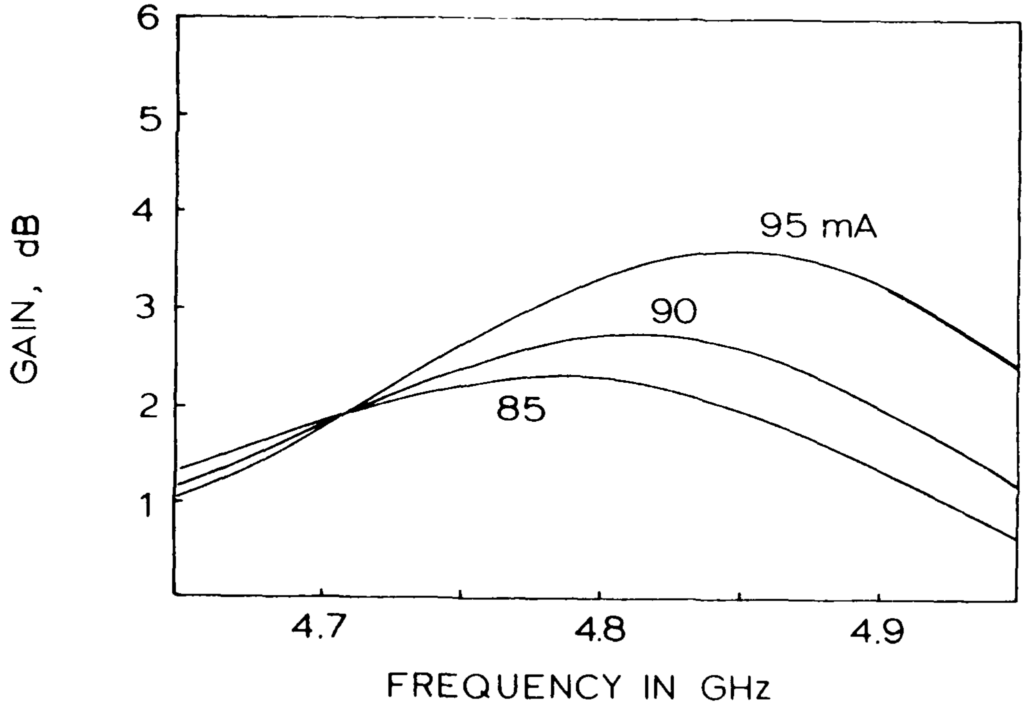


FIG. 3.24 REFLECTION GAIN OF A TYPICAL DIODE AS MEASURED IN THE MICROSTRIP COMBINER CIRCUIT.

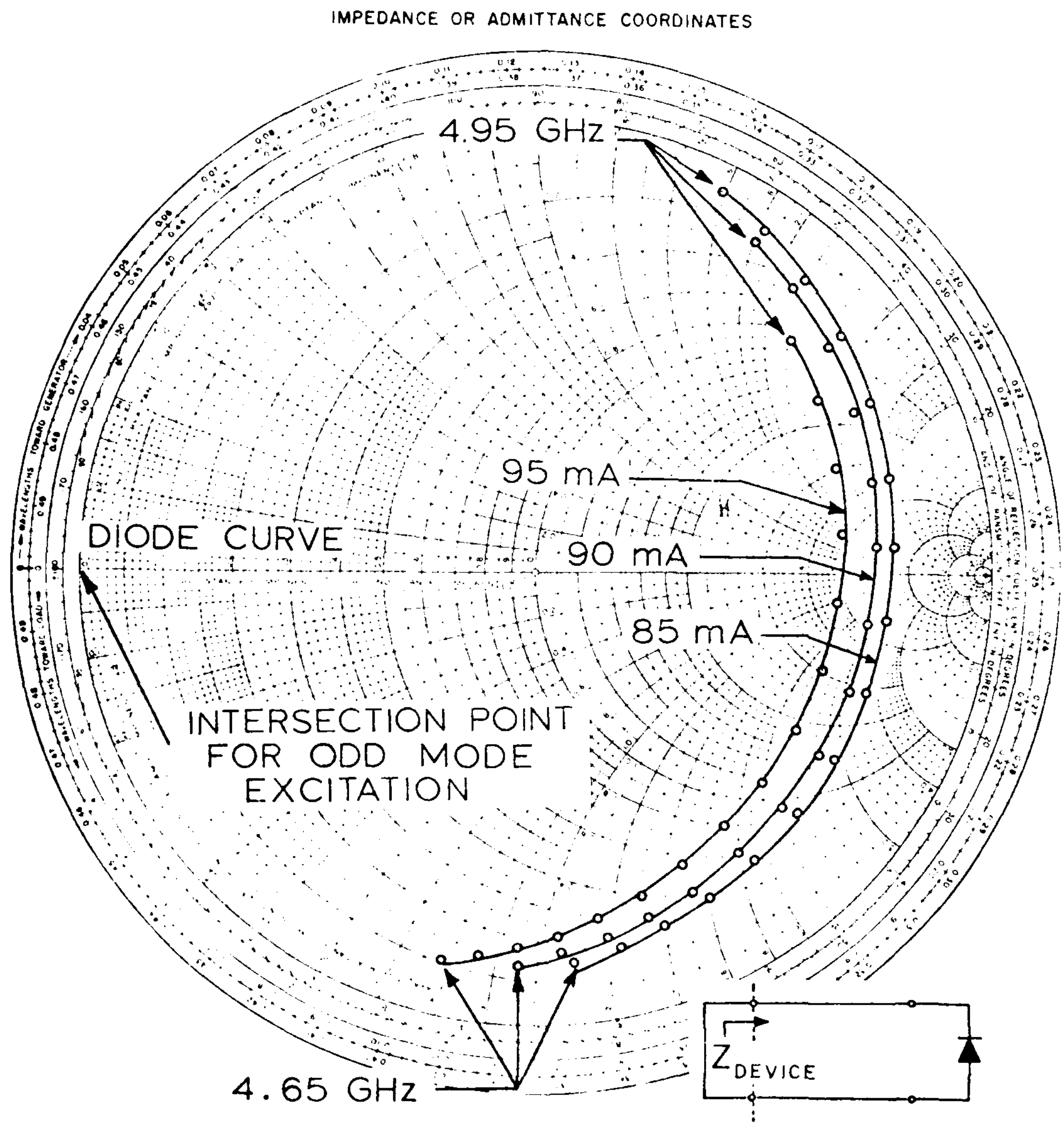

IMPEDANCE OR ADMITTANCE COORDINATES
4.95 GHz
95 mA
DIODE CURVE
90 mA
85 mA
INTERSECTION POINT
FOR ODD MODE
EXCITATION
4.65 GHz
Z_{DEVICE}

FIG. [illegible]

The reduced phase variation of the device curves in the combiner test circuit with respect to the microstrip test fixtures is probably attributed to less stored energy in the coaxial-to-planar transition of the two-diode circuit. This provides a large stability margin and offers flexibility in the circuit selection.

Large-signal measurements were also conducted on individual devices in the two-diode combiner circuit. Figure 3.26 illustrates reflection gain information of a typical combiner device as a function of input power level for several frequencies. The data shown is for a device biased at a current level of 100 mA. The peak gain occurs at an input power level of approximately 5 dBm and saturates gradually to passivity by 25 dBm of input power.

The performance of a power combiner is specified by its power generation capability. This can be determined by measuring the reflected and incident powers coming from the devices and taking their difference. This is the power added by the device or device generated power.

Figure 3.27 illustrates the measured generated power of an IMPATT device as a function of input power level. Data is presented for four different frequencies. The maximum generated power of 43 mW occurs at 4.65 GHz for an input power of approximately [illegible] dBm. Higher frequencies provided less generated power. Equipment limitations did not allow data to be obtained below 4.6[illegible] GHz. Also, circuit loss becomes increasingly significant for measurements under high input power, low gain conditions (as seen in Fig. 3.26) thereby reducing the effective added power.

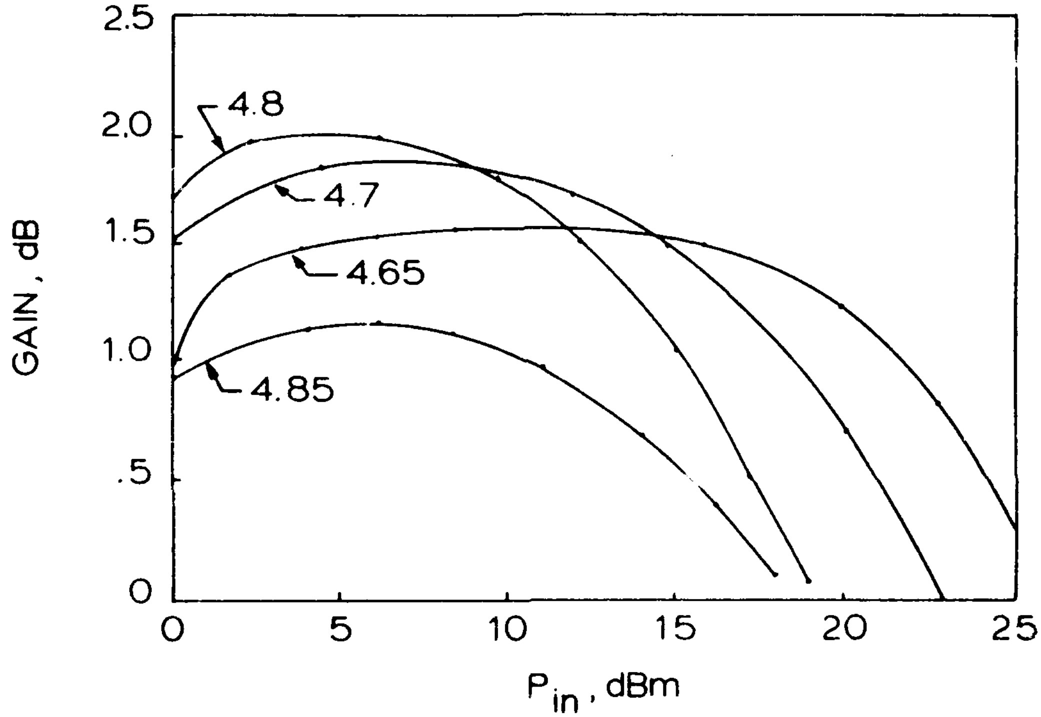


FIG. 4.[illegible] LARGE-SIGNAL DEVICE CHARACTERIZATION RESULTS AS MEASURED IN THE TWO-DIODE COMBINER CIRCUIT. DATA CORRESPONDS TO 100 mA BIAS CURRENT LEVEL.

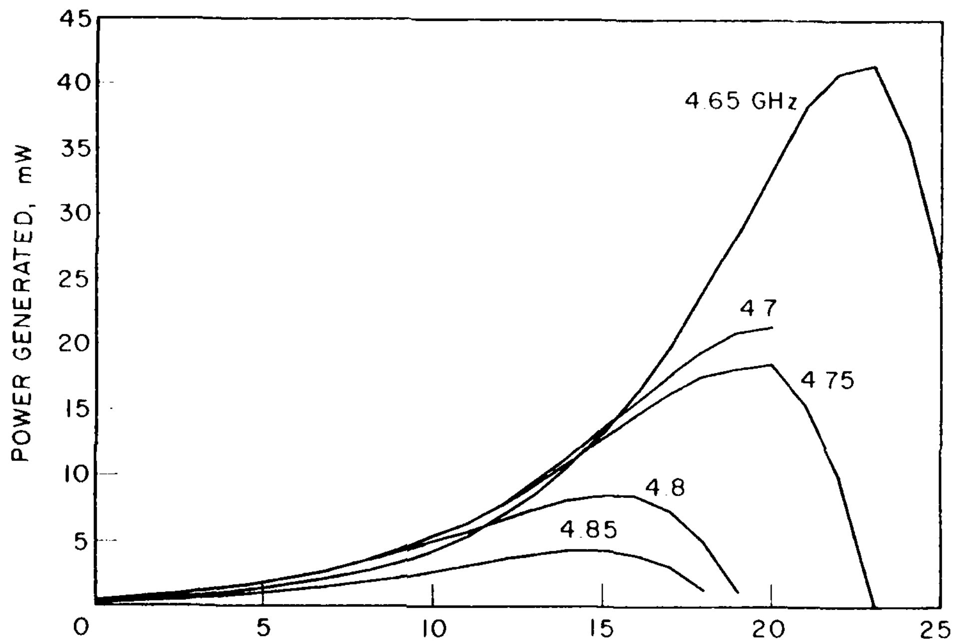


FIG. 3.27 MEASURED ADDED POWER DATA FOR A MICROSTRIP COMBINER DIODE (100 mA BIAS CURRENT).

The data acquired for individual devices in the two-diode combiner test circuit allows the performance of two-diode operation to be predicted. Measured impedance data at the combining point differs from that obtained in microstrip test fixtures which had no coaxial-to-planar transition at the output port.

In the sections that follow characterization results on the two-diode combiner will be presented. It will be shown that the stable operation predicted from the single device measurements made in the combiner circuit do indeed lead to stable combiner operation.

3.2.4 Two-Diode Microstrip Combiner Characterization. RF measurements were conducted on the two-diode microstrip combiner to determine the operating characteristics of this design as an amplifier or oscillator to verify and establish that stable, power-summing operation under both small-signal and large-signal drive levels was occurring. This section describes the experiments used to evaluate the combiner performance and summarizes the results of RF characterization on the two-diode combiner design.

3.2.4.1 Combiner dc characteristics. The dc bias required by the IMPATT devices (diodes C1 and C2 used in combiner) used in this combiner design was supplied by two independent current sources. This eliminated the problem of "thermal runaway" where one diode could steal all the current from a single supply and destroy the device. In addition, a two-bias-supply design affords a degree of tuning flexibility for improving the similarity of the devices used.

Throughout the experiments on the microstrip combiner, device bias current levels were maintained to the range of 80 to 105 mA per device with corresponding voltages of 115 to 120 V. This limitation was imposed for two reasons: (1) the 0.0007 in diameter gold bonding wire used to connect device to circuit can only sustain approximately 170 mA of current before melting, and any bends or kinks in this bond wire even further reduces the ability of the gold wire to handle current, subsequently reducing the melting current limit even further; and (2) the heat-sink properties of the packaged IMPATT devices are not adequate in a microstrip circuit environment. Bias current levels greater than 130 mA resulted in destruction of devices. Air cooling the circuit and providing heat-sink plates was necessary.

<u>3.2.4.2 Small-signal experimental results.</u> Combiner small-signal experiments were made on the two-diode microstrip combiner operating in an amplifier mode. Figure 3.28 illustrates the small-signal reflection gain measured at the combining port of the microstrip combiner. Data for different bias current levels (85 to 100 mA) are shown. Approximately 10.5 dB of small-signal gain was achieved at a 100 mA bias level at a frequency of 4.64 GHz. The typical active-device bandwith was approximately 4.6 to 4.9 GHz with fractional 3 dB bandwidths ranging from approximately 2.5 to 3.2 percent.

The small-signal combiner impedance referenced to the combining point is shown in Fig. 3.29 for bias currents of 85, 90 and 100 mA. The data is presented in the inverse reflection coefficient plane, as described earlier. The load impedance Z_L at the combining

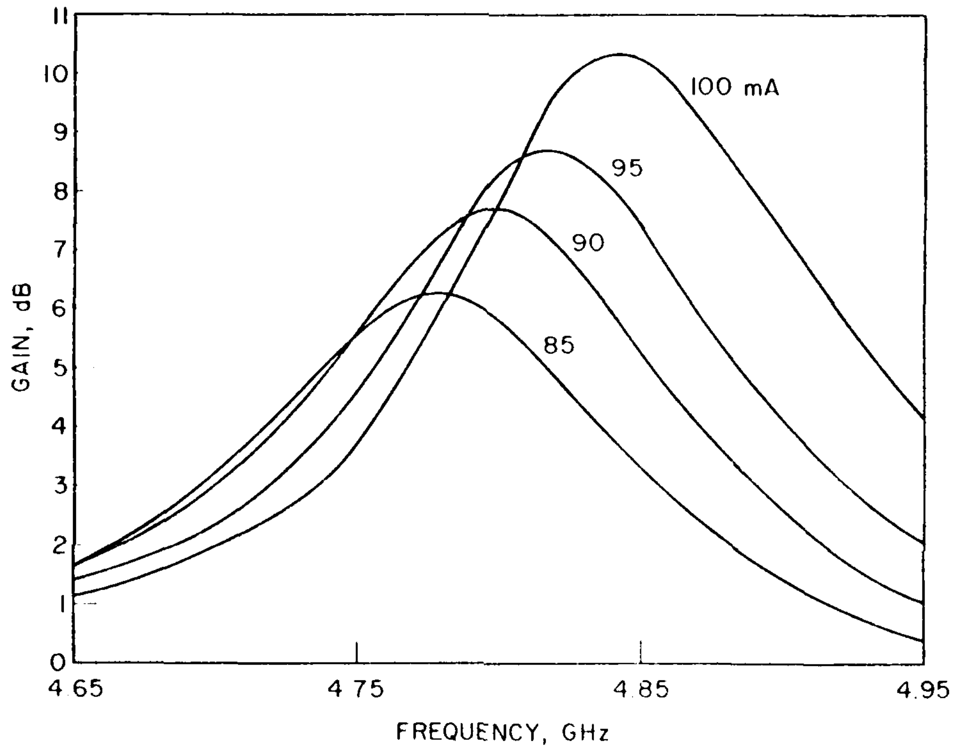


FIG. 3.28 SMALL-SIGNAL REFLECTION GAIN OF THE TWO-DIODE MICROSTRIP COMBINER.

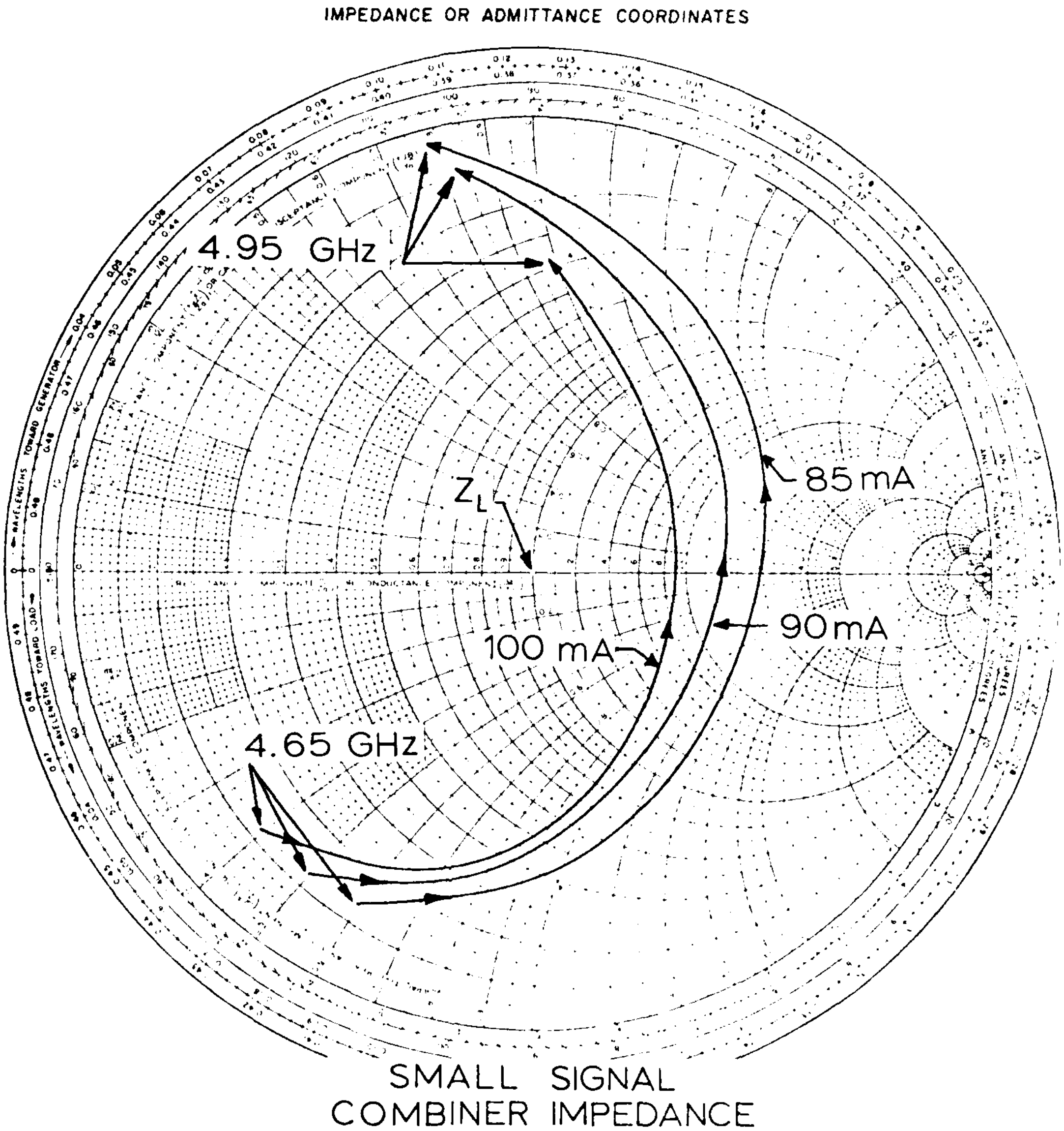


FIG. 3.29 MEASURED SMALL-SIGNAL COMBINER [illegible] MICROSTRIP COMBINER. THREE BIAS [illegible] SHOWN. THE COMBINING PORT LOAD [illegible].

point is assumed to be 50 Ω. If the bias current is increased beyond the maximum value shown in Fig. 3.29, the corresponding combiner curve moves inward toward the center of the chart, intersecting the 50 point and causing oscillations. Such oscillations represent even-mode oscillator combining.

3.2.4.3 Large-signal experimental results. The combiner reflection gain and impedance level were measured under large-signal conditions in much the same way as the small-signal combiner characterization was obtained. Using the large-signal measurement test set shown earlier, large-signal impedance information was measured for a given frequency and input power level. Figure 3.30 illustrates the measured reflection coefficient gain vs. input power level P_{in} for different measurement frequencies. The largest reflection gain, 9.5 dB, occurs at approximately 1 dBm of input power at a frequency of 4.78 GHz (96 mA). Gain compression is evident; for the frequencies considered, reflection gain drops to below [illegible] dB at an input power level of [illegible] dBm. Figure 3.31 provides additional information of large-signal reflection gains. In this figure, reflection gain is plotted vs. frequency for several different input power levels. The measured data [illegible] the reflection gain [illegible]. Data below [illegible] GHz was unobtainable due to lower frequency limitations in the available TWT amplifier used in the large-signal test set.

The reflection gain of the combiner is not the best measure of the combining function since it is dependent on the circuit in which the combining devices are embedded. A better measure of the combining capabilities of this design is to examine the combiner generated power P_{gen} (or added power). The expression for [illegible]

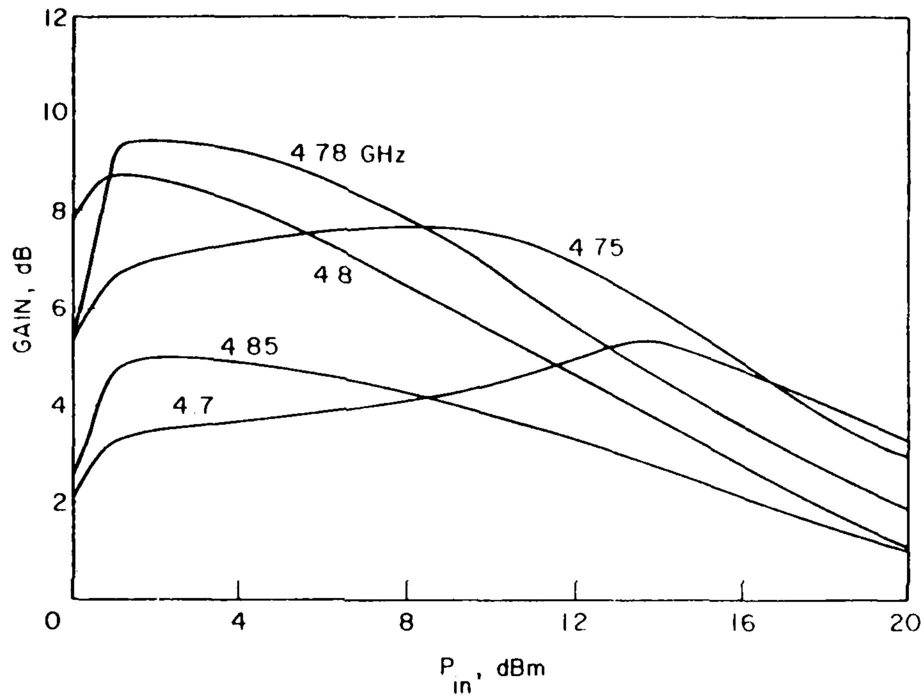


FIG. 3.30 LARGE-SIGNAL REFLECTION GAIN OF THE TWO-DIODE MICROSTRIP COMBINER.

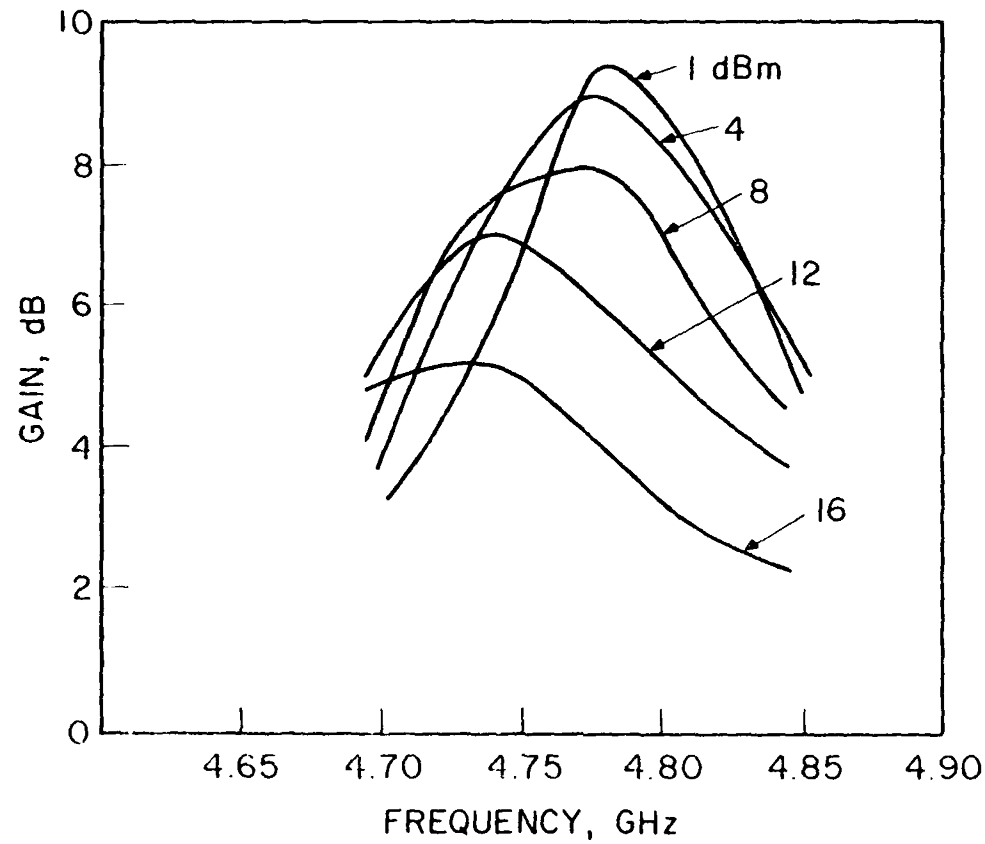


FIG. 3.31 LARGE-SIGNAL REFLECTION GAIN OF THE TWO-DIODE MICROSTRIP COMBINER.

generated power is given by

$$P_{gen} = P_{ref} - P_{in} = P_{in}(|\Gamma|^2 - 1) \quad , \qquad (3.5)$$

where P_{ref} is the reflected power coming from the combiner network, P_{in} is the incident excitation power injected into the network, and $|\Gamma|$ is the magnitude of the network reflection coefficient. Equation 3.5 represents the power generated (added power) by the device/network. The added power is a useful measure of the combining function. As indicated in Fig. 3.32, the power generated by a lossless combiner will be identical if measured at the device terminals or at some more accessable measurement plane. An efficiency can be defined as

$$\eta = \frac{P_{at}}{\sum_{k=1}^{N} P_{ak}} \quad , \qquad (3.6)$$

where N is the total number of devices, P_{ak} is the added power of the kth device, and P_{at} is the total added power of the combiner. As defined in Eq. 3.6, the combiner efficiency for a truly lossless combiner is unity. In practice, efficiencies both greater and less than unity have been observed. The value obtained is dependent on how P_{ak} is obtained. Values of η less than unity would indicate a more lossy circuit than expected. Values of η greater than unity can indicate one of two possibilities: (1) P_{ak} was not measured properly, the added power may have been measured in a circuit not optimally suited for obtaining maximum added power; or (2) the waveforms associated with multiple device operation may be more efficient than single device waveforms. This may be in part due to

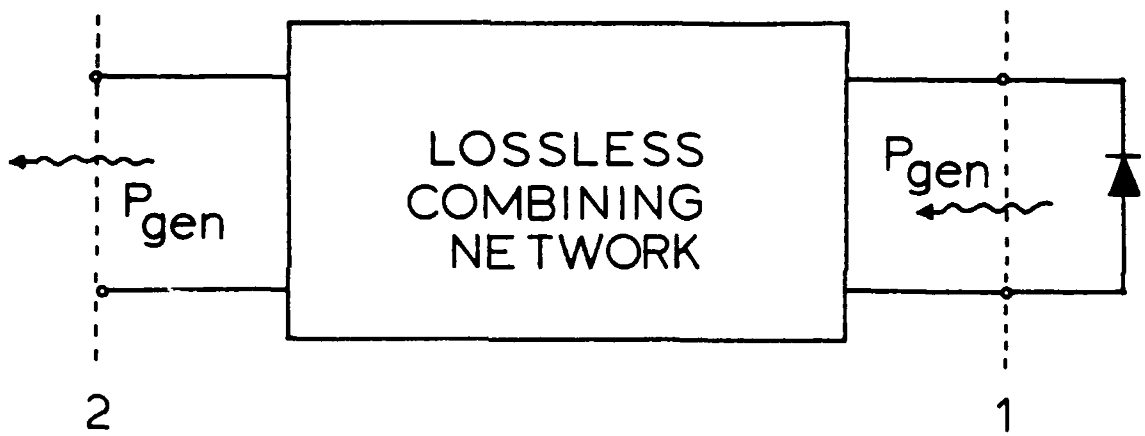


FIG. 3.3[illegible] ILLUSTRATION SHOWING THAT P_{gen} IS IDENTICAL AT THE DEVICE TERMINALS AND THE MEASUREMENT PORT IN A TRULY LOSSLESS COMBINER CIRCUIT.

differences in the circuit. Values of η slightly less than unity do offer confirmation of high combining efficiency. In a real combiner, the ideal combining efficiency of unity is often unattainable. Figure 3.33 shows the combiner generated power plotted as a function of input power level for various frequencies, and peak generated power occurs at approximately 158 mW of input power at a frequency of 4.7 GHz. The peak level corresponds to approximately 135 mW of power supplied by the combiner.

The measured large-signal impedance data for the two-diode combiner is shown in Fig. 3.34. The data is for a bias current of 90 mA. Impedance level for the frequencies 4.7, 4.75, 4.8 and 4.85 GHz are shown spiraling outward toward the perimeter of the chart as the reflection gain saturates. This data is normalized to 50 Ω and referenced to the combiner combining point. Some large-signal effects can be seen for some frequencies where gain peaks at a level just higher than the small-signal value.

3.2.4.4 Oscillator performance of two-diode combiner. If the experiment test set of Fig. 3.35 is used, a suitable circuit impedance can be provided to the combiner by the test-set tuner to result in oscillator operation. Figure 3.36 shows a display from a spectrum analyzer illustrating the oscillator signal. Peak oscillator power was achieved with both combiner IMPATT devices biased at 105 mA resulting in 126 mW (21 dbm) of oscillator power at a frequency of 4.65 GHz. The maximum oscillator power point occurs at a frequency away from the small-signal maximum gain point. This is due to the large-signal effects at 4.65 GHz which can increase the gain above that at small signal.

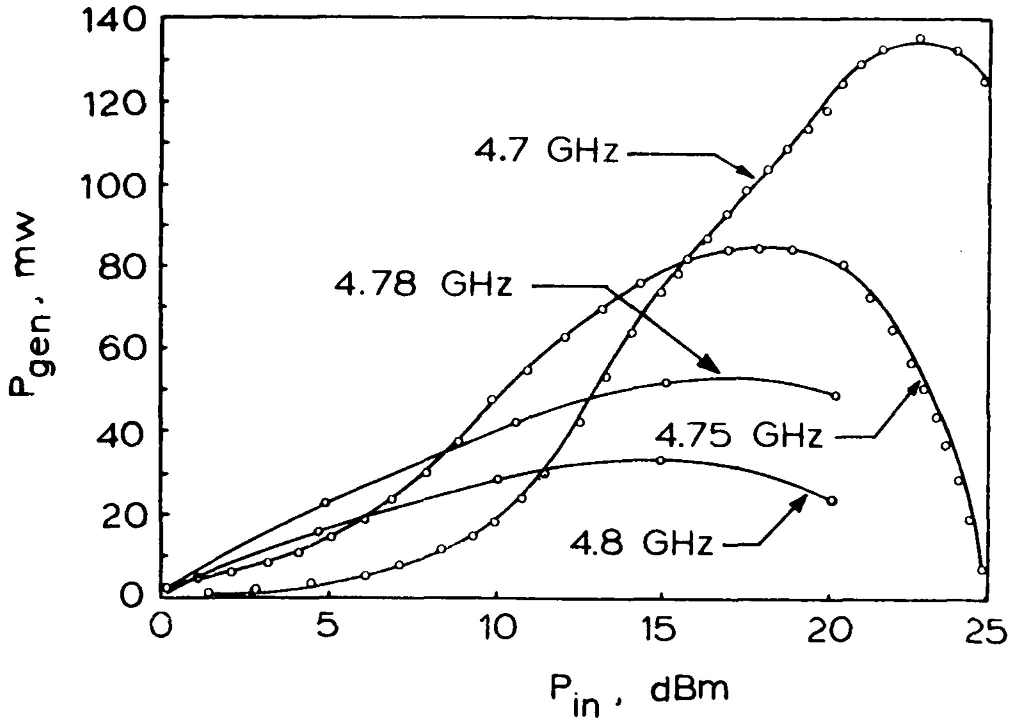
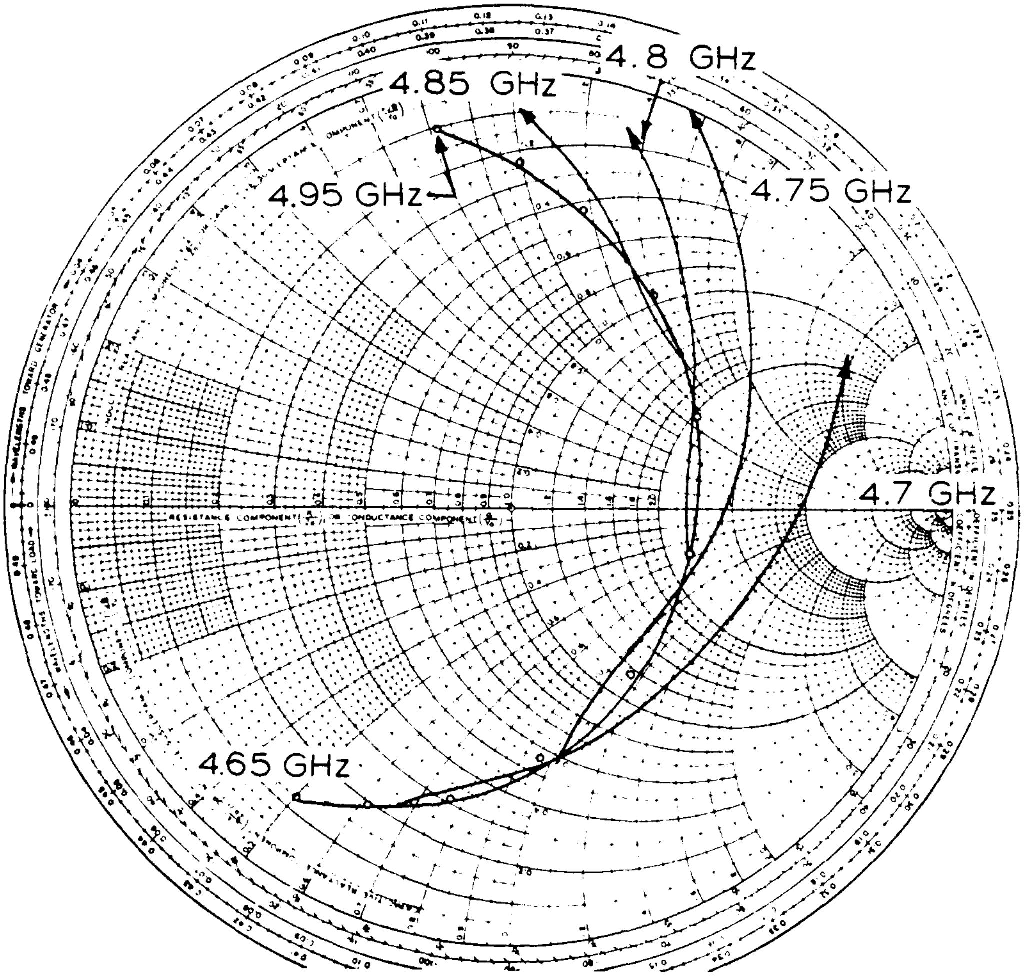


FIG. 3.33 MEASURED LARGE-SIGNAL RESULTS FOR THE THREE-DIODE MICROSTRIP COMBINER.



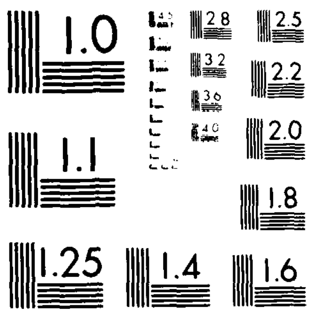
2-DIODE COMBINER
(MEASURED DATA)

FIG. [illegible] MEASURED [illegible]

AD-A142 599 LOSSLESS SYMMETRIC TEM LINE IMPATT DIODE POWER COMBINERS(U) MICHIGAN UNIV ANN ARBOR ELECTRON PHYSICS LAB R ACTIS APR 84 TR-164 AFWAL-TR-84-1035 2/2

UNCLASSIFIED F33615-81-K-1429 F/G 9/5 NL

END
DATE
FILMED
8-84
DTIC



MICROCOPY RESOLUTION TEST CHART
NATIONAL BUREAU OF STANDARDS-1963-A

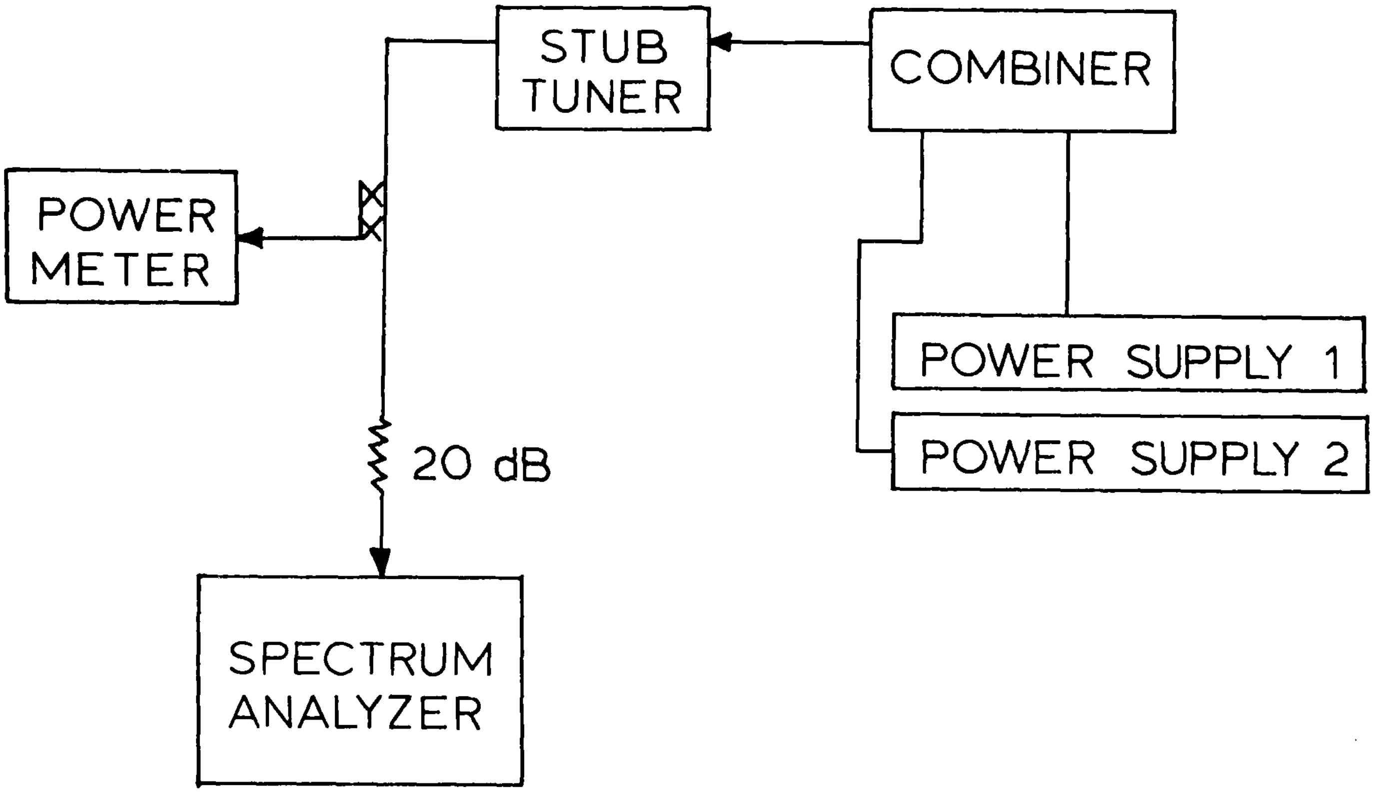
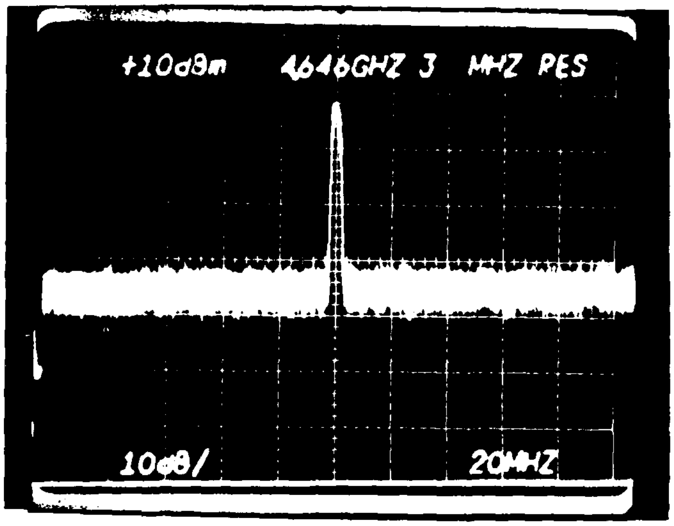
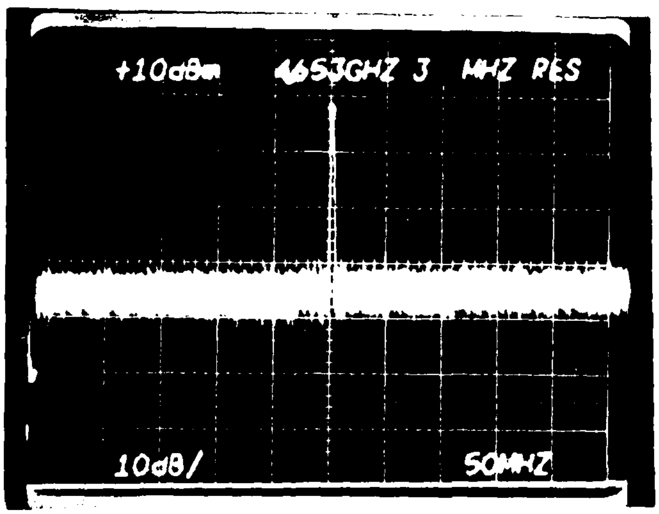


FIG. 3.35 COMBINER/OSCILLATOR MEASUREMENT TEST SET.



(a)



(b)

[illegible]. 3.36 MIC[illegible] [illegible]/[illegible] [illegible]. [illegible] 1[illegible]0 mA
AN[illegible] [illegible] mA. (20-dB [illegible] INCLUDED)

3.2.4.5 Comparison of predicted and measured combiner performance. It is of interest to compare the measured two-diode combiner with that of a single device as characterized in the combiner circuit. Since the transformed properties of the two devices add in parallel at the combining point, halving the impedance of a single device should result in a prediction of two-diode operation. The measured and calculated small-signal impedances for the two-diode combiner is shown in Fig. 3.37. The data is given for a bias current of 90 mA with the calculated impedance obtained by using one-half the measured impedance of a single device. As is evident in Fig. 3.37, close agreement has been achieved. The measured data exhibits higher gain than predicted. This is due to coupling losses when the single device was measured in the two-diode combiner circuit. The closely spaced microstrip combining lines allowed coupling to occur and lowered the effective gain achievable with a single device.

A comparison of the generated power capability of the two-diode combiner and the single device clearly verifies the power-summing function. The maximum generated power measured for a single device was approximately 45 mW at a level of 22 dBm of input power. The maximum generated power measured for the two-diode combiner was 135 mW at 22 dBm of input power. The level measured for the single device obtained under low gain conditions is, therefore, more sensitive to circuit losses. Nevertheless, improved performance in terms of added power is shown for two-diode combiner operation. Moreover, the stable operation of this combiner design has verified the improved power capability over a single device.

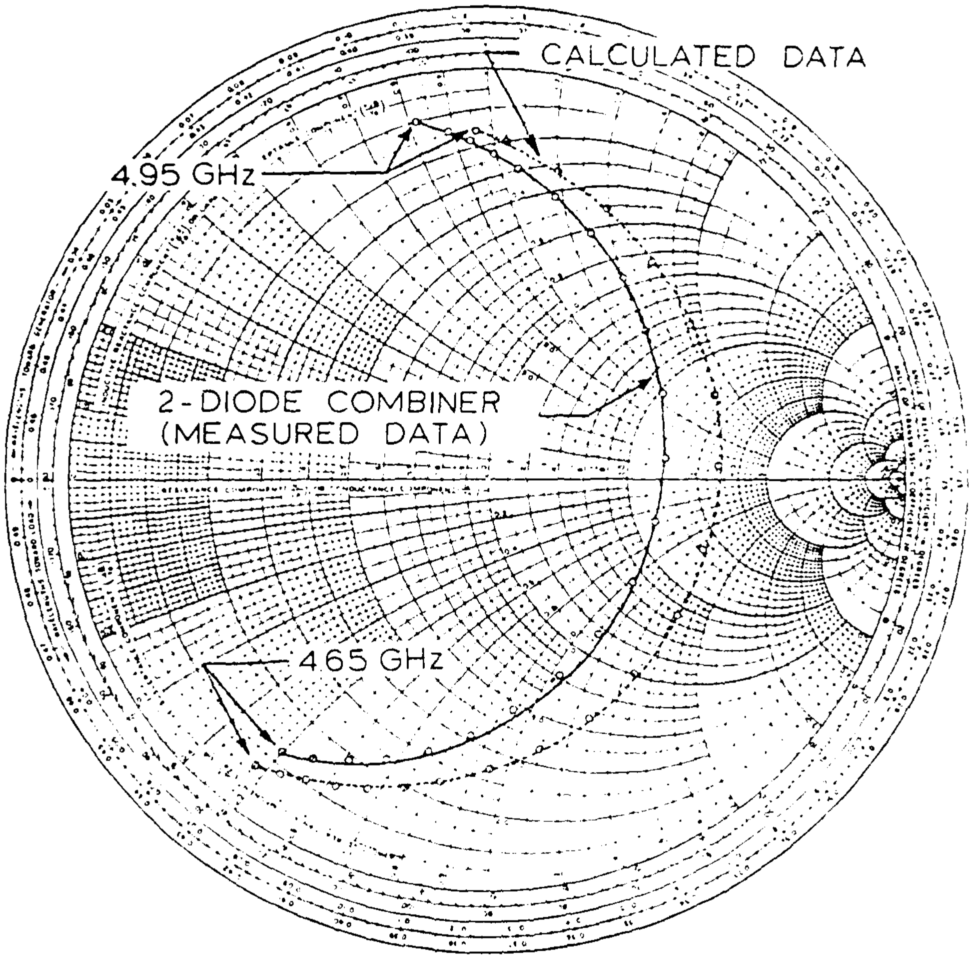


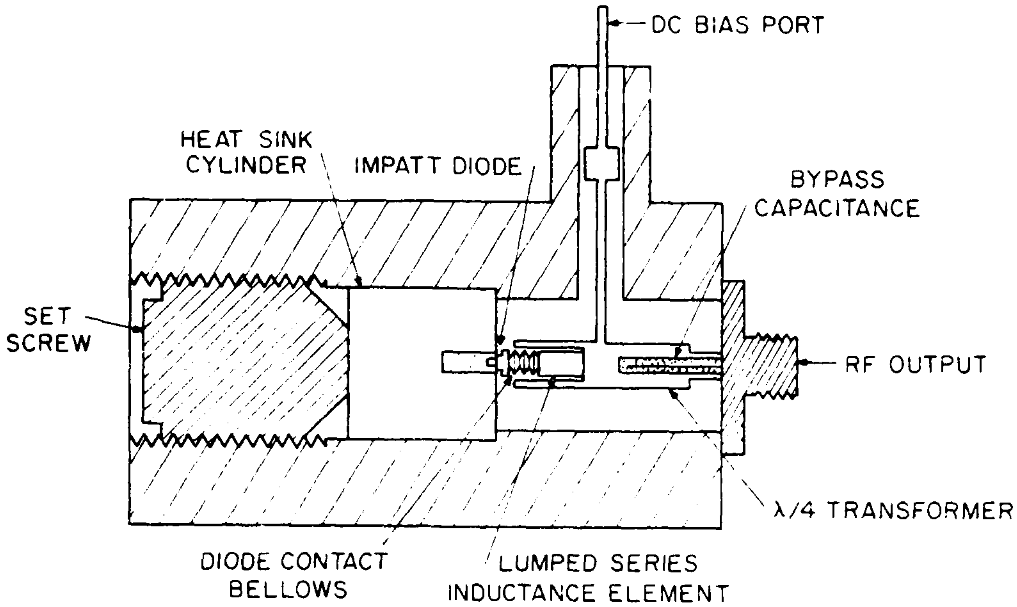
FIG. 3.37 TWO-DIODE COMBINER CHARACTERISTICS.

3.3 Coaxial IMPATT Diode Combiner Example

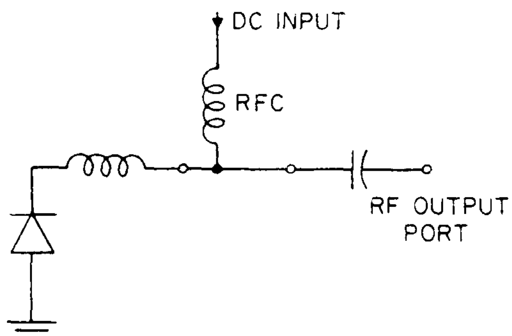
This section presents another verification of the combining approach. A lossless TEM line coaxial power combiner was realized from device characterization measurements of diodes in various coaxial test circuits.[19] The development of a stable coaxial combiner is described. Pulsed Si double-drift IMPATT diodes were once again used as the combiner devices. The IMPATT diode specifications of the combiner devices are indicated in Appendix C.

3.3.1 Single Device Test Circuit and Diode Characterization Results. A single-diode coaxial circuit was designed and constructed for use in measuring the active diode impedance and bandwidth properties of the available IMPATT devices. The circuit which is illustrated in Fig. 3.38a along with a simple electrical equivalent circuit which is shown in Fig. 3.38b was used to establish the proper design criteria for a stable multiple device combiner circuit.

The test fixture of Fig. 3.38 consists of a coaxial transmission line in which the center conductor functions as a quarter-wave impedance transformer. At a center frequency of approximately 4 GHz, the coaxial line transforms a 50-Ω impedance level at the RF output port to approximately a 6-Ω impedance level at the diode plane. The lower impedance value provides an improved match to the inherently low impedance associated with packaged IMPATT devices. Included in the test fixture center conductor are: (1) a series inductance lumped element which resonates the diode/package capacitance for proper impedance transformer operation; (2) a series bypass capacitor, realized by an open section of transmission line in series with the coaxial center conductor, providing a dc block to the output port; and (3) a single-section low-pass filter to supply



(a)



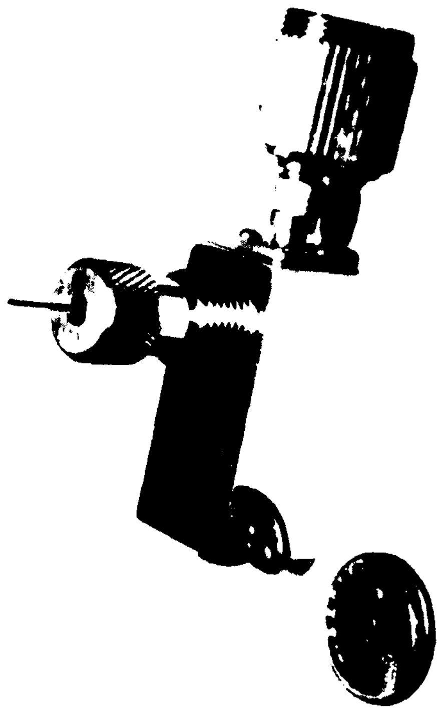
(b)

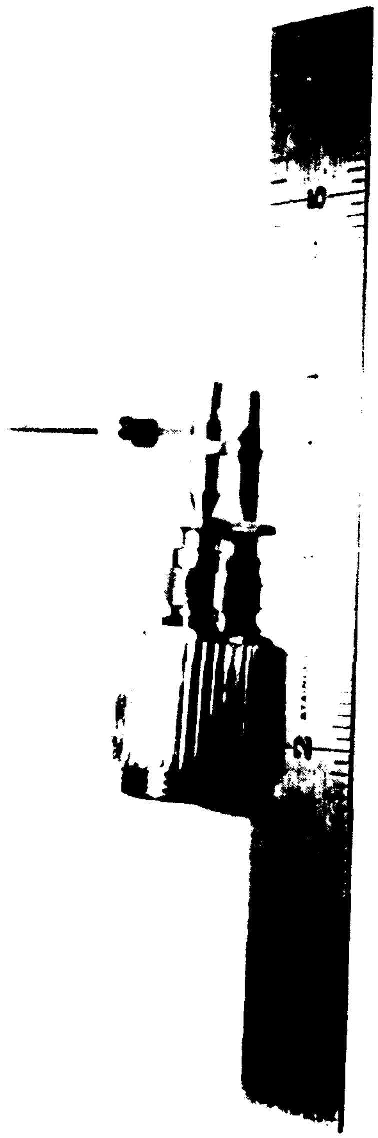
FIG. 3.38 COAXIAL TEST CIRCUIT. (a) CROSS-SECTIONAL VIEW AND (b) EQUIVALENT CIRCUIT.

dc bias to the diode and prevent RF leakage. The IMPATT device is soldered into a cylindrical copper heat sink and the entire coaxial assembly is held securely in place with a set screw. Photographs of the test fixture and inner assembly appear in Figs. 3.39 and 3.40, respectively.

Device characterizations of diodes in the coaxial test circuit of Fig. 3.38 have provided active-diode impedance and bandwidth information to realize a combiner circuit. Figures 3.41 and 3.42 illustrate typical device small-signal reflection gain and impedance referenced at a *measurement* plane corresponding to the combining point of a multiple device circuit. The data is shown as a function of frequency and bias current level. It is apparent from Fig. 3.42 that the IMPATT devices measured in the coaxial test circuit exhibit a large active bandwidth phase variation. Such a large phase variation was not observed in earlier microstrip test circuits and can be indicative of this circuit having more stored energy than previous circuits.

The impedance information presented in Fig. 3.42 corresponds to the active-diode impedance rotated through a section of TEM line as indicated in Fig. 3.43. The circuit design constraints required to suppress odd-mode combiner instabilities can be determined by examining the stability of the device-circuit situation suggested by Fig. 3.43. That is, the intersection of the rotated device impedance with the short-circuit impedance must be avoided. This constraint is not met in the device curve of Fig. 3.42. The possibility exists that under large-signal conditions, the device curve will intersect the short-circuit impedance point on the Smith chart. A solution to this problem can be found by reducing the active-device





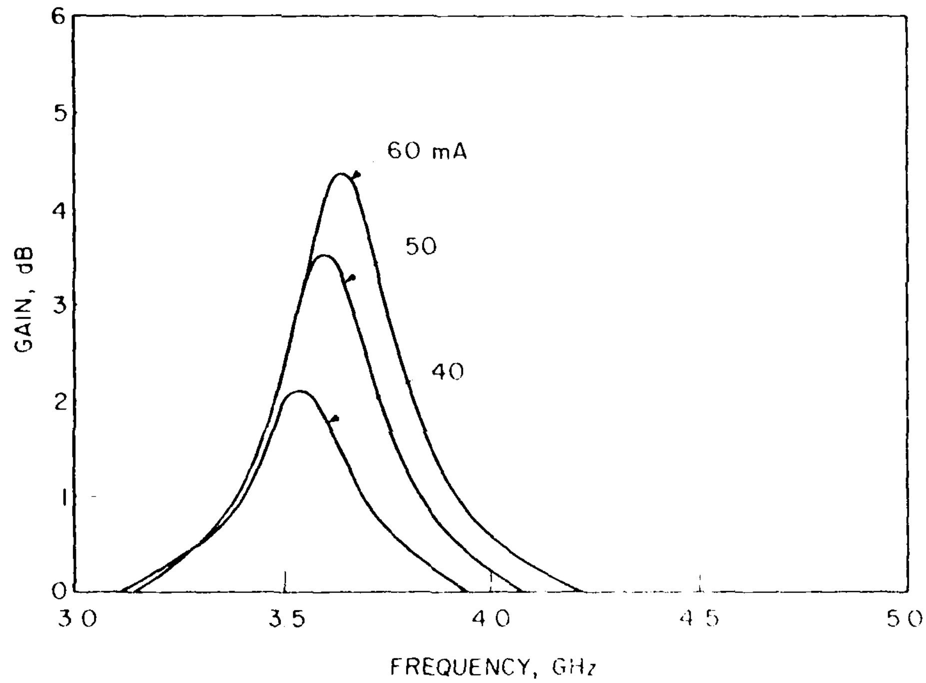


FIG. [illegible]

[illegible]

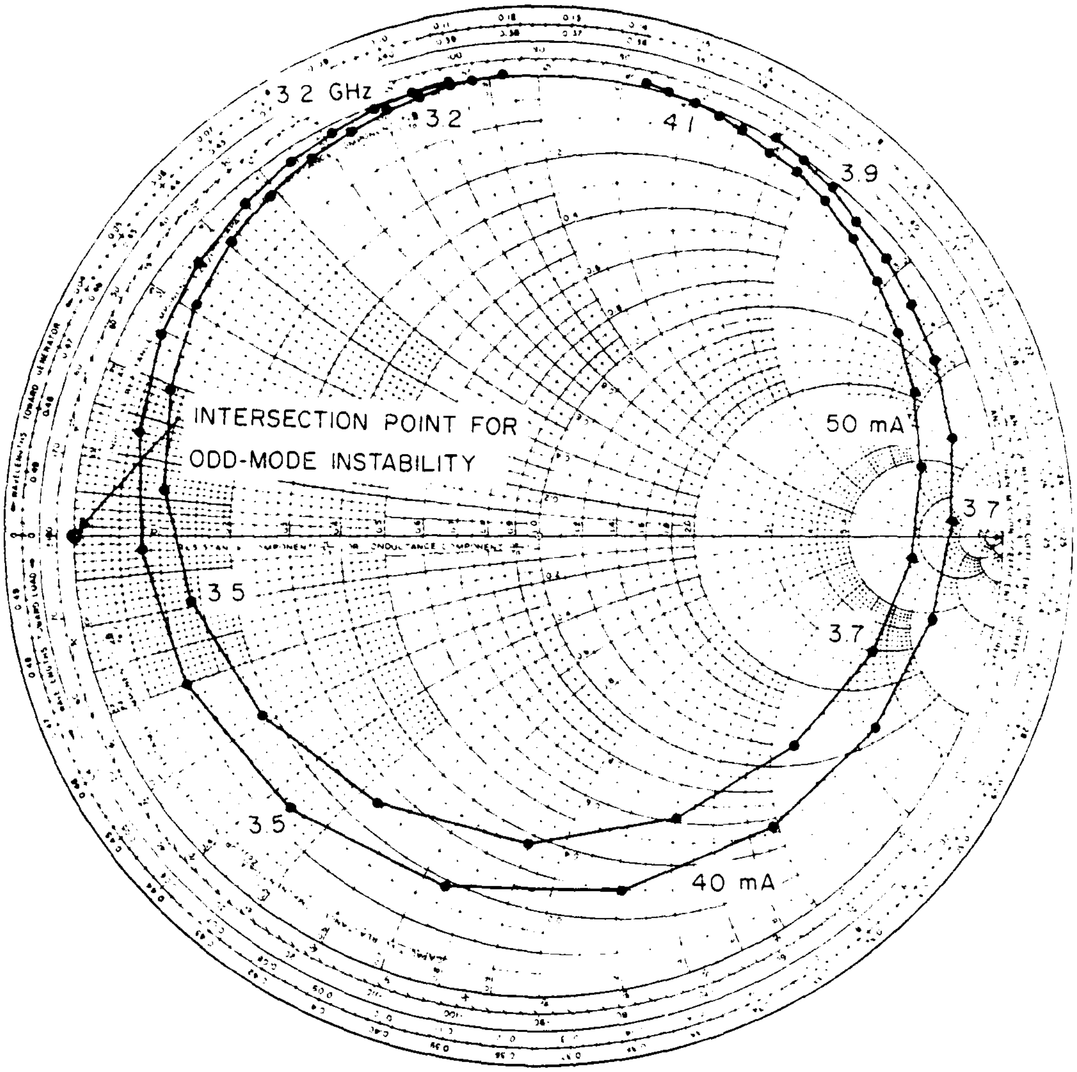


FIG. [illegible] DEVICE IMPEDANCE DATA $Z_d(\omega,I)$ OBTAINED FROM THE COAXIAL TEST CIRCUIT. DATA IS PLOTTED IN INVERSE REFLECTION COEFFICIENT PLANE, NORMALIZED TO 50 Ω, AND [illegible] A TEM COMBINING LINE.

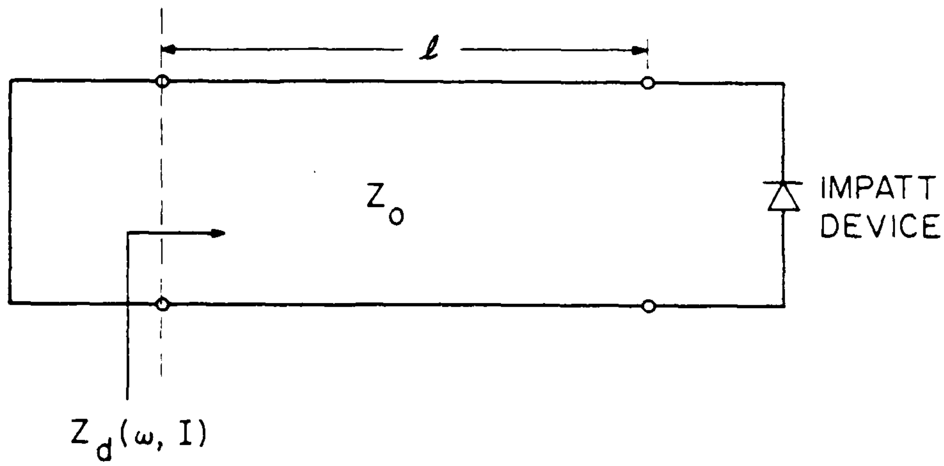
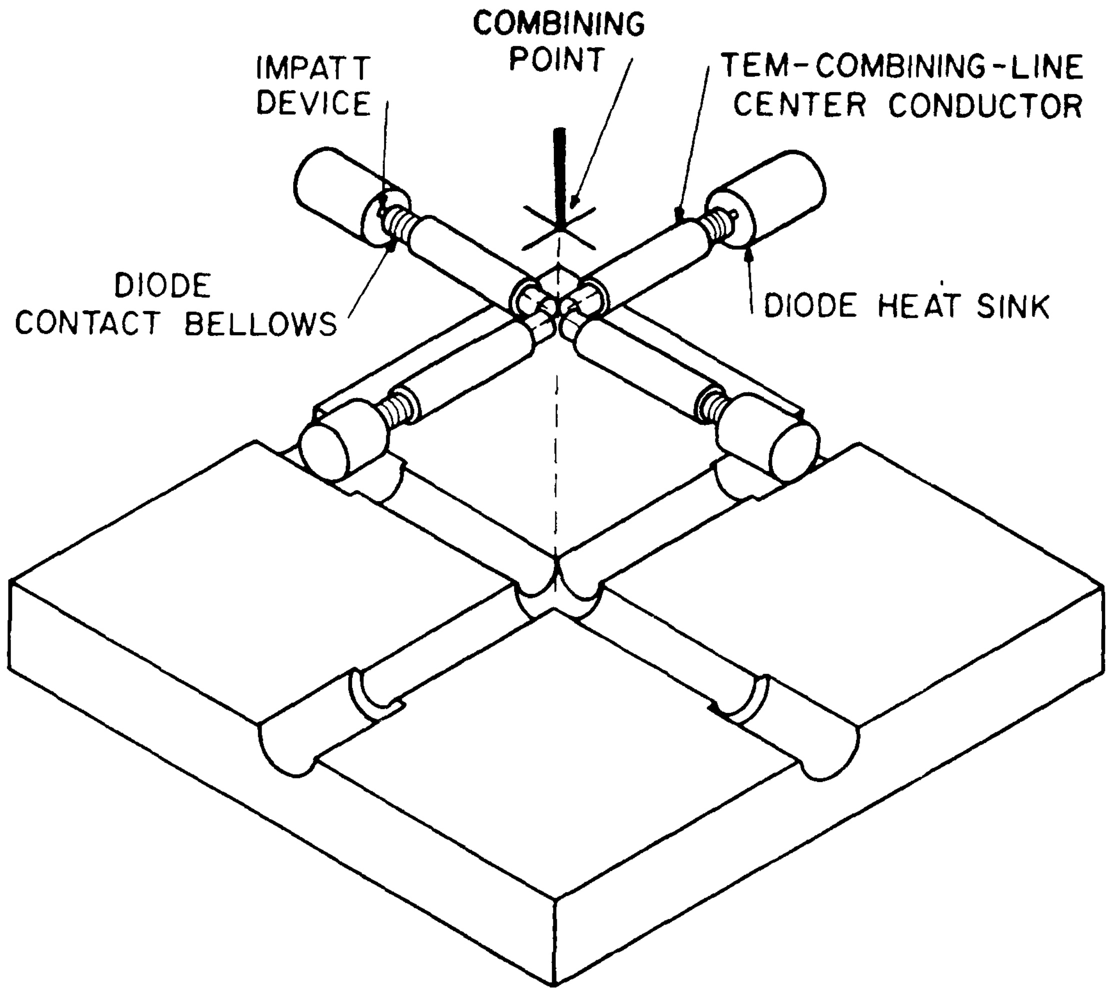


FIG. 2.43 IMPATT DEVICE WITH TEM LINE TRANSFORMATION. THE DEVICE-CIRCUIT INTERACTION SHOWN CAN LEAD TO COMBINED ODD-MODE INSTABILITIES.

phase variation or alternately adding series reactance to the device impedance to rotate the diode impedance curve to a position where the active device curve will not intersect the short-circuit impedance point.

<u>3.3.2 Coaxial Combiner Test Circuit and Characterization Results</u>. The single-diode coaxial test circuit was used as a tool to design a coaxial IMPATT diode combiner test fixture. An initial version of the coaxial combiner is partially shown in Fig. [illegible]. The combiner was initially designed to accommodate up to four IMPATT devices. However, due to the availability of primarily dissimilar devices, only a two-diode realization was attempted. The four-way junction at the combining point was replaced with a two-way junction. The unused coaxial transmission lines, deprived of a center conductor, function as cut-off circular guides with a cut-off frequency of 13 GHz, well above the design operating frequency. Their effect on the combiner circuit is to provide a reactive termination at the combining point which is not expected to affect the stability of the combining operation.

Although the combiner circuit is essentially a four-way copy of the single-diode coaxial circuit, shorter sections of combining line length were used to achieve more desired device characteristics when impedance data were rotated to the combining point. The desire was to reduce as much as possible the amount of active device phase variation without major redesign of the combiner test fixture. Such modifications, of course, can only be obtained at the expense of


COMBINING POINT
IMPATT DEVICE
TEM-COMBINING-LINE CENTER CONDUCTOR
DIODE CONTACT BELLOWS
DIODE HEAT SINK

reduced gain and obvious shift in the center frequency of the quarter wavelength impedance transformer.

Measurements of individual diodes in the coaxial combiner circuit established the active-device gain and bandwidth properties of diodes in the combiner circuit. Figure 3.45 illustrates the typical small-signal device impedance referenced to the combining point. In spite of shorter combining line length, the active-device phase variation is still too large. This may be partly due to the larger stored energy capacity of the four-way circuit over the single-diode circuit. Figure 3.46 shows the device small-signal reflection gain corresponding to Fig. 3.45. Two observations are evident from the figures: (1) additional circuit modification is required to decrease the still-too-large active-device phase variation; and (2) the maximum device gain occurs at a higher frequency in the combiner circuit than in the single diode circuit. Gain is still observed at 3.6 GHz (where maximum gain occurred for devices in the single-diode circuit); however, it is greatly reduced. The differences in frequency of maximum gain may be attributed to the cut-off guide reactances of the unused combining lines. These reactances may tune the combiner circuit for maximum gain at the higher frequency.

Additional reduction in active diode phase variation was obtained by replacing the diode contact bellows with a series [illegible] inductance, a short section of slightly higher impedance line (lumped inductance of 0.4 nH). The absence of the contact bellows necessitated close machining tolerances to achieve good diode-transformer contact without device destruction. In addition, the series by-pass capacitance was increased for each combining line

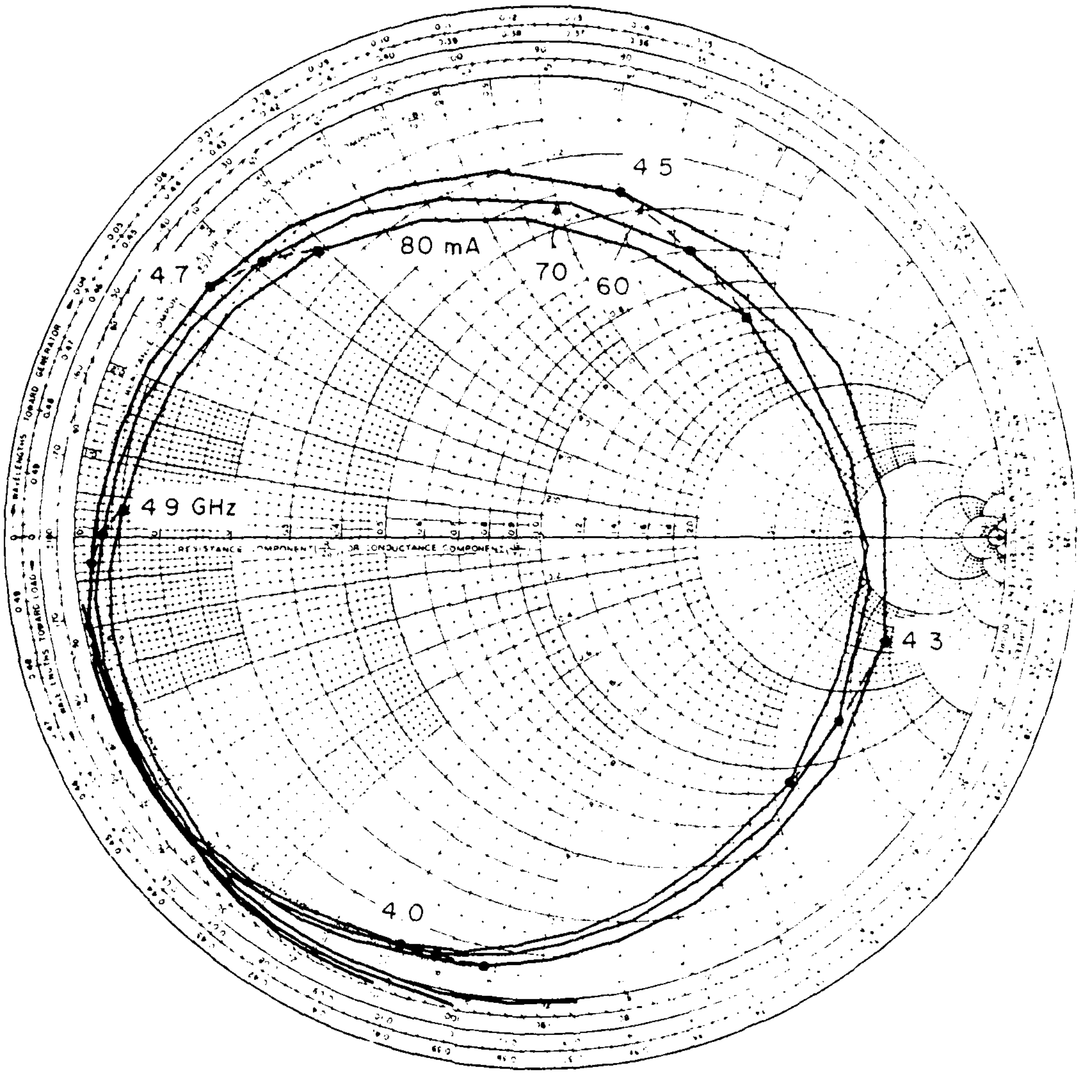


FIG. 3.46 SINGLE-DIODE IMPEDANCE AT [illegible]
CIRCUIT. DATA IS PLOTTED IN THE [illegible]
COEFFICIENT PLANE, [illegible] THE [illegible]
AND NORMALIZED TO [illegible].

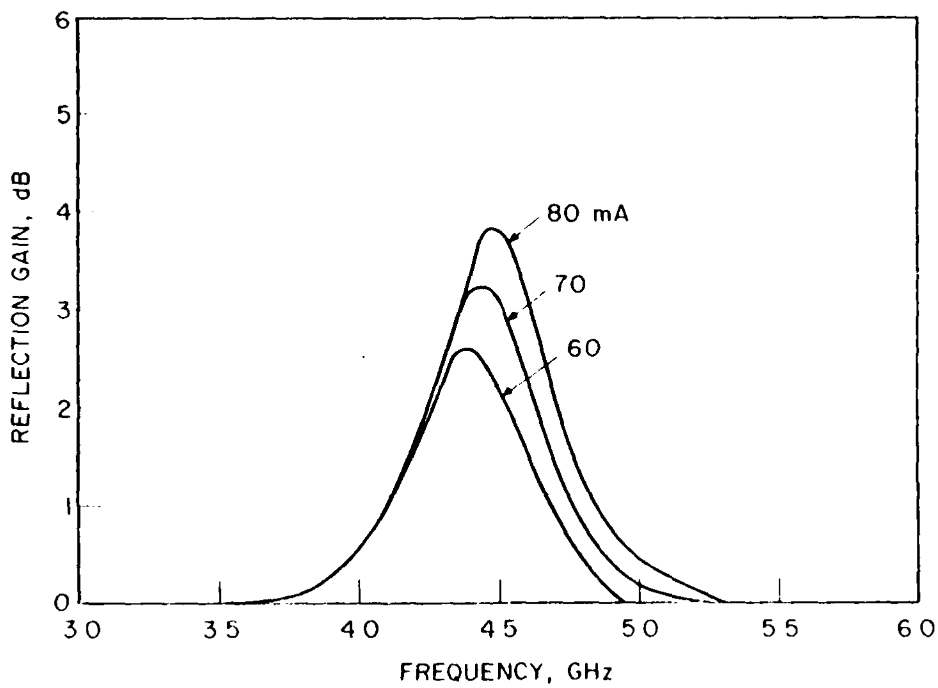


FIG. 3.46 REFLECTION GAIN OF A TYPICAL DEVICE AS MEASURED IN THE COAXIAL COMBINER CIRCUIT. (DATA CORRESPONDS TO THAT IN FIG. 3.45.)

line to rotate the diode curve to a position where odd-mode instabilities could be avoided. The results of these additional circuit modifications can be seen in the measured gain and impedance characteristics shown in Figs. 3.47 and 3.48. The data shown are again referenced to the combining point and illustrates the reduced active-device phase variation with an accompanying reduction in gain. The diode curve shown in Fig. 3.48 prohibits the possibility of a large-signal intersection of the diode curve with the short-circuit point on the Smith chart. The fact that this combiner circuit successfully provided stable two-diode combiner operation verifies the proper circuit design.

The coaxial two IMPATT diode combiner which successfully combined power from two devices is shown in Figs. 3.49 through [illegible]. Individual device bias control similar to that found in the single-diode coaxial circuit is provided. The transformers are tapered to provide the closest placement of each combining line to the combining point. Fine adjustment in achieving [illegible], in the absence of contact bellows, is obtained with fine thread screws drilled into the original set screws.

3.3.2 Two-Diode Combiner Characterization Results. The measured small-signal combiner impedance and reflection gain are shown in Figs. 3.52 through 3.54 for a two-diode version of the coaxial combiner. Two regions of peak gain can be observed. One region is centered around [illegible] GHz and is predictable from previous single-diode measurements of devices in the combiner circuit. The second region of gain occurs near [illegible] GHz. [illegible] not predicted from single-diode combiner circuit measurements,

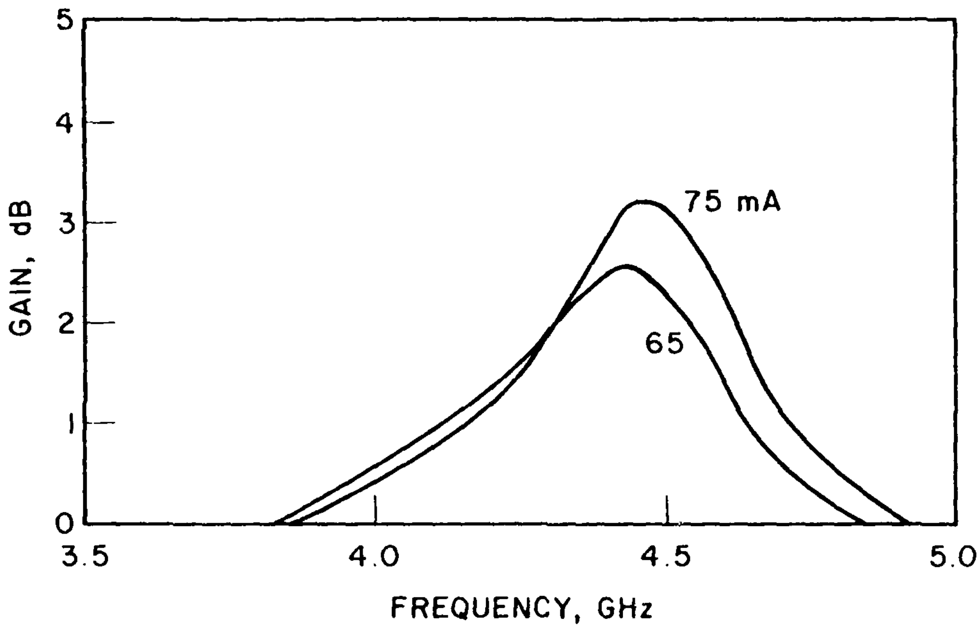


FIG. 3.47 SMALL-SIGNAL REFLECTION GAIN OF SINGLE DEVICE IN THE COAXIAL COMBINER CIRCUIT AFTER SHORTENING OF COMBINING LINE LENGTH.

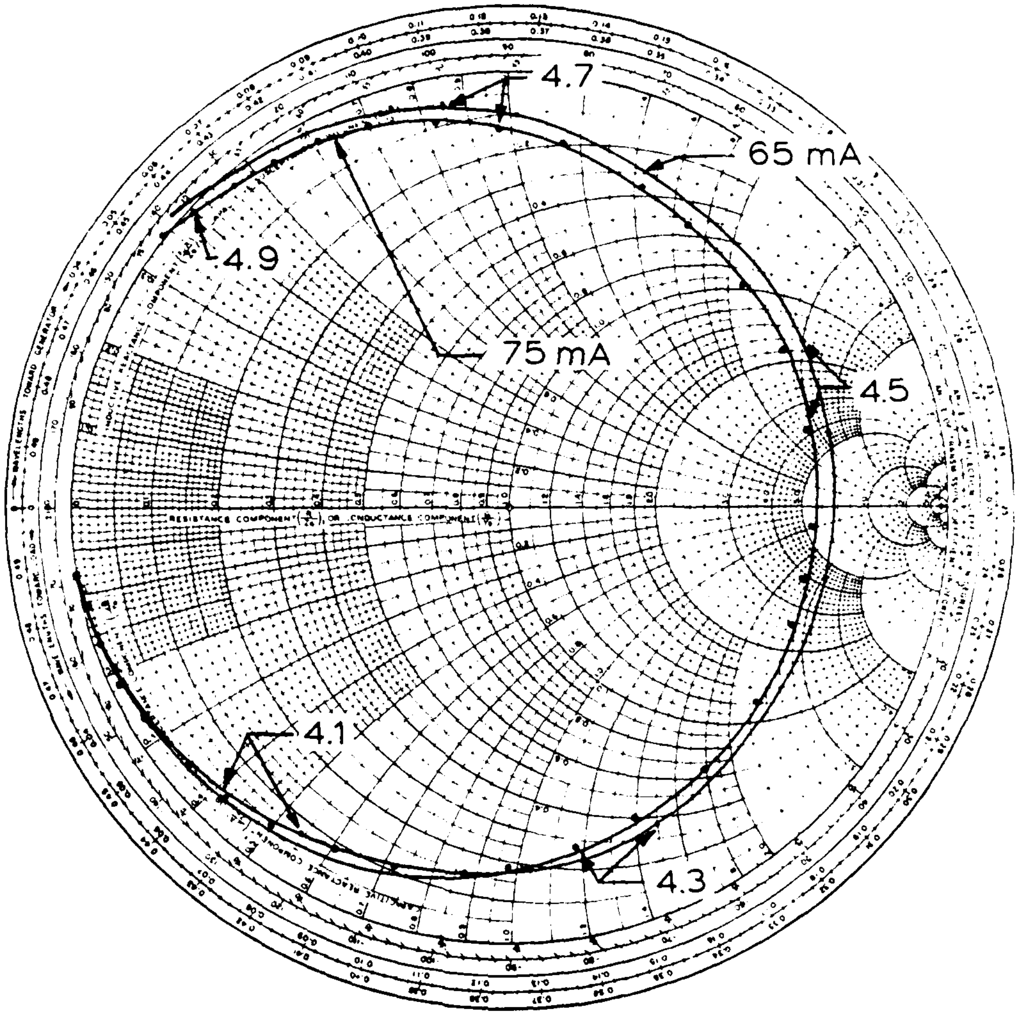
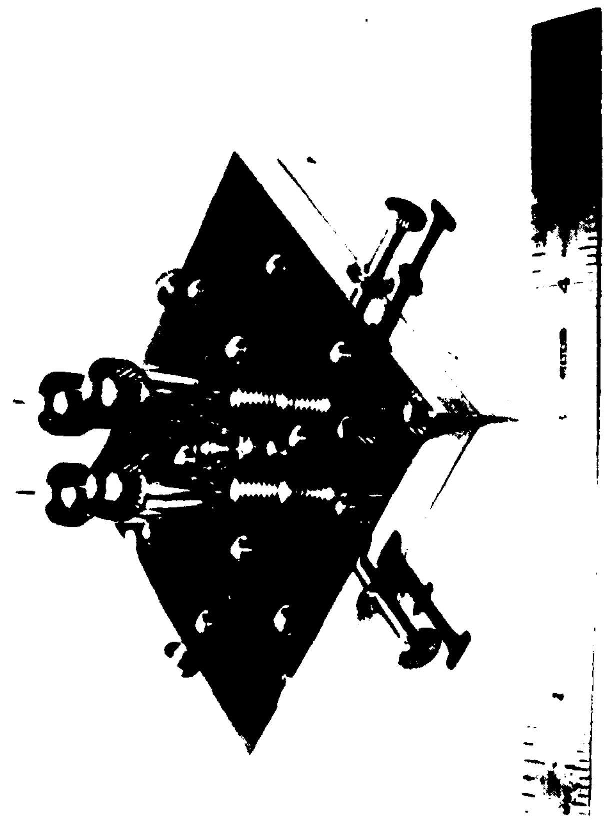
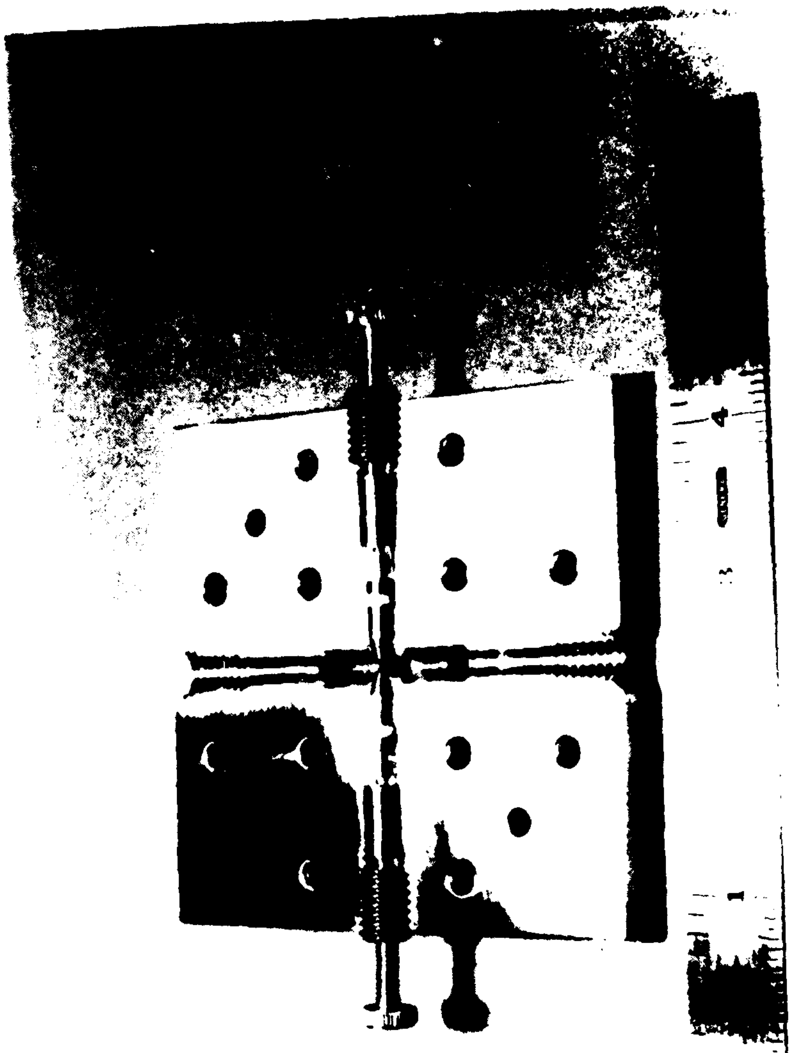
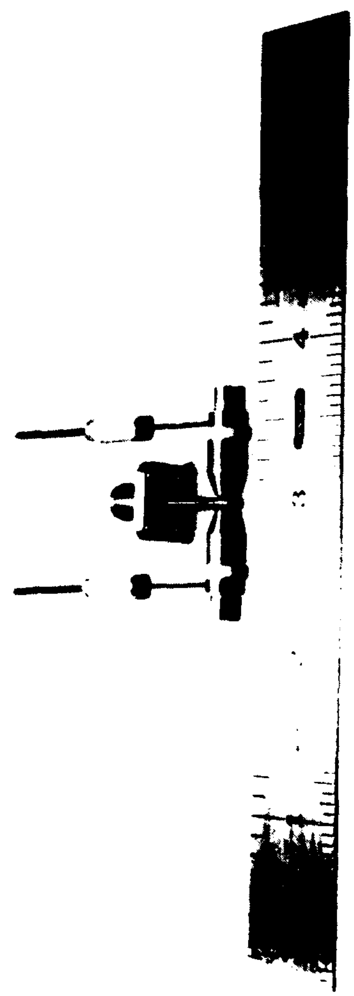


FIG. 3.48 MEASURED SMALL-SIGNAL IMPEDANCE [illegible]
MEASURED IN THE COAXIAL COMBINER [illegible]
THE COMBINING LINE LENGTH. DATA [illegible]
COMBINING POINT AND NORMALIZED [illegible].







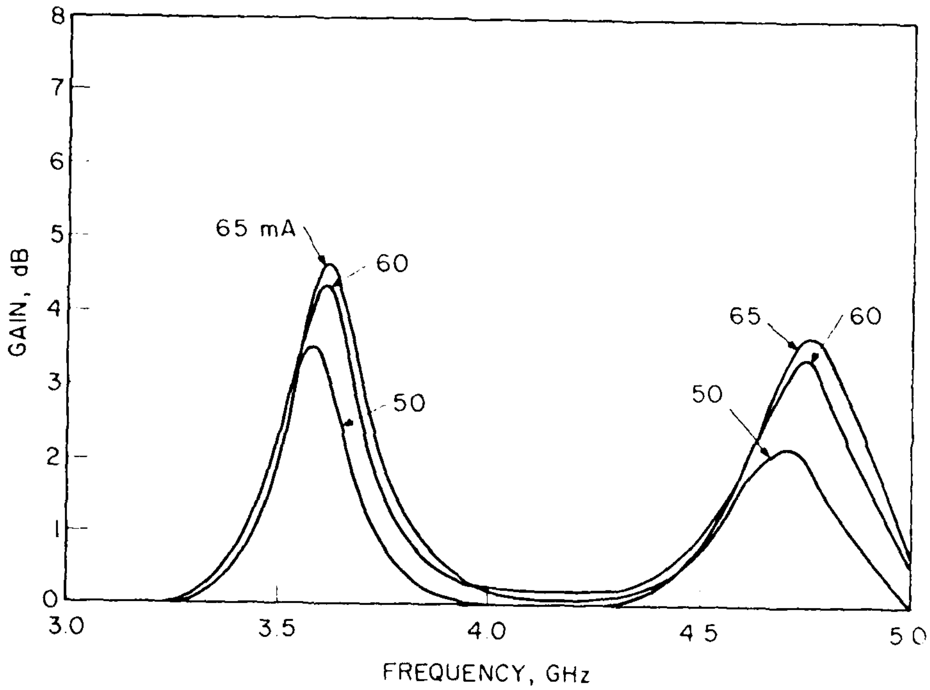
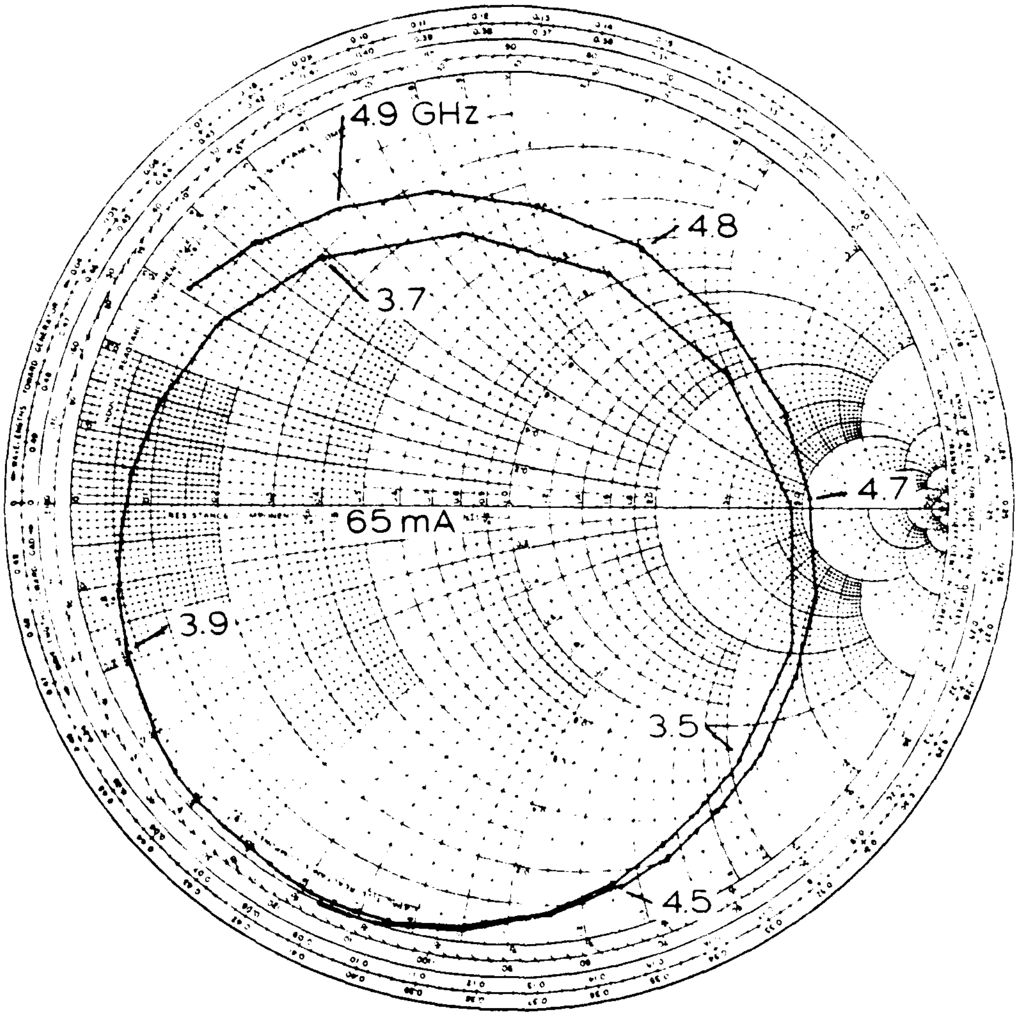
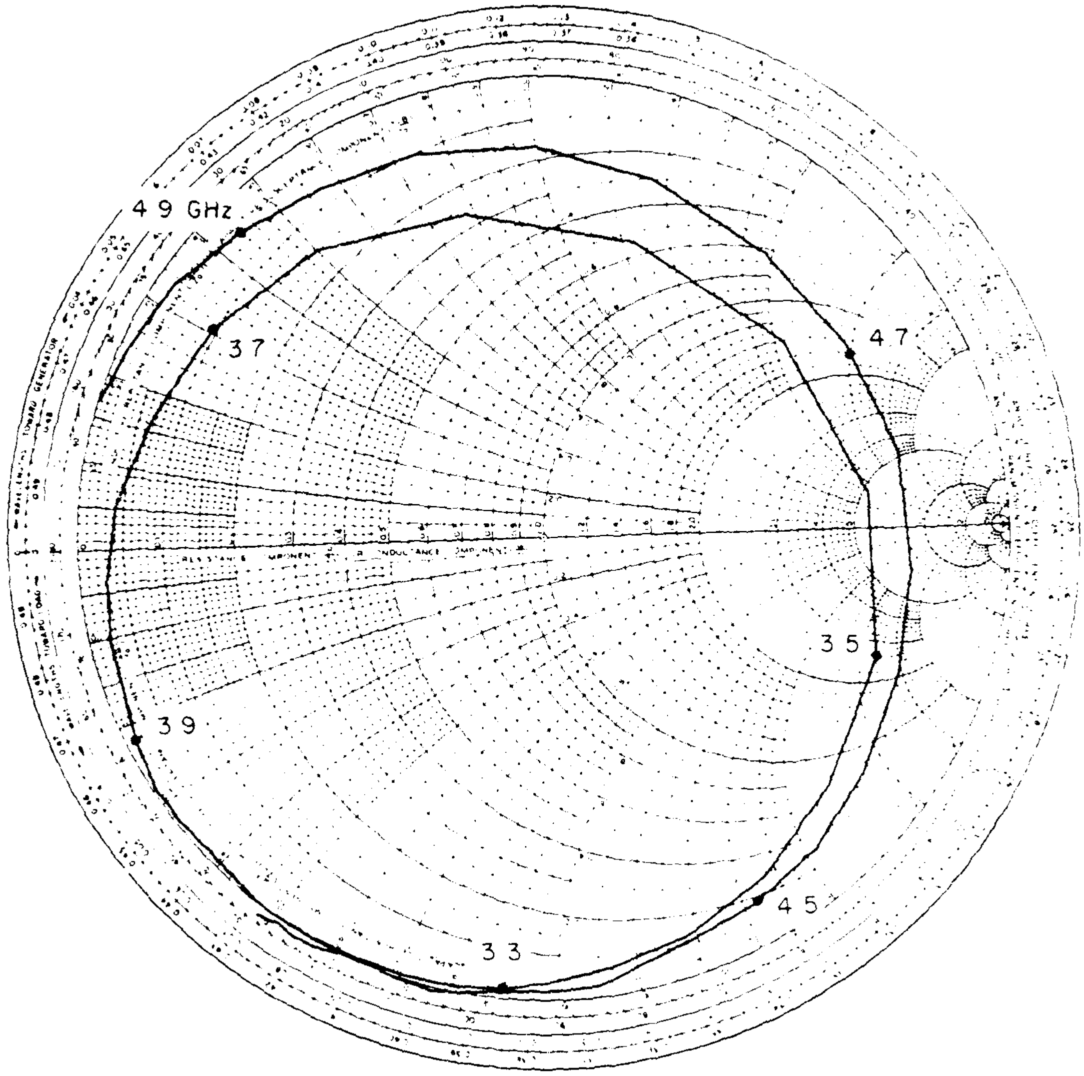


FIG. [illegible] SMALL-SIGNAL REFLECTION GAIN [illegible]
COMBINER ([illegible] mA BIAS CURRENT).



4.9 GHz
4.8
3.7
4.7
65 mA
3.9
3.5
4.5


4 9 GHz
4 7
3 7
3 5
3 9
4 5
3 3

[illegible]
[illegible]
[illegible]

although small levels of gain at [illegible] GHz were observed in Fig. 3.46 before combining line length was reduced. This phenomenon can be attributed to the circuit reactances introduced by the four-way configuration. The combiner circuit is apparently tuned in two frequency regions where the devices are active.[26] This quasi-double gain region does appear to offer a considerable improvement in operating bandwidth. In Figs. 3.53 and 3.54 the combiner small-signal active impedance is observed to "wrap around" itself before becoming passive again. This is due to the combiner remaining active over the large frequency range (for bias currents above 50 mA).

The coaxial combiner circuit was also characterized under large-signal conditions. Figure 3.55 illustrates the experimental test set. An automated system could not be utilized for these measurements because of frequency limitations with the TWT. Originally designed to operate from [illegible] to 12 GHz, the TWT provided insufficient power levels at lower frequencies requiring manual synthesizer adjustments to obtain suitable input power levels. The network analyzer phase-gain display was substituted for a polar display to more accurately obtain gain information.

Large-signal combiner characterization results are shown in Figs. 3.56 through 3.59 for an operating current bias of 75 mA. Reflection gain and combiner generated power (added power) are shown as functions of frequency and input power level. Maximum generated power for two-diode operation was measured at 180 mW at 3.7 GHz. At 4.7 GHz, generated power was 100 mW. For the purpose of comparison, the single-diode generated power as a function of frequency is shown in Fig. 3.60. At approximately 4.4 GHz, [illegible] mW of added power

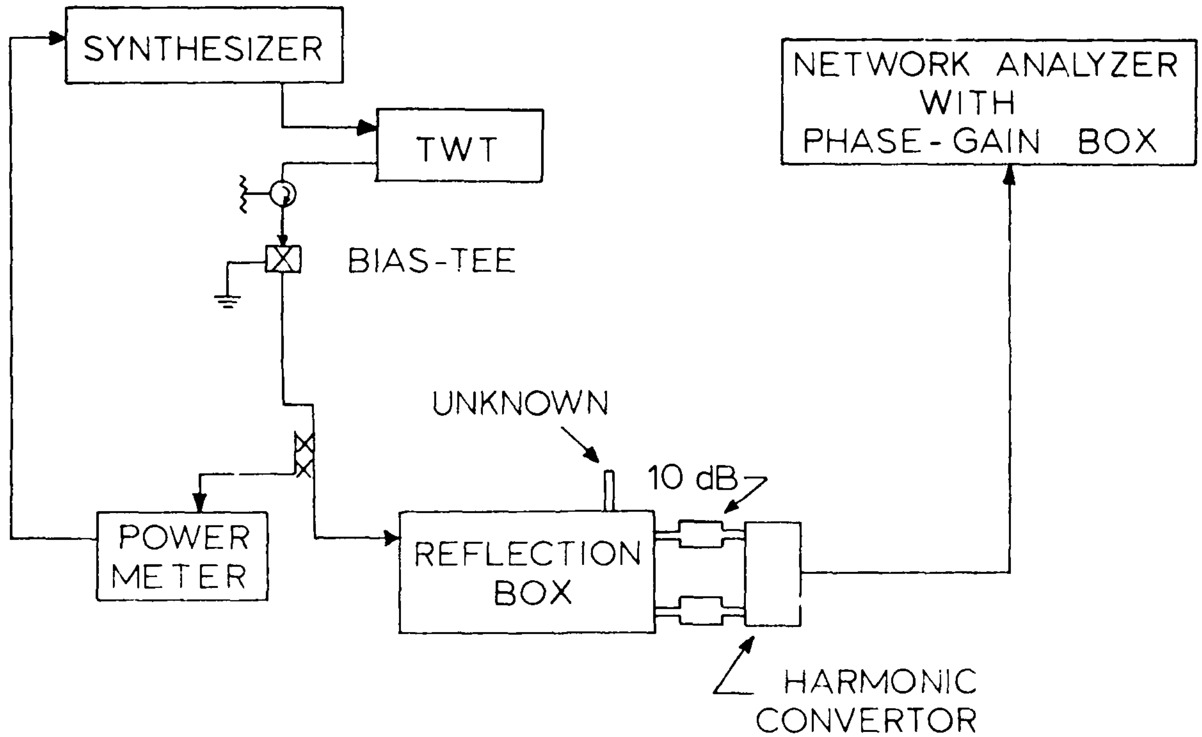
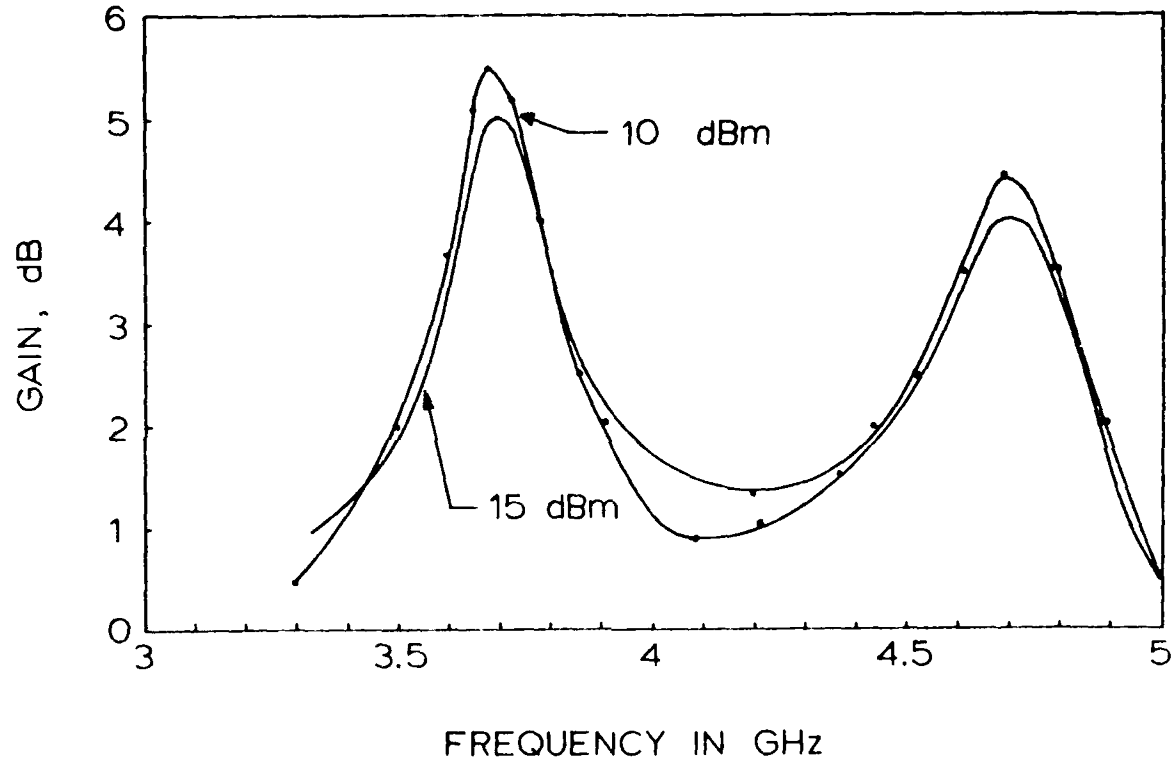
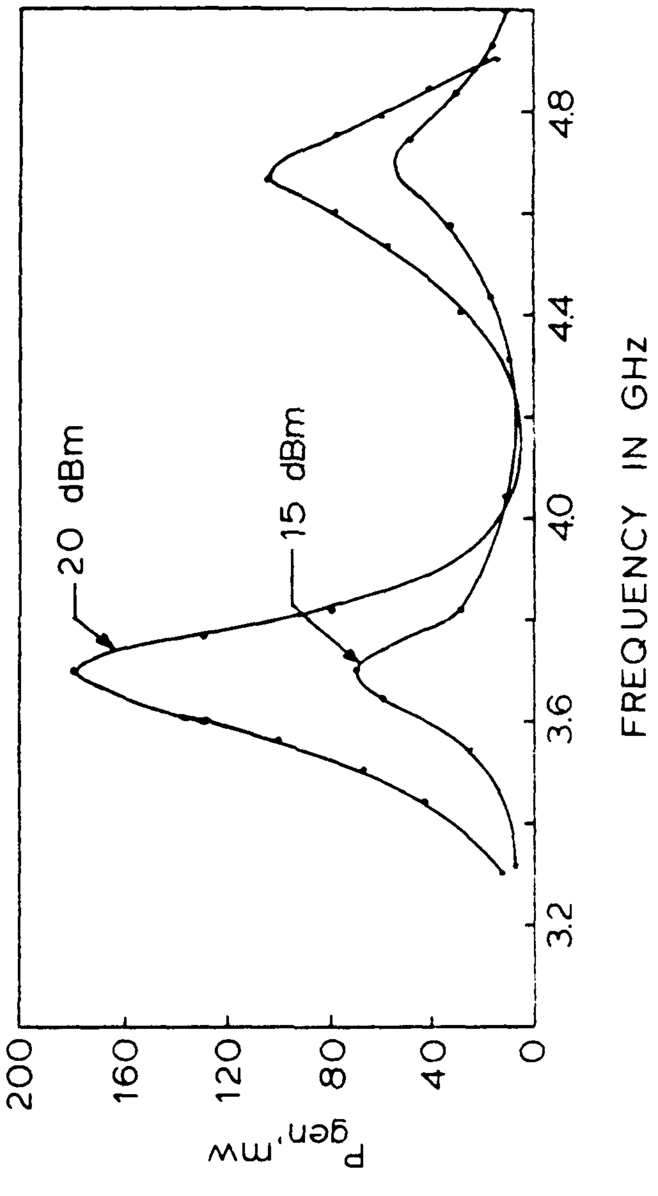


FIG. 3.[illegible] LARGE-SIGNAL TEST SET USED IN CHARACTERIZATION MEASUREMENTS

FOR THE [illegible] [illegible].


10 dBm
15 dBm
GAIN, dB
FREQUENCY IN GHz
0
1
2
3
4
5
6
3
3.5
4
4.5
5



20 dBm
15 dBm
P_{gen}, mw
FREQUENCY IN GHz
200
160
120
80
40
0
3.2
3.6
4.0
4.4
4.8

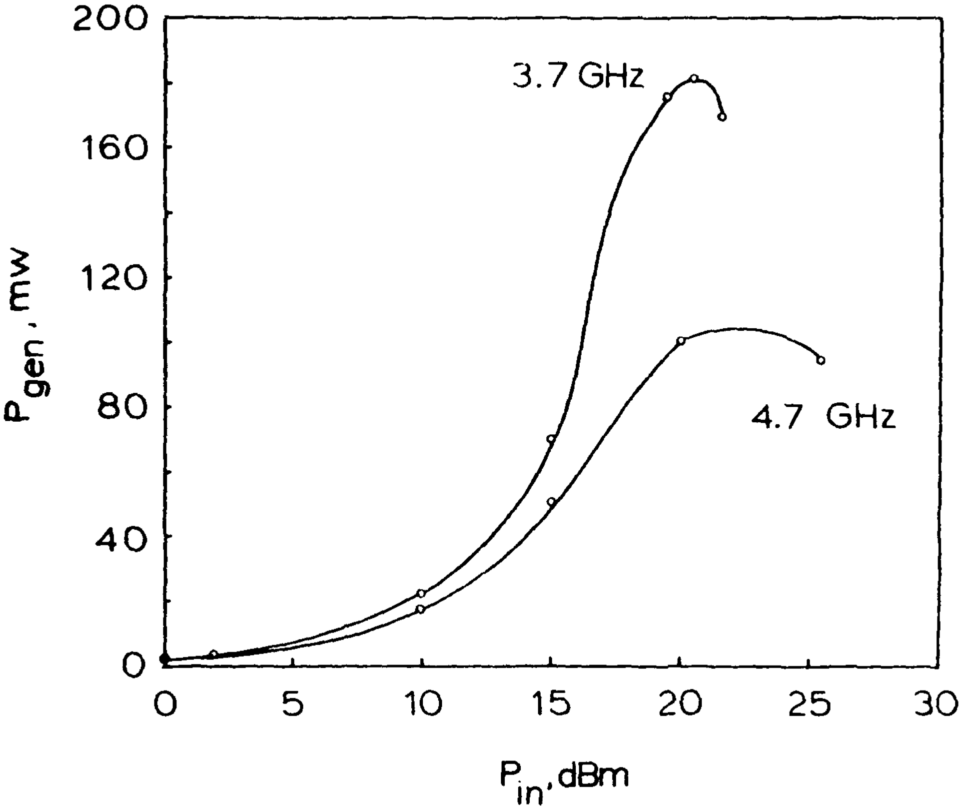


FIG. 3.58 TWO-DIODE COAXIAL COMBINER LARGE-SIGNAL DATA AT 75 mA CURRENT BIAS.

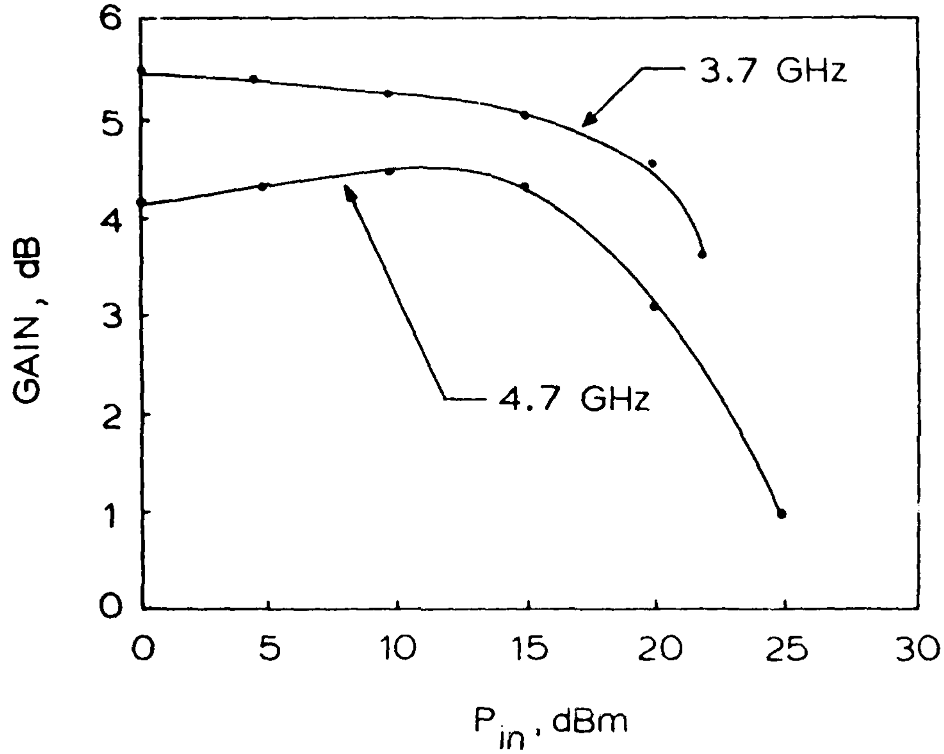


FIG. 3.59 TWO-DIODE COAXIAL COMBINER LARGE-SIGNAL [illegible]
CURRENT BIAS, ERROR ± 0.[illegible] dB.

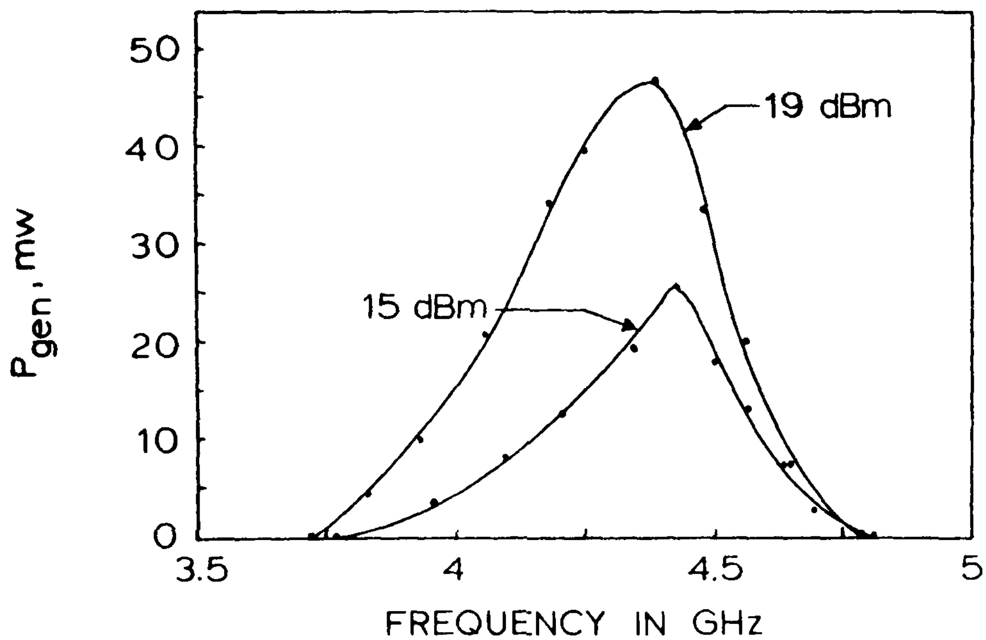
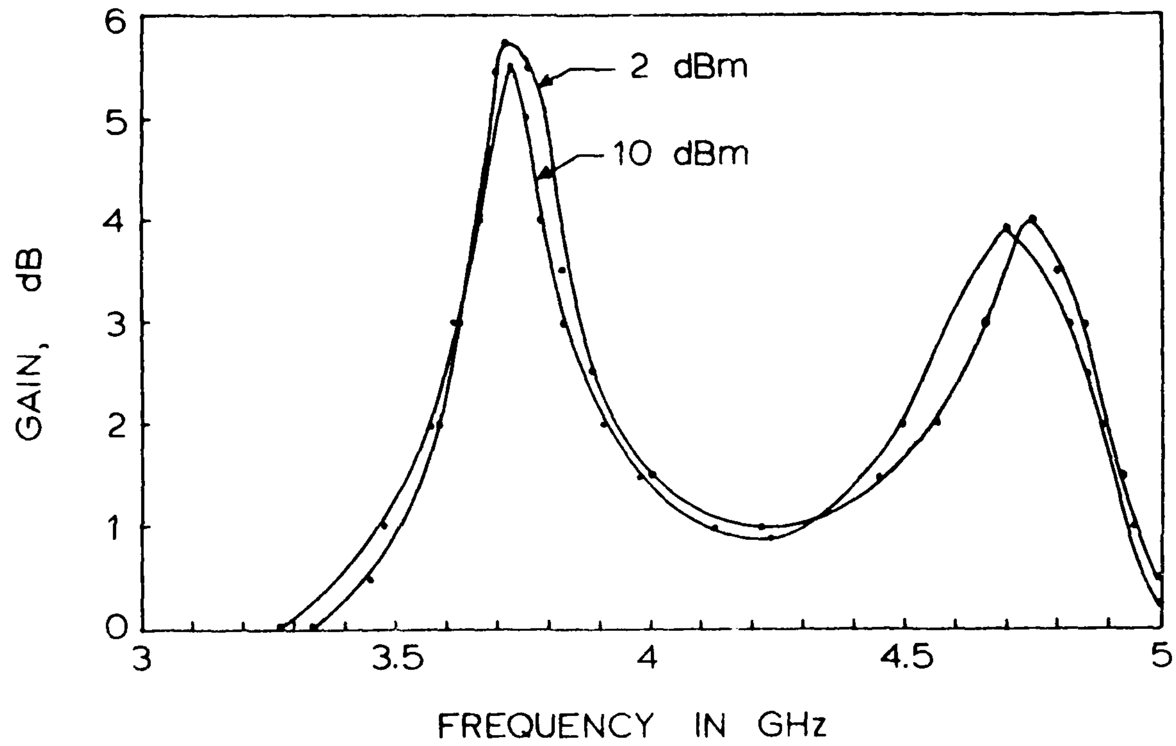


FIG. 3.60 GENERATED POWER RESULTS OF A SINGLE DEVICE AS MEASURED IN THE TWO-DIODE COAXIAL COMBINER CIRCUIT (75 mA CURRENT BIAS).

was observed. This corresponds to one-half of the 1[illegible] mW [illegible] power measured for the two-diode combiner at 4.[illegible] GHz, indicating [illegible] combining efficiency (9[illegible] percent). Figures [illegible] and [illegible] illustrate gain and generated power results for a bias current of [illegible] mA. Difficulties in obtaining adequate input power levels limited the amount of data gathered.

Table 5.1 summarizes some of the gain and bandwidth properties of the coaxial combiner. Locking bandwidths of [illegible] 16 percent were observed. For the [illegible] mA current bias [illegible], power levels of near 19.5 dB were [illegible].


2 dBm
10 dBm
GAIN, dB
FREQUENCY IN GHz
0
1
2
3
4
5
6
3
3.5
4
4.5
5

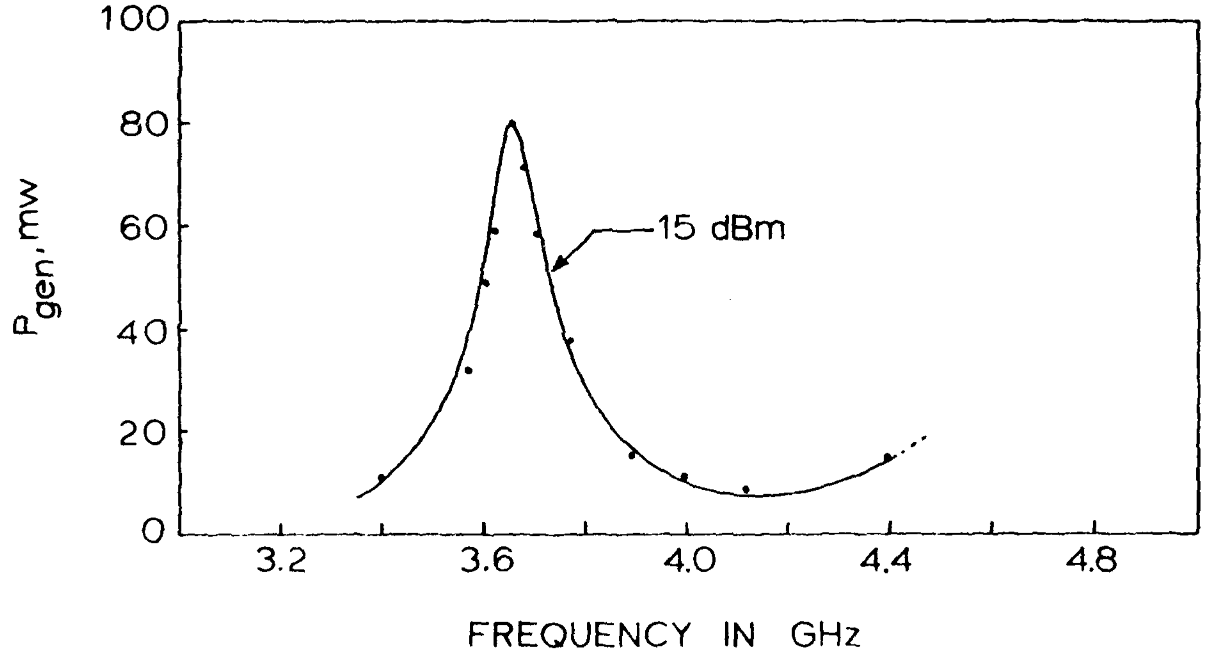

100
80
60
40
20
0
P_{gen}, mw
15 dBm
3.2
3.6
4.0
4.4
4.8
FREQUENCY IN GHz

Table 3.1

Summary of Coaxial Combiner Large-Signal Characterization Data

P_{in} (dBm)	I (mA)	Maximum Gain Frequency (GHz)	Lower 3-dB Frequency	Upper 3-dB Frequency	Fractional BW (Percent)	Gain
10	85	4.696	[illegible]	[illegible]	[illegible]	[illegible]
10	85	3.720	[illegible]	[illegible]	[illegible]	[illegible]
10	75	3.686	[illegible]	[illegible]	[illegible]	[illegible]
10	75	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
15	75	3.701	[illegible]	[illegible]	[illegible]	[illegible]
15	75	4.663	[illegible]	[illegible]	[illegible]	[illegible]
19.5	75	3.708	[illegible]	[illegible]	[illegible]	[illegible]
19.5	75	4.708	[illegible]	[illegible]	[illegible]	[illegible]

CHAPTER IV

SUMMARY AND CONCLUSIONS

4.1 Summary

The combining circuits studied in this investigation use lossless symmetric TEM line networks together with bandlimited IMPATT devices to realize stable combiners. This design approach differs from other approaches in that the device and circuit properties are closely intertwined and cannot be specified separately. The combiner can be thought of as an optimal "marriage" of device and circuit which suppresses undesired odd-mode instabilities without resistive stabilization.

In Chapter II of this report, the theory of this combining approach was reviewed. Normal modes of oscillation of the combiner system were determined from the network eigenvalues [illegible] the oscillation condition. From this analysis, [illegible] circuits were associated with the combiner [illegible]. Suppression of the undesired modes was achieved [illegible] circuit design.

Two examples of combiners that were developed and have successfully demonstrated the approach were presented. Each combiner utilized two IMPATT devices. One design was realized in microstrip and the other was developed for a coaxial circuit environment. The device selection and device characterization [illegible] was also described.

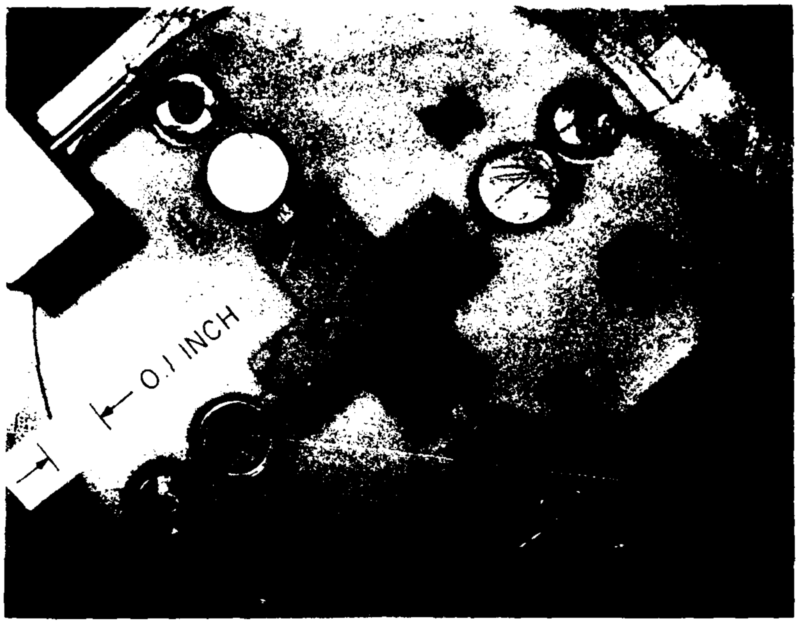
The microstrip and coaxial combiners were described in Chapter III. Both combiners provided stable, nonspurious combiner/amplifier performance. The microstrip design exhibited a bandwidth of 4.6 to 4.9 GHz. Ten dB of small-signal reflection gain at 4.85 GHz (100 mA bias current) was observed. A [illegible] percent 3-dB fractional bandwidth with [illegible] dB of gain at [illegible] GHz was obtained. This bandwidth could be increased if the large stability margin exhibited by the devices could be traded for more active bandwidth. Large-signal characterization demonstrated high efficiency combining (136 mW of added power for two-diode operation vs. [illegible] mW of added power for a single diode). The coaxial combiner provided an additional verification of the combining approach. The cylindrical geometry of the coaxial circuit was better suited to accommodate the packaged IMPATT devices. The devices in this combiner exhibited slightly larger active bandwidths than the devices used in the microstrip combiner with a stable bandwidth of [illegible] to [illegible] GHz. Peak gain ([illegible] dB) occurred near [illegible].7 GHz ([illegible] mA current bias). An added power of 180 mW was measured at 100 mW of input drive. A 3-dB fractional bandwidth of [illegible] percent was observed with 4.5 dB of gain.

4.2 Conclusions and Suggestions for Further Work

This work sought to experimentally verify a new approach to circuit level power combining of negative-resistance devices. The combining circuits developed have succeeded in demonstrating stable, nonspurious combiner operation. In this respect, the initial investigation goal of developing a stable combiner design has been achieved.

Due to equipment limitations and device availability, the IMPATT diodes used in the combiners were not optimally suited for combining applications of this type. Although this did not prevent realization of a stable design, it did, however, limit the combiner output power to lower levels. In future work with this combining approach it would be desirable to give more consideration to device selection particularly in terms of the trade-off between device power output and device impedance level. Since the purpose behind power combining is to obtain the highest power levels, it would appear that the best approach would be to select the highest power devices and combine a selected number of them. However, because of thermal limitations the use of such devices requires large diode area. This reduces the device impedance level and generally requires some form of matching circuitry to efficiently couple energy from device to circuit. The use of additional circuitry adds further stored energy to the circuit and may prohibit a stable design from being realized. Further work is required to determine the ramifications of a device impedance-device power capability trade-off. At this point, single-drift chip devices appear to be the most likely candidates for this combining approach.

This investigation has provided some useful groundwork for future experimental work using this combining approach. A logical direction for future studies would be to extend this approach in frequency, number of devices, and overall power output. To this end, a suggested design for a four-[illegible] is shown in Fig. 4.1. The lack of enough suitable devices prevented this design from being tested. Nevertheless, the circuit


0.1 INCH

[illegible]

demonstrates a useful technique for fabricating self-aligning concentric substrate vias. Prior to this design, hole vias (required for coaxial-to-planar transitions at the combining point) were drilled after the substrate board was cut. Due to ultrasonic impact drill limitations, this appraoch made it very difficult to accurately center the hole via on the circuit board. The problem was overcome by utilizing a concentric hole symmetry; the via drilling was performed simultaneously with the circuit board cutting (using a single, circular drill bit). Fabrication of circuit boards that require centered vias is made more straightforward by using this technique.

Hopefully, the experimental work accomplished in this study has led to a practical understanding of the device-circuit interactions involved in multiple device power combining. The successful results obtained with this approach will hopefully foster additional activity in extending the frequency, power output and number of combined devices.

APPENDIX A

ODD- AND EVEN-MODE EQUIVALENT CIRCUIT DERIVATION FOR A THREE-DIODE LOSSLESS COMBINER

The general oscillation condition for a radial-symmetric combiner was given in Eq. 2.3. This appendix will present the derivation of the normal modes of oscillation for a three-diode combiner system, beginning with the general constraints imposed by the oscillation condition and ending with the equivalent circuits associated with the odd and even modes.

Figure A.1 illustrates the three-device combiner circuit. The circuit matrix associated with this combiner incorporates reciprocity with radial symmetry to give

$$[Z_c] = \begin{bmatrix} Z_{OD} & Z_{OD} & Z_{OD} & Z_{OD} \\ Z_{OD} & Z_{11} & Z_{12} & Z_{12} \\ Z_{OD} & Z_{12} & Z_{11} & Z_{12} \\ Z_{OD} & Z_{12} & Z_{12} & Z_{11} \end{bmatrix} , \qquad (A.1)$$

where use has been made of the fact that for such a circuit symmetry $Z_{01} = Z_{02} = Z_{03} \stackrel{\Delta}{=} Z_{OD}$, $Z_{12} = Z_{13} = Z_{23}$, $Z_{mn} = Z_{nm}$, and $Z_{11} = Z_{22} = Z_{33}$. With the elimination of combining port terms and utilizing Eq. 2.5, the oscillation condition can be written as

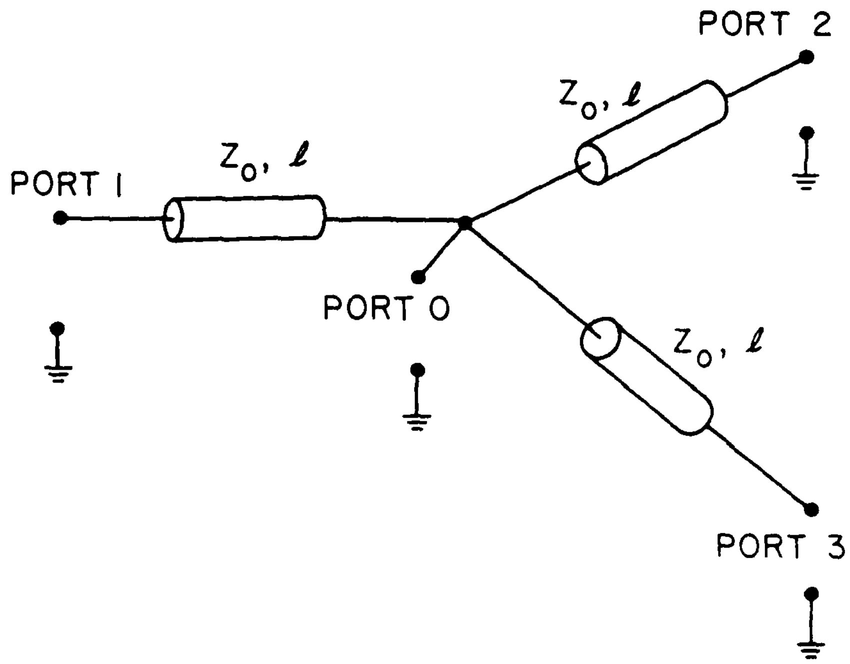


FIG. A.1 FOUR-PORT COMBINING NETWORK OF A THREE-DIODE [illegible] UTILIZING THREE-WAY RADIAL SYMMETRY AND [illegible] [illegible] COMBINING LINES.

$$\begin{bmatrix} Z_{11} - Z' & Z_{12} - Z' & Z_{12} - Z' \\ Z_{12} - Z' & Z_{11} - Z' & Z_{12} - Z' \\ Z_{12} - Z' & Z_{12} - Z' & Z_{11} - Z' \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \\ I_3 \end{bmatrix}$$

$$+ \begin{bmatrix} Z_{d1} & 0 & 0 \\ 0 & Z_{d2} & 0 \\ 0 & 0 & Z_{d3} \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \\ I_3 \end{bmatrix} = \begin{bmatrix} 0 \\ 0 \\ 0 \end{bmatrix} , \qquad (A.2)$$

where $Z' = Z_{op}^2/(Z_{oo} + Z_L)$. Equation A.2 corresponds to Eq. [illegible] given in the earlier part of this report. Letting $Z'_{11} = Z_{11} - Z'$ and $Z'_{12} = Z_{12} - Z'$, Eq. A.2 may be solved as an eigenvalue problem where the eigenvalues of

$$[Z'] = \begin{bmatrix} Z'_{11} & Z'_{12} & Z'_{12} \\ Z'_{12} & Z'_{11} & Z'_{12} \\ Z'_{12} & Z'_{12} & Z'_{11} \end{bmatrix} \qquad (A.3)$$

are obtained from the characteristic equation

$$(Z'_{11} - \lambda)^3 - 3(Z'_{12})^2(Z'_{11} - \lambda) + 2(Z'_{12})^3 = 0 , \qquad (A.4)$$

where λ is the eigenvalue of the equation,

$$[Z']\vec{X}_K = \lambda_K \vec{X}_K . \qquad (A.5)$$

Solving Eq. A.4 results in the three eigenvalues

$$\lambda_0 = Z'_{11} + 2Z'_{12} \qquad (A.6)$$

and

$$\lambda_1 = \lambda_2 = Z'_{11} - Z'_{12} \quad . \qquad (A.7)$$

The corresponding eigenvectors are seen to be

$$\vec{X}_0 = \begin{bmatrix} 1 \\ 1 \\ 1 \end{bmatrix} , \quad \vec{X}_1 = \begin{bmatrix} 1 \\ e^{j(\pi/3)} \\ e^{-j(\pi/3)} \end{bmatrix} , \quad \vec{X}_2 = \begin{bmatrix} 1 \\ e^{-j(\pi/3)} \\ e^{j(\pi/3)} \end{bmatrix} .$$

The relevant impedance parameters for the network of Fig. A.1 are

$$Z_{00} = -j\frac{Z_0}{3}\cot\beta\ell \quad , \qquad (A.8a)$$

$$Z_{01} = -j\frac{Z_0}{3}\csc\beta\ell \quad , \qquad (A.8b)$$

$$Z_{12} = -j\frac{Z_0}{3}\csc\beta\ell\ \sec\beta\ell \qquad (A.8c)$$

and

$$Z_{11} = j\frac{Z_0}{3}(2\tan\beta\ell - \cot\beta\ell) \quad . \qquad (A.8d)$$

With the use of Eqs. A.6 through A.8, the circuit eigenvalues become

$$\lambda_0 = Z_0\frac{3Z_L + jZ_0\tan\beta\ell}{Z_0 + j3Z_L\tan\beta\ell} \qquad (A.9)$$

and

$$\lambda_1 = \lambda_2 = jZ_0\tan\beta\ell \qquad (A.10)$$

which are seen to represent the equivalent circuits in Fig. A.4.

APPENDIX B

MICROSTRIP CIRCUIT BOARD FABRICATION

Numerous microstrip device and combiner test circuits have been designed and fabricated in this investigation. The steps involved in the circuit board fabrication procedure are described in this appendix.

The substrate material used for the microstrip circuits in this study has been exclusively alumina boards. These dielectric boards were available in 1 x 1 in and 2 x 2 in squares, 0.025 in thick with one side highly polished. With some of the combiner test circuits, an ultrasonic impact drill was used to drill vias to realize a *common* combining port before any circuit fabrication processing.

Once completed, each circuit board was epoxied onto a gold-plated test fixture with conductive two-component epoxy. Thermo-compression wire bonds made at 150°C to 225°C were used to connect the devices to the circuit board.

A summary of the fabrication process for a microstrip circuit board is as follows:

1. The blank alumina board is placed into a 50 percent solution of hydrogen peroxide and sulfuric acid ($H_2O_2 + H_2SO_4$), and heated under low heat for approximately 30 min. This procedure cleans the alumina and removes potential contaminants which might interfere with the photolithography.

2. The board is removed from the cleaning bath, rinsed and dried with nitrogen gas. It is immediately placed in a clean, closed container.

3. The clean board is placed without delay into a bell jar evaporator where approximately 500 Å of chrome and 2000 to 3000 Å of gold are evaporated on both sides of the board (chrome used as an adhesive for gold on alumina).

4. Following chrome-gold evaporation, the board undergoes a degreasing step in preparation for photoresist deposition:

a. Board is heated in trochloroethylene for 5 to 10 min.

b. Trichloroethylene is drained out and board is heated in acetone for 5 to 10 min.

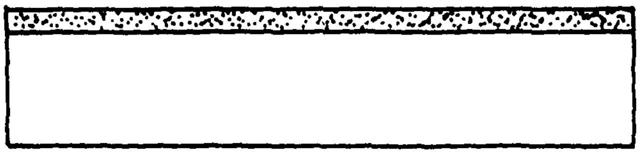
c. Acetone is drained and board is rinsed in methynol and then in di-ionized water (DI).

d. After DI rinse, board is dried with nitrogen gas and placed in a clean oven (~ 60°C) to thoroughly dry for approximately 5 min.

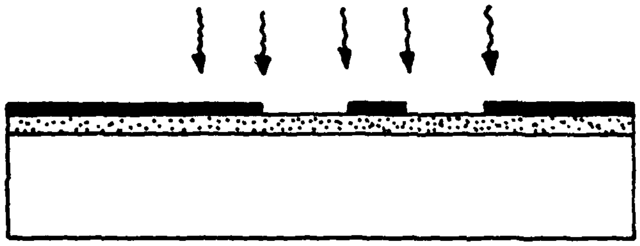
5. AZ-1375 full strength (positive) photoresist is applied onto the smooth side of the board. The board is then spun at approximately 3000 to 3500 rpm for approximately 20 s. This results in the situation shown in Fig. B.1a.

6. After air drying for approximately 2 to 3 min, the alumina board is baked in a 90°C overn for one hour.

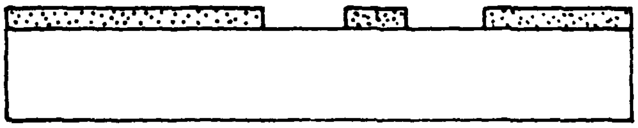
7. After photoresist baking is completed, the board is removed from oven and cooled. The microstrip circuit mask is aligned on the board as indicated in Fig. B.1b and exposed



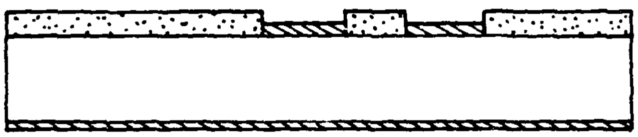
(a) Photoresist Baked on Substrate.



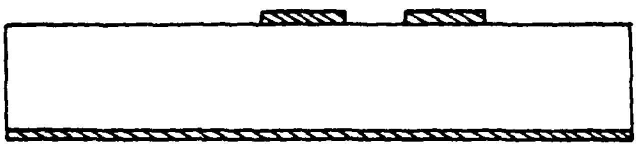
(b) Board Is Masked And Exposed.



(c) Board after Developing.



(d) Gold Is Electroplated onto Regions Defined by the Photolithography.



(e) Final Result.

FIG. B.1 MICROSTRIP CIRCUIT BOARD FABRICATION STEPS.

(typically with the available mask aligner, exposure time required was approximately 3.5 min).

8. The board is developed in AZ-developer for 4 min, vigorously shaking the board in solution.

9. After developing, the board is rinsed in DI water, resulting as shown in Fig. B.1c.

10. The photoresist protective coating is examined under a microscope for flaws. Bottom side is also checked for residual photoresist, and if any is present it is carefully removed with acetone-tipped swabs.

11. After a satisfactory microscope check, the board is placed into a gold plating bath solution which has been filtered and heated to 60°C. Current gold-plating bath has the following specifications:

a. Plating rate: 3 A/ft^2

b. Deposit rate: 0.001 in in 14 min (at plating rate)

c. Plating temperature: 60°C

In practice, plating time is adjusted so as to plate at current levels of 20 to 40 mA, with higher current level used with larger plating areas. If unsuitable current levels are used, a soft, dark-colored gold is obtained. This situation is undesirable for bonding purposes.

12. After plating for a specified time, the board is removed from the plating bath and rinsed thoroughly with DI water. At this point the alumina board appears as in Fig. B.1d.

13. The board is now soaked in acetone to remove all photoresist and then rinsed with DI water.

14. After drying with nitrogen, the alumina board is placed in a gold-etch solution for approximately 15 to 30 s (until chrome is visible) to remove the photoresist protected Au, rinsed in DI water, and again dried.

15. A final etching step is performed by placing the board in a chrome etch solution until all visible chrome is removed as shown in Fig. B.1e.

16. The microstrip circuit board is completed and a final microscope examination is performed to confirm a suitable line quality.

APPENDIX C

DIODE DATA

C.1 Microstrip Diodes

Diode No. 22

QIMP-7999

F_o = 14.3 GHz

V_b @ 0.5 mA, 93.4 V

Peak P_o = 17.5 W

Peak I_{op} = 1.6 A

θ_T = 7.2°C/W

Lot No. L3706-4C

C_T @ V_b 1.65 pF

η = 9.0 percent

Peak V_{op} = 122 V

ΔT_{jave} = 128°C

Diode No. 21

QIMP-7999

F_o = 14.2 GHz

V_b @ 0.5 mA, 93.5 V

Peak P_o = 17.5 W

Peak I_{op} = 1.5 A

θ_T = 7.1°C/W

Lot No. L-3706-4C

C_T @ V_b 1.79 pF

η = 9.5 percent

Peak V_{op} = 123 V

ΔT_{jave} = 119°C

Diode No. 36

QIMP-7999

F_o = 14.3 GHz

V_b @ 0.5 mA, 93.8 V

Peak P_o = 17.5 W

Peak I_{op} = 1.5 A

θ_T = 7.3°C/W

Lot No. L-3706-4C

C_T @ V_b 1.77 pF

η = 9.5 percent

Peak V_{op} = 123 V

ΔT_{jave} = 1[illegible]°C

Diode No. 43

QIMP/7999

F_o = 14.2

V_b @ 0.5 mA, 93.4 V

Peak P_o = 17.5 W

Peak I_{op} = 1.7 A

θ_T = 7.2°C/W

Lot No. L-3706-4C

C_T @ V_b 1.93 pF

η = 8.4 percent

Peak V_{op} = 123 V

ΔT_{jave} = 138°C

Diode No. 31

QIMP/7999

F_o = 14.2 GHz

V_b @ 0.5 mA, 93.5 V

P_o = 17.5 W

I_{op} = 1.6 A

θ_T = 6.7°C/W

Lot No. L-3706-4C

C_T @ V_b 1.83 pF

η = 9 percent

V_{op} = [illegible] V

ΔT_{jave} = 119°C

Diode No. 34

QIMP/7999

F_o = 14.4 GHz

V_b @ 0.5 mA, 93.9 V

P_o = 17.5 W

I_{op} = 1.5 A

θ_T = 7.4 °C/W

Lot No. L-3706-4C

C_T @ V_b 1.63 pF

η = 9.3 percent

V_{op} = [illegible] V

ΔT_{jave} = [illegible]°C

C.2 Coaxial Diodes

5082-0710	Lot No. R-4-5B
f_o = 10.1	No. 20
V_b @ 0.5 mA, 116 V	C_T @ V_b 1.97 pF
P_o = 12.8 W	η = 10.4 percent
I_{op} = 84 A	V_{op} = 147 V
θ_T = 6.1°C/W	ΔT_{jave} = 169 °C

5082-0710	R-4-5B
f_o = 10.1 GHz	No. 63
V_b @ 0.5 mA, 116 V	C_T @ V_b, 198 pF
P_o = 12.8 W	η = 10.2 percent
I_{op} = 0.84 A	V_{op} = 150 V
θ_T = 7.0°C/W	ΔT_{jave} = 198°C

REFERENCES

1. Peterson, D. F., "Radial-Symmetric N-Way TEM Line IMPATT Diode Power Combining Arrays," IEEE Trans. on Microwave Theory and Techniques, vol. MTT-20, No. 2, pp. 163-173, February [illegible].

2. Russell, K. J., "Microwave Power Combining Techniques," IEEE Trans. on Microwave Theory and Techniques, vol. MTT-[illegible], No. 5, pp. 472-478, May 1979.

3. Thoren, G., "IMPATTs Combine to Power Systems," Microwave System News, pp. 110-120, October 1980.

4. Chang, Kai and Sun, Cheng, "Millimeter Wave Power Combining Techniques," IEEE Trans. on Microwave Theory and Techniques, vol. MTT-31, No. 2, pp. 71-107, February 1983.

5. Kurokawa, K. and Magalhaes, F. M., "An X-Band 10 Watt Multiple-IMPATT Oscillator," Proc. IEEE, vol. 59, No. 1, pp. [illegible], January 1971.

6. Harp, R. S. and Stover, H. C., "Power Combining of X-Band IMPATT Circuit Modules," IEEE Int. Solid-State Circuits Conf. Digest, Philadelphia, PA, pp. 118-119, 1973.

7. Wilkenson, E., "An N-Way Hybrid Power Divider," IRE Trans. on Microwave Theory and Techniques, vol. MTT-8, No. 1, pp. 116-118, January 1960.

8. Rucker, C. T., "A Multiple-Diode, High-Average Power Avalanche-Diode Oscillator," IEEE Trans. on Microwave Theory and Techniques, vol. MTT-17, No. 12, pp. 1156-1158, December 1969.

9. Kurokawa, K., "An Analysis of Rucker's Multidevice Symmetrical Oscillator," IEEE Trans. on Microwave Theory and Techniques, vol. MTT-18, No. 111, pp. 967-969, November 1970.

10. Peterson, D. F. and Haddad, G. I., "Design, Performance and Device/Circuit Limitations on N-Way Symmetrical IMPATT Diode Power Combining Arrays," Tech. Report AFWAL-TR-81-1107, Electron Physics Laboratory, The University of Michigan, Ann Arbor, February 1981.

11. Hewlett-Packard Co., "Diode and Transistor Designer's Catalog," 1980.

12. Hewlett-Packard Application Note 221, "Semi-Automatic Measurements Using the 8410B Microwave Network Analyzer and the 9825A Desk-Top Computer," 1978.

13. Hewlett-Packard Application Note 117-1, "Microwave Network Analyzer Applications," June 1970.

14. Hewlett-Packard Application Note 218-1, "Applications and Performance of the 8671A and 8672A Microwave Synthesizers," September 1979.

15. Hewlett Packard Application Note 282-1, "6942A Multiprogrammer System Throughput Analysis for Multiprogrammer Systems Using the 9825A Desk-Top Computer," September 19[illegible].

16. Hewlett-Packard Application Note 221A, "Automating the HP 8410B Microwave Network Analyzer," June 19[illegible].

17. Hooker, S. A., [illegible], Haddad, G. I. [illegible], Y. [illegible], [illegible], N. A., Peck, D. E., Peterson, D. F. and Yang, D. [illegible], [illegible] Technology Final Report,

18. Den Linger, E. T., Rosen, J., "Microstrip Varactor-Tuned Millimeter-Wave IMPATT Diode Oscillators," IEEE Trans. on Microwave Theory and Techniques, vol. MTT-23, No. 12, pp. [illegible]-958, December 1975.

19. Snider, D. M., "A One-Watt CW High-Efficiency X-Band Avalanche-Diode Amplifier," IEEE Trans. on Microwave Theory and Techniques, vol. MTT-18, No. 11, pp. 963-967, November 1970.

20. Ku, W. H. and Scherer, E. F., "Gain-Bandwidth Optimization of Avalanche-Diode Amplifiers," IEEE Trans. on Microwave Theory and Techniques, vol. MTT-18, No. 11, pp. 932-942, November 1970.

☆U.S.Government Printing Office: 1984 759-062/908

DATE
FILMED