Contract No. N00173-79-C-0010

R83AEB637

HIGH TEMPERATURE ELECTRONICS TECHNOLOGY

PHASE II — FINAL REPORT

MAY 1984

PROGRAM MANAGER
M.D. Marvin

ENGINEERING MANAGERS
D.C. Doning
J.E. Hurtle

GENERAL ELECTRIC
AIRCRAFT ENGINE BUSINESS GROUP
ADVANCED TECHNOLOGY PROGRAMS DEPARTMENT
CINCINNATI, OHIO 45215

Contract No. N00173-79-C-0010

R83AEB637

HIGH TEMPERATURE ELECTRONICS TECHNOLOGY

PHASE II — FINAL REPORT

MAY 1984

PROGRAM MANAGER
M.D. Marvin

ENGINEERING MANAGERS
D.C. Dening
J.E. Hurtle

GENERAL ELECTRIC

AIRCRAFT ENGINE BUSINESS GROUP
ADVANCED TECHNOLOGY PROGRAMS DEPARTMENT
CINCINNATI, OHIO 45215

Unclassified

SECURITY CLASSIFICATION OF THIS PAGE

REPORT DOCUMENTATION PAGE

1a. REPORT SECURITY CLASSIFICATION Unclassified	1b. RESTRICTIVE MARKINGS None
2a. SECURITY CLASSIFICATION AUTHORITY	3. DISTRIBUTION/AVAILABILITY OF REPORT Unrestricted
2b. DECLASSIFICATION/DOWNGRADING SCHEDULE	
4. PERFORMING ORGANIZATION REPORT NUMBER(S) R83AEB637	5. MONITORING ORGANIZATION REPORT NUMBER(S)
6a. NAME OF PERFORMING ORGANIZATION General Electric Company Aircraft Engine Business Group 6b. OFFICE SYMBOL (If applicable)	7a. NAME OF MONITORING ORGANIZATION Naval Research Laboratory
6c. ADDRESS (City, State and ZIP Code) Cincinnati, Ohio 45215	7b. ADDRESS (City, State and ZIP Code) Washington, D.C. 20375
8a. NAME OF FUNDING/SPONSORING ORGANIZATION Naval Air System Command 8b. OFFICE SYMBOL (If applicable) AIR-330	9. PROCUREMENT INSTRUMENT IDENTIFICATION NUMBER N00173-79-C-0010
8c. ADDRESS (City, State and ZIP Code) Washington, D.C. 20361	10. SOURCE OF FUNDING NOS. PROGRAM ELEMENT NO. 62762 N; PROJECT NO. W.F. 584; TASK NO. ---; WORK UNIT NO. 68-0818-0-0
11. TITLE (Include Security Classification) High Temperature Electronics Technology	
12. PERSONAL AUTHOR(S) Dening, David C., General Electric Company, Electronics Laboratory, Syracuse, N.Y. 13221	
13a. TYPE OF REPORT Final	13b. TIME COVERED FROM 4/80 TO 9/83
14. DATE OF REPORT (Yr., Mo., Day) 1984 March	15. PAGE COUNT 209
16. SUPPLEMENTARY NOTATION	

17. COSATI CODES		
FIELD	GROUP	SUB. GR.
09	01	
20	12	

18. SUBJECT TERMS (Continue on reverse if necessary and identify by block number)
Refractory Metallization, Integrated Injection Logic, High Temperature Aircraft Engine Digital Controls, Full Authority Digital Electronic Control

19. ABSTRACT (Continue on reverse if necessary and identify by block number)

This report summarizes the barrier metallization developments accomplished under the subject contract, during the period of performance from April 1980 to September 1983, of a program intended to develop 300°C electronic controls capability for potential on-engine aircraft engine application. In addition, this report documents preliminary life test results at 300°C and above and discusses improved design practices required for high temperature integrated injection logic semiconductors. Previous Phase I activities focused on determining the viability of operating silicon semiconductor devices over the -55°C to +300°C temperature range. This feasibility was substantiated but the need for additional design work and process development was indicated. Phase II empasized the development of a high temperature metallization system as the primary development need for high temperature silicon semiconductor applications.

20. DISTRIBUTION/AVAILABILITY OF ABSTRACT UNCLASSIFIED/UNLIMITED ☒ SAME AS RPT. ☐ DTIC USERS ☐	21. ABSTRACT SECURITY CLASSIFICATION Unclassified
22a. NAME OF RESPONSIBLE INDIVIDUAL Dr. A. Christou, Scientific Officer	22b. TELEPHONE NUMBER (Include Area Code) (202)-767-2799 22c. OFFICE SYMBOL 6815

DD FORM 1473, 83 APR EDITION OF 1 JAN 73 IS OBSOLETE.

Unclassified

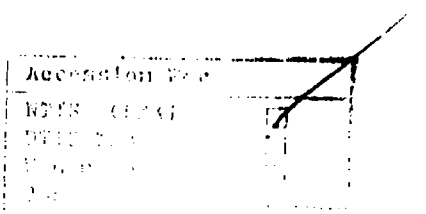
SECURITY CLASSIFICATION OF THIS PAGE

FOREWORD

This report covers the Phase II tasks of a program to develop high temperature digital electronic controls for advanced aircraft gas turbine usage. The program was conducted by the Aircraft Engine Business Group of the General Electric Company for the Naval Research Laboratory under Naval Air Systems Command sponsorship.

The work reported herein was performed during the period from May 1980 through September 1983. The Navy Scientific Officer for a major segment of this period was Dr. A. Christou, NRL Code 6815. The General Electric Program Manager was Mr. Mason D. Marvin; the semiconductor development work at the Electronics Laboratory in Syracuse, New York was performed under the direction of Dr. David C. Dening. Mr. James Hurtle provided overall program technical direction consistent with the needs of advanced design digital aircraft engine controls.

The work was in accordance with Contract Modifications P00005 through P00011 of the High Temperature Electronics Technology Program, Contract N00173-79-C-0010. This portion of the program concentrated on barrier metallization improvements. In addition, the initial life testing of high temperature circuits and development of improved design practices for high temperature integrated injection logic circuits were accomplished.



A-1

TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

LIST OF ILLUSTRATIONS (Continued)

LIST OF ILLUSTRATIONS (Continued)

LIST OF ILLUSTRATIONS (Continued)

LIST OF ILLUSTRATIONS (Continued)

LIST OF ILLUSTRATIONS (Continued)

LIST OF ILLUSTRATIONS (Continued)

LIST OF ILLUSTRATIONS (Continued)

LIST OF ILLUSTRATIONS (Concluded)

LIST OF TABLES

LIST OF ACRONYMS

AES	Auger Electron Spectroscopy
CERDIP	Ceramic Dual In-Line Package
CMOS	Complementary Metal Oxide Semiconductor
DIP	Dual In-Line Package
FADEC	Full Authority Digital Electronic Control
IC	Integrated Circuit
I^2L	Integrated Injection Logic
ISL	Integrated Schottky Logic
LSI	Large Scale Integration
MSI	Medium Scale Integration
MTBF	Mean Time Between Failures
SEM	Scanning Electron Microscope
SIMS	Secondary Ion Mass Spectrometry
VCE	Variable Cycle Engine
VHSIC	Very High Speed Integrated Circuits
VLSI	Very Large Scale Integration

SUMMARY

Silicon based Integrated Injection Logic (I^2L) circuits tested during this program phase have survived a life test for over 5000 hours at 360° C without degradation. These chips used aluminum metallization with low current densities (below 10,000 amp/cm^2) to avoid electromigration failures. The need for a gold based metal system for high temperature applications has led to the development of Ti-W diffusion barriers which have withstood temperatures of 360° C for longer than 3500 hours without change. MSI integrated circuits with a Ti-W/Au metallization system have withstood stress tests of over 2000 hours at 360° C. Gold hillock formation has been shown to be caused by the compressive strains induced in the gold film by thermal expansion mismatches. The driving force for gold hillock formation may be eliminated by depositing the gold film at elevated temperatures. Passivation can also be utilized to inhibit gold hillock formation. Dual level metallization development efforts have been initiated utilizing silicon nitride as a dielectric and passivation medium.

Program test results have shown that the high temperature life of an I^2L integrated circuit is not limited by degradation of the silicon itself, but rather by the degradation of the metallization system or by the interaction between the metallization and the silicon. In particular, aluminum metallization is limited both by electromigration and by its interaction with silicon. A gold metallization system with a metallurgical barrier was chosen for this work because of its lower susceptibility to electromigration.

The conventional Ti-W/Au system was found to be inadequate at temperatures above 300° C for two basic reasons: the conventional Ti-W system was not an effective barrier to gold penetration at these temperatures, and rapid gold hillock formation occurred due to residual strains in the gold film. An adequate barrier was achieved by "stuffing" the Ti-W layer with nitrogen and the gold hillocks were suppressed by depositing the gold at elevated temperatures. Since the "stuffing" adversely affected the adhesion of the Ti-W to both the gold and the silicon oxide, a more complex layered system has been evolved to solve these problems. The results of life tests carried out to

evaluate this multilayered metallization system are encouraging. MSI circuits have operated for over 2000 hours at 300° C without failure as part of a separately contracted follow-on program.

1.0 INTRODUCTION

1.1 POTENTIAL APPLICATION OF HIGH TEMPERATURE ELECTRONICS ON AIRCRAFT ENGINES

Over the past decade, numerous technology improvements have been made in broad areas of aircraft turbine propulsion. These improvements involve significant emphasis on both turbine engine components and on the associated propulsion systems. A notable development is the introduction of the Variable Cycle Engine (VCE) which utilizes variable bypass airflow from the fans to the jet nozzle. This feature extends the efficient flight and power domains of the engine but requires a significant increase in the number of manipulated variables and regulating functions handled by the control. Further, to obtain the advantages offered by such an engine, a much more complex control strategy must be used to govern the manipulated variables.

As a consequence of the expanding need for additional control functions together with the timely progress in microprocessor-based digital circuitry, there is now considerable activity in the development of computer-based digital engine controls. In fact, these technologies have reached the point where "full authority" for the engine control and for operating integrity is being handled by digital electronics. It should be noted that this contractor has recently completed such a Full Authority Digital Electronic Control (FADEC) development for the Navy under Contract N00019-76-C-0423 (Reference 1).

The supersonic aircraft, especially the modern military fighter, introduces cooling limitations associated with the fact that both aircraft/nacelle surfaces and ram air reach elevated temperatures which render ineffective any attempts to directly cool electronic packages to levels suitable for 125° C semiconductor operation. Current practice is to use engine fuel as the cooling/heat sink medium. This requires pumping, fuel interfacing, and electronics packaging having integral fuel-fed cooling tubes which increase cost, limit reliability, and add to the system weight.

Now there is some recent evidence that certain modern fighter configurations can experience engine intake fuel temperatures in excess of the 100° C usually specified. In such situations, fuel must be routed directly from the

fuel tank to the control prior to the aircraft Environmental Control System and lube oil heat exchangers, both of which contribute to fuel temperature rise. This "control first" routing introduces considerable additional fuel line length with an associated vulnerability and weight increase.

Today's electronic controls are based on existing military-type semiconductors which are rated for 125° C operation. Without fuel cooling, on the other hand, engine-located electronics in supersonic aircraft will face operating temperatures between -55° and +300° C. Thus the development of appropriate 300° C semiconductor devices and associated circuit elements will make it possible to utilize engine bleed air or nacelle air as the cooling medium, thus eliminating the liquid-fuel cooling system.

The reduction to practice of 300° C on-engine electronics will make possible direct conduction of internal heat to the surface of the electronic on-engine control and direct heat transfer to the engine fan discharge airflow. Reduced procurement costs, system weight reductions, and simplified control interfaces leading to higher reliability can be obtained through the elimination of fuel cooling within the control.

The question is occasionally raised as to the feasibility of removing the digital electronic control from the engine and remotely locating it in the more benign environment of the aircraft electronic bay. This action would result in a net decrease in overall propulsion system reliability, because what is gained in electronic reliability (realizable only if on-engine control electronic construction quality were maintained in the off-engine location) is less than what is lost in increased vulnerability of the overall propulsion control system. The increased vulnerability results from (1) risk of loss of continuity between control and engine and (2) risk that a single event could affect multiple engine controls.

Mounting the engine controls on each engine assures that a single failure or common event affecting only one of the engine controls will not propagate to the other engines as would be the case if the engine control computations were performed in a single aircraft computer or in aircraft computers mounted in proximity within the electronics bay.

Distributed computers for computation and control offer an additional advantage in that data may be consolidated and utilized locally with only that data needed for the next higher echelon level being transmitted beyond the immediate confines of the engine. The weight and complexity of the transmission paths are less and their vulnerabilities and failure consequences are reduced. Mounting the engine control on the engine assures the shortest, least vulnerable paths for critical engine-level control logic.

The on-engine control provides a degree of protection from momentary interruptions of command data from the pilot and aircraft by continuing uninterrupted engine operation using the most recent good thrust command until faults are cleared or redundant paths energized.

The on-engine control establishes a complete powerplant assembly. This completeness assures system accountability which is an advantage to the aircraft manufacturer and the operating service from both a contractual and maintenance viewpoint since the engine cannot be operated or tested without its control.

All of these advantages and needs for on-engine control require design diligence in meeting the environmental requirements of on-engine vibration and temperature. Integrated efforts which couple the high temperature development of advanced control electronics with advanced engine technology are being pursued by General Electric's Aircraft Engine Business Group with support from Government-sponsoring agencies. The program reported herein addresses the high temperature electronics developments which will make possible utilization of engine-supplied cooling air as a superior approach for supersonic flight.

1.2 OVERVIEW OF HIGH TEMPERATURE ELECTRONICS DEVELOPMENT PROGRAM

The Naval Research Laboratory initiated this program in December 1978. The first phase, completed in March 1980, provided an evaluation of existing high temperature capabilities found in conventional electronic parts. An important part of this task was a literature search. Experimental measurements were also made on those control circuit devices for which the literature lacked 300° C operating data. Observed device degradation was categorized. The data from Phase I, in conjunction with FADEC requirements, led to the

selection of Integrated Injection Logic (I^2L) and Complementary Metal Oxide Semiconductor (CMOS) as the technologies for high temperature large scale integration (LSI) engine control development. An interim report (Reference 2) dated March 1980 documents the results of this initial phase.

Phase II of the program involves developing basic integrated circuit (IC) technology to achieve 10,000 hours mean time between failures (MTBF) at 300° C. The Phase II activities as reported herein have concentrated on developing a refractory metallisation system. Dual layer development, design rule optimisation, and fabrication processing development have also been pursued.

Phase III is planned to utilize the basic high temperature technology developed in Phase II for the design and fabrication of large scale integration devices (over 1000 gates per chip) which have 300° C capability and which incorporate FADEC circuitry. Fabrication and high temperature evaluation will be involved.

Three activities are planned in Phase IV: the development of (1) passive parts, (2) interconnection/bonding/metallurgy, and (3) packaging techniques. Passive parts will be upgraded as necessary and tested. The interconnection system development will be based on extending Kovar TAB techniques to enhance thermal cyclic life. Candidate bonding techniques for refractory metallisation systems will be investigated to establish one or more processes suitable for 300° C. General Electric has a unique hybrid microelectronic package under development for on-engine-mounted controls having fuel cooling. This is based on multilayer refractory metal ceramic substrate techniques, a technology which will serve as a starting point for moving up to a 300° C capability.

Phase V involves the application and circuit demonstration of the high temperature electronics capability developed in the earlier tasks. Using the circuitry from the Navy's Full Authority Digital Electronic Control Program, an actual control subsystem will be prototyped and operated over the -55° to +300° C temperature range.

In Phase VI, the balance of a complete electronic engine control will be developed. In addition to the electronic circuitry, this will include such control-located parts as pressure sensors, filters, and connectors. The resulting control will be demonstrated in the laboratory, both open and closed

loop, using a computerized engine simulation. Later, a system's test will be run in which the control operates sensor and actuator hardware, again with a simulated engine.

1.3 THE PERFORMANCE OF INTEGRATED INJECTION LOGIC AT HIGH TEMPERATURE

The contract effort for this phase concentrated on barrier metallization development. As a result, a report of this work does not include information on the operating performance of I^2L at high temperatures. The initial work documenting the intrinsic high temperature properties of integrated injection logic was performed in 1979 under an IR&D program sponsored by the Aircraft Engine Business Group. The relevant section of that IR&D report has been included herewith as Appendix A to supply background information. Devices similar to those discussed in this appendix were used as life test vehicles in this program.

It should be noted that Section 5.0 of this contract final report discusses a computer modeling study for improving the high temperature properties of this older style of double diffused bipolar I^2L process. Analysis of the newer generations of ion implanted bipolar processes have shown that they are capable of producing I^2L with a faster switching speed and operating at even higher temperatures than those discussed in Appendix A.

2.0 METALLIZATION TEST MASK DESCRIPTIONS

Two mask sets were employed during the course of this program. The 7-471 metallization development masks were used to fabricate preliminary life test samples and metallization samples. The E115 mask set was designed during this period of the program to serve as a process development aid and to supply life test circuits with an MSI level of complexity. This report section describes the features of the two mask sets.

2.1 7-471 METALLIZATION DEVELOPMENT MASK

In the previous phase of this program, a custom Integrated Injection Logic (I^2L) metallization test mask set was designed. The resulting 7-471 test mask includes a number of different test elements which are aimed at determining constraints on ohmic contact size, metal width, and spacing, as well as generating a test element which includes symmetrical cell integrated injection logic gates and ring oscillators. A description of this mask pattern is repeated for continuity and background since much of the work in this phase was based on experiments with chips fabricated using this pattern.

The test elements were designed in a manner which allows (1) ohmic contact resistance to be accurately measured from external package leads, (2) series resistance to be accurately measured while arbitrary current levels are passed through a metal thin-film conductor element, (3) arbitrary voltage levels to be applied between adjacent metallization runs for dielectric evaluation using external package leads, (4) integrated injection logic gate digital gain to be measured from external package leads, as a function of temperature, and (5) integrated injection logic propagation delay to be externally measured using seven-stage ring oscillators. The mask consists of a repetition of the 190 x 186 mil master cell shown in Figure 2-1. The master cell is divided by scribe lanes into four separable chip types. Each chip, therefore, has an area of 95 x 93 mils. Within each chip there are two different test element cells. Cells A1, A2, A3, A4, B1, B2, and B3 are metallization test elements. The final cell is an integrated injection logic active test circuit.

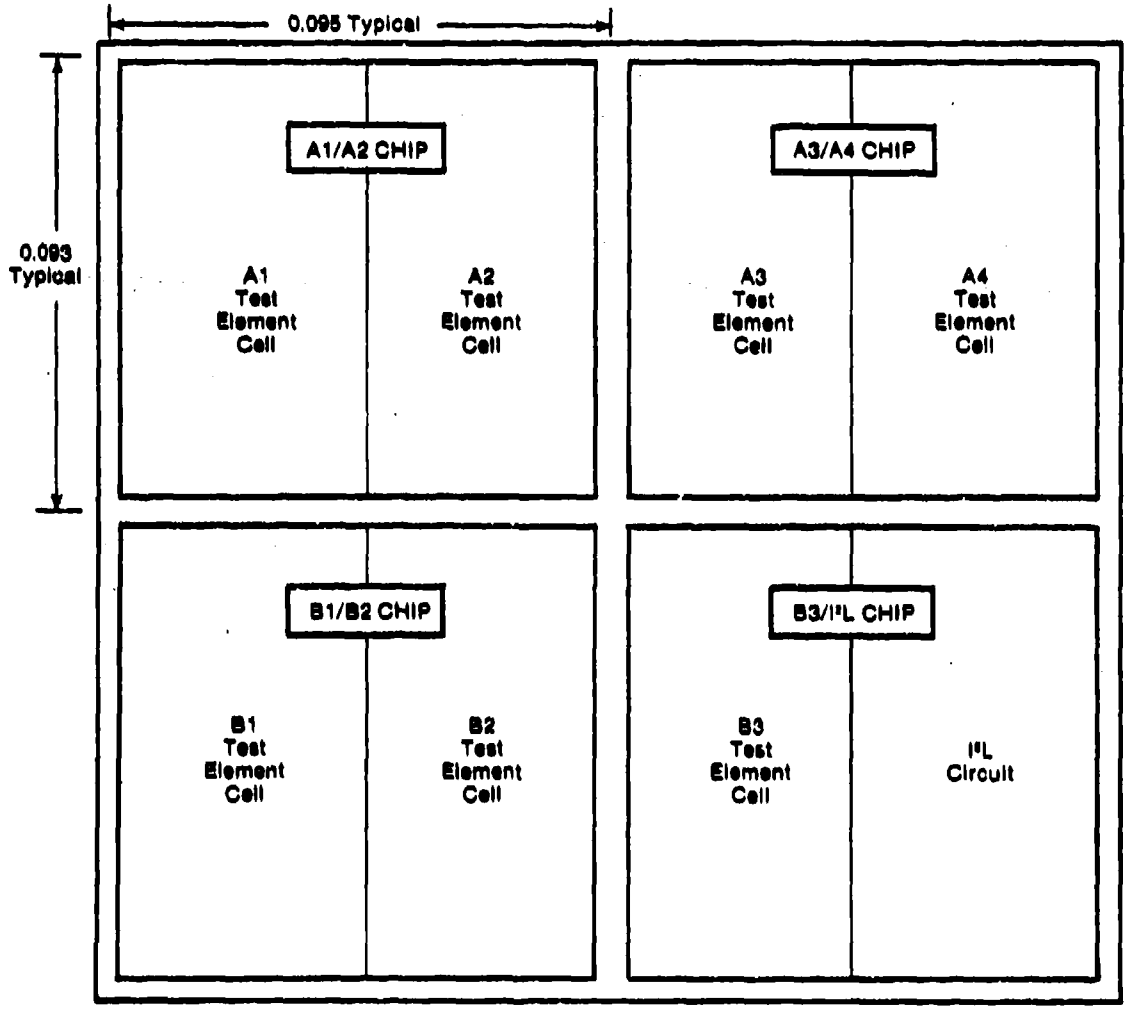


Figure 2-1. Master Cell Block Diagram of the 7-471 Metallization Mask.

The metallization test cells were designed to investigate the electromigration effect of the thin metal layer as a function of the metal line width and metal line spacing at elevated temperature. The electromigration effect could eventually cause metal line voiding and resulting open-circuit and short-circuit situations between separated metal lines. The metal test elements were designed with a four-point probe capability to enable precise measurements to be made to detect effects of electromigration long before catastropic failure.

Figure 2-2 shows a plot of the metal test element Cell A1, which is also representative of A2, A3, A4, B1, B2, and B3. Like all the test elements, A1 has 24 input/output pads. Pads 1, 2, 3, 4, 13, 14, 15, and 16 are used for ohmic contact evaluation. Pads 5, 8, 21, and 24 constitute a four-point probe for the precise measurement of a metal conductor which is 0.25 mil in width. Pads 6 and 7 contact both ends of a second 0.25 mil wide metal conductor, which is spaced 0.25 mil away from the original central metal conductor. Pads 22 and 23 contact both ends of a third 0.25 mil metal conductor, which is also spaced 0.25 mil from the original central conductor. Pads 9, 10, 11, 12, 17, 18, 19, and 20 perform a second experiment, where the conductor width and spacing are both 0.3 mil (instead of the 0.25 previously discussed).

To cover the range of the current integrated injection logic fabrication process, four different widths of metal stripes were chosen: 0.2, 0.25, 0.3, and 0.4 mil. The metal stripe spacing was matched to the metal stripe width in each test element.

The metallization test elements also investigate the effect of contact hole size on the ohmic contact resistance for each type of doped region. On each metallization test cell (from A1 to B3), the top and bottom four pads were used for ohmic contact studies.

For the electromigration studies, each test cell contains two electromigration test vehicles containing three parallel metal stripes which are greater than 10 mils in length.

The stress pull test on wire bonding can be done on the enlarged metal pad of 8 x 8 mil size near the center of the test chip (numbered 25).

Note: This Metal Pattern is Typical of the Seven Metallization Patterns on the 7-471 Mask.

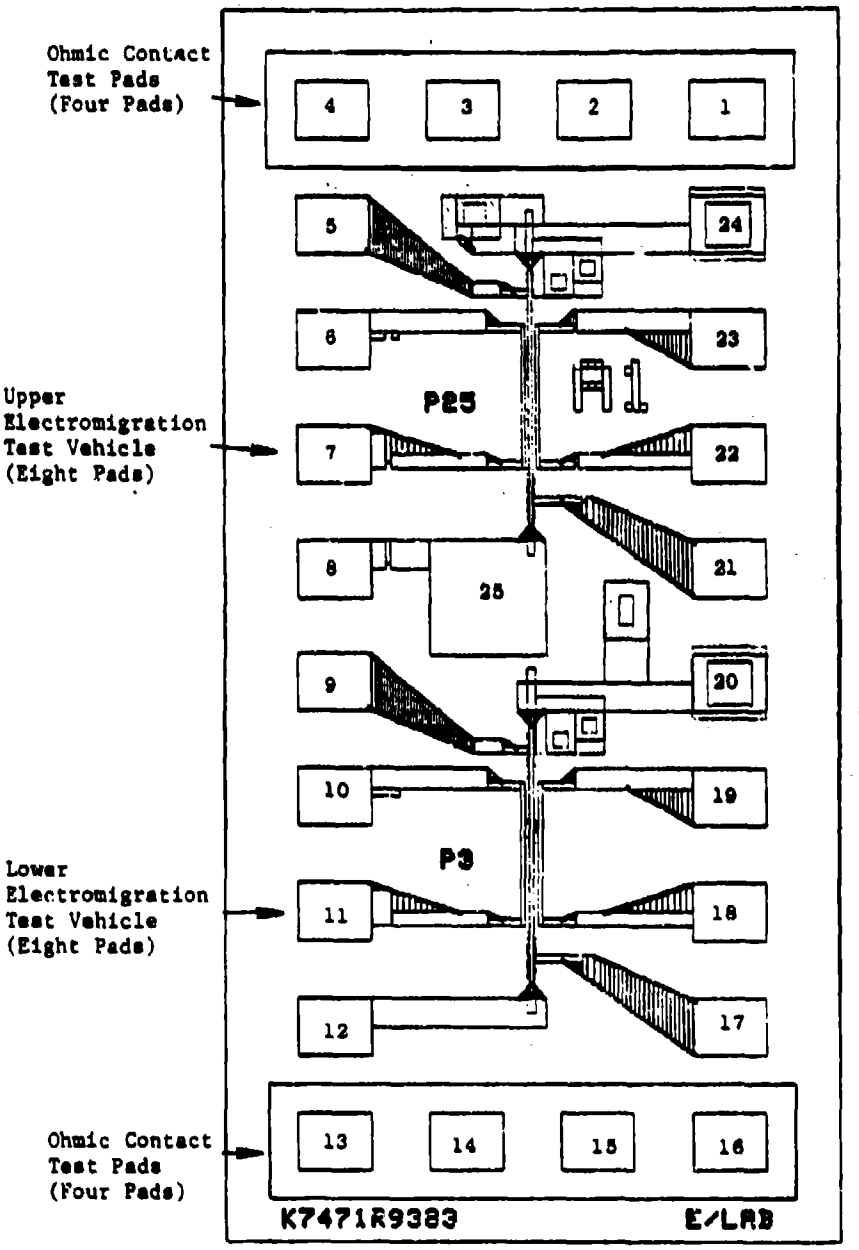


Figure 2-2. Metallization Test Element, Cell A1.

Steps in the surface contour of a monolithic circuit are known to degrade the useful resolution capability of any given metallization system as well as increase electromigration effects. To reveal possible problems, various combinations of these steps were intentionally designed into the metal test elements. Thus seven test element cells are devoted to the evaluation of conductor line width, spacing, and ohmic contact resistance. Table 2-1 indicates the line width, the line spacing, and the type of contact being tested in each of the metallization test cells.

Table 2-1. Metal Test Cell Features.

Cell Designation	Oxide Feature Under Four Probe Electromigration Line	Contact Opening, Line Width, and Line Spacing, mils	Contact Test
A1	p p	0.25 0.3	p p
A2	n n	0.25 0.3	n n
A3	pn -	0.25 0.25	np Schottky
A4	pn -	0.3 0.3	np Schottky
B1	pn -	0.4 0.4	np Schottky
B2	p n	0.4 0.4	p n
B3	n -	0.2 0.2	np p

Figures 2-3 through 2-6 show the four chip types. Figure 2-3 is a photograph of a chip which includes both A1 and A2 test devices. Figure 2-4 is a photograph of the A3 and A4 chip and Figure 2-5 is a photograph of the B1 and B2 chip. Figure 2-6 is a photograph of the B3 metal test configuration along with an integrated injection logic test cell. This test cell is aimed at evaluating integrated injection logic active circuits with the barrier metallization

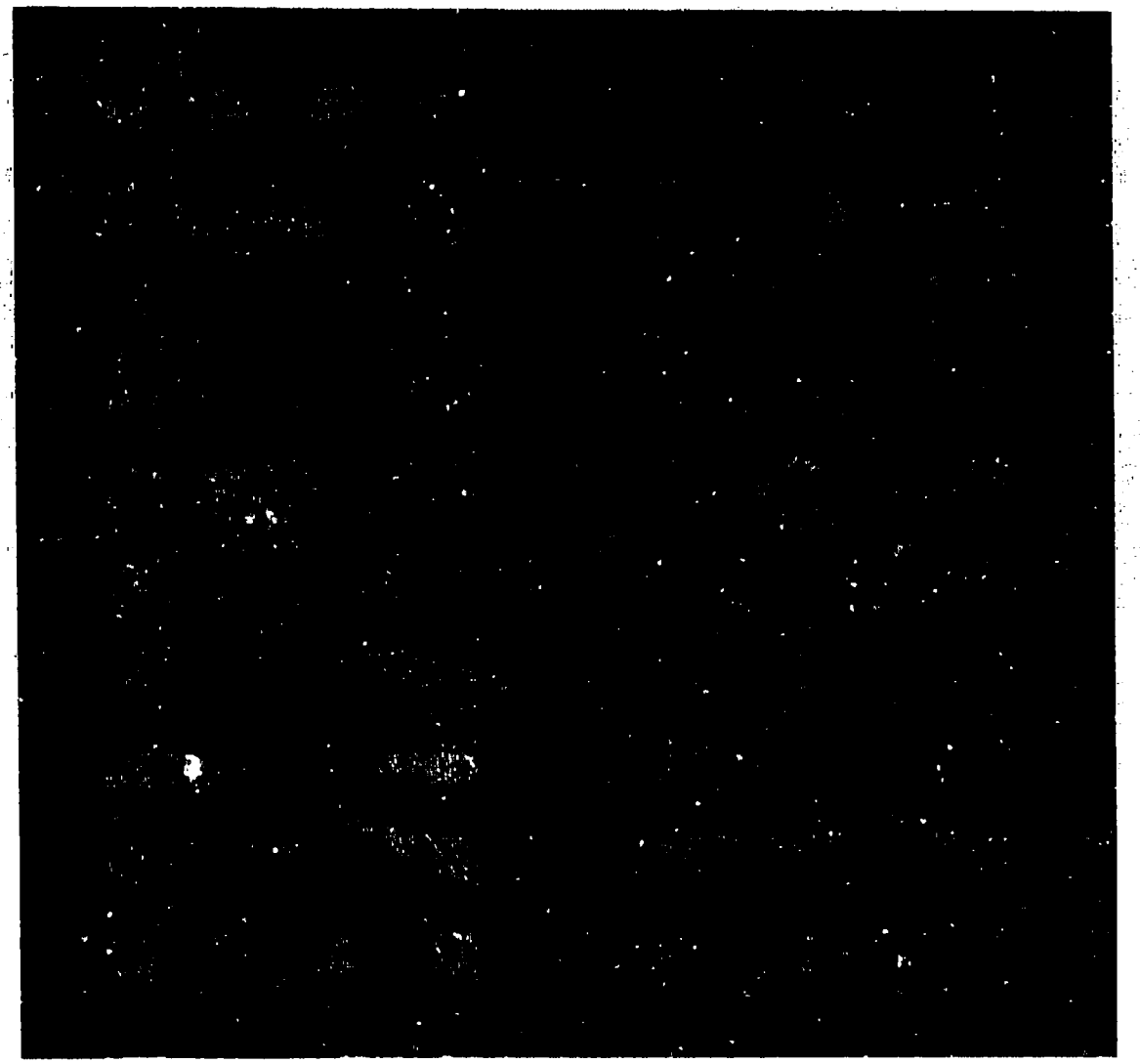


Figure 2-3. Photograph of A1/A2 Chip.

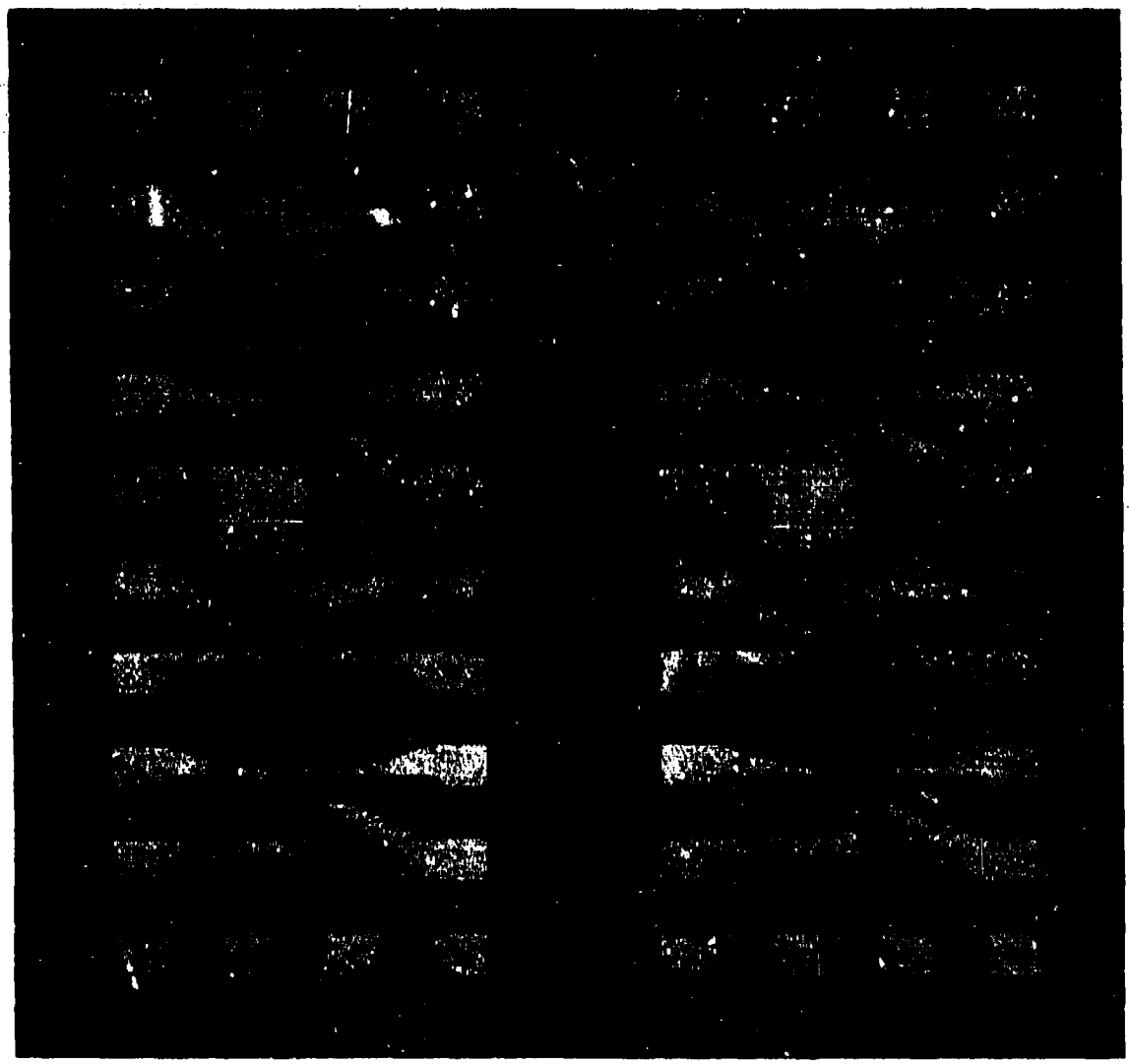


Figure 2-4. Photograph of A3/A4 Chip.

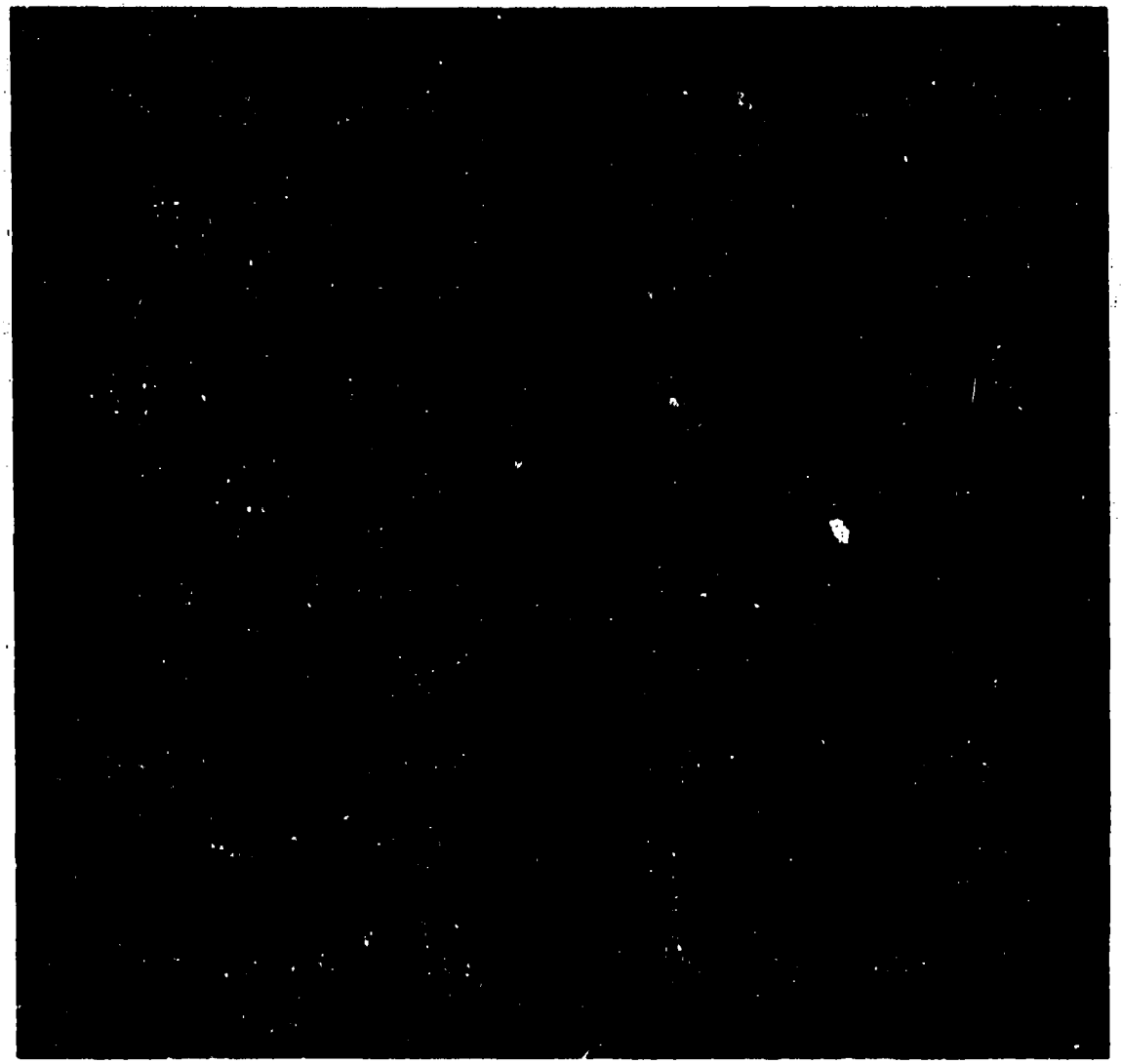


Figure 2-5. Photograph of B1/B2 Chip.

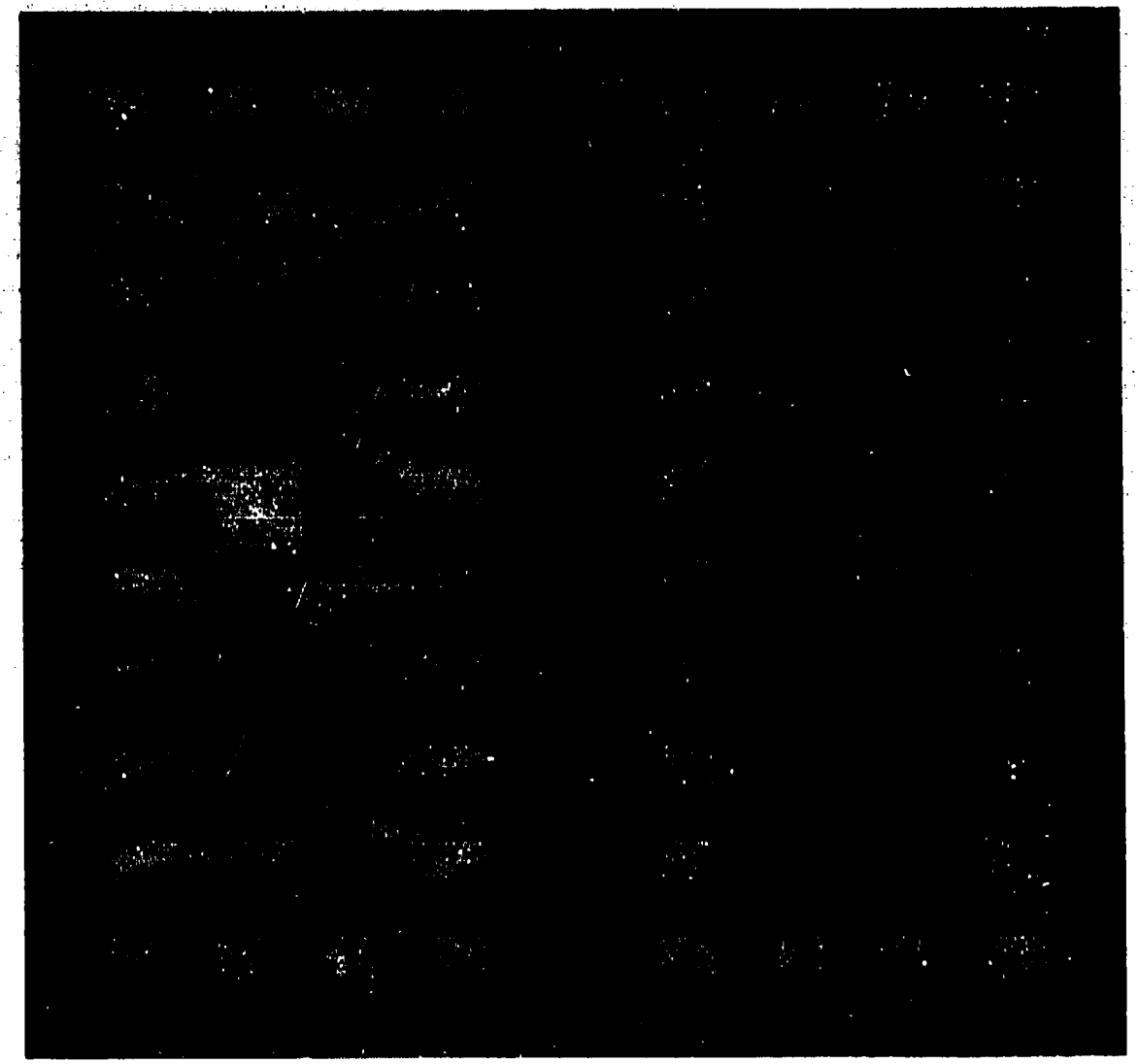


Figure 2-6. Photograph of B3/I^2L Chip.

system. The integrated injection logic circuit test cell consists of the following components:

1. A rectangular symmetrical gate cell and a slanted symmetrical gate cell, each cell containing a dual output logic gate and a quad output logic gate as shown in Figure 2-7.

2. Seven-stage ring oscillators using the same basic gates described above.

3. A seven-stage ring oscillator with reduced geometry gates.

2.2 E115 DUAL LEVEL METALLIZATION DEVELOPMENT MASK

A test mask needed for the development of the dual level metallization system was designed using the Calma layout equipment. The mask set design objectives were the following:

- Provide a test vehicle for the processing development of a dual level metallization system.
- Provide potential yield information for the dual layer metallization system in conjunction with a General Electric standard I^2L bipolar process.
- Provide a life test vehicle for components with MSI level gate complexity as a means of evaluating the various elements used in a larger chip design.
- Provide the ability to monitor electrical properties of the diffused semiconductor regions and the metal system before and after high temperature life tests.

The overall master cell produced from the mask set measures 7852 microns (309 mils) by 5478 microns (216 mils) from the inside of the scribe lines. The master cell is divided into six sectors as shown in Figure 2-8. Each sector is 2484 microns (97.8 mils) by 2639 microns (103.9 mils).

Sector 1 is used to evaluate resistance parameters. Sectors 2 through 6 are devoted to metallization experiments. The metallization experiments employ a standardized pad placement so that a single probe card can be used for testing. Each of the metallization sections may be packaged in a standard 24 pin dual in-line package for individual testing. Various metal design rules are being evaluated through the use of this mask including both a conservative and an aggressive approach.

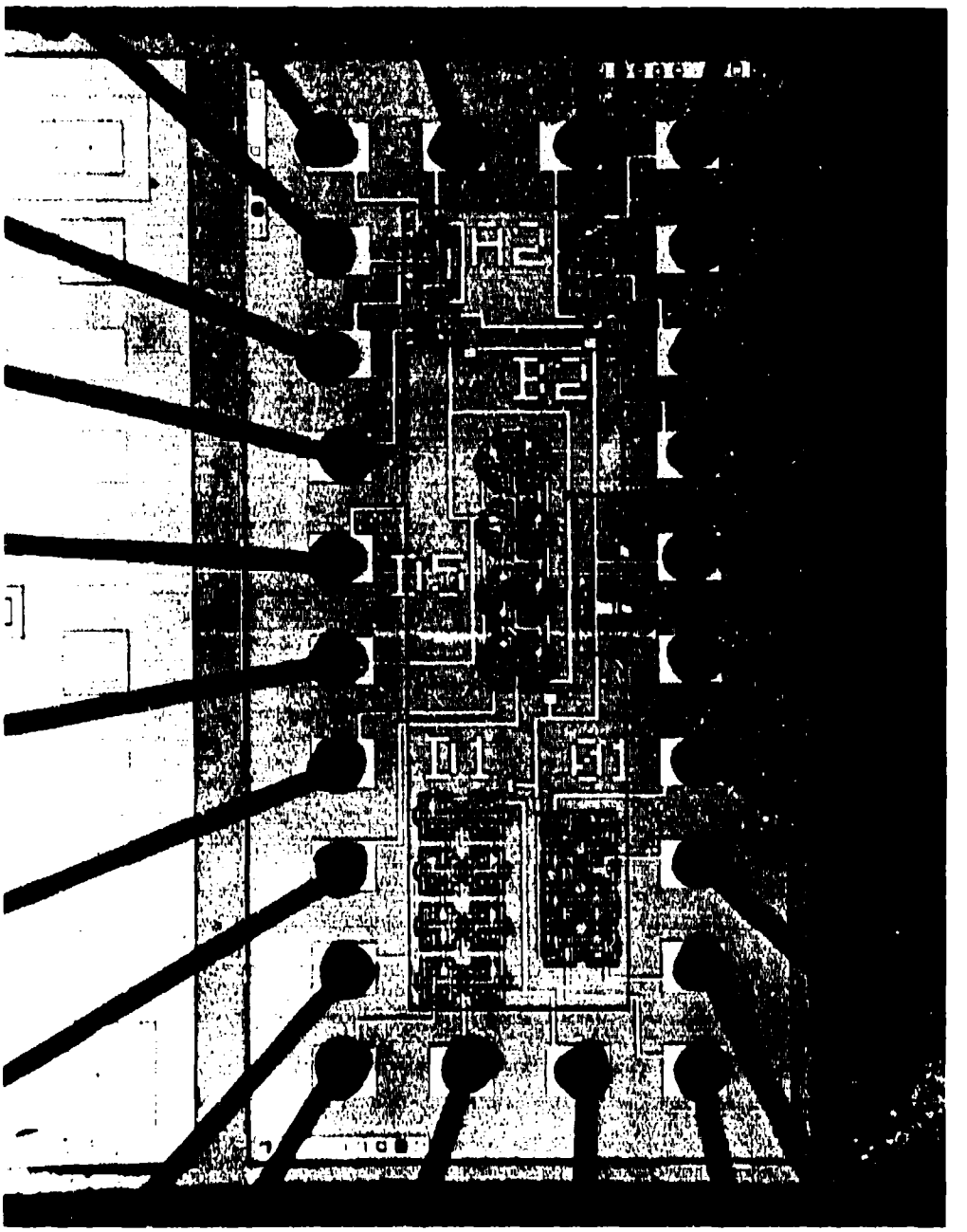


Figure 2-7. Packaged I^2L Ring Oscillator Test Circuit.

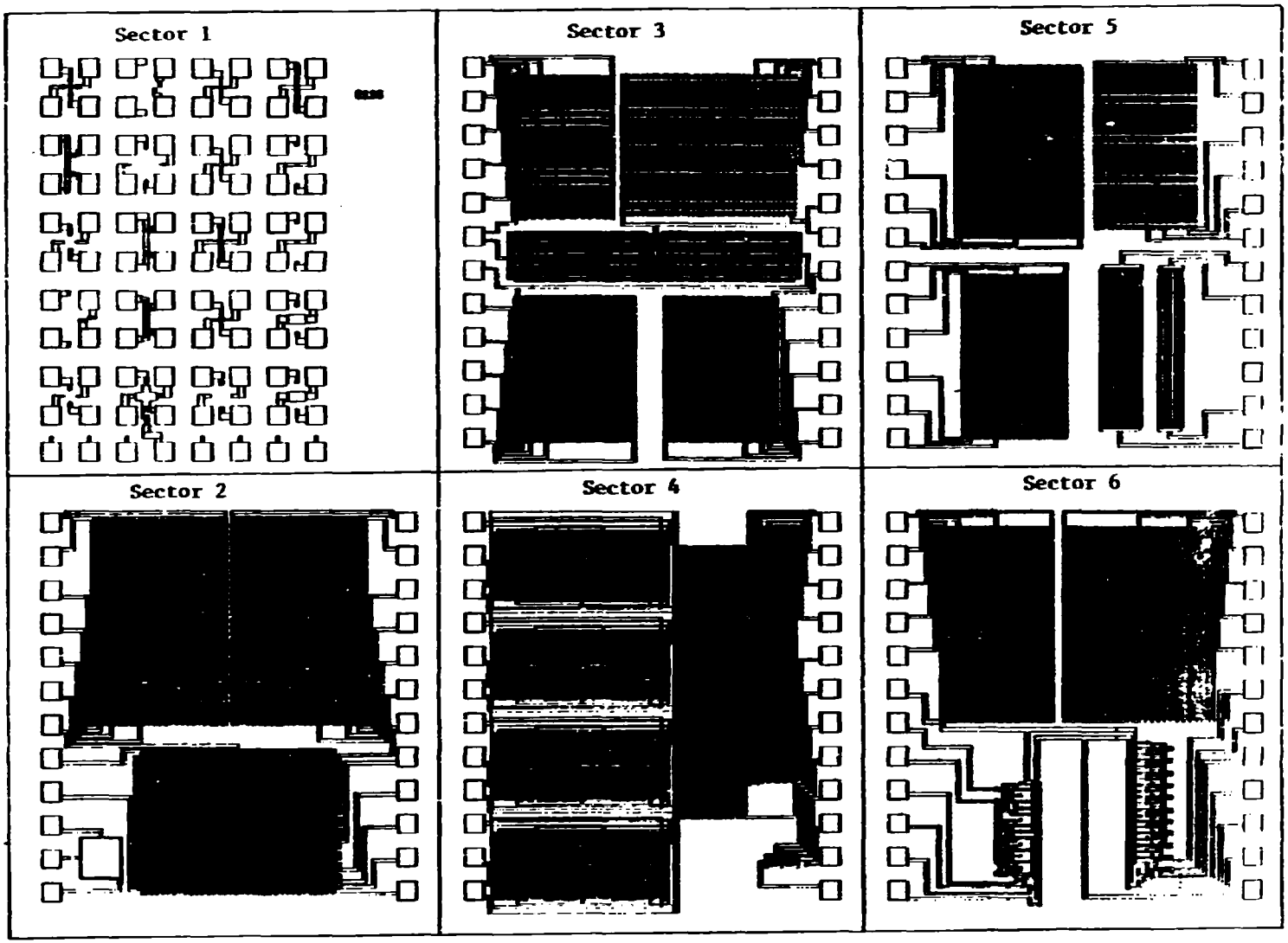


Figure 2-8. E115 Metallization Development Test Mask.

2.2.1 Sector 1 Description

The first sector (Figure 2-9) provides a means of monitoring many of the processing variables that could be of interest in developing the metallization system and improving the high temperature performance of the integrated circuits. In general, the structures in this sector can be used to monitor the sheet resistance of the various diffusions, resistors, and metal layers. In addition, the contact resistance between the metal layers and the various elements which they normally touch may also be monitored. A listing of these structures is given in Table 2-2.

Table 2-2. Test Elements Located in Sector 1 of E115 Mask Set.

Location Call Out	Structure Description	Measurement Purpose
A1	Greek Cross	Shallow n^+ Sheet Resistance
A2	Van der Paul	Shallow n^+ Sheet Resistance
A3	Greek Cross	Base Sheet Resistance
A4	Van der Paul	Base Sheet Resistance
A5	Greek Cross	Oversized Base Implant Resistance
B1	Van der Paul	Oversized Base Implant Resistance
B2	Greek Cross	Epi Layer Sheet Resistance
B3	Van der Paul	Bottom Metal Sheet Resistance
B4	Van der Paul	Top Metal Sheet Resistance
B5	Greek Cross	Pinch-off Base Sheet Resistance
C1	Greek Cross	Bottom Metal Sheet Resistance
C2	Greek Cross	Top Metal Sheet Resistance
C3	Greek Cross	Top and Bottom Metal Resistance
C4	Greek Cross	Top to Bottom Metal Contact Resistance
C5	Greek Cross	Thin Film Resistance
D1	Greek Cross	Bottom Metal to Shallow n^+ Contact Resistance
D2	Greek Cross	Bottom Metal to Base Contact Resistance
D3	Greek Cross	Bottom Metal to Implanted Base Contact Resistance
D4	Greek Cross	Bottom Metal to Epi Layer Contact Resistance
D5	Greek Cross	Top Metal to Epi Layer Contact Resistance

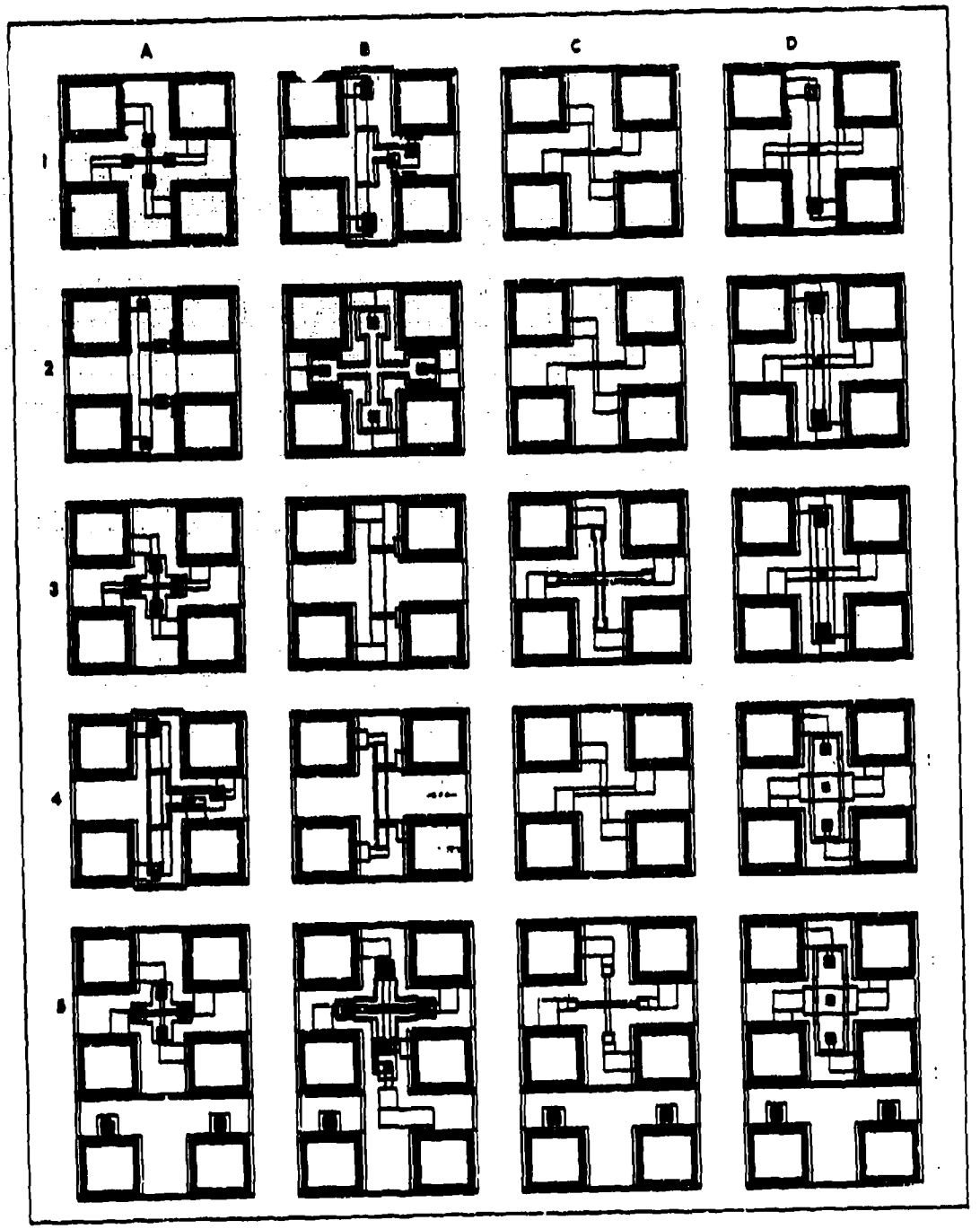


Figure 2-9. Sector 1 of The E115 Test Mask Addresses Process Monitoring and Evaluation.

2.2.2 Sector 2 Description

This is one of the sectors which will be heavily utilised in the development of the dual metallisation system. This particular sector (Figure 2-10) concentrates on the step coverage ability of the two metal levels. The significant features of each sector structure are described as follows:

- (A1) Bottom Metal Continuity Test

  A bottom metal serpentine runs across diffusion stripes. The diffusion stripes are formed by interlacing shallow n+ atop the deep n+ diffusions and base atop the deep p+ diffusions. Each diffusion stripe is 10 um wide with a 10 um spacing. The serpentine is 9 um wide with a 9 um spacing. Contact taps are brought out at 1,300, 3,900, 9,100, 22,100, and 62,400 um.

- (B1) Top Metal Continuity Test

  Same arrangement as bottom metal (above) but material is top metal instead of bottom metal.

- (A2) Capacitor Test

  A capacitor is formed from three conduction layers (top metal - insulator - bottom metal - oxide - shallow n+). The size is 250 x 250 um. This will allow an evaluation of pinhole defects in the dielectric layers and a large enough region for an Auger profile of the dual metal system if needed.

- (B2) Metal-to-Metal Bridge Test

  A top metal serpentine runs over a bottom metal serpentine with diagonal diffusion stripes underneath. This is a combined test for metal-to-metal shorts and open metal lines.

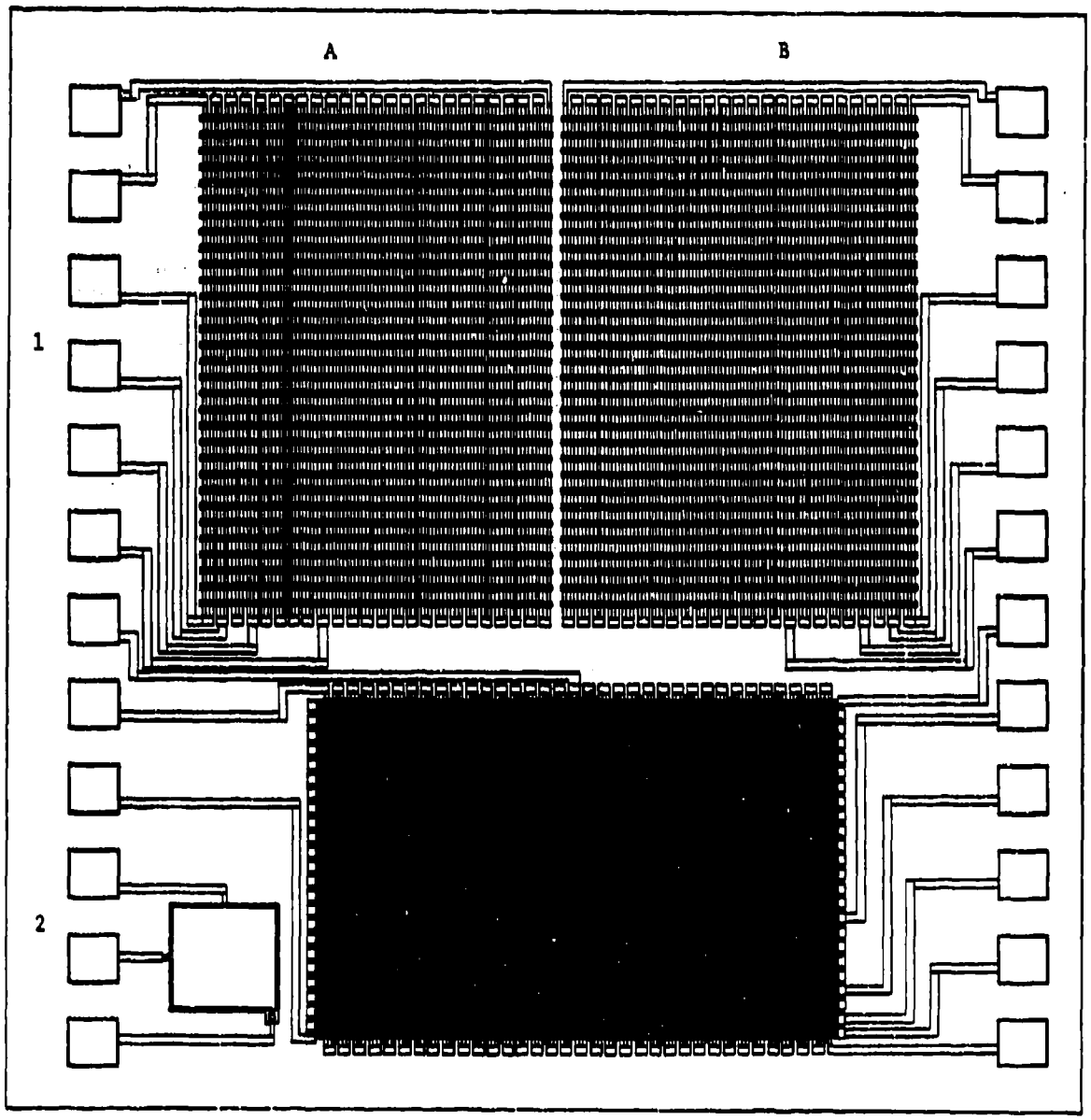


Figure 2-10. Sector 2 of the E115 Test Mask Addresses Step Coverage Evaluation.

2.2.3 Sector 3 Description

This group of test elements (shown in Figure 2-11) will be used to evaluate contacts between the metal layers and contacts to various active and passive devices. In addition, metal patterning ability will be evaluated using the interdigitated fingers. The 6 um epi bipolar process design rules are used. The sector structures are described as follows:

- (A1) Metal/Thin Film Resistor Continuity Chain

  Evaluates contact integrity and potential yield between bottom metal and thin film resistors. Thin film resistors are 9 um wide. The bottom metal overlap of the thin film resistor is 9 x 11 um. The chain is tapped out after 38, 76, 152, 304, and 1026 contacts.

- (B1) Metal/Base Contact Continuity Chain

  Evaluates contact integrity and potential yield for a series of contacts between base material (ion implant optional) and bottom level metal. All contact openings are 8 x 8 um with a metal overlap of 2 um (6 um design rules). The chain is tapped out after 30, 60, 120, 240, and 1020 contacts.

- (A2) Top Metal Interdigitated Lines

  Evaluates patterning capability for a series of parallel lines and the occurrence of shorts between adjacent runs. The fingers are 9 um wide with a spacing of 9 um. Each finger is 875 um long.

- (B2) Bottom Metal Interdigitated Lines

  Fingers are 9 um wide; spacing is 9 um; length is 875 um. (Same as for top level metal.)

- (A3) Metal/Metal Contact Continuity Chain

  Provides a via integrity test between top metal and bottom metal. Each via is 8 x 8 um with a 2 um top metal overlap. The chain has taps brought out after 34, 68, 136, 272, and 1030 contacts.

- (B3) Metal/Shallow n+ Contact Continuity Chain

  Provides a chain of contacts between bottom metal and the shallow n+ diffusion layer. Each contact opening is 8 x 8 um with 2 um of metal overlapping the contact opening. The chain has taps brought out after 36, 72, 144, 288, and 1008 contacts.

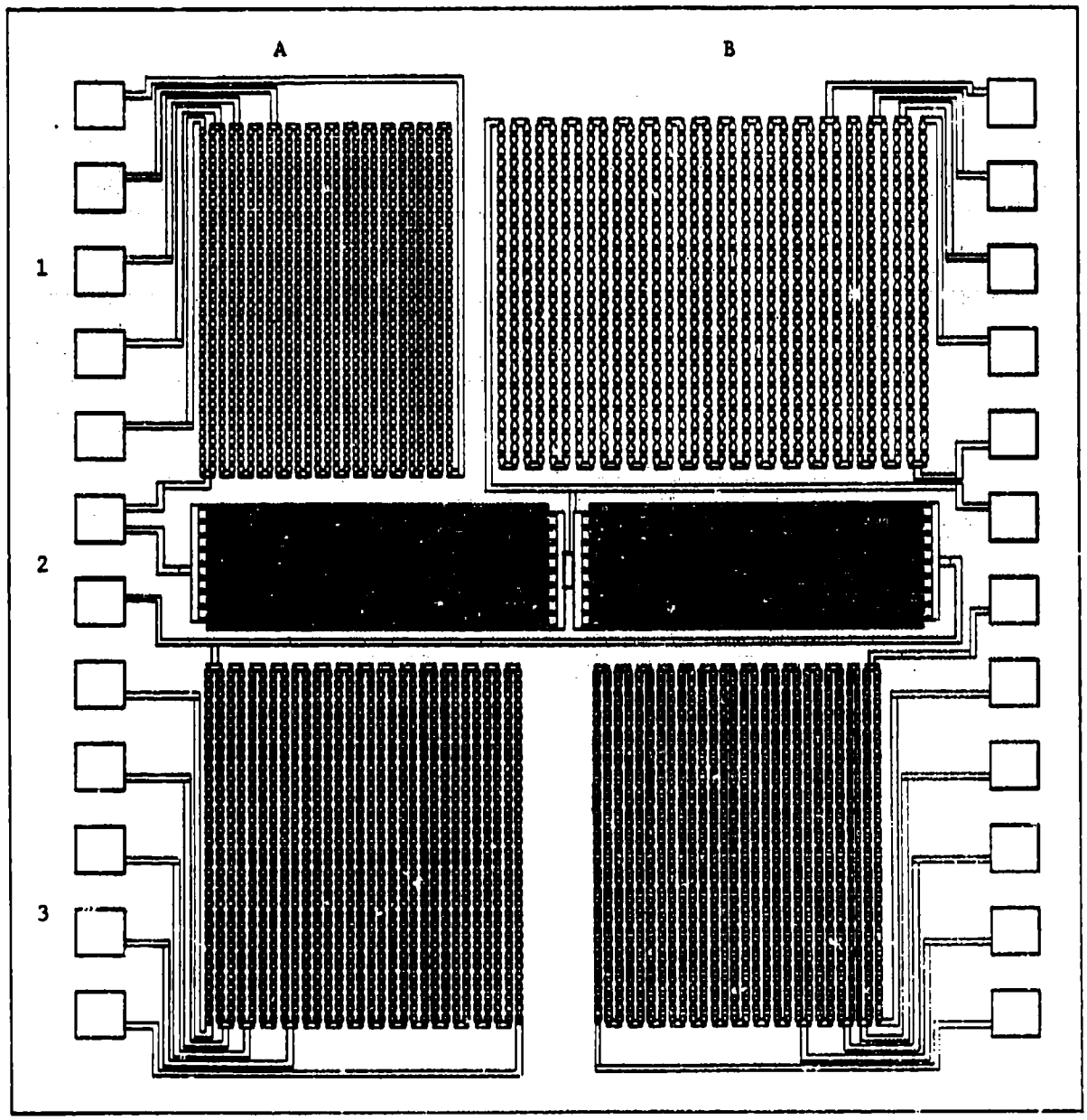


Figure 2-11. Sector 3 of the E115 Test Mask Addresses Evaluation of Inter-Layer Vias and Contacts to Various Active and Passive Devices.

2.2.4 Sector 4 Description

This sector contains the test elements (Figure 2-12) that will be employed in the MSI complexity high temperature life test demonstration. Nominal design rules for the 6 um epi bipolar process are used. Also, a single I^2L gate has connections brought out for processing evaluation, and metallization structures are included for high temperature evaluation during the demonstration. The sector structures are described as follows:

- (A1 to A4) MSI Complexity High Temperature Demonstration

  This consists of an integrated seven-stage ring oscillator and four-bit binary counter. A clock is generated by a seven-stage I^2L ring oscillator. The clock frequency is counted down by a factor of 16 through four toggle flip flops. The resulting signal pulses are buffered and brought out to a pad for monitoring.

- (B1) Bottom Metal Continuity Test

  The serpentine is constructed of a metal run 9 um wide with a 9 um spacing. The total length is 34 mm with alternating base on p-iso and emitter on n+ sinker diffusion steps underneath.

- (C1) Metal/Metal Contact Continuity Chain

  Via integrity test between top and bottom metal. Each via is 8 x 8 um with 2 um top metal overlap and a 4 um bottom metal overlap. The serpentine is tapped out after 60, 120, 240, and 660 vias.

- (C2) I^2L Evaluation Gate

  All necessary connections to a pair of dual-collector I^2L gates are brought out to the pads for process evaluation.

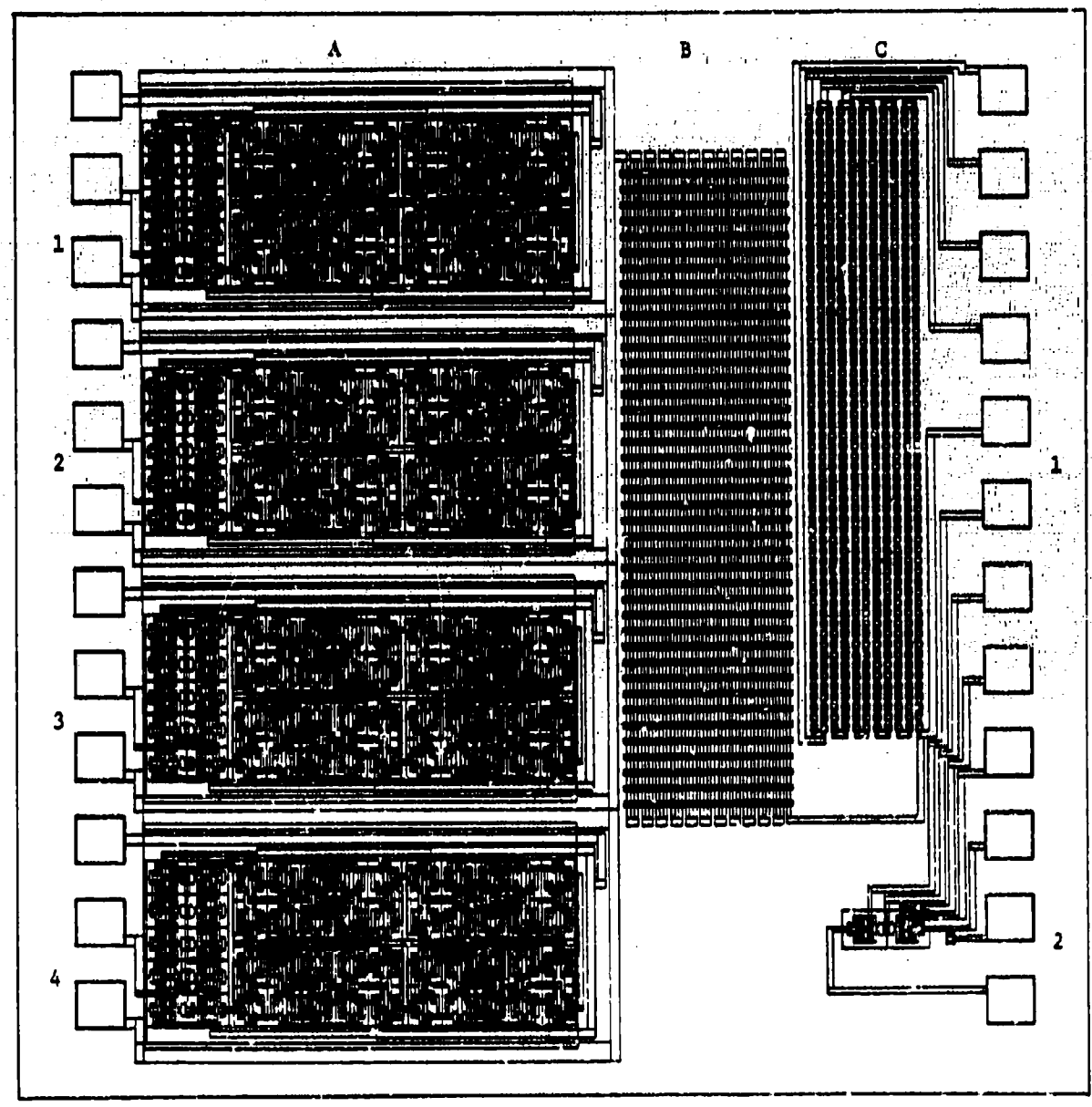


Figure 2-12. Sector 4 of the E115 Test Mask Provides MSI Specimens for Life Testing.

2.2.5 Sector 5 Description

This group (Figure 2-13) evaluates some of the more conservative and some of the more aggressive design rules. The sector structures are described as follows:

- (A1) Metal/Metal Contact Continuity Chain

  Via integrity test with conservative metal overlap rules. Via openings are 8 x 8 um with a 5 um top metal overlap and a 6 um bottom metal overlap. The serpentine is tapped out after 36, 72, 288, 468, 972 vias.

- (A2) Metal/Metal Contact Continuity Chain

  Via integrity test with aggressive design rules. Via openings are 5 x 4 um with a 5 um top metal overlap and a 6 um bottom metal overlap. The serpentine is tapped out after 40, 80, 320, 520, and 1000 vias.

- (B1) Thin Film Resistor/Metal Continuity Chain

  Contact integrity test between thin film resistor and bottom metal with aggressive design rules. The thin film resistor material is 6 um wide. The overlap area between bottom metal and thin film resistor is 10 x 6 um. The serpentine is tapped out after 40, 80, 320, 400, and 1000 contacts.

- (B2) Top Metal Interdigitated Lines (not visible on figure)

  Interdigitated fingers for patterning evaluation of aggressive metal design rules. Fingers of top metal are 10 um wide and spaced 5 um apart. The total finger length is 1000 um.

- (C2) Bottom Metal Interdigitated Lines

  Interdigitated fingers for patterning evaluation of aggressive metal design rules. The fingers of bottom metal are 6 um wide and spaced 3 um apart. The total finger length is 1000 um.

- (D2) Thin Film Resistor

  Thin film resistor 25 by 250 um (10 squares) with a substantial bottom level metal overlap contact to each end.

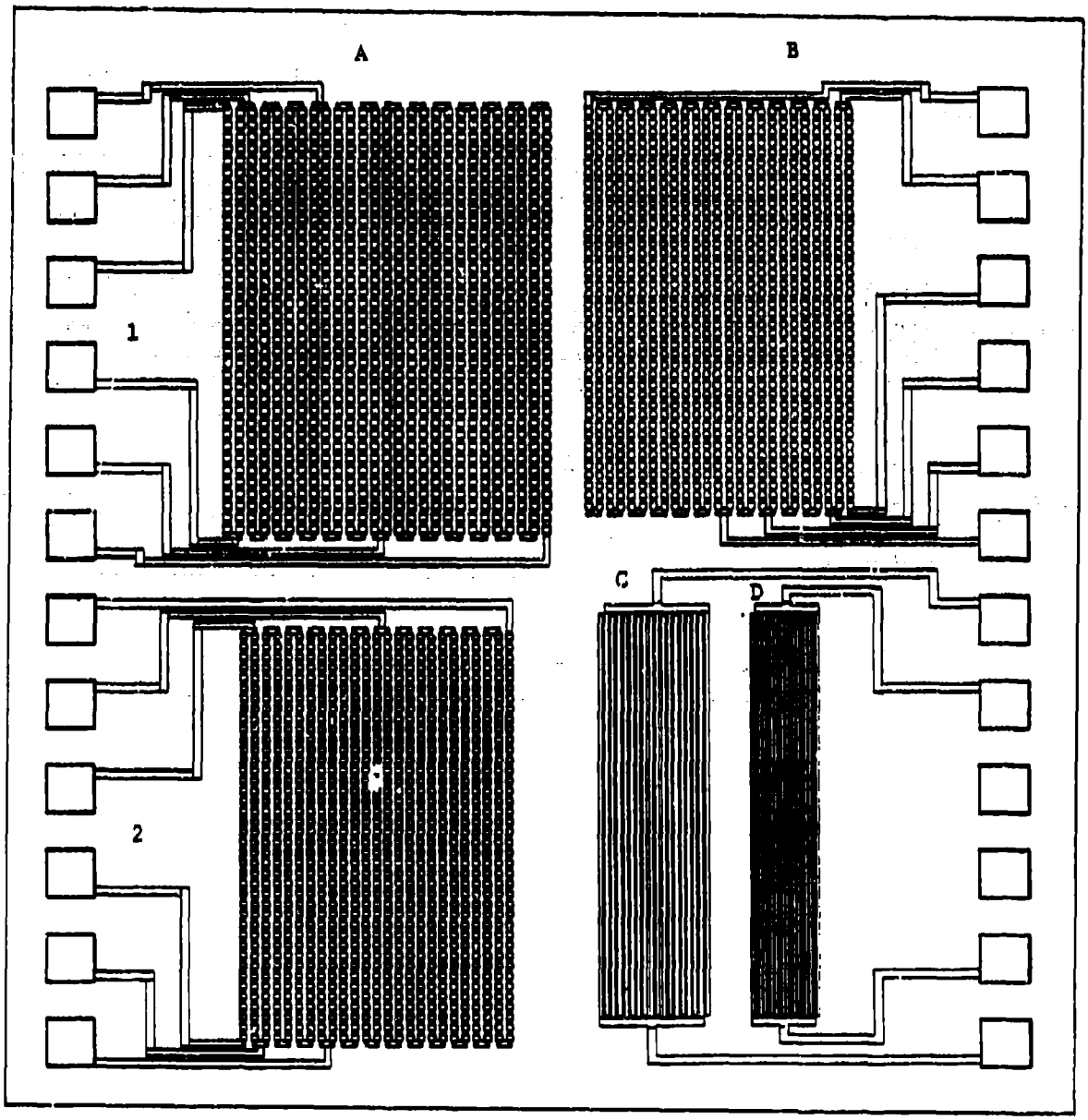


Figure 2-13. Sector 5 of the E115 Test Mask Addresses Evaluation of Various Design Rules.

2.2.6 Sector 6 Description

This sector (Figure 2-14) evaluates patterning ability using conservative design rules and Integrated Schottky Logic (ISL). The integrated Schottky gates will need special processing to open the collector contacts through the thicker field oxide so these circuits will not always be available. The various sector structures are described below.

- (A1) Bottom Metal Continuity Test

  This continuity test evaluates narrow bottom metal lines with the spacings so that there is a high probability that they can be patterned. The metal serpentine is 6 um wide with a 9 um spacing. Taps are brought out at 1,200, 2,400, 9,600, 28,800, and 57,600 um intervals.

- (B1) Top Metal Continuity Test

  This continuity test of top metal uses conservative design rules. The serpentine metal line is 10 um wide with a 10 um spacing. It is tapped out after 1,200, 2,400, 9,600, 28,800, and 57,600 um.

- (A2) ISL Toggle Flip-Flop

  A one-bit toggle flip flop is implemented with ISL which utilizes the Schottky diodes between the bottom metal and the epi region in the gate's collector. Current mirrors are used as power source.

- (B2) ISL Ring Oscillator

  A nine-stage ring oscillator and a one gate test cell were constructed using integrated Schottky logic. Current mirrors are used to power the ISL gates. One ISL gate has all its connections brought out to pads for external evaluation.

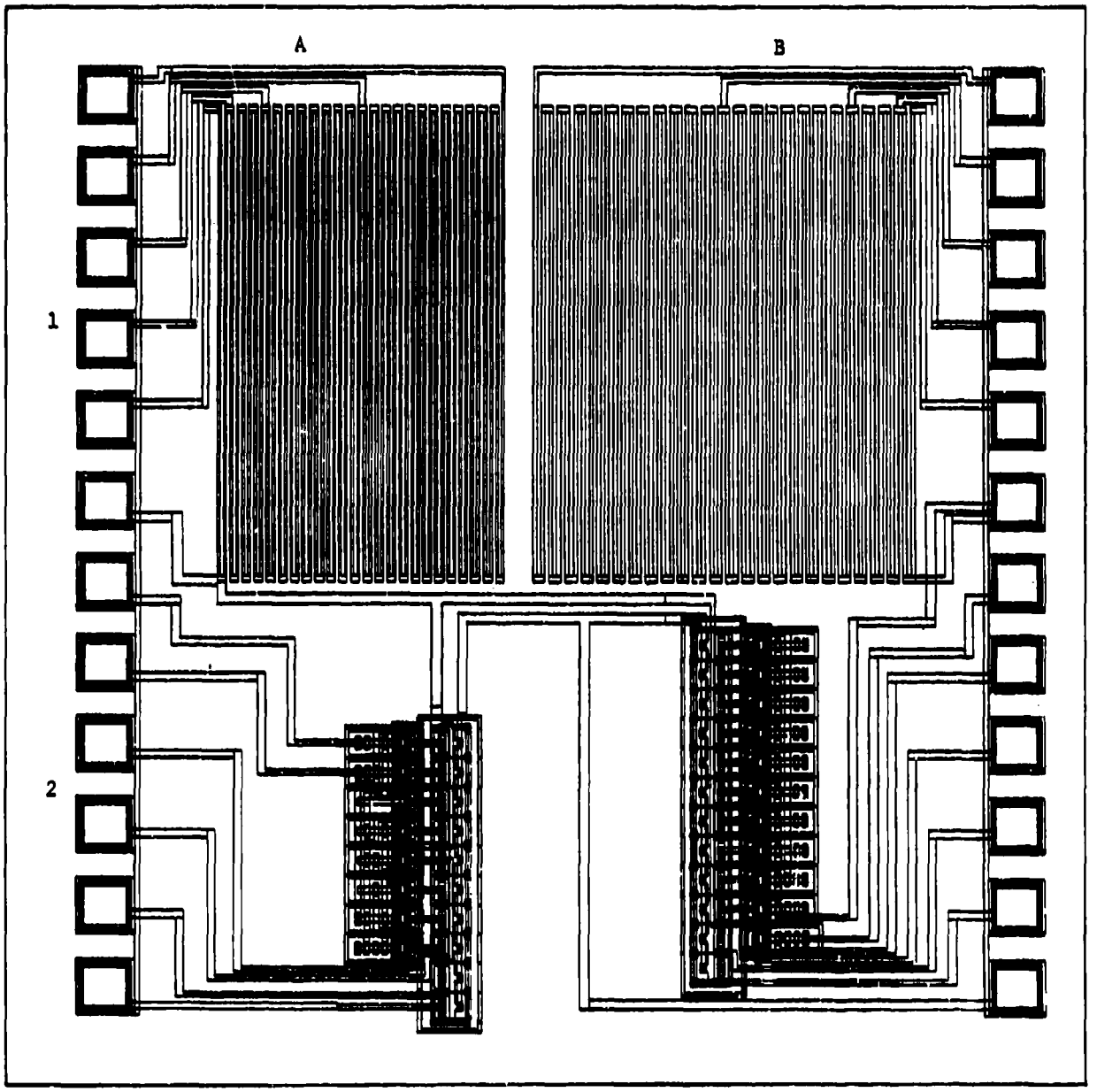


Figure 2-14. Sector 6 of the E115 Test Mask Enables Evaluation of Conservative Design Rules and ISL Gate Evaluations.

3.0 HIGH TEMPERATURE METALLIZATION DEVELOPMENT

The intrinsic capability of silicon semiconductors to function at the 300° C level was established during Phase I of this program. The metallisation development, however, has turned out to be far more difficult than initially contemplated and has received a major portion of the program development effort over the past several years. This section of the report describes the metallisation development progress that was accomplished during this program phase.

Section 3.1 describes the metallisation status at the beginning of the program phase. Auger electron spectroscopy accomplished during a 2000-hour 300° C evaluation provided a preliminary indication that the diffusion barrier capabilities of the metallisation system were satisfactory.

Section 3.2 describes the shortcomings of the diffusion barrier which became apparent when accelerated testing at 350° C was initiated. The use of nitrogen to "stuff" the Ti-W grain boundaries as a solution to the diffusion problem and the development of an optimum sputtering deposition process are described. This section also discusses the elimination of the stuffing at the silicon oxide interface as a solution to the resulting adhesion problem.

Section 3.3 describes the experiments which substantiated that internal stress in the metallisation resulting from differential thermal expansion was the driving impetus behind the crystal formation observed in the gold conductive layer. Metallisation deposition at high temperature to eliminate the thermal stress is described in addition to the use of hydrogen doping as a crystal formation retardant. The use of wet chemistry patterning with resultant undercutting, contaminant entrapment, and bubble-void formation is described.

Section 3.4 describes the effort which led to the local elimination of the nitrogen stuffing at the Au/Ti-W interface as the final solution to the metallization adhesion problem.

Section 3.5 specifies in detail the metallisation process which has been developed during this program phase to solve the diffusion, adhesion, voiding, and crystal growth problems which have been encountered.

Section 3.6 describes the preliminary work that was performed to show the feasibility of a dual-level system. The ion milling and lift-off patterning processes are discussed.

3.1 STATUS AT BEGINNING OF PROGRAM PHASE

As this phase was initiated there was a premise that a standard barrier metallisation system could be adopted for the high temperature integrated circuit metallisation for the program. Two candidates were (1) a platinum silicide/titanium (10%)-tungsten/gold barrier metal system and (2) a chromium/molybdenum/gold barrier metal system. Initial investigations indicated that both metal systems were capable of extended operation at 300° C. However, patterning problems, adhesion problems, and a need for accelerated life testing above 300° C eventually necessitated the development of an improved metallisation.

Both metallisation systems which were investigated were comprised of three individual layers: the bottom layer (platinum silicide or chromium/chromium silicide) is intended to form ohmic and metallurgical contact to the silicon semiconductor, a top layer of gold provides low impedance electrical interconnection between regions of the silicon chip, and the middle layer (titanium-tungsten or molybdenum) provides a diffusion barrier between the silicon and gold layers. The diffusion barrier properties may be improved by the addition of a grain boundary stuffing material such as oxygen or nitrogen. In many cases, oxygen is naturally incorporated into the barrier as a contaminant from the sputtering system.

Both metallisation systems were studied using auger electron spectroscopy (AES) before and during an extended annealing cycle at 300° C. The information plotted from the AES profiles are the signal intensity and the sputtering time. Thus the relative percentage composition of a layer may not be determined from

these results. However, the AES profiles do provide relative positional indications of the various metallization layers. Figures 3-1 through 3-4 show profiles taken before, during, and after annealing at 300° C for 2000 hours. The Ti-W diffusion barrier is intact afer 2000 hours at 300° C and appears to be stable.

The AES profiles of the Cr/Mo/Au system are shown in Figures 3-5 through 3-8. Profiles are shown for the as-sputtered sample and at various times during the subsequent anneal. The oxygen present on the diffusion barrier layer is believed to stuff the molybdenum grain boundaries, thus suppressing the interdiffusion.

Both metallization systems provided satisfactory barrier properties for long periods of time at 300° C as can be seen in Figures 3-4 and 3-8. However, problems with the barrier metal adhesion to the chips, the ability to pattern the metal system for integrated circuit interconnect, and the ability of the metal system to withstand the rigors of the higher temperatures required for accelerated life testing mandated that further improvements be made.

3.2 IMPROVEMENTS TO DIFFUSION BARRIER SYSTEM

The goal of 10,000 hours operation at 300° C can only be demonstrated through accelerated life testing. With this in mind, samples of the titanium-tungsten barrier metallization system on blank wafers with platinum silicide were annealed in a diffusion furnace for 50 and 100 hours at 350° C. All samples had platinum silicide formed on blank silicon wafers. Then the titanium-tungsten diffusion barrier was sputtered down at 200 W (1.09 W/cm^2) in a 10 micron argon atmosphere in both a static mode, where the wafers remain stationary beneath the target, and a dynamic mode, where the wafers rotate on a carousel passing under the target once per revolution. After depositing 2500 A of barrier, the top gold layer was deposited (5000 A also sputtered).

These samples were annealed for 50 and 100 hours at 350° C in a furnace with a nitrogen ambient. The results shown in Figures 3-9 and 3-10 were encouraging but not up to the required standards. The dark region in the dynamically deposited wafer shown in Figure 3-9 is, in reality, a specular surface; while the lighter colored statically deposited wafer has a slightly

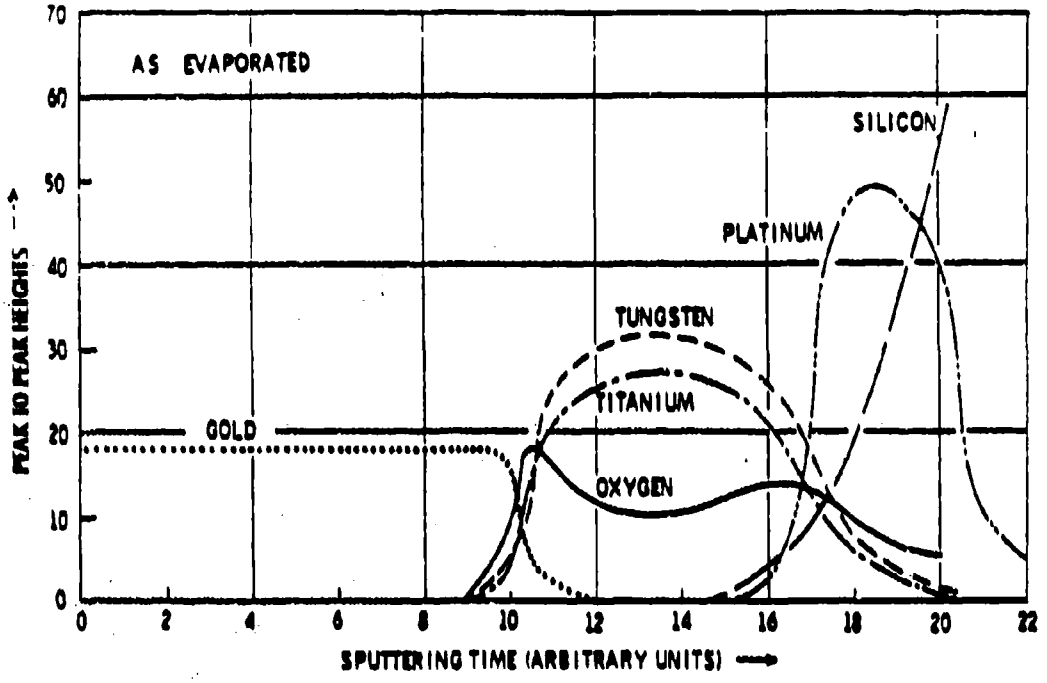


Figure 3-1. AES Profile of PtSi/Ti-W/Au Metal System as Deposited.

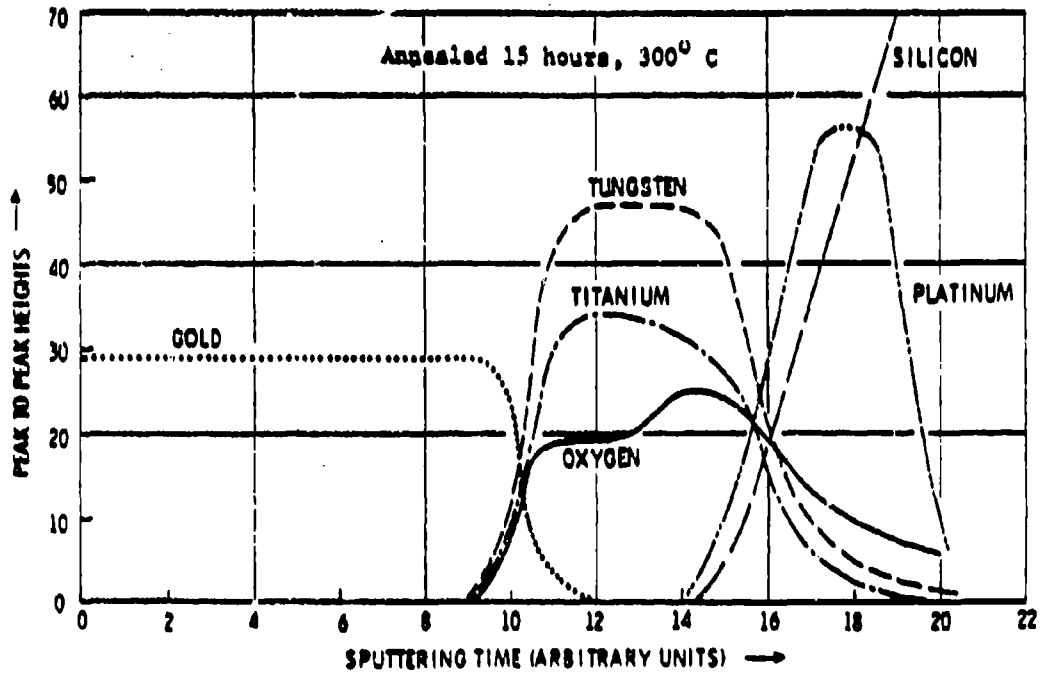


Figure 3-2. AES Profile of the PtSi/Ti-W/Au Metal System After Annealing 15 Hours at 300° C.

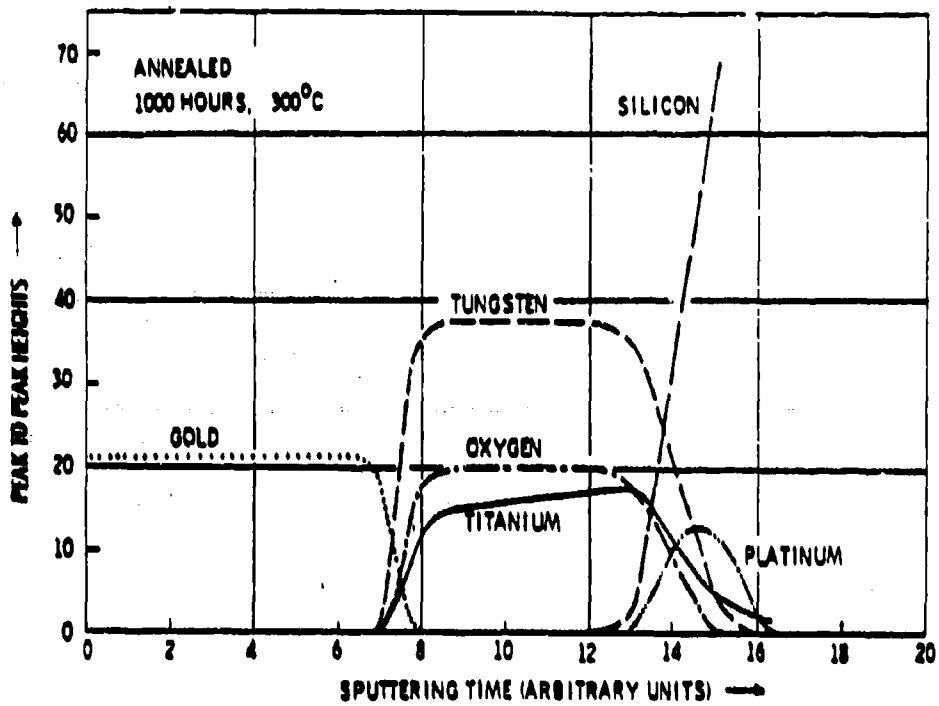


Figure 3-3. AES Profile of the PtSi/Ti-W/Au Metal System After Annealing 1000 Hours at 300° C.

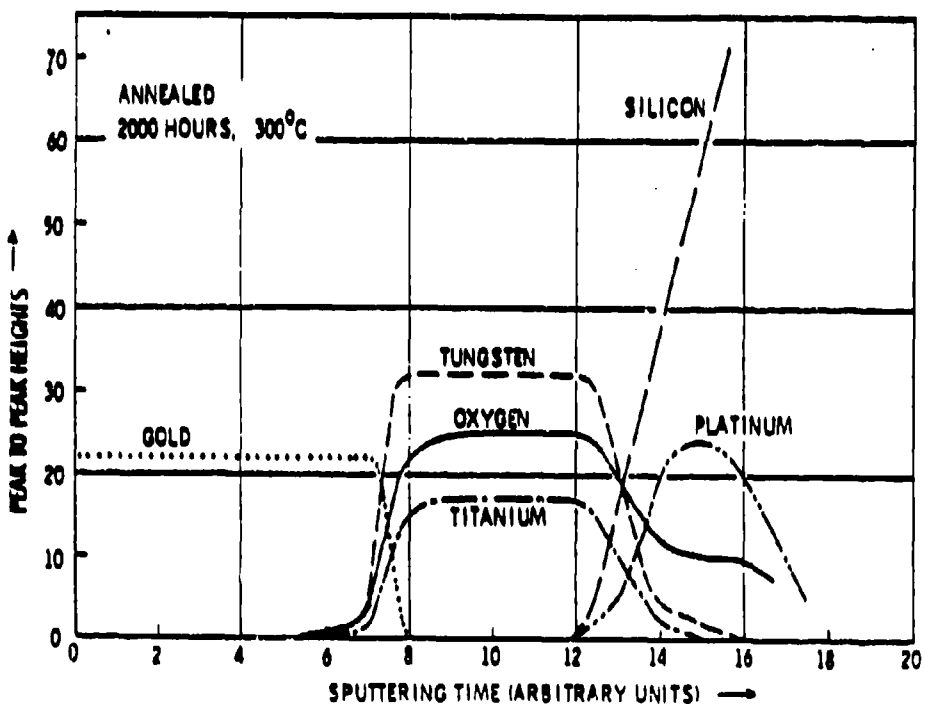


Figure 3-4. AES Profile of the PtSi/Ti-W/Au Metal System After Annealing 2000 Hours at 300° C.

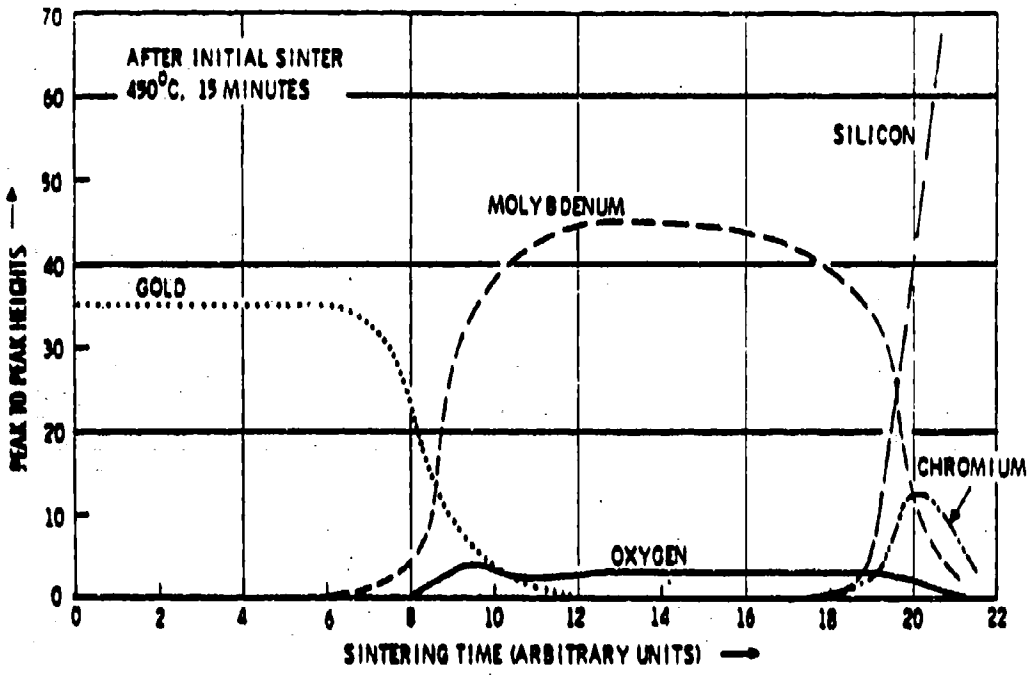


Figure 3-5. AES Profile of the Cr/Mo/Au Metal System After Deposition and the Initial Sinter.

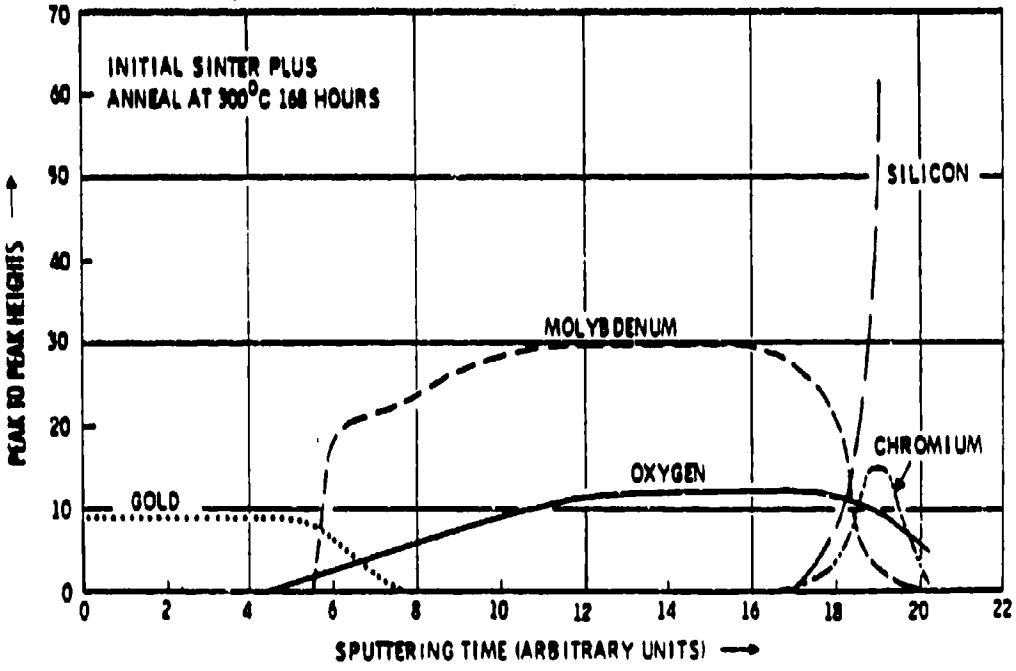


Figure 3-6. AES Profile of the Cr/Mo/Au Metal System After Annealing 168 Hours at 300° C.

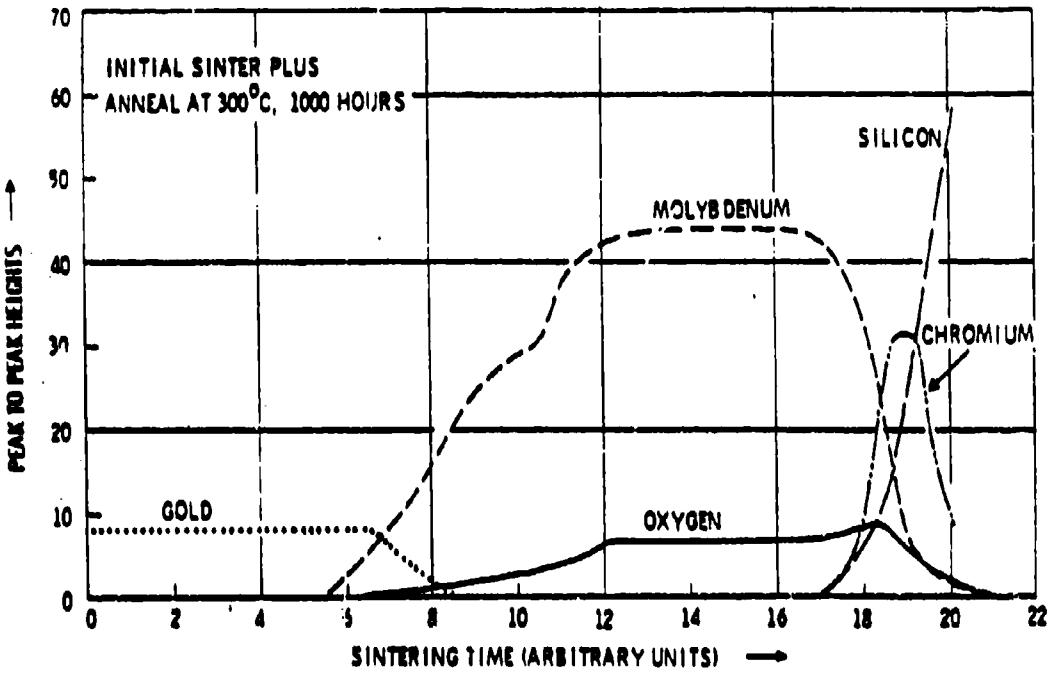


Figure 3-7. AES Profile of the Cr/Mo/Au Metal System After Annealing 1000 Hours at 300° C.

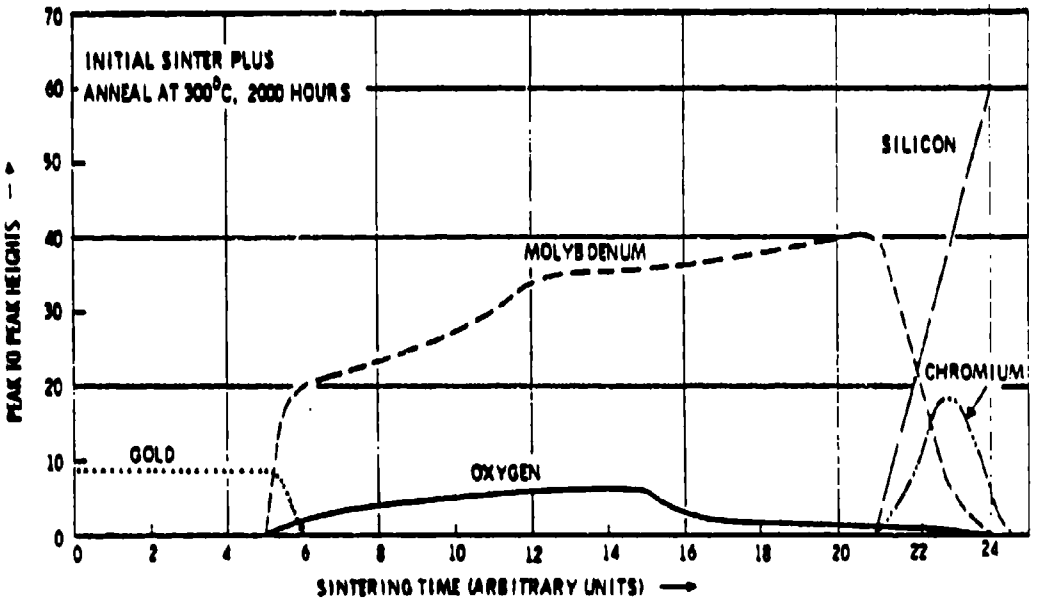


Figure 3-8. AES Profile of the Cr/Mo/Au Metal System After Annealing 2000 Hours at 300° C.

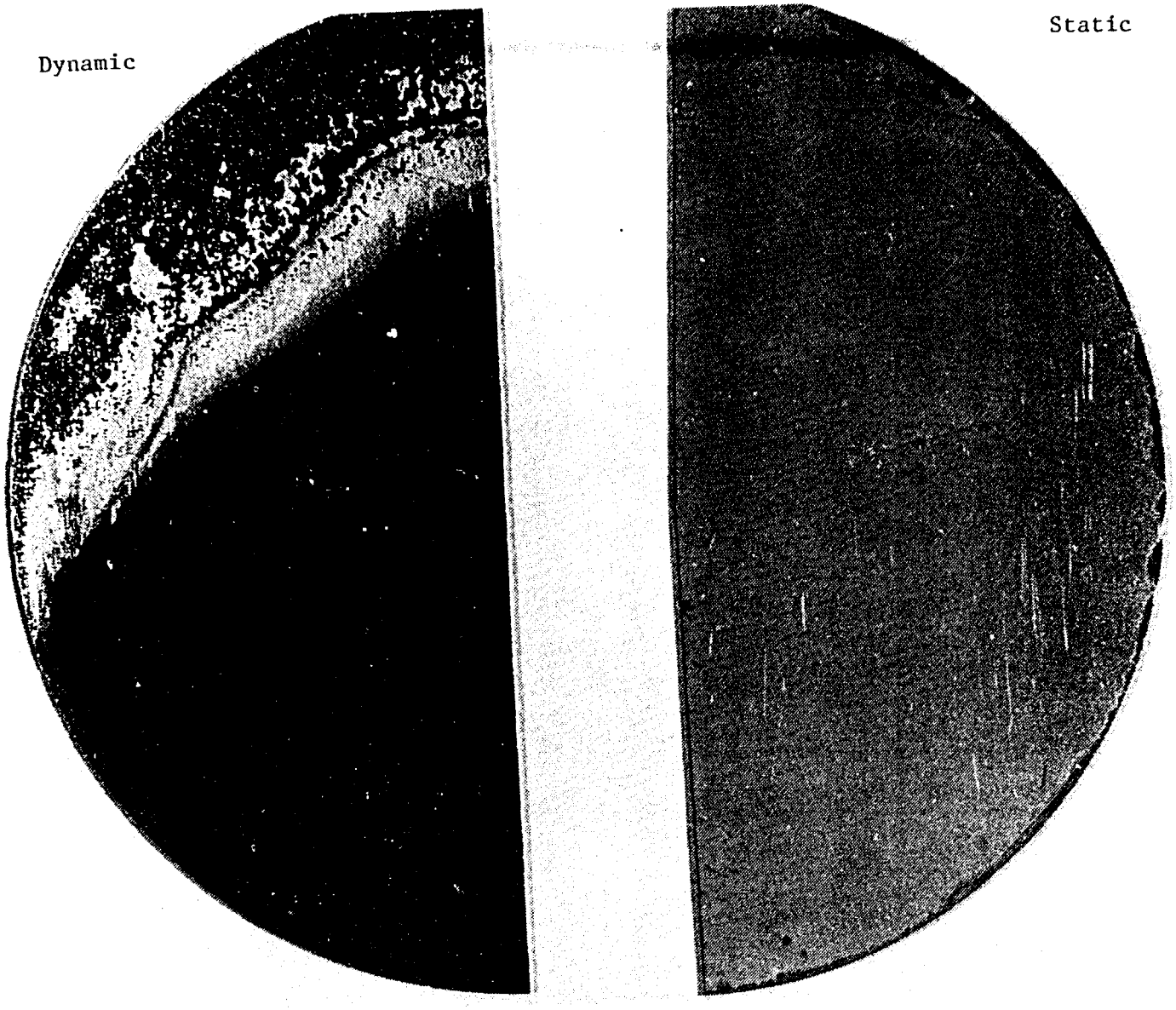


Figure 3-9. Ti-W Barrier Metallization System After Annealing 50 Hours at 350° C.

Dynamic

Static

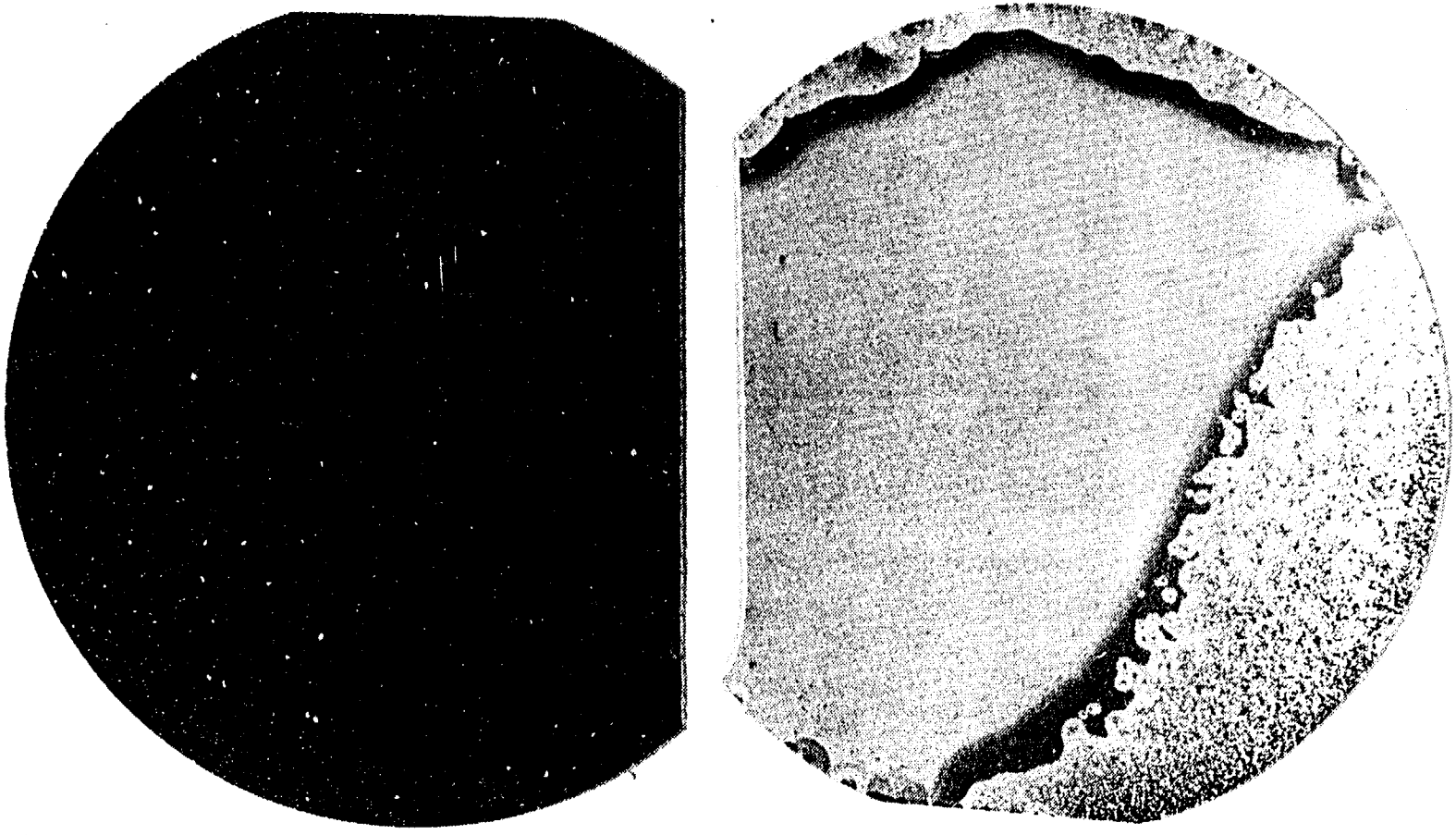


Figure 3-10. Ti-W Barrier Metallization System After Annealing 100 Hours at 350° C.

grainy feature when viewed under high magnification. The circular patterns are a result of the gold and silicon intermixing through point defects in the barrier.

The properties of the barrier metallization system needed to be improved to enable long term accelerated life testing at temperatures approaching 350° C. Previous investigations reported in the literature indicated that either oxygen or nitrogen could be incorporated in the titanium-tungsten barrier via reactive sputtering (Reference 3). In addition, it has been shown that pure titanium-tungsten films form relatively poor diffusion barriers to gold (Reference 4). The work reported by Baker et al. (Reference 5) shows that the incorporation of oxygen into the diffusion barrier produces a barrier resistant to silicon and gold diffusion up to 400° C.

At this point, it was decided to concentrate the effort on the PtSi/Ti-W/Au metal system. This decision was not arbitrary but was based on the projected improvements of the Ti-W based system relative to the chromium/molybdenum barrier system. After this decision was made, a report (Reference 6) was found in the literature indicating that nitrogen stuffed molybdenum was as effective as nitrogen stuffed Ti-W for a diffusion barrier. However, judging from the relative number of publications, it was felt that the Ti-W approach provided a higher probability of success for the program.

The titanium-tungsten barrier properties were improved as a result of a series of deposition experiments. In a static mode, the wafers remain under the target and the titanium-tungsten barrier was sputtered down with a power of 300 W (4 inch target) on blank silicon wafers upon which platinum silicide had already been formed. Nitrogen partial pressures of 0, 0.4, 1.0, and 5.0 microns were used in four test runs where the sputtering pressure was raised to 10 microns with argon supplementing the nitrogen. After annealing for 100 hours at 350° C in a nitrogen ambient, the film which had been sputtered at 1.0 micron nitrogen partial pressure looked the best but still showed some signs of barrier breakdown.

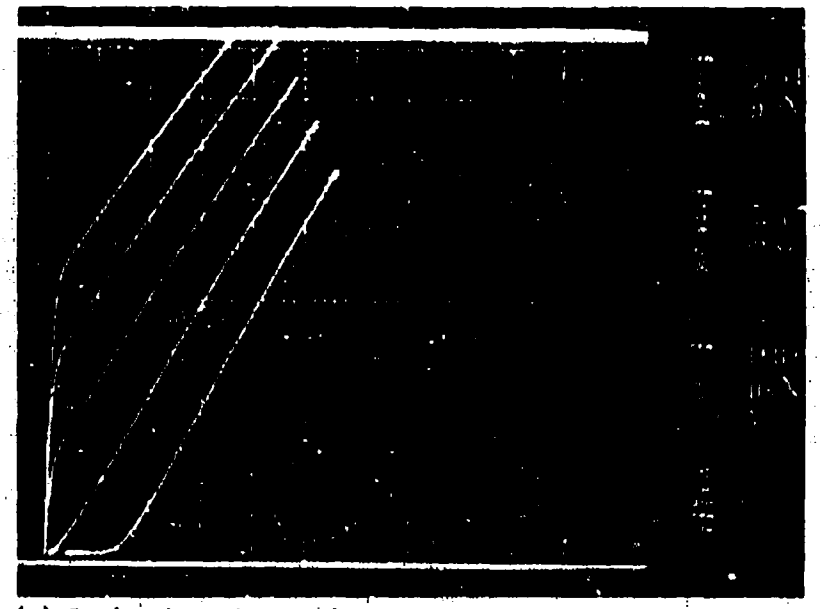
A second deposition matrix was fabricated using a 1.0 micron nitrogen partial pressure with enough argon to bring the system pressure up to 10 microns. The deposition power was varied in the following steps: 100, 300,

500, and 1000 Watts. After annealing for 100 hours at 350° C in nitrogen, the 1000 Watt 1.0 micron nitrogen stuffed sample demonstrated the best stable barrier capability.

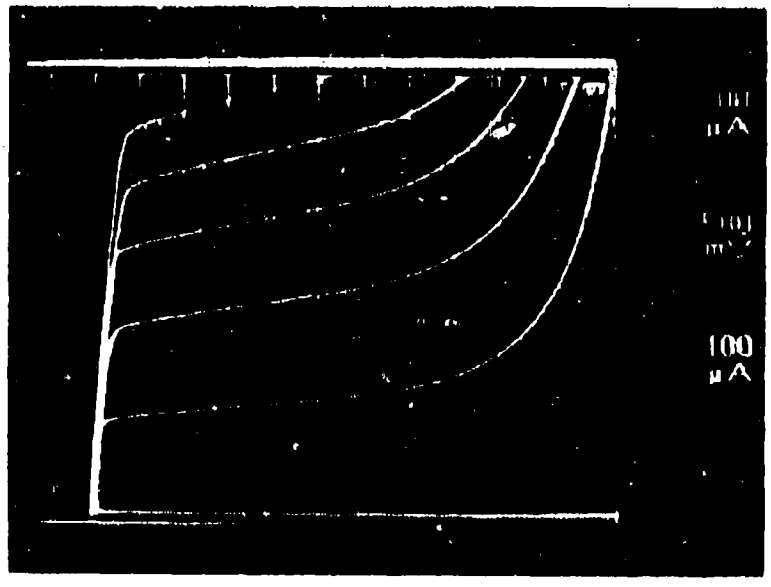
A Ti-W barrier which was deposited in a 1.0 micron nitrogen and 9.0 micron argon partial pressure at a 1000 Watt deposition power using an 8-inch target demonstrated excellent stability. This became the standard gold/silicon diffusion barrier for this project. However, it soon became apparent that selectively etching the nitrogen stuffed titanium-tungsten layer was difficult with wet chemistry techniques. Normal etch cycles would leave a thin remnant layer of titanium-tungsten over the dielectric area of the chip which resulted in apparently "leaky" active devices. Attempts at completely etching the thin layer resulted in undercutting the metallization. Figure 3-11(a) shows the integrated injection logic gate transistor characteristics on a wafer with this leakage problem. From the figure, the total resistance between collector and base contact can be deduced to be about 7000 ohms (assuming a transistor gain of 10). Although this is a large resistance, it did not pose a significant problem for logic gate operation.

Another problem which became apparent after the first life test with the initial metallization system was that there was poor adhesion between the titanium-tungsten metal and the field silicon dioxide. This problem was partially attributed to the undercutting of the metallization but was also a factor in large metal regions which would not be significantly affected by undercutting. Figure 3-12 shows the results of a tape peel test on an electromigration test cell. The poor adhesion was thought to be a result of the nitrogen doping of the barrier which modified the tenacity of the Ti-W diffusion barrier to adhere to the wafer oxide.

In the end, the simple addition of an oxidizing cleaning step and the employment of an undoped sublayer of titanium tungsten for about 10% of the total barrier thickness (200 A) before the deposition of the main barrier solved the adhesion problems. Also, since the undoped titanium tungsten tends to etch faster than the doped barrier material, the final sublayer was removed completely without overetching or leaving a thin resistive film. The barrier metallization system cross section at this point in the program is shown in



(a) Leaky Transistor Characteristics Associated with Inadequate Field Metal Removal (Wafer No. 21)



(b) Low Leakage Associated with Process Refinements (Reworked Wafer No. 21)

Figure 3-11. Active Device Characteristics.

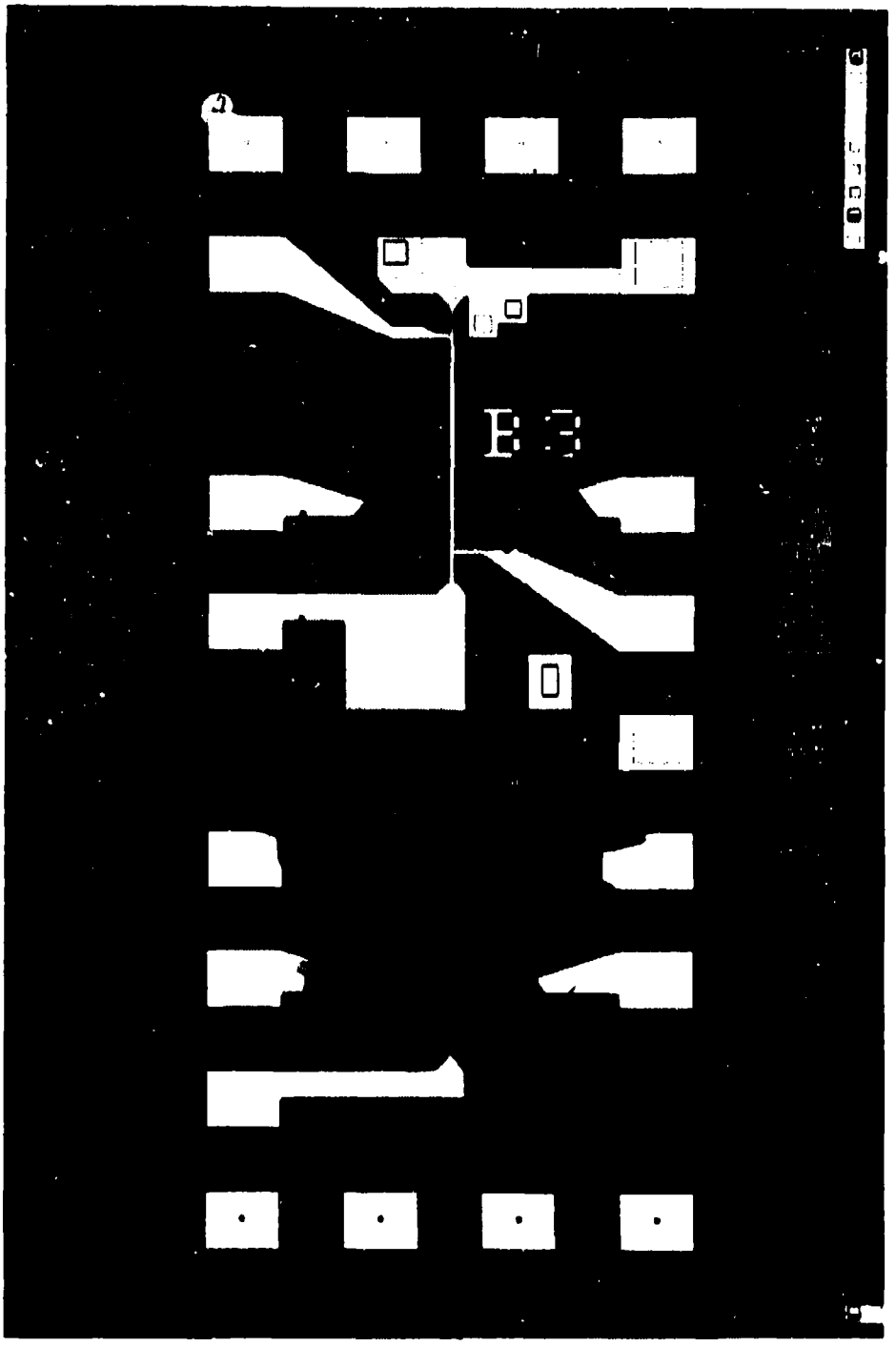


Figure 3-12. Metal Lifting as a Result of a Peel Test Before Any Metallization Improvements Were Implemented.

Figure 3-13. The scale in the figure is distorted to illustrate the details. The total Ti-W barrier thickness is about 2000 to 2500 A with the bottom 10% undoped. The silicon oxide thickness can range from 5,000 to 10,000 A and the top gold layer is currently 5000 A.

The addition of the undoped Ti-W sublayer improved the wet chemistry patterning accuracy of the metal system. Figure 3-14 shows an example of these patterning results on the electromigration test cell. The minimum line width and spacing is 0.2 mil (5 microns). Figure 3-15 shows a closeup of the upper four point probe electromigration test vehicle with a 0.2 mil line, with a 0.2 mil spacing between the electromigration test line, and a 0.2 mil guard line on each side. It will be noted that the center conductor is slightly wider than the outside conductors due to the n-type diffusion cut within which the center conductor is positioned.

Figure 3-16 shows how logic gates and ring oscillator sections appeared on the patterned wafers. The metallisation system (shown typically in Figure 3-13) was patterned using a wet chemistry etching sequence. The narrowest line width in Figure 3-16 is 0.3 mil. A tape peel test removed none of the barrier metallisation. In addition, curve tracer plots of similar sites on all wafers indicate that base collector leakage currents were all less than 0.2 microamperes. Figure 3-11(b) shows the improved electrical performance due to this process compared with leaky characteristics experienced earlier and shown in Figure 3-11(a). The results shown in Figure 3-11 were obtained from the same wafer after the original metallisation was stripped off and reapplied.

For metallisation development, blank silicon wafers completely covered with platinum silicide were utilised for process monitoring of the barrier integrity. One of these 2 inch wafers was annealed for 100 hours at 365° C in a diffusion furnance with a nitrogen ambient. One defect in the barrier metal was examined using the scanning electron microscope. Figure 3-17 shows the edge of the wafer (left) and the defect (lower right) at 20X magnification. The defect size is about 17 mils in diameter. Figure 3-18 shows the defect area at 200X magnification. A depression is visible in the center of the defect region where the gold layer was diffused down through a channel in the

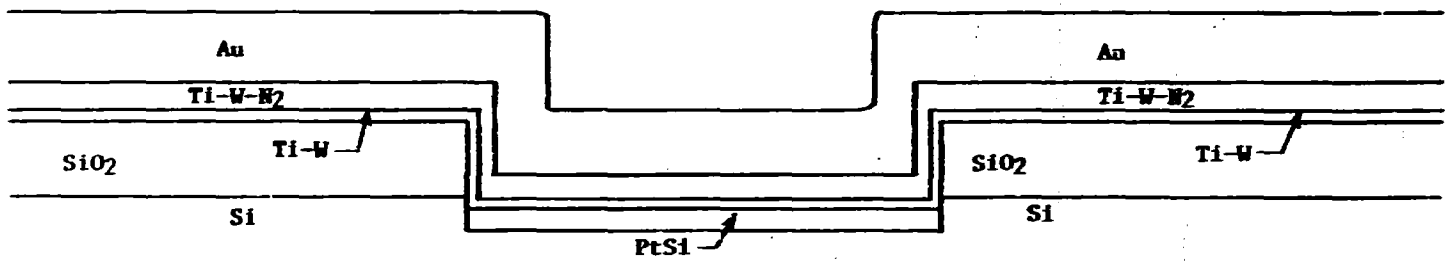


Figure 3-13. Cross Section of Diffusion Barrier Metallization System Showing Barrier Metal on the Field Oxide and the Platinum Silicide Ohmic Contacts to the Silicon Substrate.

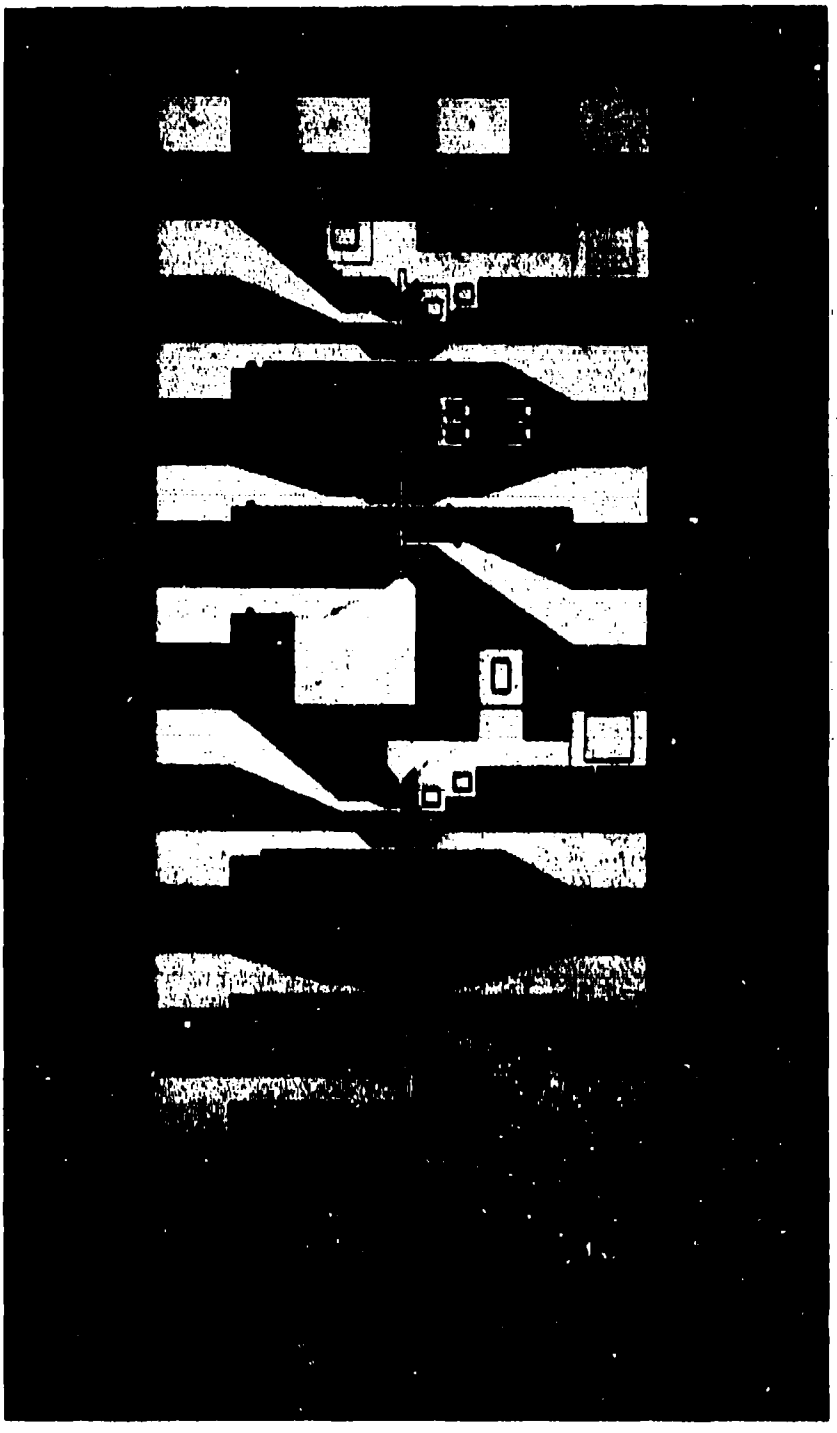


Figure 3-14. Electromigration Test Cell.

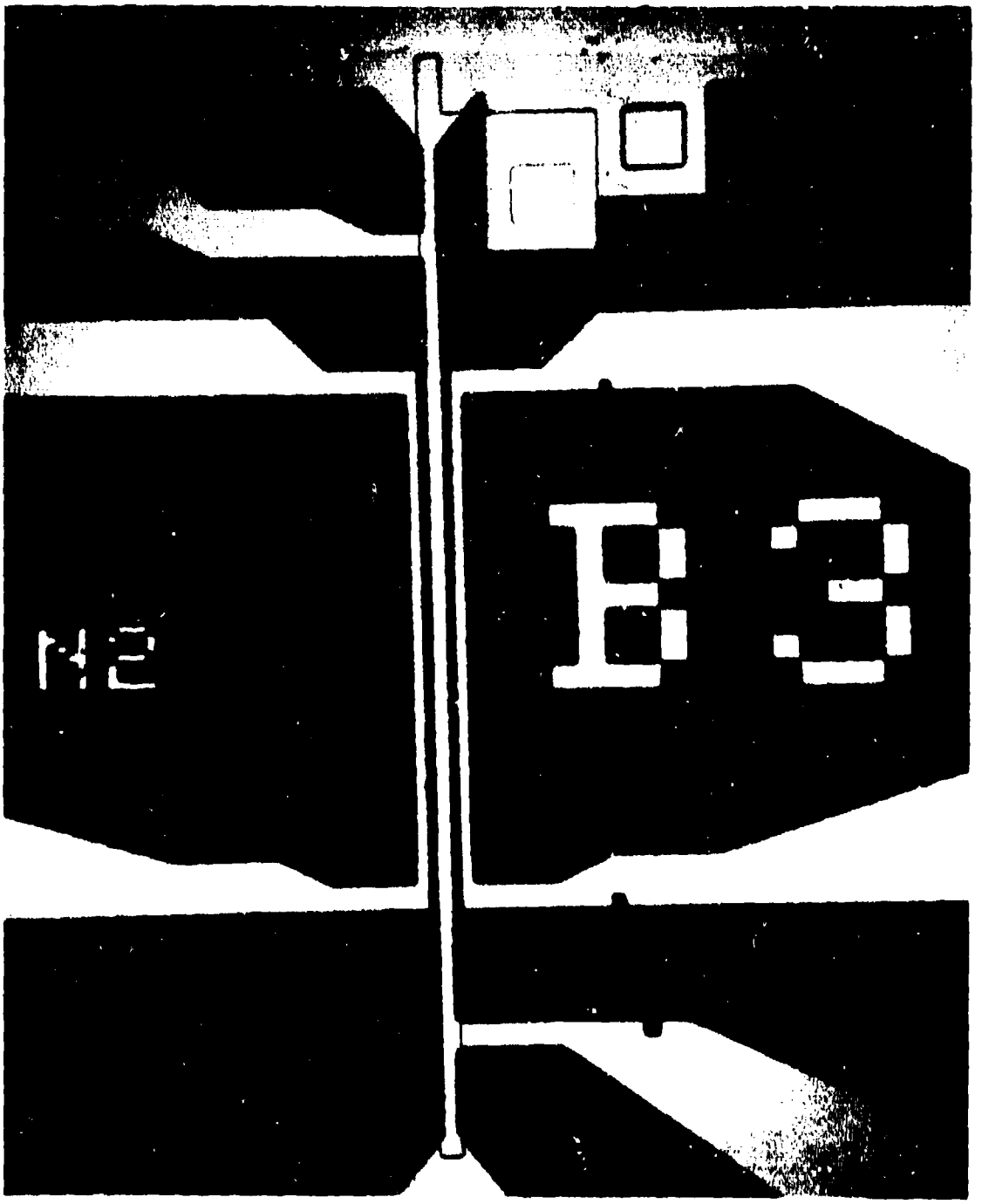


Figure 3-15. Closeup of Metal Etch Resolution Capability (0.2 mil Metal and 0.2 mil Space).

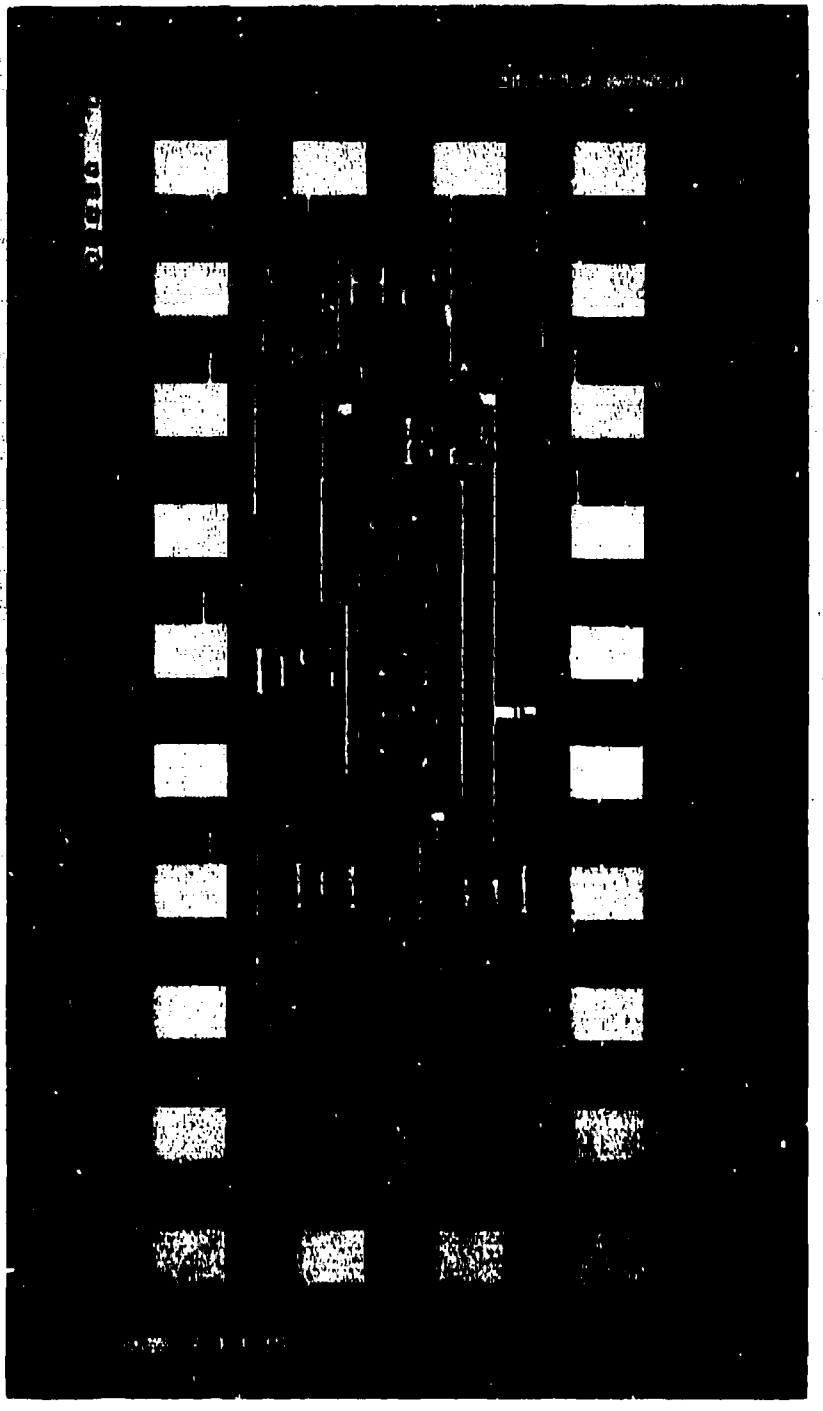


Figure 3-16. Integrated Injection Logic Test Chip Using Metallization Process Improvements.

Figure 3-17. Point Defect in Barrier Metallization After 100 Hours at 365° C.

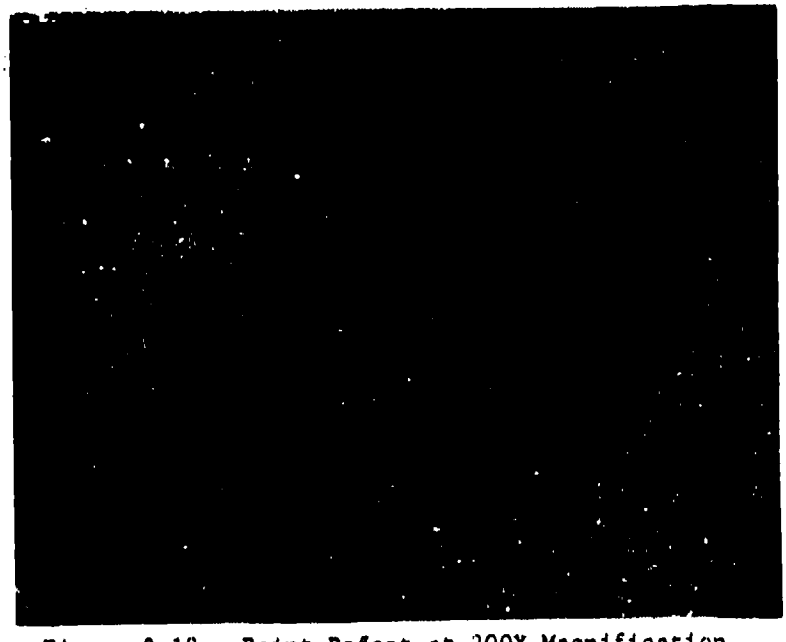


Figure 3-18. Point Defect at 200X Magnification Annealed 100 Hours at 365° C.

barrier. Silicon has diffused up through this same channel and spread out into the gold layer causing the circular pattern. Figure 3-19 is a closeup of the depression region at 2000X magnification. It appears that the gold melted and flowed down through a hole in the diffusion barrier. Figure 3-20 is a closeup of the depression area showing a small pit in the center about 2 microns in diameter. Microprobe analysis of this pit shows almost equal concentrations of tungsten and gold indicating that the barrier layer itself is exposed.

These defects in the barrier metallization system could represent a latent failure mechanism. If the barrier defect occurred in a contact opening, the resulting gold diffusion into the silicon from the contact would reduce the minority carrier lifetime and cause that gate to fail due to reduced gain and increased contact resistance. This problem can only occur if the defect is positioned in a silicon contact region. At all other locations, such a defect would be over the chip field oxide which in itself provides an excellent diffusion barrier.

To determine if barrier defects would cause any chip yield problems, one of the metallization process monitor wafers with the metal system on platinum silicide was patterned using the electromigration test cell metal mask and then annealed at 367° C for 100 hours. Figure 3-21 shows a typical ring oscillator metal pattern after the anneal. For a barrier defect to affect chip yield, the defect must occur in a contact opening where the metallization contacts the silicon (for example, the small rectangular areas under the "D1"). All the metallization shown in Figure 3-21 was formed on top of platinum silicide as contrasted with an actual working die (shown in Figure 3-16) where the majority of the metallization is on top of a field oxide. A barrier defect was found within the metallization pattern on another die site as can be seen in the large 8 by 8 mil bonding pad shown in the center of Figure 3-22. It should be noted that if this metallization was actually on a diffused wafer, the defect shown in the figure would be on top of the field oxide and would not have been exposed by this anneal. This exercise provides some indication that the defect density in the barrier metallization will enable reasonable chip yields.

Figure 3-19. Center of Point Defect at 2000X Magnification Annealed 100 Hours at 365° C.

Figure 3-20. Two Micron Pit at Center of Point Defect Annealed 100 Hours at 365° C.

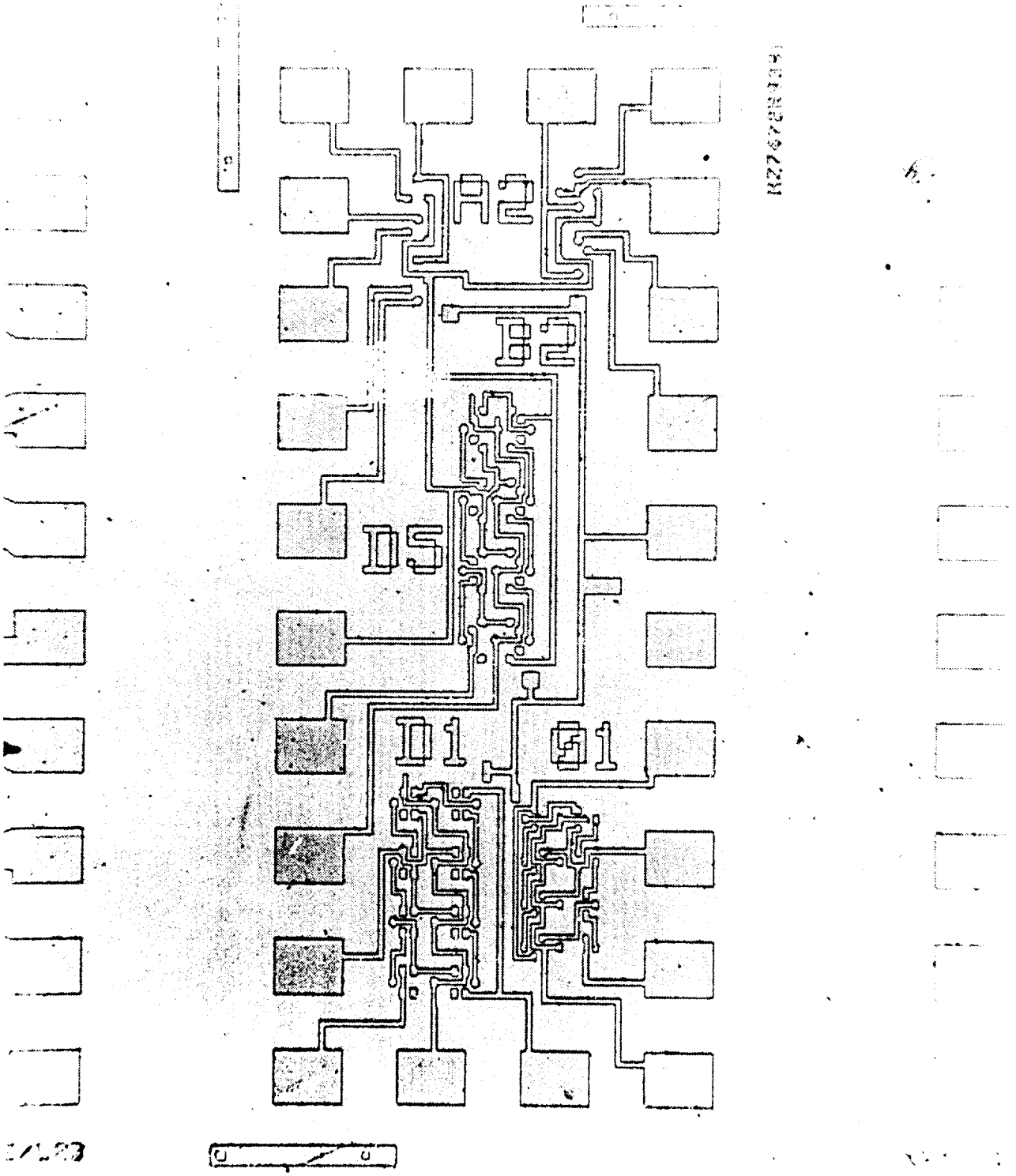


Figure 3-21. Ring Oscillator Metallization Pattern on Platinum Silicide.

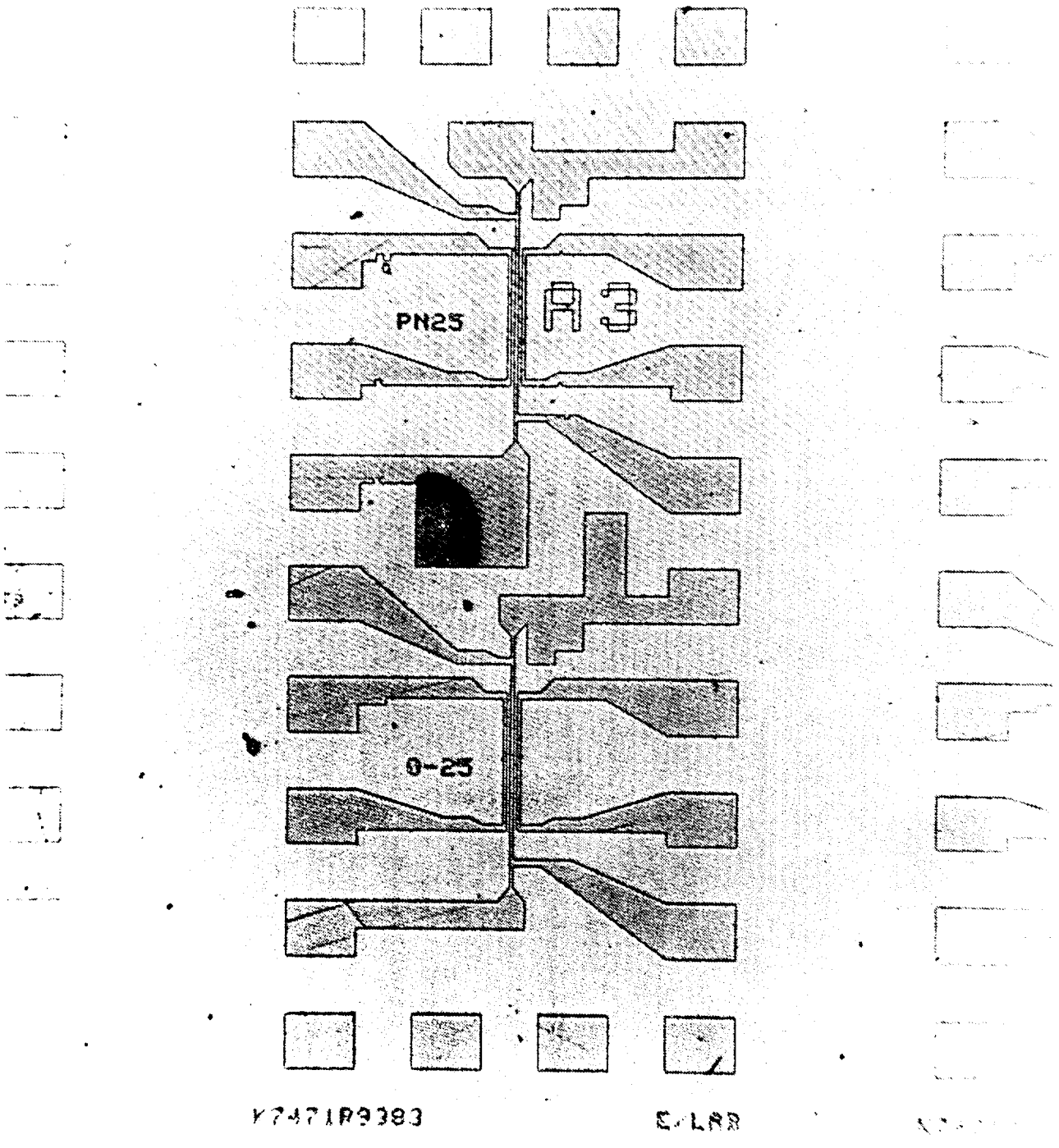


Figure 3-22. Barrier Metallization Test Pattern on Platinum Silicide Showing a Defect in the Barrier.

3.3 INVESTIGATIONS OF HILLOCKS AND VOIDS

One of the discoveries in the failure analysis of the initial life tests was the presence of hillocks and voids in the unpassivated metallization layers. The hillocks could be classified under three general categories. Single crystals were observed growing from the top and sides of the metal runs (Figure 3-23). SEM microprobe analysis of these crystals indicated that they were composed of almost pure gold within the limits of the measurements. In many cases, mounds were observed associated with the crystals (Figure 3-24) which were thought to be large crystals buried inside the gold metal layer. Finally, hillocks were observed which can best be described as bubbles in the gold layer (Figure 3-25). In some cases (Figure 3-26), all three types were observed in one sample. These hillocks and associated voids in the metallization were the cause of many of the initial life test failures. As a result, an attempt was made to understand and control the phenomenon. The gold crystal growth was thought to be related to a thermally induced migration of gold atoms. In addition, there was some concern that low level electromigration could also cause the same sort of failure mode so a search for a passivation layer or treatment was initiated.

A literature search found references to the use of hydrogen as a passivation treatment for gold (Reference 7) and the effects of hydrogen environments or incorporation on the electromigration resistance in thin metallic films (References 8 and 9). At about this same time, a silicon nitride passivation experiment on gold (Figure 3-27) resulted in crystal growth being suppressed by the plasma nitride deposition process. The nitride layer had flaked off the gold early in the annealing cycle but only a few gold crystals were observed. The key similarity is that hydrogen is a byproduct of the nitride process and the heated wafer had been exposed to this gas during the deposition.

An experiment was conducted wherein a 5000 A gold film was sputtered on top of a Ti-W diffusion barrier in an argon atmosphere with 0.5, 0.69, 1.0, and 5.0 microns of partial pressures of hydrogen. The Ti-W/Au films were patterned using wet chemistry techniques (which did undercut) and annealed for 523 hours at 360° C. Optical inspection after the anneal indicated that there were no significant crystal growths, even for the lowest hydrogen doping. SEM evaluation

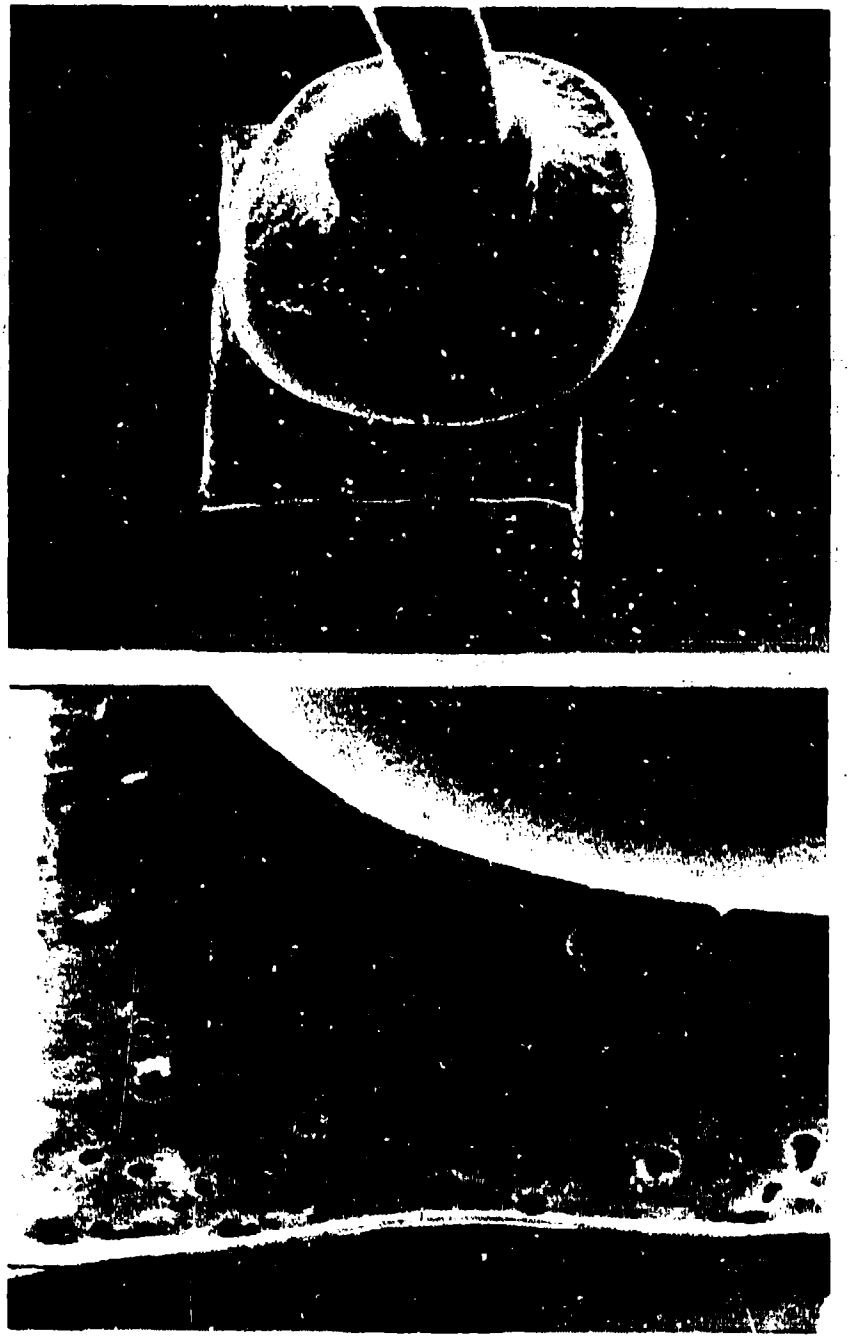


Figure 3-23. Bonding Pad of a Chip Exposed to 340° C for 1600 Hours Illustrates a Single Crystal Hillock Formation.

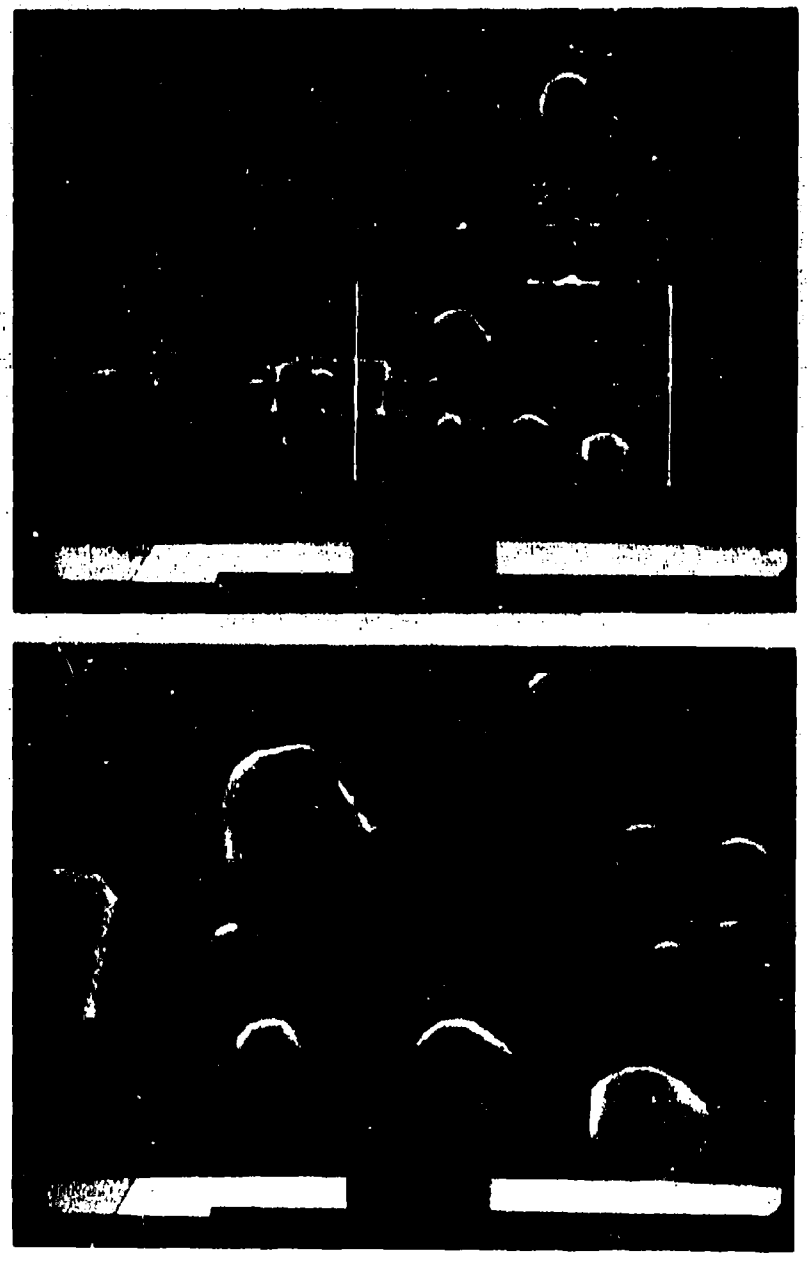


Figure 3-24. Closeup of Metal Runs After 420 Hours at 340° C, Mound-Type Hillock Formation is Illustrated.

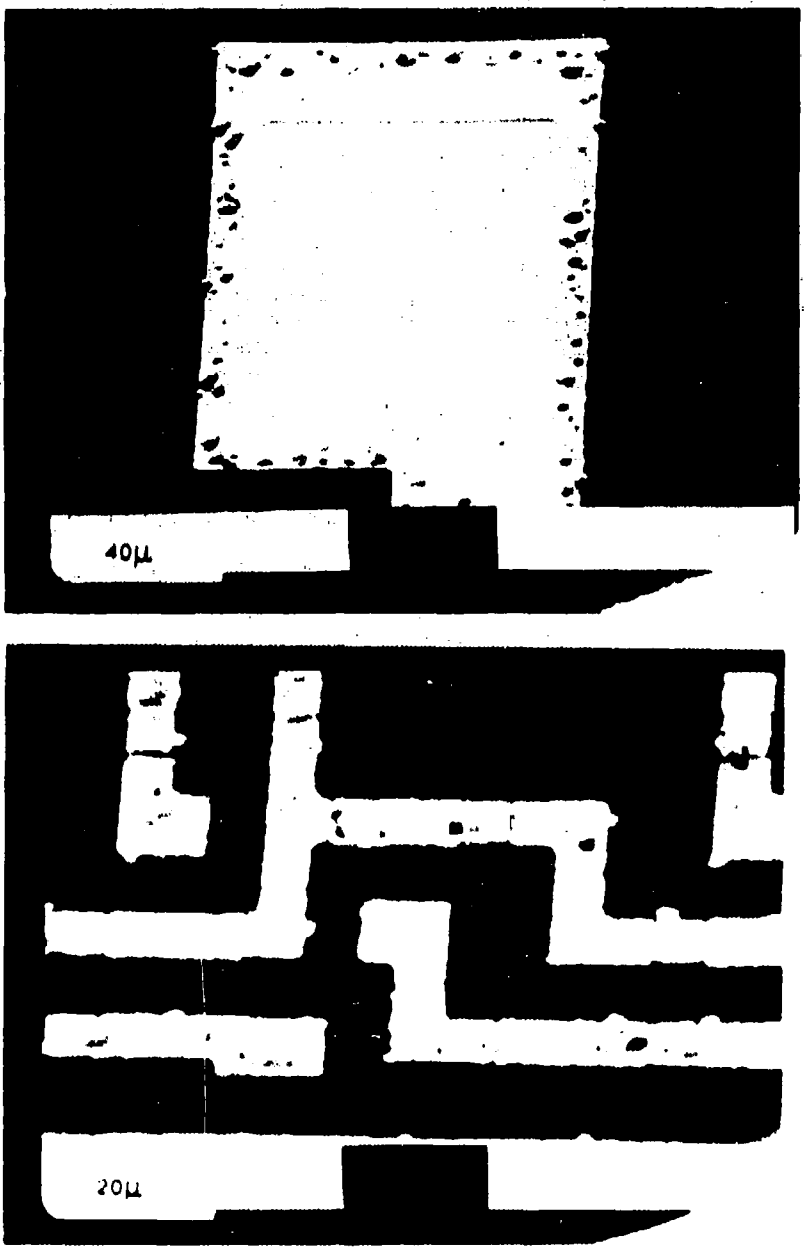


Figure 3-25. Metallization on a Chip That Failed After 210 Hours at 350° C, Bubble-Type Hillock Formation is Illustrated.

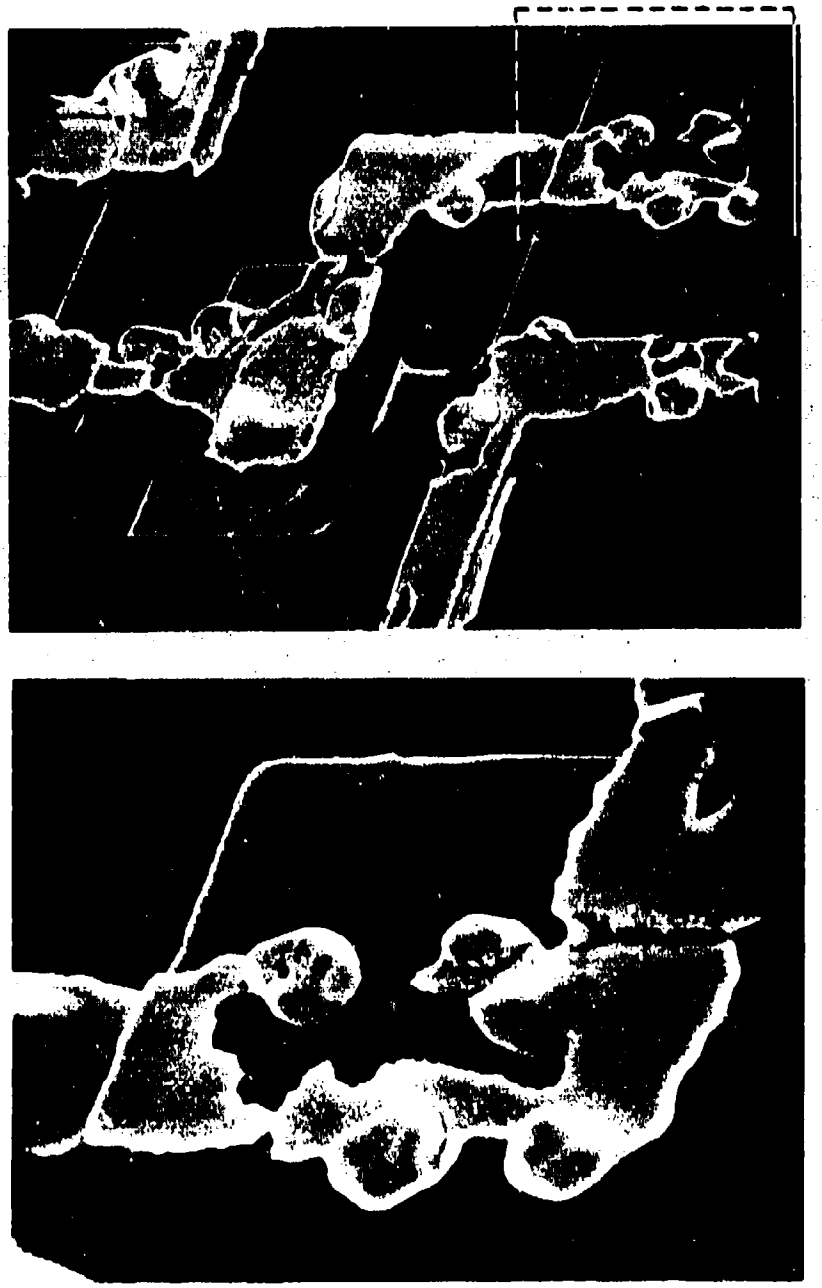


Figure 3-26. Closeup of Ring Oscillator Metallization That Failed After 320 Hours at 320° C, Single Crystal, Mound and Bubble-Type Hillock Formations are Present.

The Specimen was Initially Passivated With 7000 A of Silicon Nitride Which Flaked Off Early in the Testing.

Figure 3-27. Relatively Few Gold Crystals are Observed on the 4 x 5 mil Bonding Pad of This Test Specimen Which Was Annealed at 360° C for 509 Hours.

(Figure 3-28) confirmed the lack of crystal formation but showed a slight curling at the edges of all the metallization where it had peeled at the Si/Ti-W interface (Figure 3-29).

A longer term evaluation of hydrogen doping of the gold layer as a means of suppressing hillock growths was initiated. Unpatterned Ti-W/Au samples with and without the hydrogen doping were tested. Figure 3-30 shows a comparison of two such samples that were annealed for over 3500 hours at 360° C. Little correlation can be seen between the size or occurrence of gold crystals and the presence or absence of a hydrogen partial pressure in the deposition chamber. Clearly the short term effect that the hydrogen contributed to hillock suppression was not substantiated for long periods on unpassivated samples.

To provide a definitive test of the usefulness of hydrogen in the gold sputtering atmosphere, life test samples were deposited with and without the hydrogen. These samples will be put on life test and evaluated in a follow-on program supported by Contract N00014-83-C-2393. The interested reader is referred to the reports from that program for the evaluation results.

The cause of the gold crystal growth was hypothesized to be due to the thermal expansion mismatch between gold and the silicon wafer substrate. At some elevated temperature, the gold film would be placed in compression since gold expands more rapidly than silicon. The mobility of gold atoms is increased at elevated temperatures. The compressive force on the gold provided the driving function for crystal growth as gold atoms migrated to regions of lower potential energy.

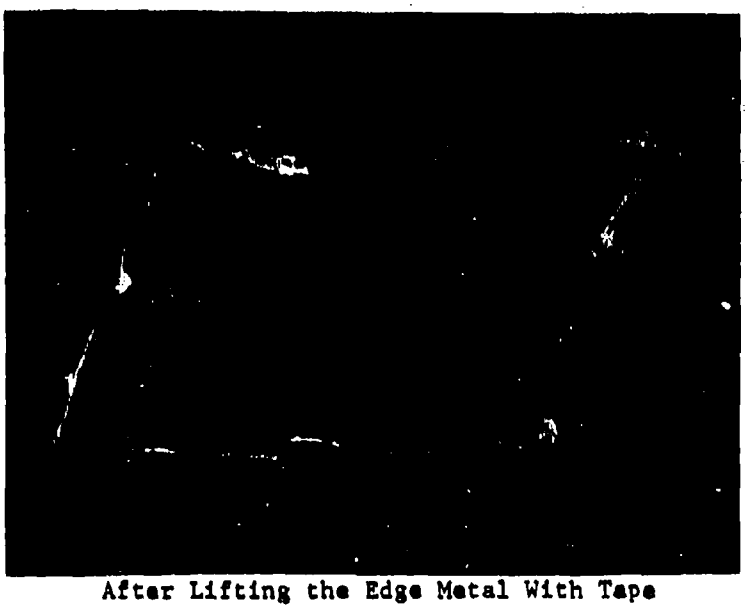
A wafer stress fixture was constructed to verify this crystal growth hypothesis by mechanically providing strain in the wafer. The fixture was designed to support a wafer around its circumference and to deflect the wafer center with a screw (40 threads per inch) to provide a strain. Experiments with dummy 3-inch wafers indicated that 40 mils was the maximum deflection that could be applied to the wafer center before the wafer broke. To calibrate the fixture, a Ti-W/Au metallized 3-inch wafer was fitted with 0.015 by 0.020 inch strain gages. Strain gages were mounted at the wafer center, and 0.25, 0.75, and 1.25 inch radially out from the center on one side of

- No Hillocks are Visible on 4 x 5 Mil Bonding Pad.
- Peeling and Curling of the Edges are Visible.

Figure 3-28. SEM Photograph of Annealed Samples (523 Hours at 360° C) With Gold Deposited in 0.69 Micron Hydrogen Partial Pressure.

- Ti-W Residue. Undercutting of 4 x 5 Mil Bonding Pad is Evident.

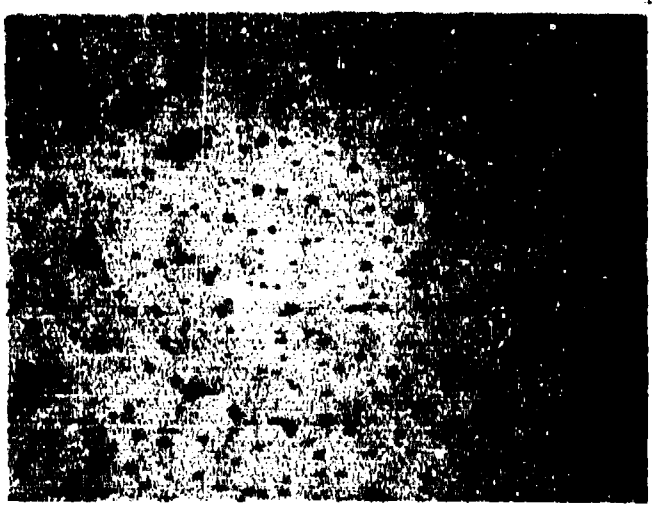
Before Lifting the Edge Metal With Tape



After Lifting the Edge Metal With Tape

Figure 3-29. SEM Photographs of Annealed Samples (523 Hours at 360° C) With Gold Deposited in 5 Micron Hydrogen Pressure.

Normal Ti-W/Au System (1000X)



Gold Film That Was Deposited in a Hydrogen Partial Pressure (1000X)

Figure 3-30. Optical Photographs Showing the Density of Gold Crystal in Ti-W/Au Samples Annealed for Greater Than 3500 Hours at 360° C.

the wafer. Strain measurements were made (Figure 3-31) with 1/4, 1/2, and 1 full turn of the screw at room temperature and in a 66° C oven (the maximum temperature limit for the strain gage). The strain profile did not change when the fixture was placed in the oven, indicating that the strain induced by the fixture did not change with temperature.

The interface strain due to the thermal expansion mismatch between Ti-W and Au was estimated to be on the order of 2500 μ inch/inch at 350° C assuming that there was zero strain at 100° C. As can be seen in Figure 3-31, the maximum strain that could be safely produced by the fixture was about one sixth of that value. As a result of this relation, an annealing experiment could not be constructed that completely cancelled the thermal stress with mechanical stress. The stress fixture was used to modulate the thermal induced stress by adding and subtracting the mechanical strain.

Two 3-inch silicon wafers with Ti-W/Au metallization were annealed at 350° C for 347 hours. One wafer had the force applied to the gold side (gold under mechanical compression) and one with the force applied to the silicon side (gold under mechanical tension). Both wafers had one full turn of the screw which would produce a strain of approximately 400 μ inch/inch at the wafer center. After annealing the wafers, the gold under the higher compressive strain showed the formation of larger (2:1) gold crystals than the wafer with the gold under "tension." Figure 3-32 shows optical photographs of similar regions of both wafers.

If a thermal expansion mismatch is the cause of the crystal growth in the gold metal layer when they are annealed at temperatures of 350° C, then an obvious solution to the problem is to deposit the metallization onto wafers that are heated to this temperature range. Presumably at 350° C, there would be no induced strains in films deposited at 350° C; while at all lower temperatures, the strain on the gold would be tensile and not conducive to crystal formation. Accordingly, Ti-W/Au films were deposited onto test wafers at room temperature, 300° and 350° C. The texture of the films was found to be progressively rougher the higher the deposition temperature. Samples of each of these wafers were annealed for 347 hours at 350° C. Microscopic examination after the anneal indicated that a typical amount of

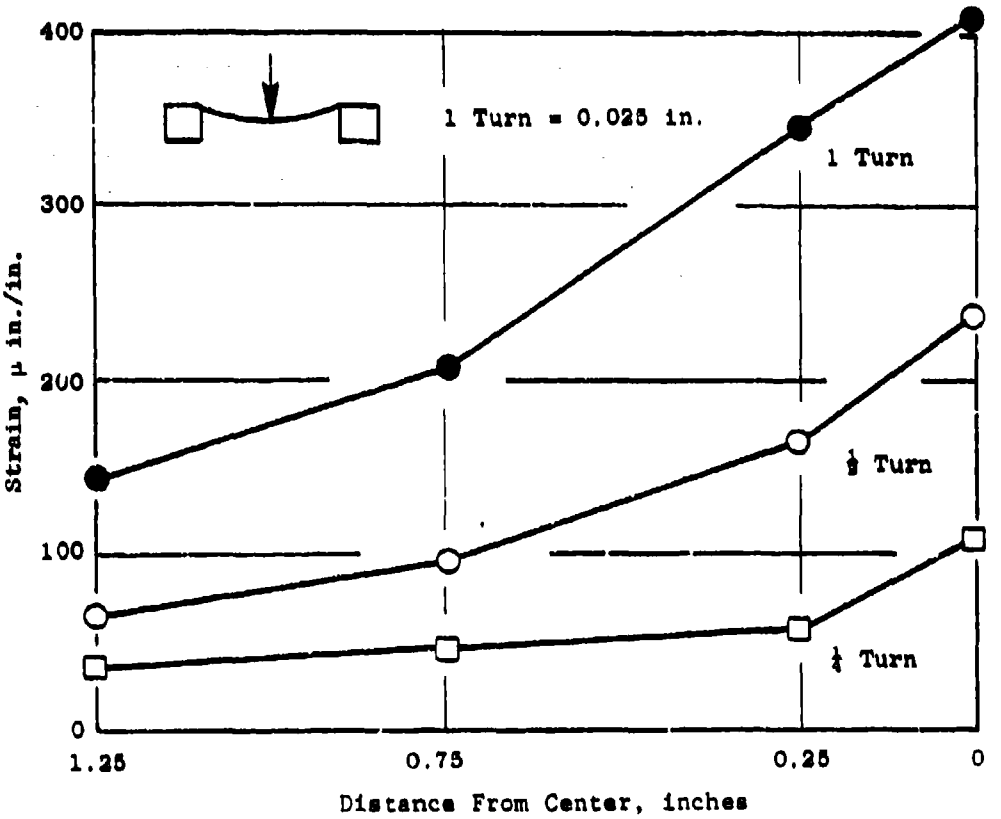


Figure 3-31. Results of Strain Gage Measurements on a Wafer Supported Around the Edge and Depressed in the Center.

Gold in Compression

Gold in Tension

- Much Larger Hillocks are Formed in the Sample Under Compression (1000X)

Figure 3-32. Comparison of Hillock Size on Annealed Samples Which Were Strained During Anneal.

gold crystals had formed on the room temperature deposited sample. The sample deposited at 300° C had few crystals and the sample deposited at 350° C was crystal-free. Also, there was no apparent change in the film texture after annealing. Figure 3-33 shows SEM photographs of the three samples after annealing The effect of the deposition temperature on the film texture is visible. Figure 3-33 (bottom) shows a crystal that formed during the anneal of the sample which was metallized at room temperature.

An interesting discovery was made while trying to suppress the growth of gold crystals through the use of a relatively thick top Ti-W layer. Samples were deposited with 5000 A of gold on top of a Ti-W diffusion barrier. One sample had an additional layer of 2000 A of Ti-W deposited on top of the gold. The gold layer and the top Ti-W layers were patterned with wet chemistry techniques and the gold etchant undercut the top Ti-W layer on that sample. The bottom Ti-W diffusion barrier was not etched since the goal was to try to mechanically constrain the gold using the Ti-W layers. Figure 3-34 shows the results of the control sample without the top Ti-W layer after annealing for 600 hours at 360° C. Gold crystals were observed growing in the surface and edges of the metal regions. The result of adding a 2000 A top Ti-W layer is shown in Figure 3-35. Gold whiskers estimated to be 5 mils in length can be seen growing from the edge of the gold layer but no hillocks or crystals are visible on top of the gold layer. This indicates that a physical constraint will prevent gold crystal formation. However, the gold film does whatever it can to relieve induced stresses (such as the whisker growth indicated).

The hillock growth resulting from life testing of unpassivated samples using wet chemistry etching techniques varied widely from sample to sample. For example, in one early life test two apparently identical samples experienced entirely different hillock growth results. One sample had gross hillock growths at the edges of the metallization runs while its twin had very little. In searching for an explanation, it was recognized that the wet etching process utilized can produce etching variations from the wafer edge to the center which might explain the apparent randomness of the hillock formation in supposedly identical die. This hypothesis was further reinforced by the fact that the life test samples were not chosen from specific sites on the wafer nor was a location catalog recorded.

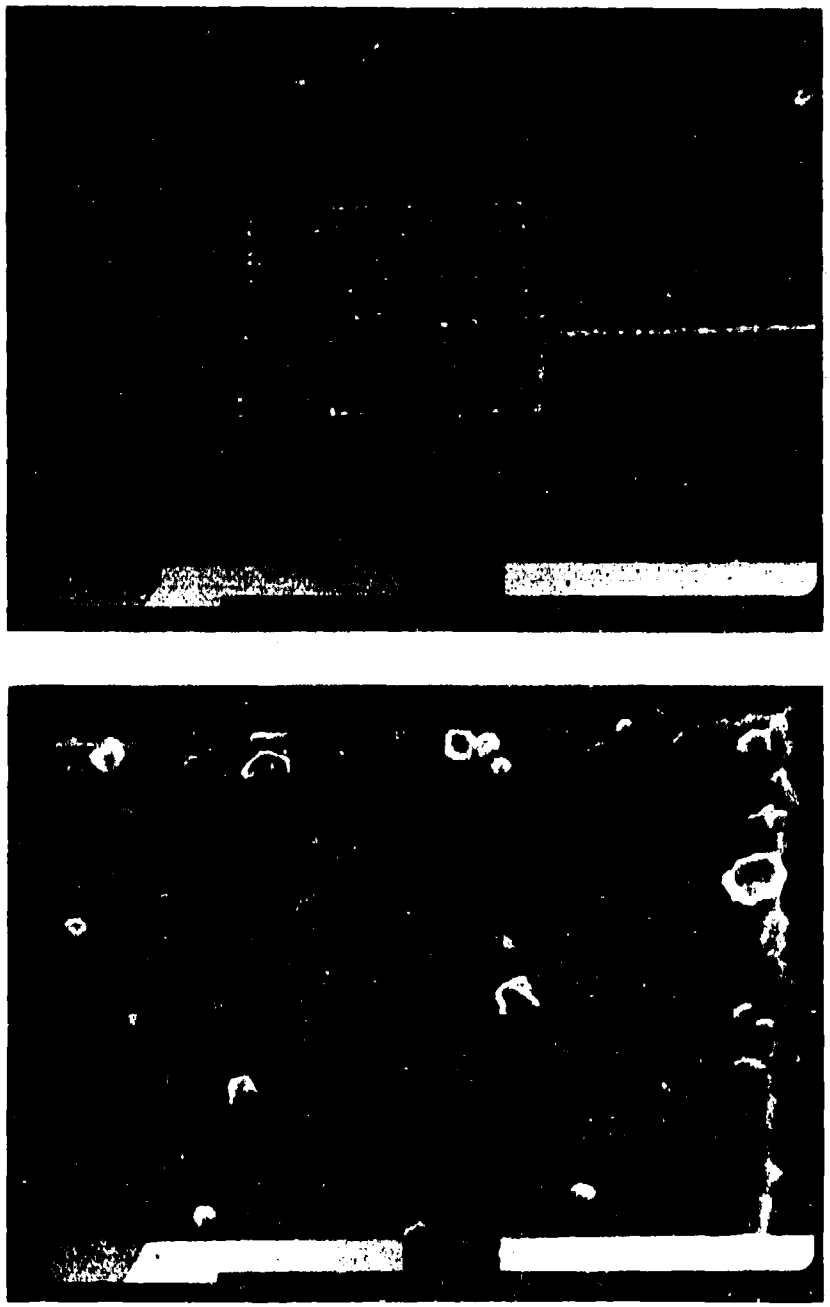
350 C Gold Deposition (5000X)

300 C Gold Deposition (5000X)

Room Temperature Gold Deposition (5000X)

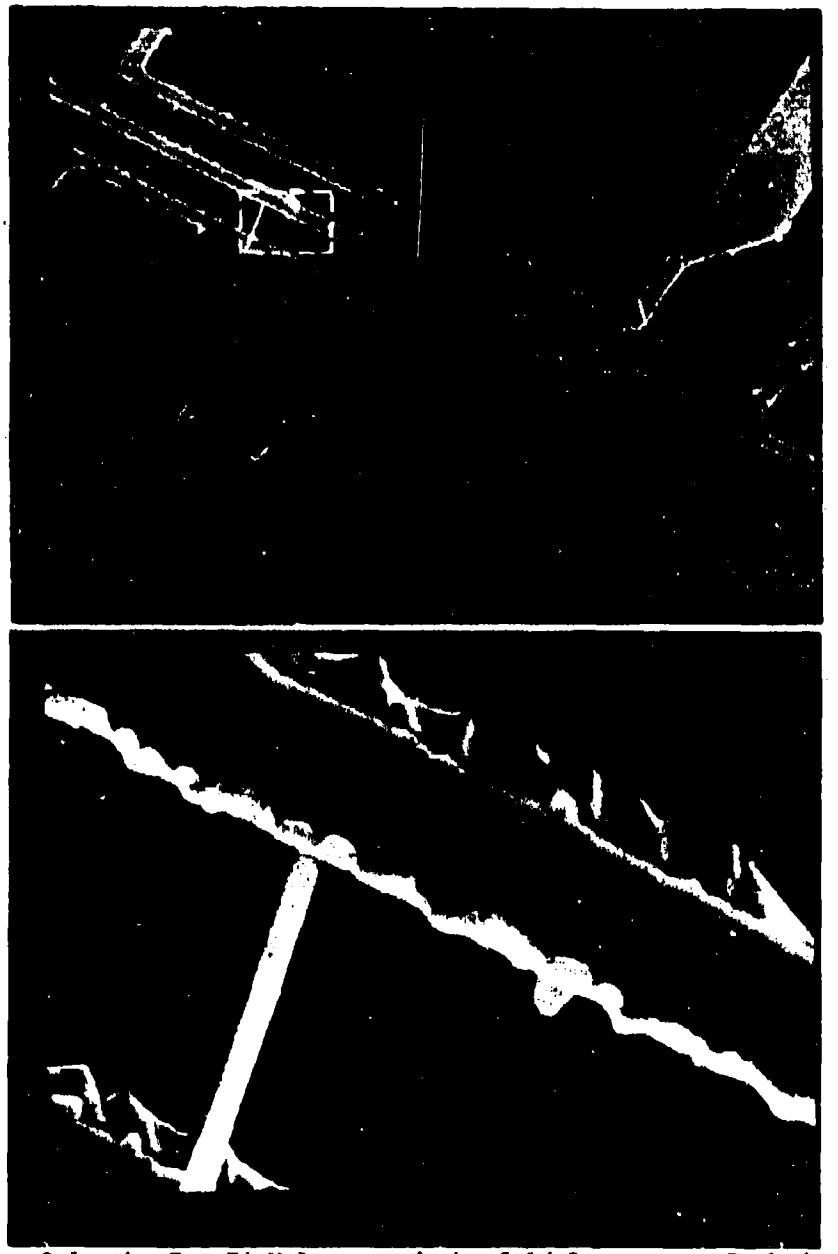
- Increasing the Temperature Increases the Roughness of the Film
- The Texture Does Not Change With Annealing
- Large Hillock Growth in Room Temperature Sample is Visible
- Very Small Nodules on Higher Temperature Samples Were Visible Before Annealing

Figure 3-33. Comparison of Film Texture.



• Note the Hillock Formation

Figure 3-34. A Control Sample with Ti-W/Au Metallization After Annealing for 600 Hours at 360° C.



- Only the Top Ti-W Layer and the Gold Layer were Etched
- Note Undercut of Top Ti-W Layer (Thin Upturned Edge) and the Formation of the Gold Whiskers from Constraining the Gold Surface

Figure 3-35. A Ti-W/Au Metallization Sample With a Top Ti-W Layer (2000 A) After Annealing for 600 Hours at 360° C.

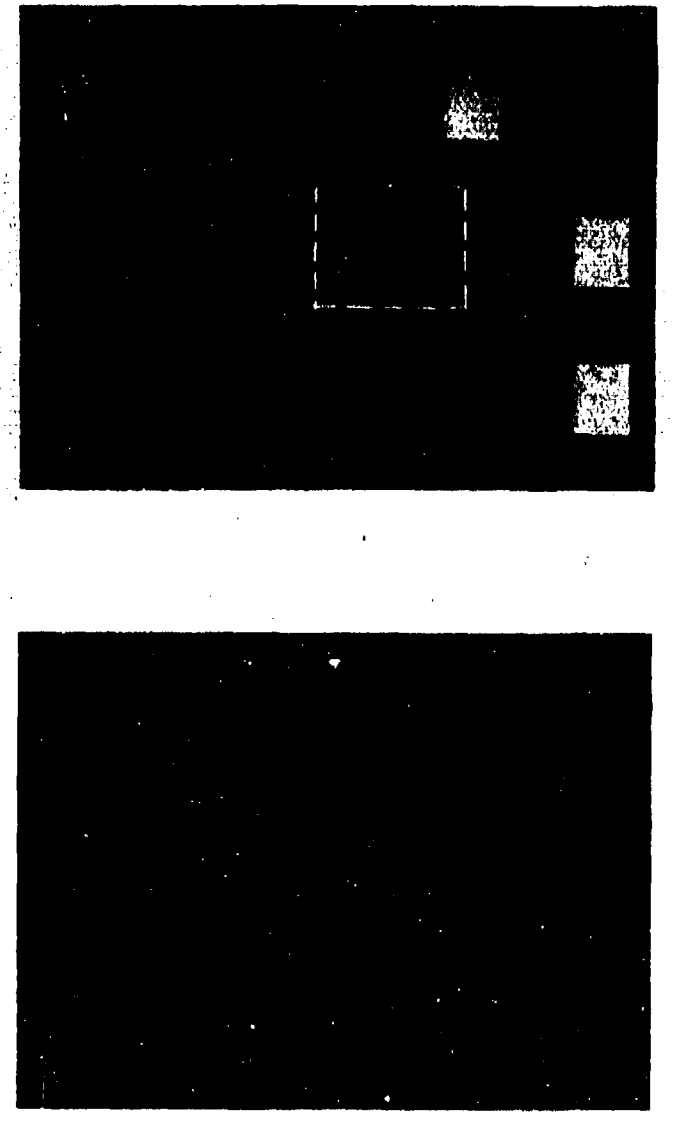
The supposedly identical die were cleaved and cross sections examined in the SEM/microprobe. It became apparent that the sample with the gross voiding and edge hillock density had experienced significant undercutting of the gold metallization layer during the Ti-W etch. The extent of the undercutting matched that of the voiding. It was also noted that the gold at the edge of the runs was reduced in thickness on the severely undercut sample. The other sample had very little undercutting or thinning. In addition, it was noted that the hillocks at the edges of metal lines appeared to be bubbles which had burst open.

Another sample, which had failed during the life test due to metal voiding at an oxide step, was subjected to a tape test in which scotch tape was used to lift the metallization where it was not well adhered. The gold lifted from certain regions of the chip, revealing areas where the Ti-W layer had been completely etched away. The undercutting of the gold on these samples had caused bubbles in the metallization and voiding which resulted in their ultimate failure.

Based on these results, it appeared that the voiding was due to undercutting of the gold metallization which randomly led to entrapment of the etchant or other contaminants. Then during subsequent high temperature life tests, the residual contaminants caused the formation of bubbles. Eventually, the bubbles burst causing voids in the gold. Examples of these failure mechanisms are shown as follows:

- Figure 3-36 shows severe undercutting of the Ti-W/Au metal system to an extent which allowed a tape test to remove some of the metal lines and bonding pads.
- Figure 3-29 illustrates where gross voiding of the metallization has resulted after annealing; in conjunction with undercutting which occurred during patterning.
- Figures 3-24, 3-25, 3-26, 3-37, 3-38, and 3-39 show examples of metallization anomalies resulting from life testing which clearly resemble bubbles or blisters.

The elimination of this failure mode was accomplished through the application of alternative methods for patterning the metallization layers. Ion milling and lift-off techniques were explored for this purpose. Both approaches have advantages and disadvantages. The techniques of ion milling and lift-off patterning are discussed later in this section under the heading entitled "Dual Level Metallization Development."



- The Tape Removed Some of the Gold Metal Lines and Bonding Pads Leaving the Ti-W Diffusion Barrier
- Note the Extent of the Undercutting Resulting from the Ti-W Etching

Figure 3-36. Optical Photographs of the Ti-W/Au Metal System from a Wafer Portion That was Tape Tested for Metal Adhesion Prior to Annealing (144 Hours at 360° C).

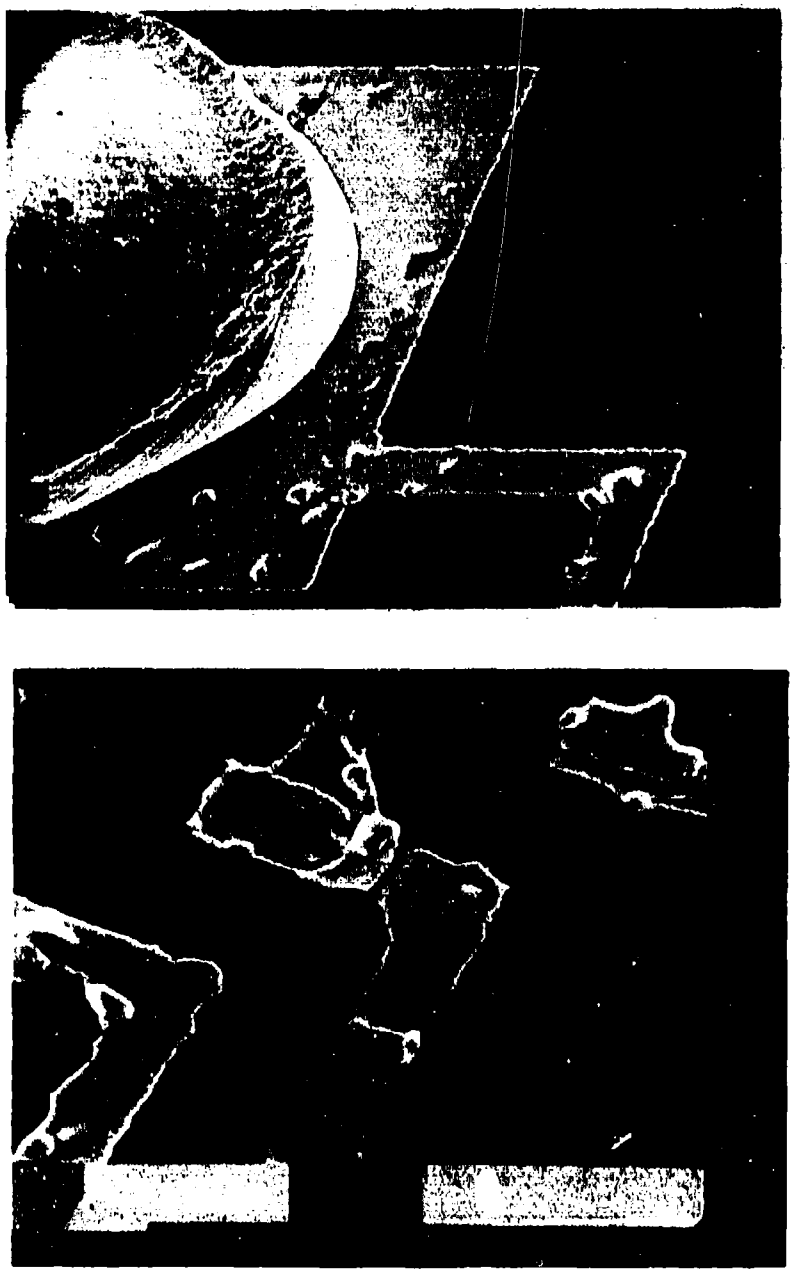


Figure 3-37. Bonding Pad and Ring Oscillator Metallization from Chips Which Failed After 320 Hours at 320° C.

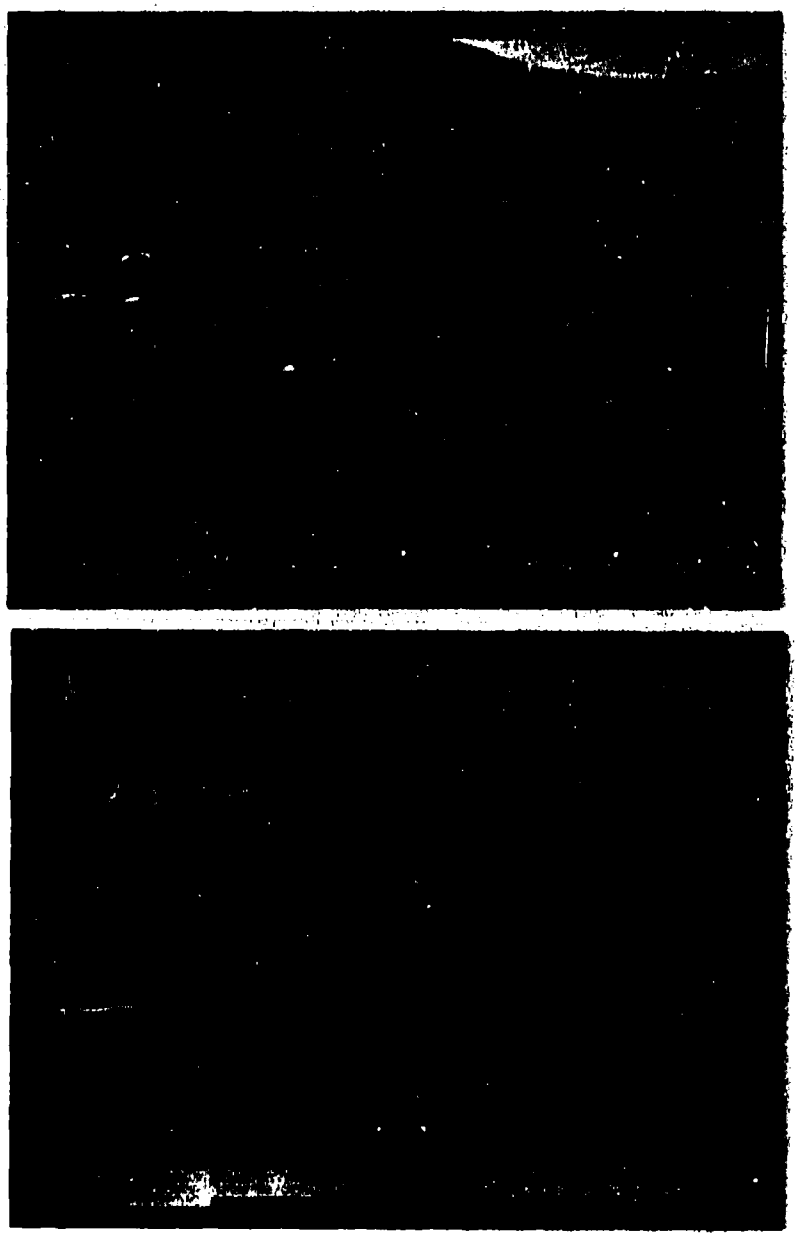


Figure 3-38. Metallization Anomalies Observed After 2200 Hours at 320 Hours at 320° C.

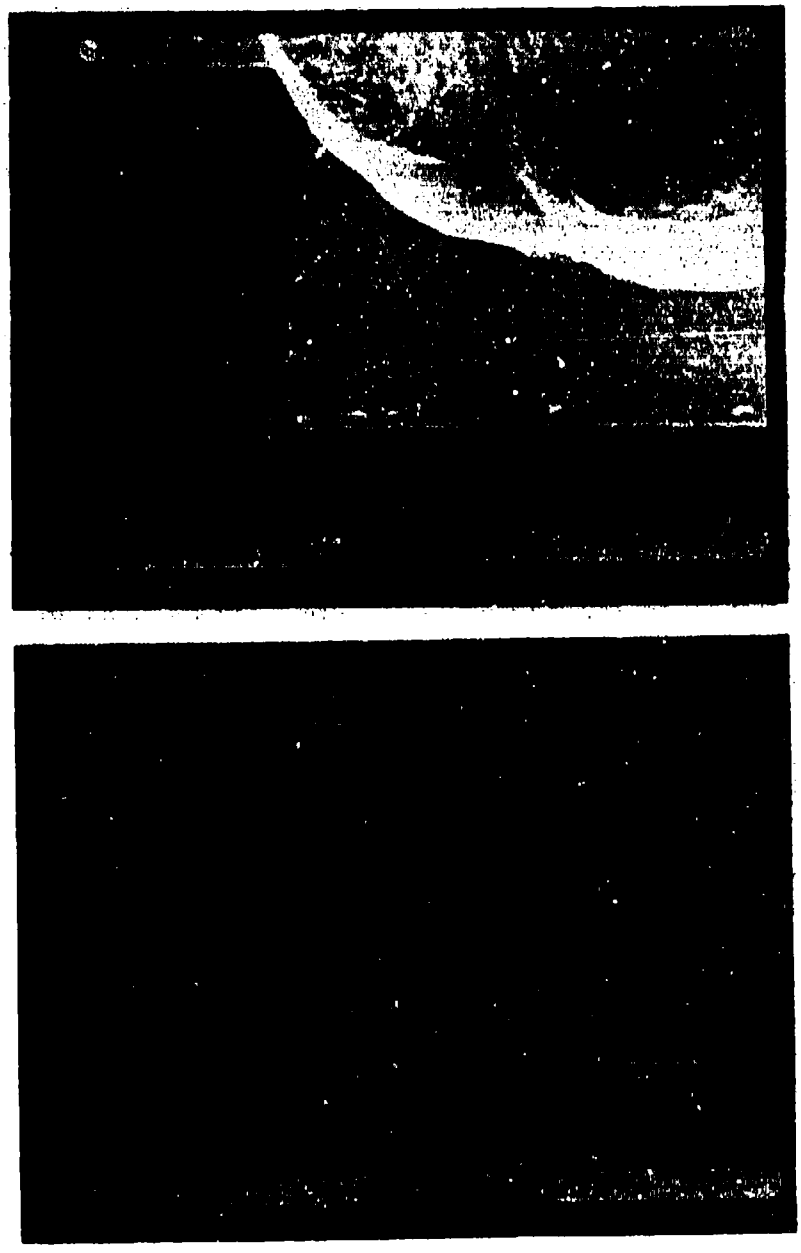


Figure 3-39. Barrier Metallization Anomalies Observed After 420 Hours at 340° C.

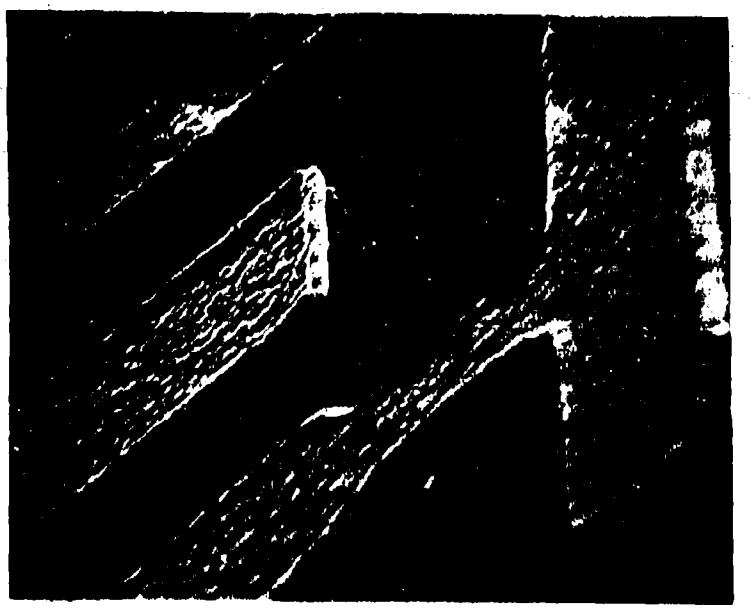
3.4 METALLIZATION ADHESION STUDIES

The purpose of the diffusion barrier in this metallization system is to prevent the diffusion mixing of the gold current carrying layer and the silicon semiconductor material. Titanium-tungsten was chosen as the initial diffusion barrier partly for its adhesive qualities to both gold and oxidized silicon wafers. The Ti-W diffusion barrier produced by sputtering from a Ti(10%)/W(90%) target was found to be ineffective for the desired task early in this program. The solution that provided an effective diffusion barrier was to reactive-sputter the Ti-W in a partial nitrogen atmosphere. This process "stuffed the grain boundaries" and transformed the Ti-W layer into a diffusion barrier that filled the needs for the desired range of times and temperatures.

The process of adding nitrogen to the Ti-W diffusion barrier affected the adhesion qualities of the material. A standard tape test easily removed large regions of the patterned metallization (Figure 3-12). The solution was to deposit a thin layer of undoped Ti-W first before "stuffing" the bulk of the diffusion barrier. This procedure provided the adhesion qualities of the "as sputtered" Ti-W on the wafer surface and solved the initial adhesion problem. Tape tests on the resulting metallization did not remove any of the metal from the wafer.

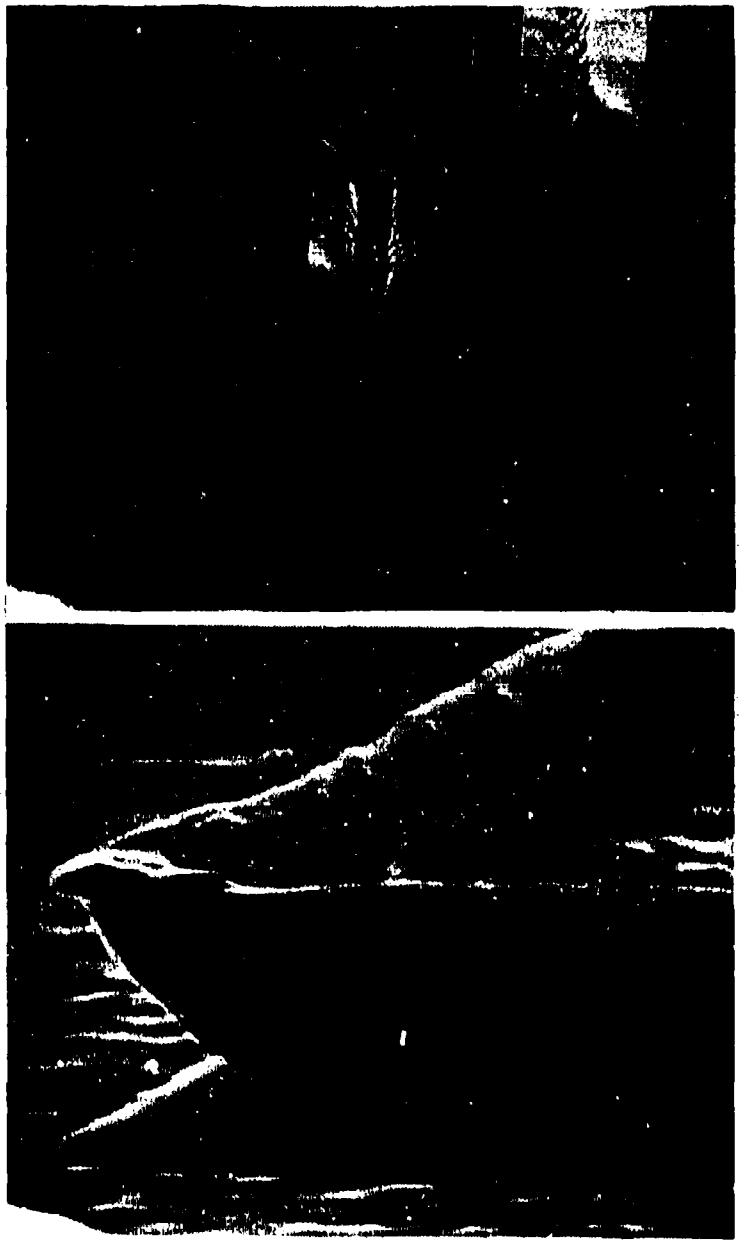
The next hint that an adhesion problem still existed was seen in some evaluation experiments conducted at 350° C. Figures 3-40 and 3-41 show SEM evaluations of pieces from the same sample after annealing for 92 hours and 192 hours at 350° C. Although the crystal growth problem being investigated by the experiment appeared to be solved, a progressive delamination of the gold layer from the Ti-W diffusion barrier can be seen. The delamination was not due to the ion milling used to pattern the metallization since, as can be seen in Figure 3-42, lift-off patterned metal samples also showed the same symptoms. In all cases, the gold lifted leaving the Ti-W barrier stuck to the wafer.

Attempts were made to artificially improve the bonding between the Ti-W and gold layers by forcing a smearing of the interface. The entire metallization system was deposited without venting the sputtering system. The approach



- The Loss of Adhesion is Between the Ti-W Diffusion Barrier and Top Gold Layer
- Minimum Line Width is 7.5 Microns.

Figure 3-40. SEM Photograph of the High Temperature Gold Metallization After Annealing for 95 Hours at 350° C.



- The Metal Separation is More Pronounced Than After 95 Hours Indicating That the Process is Not Self Limiting

Figure 3-41. SEM Photograph of the High Temperature Gold Metallization After Annealing for 192 Hours at 350° C.

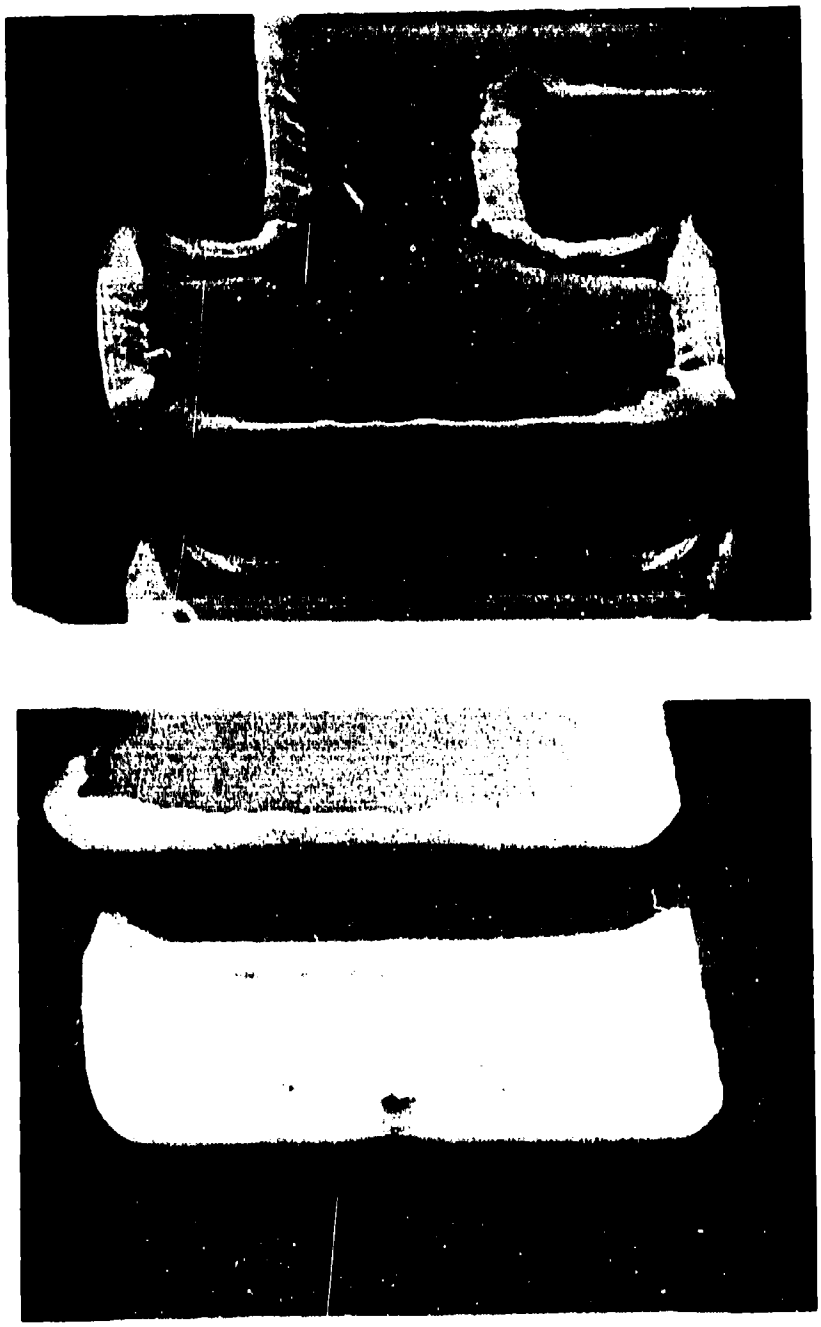
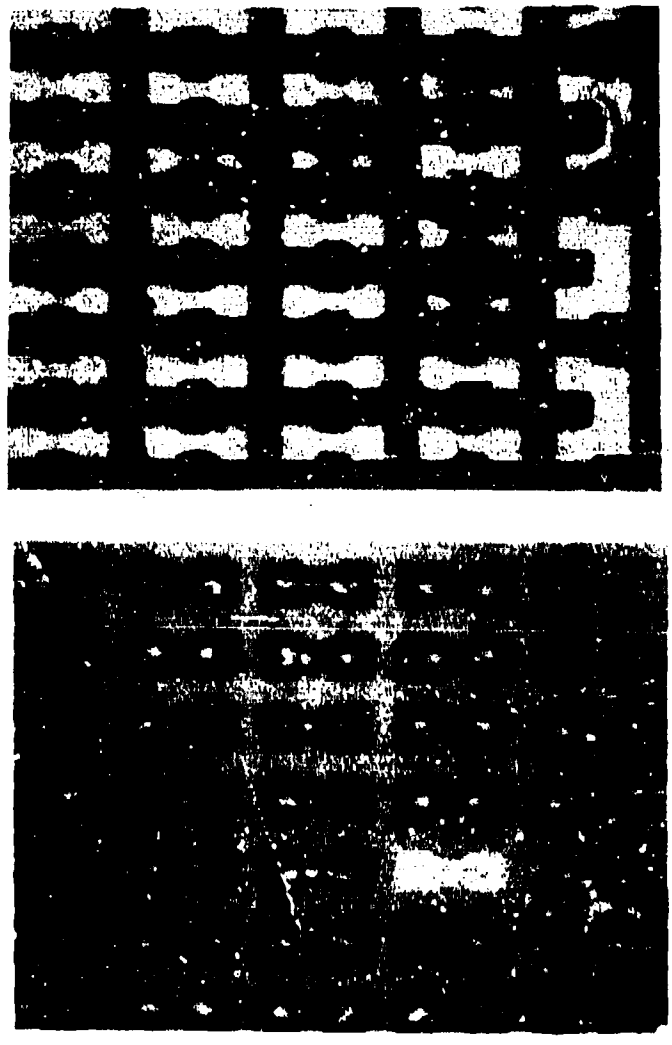


Figure 3-42. SEM Photographs of a Portion of a Lift-off Patterned Metallization After Annealing for 270 Hours at 350° C and Also Shows Delamination.

taken was to split the power between the Ti-W and gold targets after the diffusion barrier had been deposited. As the power fraction was gradually shifted from Ti-W to gold, the fraction of gold deposited increased from zero to 100% over about a 1000 A thickness. This approach was not completely successful as can be seen in Figures 3-43 and 3-44. However, as shown in Figure 3-44, the hydrogen in the gold layer apparently was successful in suppressing the gold crystal growth.

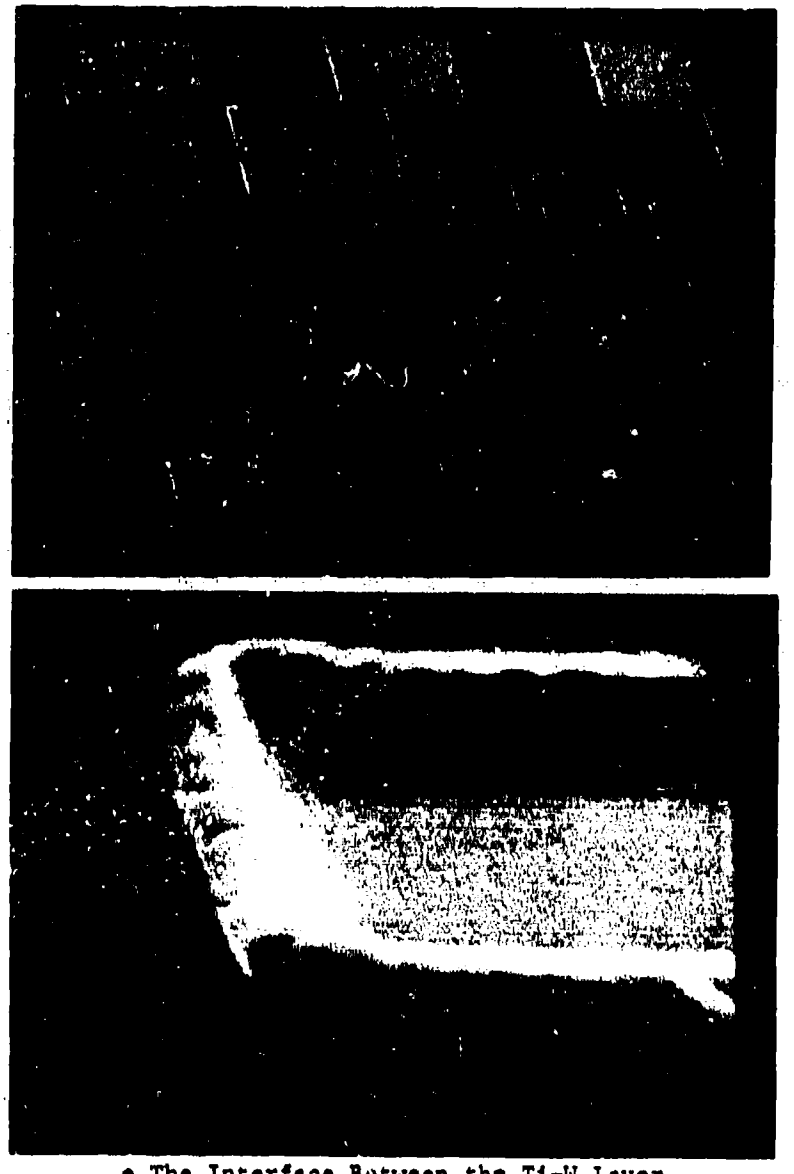
Since tape tests removed almost none of the metallization immediately after it was pattterned, the thought was that the Ti-W/Au "interface smearing" and a silicon nitride passivation layer would mechanically constrain the metal and improve the device reliability. The attempts that were made at implementing this approach produced mixed results. After wafers were metallized and patterned, sample sites were probed to provide an indication of the wafer yield and device quality. The silicon nitride layer was then deposited. After the bonding pad windows were etched on a few wafers, it was found that the probe marks on the pads had caused a localized delamination (Figure 3-45). On some dummy wafers, SEM evaluation showed where metallization lines were lifting with the nitride (Figure 3-46). Other wafers appeared normal (that is, no delaminations or metal lifting) until sample chips were packaged. On these wafers, the wire bonding operation failed when the ball bonds lifted the gold layer off the Ti-W diffusion barrier. Figure 3-47 shows one of these chips where the first three ball bonds were successful and the next two attempts failed. The chips from a different wafer were all successfully packaged and put on life test. However, the devices failed the life test when the metal runs broke as they crossed an oxide step (Figure 3-48).

A portion of an unpatterned sample deposited at the same time as the life test sample was analyzed using Secondary Ion Mass Sepctrometry (SIMS). Material is sputtered from the sample and the charge to mass ratio analyzed to determine the types of material that were present. The purpose of this exercise was to determine if contaminants were present at the metal interfaces which could account for the loss of adhesion. The results of the analysis on the "as sputtered" film indicated that the metal interfaces were clean and abrupt. No contaminants were found piled up at the interface between the gold and the Ti-W diffusion barrier.



- Ti-W/Au Interface was Smeared During Deposition of the Sample Shown in Top Photo
- An Abrupt Interface was Formed in the Sample Shown in the Bottom Photo
- Note the Darker Lines Indicate a Lifting of Metallization
- A Portion of the Lifted Gold Has Fallen Off the Ti-W in Bottom Photo

Figure 3-43. Optical Photographs of Similar Portions of Metallization Samples After Annealing for 659 Hours at 360° C.

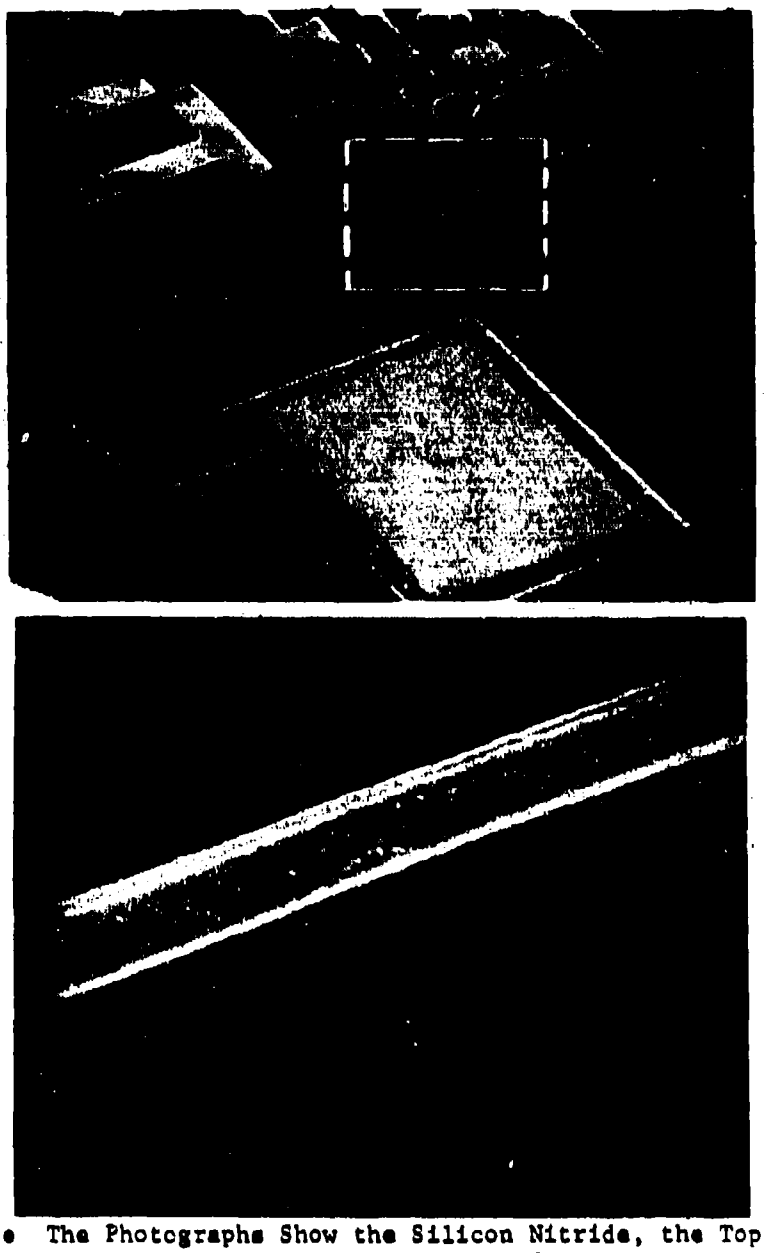


- The Interface Between the Ti-W Layer and the Gold Has Been Smeared Out Over About 1000 A Using a Power Splitting Sputtering Technique.
- The Layer Peeling Previously Observed is Still Present.

Figure 3-44. SEM Photographs of the Ti-W/Au Metal System With Hydrogen Doped Gold After Annealing for 687 Hours at 360° C.

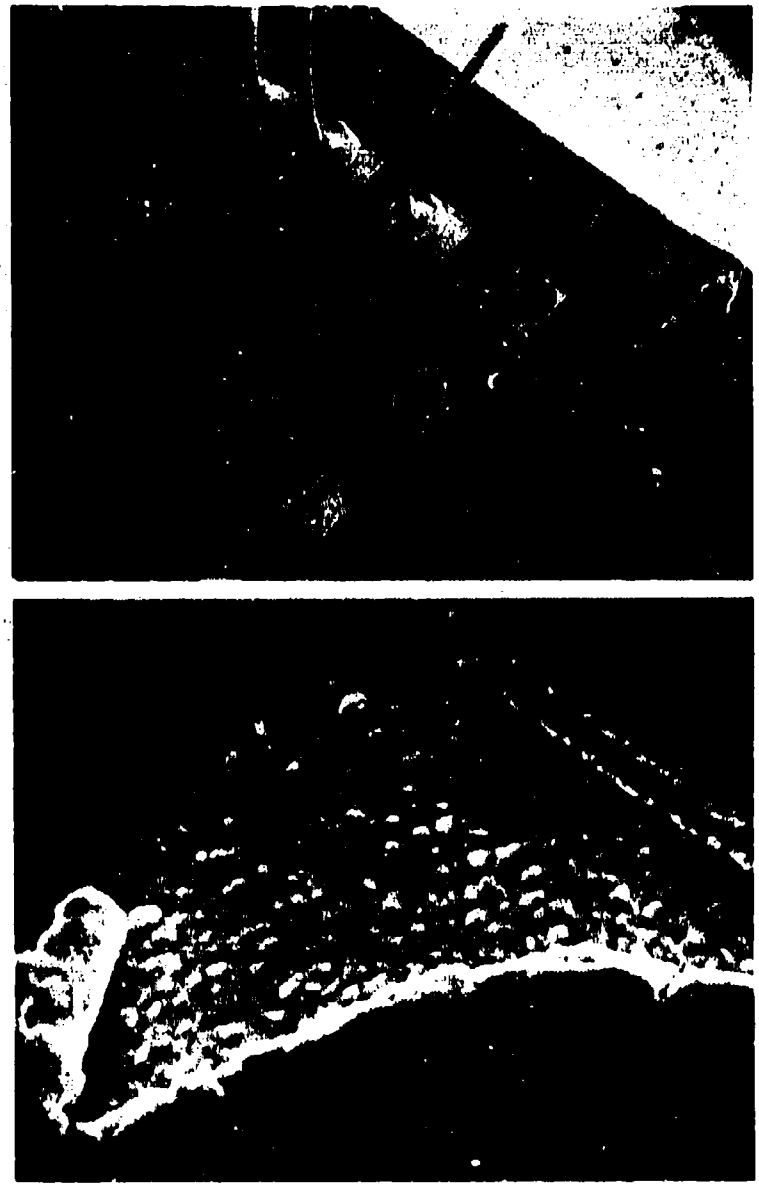
• A Close-up of a Bonding Pad Shows Where a Probe Mark Has Created a Damage Center Around Which the Metallization Has Lifted.

Figure 3-45. Optical Photographs of a Ring Oscillator Circuit on a Wafer That Was Probed for Chip Yield Prior to Silicon Nitride Deposition.



- The Photographs Show the Silicon Nitride, the Top Ti-W Layer, and the Gold Layer Lifting From the Bottom Ti-W Diffusion Barrier. 4 x 5 Mil Bonding Pad and 7.5 Micron Interconnect Lines are Shown.

Figure 3-46. SEM Photographs of a Portion of the Metallization From a Wafer Which Optically Had Shown Some Lifting After the Bonding Pad Windows Had Been Etched.



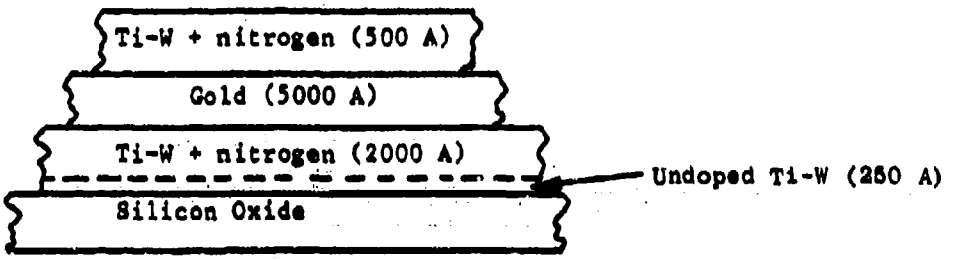
- The Bottom Photograph Shows a Close-up of the Corner Bonding Pad.
- The Surface Texture of the High Temperature Deposited Gold Can Be Seen.

Figure 3-47. SEM Photographs of a Chip From a Wafer That Could Not Be Packaged Because of the Inadequate Metal Adhesion.

- Cause of Failure is Broken Metallization Runs Caused by Metal Lifting.
- The Nitride Passivation Was Removed From This Sample Before the Photographs Were Taken.

Figure 3-48. SEM Closeup Photographs of Failed Metallization Runs Which Resulted During Life Testing.

The most interesting results were discovered during adhesion tests run on "as sputtered" samples. The testing was performed with a stud glued to the metallized wafer surface (with epoxy) and the back of the wafer glued to a mechanical support. The system was then pulled apart. The metal system that was evaluated is shown schematically below:

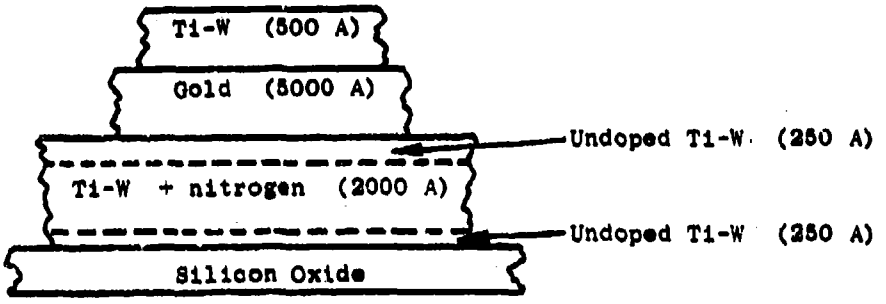


The top Ti-W layer was included to promote adhesion between the metal system and the chip passivation material. Various top layers were chemically etched from the metallization so that adhesion testing (pull tests) could be performed on all the interfaces. The first adhesion test was performed between the bottom Ti-W layer and the wafer oxide (the top Ti-W layer and the gold layer had been chemically removed). At a force equivalent to 9000 psi, the epoxy broke. The Ti-W layer remained on the wafer.

The second test was performed on a wafer with just the top Ti-W layer etched off. The stud was glued onto the gold layer. In this case a force equivalent to 900 psi was sufficient to pull the stud from the wafer. The gold layer was removed with the stud while the Ti-W remained on the wafer.

The poor adhesion in the "as sputtered" metallization films immediately explained many early failures that had been disguised with different symptoms. For example, the gold curling problems after annealing at 360° C (Figure 3-41), the bonding failures in packaging samples (Figure 3-47), and life test failure (Figure 3-48) could now be understood. The traditional adhesion test using scotch tape had not detected the marginal adhesion. If scotch tape is stuck onto the metallized wafer surface and peeled off, it exerts a force equivalent to about 1000 psi. In fact, the gold could be peeled from the Ti-W layer in the samples where the 900 psi adhesion was measured. Processing variables and wafer surface conditions could explain why tape tests had not detected this problem earlier.

As soon as the marginal adhesion was recognized in the "as sputtered" films, an obvious solution was investigated and implemented. The general belief from experience and discussions with others in the industry is that gold adheres well to Ti-W. This refers to the undoped (no nitrogen stuffing) variety not the Ti-W diffusion barrier material that this program had developed. New samples were deposited on blank oxidized wafers with the same metal system as before except that a layer of undoped Ti-W was deposited on top of the nitrogen doped Ti-W layer. This metal system appears as follows:



Samples of this metal system were subjected to adhesion testing with various top layers removed. The results were the same for all cases. Not a single film failure was observed. Equivalent forces up to 8000 psi were measured pulling on all interfaces before the epoxy broke. The results of life tests of circuits with this metal system can be found in the reports for the follow-on program supported by Contract N00014-83-C-2393.

3.5 BARRIER METALLIZATION DEPOSITION SEQUENCE

The following processing steps are used to deposit the PtSi/Ti-W/Ti-W-N/-Ti-W/Au improved barrier metal system and pattern it into a usefull interconnect pattern for high temperature integrated circuits. The process assumes that incoming diffused wafers have had the contact windows opened down to silicon and and the photoresist stripped off.

The first step is to clean the wafers to remove any residual films remaining from the plasma photoresist stripping. The first cleaning step is accomplished in a concentrated sulfuric acid (18 molar)/hydrogen peroxide (30%) (2000/1000 cc) solution for 20 minutes, and a 10-minute rinse in deionized water.

This is followed by a 15-minute cleaning step in a water, ammonium hydroxide (14.5 molar), hydrogen peroxide (30%) solution (1100/500/500 cc) and a 10-minute rinse in deionized water. The wafers are then run through an automated rinse-dry cycle.

The wafers are then placed in the sputtering system for platinum deposition. A plasma etch at 500 Watts in 10 microns of argon is used to remove a thin layer of silicon especially from the p-doped base contact regions to improve ohmic contact. If the wafers have had an ion implant for base contact, the reverse sputter is limited to 1-minute duration but if the wafers have not had an implant, a sputtering time of 4 to 5 minutes has been found necessary for good ohmic contacts. 500 A of platinum is then deposited at 200 Watts.

Platinum silicide is formed in the contact opening by sintering for 15 minutes in nitrogen at 500° C. This reacts all the platinum in the contact regions. The unreacted platinum on the circuit's field oxide is removed by boiling the wafers in aqua regia for 15 minutes followed by a rinse in deionized water.

The formation of PtSi is important for the creation of good ohmic contacts. Conversely, the absence of platinum silicide in the device contact regions after the PtSi formation step indicates that ohmic contacts may not have been created. If a thin oxide layer remains in the contact region prior to the platinum deposition, then the sinter cycle will not form PtSi. The unreacted platinum will be removed with the aqua regia. If this occurs, the transistor characteristics may appear as shown in the top portions of Figures 3-49 and 3-50. The photographs shown in Figure 3-49 were taken from a curve tracer display on the same device with about a 2-minute time interval. The photographs in Figure 3-50 were taken on a device from a different wafer. The bottom photograph in each of these figures was taken after a thin oxide resistive layer in the contact regions had been broken down.

The presence of PtSi in the device contact regions can be confirmed by using the SEM microprobe (KEVEX). The X-rays emitted by the sample due to the scanning electron beam can be analyzed for the characteristic energies of platinum. The signal may be quite low due to the relatively small amounts

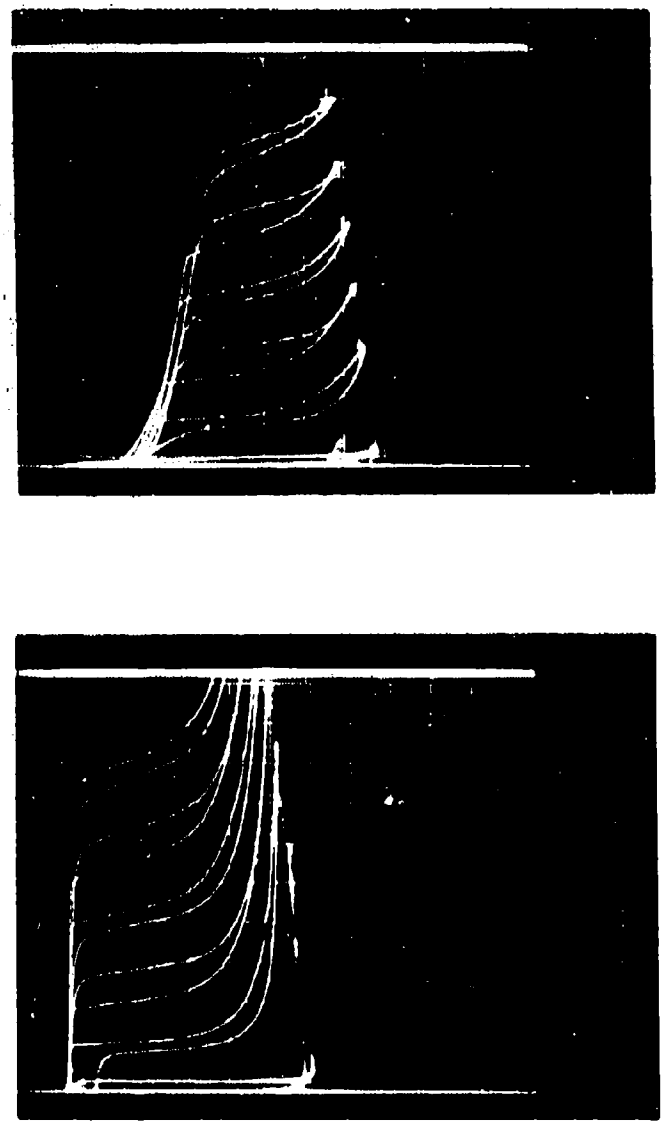
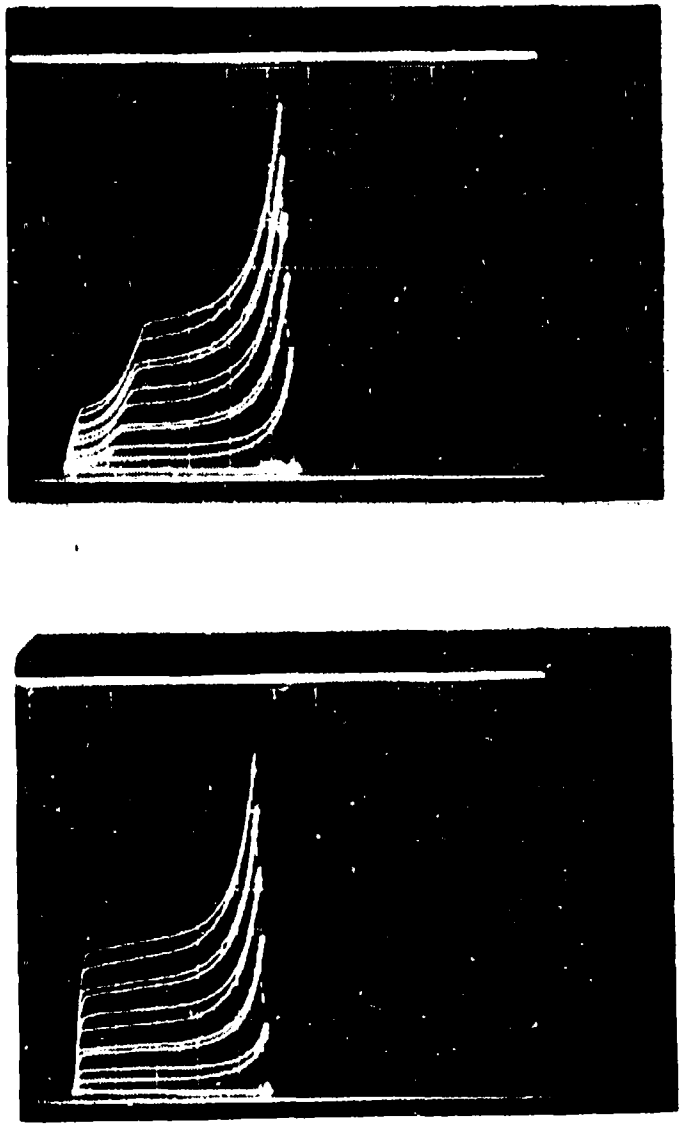


Figure 3-49. Transistor Characteristics Observed on a Wafer Before and After the Oxide Layer Was Broken Down in the Device Contacts.



- Pin Holes Through the Thin Oxide Layer Could Account for the Slight Initial Gain.

Figure 3-50. Transistor Characteristics Observed on Another Wafer Before and After the Oxide Layer Was Broken Down in the Contacts.

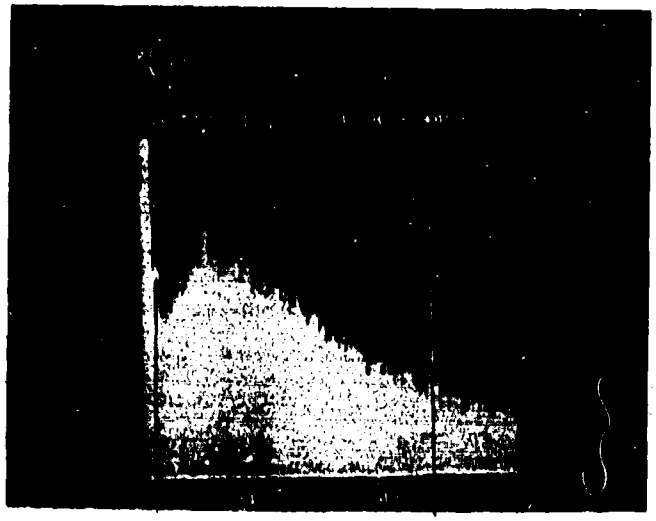
of platinum present in the emitting volume. For example, if a total of 500 A of platinum was deposited on the wafer prior to PtSi formation and stripping; at 15 keV, the electron beam will penetrate about 3 microns into the silicon sample generating X-rays from an ellipsoidal shaped volume. If the X-ray absorption is ignored and some first order assumptions relative to the sensed volume are made, then the amount of platinum in the X-ray emitting volume is (at best) less than 1/60 of the total material. The observed signals sometimes approach the minimum resolution of the microprobe system.

Figure 3-51 shows the X-ray energy histogram from the microprobe analysis on a wafer after PtSi was formed and the excess platinum etched off. The top photograph shows a probe of a device contact that contained about the minimum detectable amount of platinum. The bottom photograph shows the microprobe results on the oxide region of the wafer adjacent to the contact. The platinum emission lines are shown in the top photograph at 2.04 keV (M-alpha) which is the strongest cluster of platinum lines and at 9.44 keV (L-alpha). The left side of the display shows part of the base of the silicon line centered at 1.74 keV and a ghost silicon line can be seen at 3.48 keV.

After verifying that PtSi has been formed, the metallization can be deposited. If the metallization system is to be patterned with a lift-off technique, the lift-off photoresist is deposited and patterned before the metal system is deposited. About 1.5 microns of positive photoresist is deposited on the wafers and the surface hardened with a 7-minute chlorobenzene soak. After baking, the resist is exposed (with a dark field mask) and developed. The hardened surface of the resist forms an overhang since it does not dissolve as readily in the developer as the bottom layer of photoresist. This overhang provides a negative sidewall angle which will result in thin metallization coverage on the sidewalls when the metal is deposited. This feature is necessary for lift-off patterning since the unwanted metallization is physically torn from the desired metallization during the lift-off operation and the thin sidewall metal sections facilitate and control the tearing operation.

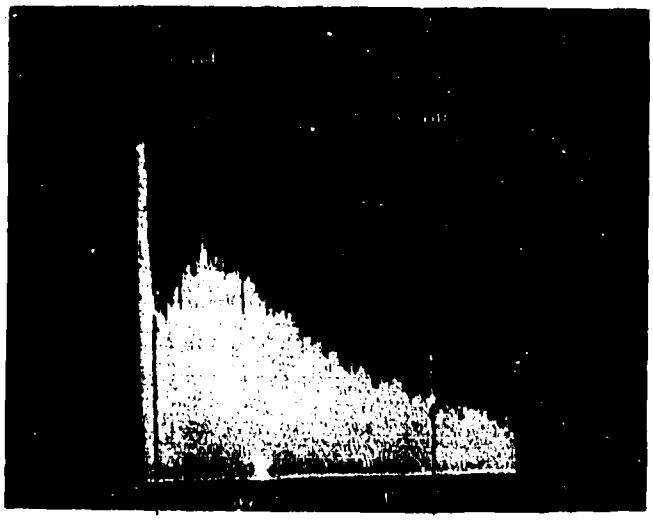
The wafers are then placed in the sputtering system which is evacuated to drive off any adsorbed water vapor. Typical pump down base pressures are on the order of 1×10^{-6} torr. The wafers are reverse-sputter etched for

20 KeV Defocused Beam



Pt 2.04 9.44

20 KeV Defocused Beam



Pt 2.04 9.44

- The Contact Region Contains About the Minimum Detectable Amount of Platinum.

Figure 3-51. KEVEX Photographs Showing the X-ray Energy Histogram From the Microprobe Analysis of a Device Contact (Top) and Adjacent Oxide Region (Bottom).

1 minute at 500 Watts in an argon atmosphere at 10 microns pressure. Then titanium-tungsten is deposited for 1 minute at 1000 Watts (250 A) in 10 microns of argon. The system is then pumped down to the base pressure. The nitrogen dopant gas is introduced and the system refilled with argon to a pressure of 10 microns (1 micron nitrogen/9 microns argon). The diffusion barrier is deposited at 1000 Watts for 9 minutes (2000 A). The system is then pumped to the base pressure, refilled with argon to 10 microns and a thin top Ti-W layer deposited without the nitrogen doping (250 A).

Without breaking vacuum, the wafers are moved under the gold target. The top gold layer is then deposited at 280 Watts for 53 minutes in 10 microns of argon. After the gold layer has been deposited, the wafers are moved back under the Ti-W target and a 500 A layer of this material is deposited at the 500 Watt power level. The wafers are then removed from the sputtering system in preparation for patterning.

If the metallization is not being patterned by a lift-off technique, positive photoresist is applied, exposed, and developed. The metallization sandwich can be patterned by ion milling or by wet chemistry etching. The ion milling process gives superior line width and edge definition but causes radiation damage to the bipolar devices. This radiation damage has been successfully annealed out with a 30-minute anneal in nitrogen at 500° C. If a wet chemistry process is to be used, the gold layer may be etched using a potassium iodide etch (25 g-potassium iodide, 6.25 g-iodine, 100 ml-water) which does not attack the titanium-tungsten layer. The Ti-W diffusion barrier layer is etched initially using hydrogen peroxide at 40° C and finished with a potassium ferri-cyanide etch (2g K3(Fe(CH)6), 1 g KOH, 100 cc H_2O). During the etching process, it has sometimes been useful to reflow the developed photoresist down over the edges of the metal pattern by heating the wafers to moderate temperatures for 30 minutes. The positive photoresist will soften and flow down over the pattern edges to minimize undercutting. After etching, the photoresist is stripped and the wafers rinsed in deionized water.

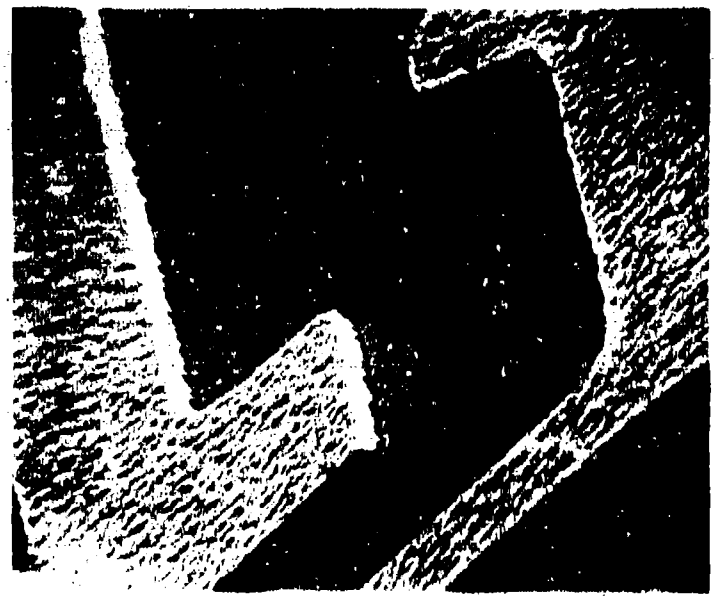
If a lift-off patterning technique is used, the metal is lifted off through the use of ultrasonics and high pressure water jets. The remaining photoresist is stripped and the wafers are rinsed in deionized water.

3.6 DUAL LEVEL METALLIZATION DEVELOPMENT

The resources of this program were devoted toward the development of integrated circuits capable of high temperature operation. Most of the effort was concentrated on development of a single level diffusion barrier/metallization but preliminary work was performed to show the feasibility of a dual level system. Ion milling and lift-off techniques were employed in defining the interconnect pattern in the Ti-W/Au metal system.

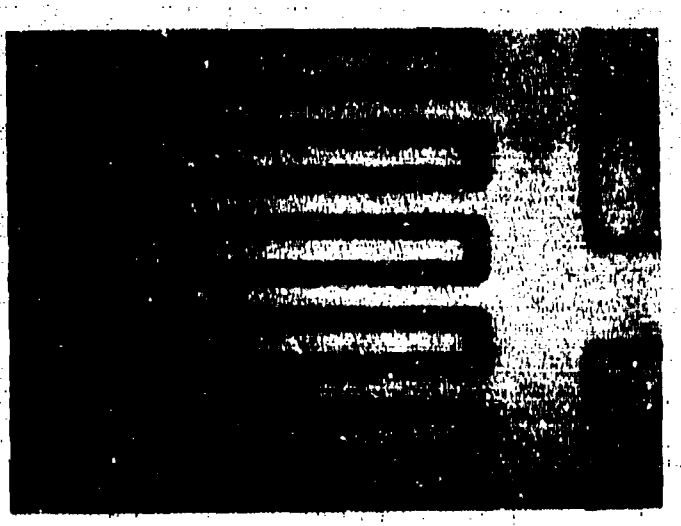
Ion milling is precise in cutting straight down through multiple metal layers in the metallization. The material is removed from the wafer due to collisions from particles in a high energy ion beam. The material removal is by a completely physical process that mechanically knocks atoms from the wafer. Figure 3-52 shows a SEM closeup of an ion beam milled Ti-W/Au metal system. The different metals may be seen on the vertical walls of the interconnection runs since the gold and Ti-W have different reflection coefficients with the electron beam in the SEM. An example of the small geometries that can be produced with the ion mill is shown in Figure 3-53. This photograph was taken of a portion of an interdigitated finger structure that has 5 μ wide lines and 4 μ wide spaces. In general, the ion mill can produce any pattern that can be resolved in the photoresist. The disadvantages of the ion milling process are that the process is slow from a throughput point of view, it tends to polymerize the photoresist such that it is difficult to remove from the wafers and the ion beam striking the wafer causes radiation damage in the bipolar devices.

A lift-off metallization patterning technique was explored to eliminate some of the problems inherent in the ion milling method. Many of the same process steps are used with lift-off and ion milling except that the order is changed and the milling step is not needed. Wafers are cleaned and photoresist is deposited and exposed. The surface of the exposed photoresist is hardened by soaking the wafers in chlorobenzene. Then, during the developing process, the softer bottom layers tend to dissolve more and undercut slightly. Figure 3-54 shows SEM photographs of the lift-off photoresist before metal deposition. The hardened edge on the top and the resulting undercut are clearly visible. The Ti-W/Au metallization is sputtered down on the wafer oxide through the photoresist openings and on top of the photoresist elsewhere. The photoresist with the metallization on top is shown in Figures 3-55 and 3-56.



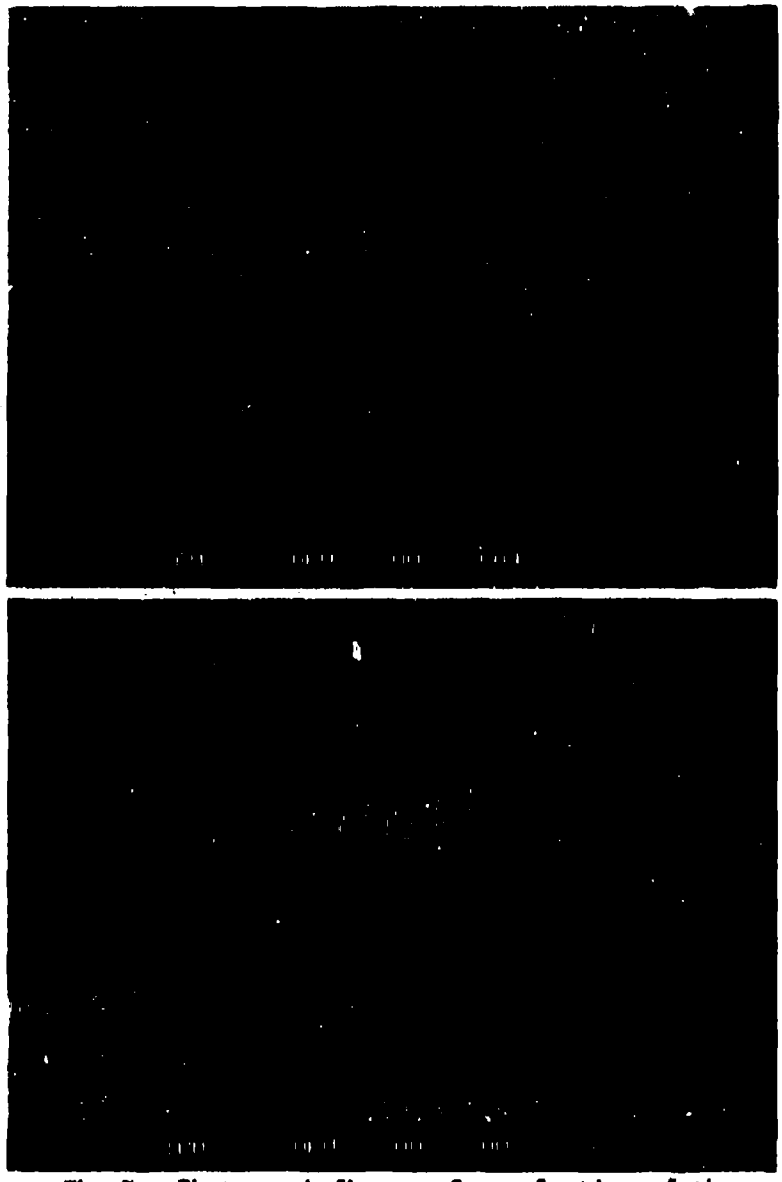
- The Bottom Metal Layer (Darker Color Seen on the Patterned Edge) is the Ti-W Diffusion Barrier.
- The Top Metal is Gold Deposited at 350° C.
- 7.5 Micron Interconnect Lines are Shown.

Figure 3-52. SEM Closeup of Ion Milled Metallization on Oxidized Wafers.



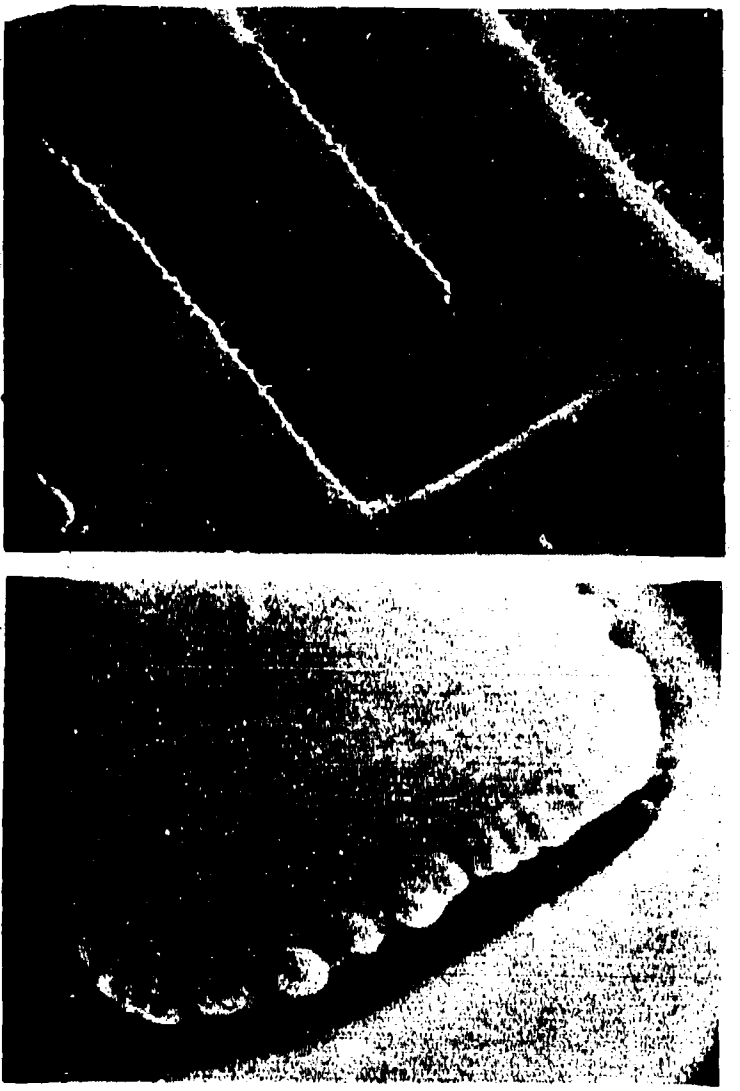
- The Ti-W/Au-Ti-W (Top Layer) Metallization Was Patterned Using the Ion Mill.
- The Metal Line Widths Are 5 Microns Wide With 4 Micron Spaces.

Figure 3-53. This Optical Photograph Shows Some of the Smallest Geometries on the E115 Mask Set.



- The Top Photograph Shows a Cross Section of the Photoresist Between What Will be Two Metal Runs.
- The Bottom Photograph Shows Part of the Photoresist Structure in an Integrated Finger Pattern.

Figure 3-54. SEM Photographs of the Lift-off Photoresist.



- The Photograph Shows the Wafer With Lift-off Photoresist After the Metal Deposition.
- The Metal Thinning at the Edge of the Run and the Photoresist Undercut Are Shown in the Closeup.

Figure 3-55. SEM Photographs of a Portion of the E115 Mask Pattern Being Used in the Development of a Dual Level Metal System.

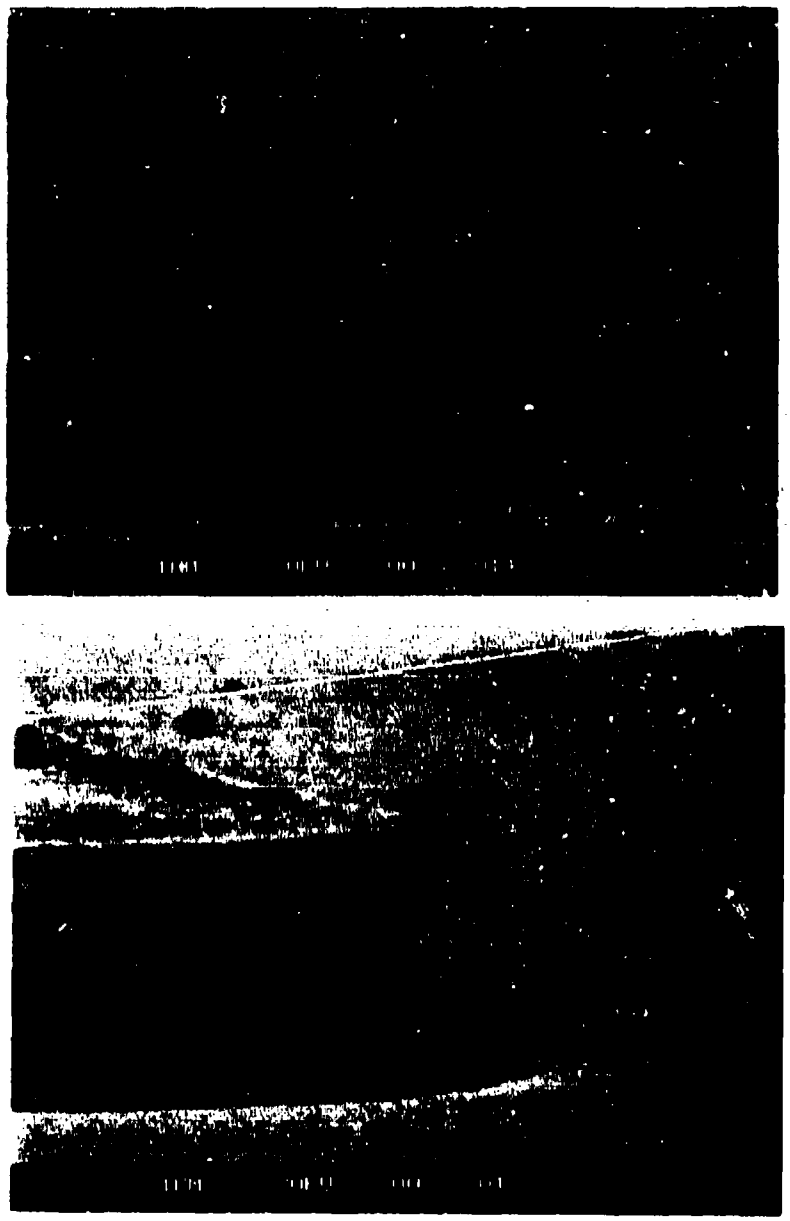


Figure 3-56. SEM Closeups of the Ti-W/Au/Ti-W Metal System Sputtered Onto the Lift-off Photoresist.

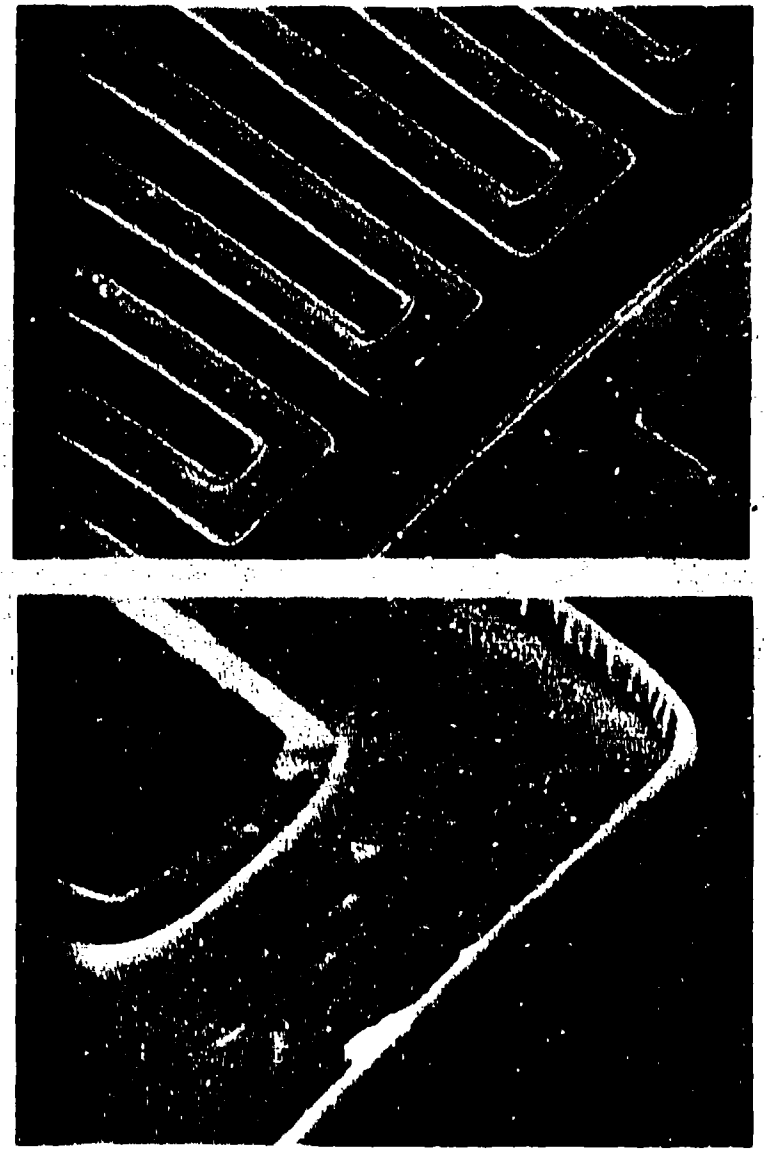
After depositing the metal, the photoresist is removed with normal solvents which lift the unwanted metallization off the wafer except where it was sputtered directly onto the oxide. Figure 3-57 shows a closeup of the actual lift-off process where the unwanted metallization is being torn or lifted off the desired metallization. An example of the resulting Ti-W/Au metal system patterned using the lift-off process is shown in Figures 3-58 and 3-59. These figures also illustrate the most serious disadvantage of this process. The metal layers are sputtered in sequence without breaking vacuum and the inside of the photoresist overhang receives a thin coating of the metallization. As a result, the lift-off is not "clean" but tears at the overhang region leaving a thin edge sticking up.

More work will be needed to eliminate the upturned edge of the lift-off metallization. This metal edge does not cause any problems for the single level metallization but it must be removed or eliminated for a dual level system. Two approaches are promising. First, the vertical distance from the underside of the photoresist overhang to the oxide floor could be reduced so that the edge remaining after the lift-off has no significant height. This can be achieved by using a thinner photoresist layer or by increasing the overhang thickness by modifying the photoresist hardening and developing steps. Second, the upturned edge of the metal could be removed after lift-off by etching techniques. This could be accomplished by evaporating about 1000 A of gold on top of the metallization to form a self-aligned mask. A Ti-W etch could then be used to remove the top and bottom Ti-W layers (both sides) on the upturned edge without removing the top Ti-W layer from the metal runs. Then a gold etch to remove the evaporated gold mask would also dissolve the gold core of the upturned edge. Figure 3-60 shows the results of the first attempt at implementing this etching process. The Ti-W layers were not etched long enough but the gold was removed from the center of the lift-off edge. Once these fabrication techniques are developed, the dual level metal system can then be evaluated to demonstrate its reliability at high temperature.

A preliminary processing run was performed to demonstrate the feasibility of dual level metallization for high temperature electronics and to determine if potential problems existed. A standard Ti-W diffusion barrier, sputtered gold, and a thin top Ti-W layer were used for the bottom metal level. The

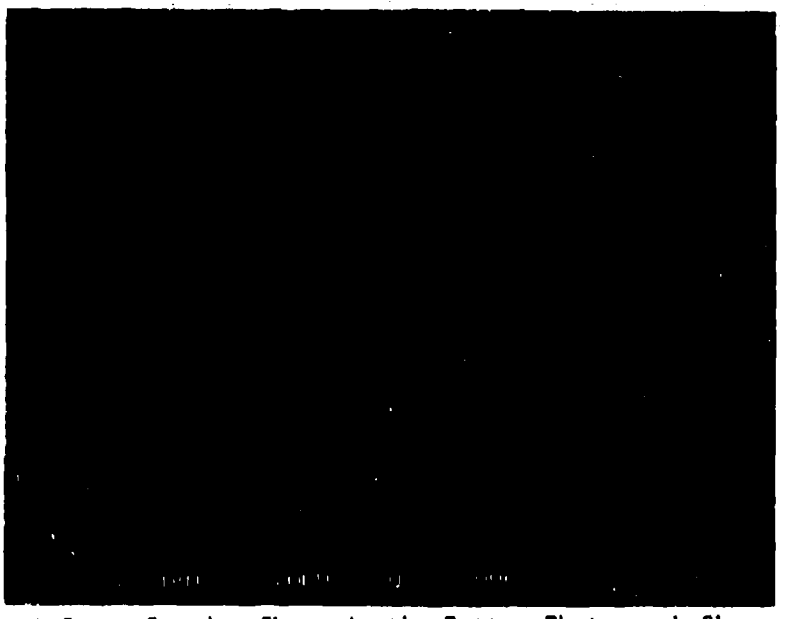
- A Ti-W/Au/Ti-W Metallization Has Been Sputtered on Top of Lift-off Photoresist.
- The Photograph Shows the Point Where the Metal Tears During the Lift-off and Leaves an Upturned Metal Edge.

Figure 3-57. SEM Closeup of the Lift-off Process.



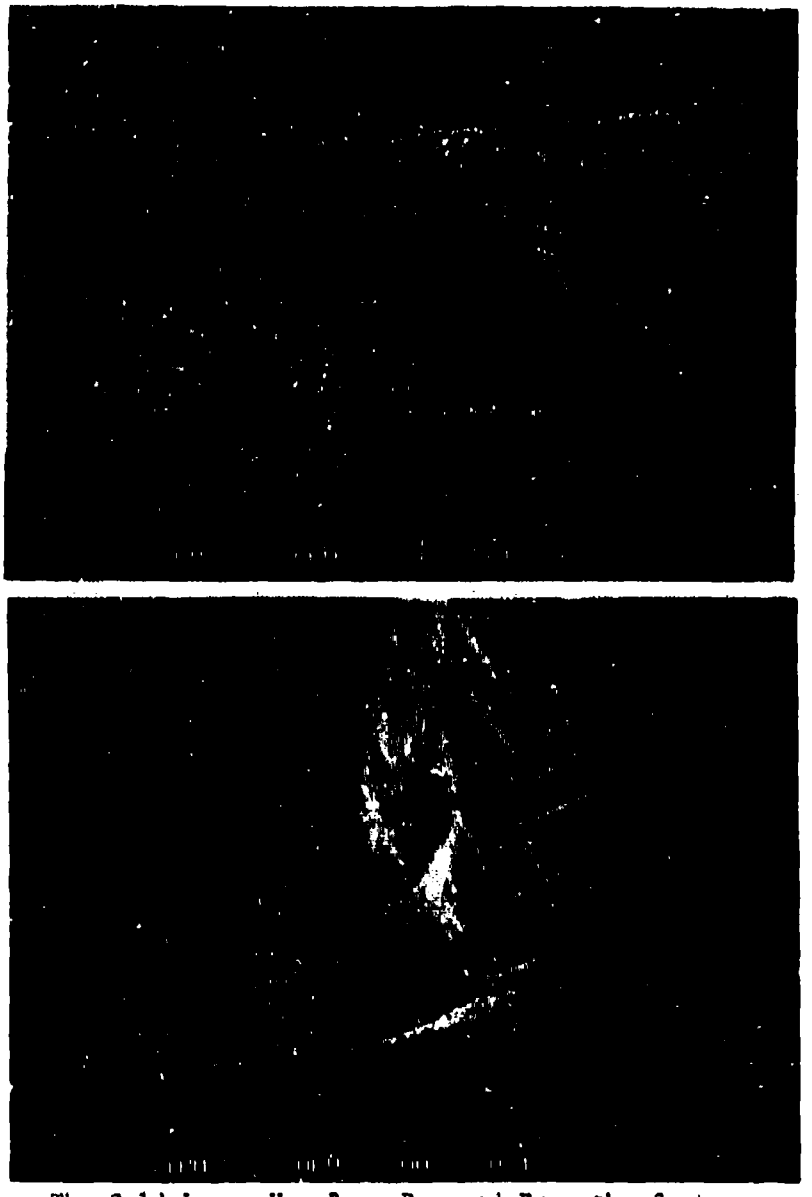
- The Patterned Metallization After the Lift-off Process is Shown.
- An Almost Vertical Strip (Upturned Edge) is Clearly Visible.

Figure 3-58. SEM Photographs of a Portion of the E115 Mask Pattern.



- A Cross Section Shown in the Bottom Photograph Shows the Ti-W/Au/Ti-W Metallization and an Evaporated Top Gold Layer (1000 A).

Figure 3-59. SEM Closeups of the Lift-off Patterned Metallization.



- The Gold Layer Has Been Removed From the Center of the Ti-W/Au/Ti-W Metal System by a Gold Etch.

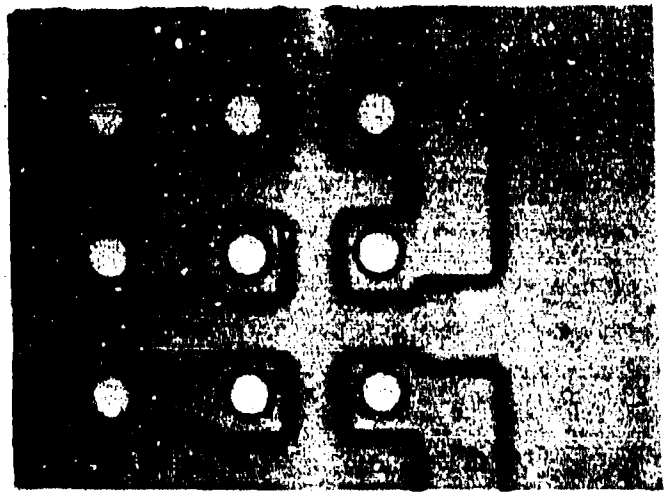
Figure 3-60. SEM Closeups Showing the Results of a First Attempt at Removing the Upturned Edge With an Etching Sequence.

bottom level was patterned using lift-off. Plasma nitride was deposited and via holes etched using buffered HF. Figure 3-61 shows the smallest vias on the mask after etching. After etching the vias through the dielectric, the wafer was put in a Ti-W etch to remove the top Ti-W layer where it was exposed through the via openings. This provides a check to assure that the vias are completely opened up and exposes the gold layer so that the second level metal can make a better contact.

Two experimental second level metallizations were deposited. The first was a duplication of the sequence used for the bottom metal layers while the second used a thicker (7000 A) gold layer sandwiched between a top and bottom Ti-W (500 A) layer. All metallization was patterned using lift-off and no passivation was applied to the second metal layers.

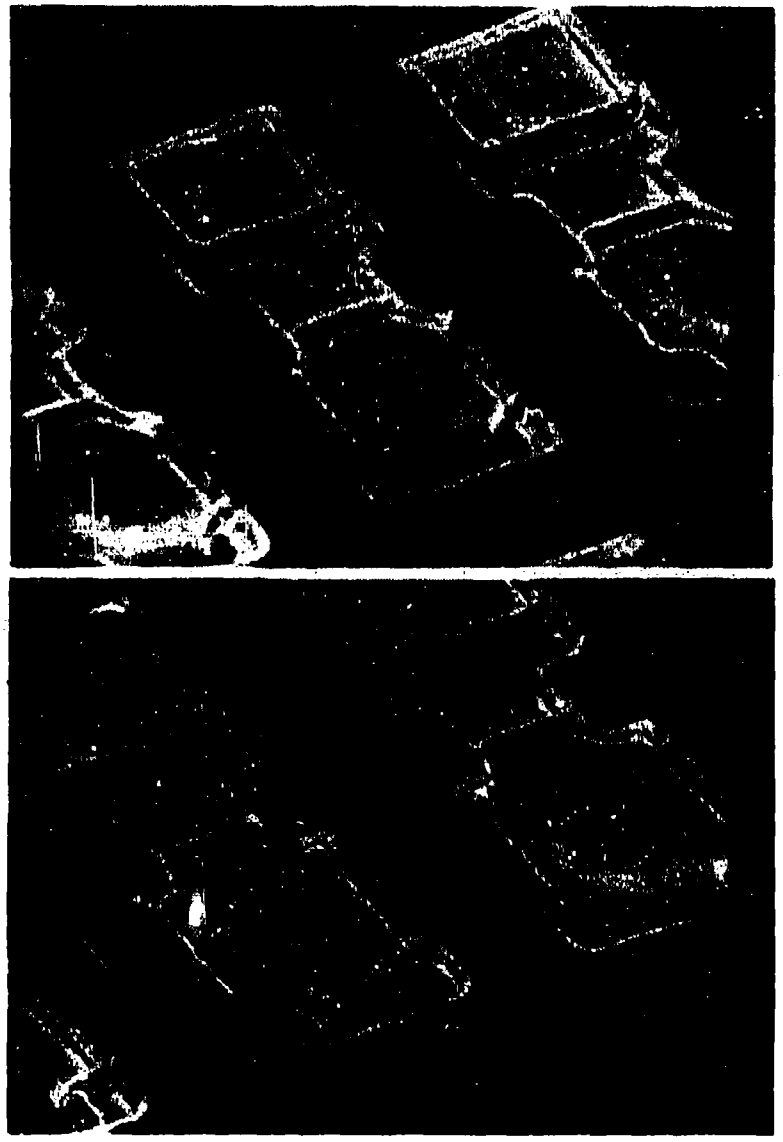
Two arrays of via chains between the top and bottom metallization levels were probed. Figure 3-62 shows SEM photographs of a portion of the 4 by 5 micron and 8 by 8 micron via chains. The resistance between the ends of the via chains ranged from 270 to 307 ohms with the same metal system on the top and bottom levels and from 187 to 204 ohms with the thicker gold on the top level. One chain out of eight was found to be open.

A crossover pattern that used serpentine structures at right angles on the top and bottom metal levels was tested to study the dielectric integrity. Figure 3-63 shows the crossover test pattern that was evaluated. The problem due to the lift-off patterning technique is clearly shown in this and the previous figure. The edges of the metal lines form an upturned cusp which can be seen on both the top and bottom metal levels. This cusp increases the step coverage problem for both the silicon nitride dielectric material and the metal levels.



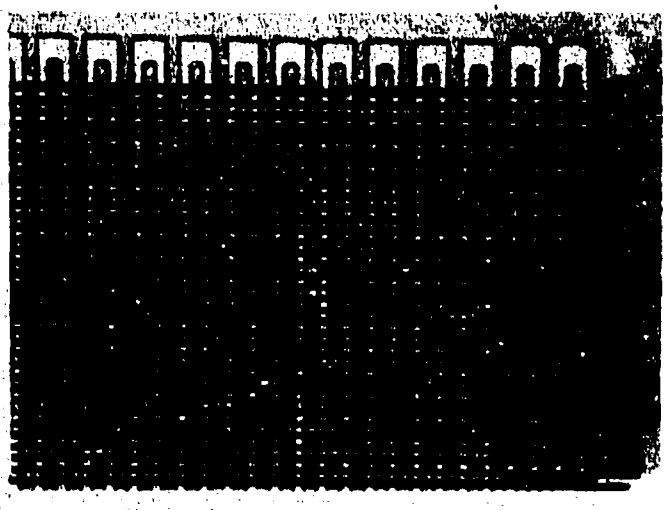
- The Photograph Shows a Via Pattern Etched Into the Silicon Nitride Dielectric Layer on Top of the First Metal Level.
- The Mask Dimensions For the Vias in This Case Are Four by Five Microns.

Figure 3-61. Optical Photograph of a Portion of the E115 Mask Pattern Being Used For a Dual Level Metal System Development.



- The Photographs Show 4 by 5 Micron (Top) and 8 by 8 Micron (Bottom) Via Chains Between the Two Metal Levels.
- Both Metal Levels Were Patterned Using Lift-off Techniques.

Figure 3-62. SEM Photographs of a Portion of the E115 Mask Pattern.



- Both the Top and Bottom Metal Levels Have Been Patterned by Lift-off.

Figure 3-63. Optical and SEM Photographs of a Cross-Over Test Pattern on the E115 Mask Set.

4.0 HIGH TEMPERATURE STRESS TESTING

The high temperature electronics in a nonfuel-cooled on-engine digital controller must survive for at least 10,000 hours at 300° C without failure. Accelerated life testing is necessary to demonstrate that electronics components will survive for their design lifetime. Consequently, high temperature stress testing must be performed at temperatures above 300° C in order to accelerate the testing. The stress testing accomplished during this contract phase concentrated on: (1) evaluating the extent of degradation of the ohmic contacts to the silicon, (2) determining the useful lifetime of the unpassivated barrier/metal system, (3) evaluating improvements in this lifetime as a result of various passivations on top of the silicon, and (4) determining if electromigration effects limited the useful life of the metallization system. These test results are described in this section.

4.1 OHMIC CONTACT TESTING

The measurement of ohmic contact resistance between a chip metallization and the silicon is complicated by the spreading resistance which occurs as the current spreads out in the higher resistivity silicon after being channeled through the small contact opening. This spreading resistance cannot be separated from the resistance which may be present due to a high resistivity layer between the metal and the silicon since both resistors are in series. However, assuming that the geometry of the contact does not change, the spreading resistance should remain constant. As a result, any changes observed in the spreading/contact resistance can be attributed to the contact resistance itself.

The ohmic contact test pads at the top and bottom of each test cell (that is, Pads 1, 2, 3, 4, 13, 14, 15, and 16 in Figure 2-2) are designed for ohmic contact evaluation with various sizes of contact openings. A chip cross section and electrical schematic of the ohmic contact pads are shown in Figure 4-1. As represented in the figure, the resistance R_0, R_1, R_2, and R_3 are the total spreading resistance and ohmic contact resistance series equivalent.

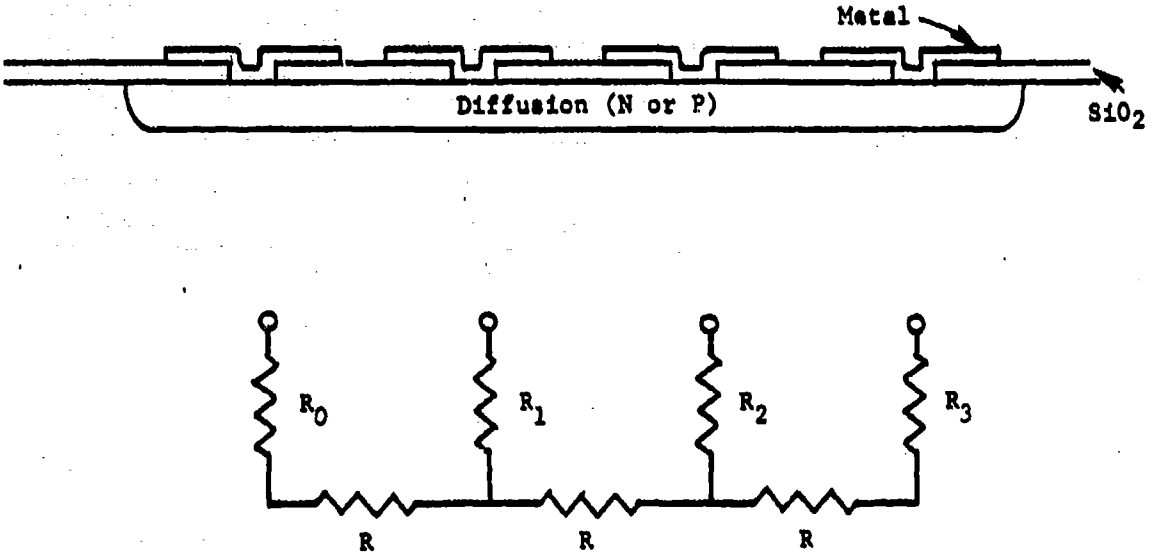


Figure 4-1. Cross Section and Electrical Schematic of the Contact Resistance Test Vehicle.

The experimental measurement procedure for the determination of the contact resistance is outlined in Figure 4-2. In this manner, the resistance in series with the two center contacts was monitored periodically during an accelerated life test.

A life test, which for purposes of distinction will be called Life Test "A", was initiated at 320° C and continued for 500 hours. At 500 hours into the test, the temperature was increased to 340° C and the test continued for another 2090 hours.

The contacts evaluated were 0.25 x 0.25 mil and 0.3 x 0.3 mil contacts from the barrier metal system to P doped (base) and n+ doped (emitter) silicon. In addition, 0.25 x 0.25 mil contacts were evaluated from the barrier metal to n+ on P doped silicon (integrated injection logic collector contacts). The life test results are shown in Table 4-1. The increases in the resistance values are attributed to increases in contact resistance. The total spreading plus contact resistance experienced from a gate output (collector) into the following gate input (base) is thus on the order of 100 ohms for 0.25 x 0.25 mil contacts.

Table 4-1. Average Contact Resistance During Life Test "A".

Type of Cell	No. of Contacts	Exposure at 320° C		Exposure at 340° C	
		0 Hours	450° Hours	0 Hours	2090 Hours
A1 (p-type)	37	79.9	83.8	84.0	90.8
A2 (n-type)	20	1.751	1.805	1.829	2.652
A3 (n-on-p-type)	10	1.632	1.680	1.701	2.175

A scanning electron microscope evaluation of the devices after the life test revealed the same sort of metallization damage that had been observed

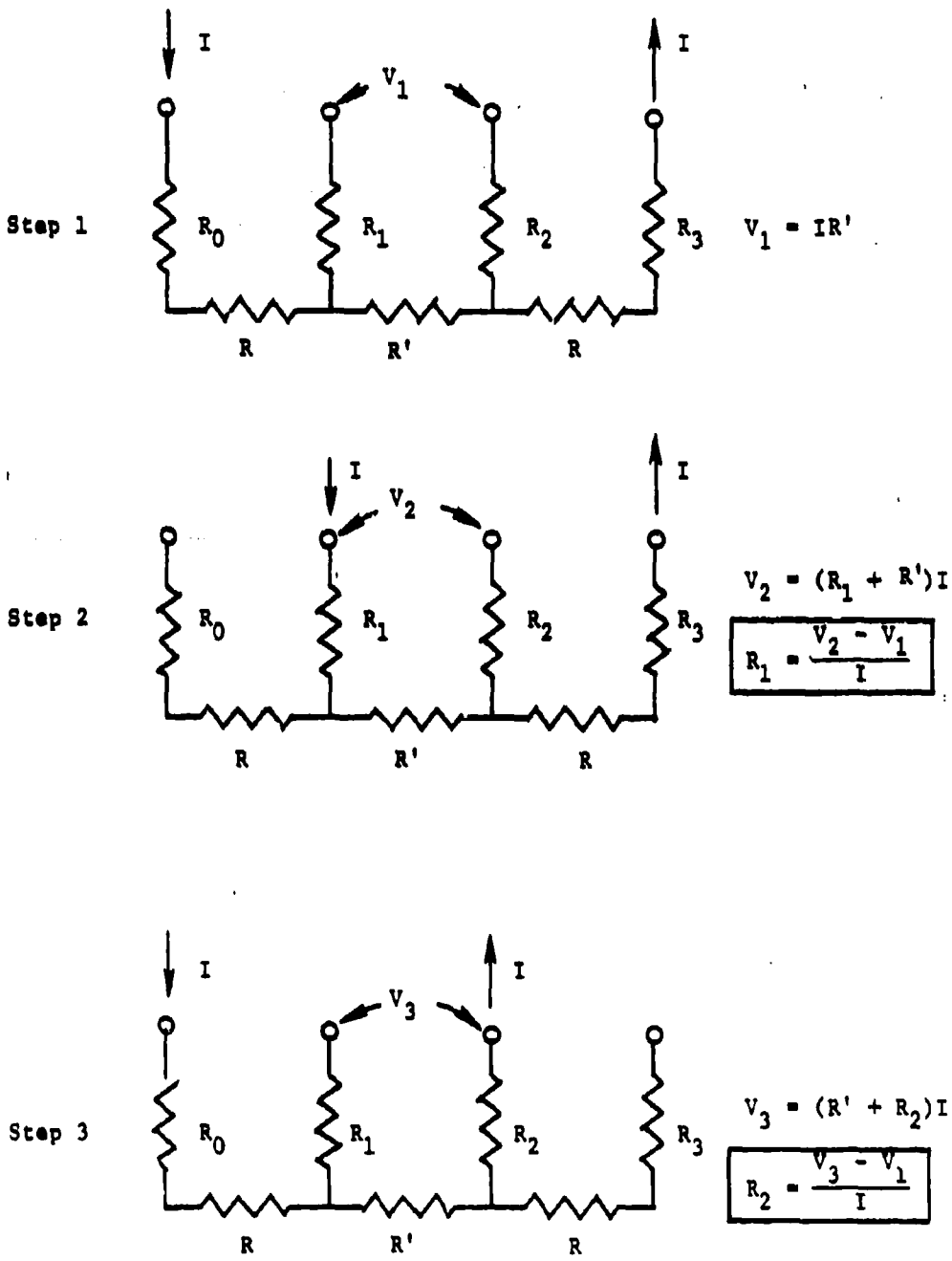


Figure 4-2. Experimental Procedure for the Determination of R1 and R2 (the Contact and Spreading Resistance Series Combination).

during earlier development experiments. The failures included metallization lifting, voiding, and crystal formation. This is shown in the SEM photographs (Figure 4-3) of a contact pad taken after the completion of Life Test "A". The ohmic contacts that were evaluated in this test were positioned at the center of the bonding pads and, as a result, were directly beneath the wire bonds that contacted these portions of the chip. By being in this location, the change of ohmic contact resistance determined during Life Test "A" may have been minimized.

4.2 RING OSCILLATOR LIFE TESTS

A series of powered and unpowered life tests was conducted during the course of this program phase using the Ti-W/Au metallization system and the ring oscillators contained on the 7-471 metallization test mask set. The life tests were used to evaluate each stage of the metallization development. When problems in the metal system were discovered as a result of a life test, the cause was investigated, and corrective action was taken to eliminate the failure mode. This portion of the report presents the life test results in chronological order. By describing the failure modes and the corrective action, a summary of the metallization development sequence is presented.

The chips for the life tests reported in this section were obtained from the 7-471 mask set. Each of the packaged circuits contained three ring oscillators and four logic gates on a single chip. All of the chips used a eutectic bond to secure the chip to the gold plating on the bottom of the package cavity. One mil gold wires were then bonded to the chips for electrical pin interconnection. The ring oscillators (except as noted) were powered at a level which resulted in 100 microamperes of current per logic gate during the stress tests. The individual logic gates were not powered during the life tests.

The first ring oscillator life test (designated Life Test "B") was conducted at 340° C. A Ti-W/Au metallization was applied to 7-471 Wafer 20 as shown below.

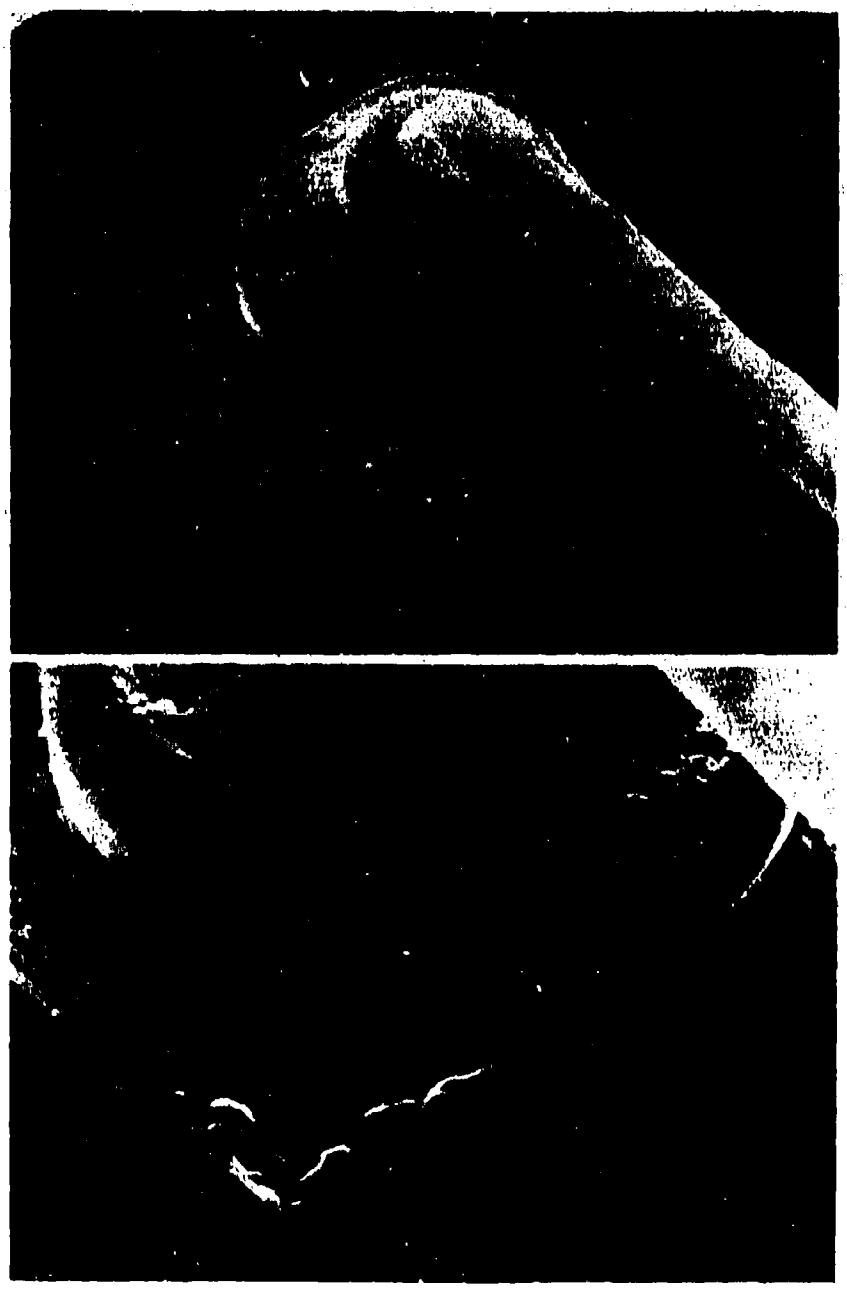
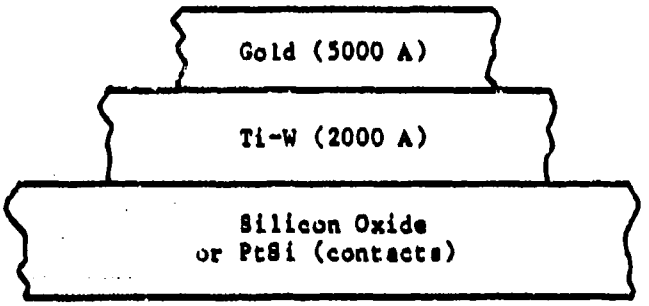


Figure 4-3. SEM Photographs of an Ohmic Contact Pad After 2590 Hours of Life Testing (Contact is in the Center of the Pad Under the Ball Bond).

Metallization Configuration for Life Test "B"



The metallization was patterned using a wet chemistry etching technique. The finished wafer was left unpassivated. The life test results are summarized in Table 4-2 below.

Table 4-2. Integrated Injection Logic Ring Oscillator Life Test at 340° C Life Test "B".

(Temperature dropped to 300° C - for each readout)

Total Hours on Test	0	24	68	163*	274	350	580	962	1220	1330	1600
Number of Functional Oscillators	26	25	25	24	20	20	19	19	10	8	0

*At this time one chip was removed from the test for evaluation (one oscillator had failed, two were still functional in this chip).

Chip No. 6 was removed from Life Test "B" after 1220 hours at 340° C when all oscillators had ceased to function. A SEM analysis revealed a metallization adhesion problem as the probable cause of failure. Figure 4-4 shows how the metallization started to lift at the edges after 1220 hours at 340° C. Figure 4-5 shows how the narrow interconnect metallization at the interior of the chips lifted except for the via contacts to active silicon. Finally Figure 4-6 shows the metallization lifting around contact openings to the active silicon. The problem with poor metal adhesion was most severe with

Figure 4-4. Metallization Lifting on a Bonding Pad After 1220 Hours at 340° C.

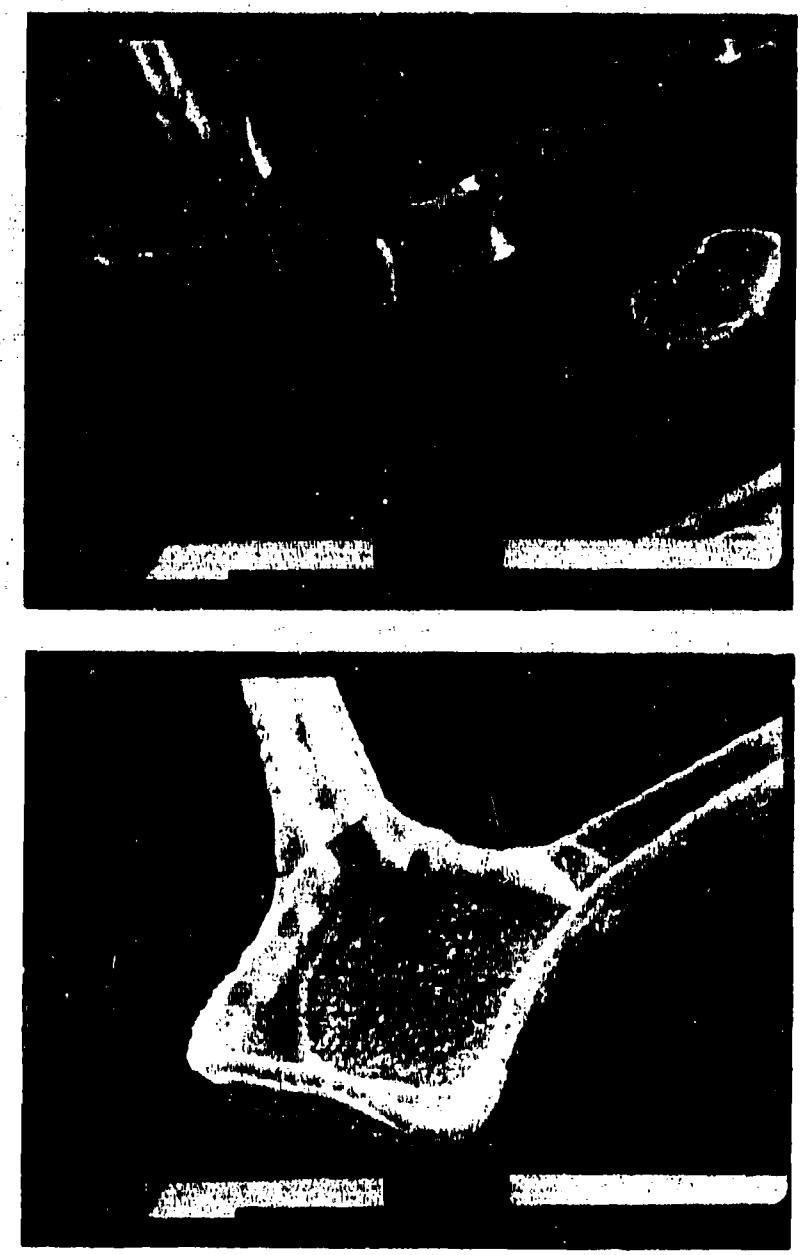


Figure 4-5. Metallization Lines Lifting After 1220 Hours at 340° C.

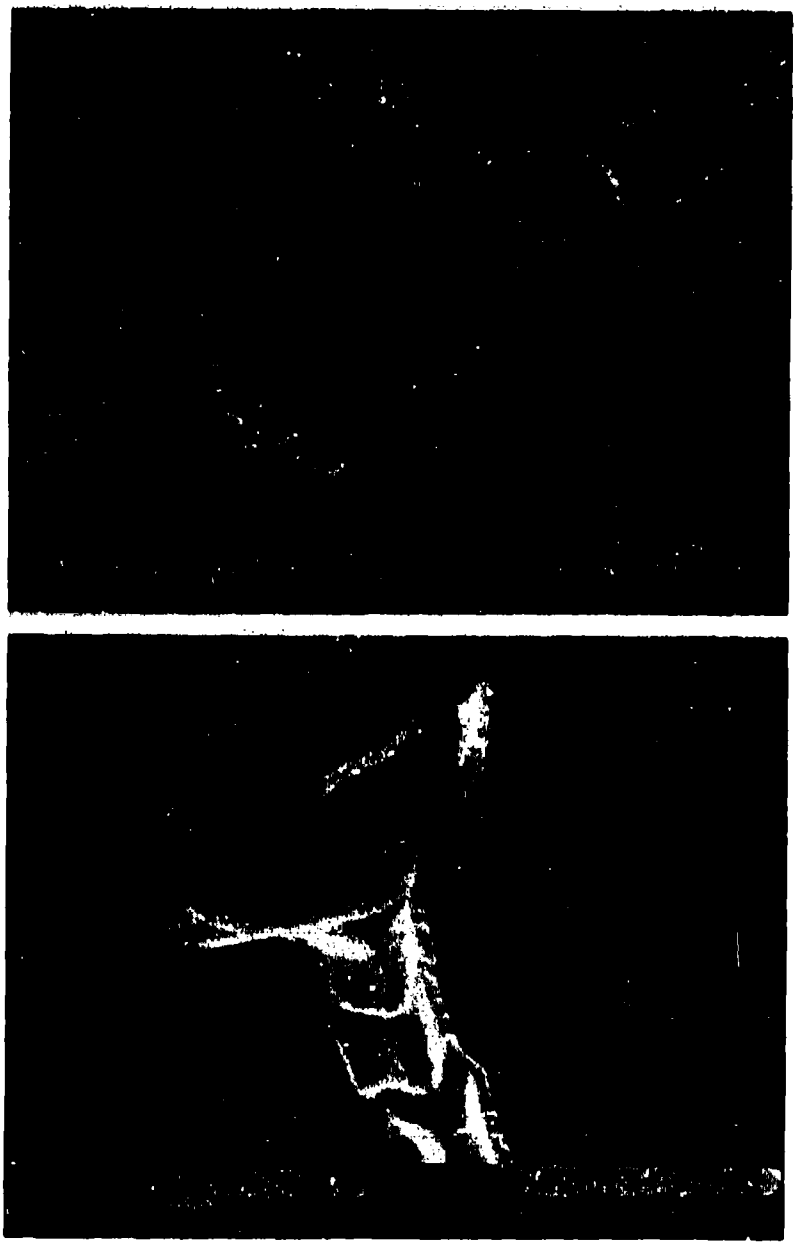


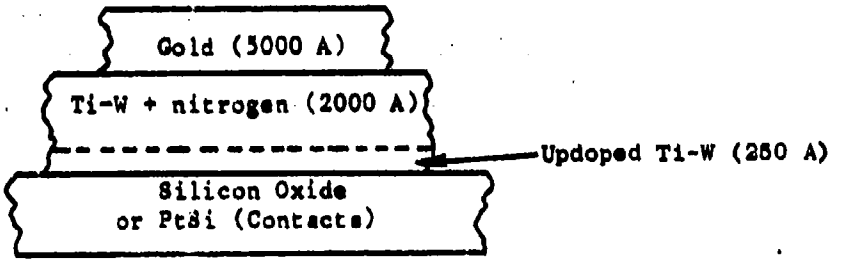
Figure 4-6. Metallization Lifting Around Contact Openings After 1220 Hours at 340° C.

narrow line widths on top of the chip field oxide. The large bonding pad regions and the contacts to silicon were not as severely degraded.

At the end of Life Test "B" (1600 hours at 340° C), various chips were examined to determine the failure modes. Although metallization adhesion remains the probable cause of failure, various other potential failure modes were evident. Figure 4-7 shows a bonding pad from a chip which was subjected to the entire life test. In addition to the adhesion problem, this sample exhibits evidence of metallization voiding and gold layer crystallization. Figure 4-8 shows gold crystal formations and metallization lifting on one of the ring oscillator circuits. Figures 4-9, 4-10, and 4-11 show details of various other metallization features observed after the life test.

At this point, the program resources were directed toward the solution of the metallization adhesion and diffusion barrier problem. This resulted in an improved barrier metallization system as shown below:

Metallization Configuration Used for Life Tests "C", "D", and "E"



This improved version of the barrier metal system was applied to wafers which were etched with a wet chemistry process in preparation for another series of life tests.

Wafers 17 and 21 were selected for packaging based on acceptable I^2L electrical characteristics as well as visual observation on metal alignment and etching accuracy. These wafers were diced and I^2L die selected for final packaging. The selected dies were eutectically bonded to the package header and gold lead wires bonded.

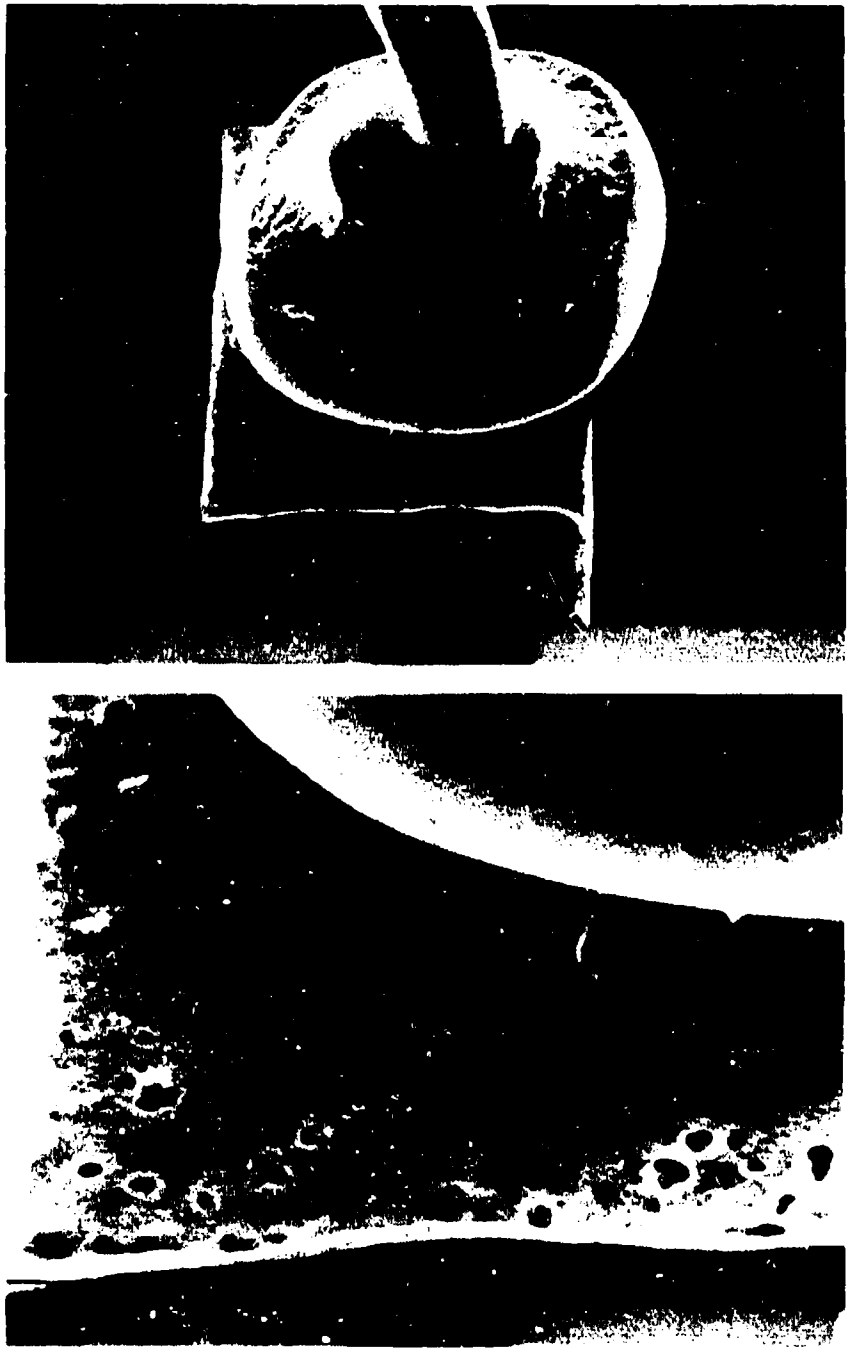


Figure 4-7. Bonding Pad of a Chip Exposed to 340° C for 1600 Hours.

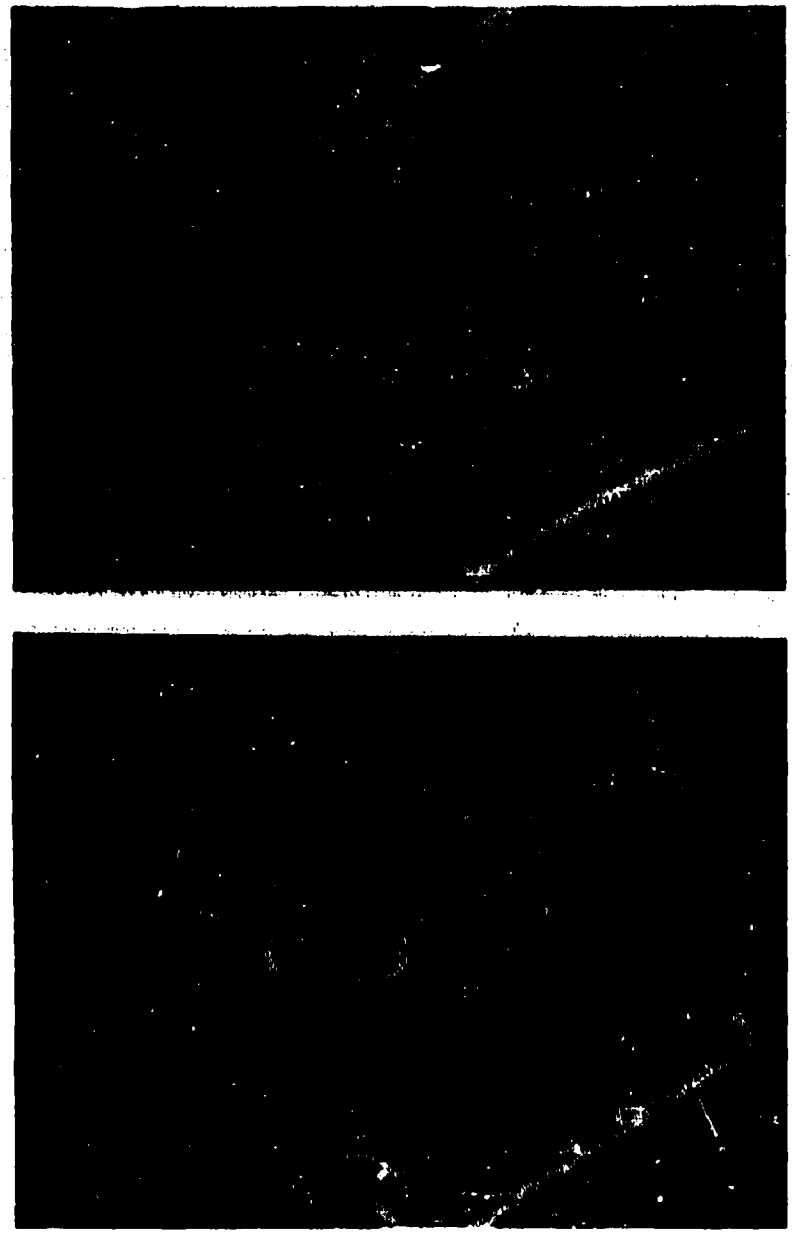


Figure 4-8. Gold Crystal Formations Observed After (Life Test "B") 1600 Hours at 340° C.

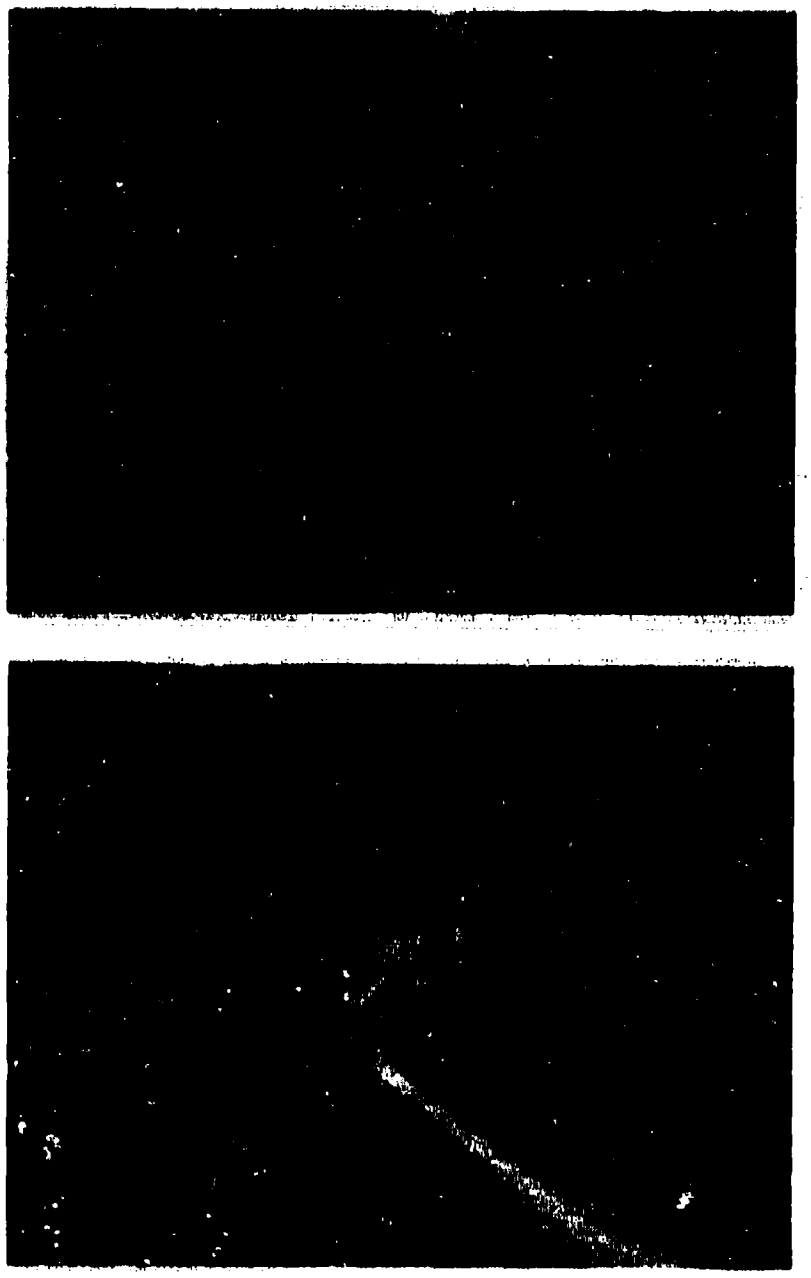


Figure 4-9. Ring Oscillator Metallization After (Life Test "B") 1600 hours at 340° C.

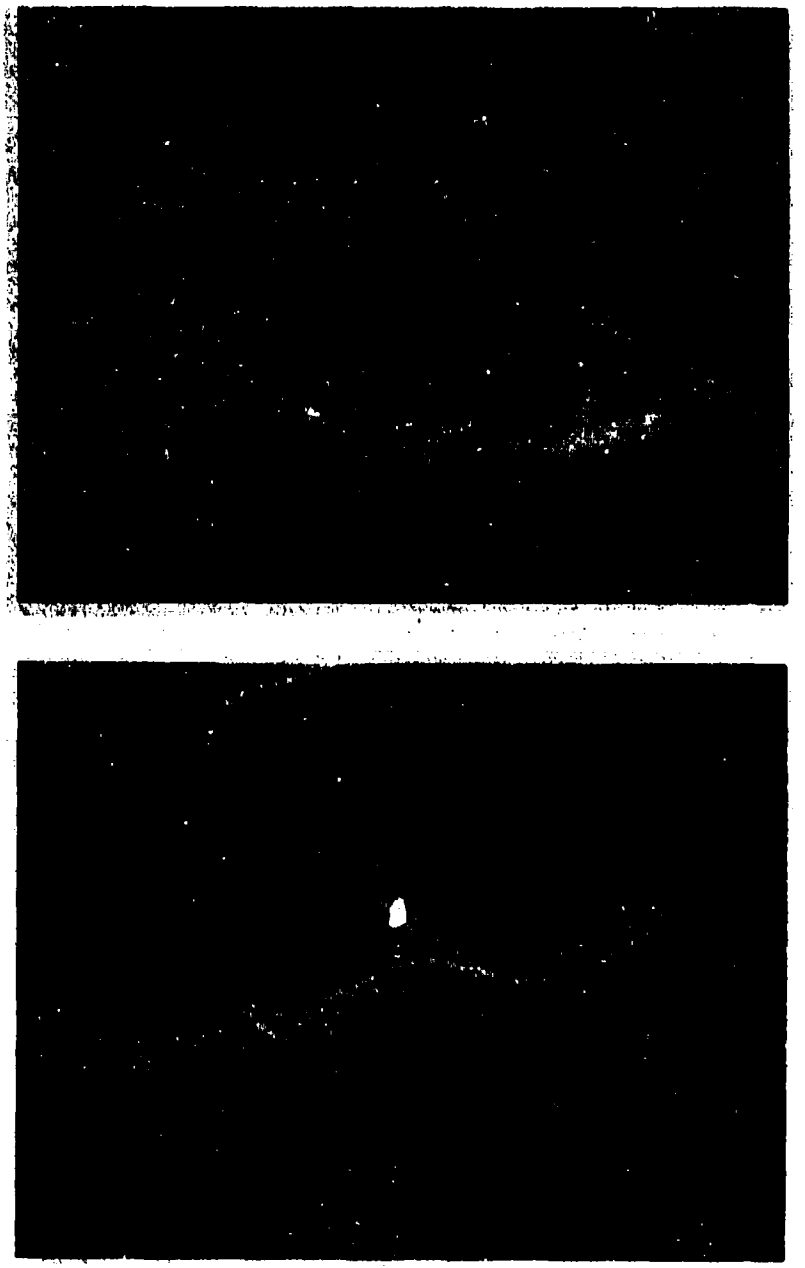


Figure 4-10. Closeup of Integrated Injection Logic Injector Contact After (Life Test "B") 1600 Hours at 340° C.

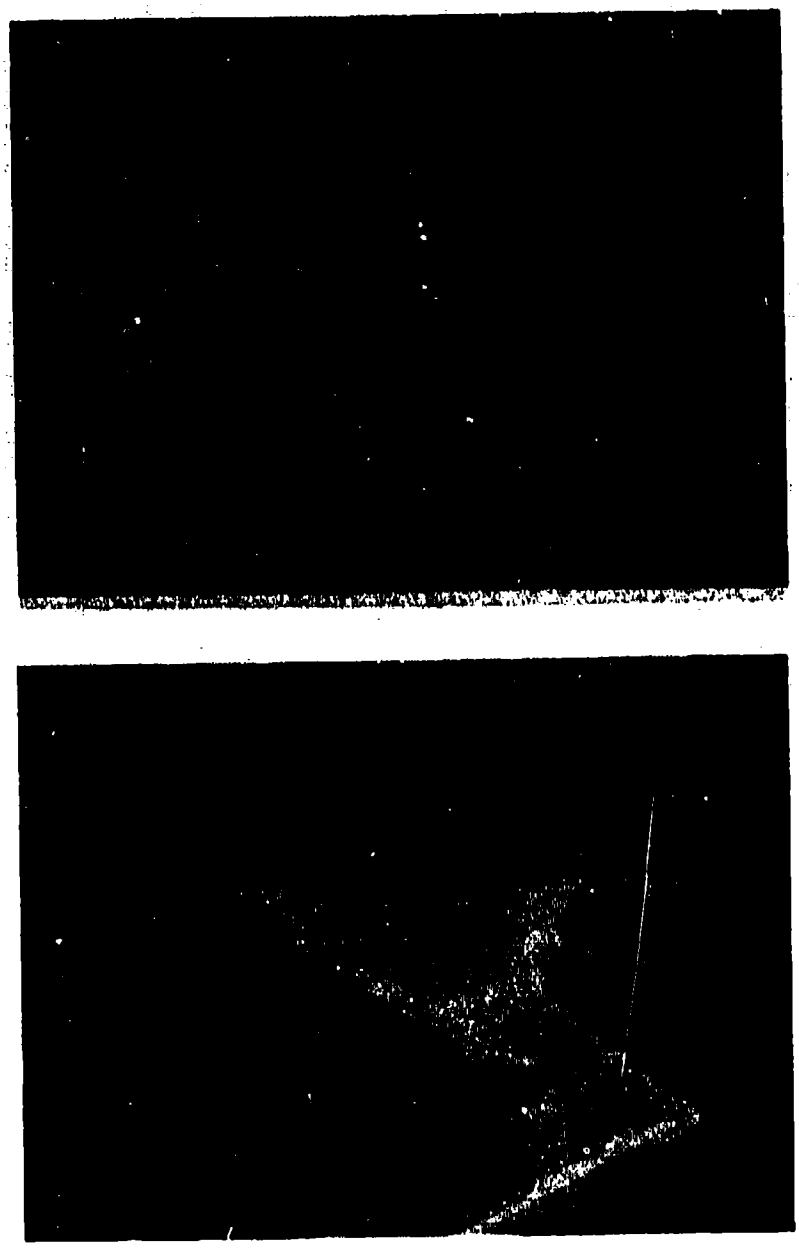


Figure 4-11. Closeup of Metallization Features After (Life Test "B") 1600 Hours at 340° C.

When the lids were put on using the high temperature gold-germanium preforms, it was found that the lid seals were not hermetic. The lack of hermeticity was found at both the fine and gross leak testing stage and was attributed to the particular die bonding procedure. It was decided to proceed with the life tests of the nonhermetic packaged devices because of time constraints and because the nonhermetic packages would provide a more severe environment than originally anticipated.

Two powered life tests (Tests "C" and "D") were conducted with the packaged circuits from these wafers. The first oven life test with this metallisation was conducted at 340° C and involved 10 powered chips (30 ring oscillators) from Wafer 21. A summary of Life Test "C" is shown in Table 4-3. The test was terminated after 341 hours when 13 out of 30 oscillators had failed.

Table 4-3. Wafer 21 Powered Life Test at 340° C - Life Test "C".

(Temperature Dropped to 300° C for Readout)

Total Hours on Test	0	104	173	341*
Number of Functional Oscillators	30	29	29	17

*Test Terminated

A parallel life test (Life Test "D") was conducted at 320° C using 10 powered chips (30 ring oscillators) from Wafer 17. Table 4-4 summarizes the results of this life test.

Table 4-4. Wafer 17 Powered Life Test at 320° C - Life Test "D".

(Temperature Dropped to 250° C for Readout)

Total Hours on Test	0	20	43	166	320	470	1000	1600
Number of Functional Oscillators	30	28	28	28	20	18	4	2

An additional unpowered life test (Life Test "E") employed packaged chips from both Wafers 17 and 21. Six chips from Wafer 21 and 10 chips from Wafer 17 were used in this test. The circuits were placed in a diffusion furnace set at 350° C with a nitrogen ambient. All circuits were removed from the furnace and cooled to room temperature for readout. The results of this test are shown in Table 4-5.

Table 4-5. Unpowered Life Test at 350° C (Diffusion Furnace) - Life Test "E".

(350° C Initial Temperature - Drifted up to 359° C at 325 Hours)

Total Hours on Test	0	20	70	210	325	420*
Number of Functional Oscillators (Wafer 21)	18	18	18	3	2	0
Number of Functional Oscillators (Wafer 17)	30	28	28	19	6	1
Total Failures	0	2	2	26	40	47

*Test Terminated

A SEM analysis of the failed devices from Life Tests "C", "D", and "E" showed that the severe metal adhesion problem, which had caused the earlier life test failures, was not the cause of failures in this case. The dominant failure mode for this series of life tests appeared to be self-diffusion in the gold layer causing crystallization and voiding in the metallization. This type of failure is indicated in Figures 4-12 and 4-13 which show SEM photographs of ring oscillators which failed after 320 hours at the 320° C. The specimens shown, although not from Life Tests "C", "D", or "E", were of that same vintage and were tested concurrently for considerably longer periods of time. Figure 4-14 shows one such specimen that was exposed to 320° C for 2200 hours. Even after this time, the metallization adhesion appears to be adequate.

Figures 4-15 and 4-16 show the metallization on a chip after 420 hours in the 350° C life test. The hillocks are confined to the edges of the pad areas but are pervasive throughout the ring oscillator metallization. Figure 4-16 shows the presence of hillocks, voids, and gold crystals. Figure 4-17 shows that similar defects appeared after 210 hours at 350° C during Life Test "E".

A variety of potential failure modes is evident from this series of life tests (C,D, and E). Metallization voiding was the immediate cause of the failures but gold mounds were also observed. The mounds were confined to a 5 to 10 μ region at the edge of the metallization pattern. It was eventually determined that these mounds were caused by wet chemistry etching techniques used in patterning the metallization. The Ti-W etchant would undercut the gold layer and leave a residue which caused the mounds which were actually bubbles.

A new lot of 7-471 wafers was diffused and the metallization reapplied to sample wafers in preparation for additional life testing. The metal system was ion milled instead of using the wet etch process. After ion milling, a silicon nitride passivation layer was deposited in an effort to physically restrain the gold crystal growth phenomena. The metal system and passivation are shown below:

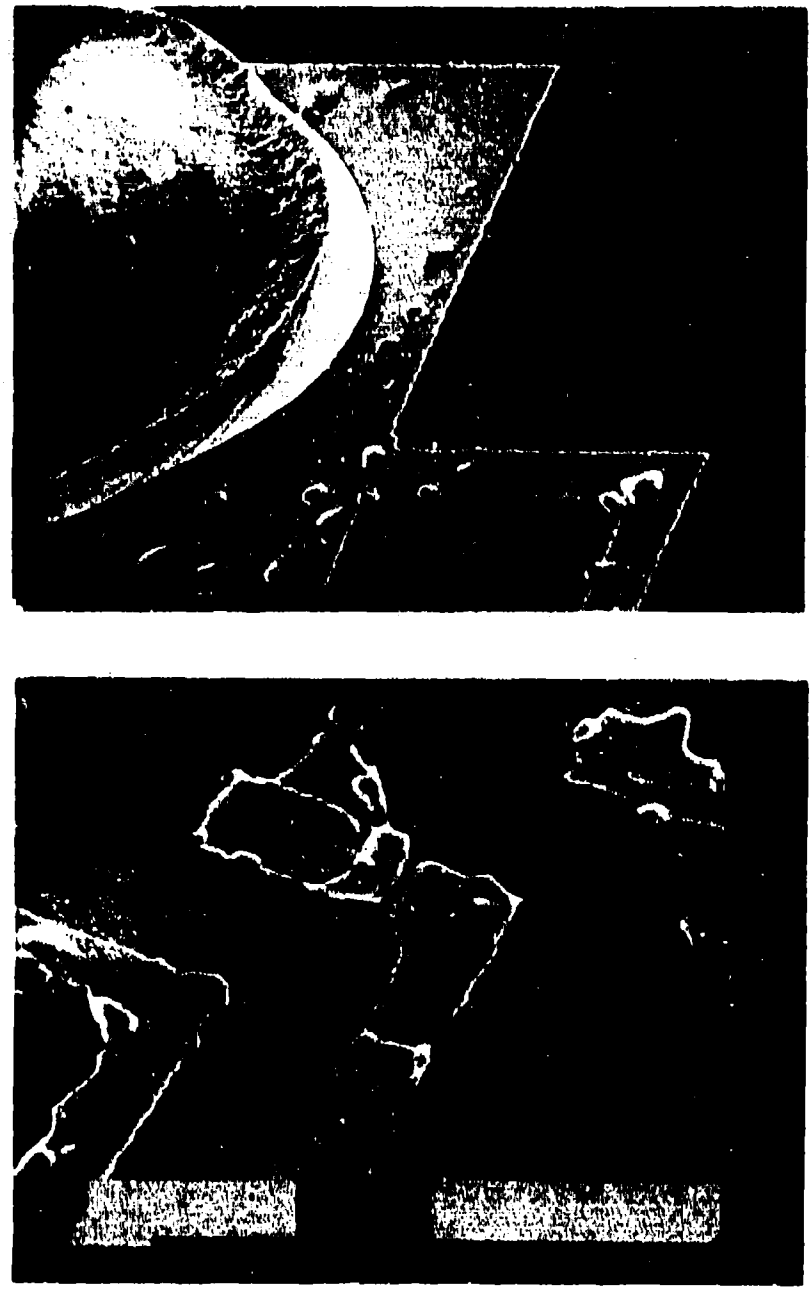


Figure 4-12. Bonding Pad and Ring Oscillator Metallization From Chips That Failed After 320 Hours at 320° C.

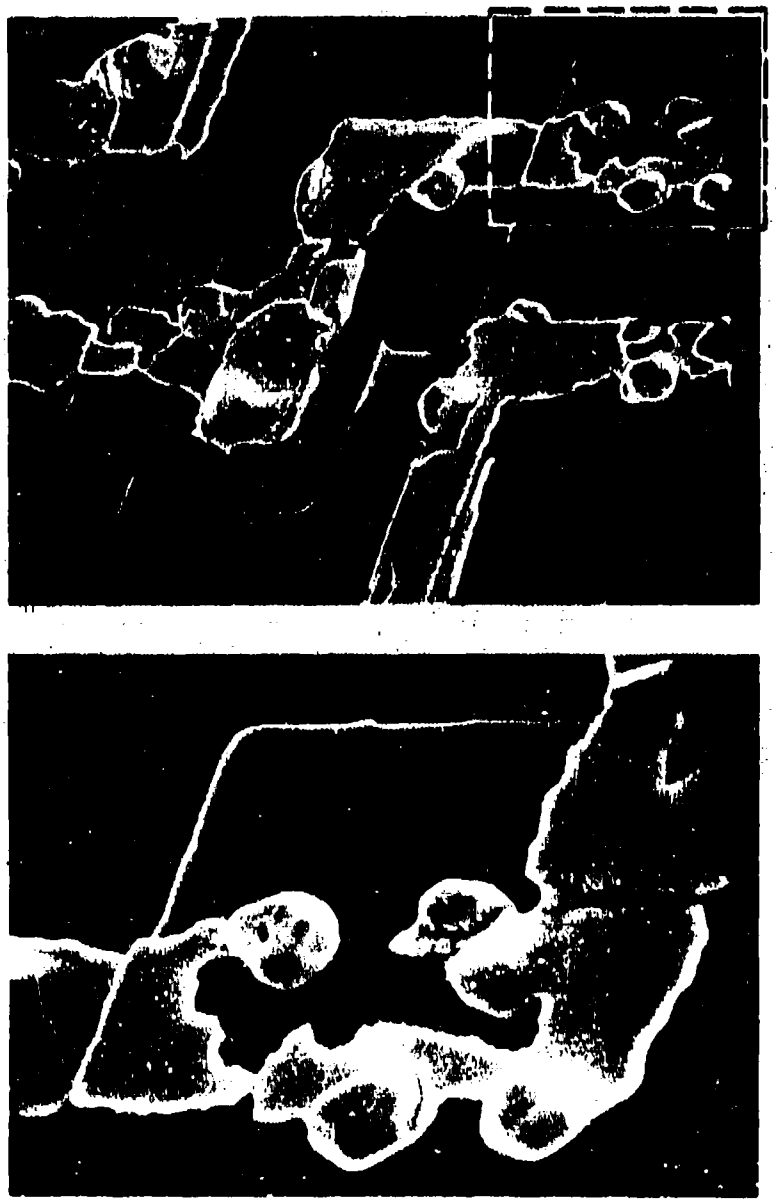


Figure 4-13. Closeup of Ring Oscillator Metallization That Failed After 320 Hours at 320° C.

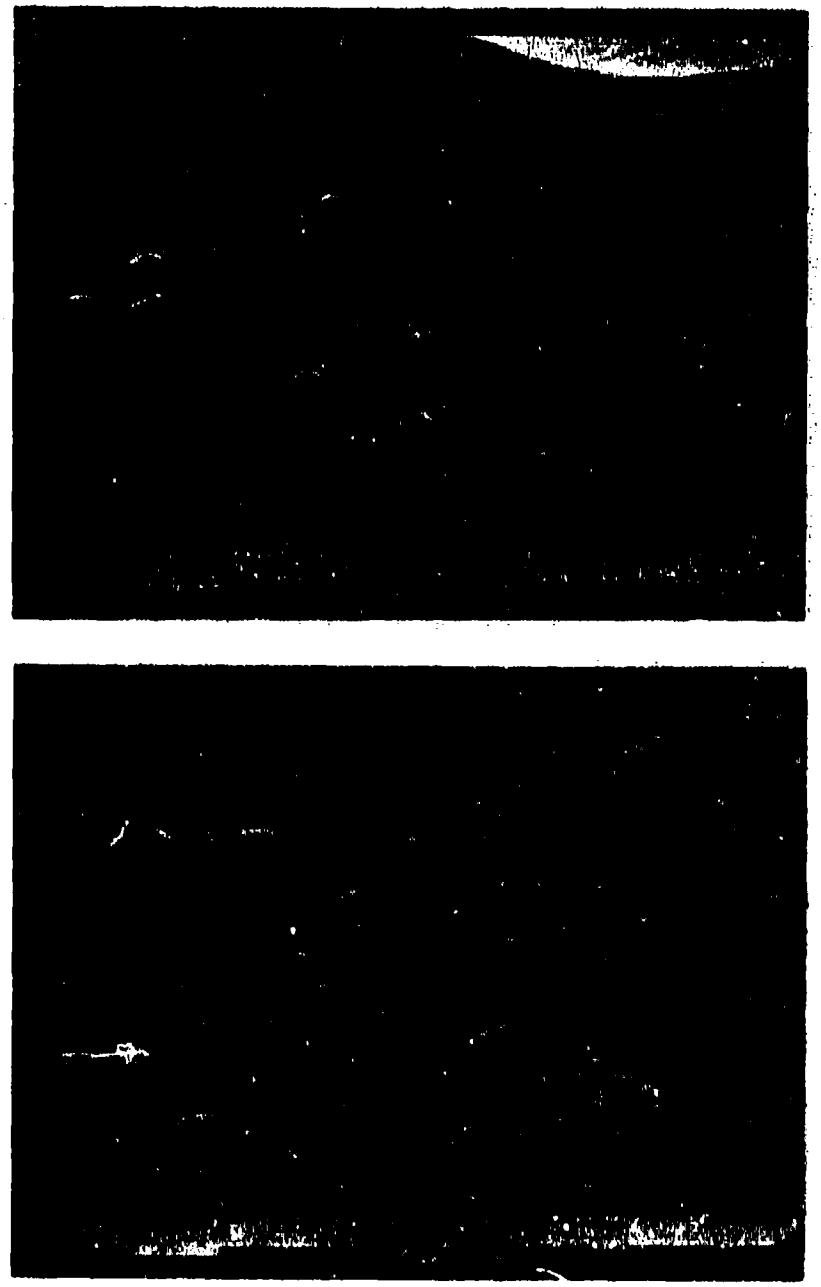


Figure 4-14. Metallization After 2200 Hours at 320° C.

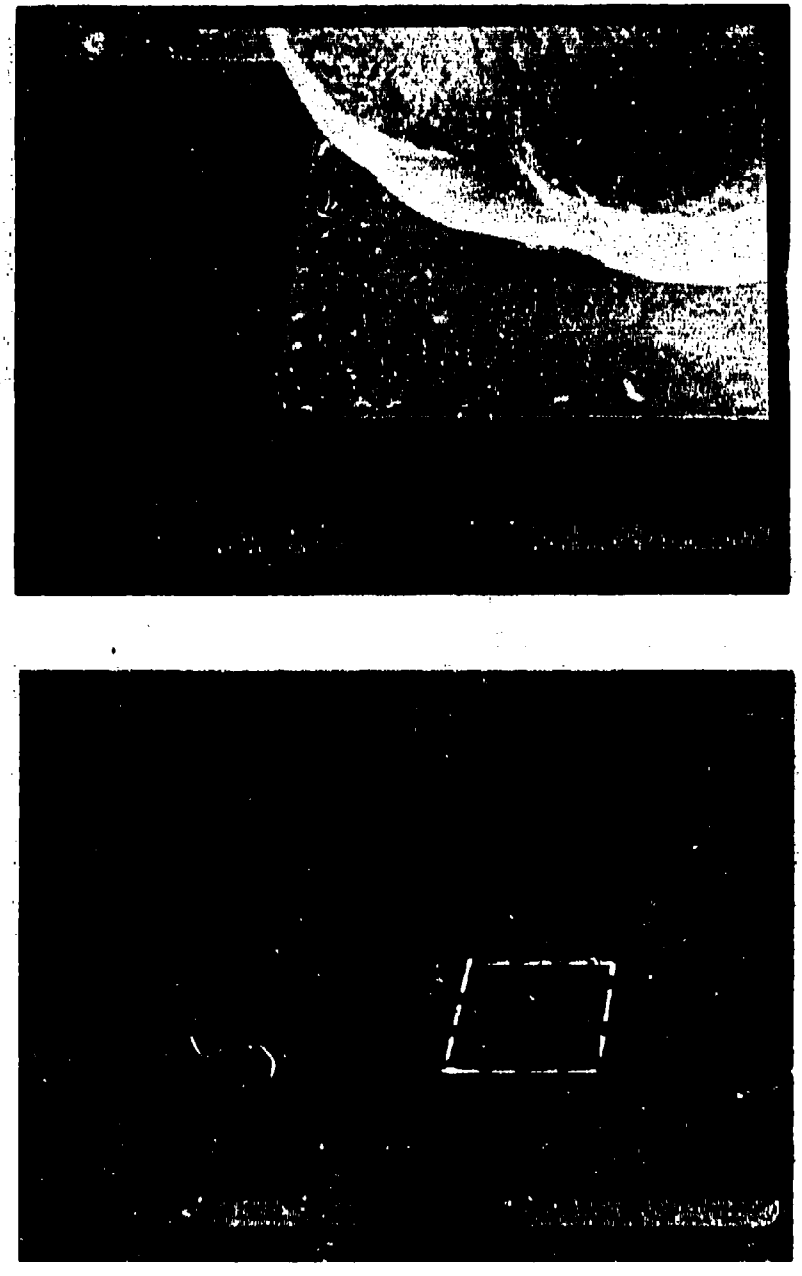


Figure 4-15. Barrier Metallization After 420 Hours at 350° C (Life Test "E").

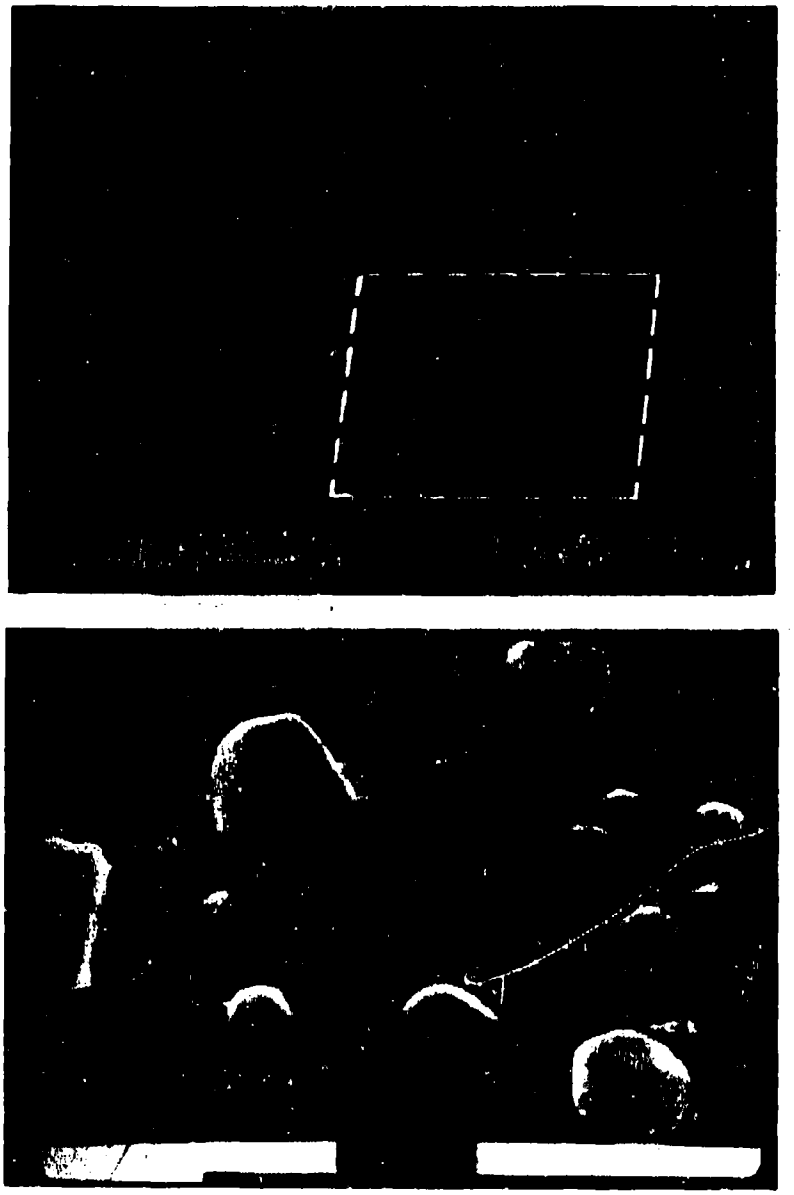


Figure 4-16. Closeup of Metal Runs After 420 Hours at 350° C (Life Test "E").

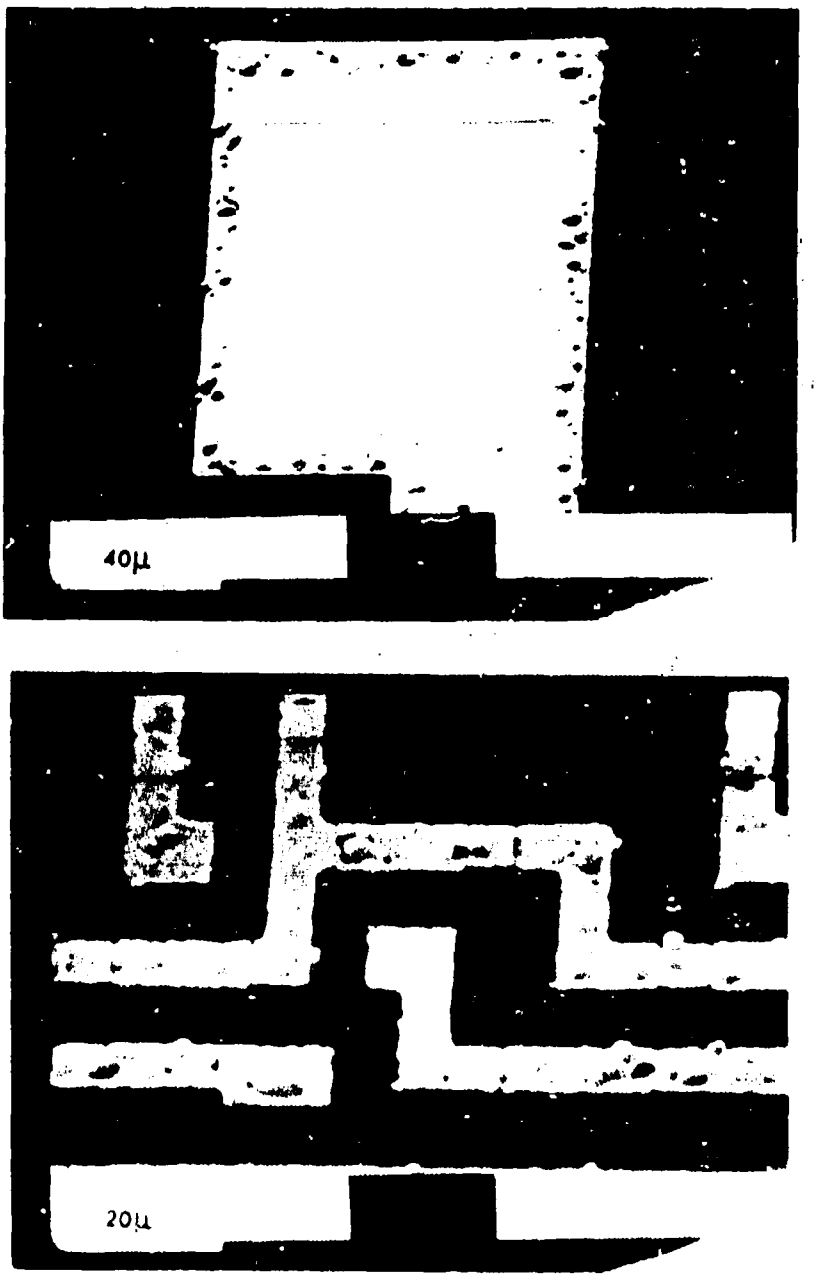
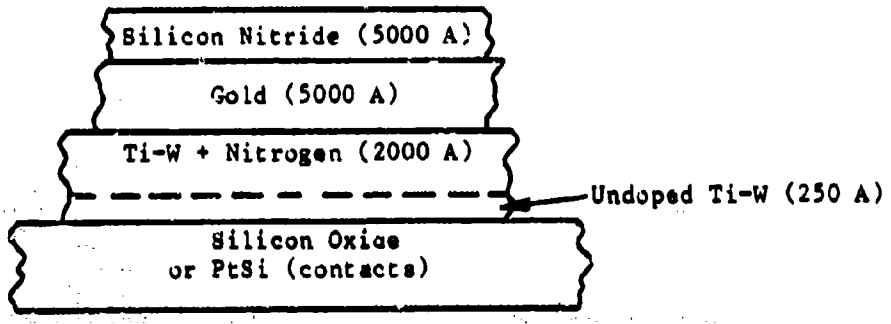


Figure 4-17. Metallization on a Chip That Failed After 210 Hours at 350° C (Life Test "E").

Metallization Configuration Used for Life Tests "F" and "G"



Two life tests (herein designated Life Tests "F" and "G") were conducted concurrently using this metal system. Ten chips (30 ring oscillators) from Wafer 19 were placed on a powered life test at 340° C. The oven temperature was lowered to 300° C to determine if the chips were still operational and then returned to the test temperature. A summary of Life Test "F" is shown in Table 4-6.

Table 4-6. Wafer 19 Powered Life Test at 340° C - Life Test "F".

Total Hours on Test	0	47	143	220	237	311	424	621	851
Number of Functional Oscillators	30	30	30	30	28	26	20	15	3

An unpowered life test at 360° (Life Test "G") was conducted to provide a leading indicator to possible failure modes. Ten packaged chips from this same wafer (No. 19) were placed in a diffusion furnace. The chips were removed and cooled to room temperature to check for correct operation. Life Test "G" was terminated when all but one of the chips had failed after 468 hours. The Life Test "G" summary is provided in Table 4-7.

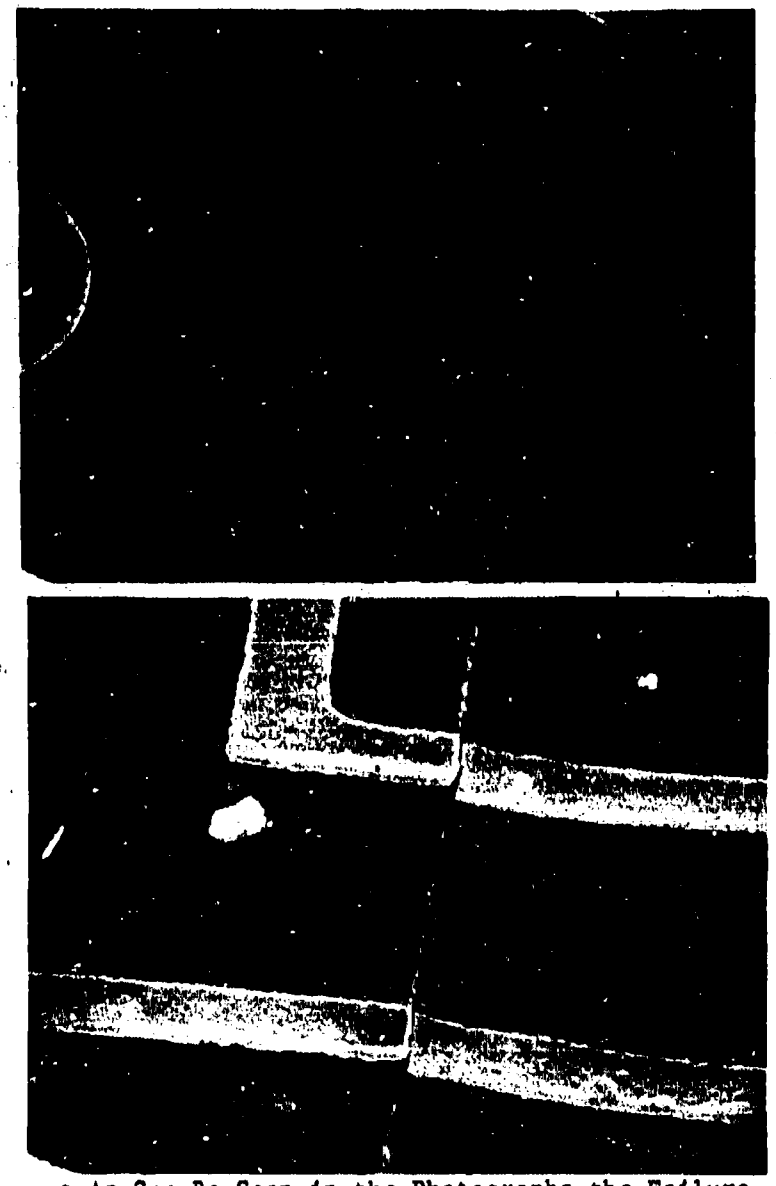
Table 4-7. Wafer 19 Unpowered Life Test at 360° C - Life Test "G".

Total Hours of Test	0	309	468
Number of Functional Oscillators	30	13	1

At 309 hours, one chip was removed from the 360° C Life Test "G" after all three ring oscillators had failed. An analysis of the ring oscillators and I^2L test cells indicated that all of the transistors that could be examined electrically with a curve tracer operated normally but that some of the chip connections to the ring oscillators were open circuits. The package lid was removed and all bonding wires were found to be intact. The silicon nitride passivation was removed with hot phosphoric acid and the chip was examined using a SEM.

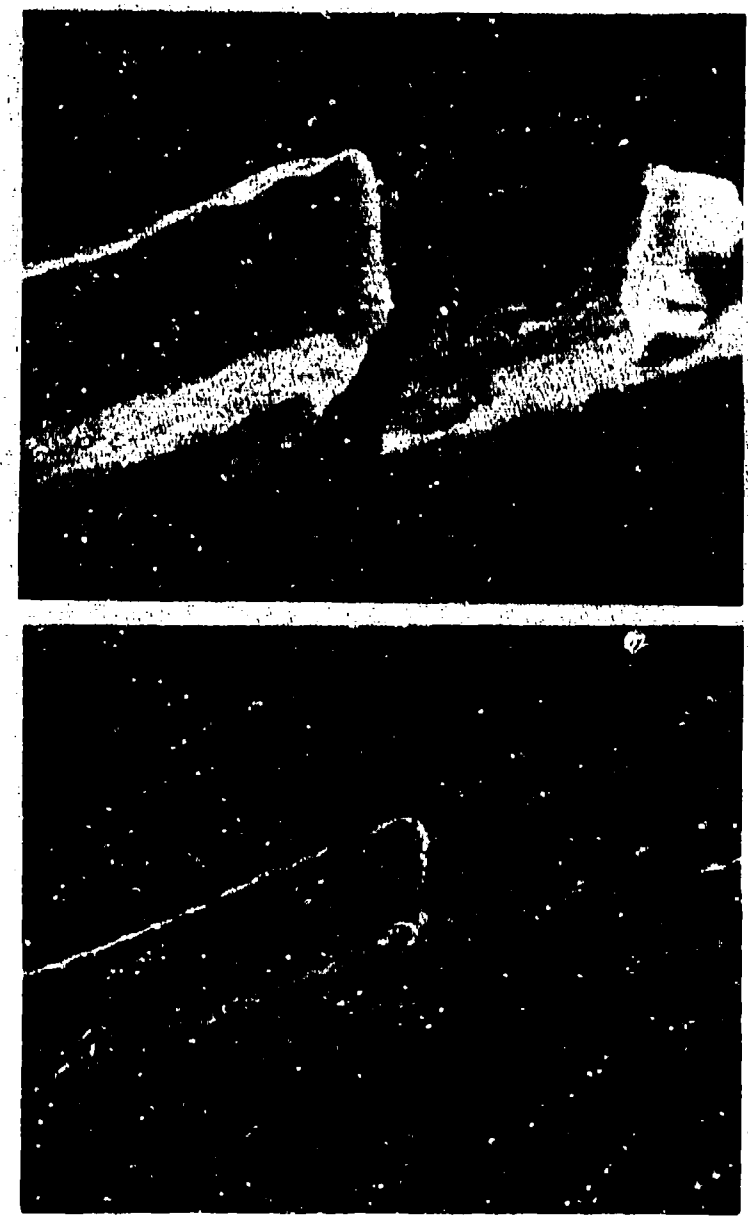
SEM analysis indicated that the causes of the failures were breaks in the metallization lines where they passed over an oxide step. Figure 4-18 shows SEM photographs of the injector (power) input and signal output lines for one of the ring oscillators on this chip. Figure 4-19 shows a SEM closeup of each of these lines from the previous figure. The pits in the silicon surface and the apparent undercutting of the Ti-W/Au metallization were caused by the acid etch used in removing the passivation layer. The failure of this chip during Life Test "G" was caused by a mechanical lifting of the metallization which, in conjunction with the oxide step, allowed the line to pull apart.

SEM voltage contrast photography was used to verify that the chip failures from the 340° C powered Life Test "F" were through the same mode just reported. At 621 hours into the powered life test, one chip was removed when all oscillators had failed. Figure 4-20 shows the SEM evaluation of that chip. The top photograph is a normal SEM view, while in the bottom photograph the voltage contrast signal is being applied to the bonding pad visible in the bottom right



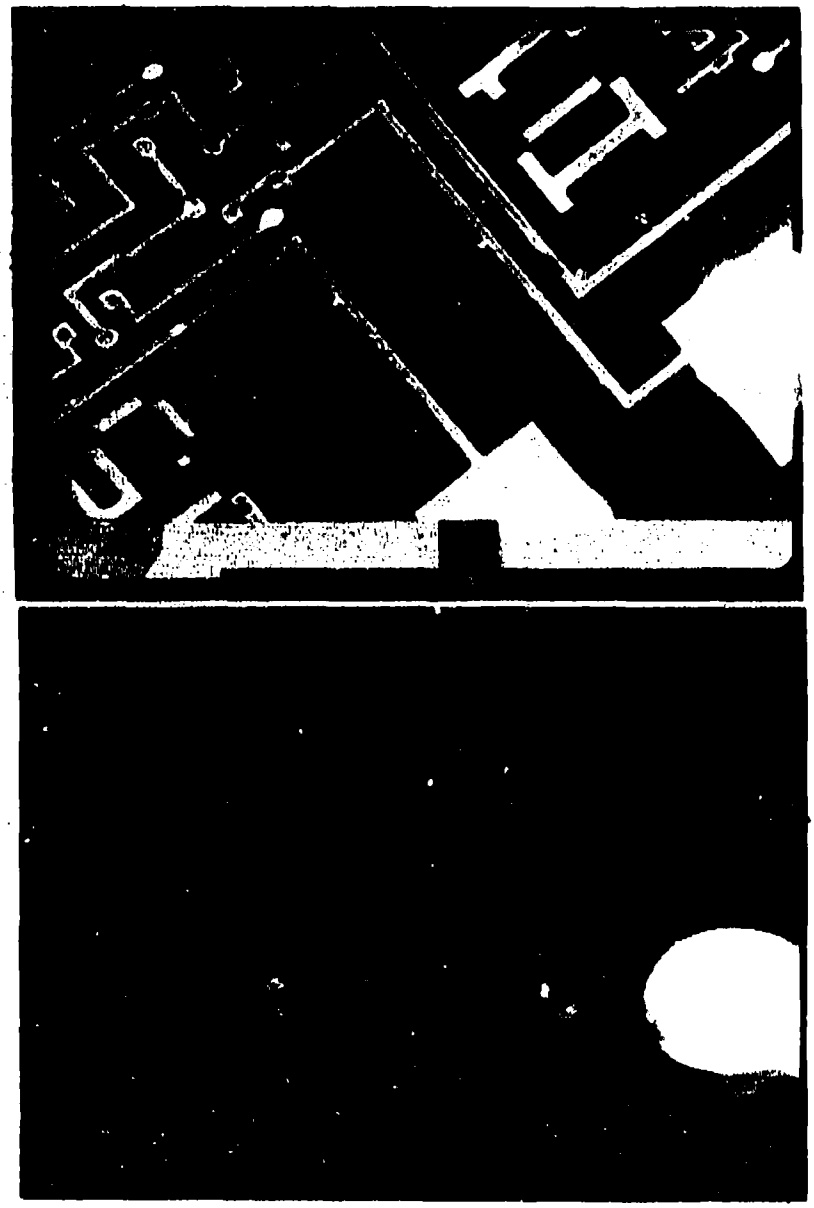
- As Can Be Seen in the Photographs the Failure is Due to Broken Metallization Runs Caused By Metal Lifting.
- The Nitride Passivation Has Been Removed From This Sample.

Figure 4-18. SEM Photographs of Chip No. 23 Which Failed After 309 Hours at 360° C (Life Test "G").



- As Can Be Seen in the Photographs the Failure is Due to Broken Metallization Runs Caused by Metal Lifting

Figure 4-19. SEM Closeup Photographs of the (Chip No. 23) Failed Metallization Runs Which Were Shown Previously



- The Top Photograph Shows a Normal SEM View of a Portion of the Chip While the Bottom Photograph Illustrates the Voltage Contrast Technique.
- The Two Metallization Runs Leading From the Bonding Pads (Bottom Right Corner) Are Open Where They Cross an Oxide Step.

Figure 4-20. SEM Photographs of Chip No. 2 Which Failed After 621 Hours at 340° C (Life Test "F").

corner. This line is the output signal from the ring oscillator. There is an induced (voltage contrast) electrical signal on the adjacent pin (bottom middle) since that pin was not grounded in the SEM. As shown in the figure, both metal lines are open where they cross the oxide step since the electrical signal used to provide the voltage contrast effect does not propagate past this step.

The metallisation open circuit failures experienced in Life Tests "F" and "G" sparked a new investigation into the metal system. This study was discussed in Section 3.4 entitled "Metallization Adhesion" and resulted in elimination of the nitrogen stuffing at the Au/Ti-W interface as well as at the PtSi/Ti-W interface. New wafers were processed using the knowledge gained in this exercise with life testing currently being under a subsequent program (Contract N00014-83-C-2393).

When the last wafer lot of 7-471 wafers was being diffused, two wafers were completed with aluminum metallisation to evaluate the lot yield before accepting the remaining wafers without metallization. A decision was made to subject some of these chips to a life test to obtain a comparison between aluminum and gold-based metal systems. The aluminum was deposited by E-beam evaporation of pure aluminum (no silicon) to a thickness of 12,000 A. An extensive sintering cycle dissolved enough silicon from the device contacts to essentially saturate the metal with silicon. A plasma deposited silicon nitride passivation layer of 7000 A was deposited and the chips from Wafer 6 were packaged in aluminum compatible CERDIP packages using aluminum bonding wires.

As before, two life tests at different temperatures were conducted with the aluminum metallized chips. A powered life test (designated Life Test "H") was conducted at 340° C using 10 of the packaged chips (30 ring oscillators). Each of the gates was biased at 30 μA. The worst case current density was in a ground return line that was 0.3 mil wide (7.5 μ). As a result, the highest current density was less than 10,000 amp/cm^2. A summary of Life Test "H" is provided in Table 4-8.

Table 4-8. Wafer 6 Powered Life Test at 340° C - Life Test "H".

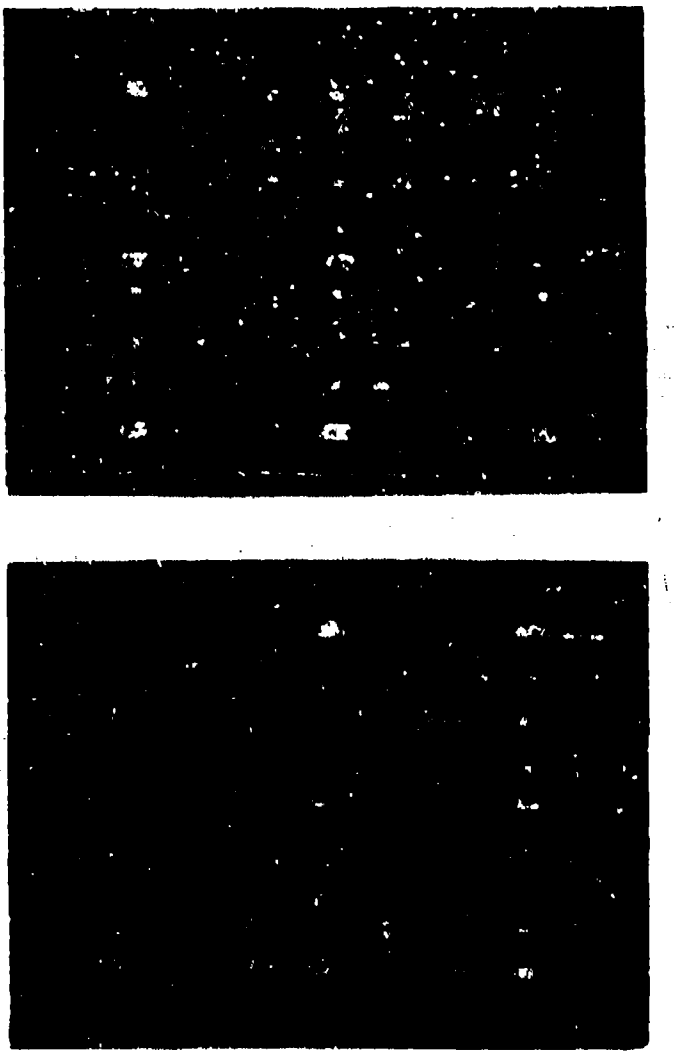
(Aluminum Metallization)

Total Hours on Test	0	21	69	134	302	376	828
Number of Functional Oscillators	30	30	30	30	30	30	30
Total Hours on Test	968	1589	2269	3244	3725	4584	5086
Number of Functional Oscillators	30	30	30	30	30	30	30

The powered Life Test "H" was terminated after 5086 hours at 340° C (a period slightly longer than 7 months). If an acceleration factor of at least 2X can be assumed for a 40° C temperature differential at these temperatures (that is, an activation energy greater than 0.525 eV), then this life test is equivalent to 10,000 hours at 300° C which meets the immediate goal of this development program.

Chip packages were opened at the conclusion of Life Test "H". No changes or observable degradation was found in these chips that had survived for over 5000 hours at 340° C. An unstressed sample from the same packaging lot (but not put on life test) was opened to compare with the life test samples. Figure 4-21 shows this comparison. As seen in the figure, no optical difference can be observed from before to after the life test.

In addition to the powered Life Test "H", an unpowered Life Test "I" was conducted at 360° C inside a diffusion furnace. The packaged chips from Wafer 6 were periodically removed from the furnace and tested at room temperature for correct operation. This life test is still continuing. A final summary will be available in the monthly reports or final report of the current contract phase. The results to date (March 1984) are summarized in Table 4-9.



- The Top Photograph is From a Chip After Packaging
- The Bottom Photograph Shows an Identical Region of a Chip After 5086 Hours at 340° C

Figure 4-21. Ring Oscillator Sections in Aluminum Metallized Chips.

Table 4-9. Wafer 6 Unpowered Life Test at 360° C - Life Test "I".

(Aluminum Metallization)

Total Hours on Test	0	25	71	165	235	401	568	813		
Number of Functional Oscillators	30	30	30	30	30	30	30	30		
Total Hours on Test	1333	1668	2269	3177	3848	4589	5285	5981	6430	6770
Number of Functional Oscillators	30	30	30	30	30	30	30	29	29	29

4.3 ELECTROMIGRATION EVALUATIONS

An early investigation into the acceleration of metallization failures due to electromigration was conducted at 320° C in the same oven as the ring oscillator life test. This test (designated Life Test "J") used five of both the A1 and A2 electromigration test cells which each contain two individual patterns. The patterns in both cells contain 0.25 and 0.3 mil lines which are approximately 14 mils long between the Kelvin probe connections.

The 0.25 mil lines were biased with a current density of 500,000 amp/cm^2. The bias current for the 0.3 mil lines was 100,000 amp/cm^2. The results from Life Test "J" are shown in Table 4-10. However, before discussing the failures, a comment is in order about this experiment. The purpose was to determine if electromigration of the gold metallization could accelerate the assumed thermal migration failure mode that had produced crystals and voids concentrated at the edges of the metallization regions. With the higher current density, the narrower lines could be expected to fail more rapidly than the wider ones. In retrospect, it is unfortunate that the higher current density was applied to the narrower line. Since the times to failure are similar to those obtained in concurrent life tests, the only conclusion that

may be drawn is that the current densities employed do not appear to have accelerated the failures.

Table 4-10. Electromigration Evaluation (320° C) - Life Test "J".

Total Hours on Test	0	28	36	42	164	244	446	640	740	880	1000	1800
Number of Intact Lines												
Al 0.25 Mil	5	5	4	4	3	3	1	0				
Al 03 Mil	5	5	5	5	5	5	5	5	4	3	2	1
A2 0.25 Mil	5	4	4	3	3	3	2	2	2	2	2	2
A2 0.3 Mil	5	5	5	5	5	4	4	4	4	4	4	3

In evaluating a device that failed after 1000 hours at 320° C, portions of the electromigration metallisation lines were found to have a different reflectivity for both optical and SEM observation. This is seen in Figure 4-22 where the top photo is an optical photograph of the device and the bottom photo in the figure is a SEM photograph of the same region. From the discoloration around the failure point, it appears that some other failure mechanism is the cause of the failure. Figure 4-23 shows SEM closeups of two sections on the electromigration line. In one, the familiar hillock/void failure mechanism is observed; while in the other, the previously described failure point is seen. Before jumping to conclusions about new failure modes, remember that these chips were unpassivated and that the packaged devices were not hermetically sealed. More work will be needed to verity the effect of electromigration and to what extent it may become a problem with the Ti-W/Au metallization system.

Other electromigration cells failed from the same hillock and void mode which was responsible for the ring oscillator life test failures. As seen in Figures 4-24 and 4-25, voiding across the 0.25 metal line caused this failure after 470 hours at 320° C.

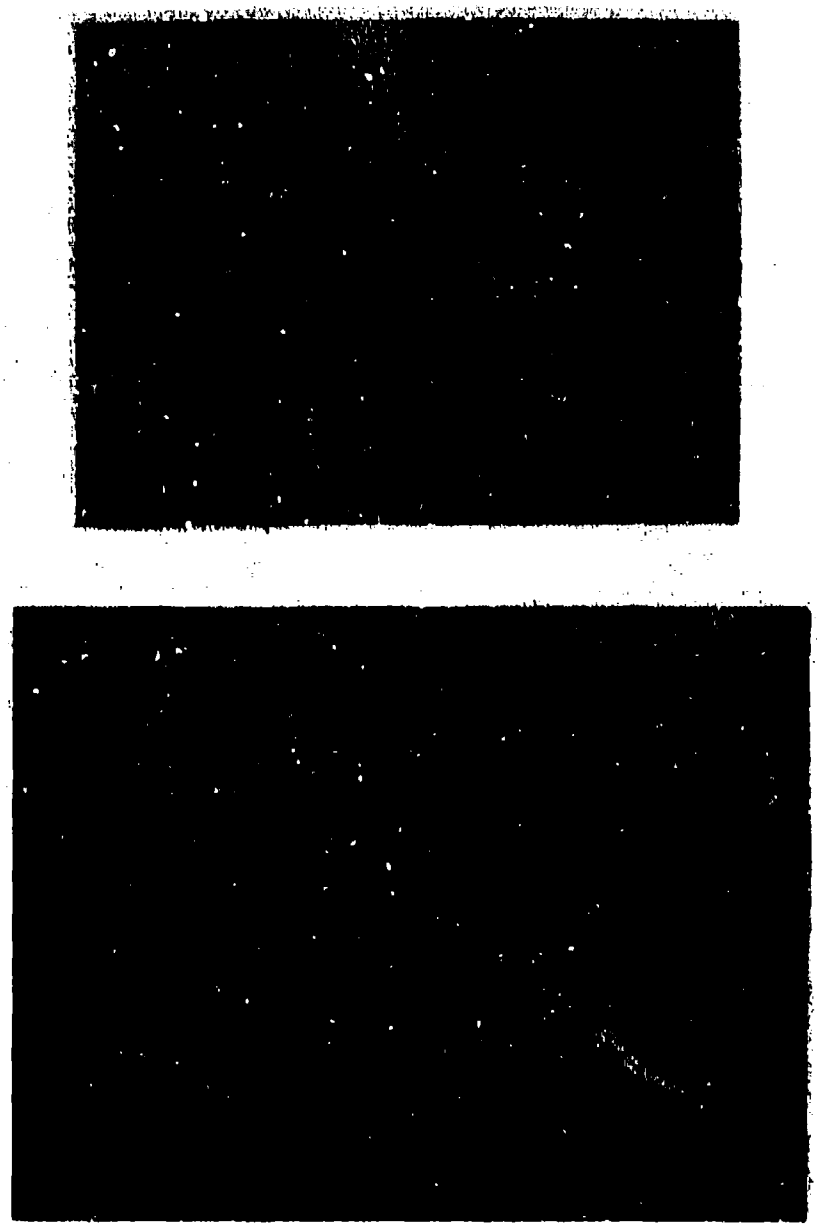


Figure 4-22. Failed Device From the Electromigration Test After 1000 Hours at 320° C.

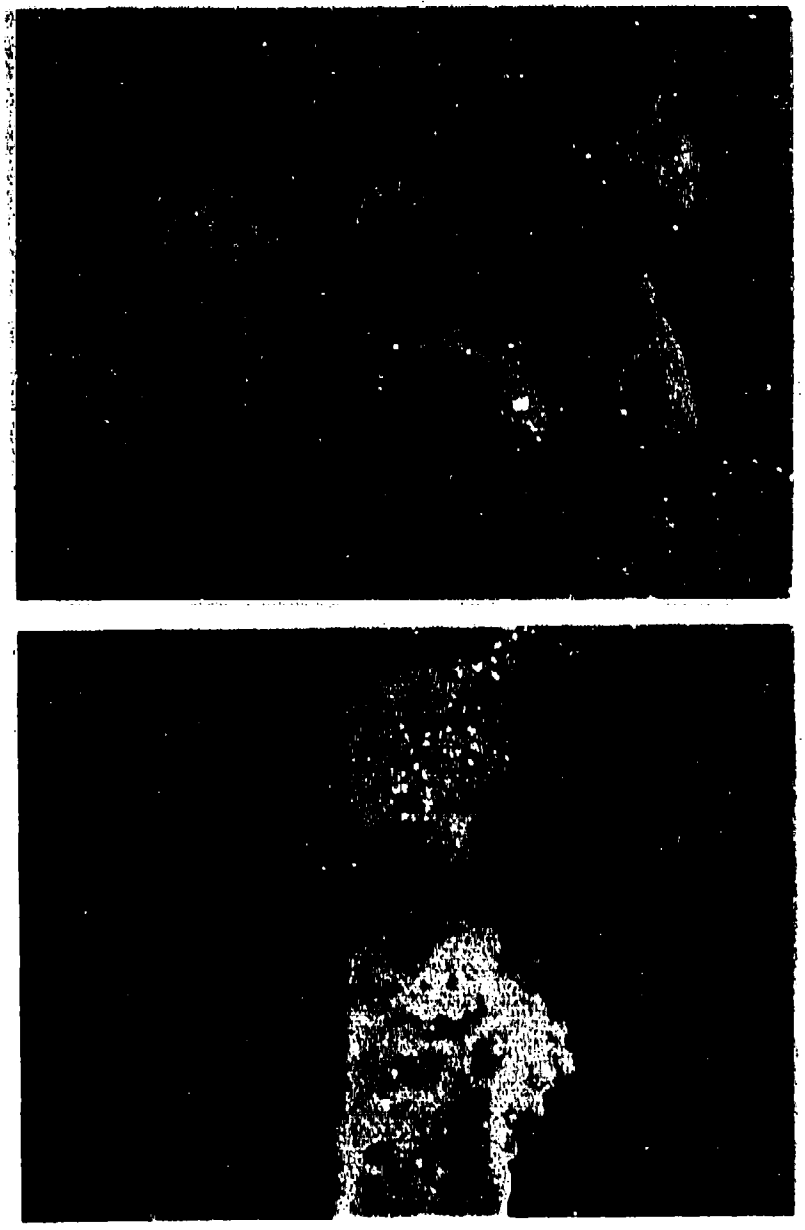


Figure 4-23. SEM Closeup of Electromigration Cell Shown in Previous Figure.

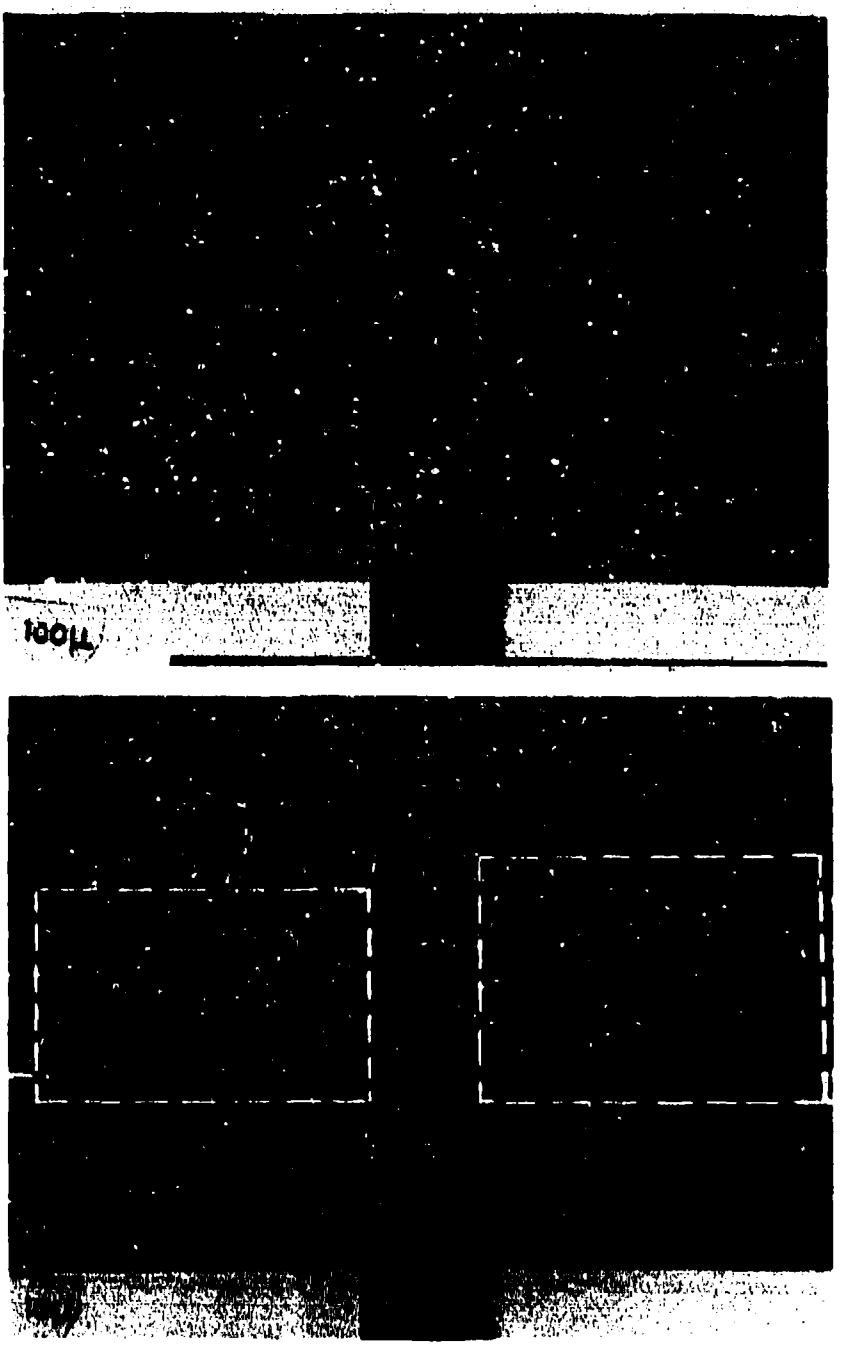


Figure 4-24. SEM Evaluation of a 0.25 Mil Electromigration Cell That Failed After 470 Hours at 320° C.

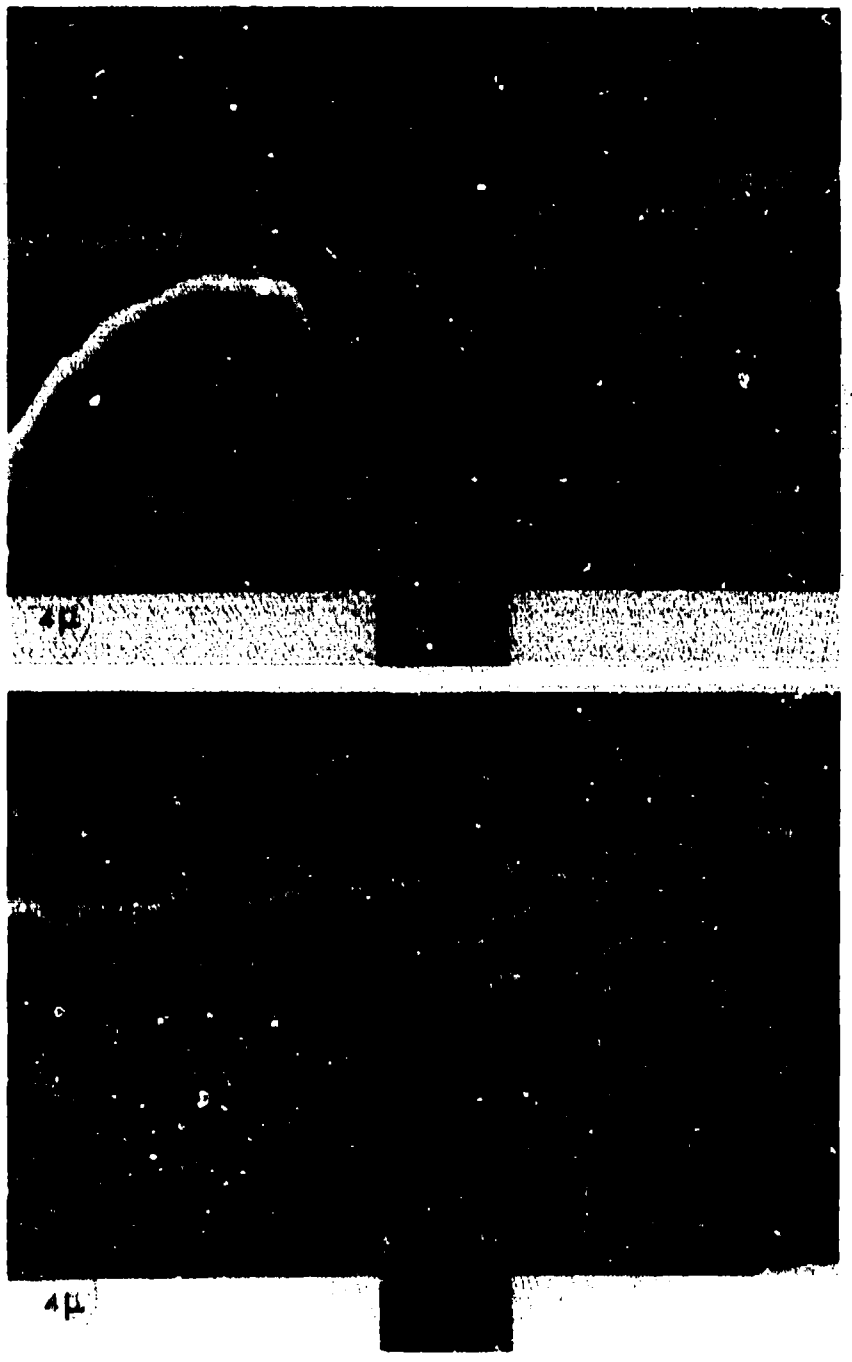


Figure 4-25. SEM Closeup of Cell Shown in Previous Figure.

4.4 PASSIVATION EXPERIMENTS

Many of the chip metallizations employed in the previously described high temperature stress tests were unpassivated. In the cases where the metallization was unpassivated, failures were due to open circuits resulting from thermally induced self-diffusion in the gold layer. A preliminary experiment aimed at controlling this thermally induced self-diffusion was conducted using the application of a passivation layer. Three different passivation approaches were independently employed:

1. 7000 A of sputtered SiO_2
2. 7000 A of plasma deposited silicon nitride Si_3N_4
3. 7000 A of Silox.

These layers were applied to complete patterned wafer sections from the same processing run that supplied the chips for the electromigration life test. The wafers were then annealed for 220 hours at 360° C in a diffusion furnace. A sample unpassivated wafer section was annealed for 122 hours in the same furnance as a control.

The SEM analysis of the annealed samples is shown in Figures 4-26, 4-27, 4-28, and 4-29. The annealing times and temperatures are comparable to those needed to produce failures in the life-tested devices. Figure 4-26 shows the control, an unpassivated sample that was annealed for 122 hours. Figure 4-27 shows the improvements obtained by sputtering 7000 A of SiO_2 on top of the metallization. Gold crystal formations are observed at the edges of the metal interconnect lines, probably due to cracking in the passivation in this high stress region. The plasma deposited silicon nitride sample shown in Figure 4-28 survived the anneal with few metallization changes. However, the silicon nitride did not adhere to the gold and, as a result, cracked and flaked off from the larger metal expanses in the electromigration test cells. The silox overglass results are shown in Figure 4-29. The silox bridged the I^2L metallization and produced favorable results similar to those outlined with plasma nitride. However, adhesion problems were also observed with the silox passivated samples where cracking in the bonding pad regions was observed. Gold crystal formation was observed as seen in the bottom photograph in Figure 4-29, growing up through these cracks.

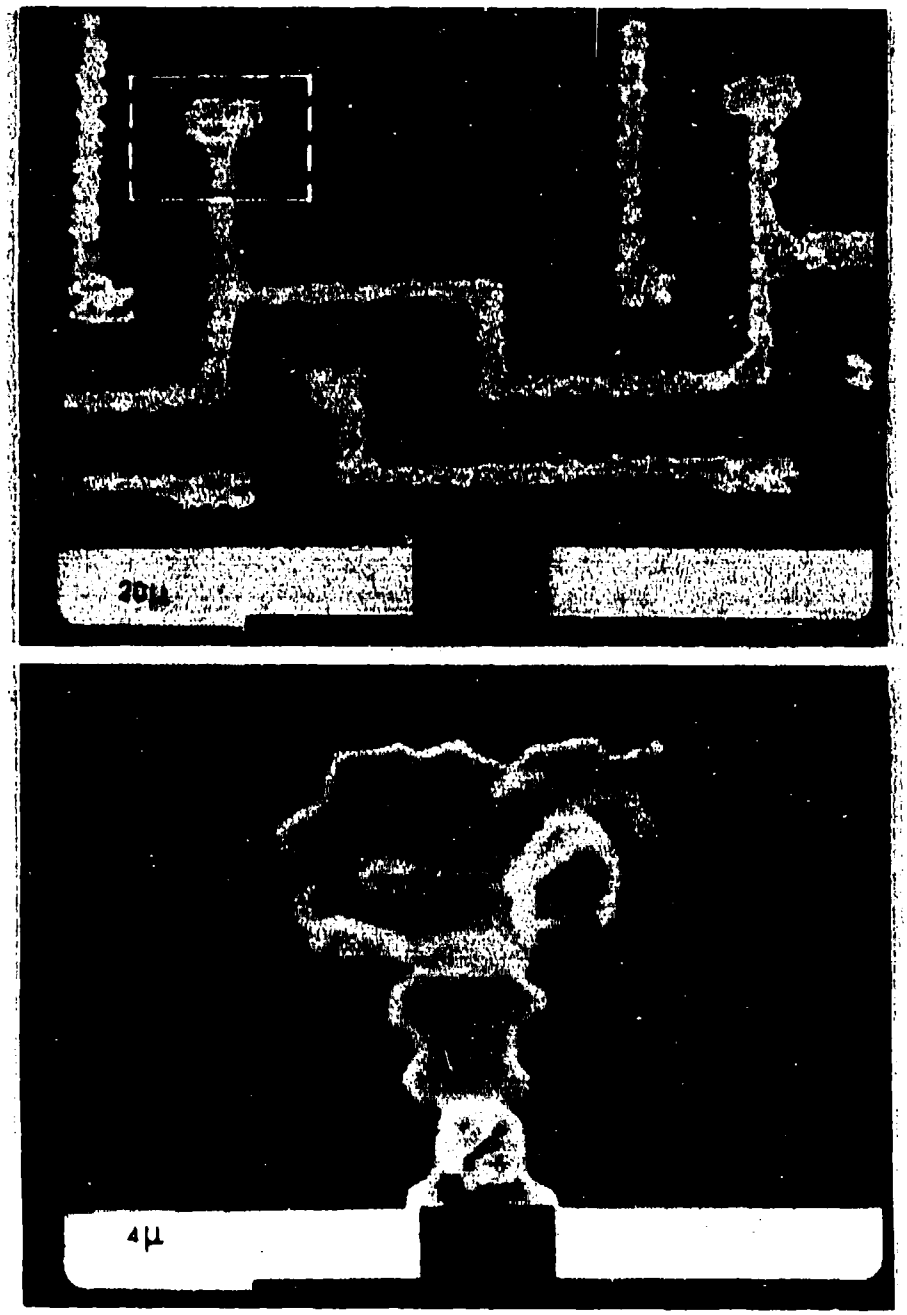


Figure 4-26. Unpassivated Gold Barrier Metallization Annealed 122 Hours at 360° C (Used as Experiment Control).

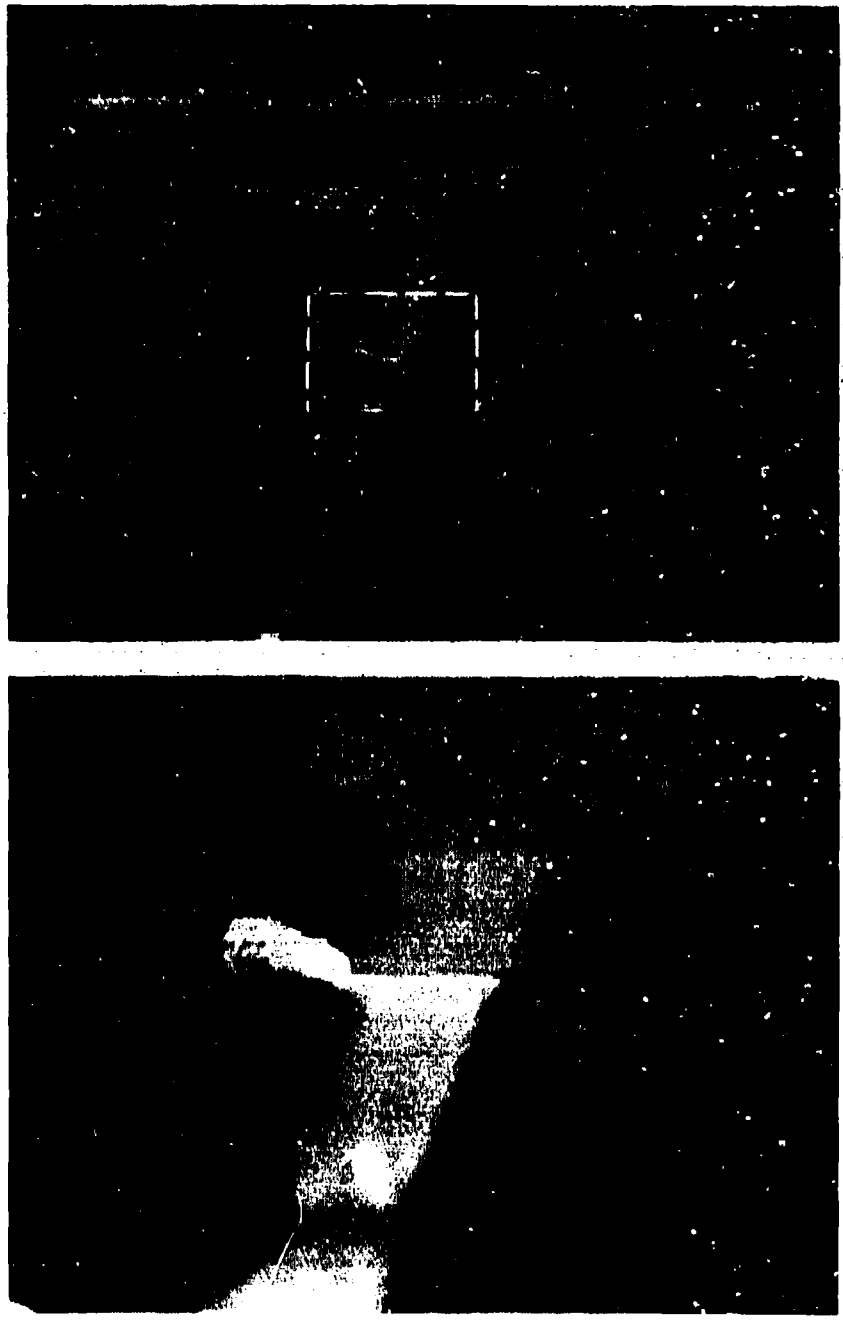


Figure 4-27. Barrier Metal System With 7000 A of Sputtered SiO_2 After Annealing 220 Hours at 360° C.

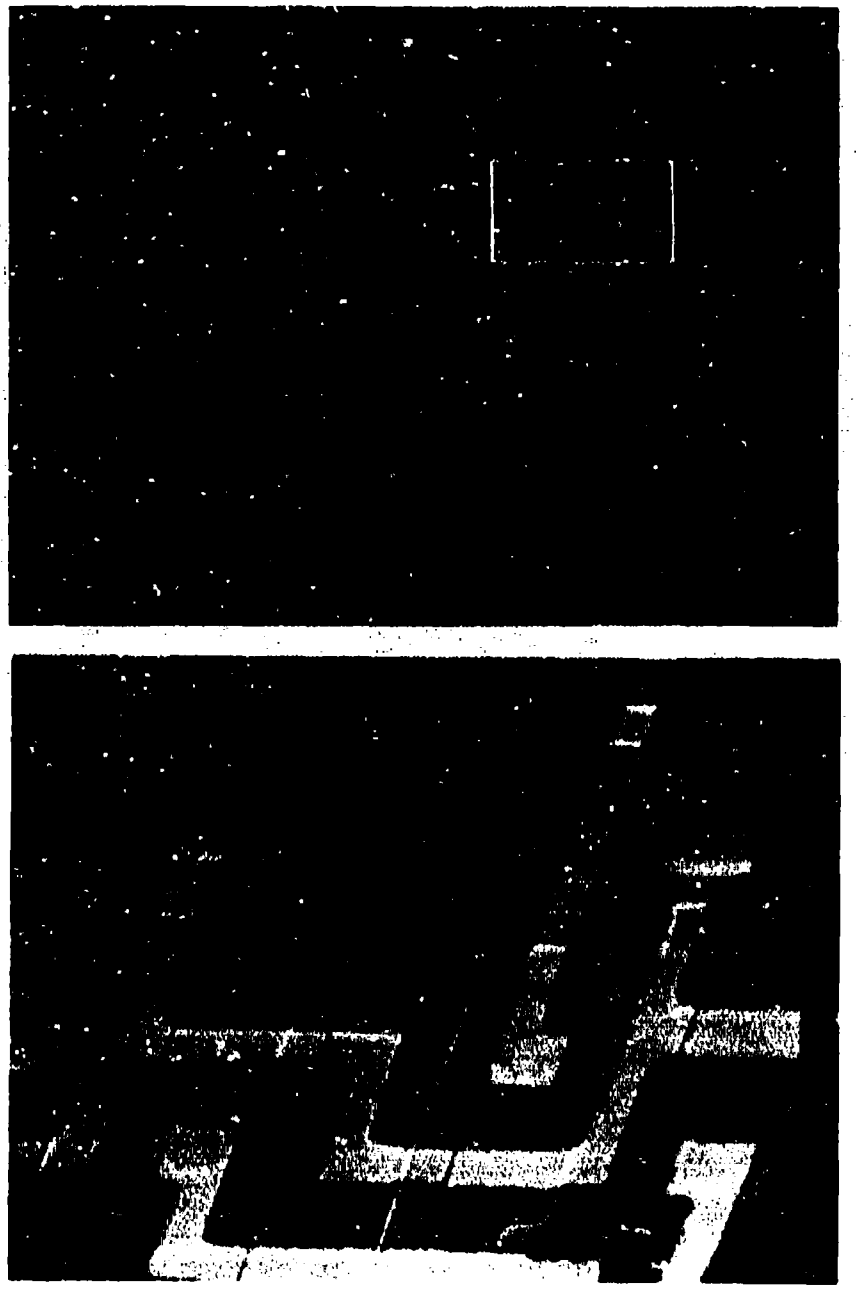


Figure 4-28. Barrier Metal System With 7000 A of Plasma Nitride (Si_3N_4) After Annealing 220 Hours at 360° C.

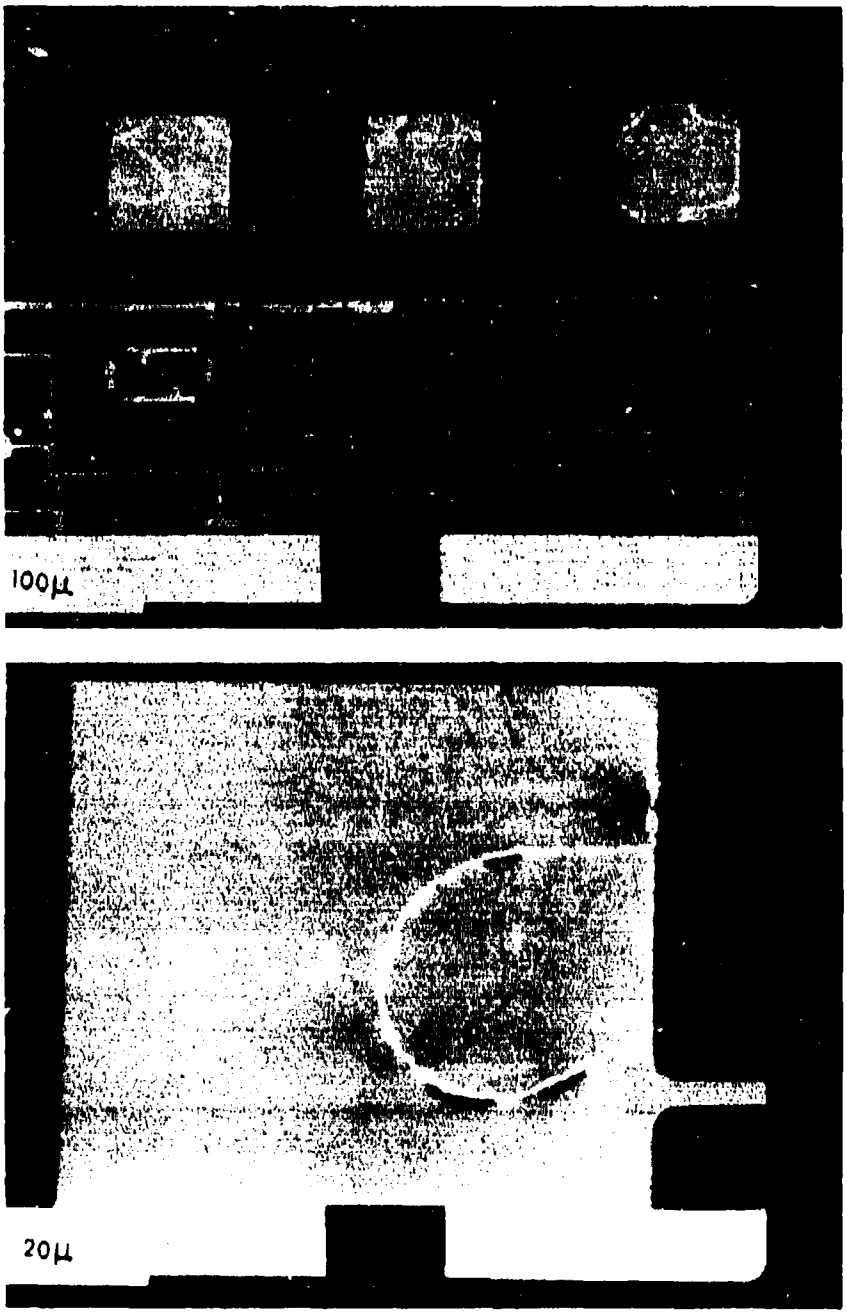


Figure 4-29. Barrier Metal System With 7000 A of Silox After Annealing 220 Hours at 360° C.

The passivation samples were returned to the furnace for an additional 289 hours at 360° C. The samples were removed and both optical and scanning electron microscope observations made. It should be noted that the unpassivated sample had accumulated 411 hours total at 360° C while the three passivated samples had been annealed for 509 hours at 360° C. In addition, the samples were beginning to accumulate surface contamination (dirt) and mechanical damage (scratches in the unpassivated metallization) due to the large amount of handling.

Figure 4-30 shows the unpassivated I^2L ring oscillators after 411 hours at 360° C. In the bonding pad regions (4 by 5 mils), it can be seen that the bulk of the hillock and crystal growth is confined to the periphery of the metallization area (Figure 4-31). Figure 4-32 shows a SEM closeup of the metal lines on the ring oscillator test circuits. These circuits would have failed in a life test due to breaks in the metallization as can be seen in the lower photo. A bonding pad on one chip (Figure 4-33) had sustained some mechanical damage (scratches) probably from handling during the previous inspection after the initial 122-hour anneal. During the subsequent anneal (289 hours at 360° C), crystal formation had proceeded preferentially along the scratches in the top gold layer.

All the passivated samples survived the anneal (509 hours at 360° C) with fewer radical changes than experienced with the unpassivated sample. In general, the passivation did not adhere well to the gold metallization but this was not entirely unexpected since no adhesion promoting layers were included in the metallization. Figure 4-34 shows an I^2L section on the wafer sample with 7000 A of silox passivation. The crystal growth observed in the unpassivated sample (Figures 4-30and 4-31) is absent but the passivation was cracked where it covers the bonding pad regions. SEM closeups (Figure 4-35) show the gold top metal layer extruding up through a crack in the passivation over a bonding pad (top) and over an I^2L injector contact (bottom). The passivation over the I^2L injector contact appeared to separate at the substrate step allowing the gold to squeeze out through the crack.

Figure 4-36 shows an I^2L section of the sample that was passivated using 7000 A of sputtered SiO_2. The gold crystal formations at the edges of the

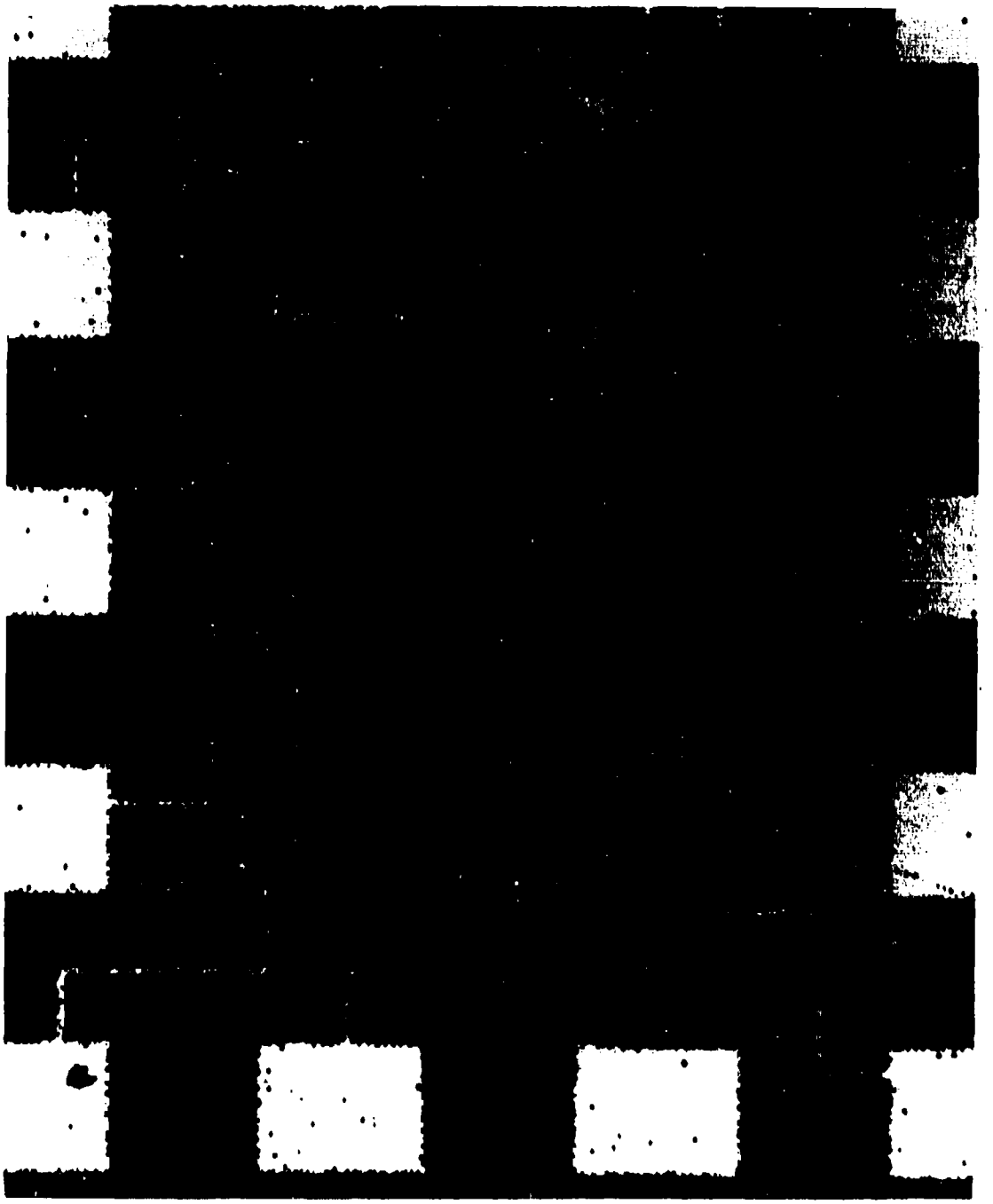


Figure 4-30. Unpassivated Sample After 411 Hours at 360° C.

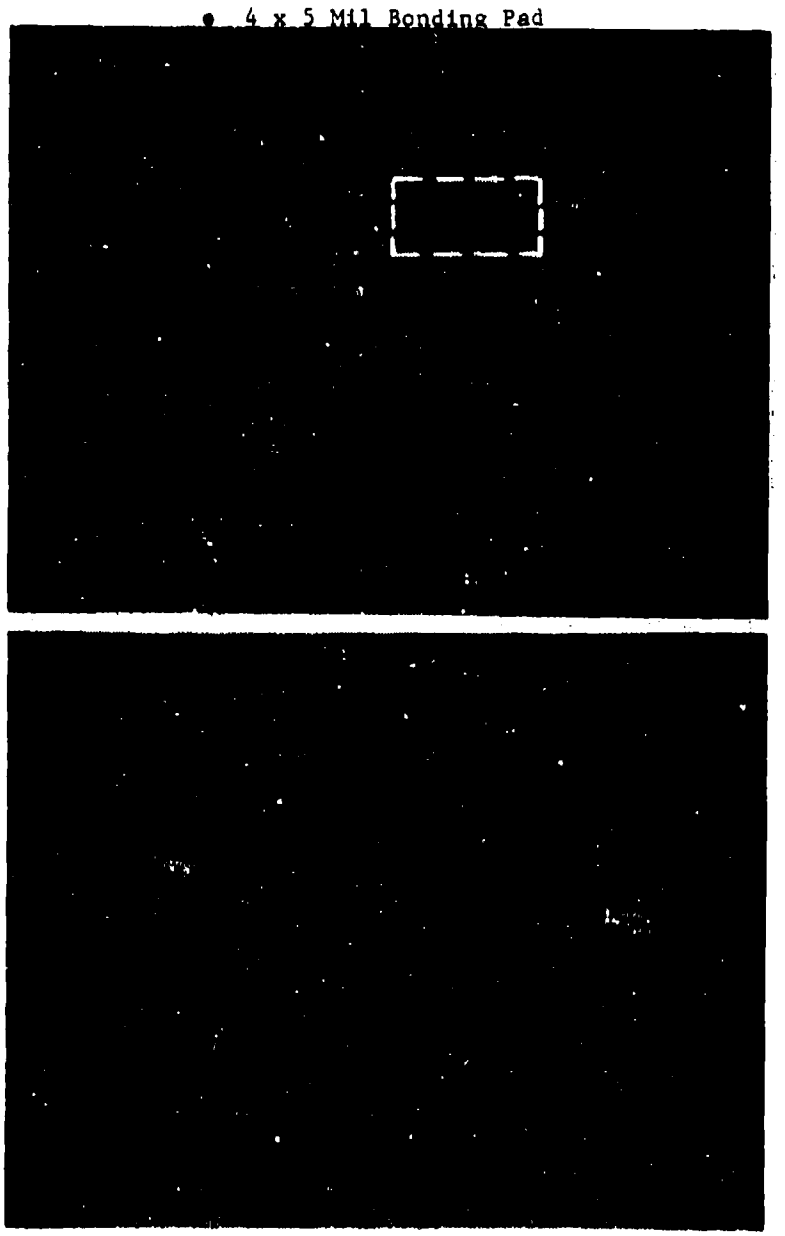


Figure 4-31. Bonding Pad Region of the Unpassivated Sample Showing the Accumulation of Crystal Growth at the Periphery (Top) and a Closeup of Two Crystals Found in the Pad Interior (Bottom).

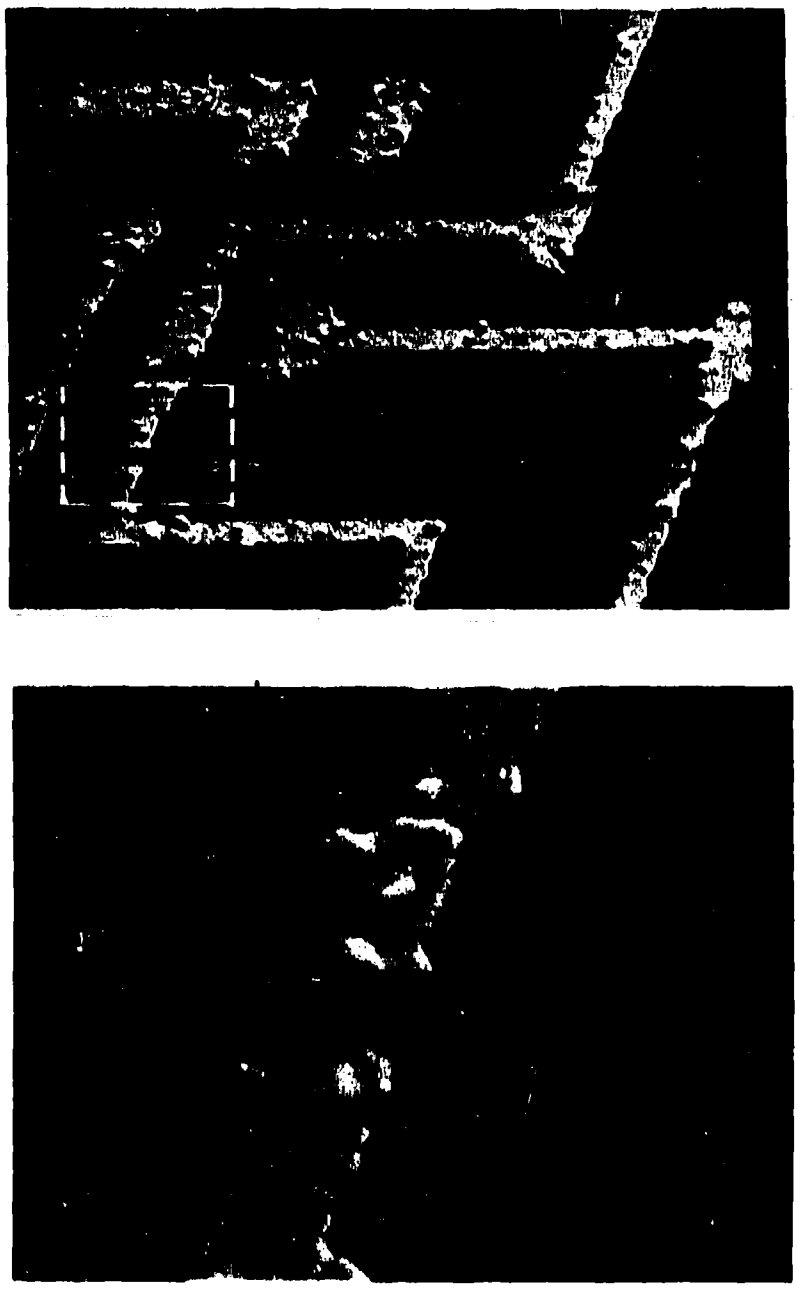


Figure 4-32. SEM Closeup of Unpassivated Ring Oscillator Barrier Metal After 411 Hours at 360° C.

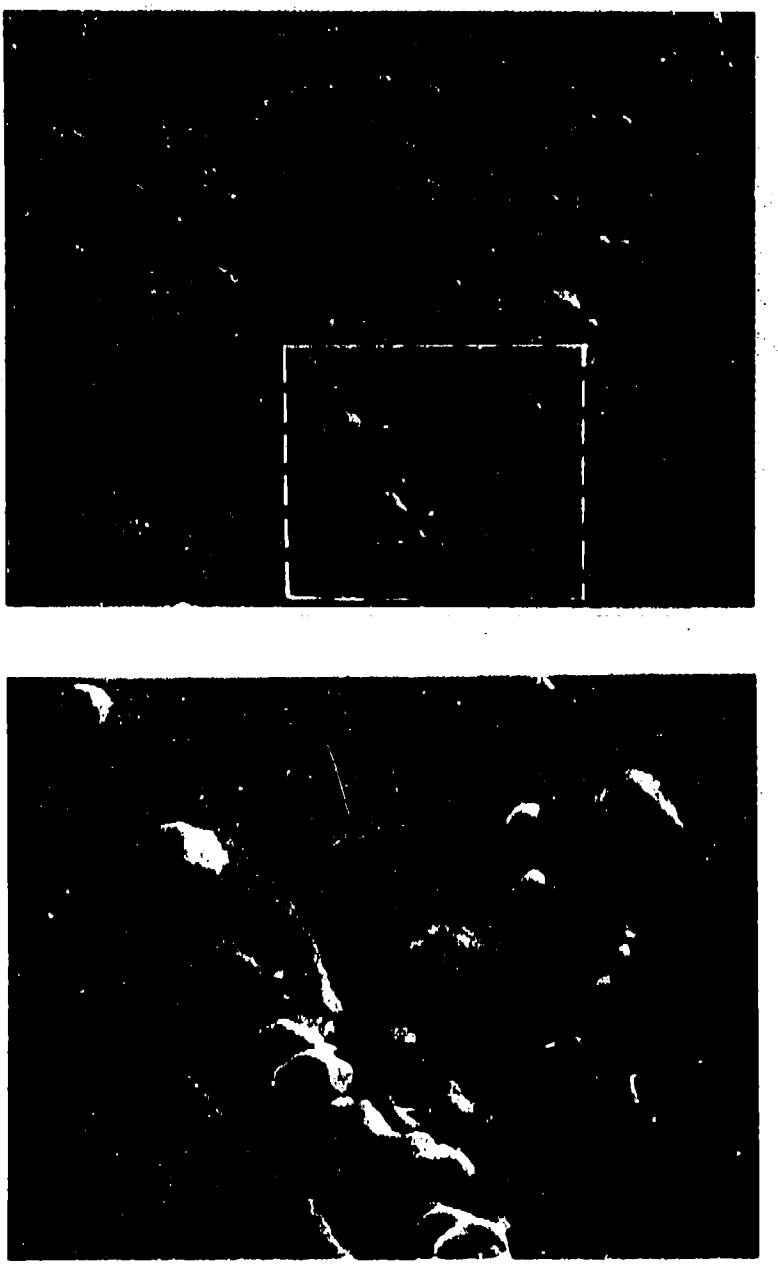


Figure 4-33. Damaged Bonding Pad Region Showing Preferential Crystal Formation Along Scratches in the Top Gold Layer.

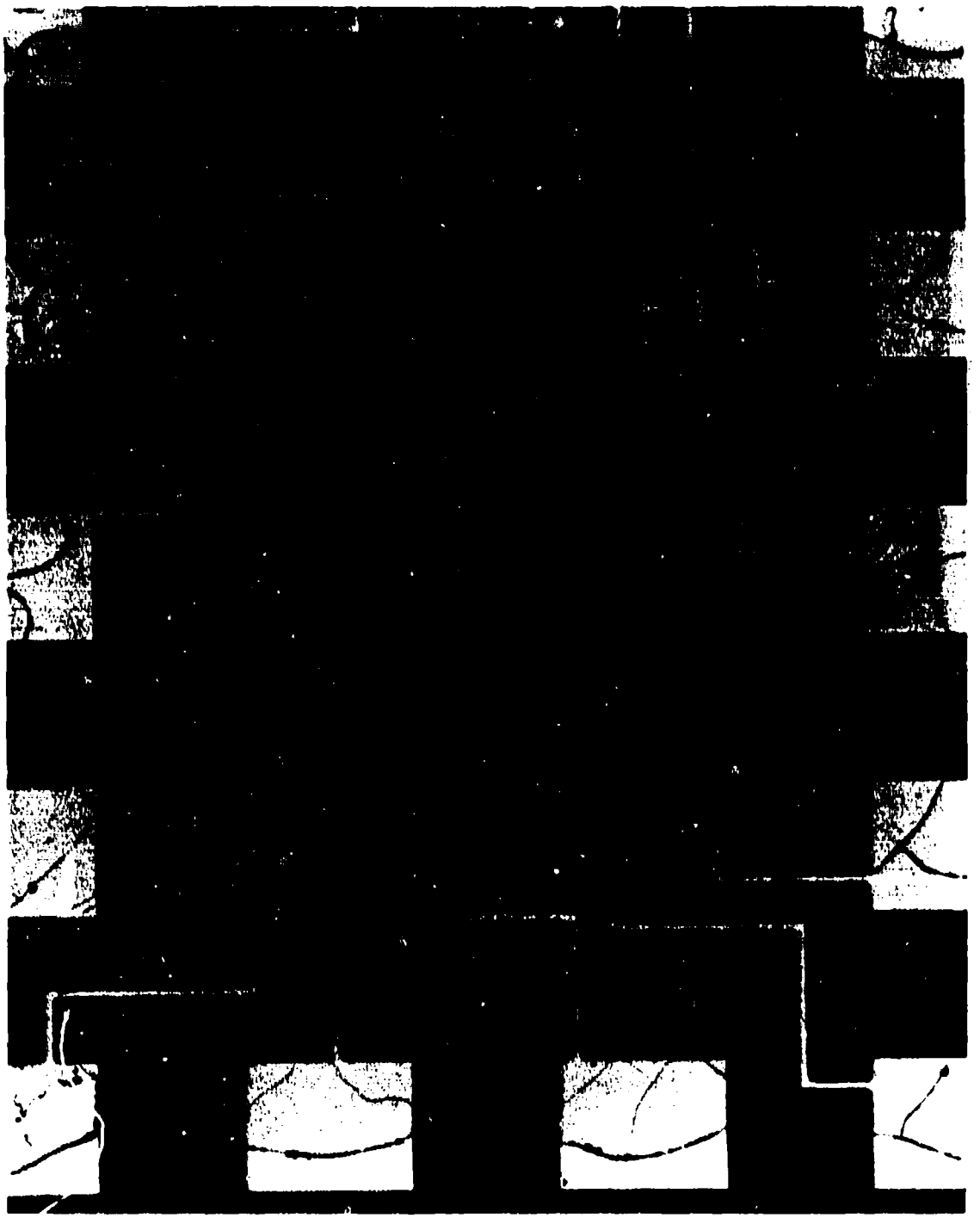
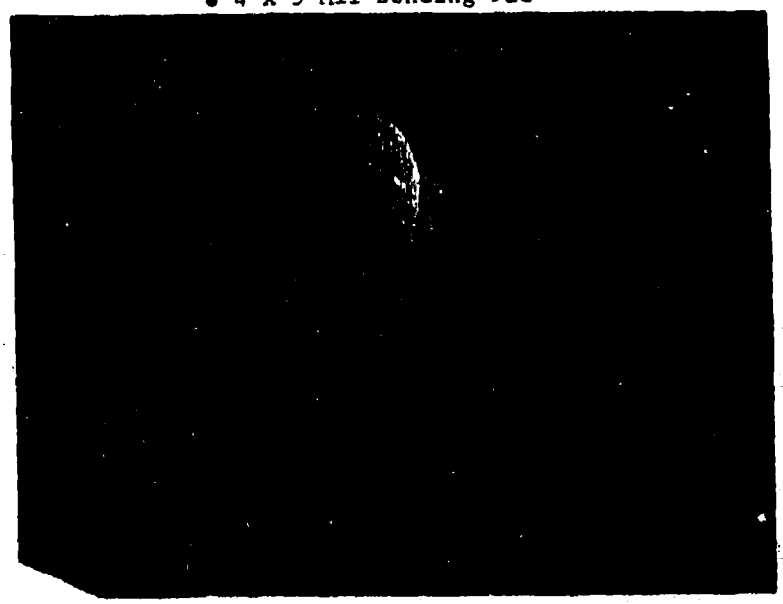


Figure 4-34. Silox Passivated Sample After 509 Hours at 360° C.

• 4 x 5 Mil Bonding Pad



• 7.5 Micron Interconnect Lines

Figure 4-35. Cracking of Silox Passivation With Gold Extruding Through the Cracks.

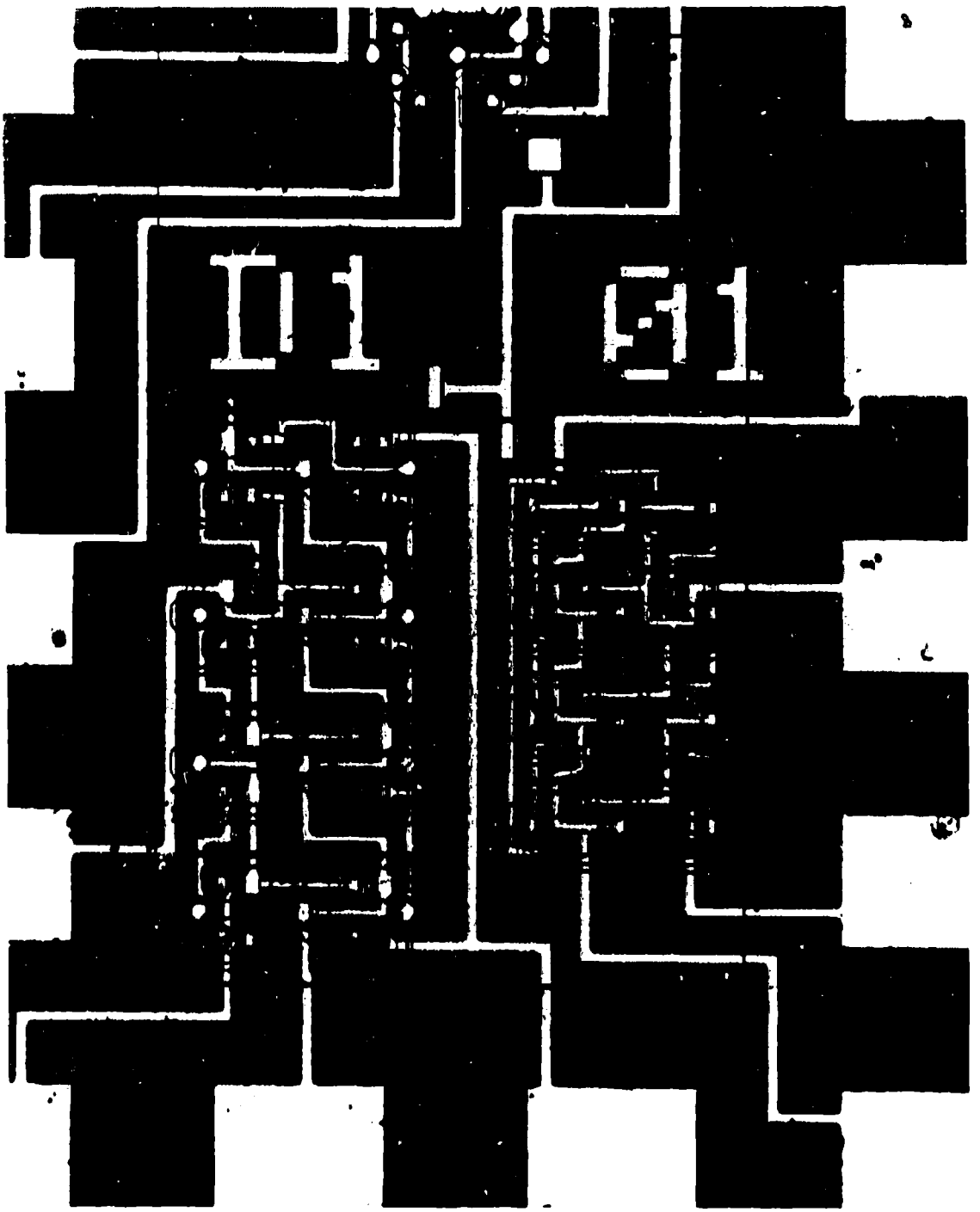


Figure 4-36. Sputtered SiO_2 Passivated Sample After Annealing 509 Hours at 360° C.

barrier metal interconnect lines are more prominent after 509 hours at 360° C. Figure 4-37 shows SEM closeups of the metallization on a ring oscillator (top) and two parallel lines on the electromigration test cell (bottom). The gold crystals apparently form through step coverage defects where the sputtered passivation does not completely cover the edges of the metallization lines.

The plasma nitride passivated sample is shown in Figure 4-38. The silicon nitride did not adhere to the gold at all but tended to bridge the gold regions from the chip field oxide. As can be seen in the figure, the passivation flaked off from numerous bonding pad regions, and in other regions it is raised above the gold metal surfaces so that optical interference patterns are visible (bottom three pads on the right side). SEM observation of the metallization on this sample provides substantial encouragement that the crystallization problem may be solved. Figure 4-39 shows a bonding pad where the passivation has flaked off. Note that no crystal formations are observed around the periphery as were seen with the unpassivated sample (Figure 4-31). This observation is typical of the metallization on this sample and many other pads that have been uncovered for at least 289 hours at 360° C.

Based on the results seen in this preliminary study, silicon nitride was chosen as the prime candidate for a passivation material. An investigation of plasma deposited silicon nitride processing revealed several variables that had to be controlled to produce a satisfactory passivation film. The keys to success were the production of a dense, slightly compressive film, deposited at a temperature less than 350° C and the addition of a Ti-W adhesion promoting layer on top of the gold.

The compressive or tensile properties of the passivation were controllable by variation of process parameters during deposition. Concurrently with the development of the plasma nitride passivation layer, a decision was made to expand the metal system into a dual level capability. Thus a passivation (dielectric) thickness of 5000 A was chosen for all further studies.

Some of the initial silicon nitride results are shown in Figure 4-40. The film in this figure was deposited with a large tensile stress. Initially, the surface appeared unblemished, but, after annealing for 471 hours at 350° C, the passivation cracked and lifted from the metallization and wafer surface.

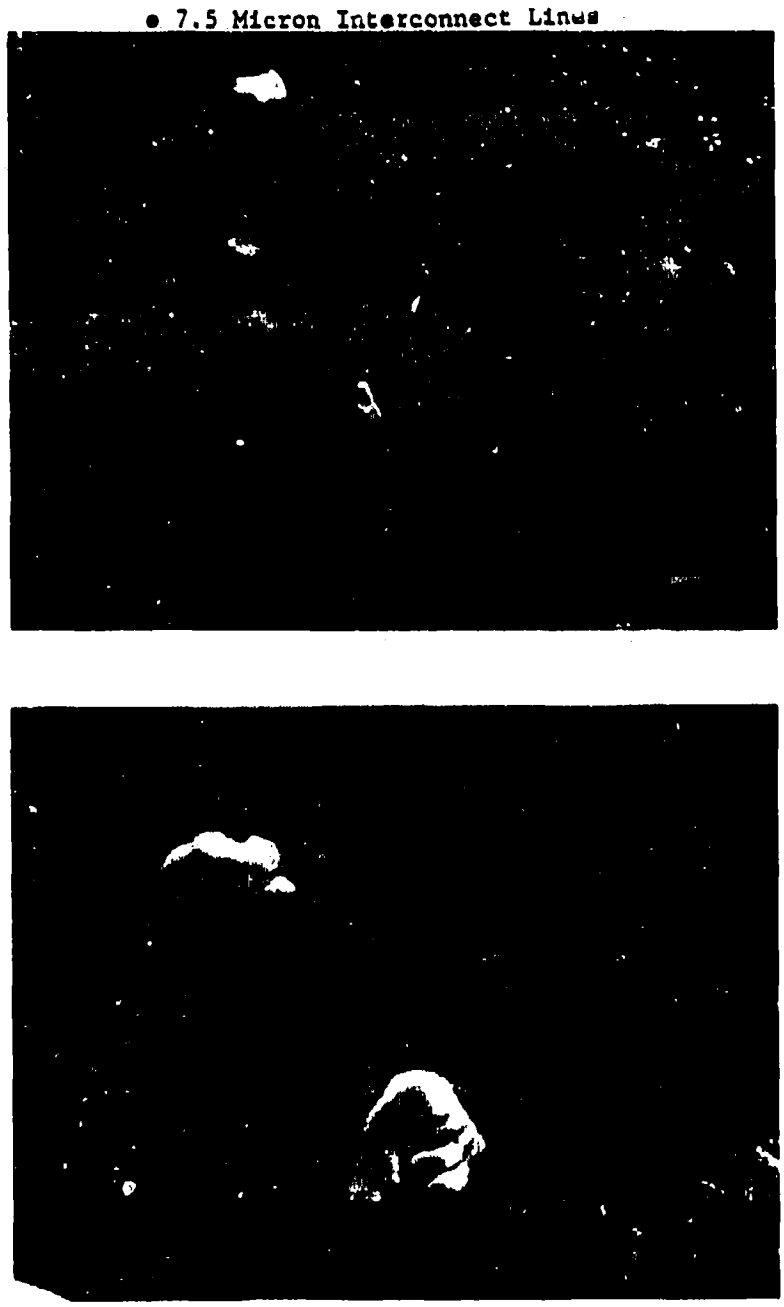


Figure 4-37. Gold Crystal Formation at Edges of Barrier Metal With Sputtered SiO_2 Passivation.

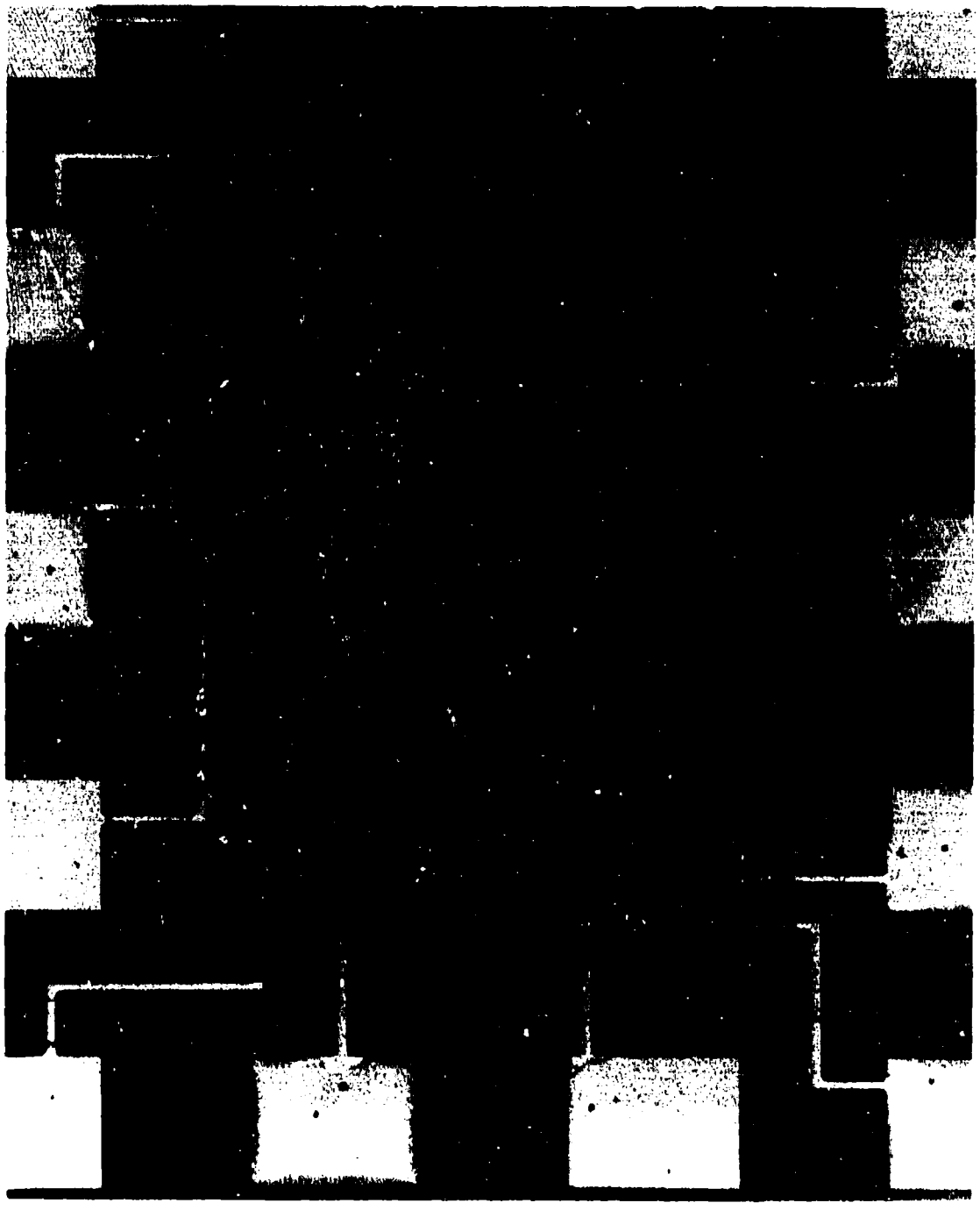


Figure 4-38. Plasma Nitride Passivated Sample After Annealing 509 Hours at 360° C.

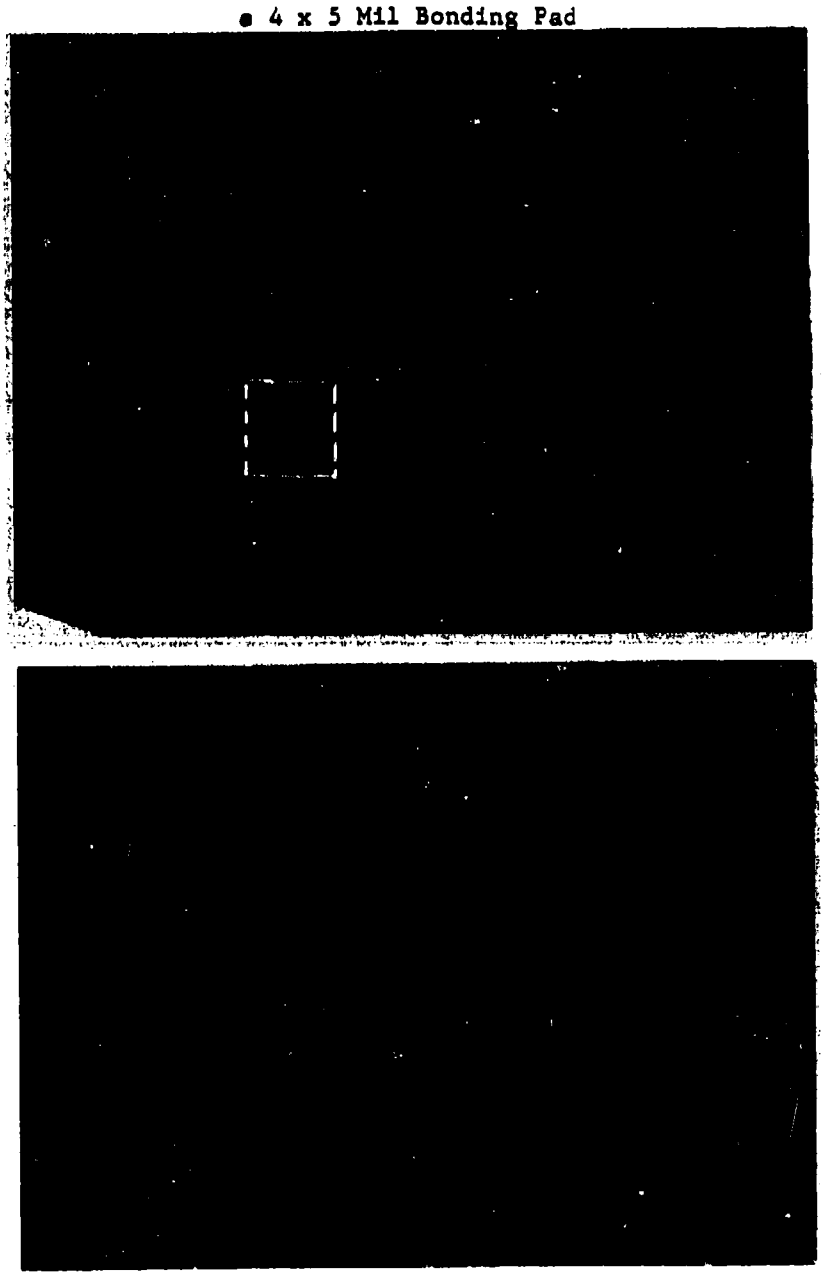
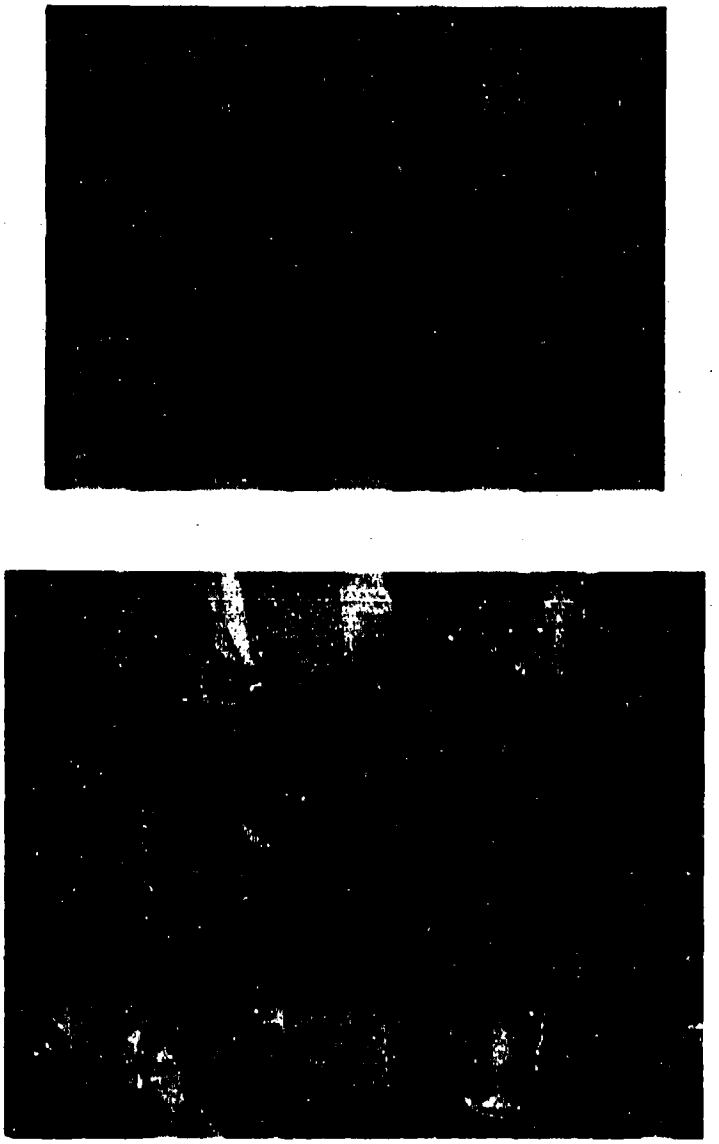


Figure 4-39. SEM Observation of Bonding Pad in Plasma Nitride Passivated Sample (Top) and Closeup of Gold Crystals in Pad Interior (Bottom).



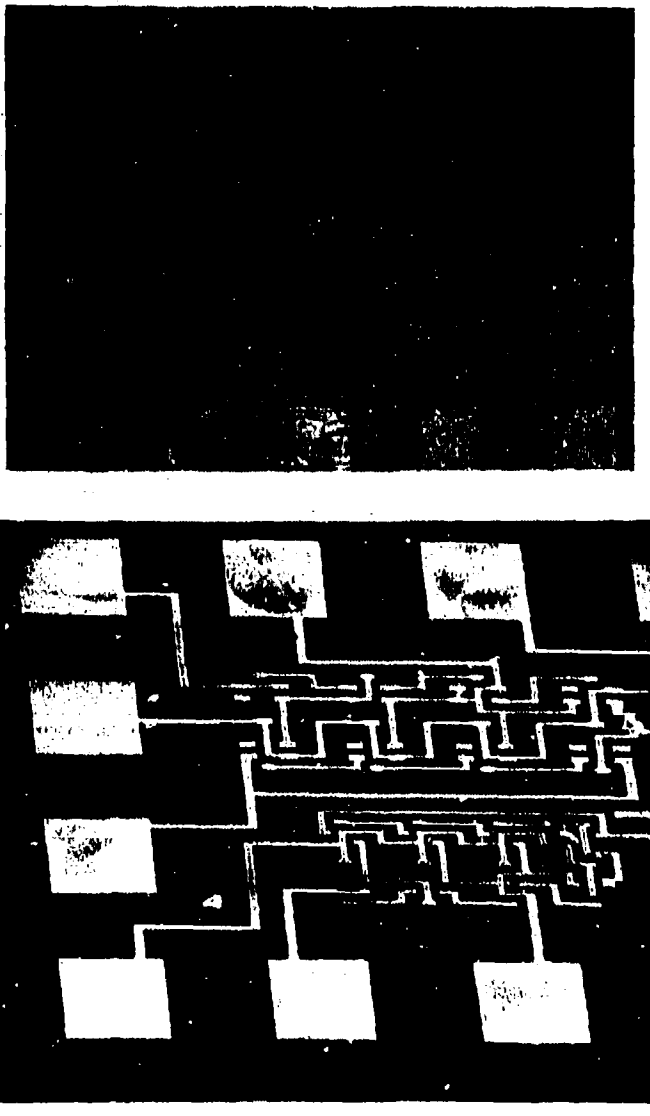
• The Samples Were Annealed For 471 Hours at 350° C.

Figure 4-40. Optical and SEM Photographs of a Highly Tensile Plasma Nitride Passivation Deposited on Gold Metallized Samples Without a Top Ti-W Layer.

Another trial, shown in Figure 4-41, had a slight tensile stress in the as-deposited film. After annealing 471 hours at 350° C, the nitride only cracked over the chip bonding pads.

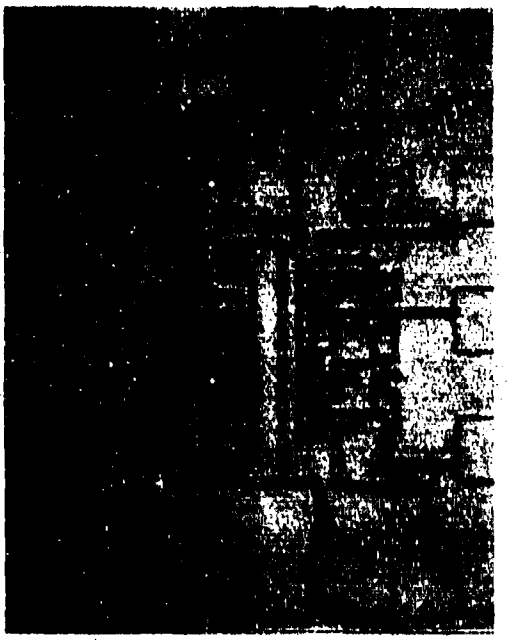
The addition of a 500 A top Ti-W layer to the gold film improved the passivation adhesion to the metal system. Figure 4-42 illustrates the results of an annealing experiment with this system where the samples were stored at 350° C for 273 hours. No cracks or passivation peeling were visible after this test but microcracks were observed in other samples after longer periods.

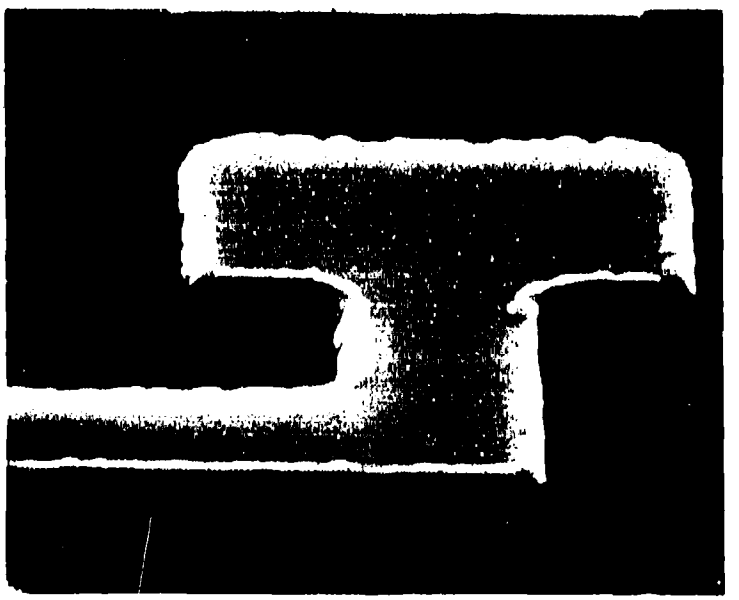
The deposition of a silicon nitride layer with a slightly compressive stress apparently solved the passivation adhesion problem. A sample with this passivation deposited over a test metallization structure is shown in Figure 4-43. The metallization had a 500 A Ti-W layer on top of the gold for adhesion purposes. This photograph was taken after the sample had accumulated 824 hours at 360° C. No cracks or signs of passivation lifting were observed in this sample.



• The Samples Were Annealed for 471 Hours at 350° C.

Figure 4-41. Optical and SEM Photographs of a Slightly Tensile Plasma Nitride Passivation Deposited on Gold Metallized Samples Without a Top Ti-W Layer.





• The Samples Were Annealed for 273 Hours at 350° C (7.5 Micron Interconnect Line)

Figure 4-42. Optical and SEM Photographs of a Slightly Tensile Plasma Nitride Passivation Deposited on Gold Metallized Samples With a Top Ti-W Layer.

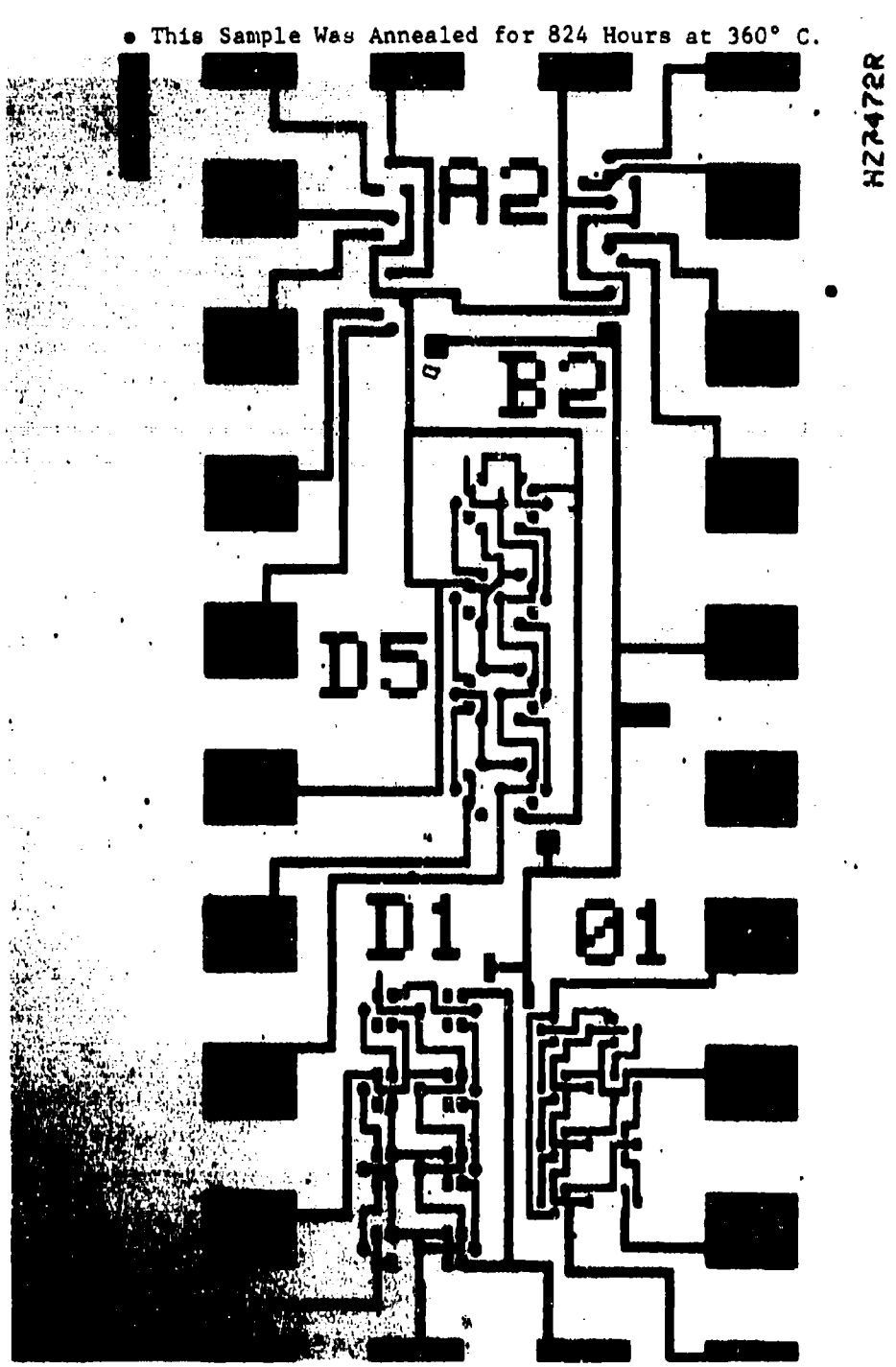


Figure 4-43. Optical Photograph of the High Temperature Gold Metallization With a Top Ti-W Layer and Compressive Stressed Plasma Nitride Passivation.

5.0 LOGIC GATE DESIGN ANALYSIS

Earlier studies (Reference 10) using the General Electric Integrated Injection Logic computer model indicated that specific doping level changes could have a first order effect on the high temperature performance. The model was employed to predict the improvements that could be obtained from these specific doping level changes. A double diffused, junction isolated, bipolar process was used as the basis for this modeling work. As a result, processing objectives were obtained which should improve the high temperature performance. This section of the report summarizes the related analytical efforts which were accomplished during the program.

The standard I^2L model was supplemented to account for second order effects such as the addition of base width modulations due to junction depletion regions and the addition of gate fan-in effects. Another change allowed the model to internally compute doping levels and junction depths based on input data and processing information. This provided more realistic simulations on devices and on process variations that can be physically fabricated. The third type of improvement was cosmetic and resulted from transferring the model to a VAX. Since the VAX line printer has graphics capabilities, the entire modeling process was automated, including the plotting of the final curves.

The initial modeling, shown in Figure 5-1, confirmed experimental evidence that the high temperature effective gain rolloff point increases with increasing injection current. However, it was found experimentally that the I^2L gates had a decreasing range of injection current over which they operated as ambient temperatures were increased. The lower limit for injection current, for which the gate still operates, occurs when the total leakage current in all of the collectors tied to a gate input (NPN base) rob that gate of its injection current. The upper limit for a gate's injection current range for which the gate still operates is related to the effects of high current densities in semiconductors. Resistive effects lead to emitter crowding plus the normal decrease in beta associated with high base currents. The model makes no pretense in accounting for resistance effects (they could possibly be added) since geometrical descriptions of the gate would then have to be

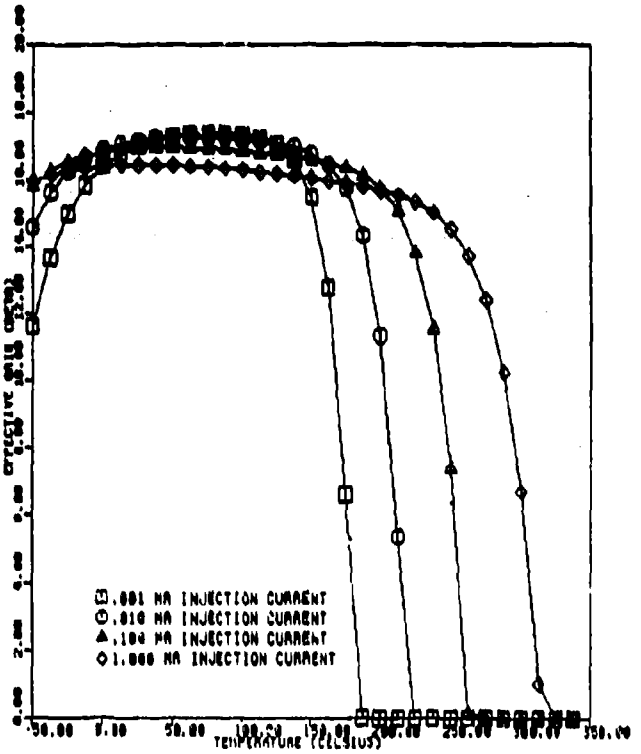


Figure 5-1. Effect of Injection Current on the Maximum Temperature for Integrated Injection Logic Circuit Operation.

included. At present, only the lower threshold point in the injection current range is predicted by the model.

The standard process I^2L (thicker epi) was modeled with variations in the NPN base doping. The doping levels were adjusted by changing the base surface deposition (the number of dopant atoms deposited on the surface per square centimeter before diffusion). Figure 5-2 shows the effect of varying the base deposition where the epi thickness after processing is held at 5 microns to prevent the base region from diffusing into the buried island (or substrate). A subsequent data fitting to a published base profile indicated that during normal production, chips had been processed with a base deposition of 5.6×10^{14} atoms/cm^2 on a reasonably thick epitaxial layer. Experimental measurements on ring oscillators, that were fabricated using a similar production process, showed a temperature limit of about 250° C at 50 microamperes injection current. Figure 5-2 (modeled using a 100 microampere injection current) shows that at the experimental base deposition, the gain drops below unity at slightly below the 250° C point.

Having produced the previous calibration point, the epi thickness was set to 2.5 microns in the model and the base deposition varied again. The effect was to vary the final doping in the intrinsic NPN base emitter junction region. In Figure 5-3, the top curve shows the effective gain with a light base deposition of 5.0×10^{13} atoms/cm^2. In this curve, the base only penetrates 2.1 microns into the epi. In the second curve with 1.0×10^{14} base deposition, the base diffuses almost completely through the epi layer. The other curves show the effect of pushing the base regions down into the buried layer (substrate). In essence, the effective gain rolloff temperature is increased with increasing base doping. Figure 5-4 if a continuation of this modeling experiment with even larger base depositions. The problem with fabricating devices with these parameters is that the intrinsic base doping and base-emitter junction depth in the final device are determined by where on the base doping profile the base doping concentration matches that of the substrate doping. Thus the base emitter junction is referenced to the substrate while the base collector junction, having been diffused last, is referenced strongly to the chip surface. As a result, epi thickness variations translate almost directly into NPN base width variations.

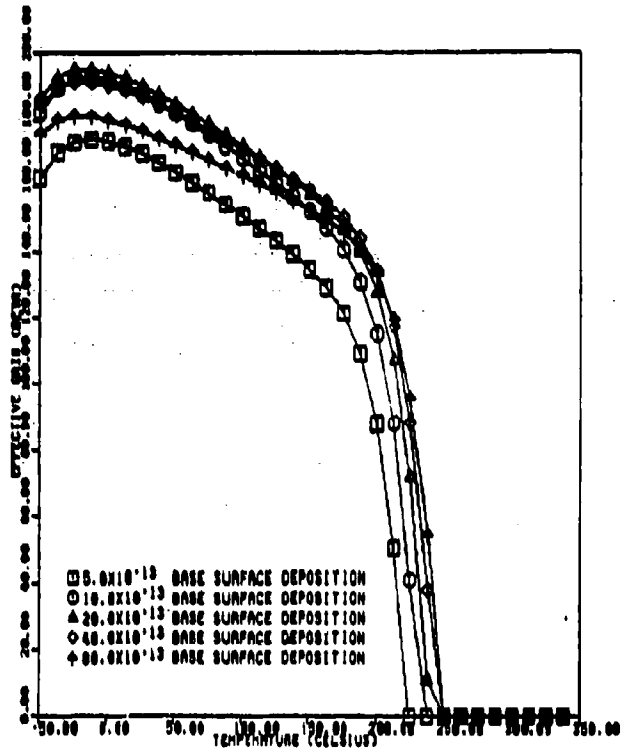


Figure 5-2. Effect of Base Doping on I^2L Operating Margin with a 5 Micron Thick Epi Layer.

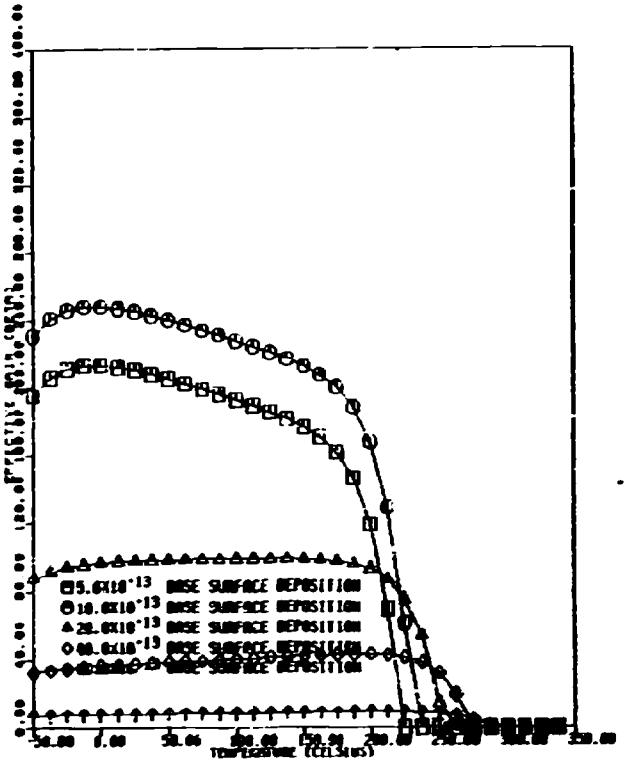


Figure 5-3. Effect of Base Doping on Operating Margin With a 2.5 Micron Thick Epi Layer.

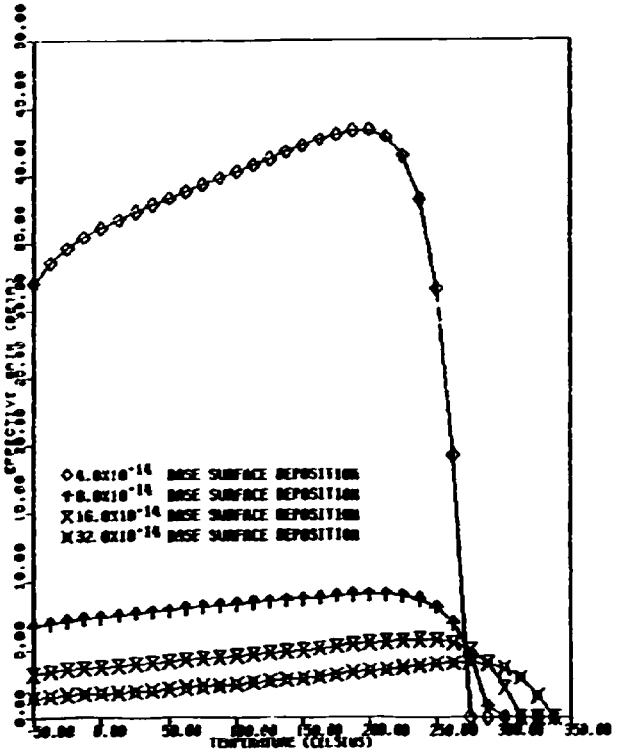


Figure 5-4. Continuation of Figure 5-3 with Even Higher Base Doping.

The large values of effective gain shown in Figures 5-3 and 5-4 are artifacts of the modeling process. The NPN transistor model gain is determined primarily by the transistor's base width which is specified in the computer model. This results in the wide gain swings for the transistor as the base doping level changes. In reality, it is the transistor gain which is a processing specification and not the base width.

The modeling results with the base deposition variations indicated that the doping at the base emitter junction strongly affected the high temperature performance. These changes could also be produced by changing the epi doping level to form the base/emitter junction closer to the chip surface at a higher base doping. To verify this, the epi thickness was set at 5 microns to keep substrate doping from influencing the experiment, and variations in the epi doping level were modeled. The results presented in Figures 5-5 and 5-6 were produced by setting the base deposition at 1.6×10^{15} atoms/cm^2 (the third curve in Figure 5-4) and varying the epi doping. The high temperature rolloff point does not exceed 300° C as predicted by the base doping variations even though the changes in the NPN emitter doping increased to a level that was five times larger than used in Figure 5-4. The reason for this was shown by the variations in the PNP alpha which is directly effected by the epi doping level. As the doping increased causing a reduction in alpha, the net result was to simulate a lower injection current level into the NPN transistor. At NEPIE = 5.1×10^{18} in Figure 5-6, the injection current into the gate has been decreased enough to cause a reduction in the high temperature performance.

A possible solution to this dilemma would involve the growth of a double layer of epi. The PNP base doping can then be controlled independently of the NPN emitter doping. Growing a double epi layer with different doping levels produces the improvements shown in Figure 5-7. A bottom epi level (NEPIE) doped at 1.0×10^{18} atoms/cc sets the NPN emitter and base doping level while the top level (NEPIB) is varied to control the PNP base doping and the PNP alpha. Figure 5-7 reproduces the corresponding curve in Figure 5-4 for a base surface deposition of 1.6×10^{15} atoms/cm^2 and a top base doping (NEPIB) of 3.0×10^{18} atoms/cc. While a double epi layer may not be a practical solution from a processing point of view, the arrival at this point has shown the direction to be taken in improving the high temperature performance of I^2L.

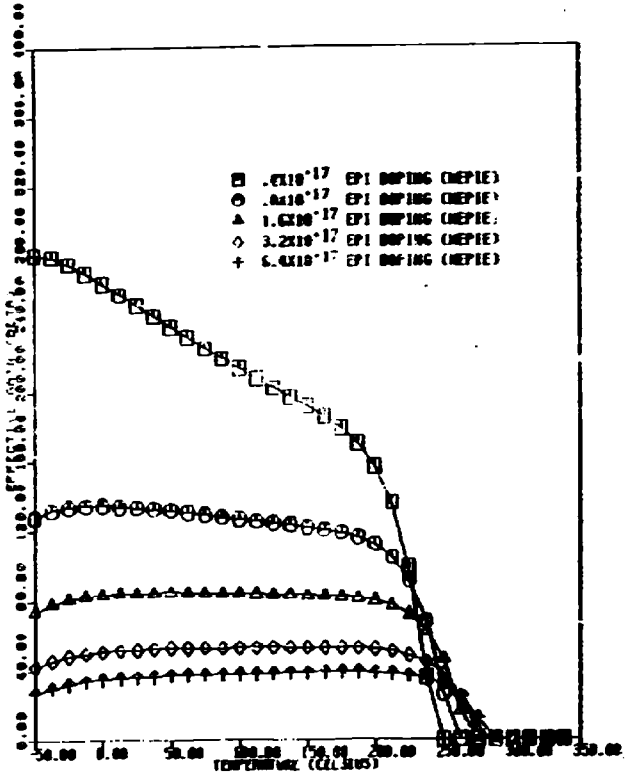


Figure 5-5. Effect of Epi Doping (5 Microns Thick) in I^2L Operating Range.

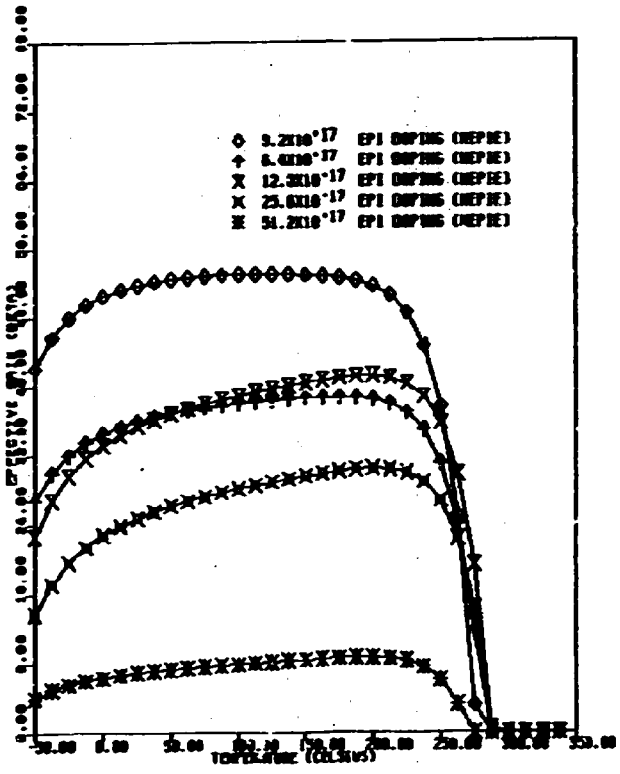


Figure 5-6. Continuation of Figure 5-5 with High Epi Doping Levels.

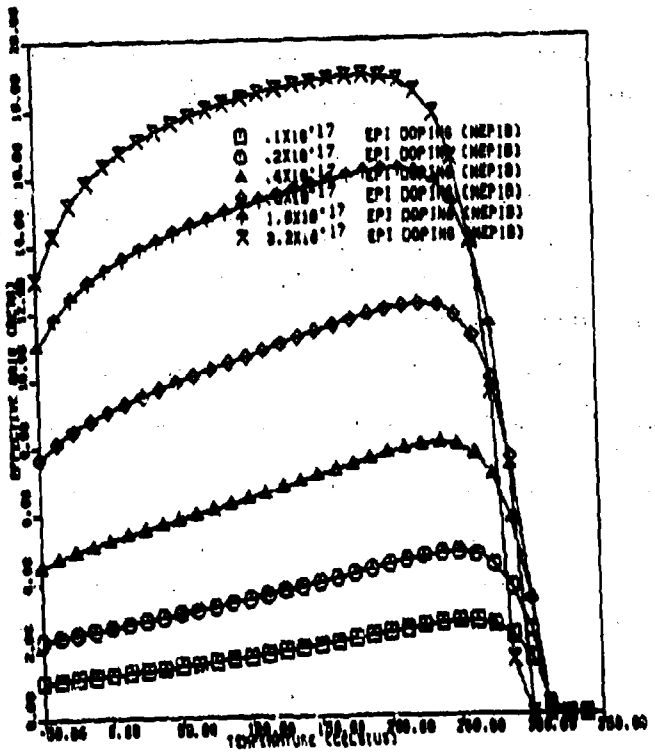


Figure 5-7. Effect of Changes in Top Epi Doping (PNP Base) with Bottom Epi Layer Doped at 1 x 10^{18}.

Reports in the literature have indicated that the slow switching speed of I^2L gates was due to a storage of minority carriers in the NPN emitter region. This situation may be improved by using a thinner epitaxial layer allowing the base to drive down to the substrate and increasing the emitter doping. Since the previous modeling results had indicated that these doping level changes would also improve the thermal operating characteristics, a study of epi thickness variations was undertaken.

The initial information needed was the base doping profile to be produced in fabricated devices. From published data, the base doping at the surface was found to be 5.0×10^{18} boron atoms/cc. At a depth of 2.5 microns, this concentration was reduced to 1.0×10^{17} atoms/cc. These values allowed a computation of the surface concentration of boron atoms before diffusion and the diffusion coefficient-time product. Once these process parameters were known, the base doping profile could be computed. As the epi thickness varied, the depth to which the base region penetrated could be computed by matching the concentration profile to the substrate or the epi concentrations. This matching resulted in a value for the junction depth and base/emitter junction doping levels. The effective gain was modeled using this standard base profile. Figure 5-8 shows the effect of epi thickness on the effective gain and the high temperature thermal roll-off.

The thinner epi approach appears to be the optimum direction in which to proceed for producing both faster devices and higher operating temperatures. This does pose a problem on device yield and gain variations since driving the base down to the substrate references the base/emitter junction to the substrate while the collector/base junction is referenced to the surface. In addition, forming the transistor base region near the epi substrate interface may introduce yield problems due to the defect density in that region. To correct this deficiency, the base deposition was increased so the base concentration could exceed that of the substrate doping. Then with a thin epi layer, the base diffusion could penetrate into the substrate and form the base/emitter junction inside the substrate instead of within the epi layer. This again references the junction depths to the chip surface and

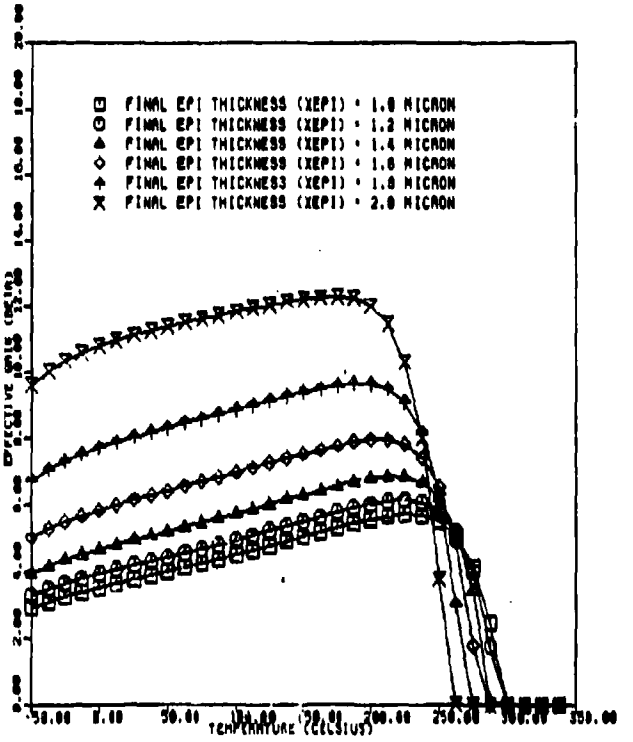


Figure 5-8. Effect of Epi Thickness on I^2L Operating Range with a Standard Base Doping Profile.

avoids the problem of epi thickness variations affecting NPN base width. In Figure 5-9, the curves for 0.8 and 1.0 micron epi thickness superimpose showing significant improvements in the upper operating limits and epi thickness immunity. With the base diffusion capable of penetrating slightly over 1 micron down into the chip substrate, the effect of a thicker epi would be to form the base/emitter junction at the epi-substrate interface where the doping level drops rapidly from substrate to epi. Forming the base/emitter junction in this transition region leads to the base width problems mentioned earlier plus a more lightly doped junction. The remaining curves in Figure 5-9 and the continuation in Figure 5-10 for even thicker epitaxial layers show how the critical parameter is the epi thickness. However, as the epi thickness reaches 3 microns (Figure 5-11), the base/emitter junction is formed in the epi layer above the substrate and the effect of the substrate and epi thickness is diminished.

Other effects were also modeled to illustrate their impact on the limits to high temperature operation. Previously, it had been assumed that the gain of the NPN transistor had little effect on the operating limits. To test this hypothesis, the base width was varied from 0.2 to 0.45 micron. The results shown in Figure 5-12 for a fan-in of one indicate that as the NPN gain changes by a factor of three, the roll-off temperature is changed by about 10° C. This sensitivity to transistor gain is caused by the leakage current amplification in the previous gate where the NPN Vbe is pulled down to Veat. An increase in gain also increases the transistor's thermal leakage current.

Design rule allowances may also affect the maximum operating temperature for I^2L. For example, the fan-out of a gate is determined by its design (number of collectors) but the fan-in may consist of an arbitrary number of collectors Or-Tied together. The modeling results for this variation shown in Figure 5-13 indicate that as more collectors are tied to a gate input (NPN base), their leakage currents divert more of the gate's injection current. Thus the maximum temperature for operation is reduced until the thermally generated leakage currents are scaled down to manageable proportions.

Realising that leakage currents into previous logic stages were affecting the desirable high temperature properties, an attempt was made to compensate for these losses. Figure 5-14 shows the effect of varying the PNP injector

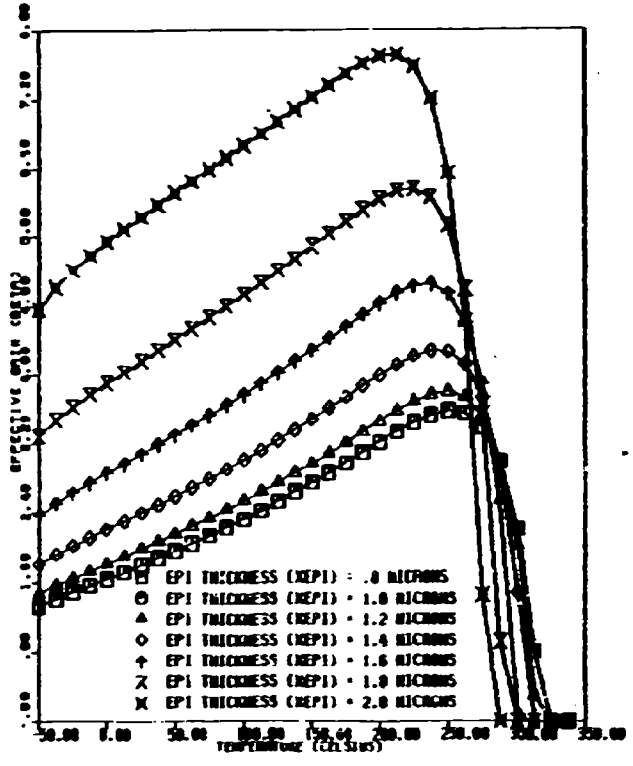


Figure 5-9. Effect of Epi Layer Thickness on I^2L Operating Range.

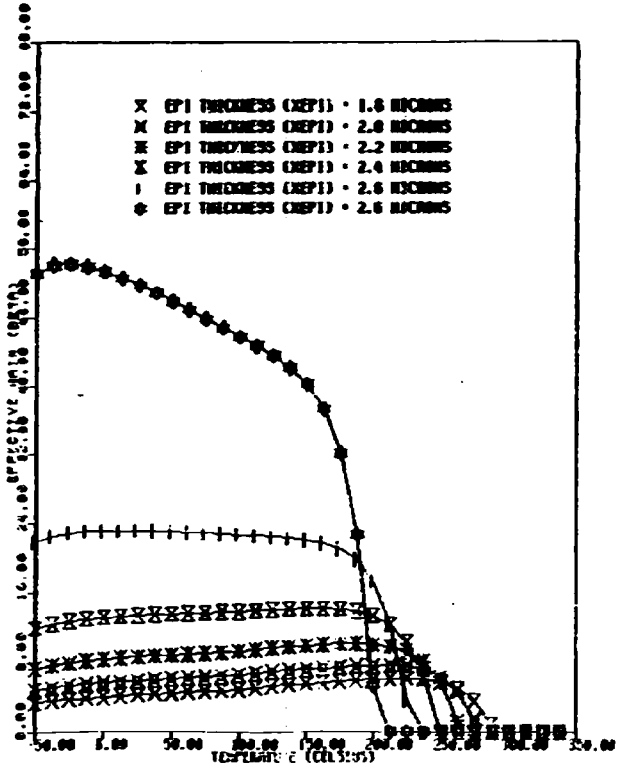


Figure 5-10. Continuation of Figure 5-9 for Thicker Epi Layers.

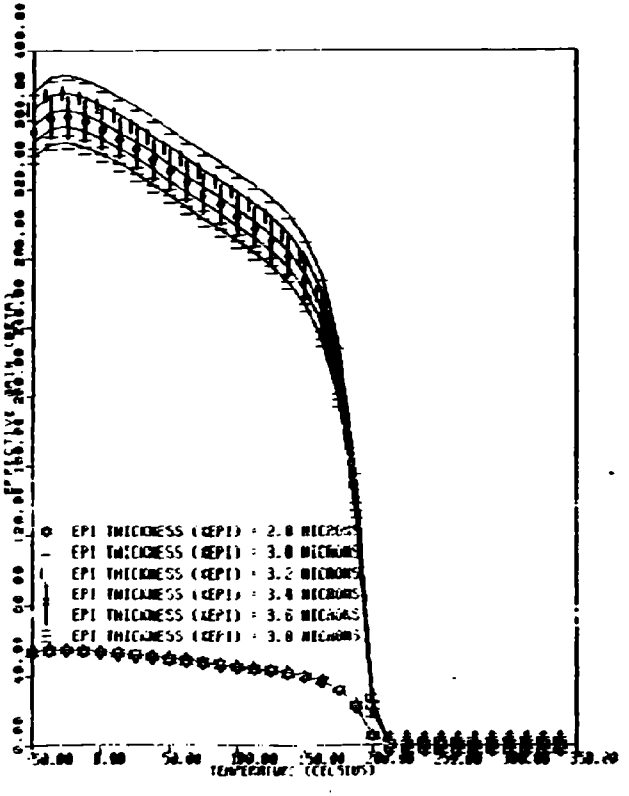


Figure 5-11. Continuation of Figure 5-9 and 5-10 for Thicker Epi Layers.

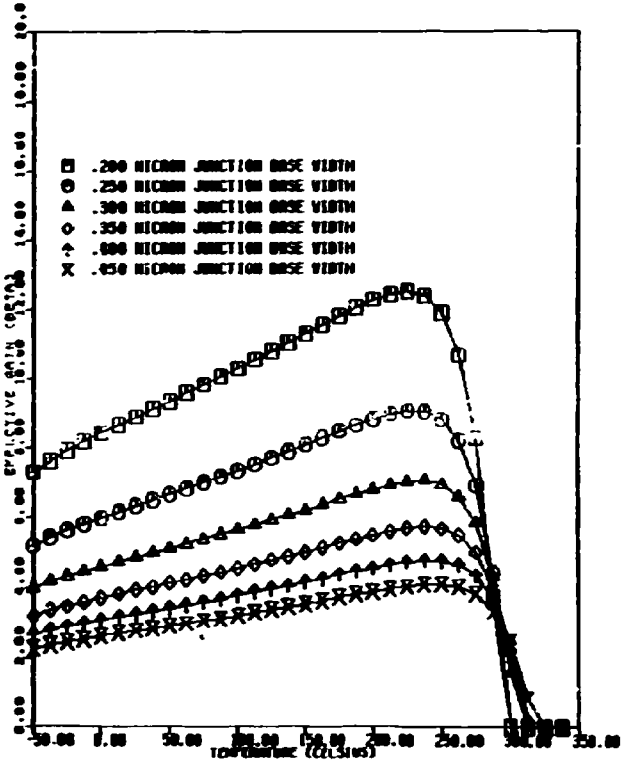


Figure 5-12. Effect of NPN Base Width Variations on I²L Operating Range.

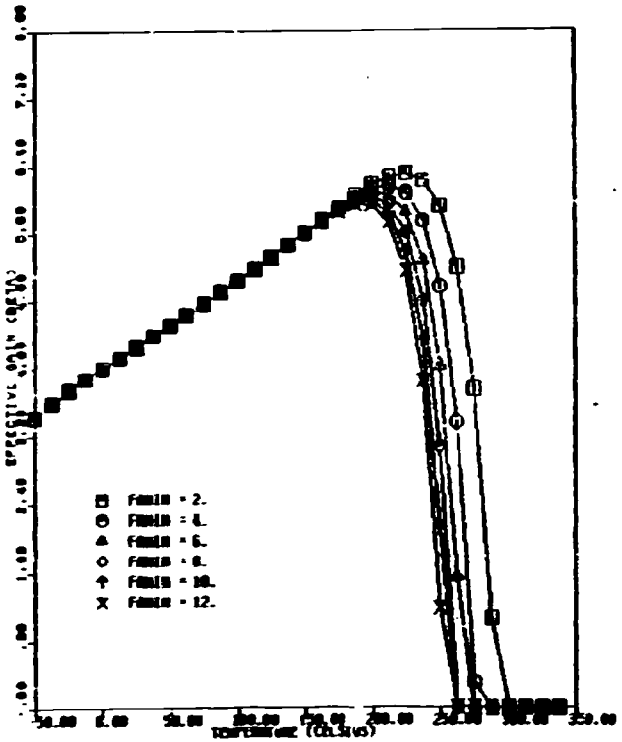


Figure 5-13. Effect of Fan-in Design Rule Variations on High Temperature I^2L Operation.

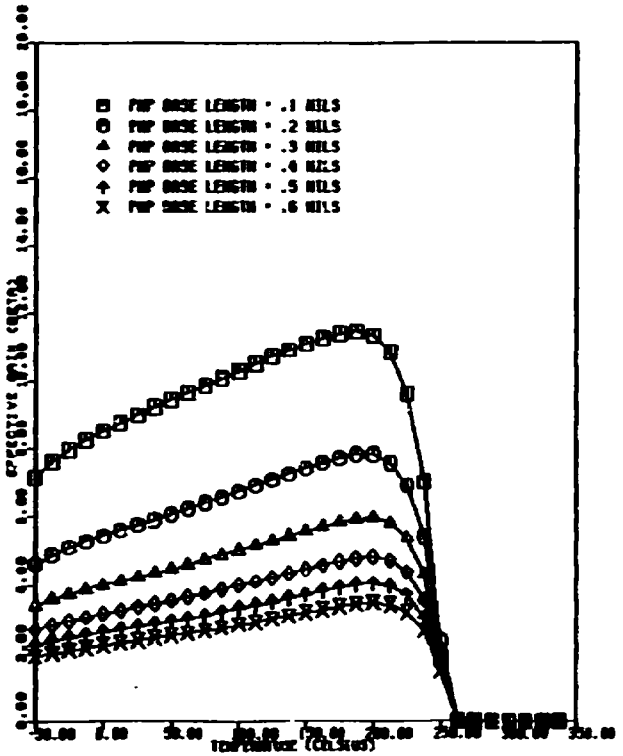


Figure 5-14. Variations in PNP Base Length (Injector Size) Show Little Influence on High Temperature Operation.

size (base length) for a gate with a fan-in of 10. The intention was to increase the injection efficiency to supply leakage currents to all the collectors tied to that input. However, leakage currents of 5 microamperes per collector at 250° C were sinking a majority of the total current (68 microamperes) injected into the NPN gate.

Finally, from the modeling results, the processing changes were specified for the fabrication of high temperature integrated injection logic and these values modeled to project what may be expected. The base surface deposition should be increased by a factor of four from the normal process to provide a margin for production tolerances. A 0.2 ohm-cm epilayer should be grown on a 0.01 ohm-cm substrate and, as a result, the base/emitter junction is expected to be formed in the substrate at a depth of 1.48 microns with thin epi. The first three curves in Figure 5-15 reflect the tolerance for epi thickness variations in the final high temperature performance. The gain decreases with decreasing epi thickness since the effective active area of the PNP injector is being decreased. At an epi thickness of 1.6 microns and larger in the figure, the base diffusion stops at the epi-substrate interface to form the base/emitter junction which becomes progressively more lightly doped as the epi gets thicker.

The lower effective gain, in general, is due to the more heavily doped intrinsic base region. This is not expected to be a problem for two reasons. First, the gate being modeled was a quad gate with two injectors where a fan-out of four was assumed. Since a fan-out of two is normally used for high temperature on radiation-hardened circuits, this would essentially double the effective gain. Second, the modeling was performed with a fixed NPN base width. In practice, this thickness is adjusted during fabrication to produce acceptable gain by trimming the collector diffusion time and thus the base collector junction depth. As a result, reasonable gain and improved high temperature performance can be expected from these devices.

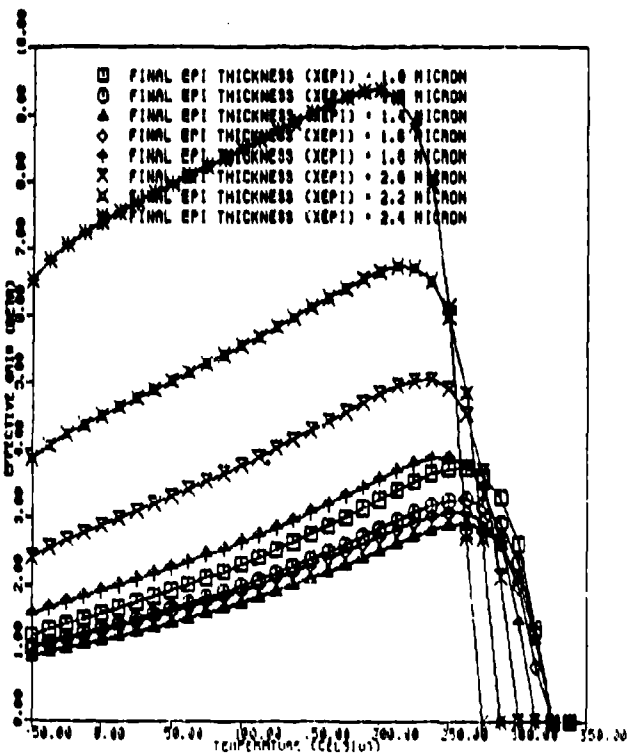


Figure 5-15. Effect of Epi Thickness Variations on High Temperature Operation with Standard Base Doping Increased by a Factor of Four.

6.0 SUMMARY AND CONCLUSIONS

The failure modes for high temperature electronics may be divided into those affecting the semiconductor material itself and those which degrade the metallization and interconnections to the external world. Life tests were run to evaluate failure modes from both categories. The alleviation of the most critical modes of device failure was the prime goal of this program.

This program phase has demonstrated that silicon based I^2L semiconductors can survive without degradation for over 5000 hours at 360° C. The circuits used in this test employed aluminum metallization in which the current densities were purposely kept low to avoid electromigration failures. Thirty I^2L ring oscillators were subjected to a powered test at 340° C while 30 more were placed in an unpowered test at 360° C. No failures were found after 5000 hours in either case. From these results, it can be concluded that the silicon semiconductor material has the intrinisic capability to function at the 300° C design point.

The majority of this program's resources were directed toward the development of a gold based metallization system and the associated diffusion barrier. The prime candidate to fill this need was a Ti-W/Au metallization. The problems that were addressed involved the diffusion barrier integrity, the cohesion of the metal system, and the reduction of hillock and void formation at elevated temperatures.

Substantial improvements have been made in the titanium-tungsten diffusion barrier during the course of this program. At the beginning of this phase, the barrier was demonstrated to be stable for up to 2000 hours at 300° C with little change from the as-deposited condition. However, a need for higher temperature accelerated testing resulted in complete barrier failures after 100 hours at 350° C. A solution to the high temperature barrier integrity problem was implemented by "stuffing" the titanium-tungsten grain boundaries with nitrogen during the deposition process. This solution resulted in diffusion barriers which have survived for thousands of hours at 360° C with no degradation.

The reactive sputtering (stuffing) of the Ti-W diffusion barrier in nitrogen created exceptional diffusion barriers but led to other problems due to inadequate adhesion. The absence of sufficient adhesion between the Ti-W layer and the gold layer or semiconductor substrate was characterized by metal runs lifting or breaking at oxide steps during life tests, problems in bonding external connections to the chip metallizations during packaging, and by the ability to remove metallization with a tape peel test. The deposition of an undoped Ti-W layer on both sides of the nitrogen "stuffed" layer is expected to eliminate these symptoms.

Gold hillock growth was found to be driven by the thermal expansion mismatch between the gold metallization layers and the underlying diffusion barrier and semiconductor substrate. The gold layer was placed in compression at elevated temperatures which caused the hillock growth. Solutions to this problem include deposition of the gold at elevated temperatures and the application of a passivation. The voiding in the gold layer that was observed in early life tests was found to be caused by undercutting during the wet chemistry etching used in defining the metallization pattern. This voiding was eliminated through the use of lift-off and ion milling techniques instead of chemical etching.

Computer modeling investigations, aimed at improving the high temperature performance of integrated injection logic, were conducted using the General Electric I^2L Gate Model. The results of this study indicated that doping changes for the epitaxial layer and base diffusion could increase the high temperature operating limits. In addition, the effects of design standards and processing variables such as gate fan-in and transistor gain (beta) were studied. A series of guidelines was developed for future designs and processing to improve the high temperature performance of I^2L.

This program has demonstrated that high temperature electronics for operation up to 300° C can be constructed with the technology which is presently available. Substantial lifetimes can be obtained as demonstrated by the accelerated life tests that were performed. The acceleration factors are not known since the corresponding activation energies have not been determined. However, if the activation energies were to fall within the range of 0.6 to 1.0 eV, then the lifetime acceleration of the 360° C tests over operation at

300° C would be between 3.2 and 6.8. This, combined with the life testing results, implies that the aluminum metallized circuits could have survived for over 2 years of continuous operation at 300° C without failure.

The Ti-W/Au metallization system developed during this program is being life-tested in MSI I^2L chip packages as part of Naval Research Laboratory follow-on program Contract No. N00014-83-C-2393. As of this report date (March 1984), over 2000 hours at 360° C have been achieved and 10% of the circuits have failed. No failures have been encountered after 2000 hours at 300° C. Testing is continuing.

Specific conclusions from this program are listed as follows:

- I^2L integrated circuits with Al metallization can operate reliably at 360° C for over 5000 hours if current densities are low.
- Life tests of MSI microcircuits fabricated using Ti-W/Au metallizations have demonstrated lifetimes exceeding 2000 hours at 360° C.
- A nitrogen doped Ti-W diffusion barrier has been shown to be an effective diffusion barrier between gold and silicon at temperatures as high as 360° C.
- Adhesion of Ti-W to gold or silicon oxides is degraded by barrier "stuffing." Good adhesion can be achieved by using an unstuffed Ti-W layer at the interfaces.
- Gold hillock formation caused by thermally induced strain can limit the life of gold metallizations. Passivation of the films with silicon nitride can retard this mechanism, as can deposition of the gold at elevated temperatures.

7.0 BIBLIOGRAPHY

1. Kreitinger, T.M., Marvin, M.D., et al., "Full Authority Digital Electronic Control, Phase II Final Report," R82AEB435, October 1983.

2. Morris, W.L., et al., "High Temperature Electronics Technology, Phase I Final Report," R80AEG212, March 1980.

3. Hill, M., "Magnetron Sputtered Titanium-Tungsten Films," Solid State Technology, Vol. 23, pp. 53-59, January 1980.

4. Nowicki, R.S., Harris, J.M., Nicolet, M.A., and Mitchell, I.V., "Studies of the Ti-W/Au Metallization on Aluminum," Thin Solid Films, Vol. 53, pp. 195-205, 1978.

5. Baker, J.E., Blattner, R.J., Nadel, S., and Evans, C.A., "Thermal Annealing Study of Au/Ti-W Metallization on Silicon," Thin Solid Films, Vol. 69, pp. 53-62, 1980.

6. Nicolet, M.A. and Bartur, M., "Diffusion Barriers in Layered Contact Structures," Journal of Vacuum Science and Technology, Vol. 19, pp. 786-793, September/October 1981.

7. Chang, C.A., "Passivating Process for the Thin Gold Layer on Silicon," IBM Technical Disclosure Bulletin, Vol. 21, p. 4244, March 1979.

8. Shih, D.Y. and Ficalora, P.J., "The Reduction of Au-Al Intermetallic Formation and Electromigration in Hydrogen Environments," IEEE Transactions on Electron Devices, Vol. ED-26, pp. 27-34, January 1979.

9. Mayer, D.E., "Effects of Hydrogen Incorporation in Some Deposited Metallic Thin Films," Journal of Vacuum Science and Technology, Vol. 17, pp. 322-326, January/February 1980.

10. Anderson, R.E., Ragonese, L.J., and Wanger, R.P., "High Temperature Electronics Technology - Interim Tasks, Final Report Draft," pp. 54-61, April 1980.

APPENDIX A

II. EXPERIMENTAL RESULTS OF HIGH TEMPERATURE I^2L TESTING*

* Extracted from report R79ELS042 published by the General Electric Electronics Laboratory, Syracuse, N.Y. and printed with permission.

II. EXPERIMENTAL RESULTS OF HIGH TEMPERATURE I^2L TESTING

The Electronics Laboratory has, on-hand, wafers and packaged chips from a series of developmental experiments aimed at improving the radiation hardness of integrated injection logic (I^2L). These were tested (under Independent Research and Development projects) at elevated temperatures to determine the operating extremes for this logic family.

The chips are a result of two bipolar processes. The older standard linear process used a P substrate, N^+ buried island and 10 μ of N^- epitaxial silicon. As a result, the NPN emitters tend to be lightly doped and an injected space charge in the emitter region slows the device switching time. A simplified linear process aimed at reducing the emitter space charge used 6 μ of N^- epi on top of a N^+ substrate. As a result, I^2L gates processed by the simplified linear process switch faster than standard linear process gates. Through high temperature testing, it was found that the simplified linear process gates, ring oscillators, flip-flops, and code generators failed at a lower temperature than the gates and ring oscillators produced by the standard linear process. Although the processes are well-behaved established production techniques, it should be remembered that the high temperature tests were run on only two lots, one from each process. As a result, it cannot be stated with certainty that one process produces better high-temperature I^2L than the other. Measurements on chips resulting from the simplified linear process will be discussed first, followed by the chip measurements on the standard linear process.

Figure 1 illustrates some of the initial measurements made at the wafer level while sorting out good chips for packaging. The figure shows variations in the speed-power product from wafer to wafer. Notice that the minimum gate propagation delay ranges from 21 to 36 ns. These measurements were made on 5 wafers from a single lot.

Figure 2 shows the effect temperature has on the speed power product for I^2L. At lower injection currents, the curves approach a constant speed power asymptote. This will be roughly parallel to a constant speed-current line, since the dissipated power is a product of the injection current and the PNP transistor base emitter voltage. The effect of increasing temperature on I^2L is to reduce the transistor base-emitter voltage, as will be seen from experimental and modeled results; thus the power dissipated for a given injection current level will be reduced at elevated temperatures. An interesting phenomena that occurs at about 150 μA injection current (in Figure 2) is a constant propagation delay over the entire temperature range from 25°C to 250°C. This has potential applications on critical high speed logic, where timing cannot be temperature sensitive.

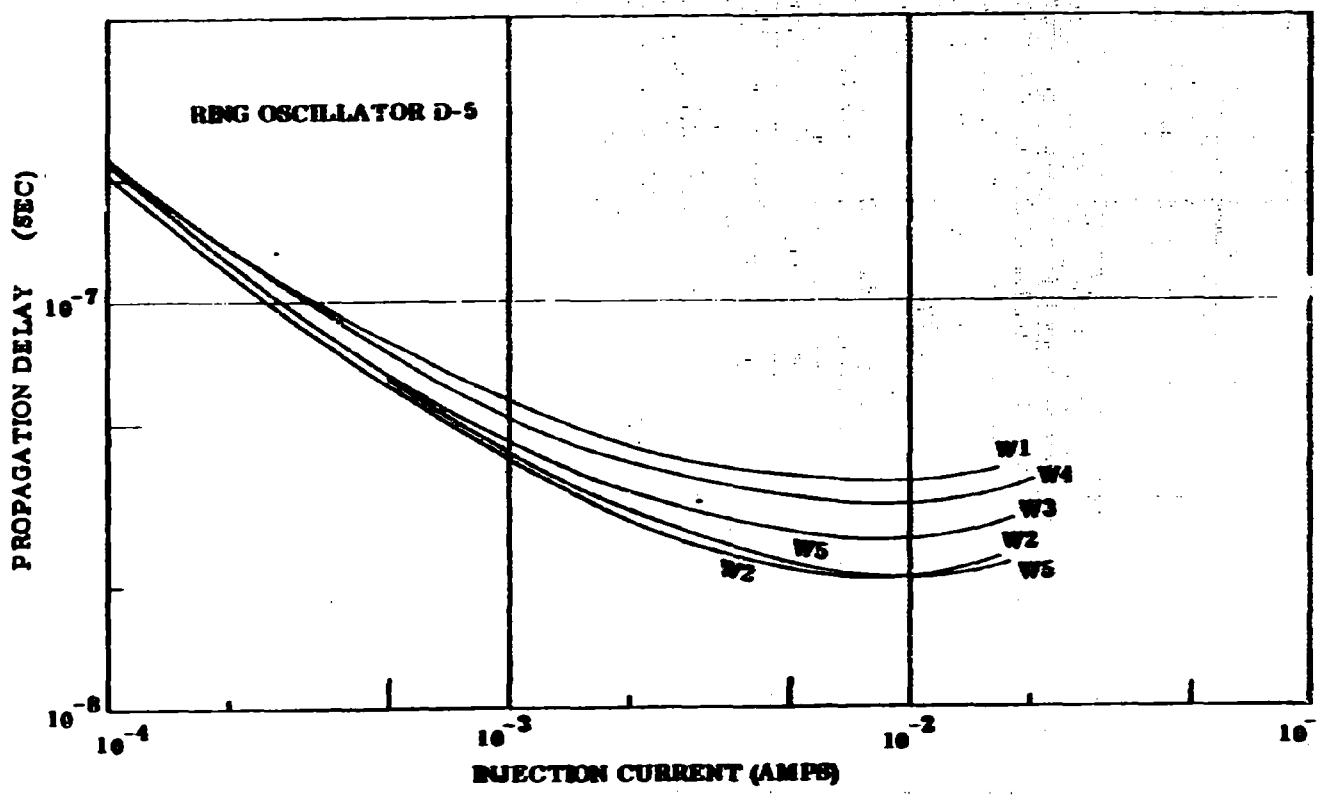


Figure 1. Room Temperature Propagation Delay Variations from Wafer to Wafer

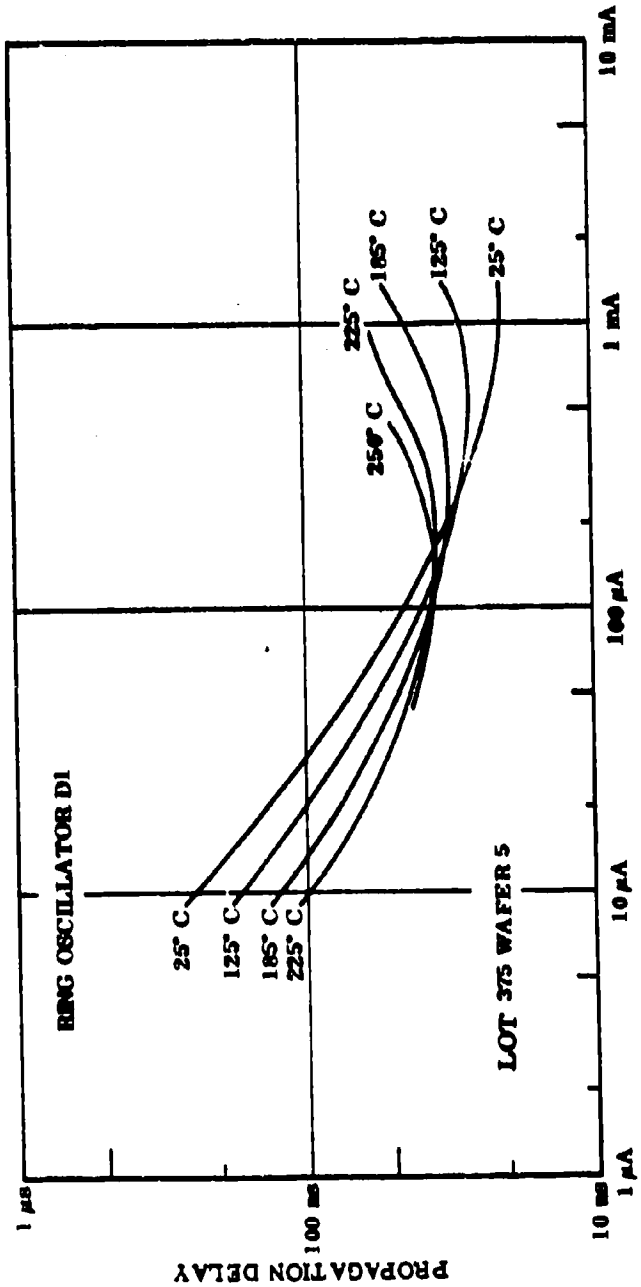


Figure 2. Effect of Temperature on Speed/Power Product

The measurements illustrated in Figure 2 were performed over injection levels ranging from 9 μA per gate to 1.4 mA per gate in a ring oscillator composed of dual fanout gates. It can be seen that the range of injection currents over which oscillations occur decreases with increasing temperature. For the low injection current end of the operating range, at 250°C, the gates will not operate below 45 μA per gate. This is a result of the effective gate gain dropping below unity due to collector leakage current from the previous off-stage. The leakage current sinks such a large fraction of the injection current that the gate cannot turn on.

As injection current increases, the propagation delay approaches a minimum value due to the frequency limitations of the transistor. This limit is related to the diffusion time needed to transport minority carriers across the base region. As temperature increases, the minority carrier mobilities decrease, increasing the base transit time. Another factor is the increased resistivity of the silicon, which, together with higher current densities, leads to problems such as emitter crowding and reduced gain. This, in turn, places a limit on the maximum injection current at which operation is possible.

Figure 3 represents typical data on the maximum frequency of operation for a D-flip-flop as a function of total injection current. The curves are similar to those presented in Figure 2 since similar effects are being represented. The total injection current is essentially shared equally by all the gates, while the maximum operating frequency is related to the reciprocal of the gate propagation delays. The relation between gate propagation times and maximum clocking speed occurs because a series of gates must change state during each clock cycle to enable the flip-flop to toggle. Although the span of the input current measurement does not reach two full decades, the range of operation for the flip-flop at 250°C is clearly limited in the same fashion as the ring oscillators in Figure 2. Again the maximum temperature of operation is in the 250°C range.

The operation of a larger array of gates than a flip-flop can be observed using the 16-bit pseudorandom code generator. The code generators were constructed from 49 dual I^2L gates. The measured results are summarized by Figures 4, 5 and 6. Figure 4 shows the wafer-to-wafer variations observed at the maximum frequency of operation at 25°C. Figure 5 again illustrates the effect of temperature on the maximum operating points. Figure 5 shows an increase in the minimum injection current operating points as temperature increases, similar to that observed in Figure 2 for ring oscillators. The operating region for the code generators is essentially all the space above the curves in Figures 4 and 5. Intuitively, this seems reasonable for any static logic family; i.e. that it will operate at any clock speed lower than some maximum. However, at temperatures near the maximum for correct operation, the code generator operating region also becomes bounded at the lower frequencies. Figure 6 shows the measurements made on one code generator at 260°C. The range of injection currents is limited from about 66 μA per gate to 250 μA per gate, which was a phenomena observed with the ring oscillators and the D flip flops. However, the bound on the lower limits of operating frequency is an anomaly only observed near the top of the temperature range.

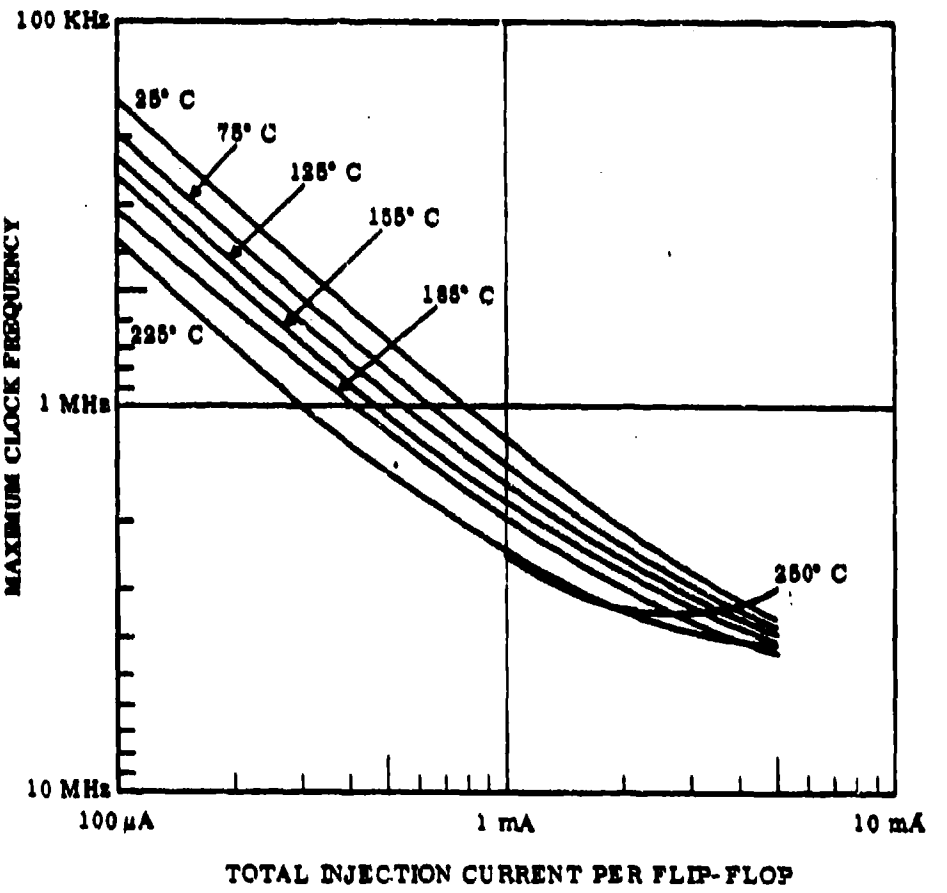


Figure 3. Maximum Operating Frequency of a Flip-Flop

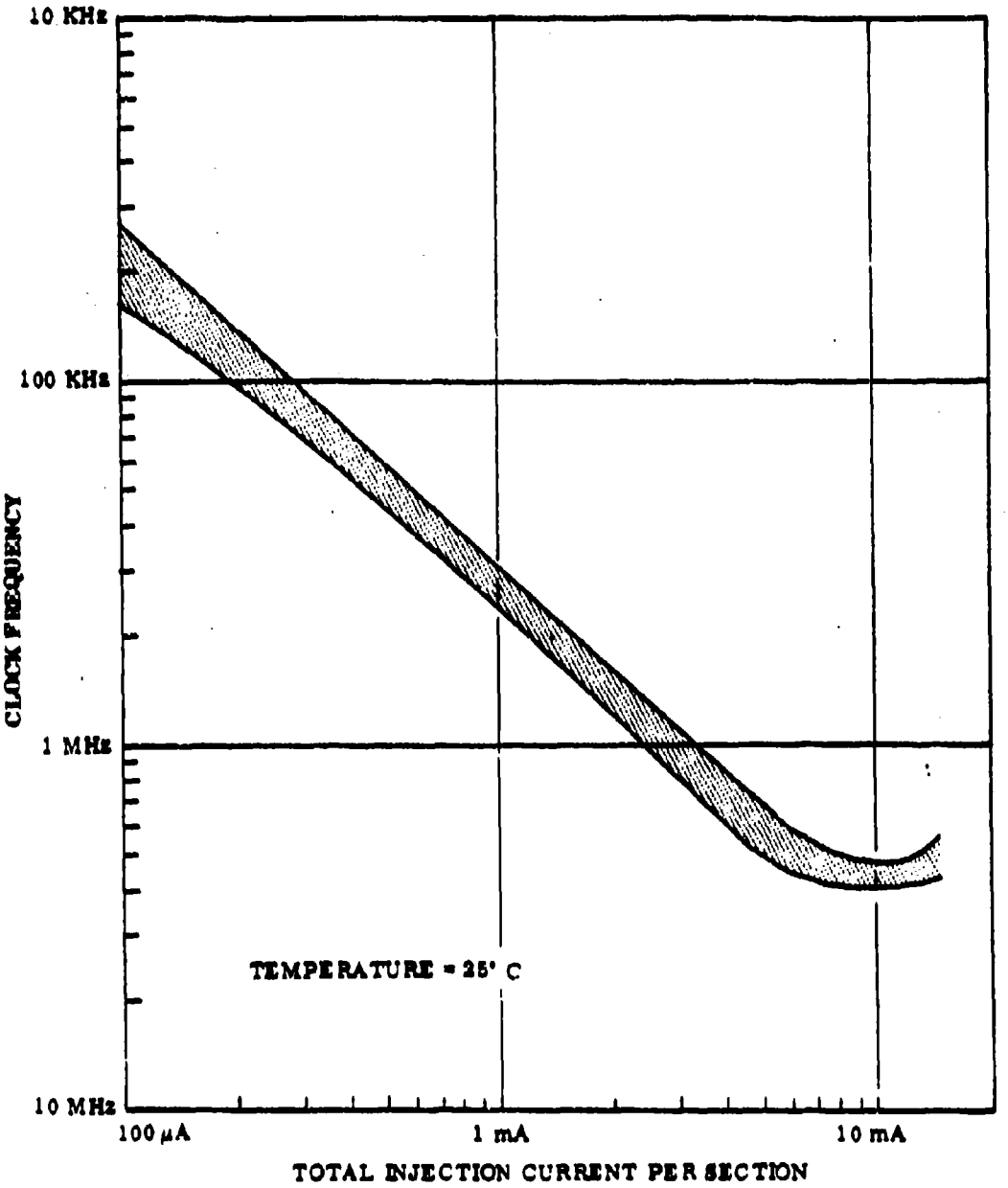


Figure 4. Variations in Maximum Operating Frequency Among Samples of Code Generators

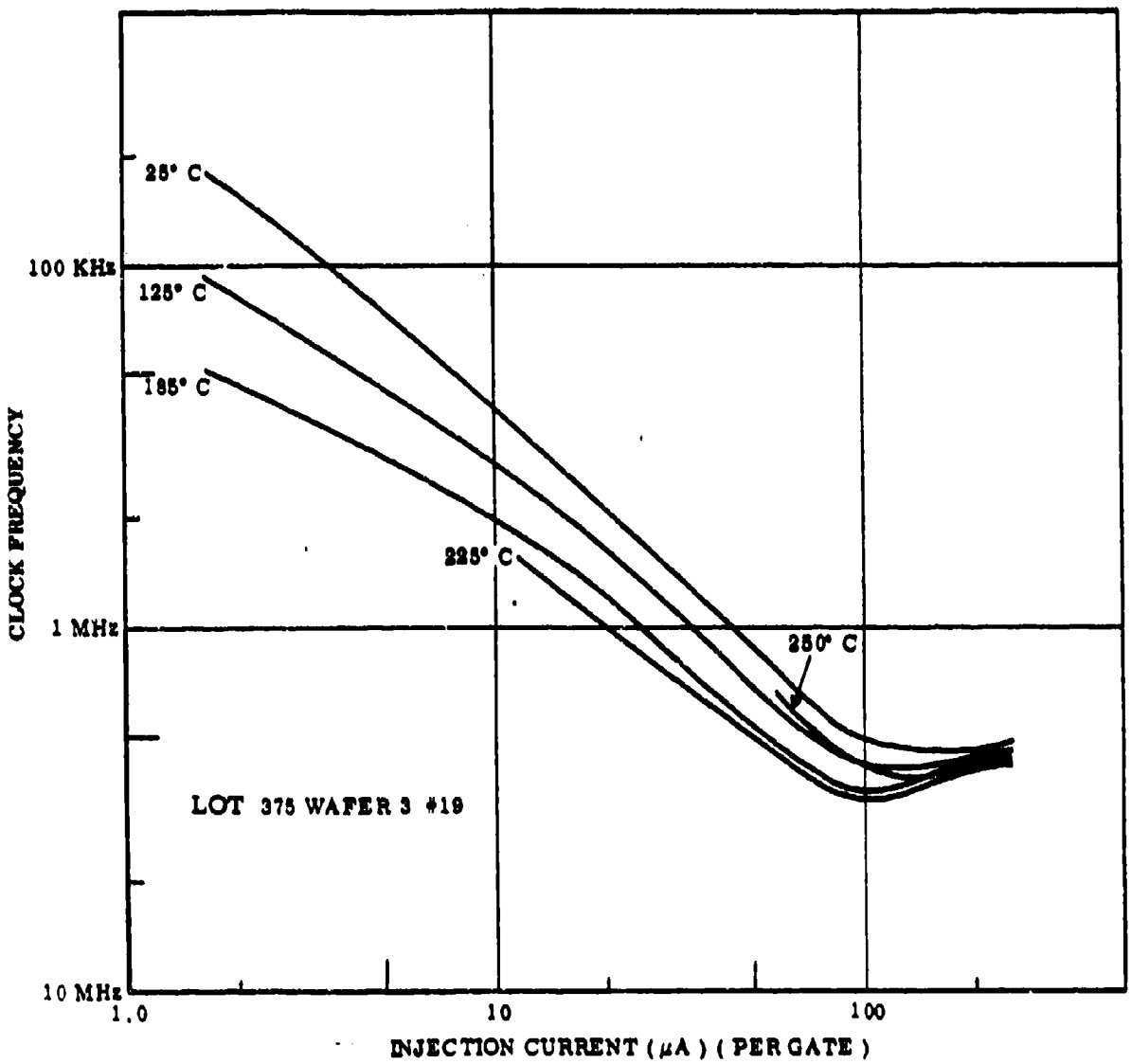


Figure 5. Effect of Temperature on Code Generator Operation

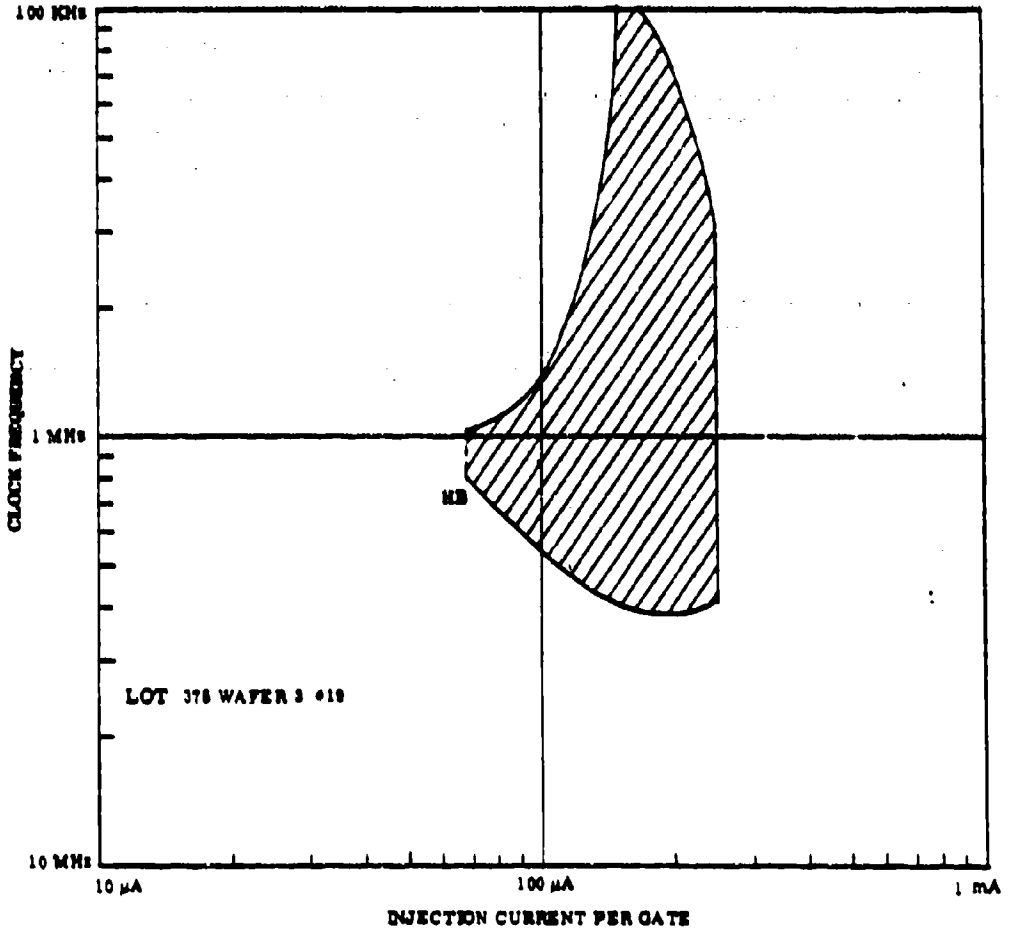


Figure 6. Operating Region for Code Generators at 260°C

Leakage currents in the reverse-biased junctions are a primary reason for the high-temperature limitations of I^2L logic. In an attempt to determine the magnitude of the problem, the collector leakage current (I_{CBO}) was measured for a quad A1 cell as a function of temperature for the standard and simplified linear processes. The leakage currents measured with a reverse bias of 3.0 volts are presented in Figures 7 and 8. The two leakage currents track, within device variations over the entire temperature range, as well they should, since the P and N^+ diffusions are similar for the two processes. An important point to note is that Figures 7 and 8 do not represent the collector leakage experienced by I^2L logic gates under operating conditions. The collector leakage current I_L will fall within a range $I_{CBO} \leq I_L \leq (\beta+1) I_{CBO}$, depending on the impedance to ground seen looking out of the base terminal. In support of this, the collector leakage currents for operating gates have been experimentally measured in the range of 20 to 30 μA. As will be seen later, when the leakage current reaches a magnitude comparable to the PNP injection current, logic signals will no longer propagate down a gate chain.

Above 150°C, the leakage current I_{CBO} increases an order of magnitude every 50°C (see Figures 7 and 8). In light of this, the results presented in Figure 9 seem more impressive since the standard linear process ring oscillators operate at 300°C over a current range comparable to the simplified linear process oscillators at 250°C. Measurements were also taken at -55°C to reconfirm that the device would operate at the bottom end of a military temperature specification. An interesting point of Figure 9 similar to one in Figure 2, is that at 40 μA injection per gate, the propagation delay essentially remains constant over the entire temperature range.

The effective gain for an I^2L gate is defined as the maximum current that a collector may sink divided by the current that will be withdrawn from the base contact by a saturated transistor collector in the previous logic stage. Obviously, if the previous stage collector cannot sink all the injection current, or if the previous stage collector leakage sinks to much NPN base injection current, the effective gain will be less than 1 and logic signal propagation will stop.

Thus, the measured effective gain, as shown in Figure 10, will also provide an indication of the operational limits of an I^2L gate. As a result, the information provided by effective gain measurements complements those obtained from ring oscillator studies. The oscillator only operates if the gain is greater than unity. Thus, they are useful when the absolute limits to operation are to be determined. However, gain measurements also indicate the available operating margin. Figure 10 shows how the effective gain varies with temperature for various injection currents. When the gain drops below 1, a logic system will not operate. This provides a quick check between effective gain and ring oscillator predictions. For example, in Figure 10, the effective gain for 10 μA injection current per gate drops below 1 at a temperature between 290°C and 300°C. Referring back to Figure 9, the lower limit for a ring oscillator operation at 300°C is about 40 μA injection current per gate. In this way, a comparison may be made between the results of the two measurements. In the previous example, a Quad-A2 gate cell was compared to results obtained from a dual fanout D2 ring oscillator. Considering these differences, the agreement is acceptable.

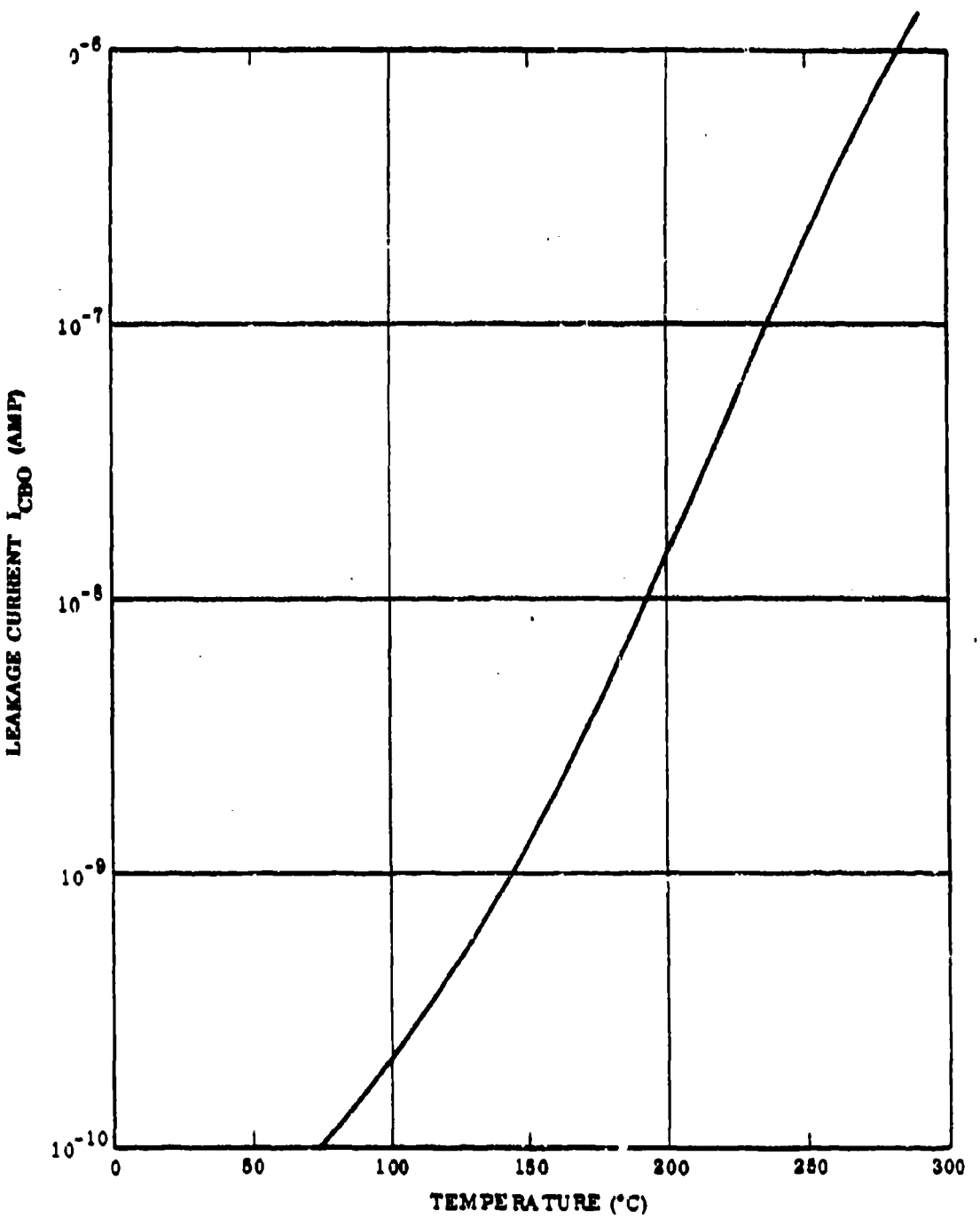


Figure 7. Simplified Linear Process Quad Collector Leakage Current (I_{CBO})

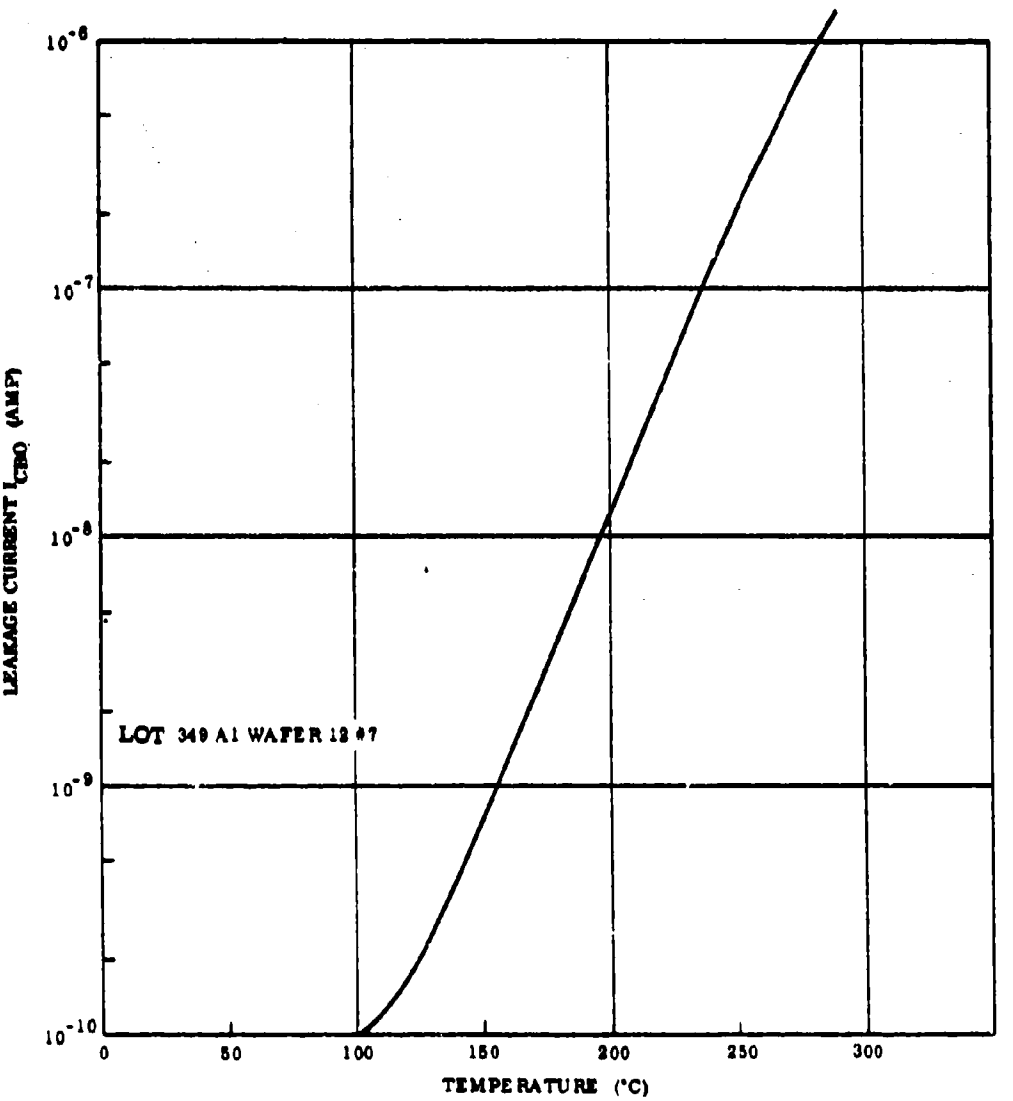


Figure 8. Standard Linear Process Collector Leakage Current (I_{CBO})

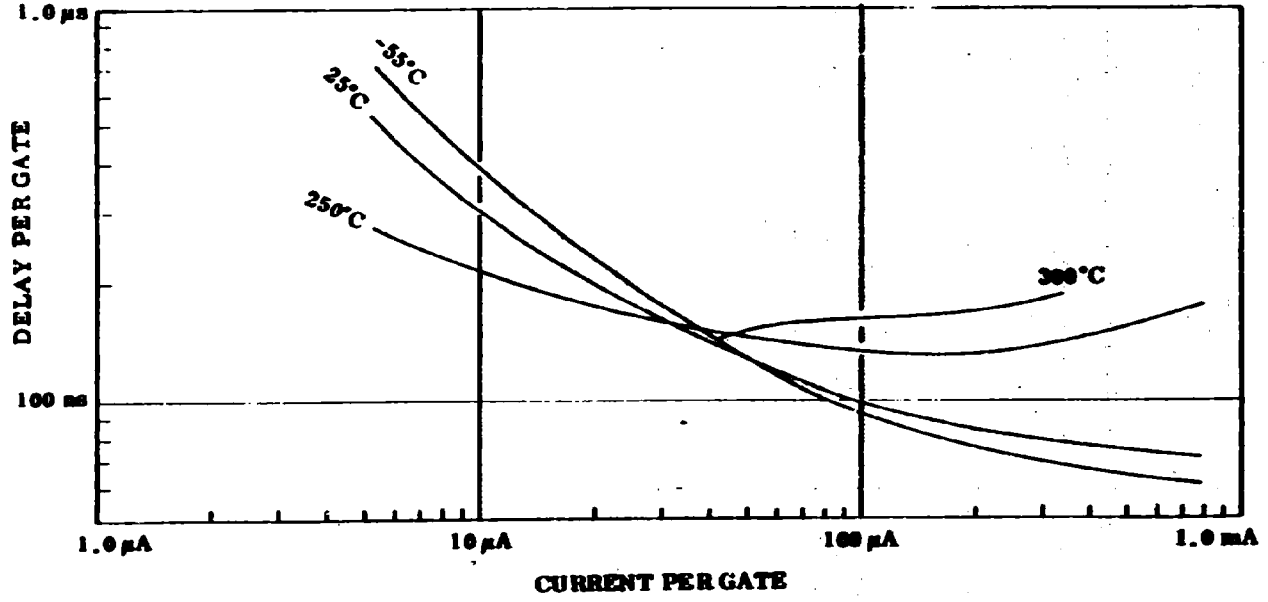


Figure 9. Effect of Temperature on Gate Delay for the Standard Linear Process

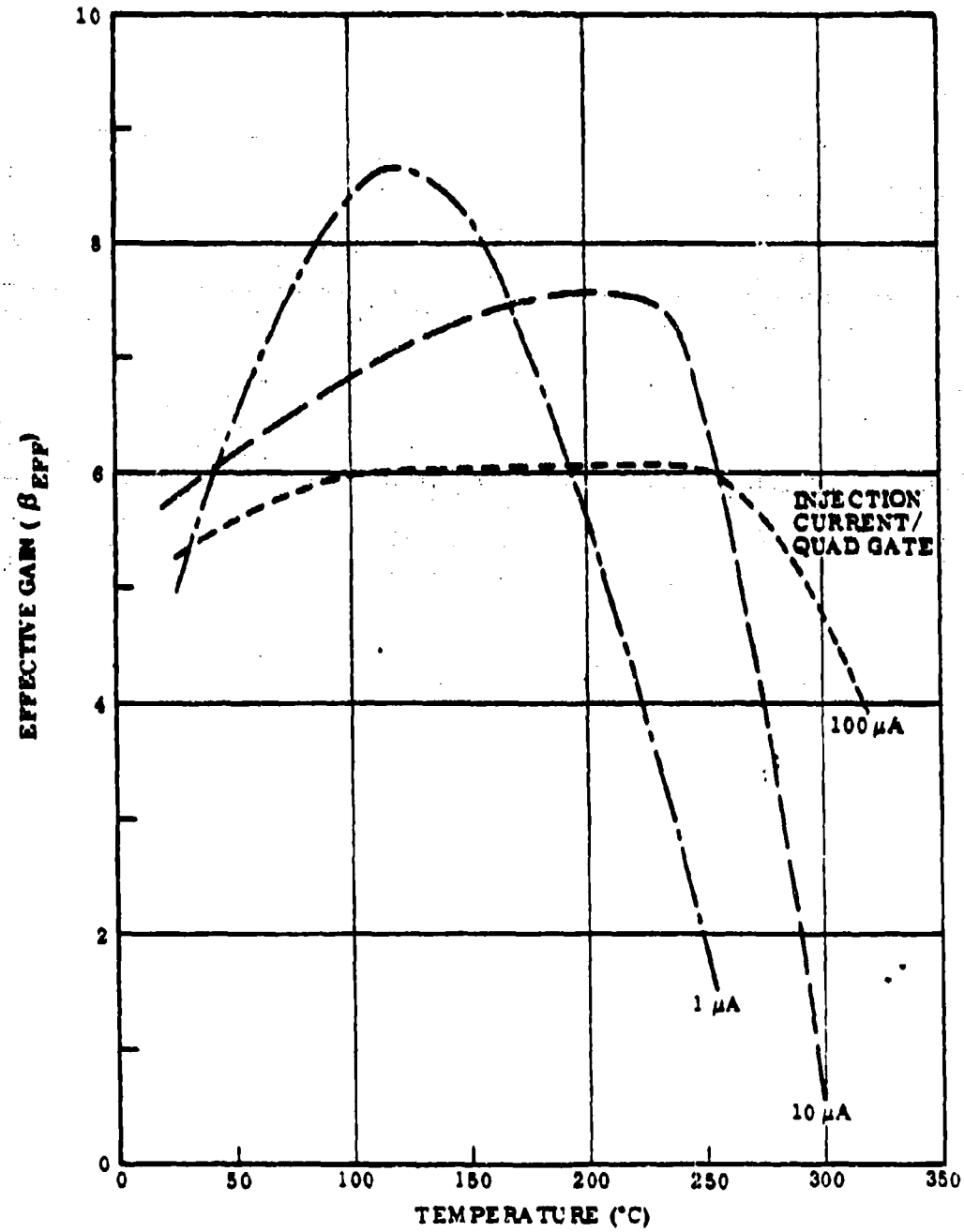


Figure 10. Measured Effective Gain versus Temperature for Quad-A2 Cell

Other measurements that can predict operating limits are the NPN base emitter voltage and the collector emitter saturation voltage. These parameters also yield a measure of the voltage noise margins. Figure 11 plots the measured base-emitter forward biased voltage drop for a Quad-A2 cell as a function of temperature. Figure 12 presents the NPN collector saturation voltages for a Quad-A2 gate, also as a function of temperature. During operation, the PNP injection forward biases the NPN base emitter junction and, with the collector conducting, a low (zero) logic level, is outputted to the following stage. The collector sinks injection current intended for the following stage, bringing its V_{BE} down to the V_{SAT} level of the collector. This essentially turns off the following stage producing a high (one) logic level. V_{SAT} must be less than V_{BE}; if V_{SAT} is equal or greater than V_{BE} there is no way to turn off any logic stage.

The effect of voltage swing margin may be observed from the data presented in Figures 11 and 12. As shown in Figure 11, the V_{BE} for 1 μA injection current is about 75 mV at about 245°C and steadily decreases with rising temperatures. Figure 12 shows that the V_{SAT} for 1 μA injection drops to 75 mV at 1 μA injection at about this same temperature. This implies that the voltage noise margin is zero and the device is about to fail. Figure 10 confirms this observation indicating that the effective gain drops below 1 at about 250°C. The voltage noise margin may be obtained for the complete operating region from the difference between the voltages presented in Figures 11 and 12. This provides a third indication of the operating bounds for an I^2L gate.

A further consideration to the high temperature operation of I^2L logic is interfacing it to the outside world. Inputting signals to an I^2L chip is straightforward since an input is left to float or is shorted to ground. Outputs from I^2L gates come from the NPN open collector. If these are to be used to drive loads off chip, then both the current leakage and voltage breakdown are important parameters. To indicate whether collector breakdown is a critical factor, V_{CEO} was measured for samples fabricated from both the standard and simplified linear process. V_{CEO} is not as appropriate as V_{CBO} for I^2L gate operation since, in the off state, the NPN base is tied to ground through a low-impedance saturated collector. V_{CEO} will provide a lower limit of the breakdown voltage since leakage current will be amplified by the gain of the transistor. Figure 13 plots the measured V_{CEO} for the two fabrication processes. As can be seen from the plot, the breakdown voltage only changes about 10% from room temperature to 300°C. As a result, the NPN collector breakdown voltage variations, with temperature, are not considered a dominant factor in high-temperature I^2L designs.

In summary, through measurements on I^2L devices conducted at the Electronics Laboratory, it has been found that collector leakage current is an important factor in the high temperature failure of I^2L digital logic. The operational bounds may be determined by various methods, the easiest of which is simply an observation of ring oscillator operation. However, ring

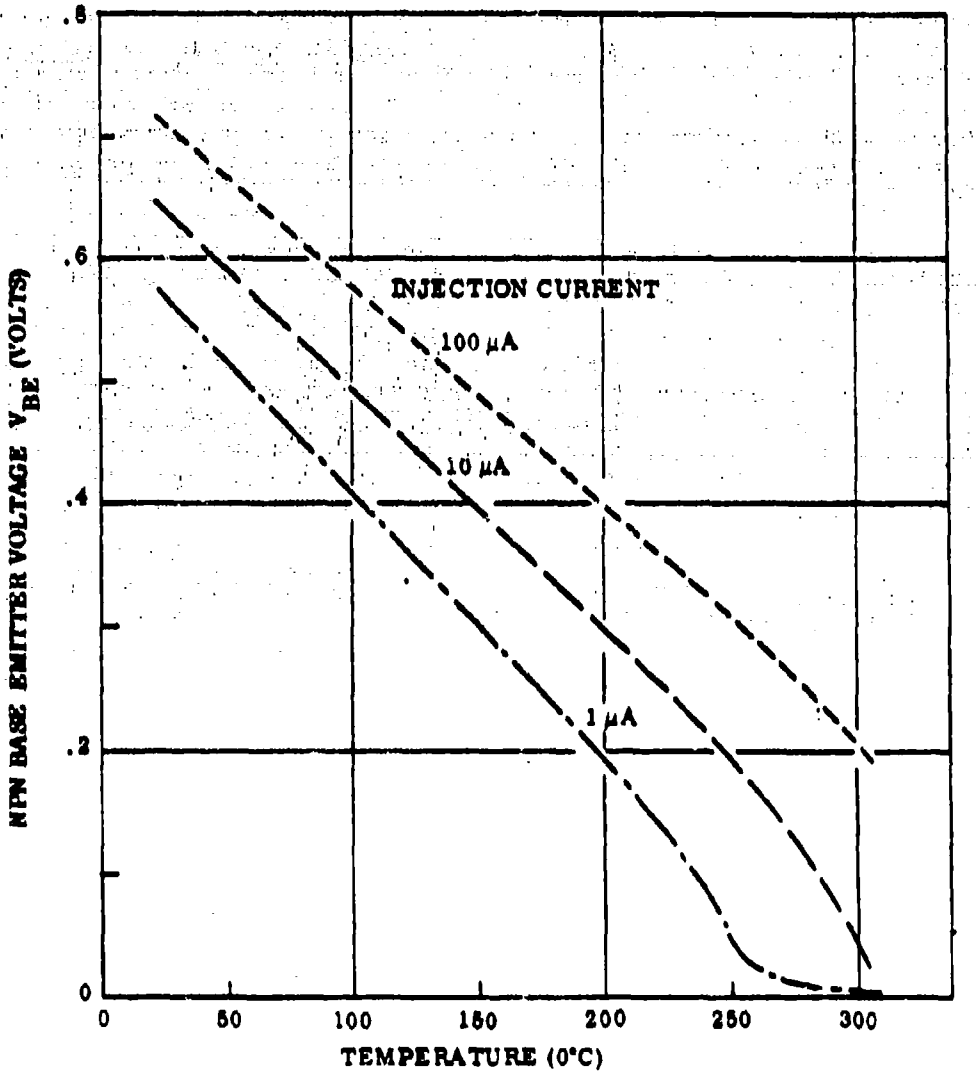


Figure 11. Measured NPN Base Emitter Voltage versus Temperature for Quad-A2 Cell

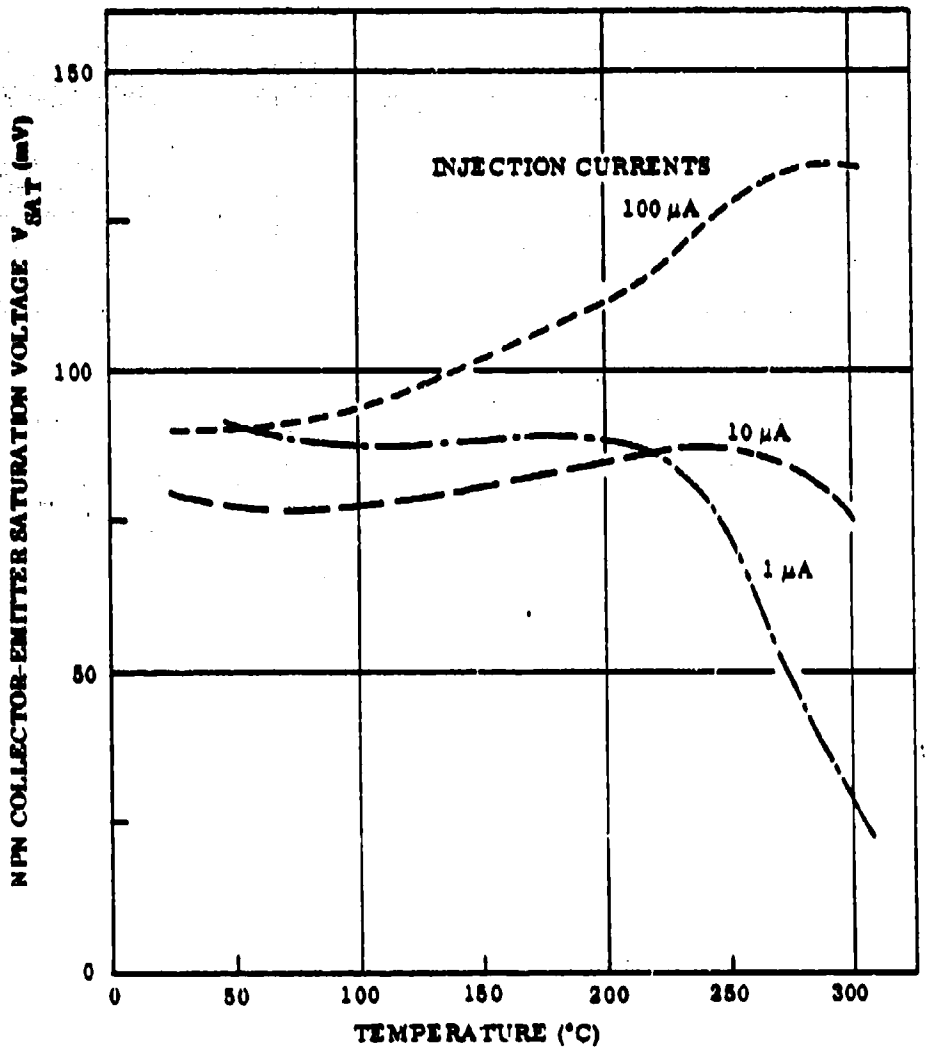


Figure 12. NPN Saturation Voltage versus Temperature for Quad-A2 Cell

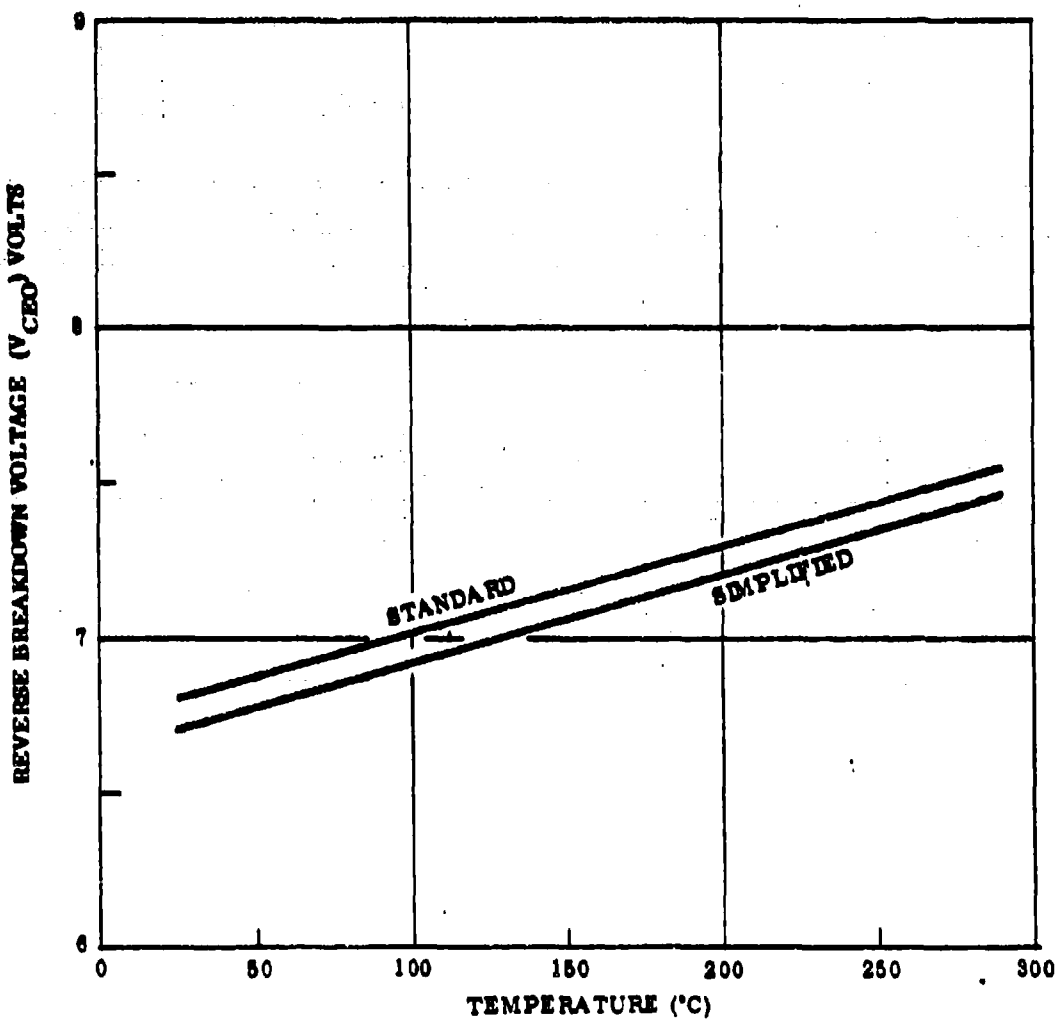


Figure 13. NPN Collector Breakdown Voltage (V_{CBO}) for the Standard and Simplified Linear Process

oscillator studies do not provide a complete description of the operating limits; they only provide an indication of effective gains greater than unity. Effective gain measurements indicate gain margins, and V_{BE} and V_{SAT} measurements provide voltage noise margins, both of which can be used to determine operating limits. The studies of ring oscillators and larger arrays of gates, such as code generators and flip-flops, provide an important additional bit of information; i.e. similar gates have similar ranges of operation independent of the size of the logic array. This implies that, at high temperatures, I^2L logic array operation does not cumulatively degrade as a function of the number of gates used in the logic. As a result, large gate arrays can be designed with confidence that they will operate under essentially the same conditions as a ring oscillator.