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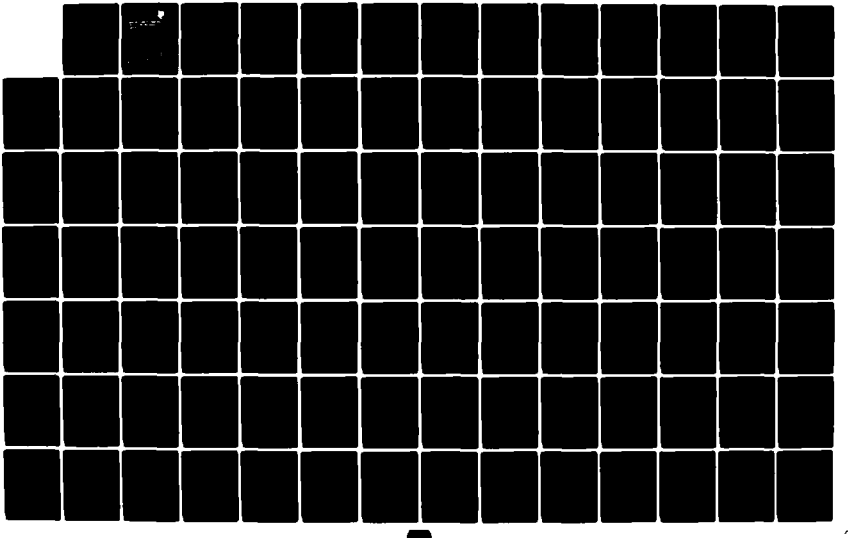

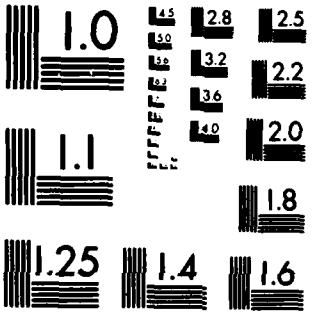

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BASIC EMC TECHNOLOGY ADVANCEMENT FOR C^3 SYSTEMS, Macromodeling of Digital Circuits

Southeastern Center for Electrical Engineering Education

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A NAND gate macro-model is developed using SPICE which allows for the complete simulation of the operation of the logic gate. The model derivation requires only external DC voltage and current measurements and logic delay times, but the model developed is shown to fully simulate the high-frequency response of the device as well, including the response of the device to interference in the 1-100MHz range.

A simpler SUPER*SCEPTRE NAND gate model is also presented, which effectively models the response up to normal switching speed limits. Also, a less complex SPICE modeling procedure is developed for the purpose of modeling large logic circuits in a minimum of computer time.

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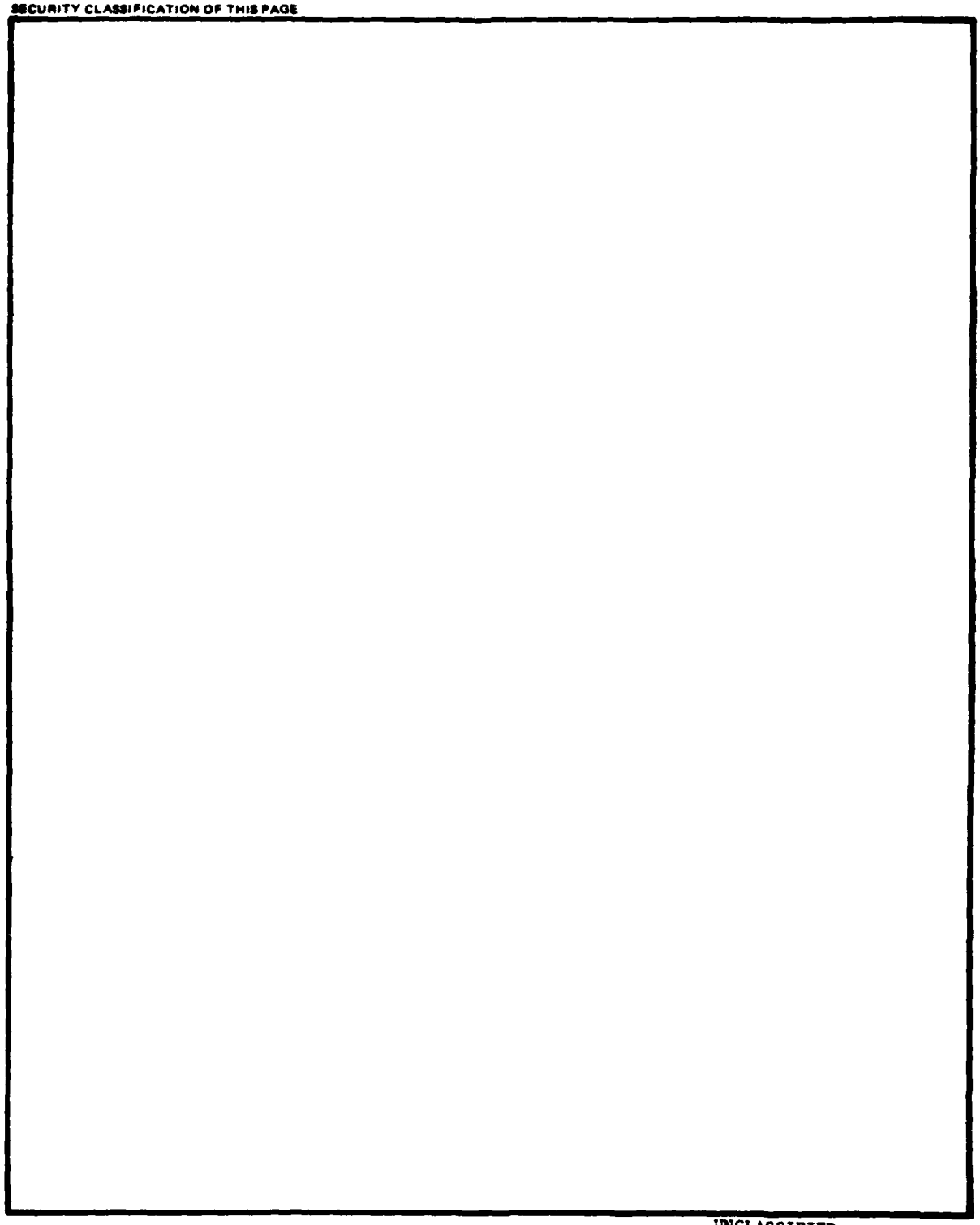

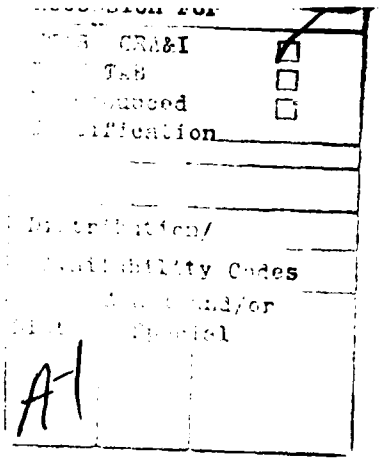

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INTRODUCTION

In designing a model for a circuit simulation program for a logic element such as a NAND gate, several approaches to the design are possible.

One method which could result in an excellent model of all phases of operation of the device would be to fully simulate every device on the chip. This would of course require extensive work, whether by knowledge of doping levels and other mask-level parameters of the chip's construction, by probing the chip, or via educated guesses at parameter values and trial-and-error manipulations to better fit the model to the device's response. This method has been successfully carried out on a 7400 TTL NAND gate[1] and the resulting discrete model will be used in this report for benchmark tests of the model developed here. Even if this type of model is constructed, in many cases it may be more model than is required -- that is, using five fully-qualified transistors plus additional diodes and resistors would

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[1] Alkalay and Weiner, 'Performance Degradation of a 7400 TTL NAND Gate due to Sinusoidal Interference', RADC-TR-80-257, August 1980 (A091745)

be a waste of computer time if only the logical NOT-AND function is required.

In simpler applications, the input/output voltage relationship could be approximated by a linear gain which saturates to the HI and LO output values. An extra stage could add an RC time constant to the response to simplistically model the rise and fall times. This type of analysis, while only a fair first-order model when built out of linear elements, can work quite well if fully tabular relationships are developed in a language such as SUPER*SCEPTRE (see Chapter 2).

The SPICE macro-model to be developed here falls somewhere between these two extremes. It was designed so that both the input stage and the output stage closely resemble their discrete counterparts, while the circuitry in between has been minimized. In this way, the current/voltage relationships at both ends remain very similar to the discrete version, as does the mechanism of signal propagation through from input to output. Thus, the SPICE macro-model yields considerably better responses to real-world external conditions, while the decreased complexity not only reduces CPU time but also allows solution for the internal model parameter values directly in terms of external measurements without the need for costly and time-consuming probing of the chip and multiple transistor characterizations.

It should be noted that the purpose of the topology to be developed here is to give the most accurate simulation of the device under all possible conditions -- including very high-frequency interference injected from any node (including power supply and ground) as described in reference [1] -- while developing the model only from externally measurable data. In this case, a considerable CPU time improvement is not possible, since three of the five internal transistors in the device are directly connected to external nodes of the device. Since they operate from cutoff, through the active region, and into saturation, they are most easily modeled as transistors.

In addition to the fully-qualified model developed for SPICE, a simpler model will be constructed for use in the SUPER*SCEPTRE simulation program which effectively models the device from DC up to normal switching speed limits.

Another look will then be taken in the final chapter of this report at developing a SPICE model of a device constructed from a large number of logic elements fabricated on a single chip. In this case, the overall complexity is such that a modeling procedure is developed based on minimizing the complexity and hence computer (CPU) time of the circuit while still maintaining the logical, input, output, and propagation delay characteristics.

1. SPICE NAND GATE MACRO-MODEL

DISCRETE NAND GATE OPERATION

In order to understand the internal operation of a NAND gate, and how the macro-model will be fitted to it, an analysis of the DC operation is presented here.

A Schematic for a 7400 TTL NAND gate is shown in figure 1. If either input is at its LO state (VIN <= 0.4V), then the base-emitter (BE) junction of that input transistor would be on, so the base voltage would be about 0.7V above the input voltage. The input current would therefore be (VCC-VIN-0.7)/R1, or about 1mA. The input transistor would attempt to turn on, but could not draw current out of the base of T2, so transistor T2 would be held in the OFF state. Similarly, no current is being supplied to T4's base, so it would also be off. The output will therefore be pulled high by T3 and D3. For small output currents, the output voltage will be two diode drops below the supply, so for VCC=5V, the output voltage is around 3.6V. The output impedance is equal to the sum of the bulk resistance of D3 and the resistance of R2 scaled down by T3's forward current gain (neglecting the dynamic resistance of the junctions).

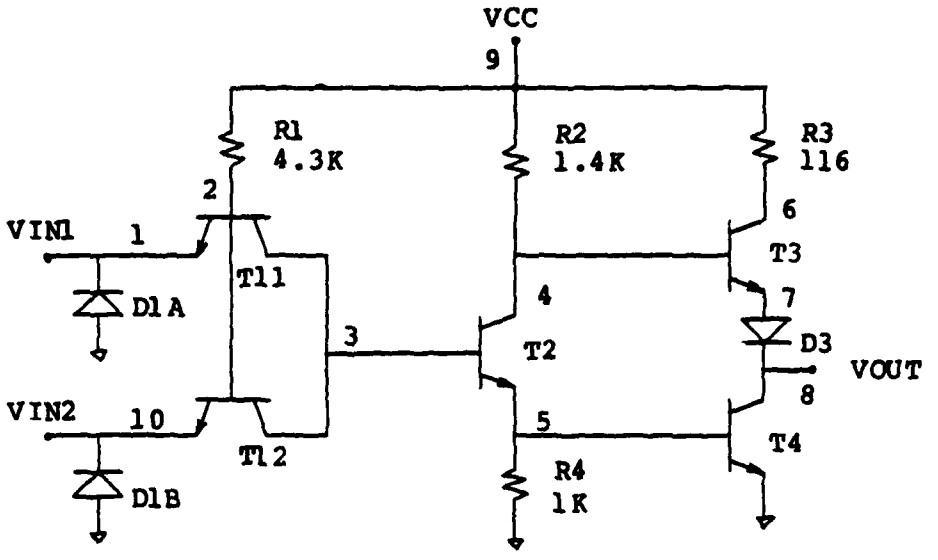


FIGURE 1: 7400 TTL NAND Gate Schematic

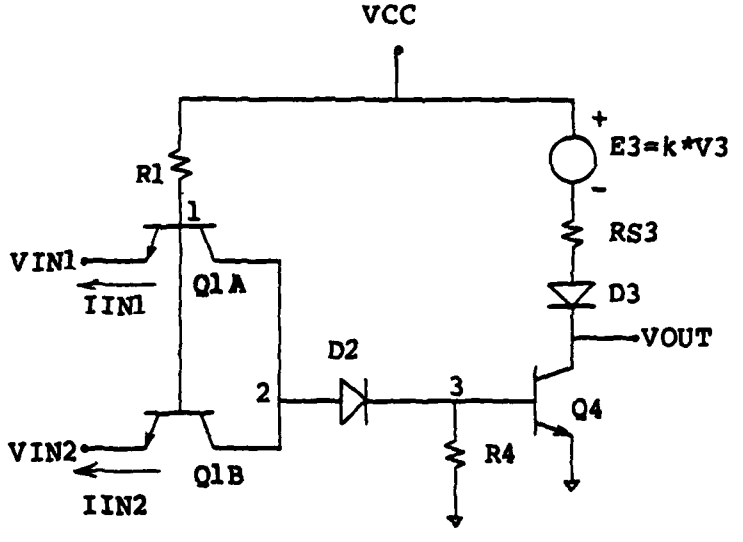


FIGURE 2: DC Equivalent Circuit

If a high input voltage is applied to both inputs, the BE junctions of both transistors would be turned off. Current would flow from VCC through R1, through the base-collector (BC) junction of T1, and on into T2 and T4. The input transistors would therefore operate in inverse-active region, drawing an emitter current equal to the inverse beta (BR) times the base current.* Since V(2) will be three diode-drops above ground, or about 2.2V, and typically BR=.02 or so, this results in a input current in this state of about IIH=14uA. Transistors T2 and T4 will be saturated, so the output voltage will be equal to VCE4sat, or about 0.2V. The output resistance in this state is essentially equal to the collector resistance of T4, or around 10 ohms.

In between these two regions of operation, T2 will pass through its active region while T4 is still considered off (that is, while IE2*R4<0.7V). T2 would therefore act like a linear amplifier with a gain of

$$K = -V(4)/V(5) = -R2/R4 = -1.4 .$$

The output voltage will then follow the voltage at node 4, two diode-drops below it.

As V(5) increases past 0.7V, corresponding to VIN around 1.5V, a small base current will flow into T4, turning it on and rapidly dropping the output voltage to the low state.

---

* The SPICE internal diode and transistor model parameters are explained in Appendix 1.

Since only a small base current is required, T2 will be in its active region and so its base current will be very small. Because of this, most of the current flowing in R1 will still be flowing out the input to the device.

A few more tenths of a volt rise in the input voltage, however, will rapidly switch the input current into T2, saturating it and T4. The rate at which VIN turns off IIN is equal to the input resistance at this point, which equals the sum of dynamic resistance of the four junctions (BE1, BC1, BE2, and BE4) and the bulk base resistance of T4 scaled up by the saturated current gain of T2.

MACRO-MODEL FOR DC OPERATION

A reasonable DC equivalent model is shown in figure 2. This model assumes the output current in the HIGH state is not too large so that Q3 does not saturate. Note that both input and the output transistor have been preserved, but transistors T2 and T3 have been reduced to a single diode each, with the approximate linear gain coefficient replaced by a linear dependent source of E3=k*V(3). Diode D3 in the device has also been merged with the B-E junction diode of T3 so that the model's D3 should have a junction coefficient of N=2 to model the two junctions in series. RS3 should be the scaled value of the device's R2 as seen from the emitter of T3.

Since device T2 has been replaced by model D2, the for-

ward active current gain will no longer be present. Hence the current flowing to R4 and the base of Q4 will be correspondingly less, so that R4 and BF4 must be scaled up by a factor of approximately BF2.

FULLY QUALIFIED MODEL

In order to completely model the device, its transient response must also be considered. When the input to the discrete device is switched from HI to LO, transistor T1 will momentarily switch into the forward active region, rapidly discharging T2. This is the primary reason T1 must be preserved in the model -- the forward current gain is only present under transient response -- hence a less-accurate model could be constructed with Q1 replaced by diodes, but this would give a less realistic response during switching, especially at higher frequencies.

T4 is then left to discharge through R4 after D2 turns off, so the primary cause of the propagation delay, Tpd(L-H) is the storage time constant of Q4, TR4. It could be specified alone to sufficiently model this propagation time. However, when Q4 would turn off, VBE4 would immediately step to zero resulting in integration problems. Specification of reasonable values for the forward transit time TF4 and emitter junction capacitance CJE4 to roughly model the initial transient VBE4 waveform results in much smoother integration steps during simulation.

Switching VIN from LO to HI (discrete) will rapidly cut off the input BE junction. Transistor T2's junction capacitances, CJE and CJC, must then be charged through R1. In the model, the substrate capacitance of Q1's collector, CCS, may be used to lump together the absent Q2's effects with its own, giving the appropriate charging time. The capacitance in diode D2 is scaled down from its typical value, since D2's current has been scaled.

To further match the device's capacitive loading characteristics, a typical junction capacitance, CJO, may be placed on diodes D2 and D3, and a transit time, TT, on diode D2.

The completed macro-model topology is shown in figure 3. One change has been made to simplify the SPICE analysis by removing a node from the circuit. A quasi-Nortonization of E3 with D3 and RS3 is possible, since the diode is normally always on, acting mostly like its series resistance (Note that we are using G3 as the current source name and g3 as the linear coefficient). Although the diode could be turned off by a voltage transient at the output in its HI state, no problems would be encountered since E3=0 yields IG3=0 in this state anyway. Of course, RS3 would be specified in SPICE as the series resistance of diode D3.

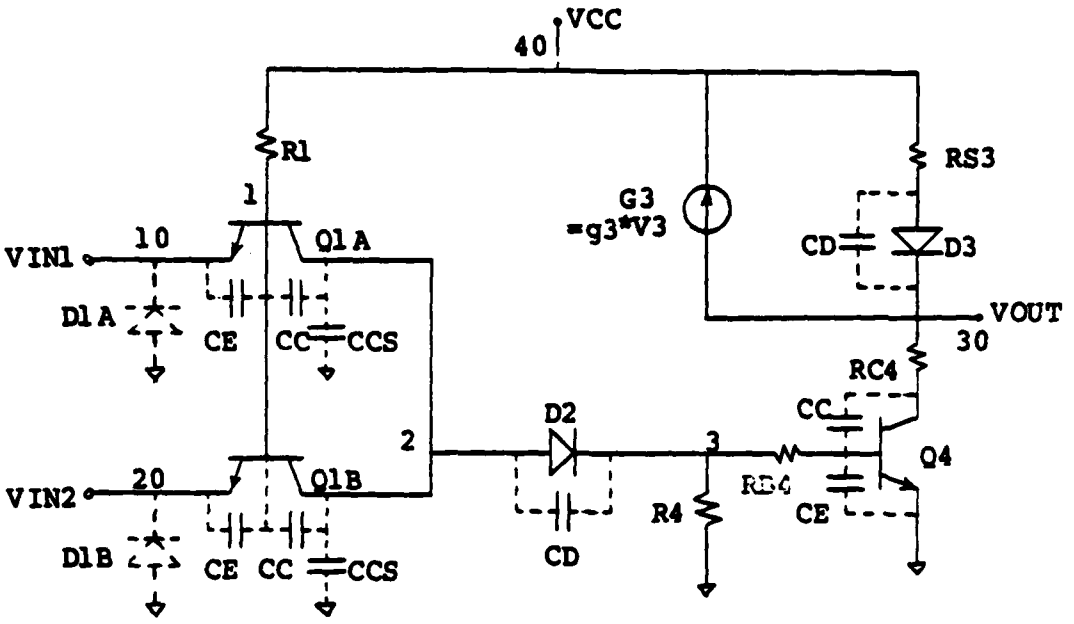


FIGURE 3: SPICE NAND Gate Macro-Model

ACTUAL MACRO-MODEL DETERMINATION

In this section, relationships will be developed to convert NAND gate measured data into macro-model parameters, resulting in a model equivalent to the discrete model found in reference [1] (circuit in figure 1, listing in table A2 of Appendix 3), using the topolgy created in the preceding section (figure 3). In figure 4 are sketches of typical NAND gate output voltage and input current vs. input voltage curves, along with markings to indicate three points at which data will be used to characterize the device:

a, around the corner of the output voltage curve;

b, around the center of the output voltage dropoff;

c, around the center of the input current dropoff. Note that the value VOX is defined in figure 4b to be the value of the output voltage extrapolated from the linear region to the given value of VIN. Data taken from the device is listed in table 1.

First, the value of R1 is simply the slope of the input characteristic at VIN=0, so

(1) R1 = 1/m1 = 4.3Kohm

In figure 5 is an expanded view of the input to the NAND gate showing the internal elements in the transistor model. From the basic defining equations of the transistor and the circuit topology we have the following relationships:

(2) JB1 = (IS1/BF1)*exp(VBE1/VT)

(3) JD1 = (IS1/BR1)*exp(VBC1/VT)

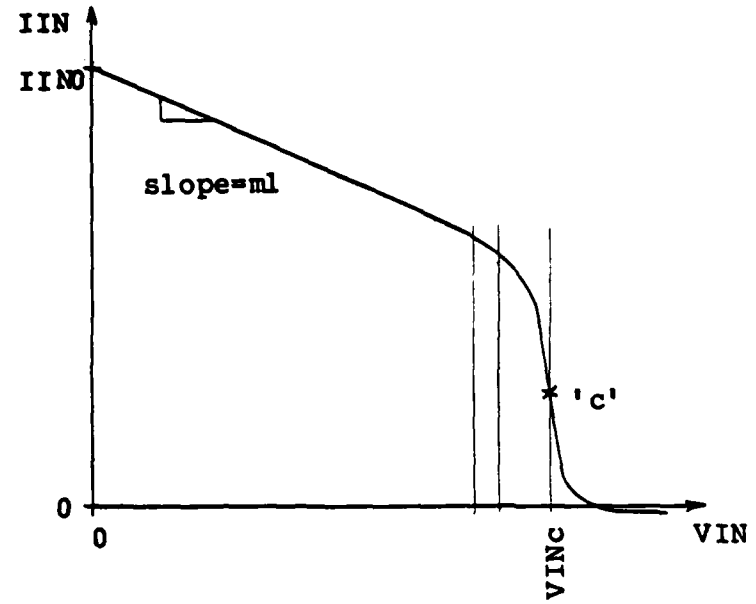
(4) JF1 = BF1*JB1

(5) JR1 = BR1*JD1

(6) ID2 = I1-IIN = IS2*exp((V2-V3)/VT)

Note that all internal SPICE model parameters are being suffixed by the number of the transistor they apply to, so BF1 is the forward beta of transistor Q1, IS2 is the saturation current of diode D2, etc.

When the input to the NAND gate is high (VIN>2.4V), the input transistor Q1 will be in inverse active mode, so JD1 will equal I1, JR1 will equal -IIN, and V1 will be three diode-drops above ground potential (roughly 2V), so



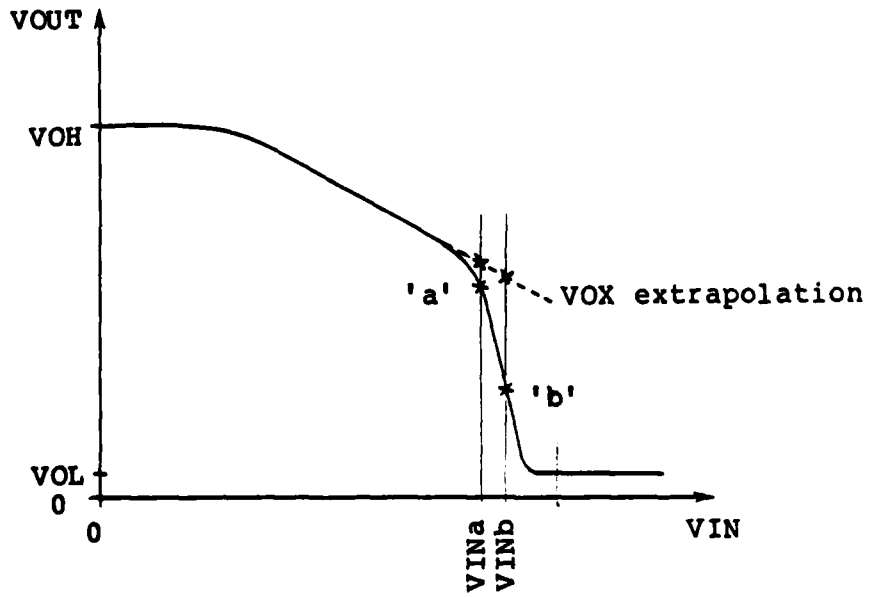


FIGURE 4: DC Curves Used to Specify Data Values
(a) Input Characteristic
(b) Output vs. Input Voltage

TABLE 1: Data from Measurements on Device-Level Model

ROL = 10 ohms
ROH = 140 ohms
VOH = 3.47V @ RL=10Kohms
VOH'= 2.59V @ RL=400ohms
VOL = 0.2V (spec typical)
IIN0= 0.99mA
1/m1= 4.3Kohms

	ZERO	a	b	c	HIGH
VIN	0.000V	1.400V	1.500V	1.700V	5.000V
IIN	.990mA	.641mA	.603mA	.337mA	-.014mA
VOUT	3.470v	2.325V	1.150V	.063V *	.063V *
VOX	-	2.50V	2.39V	-	-

* Note, typical value of VOL=0.2V will be used in analysis.

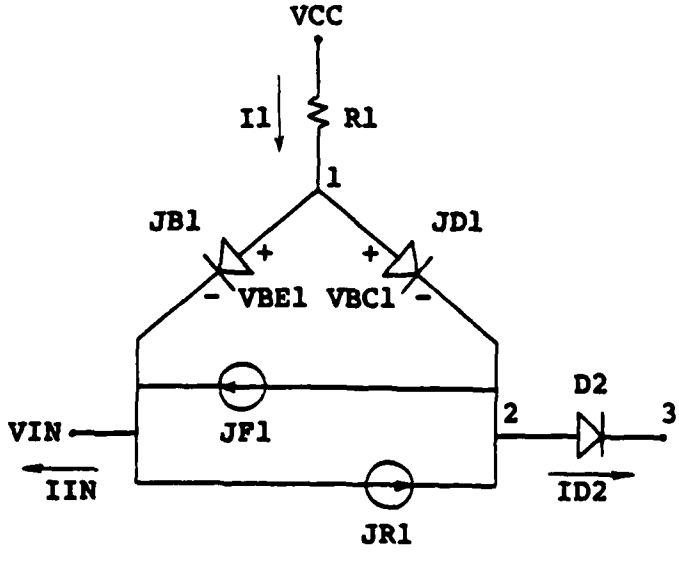


FIGURE 5: Input Stage Using Internal Transistor Representation

(7) BR1 = JR1/JD1 = -IIN/((VCC-V1)/R1)
= .014mA*4.3K/(5V-2V) = .02

Since Q1 cannot enter forward active region at DC (it would require negative current through D2), the value of BF1 will not noticeably affect the DC operating characteristics. Further, the forward active region of Q1 is only attained under transient response when the input switches from high to low, at which time the inverse current serves to rapidly discharge D2, stopping the base drive to Q4 so that it will also turn off. At the output, however, the dominant response time will be that of the storage time of Q4, since any BF1 from 0.1 to 10 will cause sufficient current to discharge D2 in just a few nanoseconds, compared to the 10ns or so storage time of Q4. Therefore the value used for BF1 is not critical to the end-to-end response, and may be chosen as a typical value for gates of this type of BF1=0.3.

Since BR1 << BF1, we can approximate

(8) JB1 = IIN/(1+BF1)

Substituting into equation 2 and solving for IS1, the saturation current of transistor Q1, gives

(9) IS1 = (BF1/(1+BF1))*IIN0*exp(-(VCC-R1*IIN0)/VT)
= (.3/1.3)*.99mA*exp(-(5-4.3K*.99m)/.02585)
= 7.52E-17 Amps.

We can now solve for V1 at each input point (a, b, and c) by solving equation 2 for VBE and again substituting equation 8 into it, to give

(10) $V1 = VIN+VBE1 = VIN+VT*\ln(IIN*BF1/(IS*(BF1+1)))$.

At each point, the current through diode D2 can be found using the first part of equation 6 with the current through R1 defined as its voltage divided by its resistance:

(11) $ID2 = I1-IIN = (VCC-V1)/R1-IIN$.

Again using equation 8 for JB1, we can find JD1 by applying Kirchoff's Current Law (KCL) at node 1:

(12) $JD1 = IR1-JB1 = (VCC-V1)/R1-IIN/(1+BF1)$.

Now using equation 3, solved for VBC1, we can find the voltage at node 2 at each data point in terms of JD1 as

(13) $V2 = V1-VBC1 = V1-VT*\ln(BR1*JD1/IS1)$.

The values of V1, ID2, and V2 at each of the defined data points are listed in table 2.

When the NAND gate has a LOW input (VIN<0.4V), no current will be able to flow through diode D2 to R4 and Q4, so V3 will be zero, transistor Q4 will be cutoff, and IG3 will be 0mA. The resulting output stage is shown in figure 6. The following relationships are present in figure 6:

(14) $VD3 = VCC-VOH$

(15) $ID3 = VOH/RL = IS3*\exp((VD3-RS3*ID3)/2VT)$

Diode D3 can be characterized from data taken in the HIGH output state for two different sized load resistors. Equations 14 and 15 can be used to find the values of the actual diode current and voltage in each case. Using the unprimed values to denote measurements with large load resistance (10Kohms) and primed values for fully loaded measurements

TABLE 2: Computed Internal Voltages and Currents

	a	b	c
V1	2.132V	2.230V	2.415V
ID2	.026mA	.041mA	.264mA
V2	1.497V	1.594V	1.763V
V3	0.712V	0.797V	0.918V
IG3	7.19mA	8.05mA	9.27mA

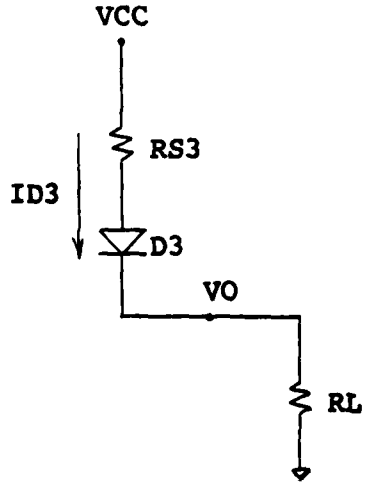


FIGURE 6: Output Stage in the HIGH State

(400ohms) we can solve equation 15 for IS3 and RS3 by using both data points as two equations in two unknowns, resulting in

(16) RS = (VD3'-VD3-2VT*ln(ID3'/ID3)) / (ID3'-ID3)
= (2.41-1.53-2(.02585)*ln(6.48/.347)) / (6.48m-.347m)
= 119 ohms,

and

(17) IS3 = ID3 * exp(-(VD3-RS3*ID3)/2VT)
= .347m * exp(-(1.53-119*.347m)/(2*.02585))
= 1.08E-16 .

The values of VOX represent what would happen if Q4 were not to turn on, and the linear region was extended downward. This is of interest because in the model G3 does stay linearly related to V3 even after Q4 turns on, hence the output while Q4 is crossing through its active region can actually be looked at as a superposition effect of IG3*RS3 with RS3*IC4. Using this relationship we can compute IG3 at point 'b' as follows:

(18) IG3b = (VCC-VOXb-2VT*ln(IG3b/IS3)) / RS3
= (5-2.39-2(.02585)*ln(IG3b/1.08E-16))/ 119
= (8.9mA)
= 8.055mA on multiple iteration.

Several things should be noted here. Any time a measurement that will be made at several different input voltages is mentioned, it is suffixed by the letter of the point in question (a, b, or c). Also, this expression contains a

weak function of itself -- that is, an initial guess of IG3b=1mA is sufficient to get a good approximation of IG3b. This approximation can then be plugged back in to get the result in a few more iterations.

Now, when Q4 begins to turn on, the current drawn through D3 will rapidly increase as VD3 increases, so that the dynamic resistance of the diode junction will be significantly less than its series resistance. In this range, we can approximate D3 by the form,

VD3 = VD3on + ID3*RS3 , where

VD3on = 2VT * ln(IG3b/IS3)

= 2(.02585)*ln(8.055m/1.08E-16)

= 1.651V

We can now find IG3a to be

(20) IG3a = (VCC-VOXa-VD3on)/RS3

= (5-2.50-1.651)/119

= 7.13mA.

At point 'b' Q4 is in its forward active region. In the discrete model, Q2 (now being modeled by D2) would also be in its active region, thus the voltage drop across the two base-emitter junctions would be approximately equal. In this model we can therefore let VBE4b=VD2b or

(21) V3b = V2b/2 = .797V .

The transconductance constant of dependent source G3 can now be computed directly as

(22) g3 = IG3b/V3b = 8.055mA/.797V = 10.1mA/V .

Equation 5 can now be solved for the saturation current of

diode D2:

(23) IS2 = ID2b*exp(-V3b/VT)

= .041mA*exp(-.797/.02585)=1.67E-18 Amps.

We can now compute two sets of data to complete table 2:

(24) V3 = V2 - VT*ln(ID2/IS2) and

(25) IG3 = g3*V3 .

When transistor Q4 is on, a significantly more complicated output topology is present, as is shown in figure 7.

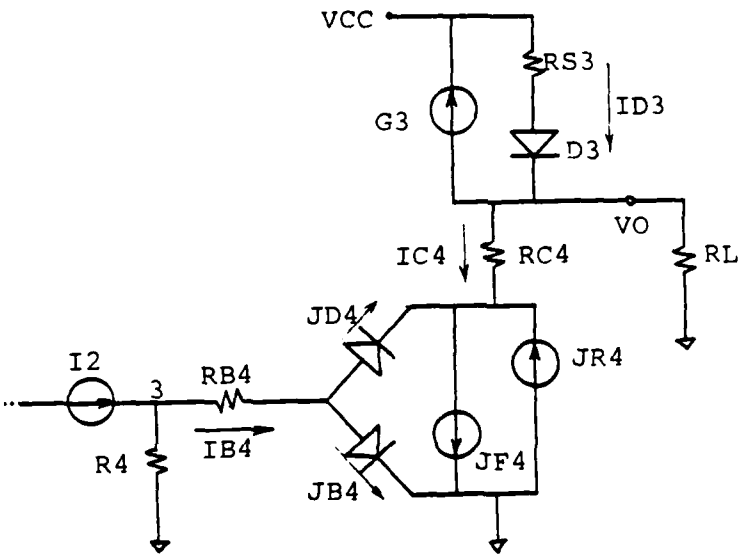


FIGURE 7: Fully Qualified Output Stage on NAND Model

The following relationships are apparent in this topology:

(26) IB4 = ID2-V3/R4

(27) ID3 = (VCC-VO-VD3on)/RS3

(28) IC4 = ID3-IG3-VO/RL

(29) JB4 = (IS4/BF4)*exp(VBE4/VT)

(30) JD4 = (IS4/BR4)*exp(VBC4/VT)

(31) JF4 = BF4*JB4

(32) JR4 = BR4*JR4

Resistor R4 can be found at 'a' since the base current of Q4 is negligible at that point:

(33) R4 = V3a/ID2a = .712/.026m = 27.4K

At point 'b', Q4 is in its active region, so JD4=JR4=0, yielding IB4=JB4 and IC4=JF4. Using equations 26 through 28, we have

(34) IB4b = ID2b-V3b/R4

= .041m-.797/27.4K = .0119mA and

(35) IC4b = (VCC-VOb-VD3on)/RS3-IG3b-VOb/RL

= (5-1.150-1.651)/119-8.055m-1.15/10K = 10.3mA .

The forward beta of Q4 is found directly using equation 31:

(36) BF4 = IC4b/IB4b = 10.3m/.0119m = 865 .

Neglecting the voltage drop produced by the small active-region current flowing in RB4, we can approximate VBE4b=V3b so that the saturation current can be found from equation 29:

(37) IS4 = IC4b*exp(-V3b/VT)

= 10.3m*exp(-.797/.02585) = 4.20E-16 Amps.

If we again apply equations 26-28, this time at point 'c', we can find the base and collector currents there to be

(38) IB4c = ID2c-V3c/R2

= .264m-.918/27.4K = .230mA and

(39) IC4c = (VCC-VOc-VD3on)/RS3-IG3c

= (5-.20-1.65)/119-9.27m = 17.2mA .

Since Q4 is saturated at this point, and we assume BF4>>BR4, we can approximate

(40) JB4c = IC4c/BF4 = 17.2m/865 = .0199mA ,

and the inverse diode, JD4, would draw the remainder of the base current:

(41) JD4c = IB4c-JB4c = .230m-.0199m = .210mA .

The base-emitter internal voltage can now be found from equation 29:

(42) VBE4c = VT*ln(BF4*JB4c/IS4)

= .02585*ln(17.2m/4.20E-16) = .810V .

So, the base bulk resistance of Q4, RB4, can be computed since its voltage and current are now both known:

(43) RB4 = (V3c-VBE4c)/IB4c

= (.918-.810)/.230m = 470 ohms.

The bulk collector resistance, RC4, is just equal to the output resistance in the LOW state, since the transistor's dynamic on-resistance is typically very small when the device is in saturation, so

(44) RC4 = ROH = 10 ohms.

The base-collector voltage can be expressed in terms of the base-emitter and output voltages as

(45) VBC4c = VBE4c-VOc+IC4c*RC4

= .810-.20+17.2m*10 = .782V ,

and the inverse current gain, BR4, can now be computed by solving equation 30:

(46) BR4 = (IS4/JD4c)*exp(VBC4c/VT)

= (4.20E-16/.210m)*exp(.782/.02585) = 27 .

If the inputs to the NAND gate are being driven directly by other NAND gates, or by any signal that always stays above ground potential, the shunt diodes on each input could be deleted from the model (to save CPU time), since they would never turn on. However, if significant swings of input voltage below -1V are possible (ringing during switching, for instance), the input diodes should be included in the model. The series resistance of this diode, RS, can be measured as the input resistance of the NAND gate at the rated maximum input current. The other diode parameters can be defaulted, since the rest of the NAND gate will dominate the response for input currents under 1mA. For this device, reasonable values for this diode are RS=60 ohms, IS=1E-16 amps, and N=1.

TRANSIENT RESPONSE PARAMETERS

The propogation delay times of the model are each dependent on just a single parameter within the model, so that fitting the response to desired on- and off-delay times is not a complicated procedure.

The low-to-high output propagation delay time, Tpd(LH), is controlled by the storage time constant of transistor Q4, TR4. A good initial guess for TR4 is

(47) TR4 = Tpd(LH)/BF4 = 12ns/27 = 440ps .

Similarly, the high-to-low output propagation time, Tpd(HL), is controlled by the substrate capacitance on transitor Q1, CCS1 (actually twice this for a two-input gate). Using the current-voltage relationship of this capacitor, a suitable guess for CCS1 is

(48) CCS1 = IC/(dV/dT)/(number-of-inputs)
= ID2on/(dVC/Tpd(HL))/2
= .6mA/(1V/12ns)/2 = 3.5pF .

These values can then be modified proportionately to the on- and off-delay times. Final values for this device came out to be TR4=200ps, CCS1=4pF.

OTHER INTERNAL TRANSIENT RESPONSE PARAMETERS

The rest of the internal capacitances are not at all critical to the operation of the model, but need to be included for smooth and realistic simulation of the transient response. The capacitances which occur across the input and output could be adjusted as desired to more closely match the capacitive loading characteristics, but the effects are rather insignificant compared to the large-signal response of the device, so simple typical values are used here.

The junction capacitances of diodes DI and D3, and both junctions of transistor Q1, all are directly equivalent to actual junctions within the device and therefore the choice of a typical value of 1pF for CJOI, CJO3, CJE1, and CJC1 is sufficient for the model. Since the current flowing through

D2 and into Q4 has been scaled down by the forward current gain of transistor Q2 in the discrete device, the junction capacitances of both need to be lowered appropriately. A value of .02pF was therefore assigned to CJO2 and CJE4.

Finally, the diffusion capacitance in D2 and the base-emitter junction of Q4 need some reasonable values. The standard form for the diffusion capacitance in a diode junction is of the form

(49) CD = TT*ID/VT

where, TT is the diffusion capacitance time constant, ID is the junction current, VT = 25.85mV at room temperature, and CD is the diffusion capacitance value (see Appendix 1). If we choose to specify the maximum value of the diffusion capacitance at fifty times the junction capacitance value we get

(50) TT2 = CD*VT/ID2on

= (.02pF*50)*.026/.6mA = 40ps.

And, for Q4, to put the forward and reverse time constants into similar relative sizes we can specify

(51) TF4 = TR4*(BR4/BF4)

= 200ps*(27/865) = 10ps.

None of these capacitances are critical to the operation of the model, but inadvertently large values for them can slow down the rise and fall times of the output as would be expected when too much capacitance is present. For this reason, the values of the noncritical capacitance parameters

on D2 and Q4 were purposely chosen on the light side to minimize this risk.

The completed SPICE model, corresponding to the topology shown in figure 3 (page 10) is listed in table 3.

TABLE 3: SPICE Macro-Model Listing

```
.SUBCKT NAND   10 20  30  40
*7400 TTL GATE: INPUTS OUT VCC
.MODEL DI    D(IS=1E-16 RS=60 CJO=1PF)
.MODEL T1 NPN(IS=7.52E-17 BF=.3 BR=.02
+              CJE=1PF CJC=1PF CCS=4PF)
.MODEL D2    D(IS=1.67E-18 CJO=.02PF TT=40PS)
.MODEL D3    D(IS=1.08E-16 N=2 RS=119 CJO=2PF)
.MODEL T4 NPN(IS=4.20E-16 BF=865 BR=27 RB=470 RC=10
+              TF=10PS TR=200PS CJE=.02PF)
*
Q1A 2 1 10 T1
Q1B 2 1 20 T1
DIA  0 10  DI
DIB  0 20  DI
R1  40 1   4.3K
D2   2 3   D2
R4   3 0   27.4K
Q4  30 3 0 T4
G3  30 40  (3,0)  10.1MA/V
D3  40 30  D3
.ENDS
```

2. SUPER*SCEPTRE NAND GATE MODEL

The SUPER*SCEPTRE simulation program is much more generalized than the SPICE2 program. It allows for specification of any relationship to define element values, whether piece-wise linear, a mathematical expression, or fortran subprogram, as functions of any voltages, currents, or user-defined parameters. Also included are mechanical and logical elements as well. (The simple DC NAND model in the logic family could be modified and extended for this use, but it is easier just to create a new model).

Due to the complexity involved, a SUPER*SCEPTRE analysis using a translation of the SPICE NAND gate model, for example, would take at least an order of magnitude more computer time for analysis, and would not be at all worthwhile for use in multiple-gate circuits.

On the other hand, very simple piecewise-linear relationships can be used to model the DC input, transfer, and output relationships, and an extra RC stage with appropriately nonlinear capacitance can neatly model the switching response.

DC CHARACTERISTICS

In figure 8 is a topology for a SUPER*SCEPTRE NAND gate model. Current sources JA and JB model the DC input current vs. voltage relationship, using the piece-wise linear format shown in figure 9(a). Voltage source E1 is dependent on the minimum of the two input voltages, VJA and VJB, by the output to input voltage characteristic shown in figure 9(b). Note that at DC, VC1 will equal E1 and so the output voltage source, EO=1*VC1, will indeed equal to E1. Resistance RO is a tabular function of EO: At EO<=0.2V, corresponding to a low output (discrete T4 saturated), RO=ROL=10ohms; while at EO>=2.4V, which is the voltage just before Q4 turns on, RO=ROH=140ohms.

Capacitances CA and CB are constant-valued 2pF capacitances included at the input to better model the input impedance.

TRANSIENT CHARACTERISTICS

Capacitor C1 is a nonlinear function of the voltage difference between E1, the DC output level corresponding to the present input, and VC1, the actual output voltage level. A sketch of a typical response curve and the tabular relation used for C1 is given in figure 10. The shape of this relationship -- minimum at DC, maximum capacitance after a step change in voltage (i.e., maximum current) -- makes C1 behave like a transistor diffusion capacitance, giving the storage time effect desired.

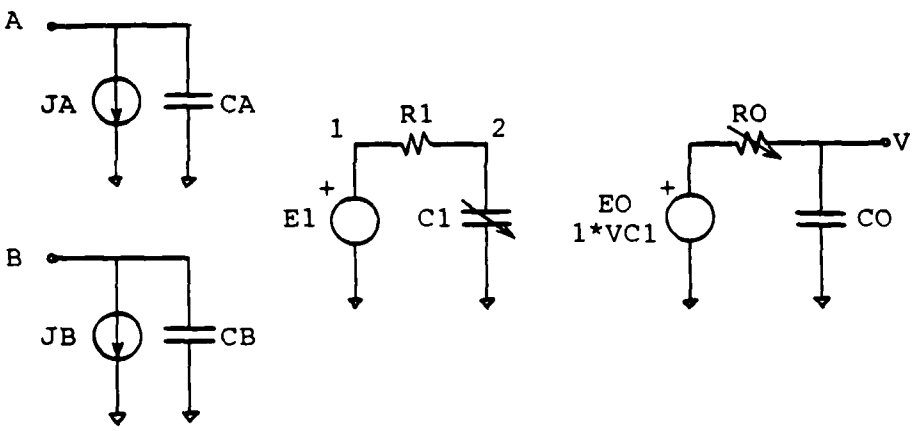


FIGURE 8: SUPER*SCEPTRE NAND Gate Model

The transient response due to this capacitance can be analyzed in the following manner. When the minimum input voltage swings from LO to HI, E1 will change immediately from its HI to LO state, before VC1 discharges substantially. C1 will therefore have stepped to its maximum value, modeling a stored charge equal to the area under this C-V curve (figure 10b). If the large triangular area is 1V wide, and R1 is 1 ohm (so the input voltage = VR1 = current), then the charge stored can be expressed as

Q = (Cmax*V)/2 = I*T, which becomes

(Coff*1V)/2 = 3.3V/1ohm*Toff or

(52) Coff = 6.6*Toff, and similarly,

Con = 6.6*Ton.

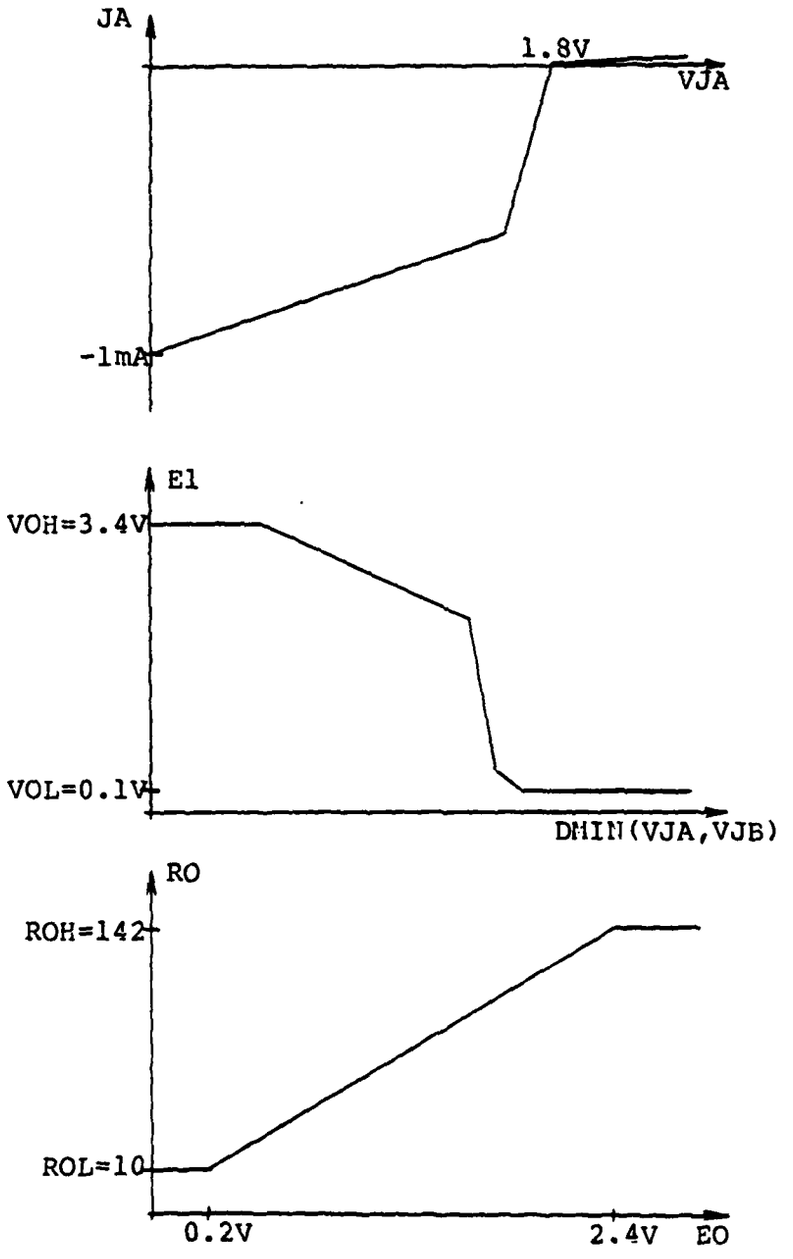
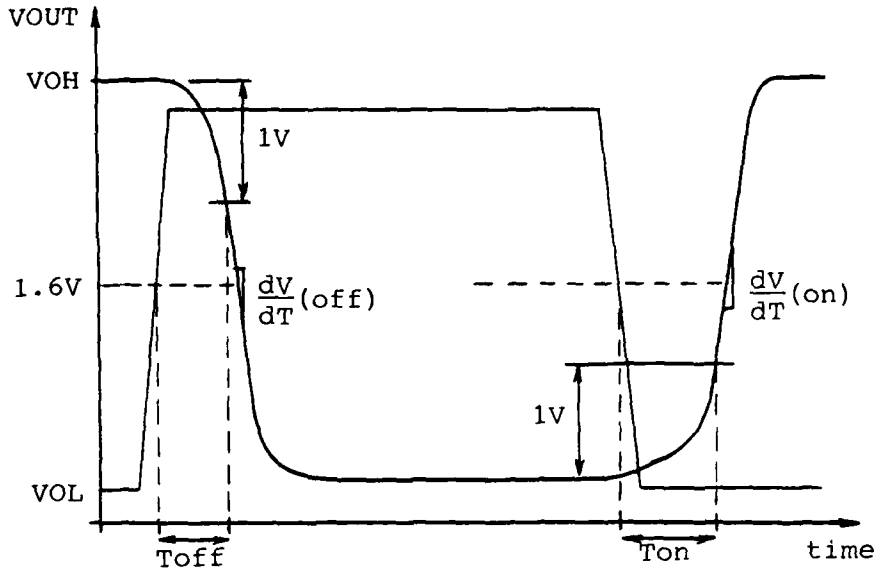


FIGURE 9: Tables Defining DC Characteristics
(a) Input Characteristic
(b) Output vs. Input
(c) Output Impedance



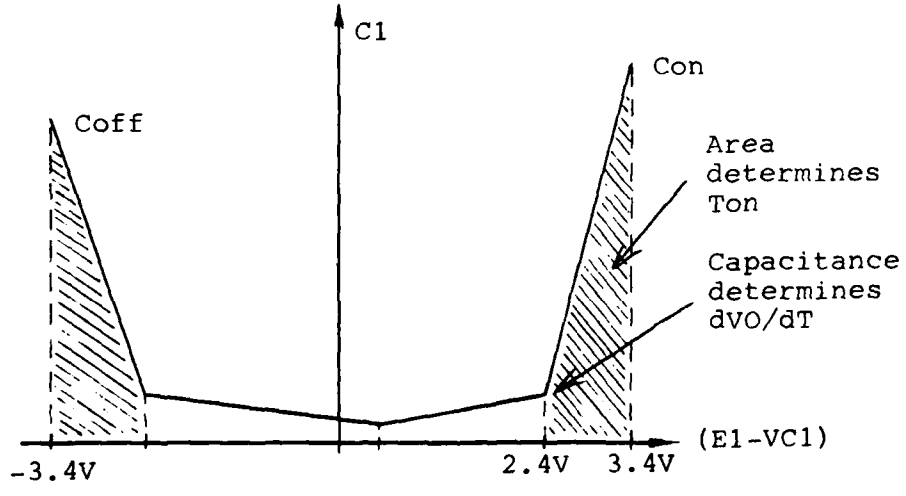


FIGURE 10: Modeling of the Transient Waveform
(a) Typical Transient Response
(b) Tabled Capacitance

The capacitance left at the point just after either large triangular area will be directly related to the rate of change of the output voltage by the relation

(53) $C = I/(dV/dT) = 2.3/(dV/dT)$.

This value should continue to decrease to a small value (C1(0)=1nF for a 1ns time constant) as the voltage approaches zero. In the particular case modeled here, the slopes at the 1V response points in both directions were about the same, but the rising output waveform responded faster toward the end of the response. To adapt to this, the center minimum was displaced by 0.5V toward the positive side to unbalance the responses appropriately.

Finally, capacitance CO was added from the output node to ground so that, in the absence of a capacitive load, a state variable would still be present so that the nonlinear output resistance RO could be integrated upon without computational delays occurring. A value of 1E-20 is chosen for CO so that after the initial voltage level is attained, its currents will be so far under the error tolerance of the integration routine that it would not effect (i.e., slow down) the analysis. Implicit integration must of course be used to handle the large time constant spread caused by CO.

The completed model is shown in table 4.

TABLE 4: SUPER*SCEPTRE Model Listing

```
MODEL NAND  (A-B-V-G)
 5V 7400 SERIES: 2IN/OUT/GND
 DEV. BY RON VOGELSONG FOR USF EE DEPT, SEPT 1982
ELEMENTS
 JA, A-G = DIODE TABLE I
 CA, A-G = 2E-12
 JB, B-G = DIODE TABLE I
 CB, B-G = 2E-12
 E1, G-1 = TABLE V (PV)
 R1, 1-2 = 1
 C1, 2-G = TABLE C (PC)
 EO, G-3 = XO(1*VC1)
 RO, 3-V = TABLE R (EO)
 CO, V-G = 1E-20
DEFINED PARAMETERS
 PV = XV(DMIN1(VJA,VJB))
 PC = XC(E1-VC1)
FUNCTIONS
 TABLE I = 0,-1E-3, 1.61,-.6E-3, 1.81,0, 5,14E-6
 TABLE V = 0,3.5, .57,3.5, 1.43,2.4, 1.56,.2,
           1.64,.1, 5,.1
 TABLE C = -3.4,70E-9, -2.4,6E-9, .5,1E-9, 2.4,6E-9,
           3.4,80E-9
 TABLE R = 0,10, .07,10, 2.4,142, 5,142
```

3. COMPARISON OF DC AND TRANSIENT RESPONSES

In this chapter, the three models (device-level, SPICE macro-model, and SUPER*SCEPTRE model) will be compared at DC and under transient analysis. The tests were performed with a full rated load equivalent to a fan-out of 10 gates. The output waveform was also checked under a light loading of 10Kohms + 2pf. Listings of the test circuits used are given in Appendix 3.

DC RESULTS

In figure 11 is a plot of the DC output vs. input voltage for a NAND gate under full load, and in figure 12 is the same with light load for each of the models. The three curves line up quite closely, with the exception of a slight difference in the low output voltage value, VOL, under light load, due to the differing values chosen, and the obvious sharp corners on the SUPER*SCEPTRE response, due to the direct piece-wise-linear representation used. During transient analysis, these sharp edges would of course be smoothed by the capacitances present to give a more natural response.

The input current vs. voltage characteristic is seen in figure 13. Again the curves show a good overall fit. The SPICE macro-model actually has somewhat less slope in the 1.6V-2V interval, but crosses around point 'c' due to the curve-fit method used. The SUPER*SCEPTRE model again shows the sharp corners at DC, but matches the slopes quite well.

Because the SPICE macro-model closely resembles the discrete in operation, the voltages at the three internal nodes of the macro-model can be directly compared to the associated values in the discrete model. In figures 14-16 are plots of the macro-model's internal voltages, V1, V2, and V3, and the associated discrete model nodes (actually nodes 2, 3, and 5 in the discrete model in figure 1), showing good overall fit in each case.

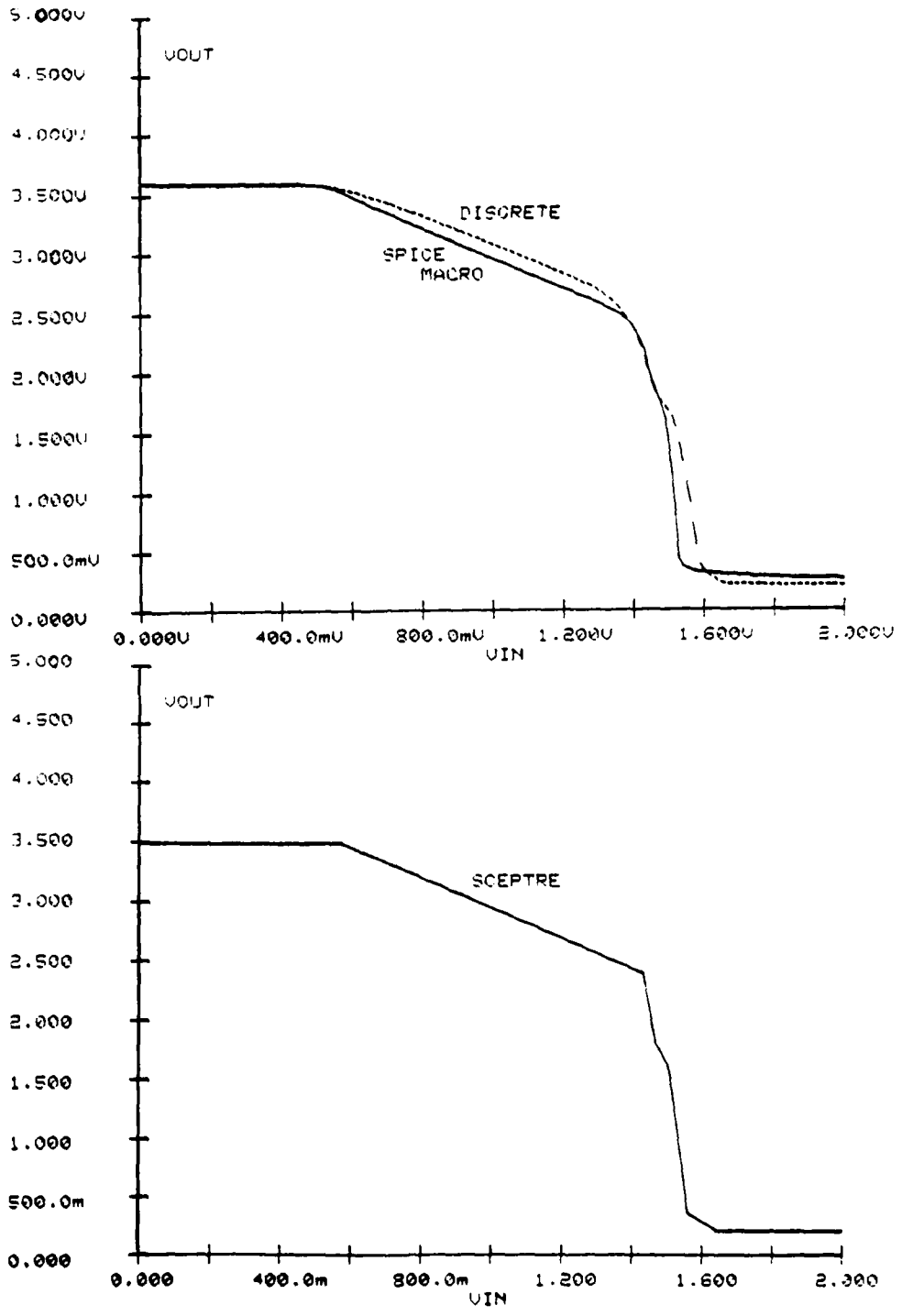


FIGURE 11: Output vs. Input Voltage for 10X Fanout Loading

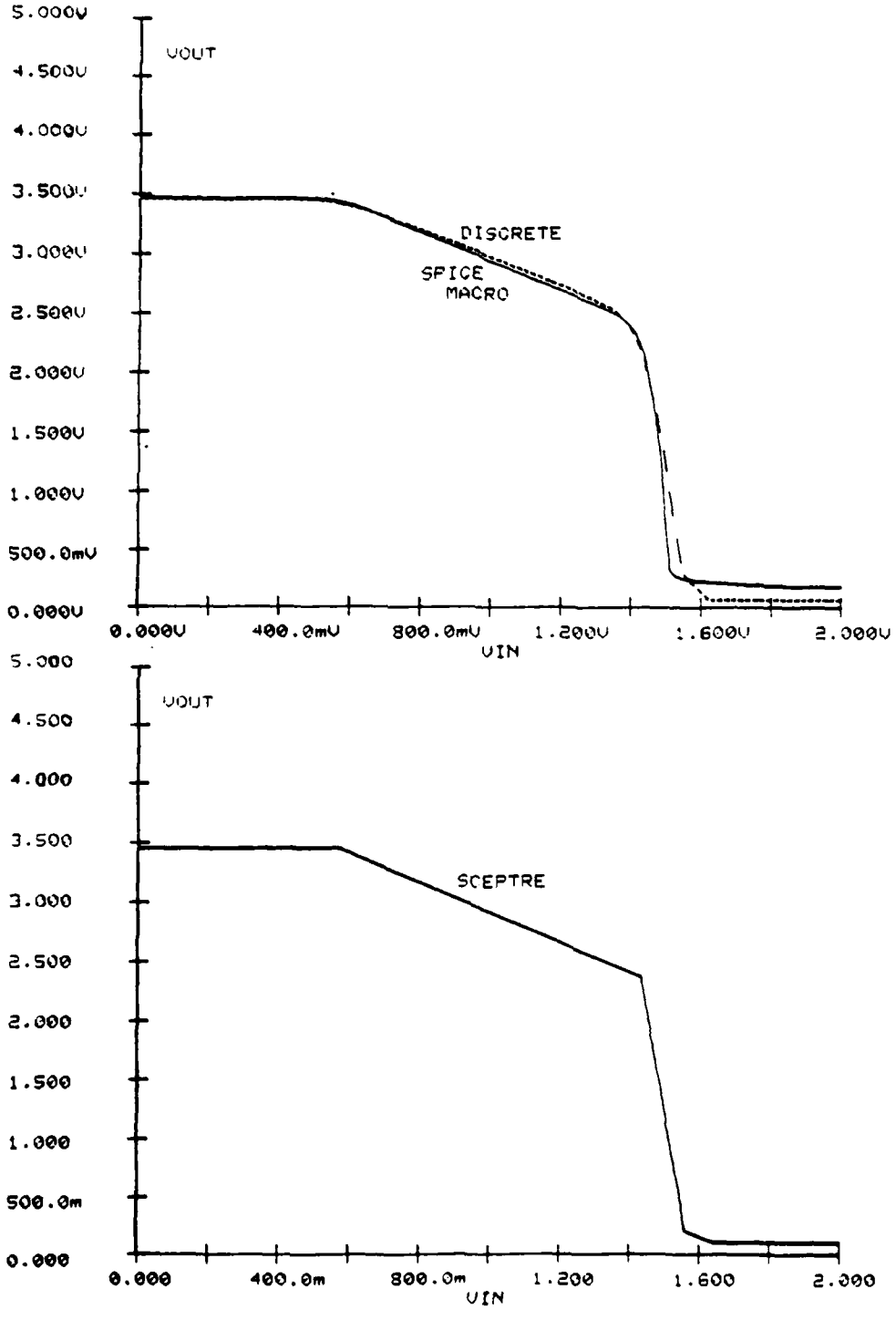


FIGURE 12: Output vs. Input Voltages for 10Kohm Load

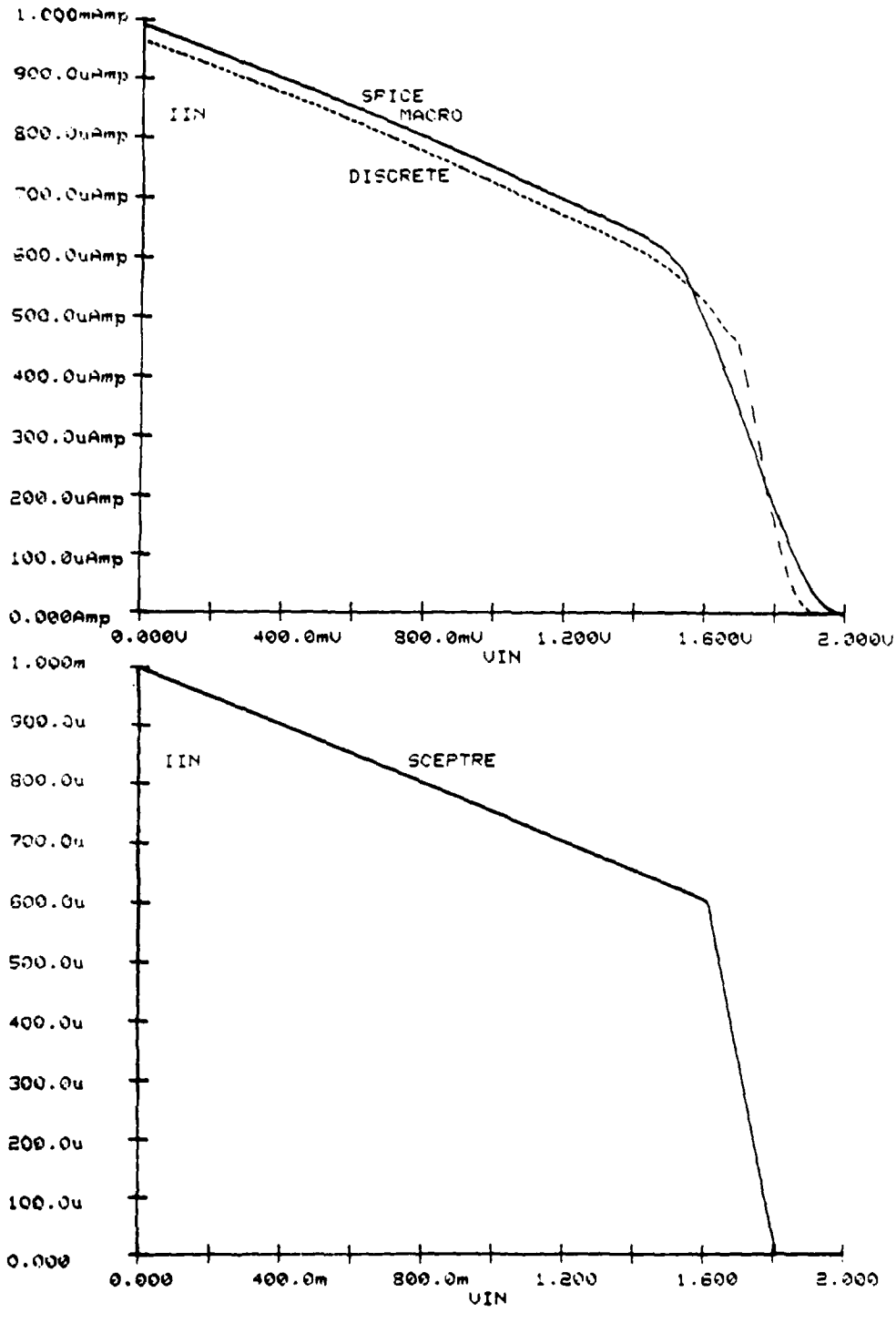


FIGURE 13: Input Current vs. Voltage

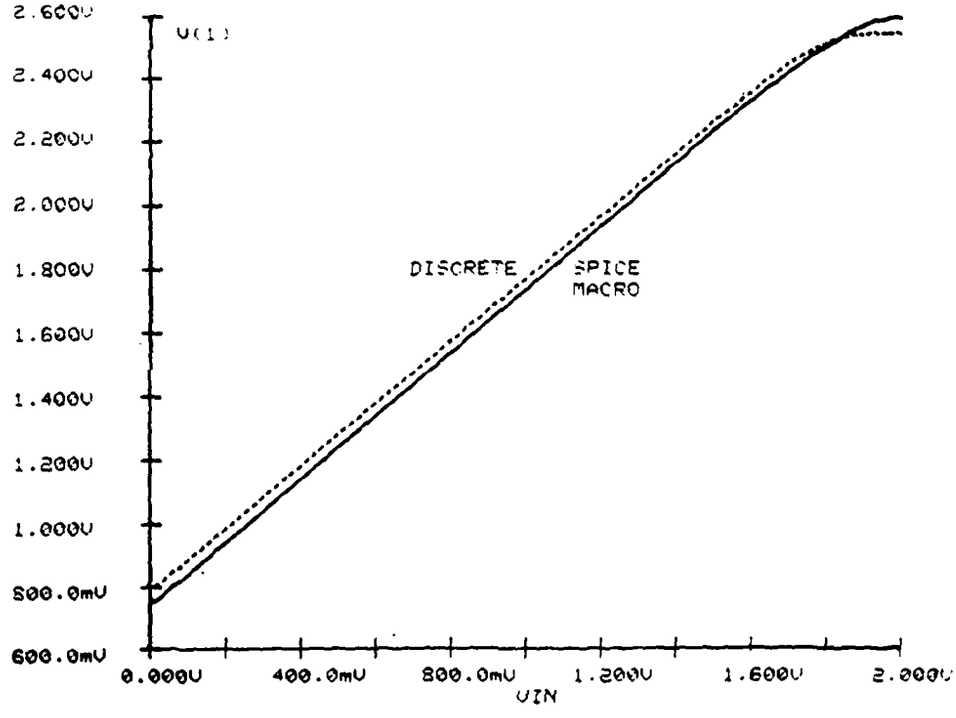


FIGURE 14: SPICE Internal Node 1 Voltage vs. Input Voltage

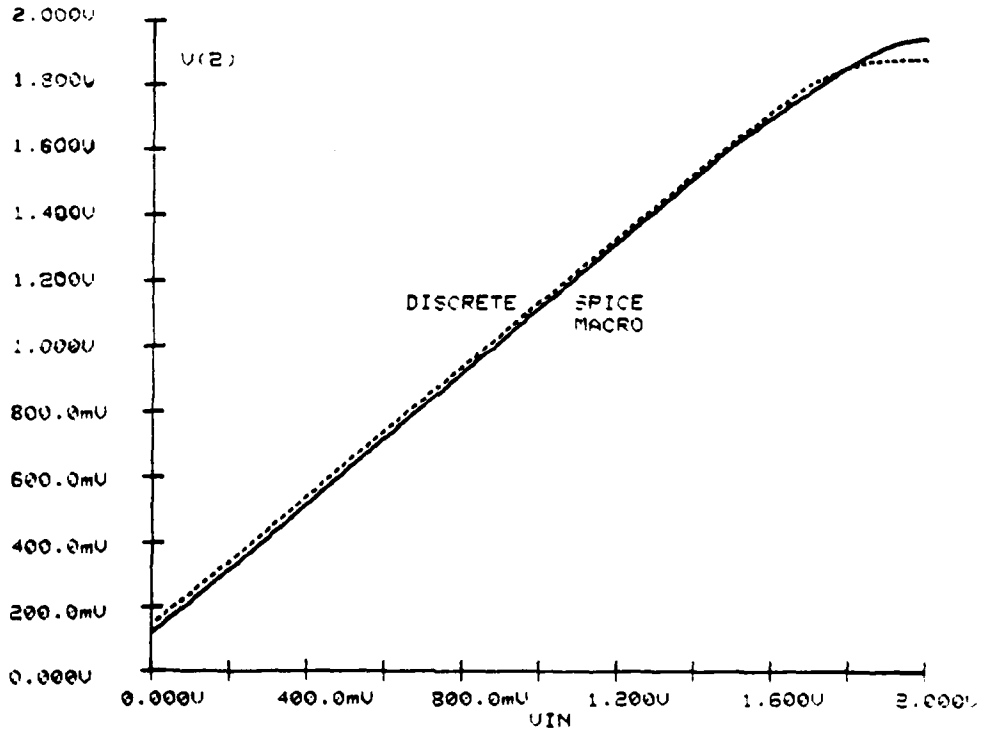


FIGURE 15: SPICE Internal Node 2 Voltage vs. Input Voltage

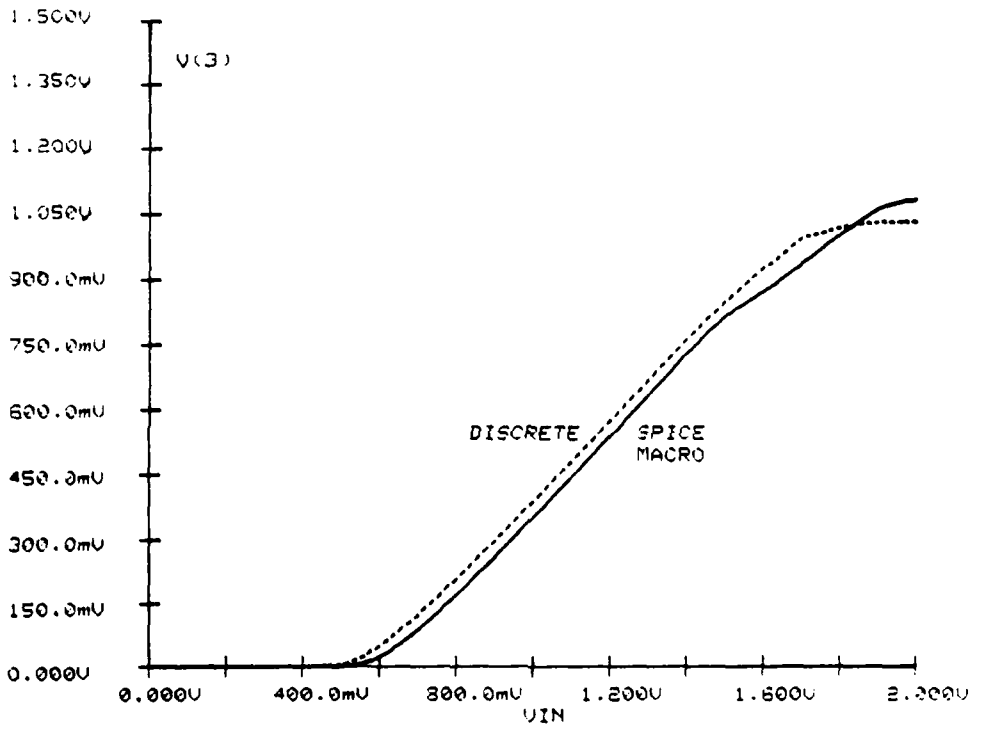


FIGURE 16: SPICE Internal Node 3 Voltage vs. Input Voltage

TRANSIENT RESULTS

The input signal used in the transient tests is shown in figure 17. The pulse is 50ns wide after a 10ns delay, and has rise and fall times of 4ns.

The output waveforms from analyses with output fanout of 10 and with the light load are shown in figures 18 and 19. In the upper plot in each figure, the SPICE macro model matches the discrete version results quite well in terms of propagation delay time in both directions as well as rise and fall times. The macro does fall somewhat during the delay time, but the change is not enough to propagate as a logic level shift since the waveforms line up long before reaching the 2v threshold of the undefined area. The output signal for the discrete model does have some overshoot when lightly loaded which is not being modeled, but under full load a very good fit is obtained.

The SUPER*SCEPTRE output waveforms in the lower portion of figures 18 and 19 show the result of the tabled capacitance delay stage. The shape of this waveform is rather symmetric due to the mechanism used: The delay time in each direction is synthesized in the first 1V of the switching waveform by a large capacitive time constant. The remainder of the waveform is fitted by decreasing the capacitance to match the rise time in the interval.

The input current waveform is shown in figures 20. In

this case, the SPICE macro-model matches the discrete very closely over the entire waveform due to the equivalence between the macro and discrete input stages, while the SUPER*SCEPTRE model, although not nearly as precise as the SPICE model, still gives a reasonably good representation of the input current.

Also, in figures 21-23 are the internal voltages at SPICE macro-model nodes V1, V2, and V3 compared again to the discrete model, as was done in the DC tests, which once again show a very good correlation.

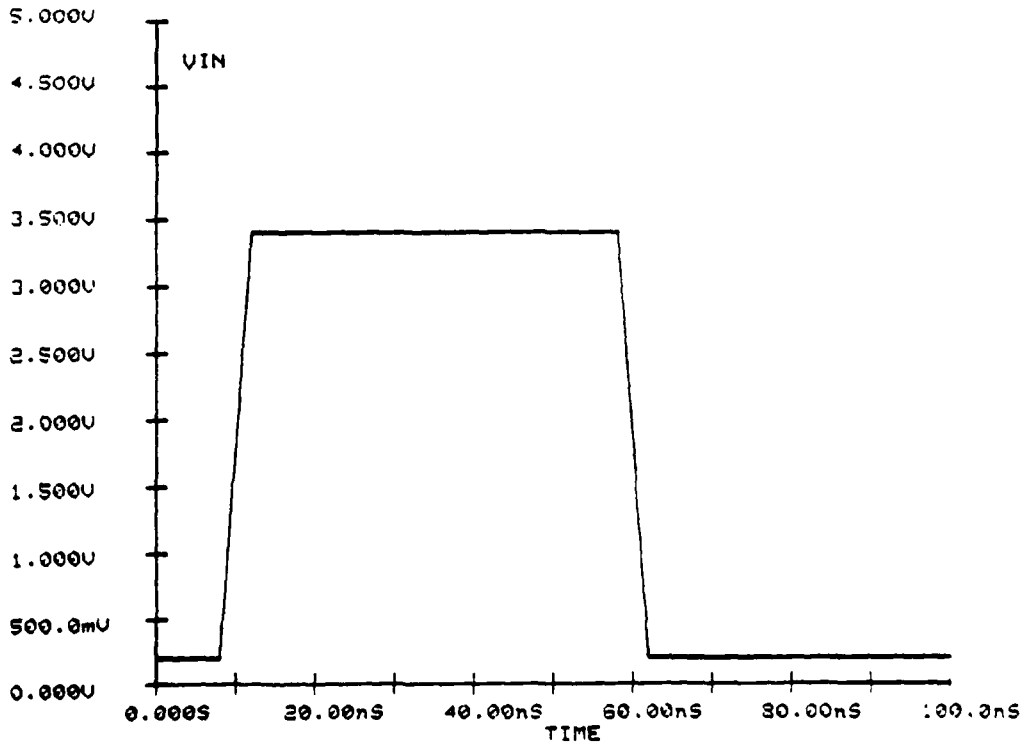


FIGURE 17: Input Signal Used for Transient Response Tests

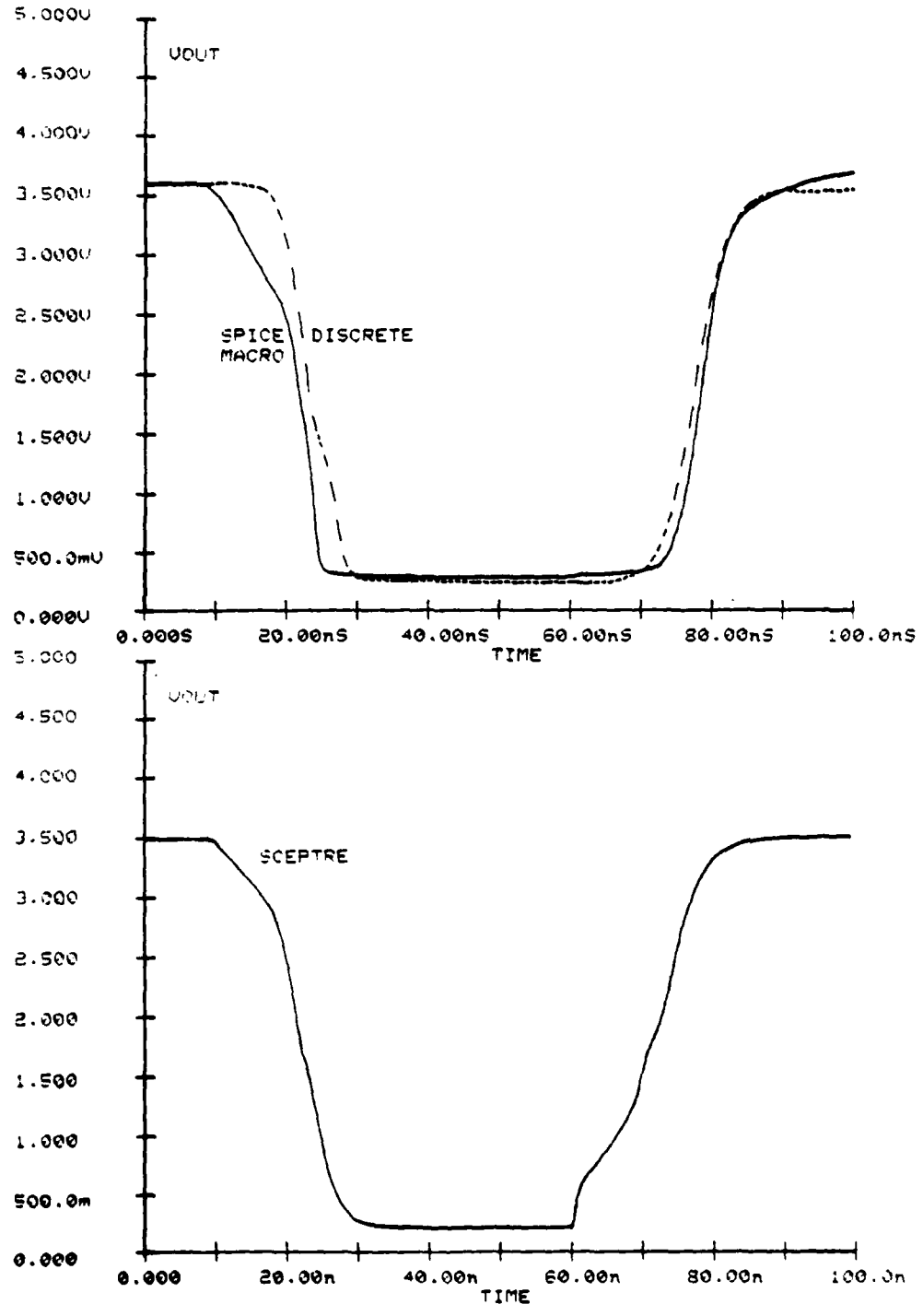


FIGURE 18: Output Voltage vs. Time - Full Load

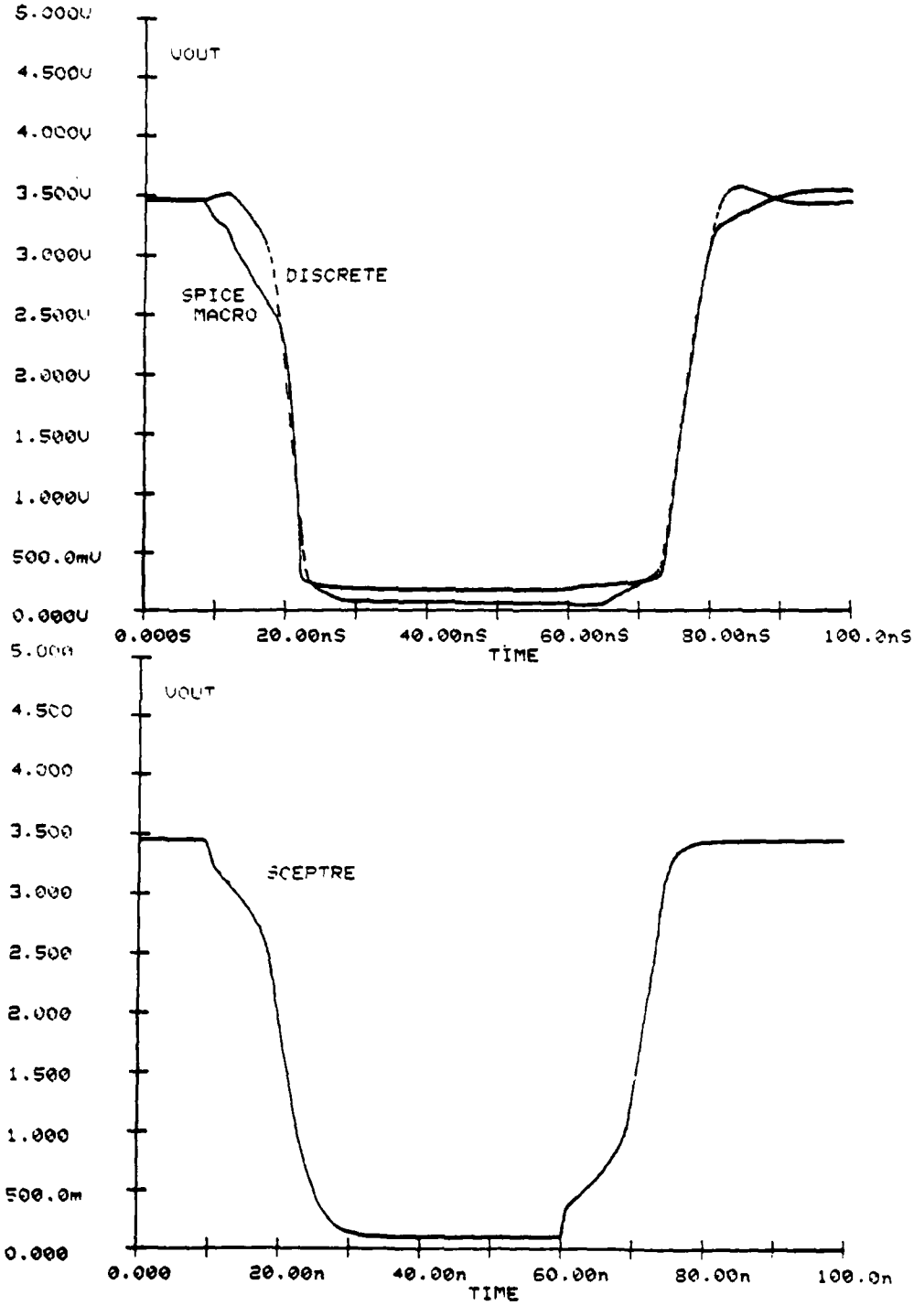


FIGURE 19: Output Voltage vs. Time - Light Load

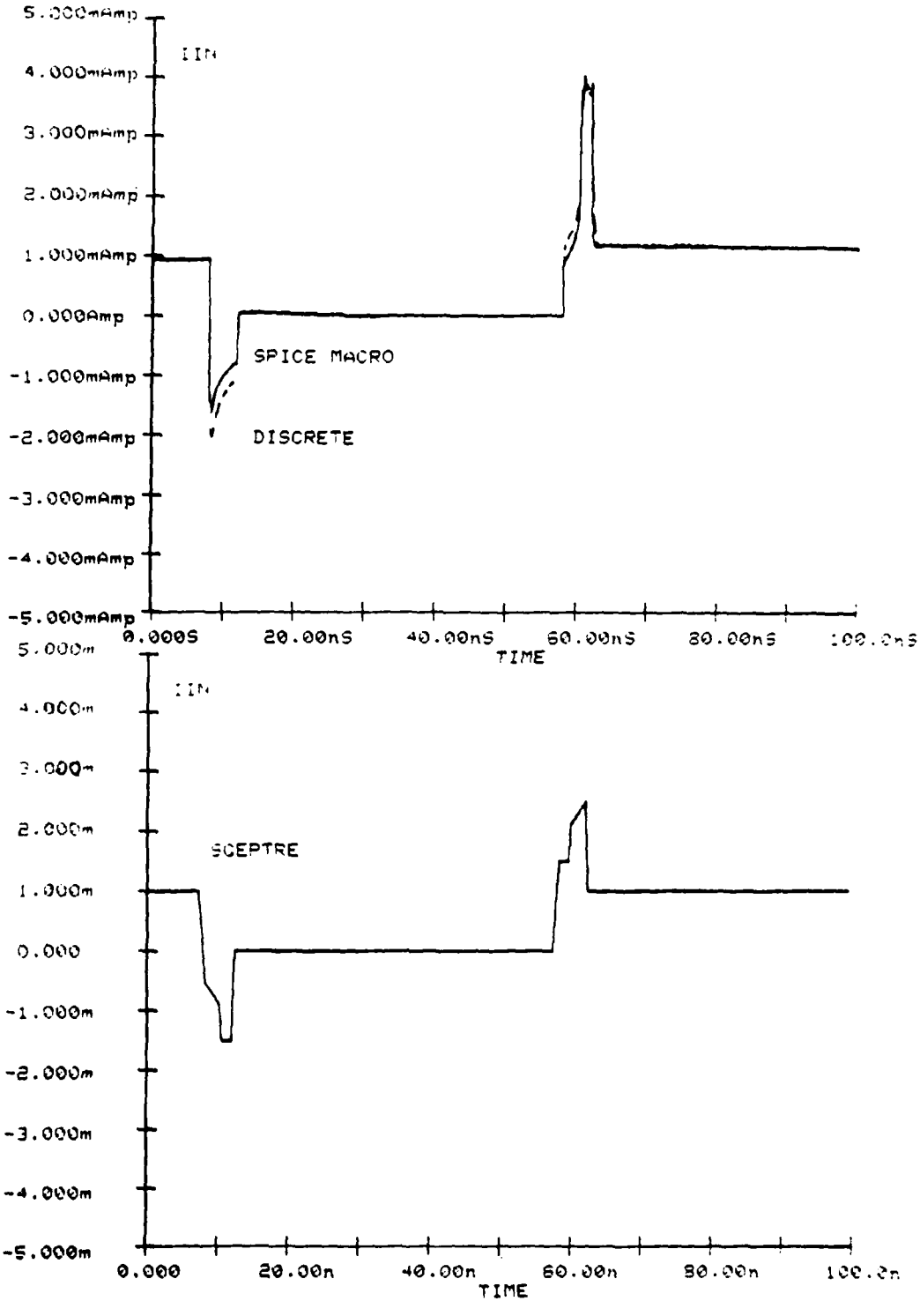


FIGURE 20: Input Current vs. Time

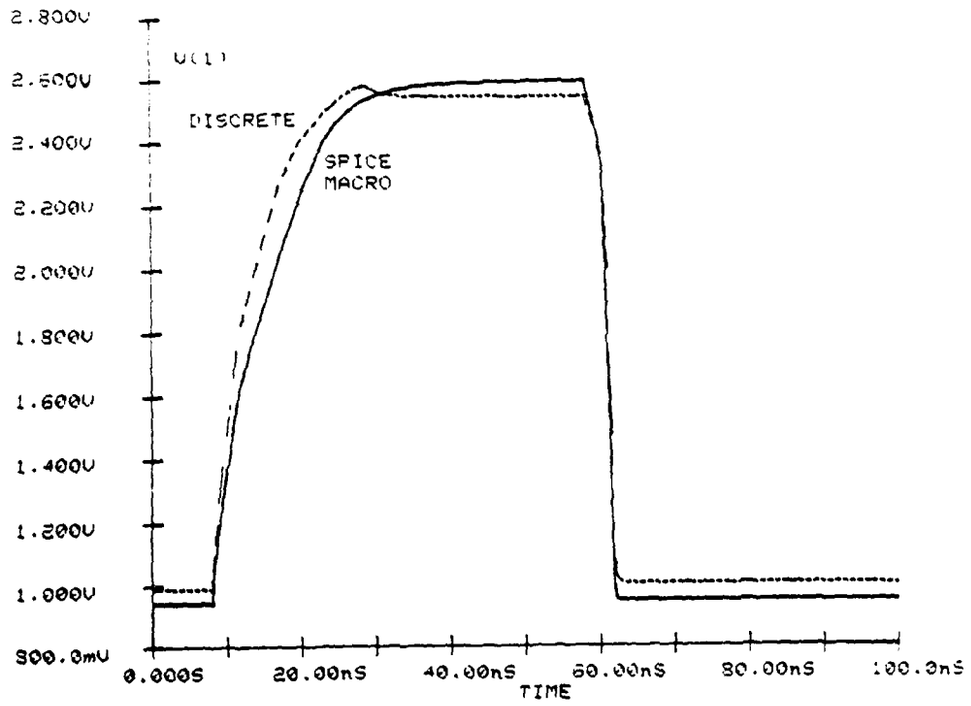


FIGURE 21: SPICE Internal Voltage V1 vs. Time

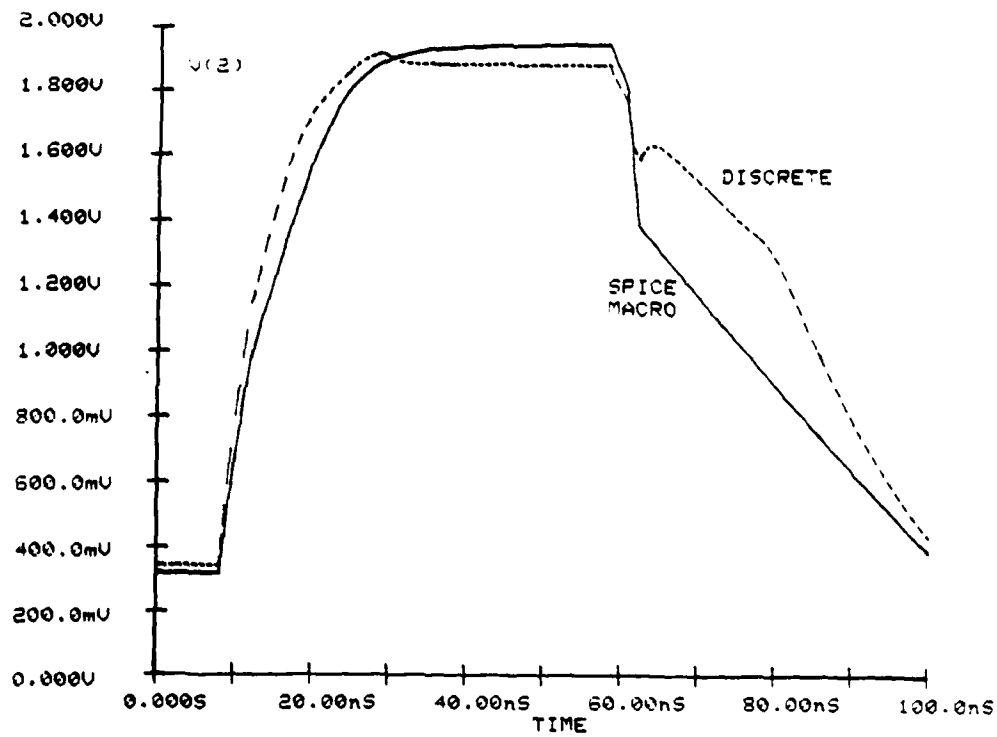


FIGURE 22: SPICE Internal Voltage V2 vs. Time

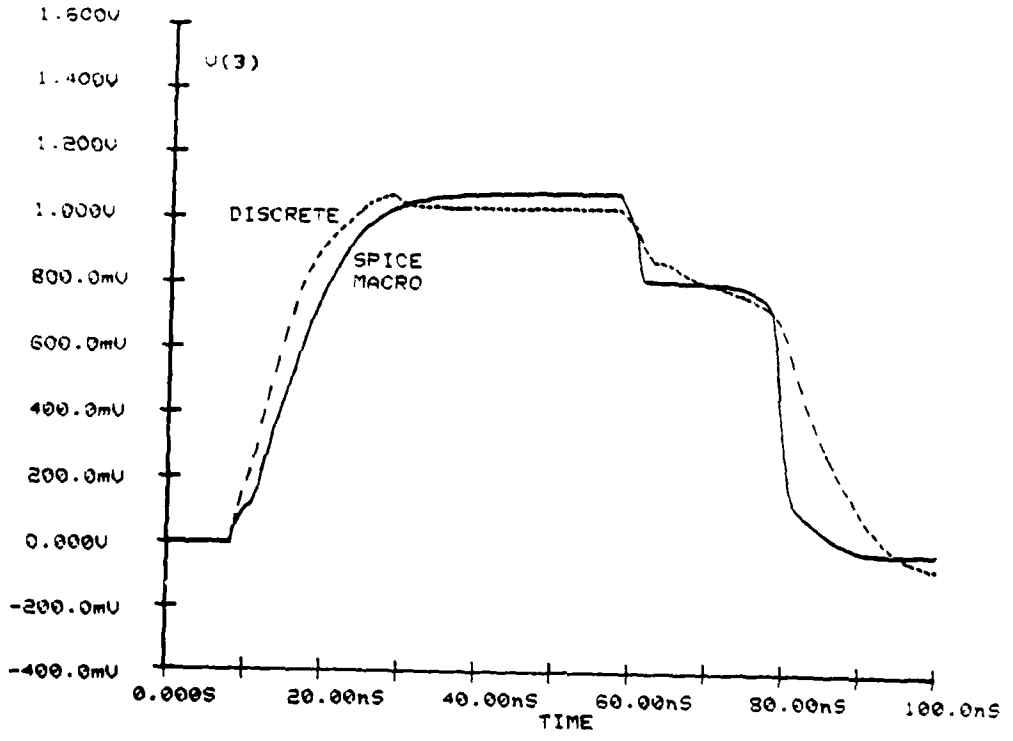


FIGURE 23: SPICE Internal Voltage V3 vs. Time

4. RESPONSE TO SINUSOIDAL INTERFERENCE

In reference [1] are analyses of the discrete 7400 NAND gate model's response when it is being interfered with by high frequency sinusoidal signals injected into each of the device's external nodes. In this chapter, several tests will be run to compare the SPICE macro-model's performance to that of the discrete under these operating conditions.

The SUPER*SCEPTRE model is not being included in these tests because it was specifically modeled only for nominal switching response, as opposed to the SPICE model which maintained most of the internal NAND gate structure. The accuracy of this structure is evidenced by the equivalence of the three internal nodes as shown in the previous chapter.

The circuit used for these tests is shown in figure 24. In this circuit, gate 2 is used to simulate a fan-out of 10 loading gate 1, so in the model used for N2, all resistances are scaled down by a factor of 10, all capacitors and currents up by 10, and each of the diodes and transistors use an area factor of 10 on the element cards so that their internal parameters will be scaled correctly as well.

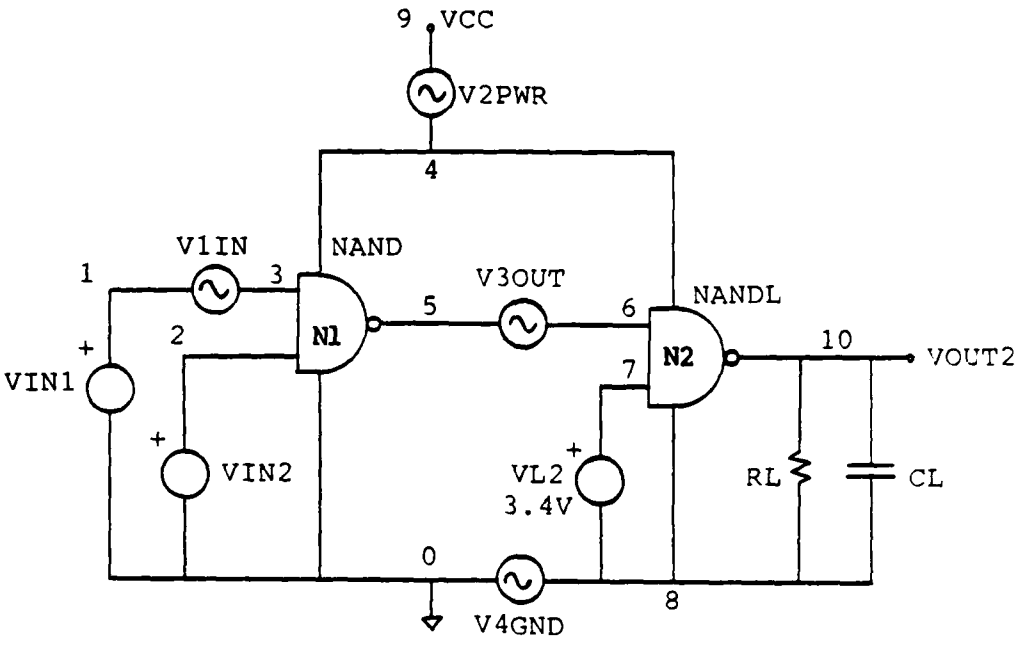


FIGURE 24: Circuit Used in Sinusoidal Interference Tests

The two input sources to the circuit are VIN1 and VIN2. The sinusoidal interference sources are:

V1IN, at the input of the first gate,

V2PWR, in the power supply line,

V3OUT, at the output of the first gate, and

V4GND, in the common ground between the gates.

INTERFERENCE BY QUADRANT

When interference is injected into a given node of the NAND gate, the change at the output will be dependent not only on the magnitude and frequency of the interference, but

also on the state (high or low) at each of the inputs.

The square waves sketched in figure 25(a&b) will be used to test this performance. The normal response of gate N1 without interference present, VOUT1, is high in the first three quadrants and low in the fourth quadrant as is shown in (c), and gate N2's output, VOUT2, is the inverse of this, shown in (d).

When a 3V, 1MHz signal is added to the input of gate 1, VOUT2 will be perturbed in the second and fourth quadrants. Figure 26 shows this response modeled by the device-level model (a) and the macro-model (b).

If the same interference is added to the output of gate 1, the response will only be perturbed in the fourth quadrant, as shown in figure 27(a&b). It should be noted that the 1MHz interferer is much slower than the response of the NAND gate, so the response in this figure and the previous show the macro-model performing almost identically as the discrete model, since the switching is primarily just based on the DC threshold voltage.

When the 3V, 1MHz interferer is injected into the power supply, the waveforms of figure 28(a&b) result. In this case the interference is again only significant in the fourth quadrant. The macro-model shows a little more interference in the other quadrants than the discrete version, but the signal (less than 0.5V) is not sufficient to change

the logic state and is therefore not very significant.

Finally, interference injected into the ground terminal of the load gate results in the waveforms in figure 29. The macro-model here shows a tendency toward amplification not present in the discrete model -- the 3V amplitude interferer causes 15V spikes in the macro output versus 5V spikes in the discrete -- hence the macro-model is somewhat more sensitive to ground interference than the device, but the waveform produced in each quadrant is still quite similar.

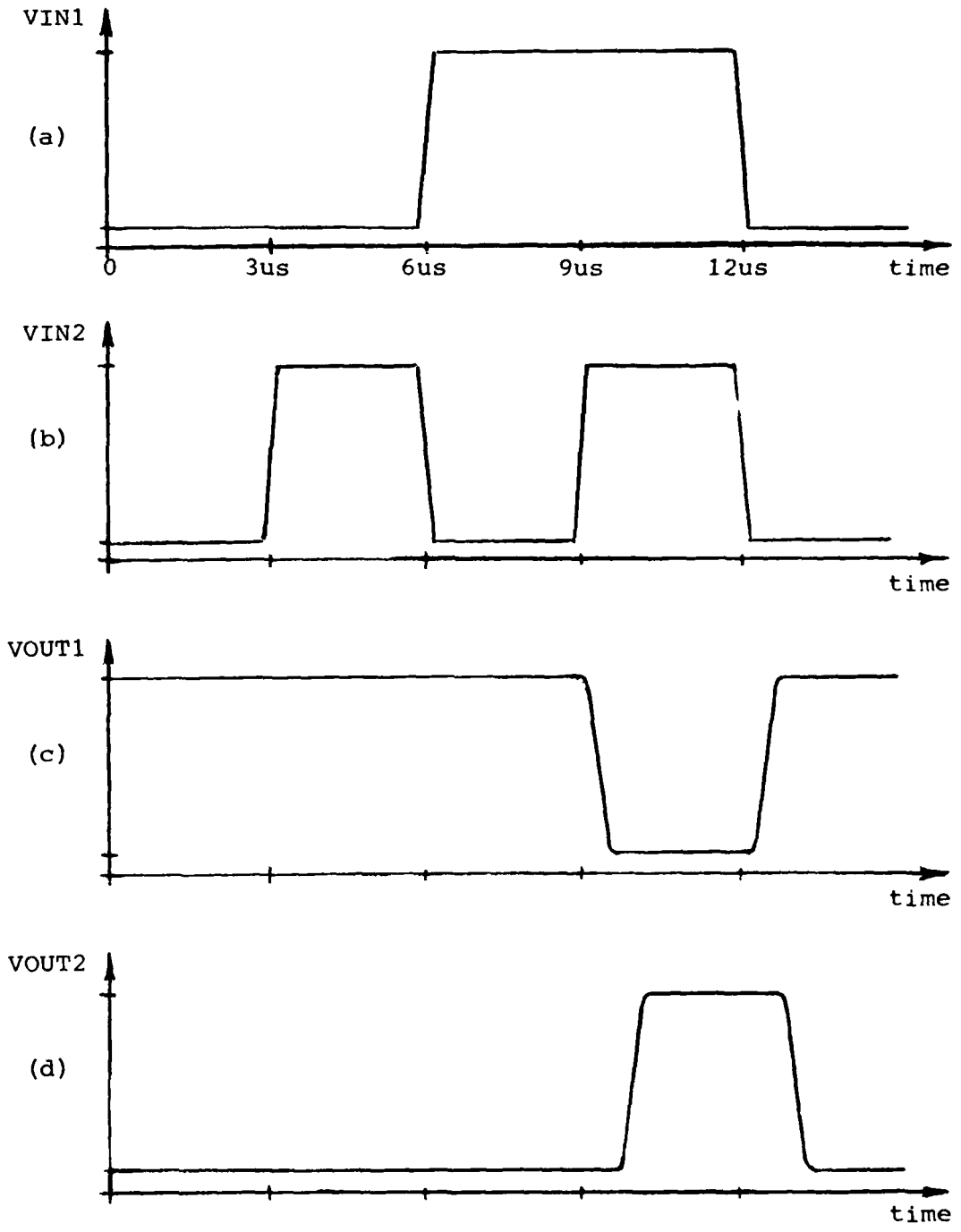


FIGURE 25: Input and Output Waveforms Without Interference

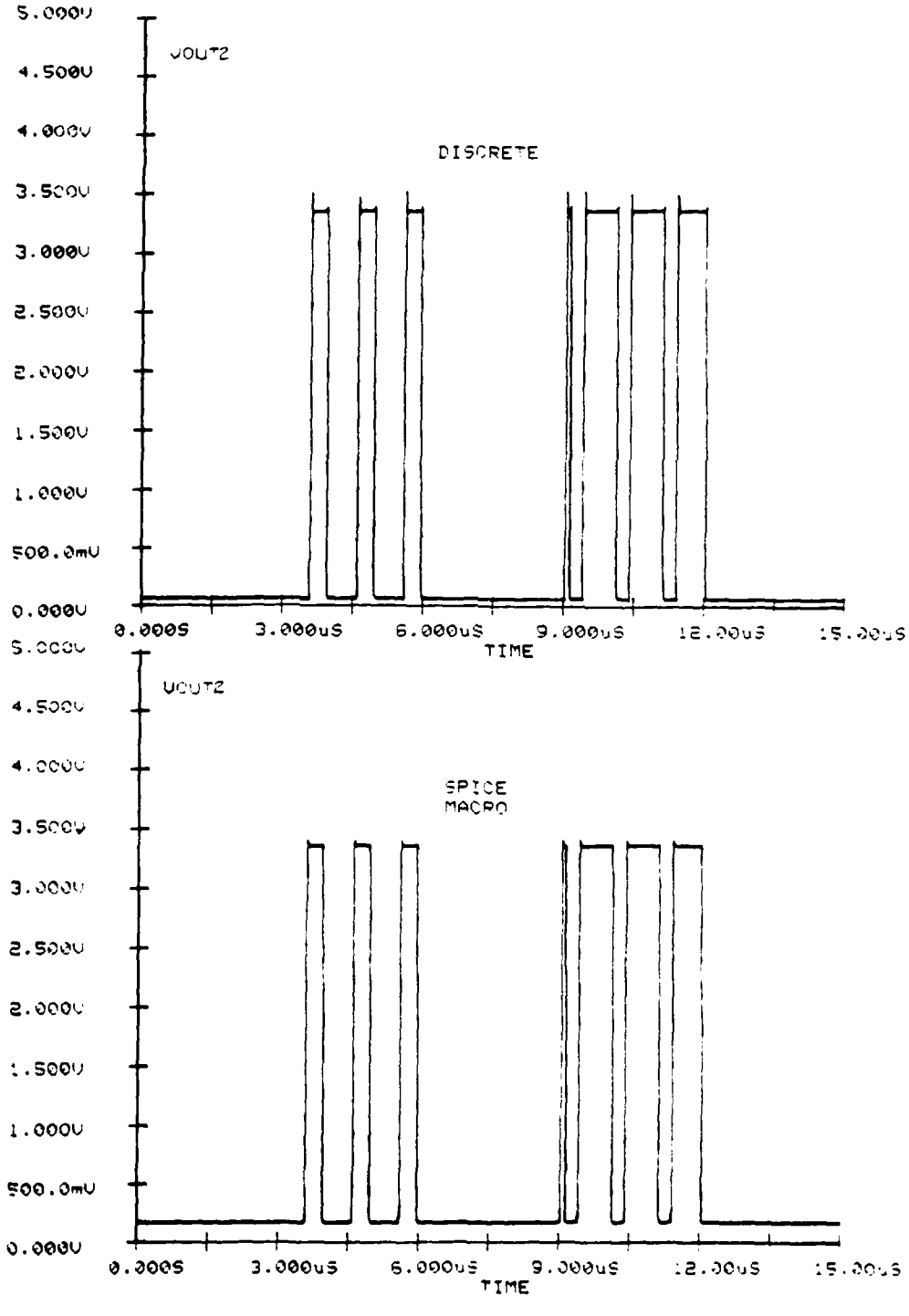


FIGURE 26: Response to Input Interference by Quadrant

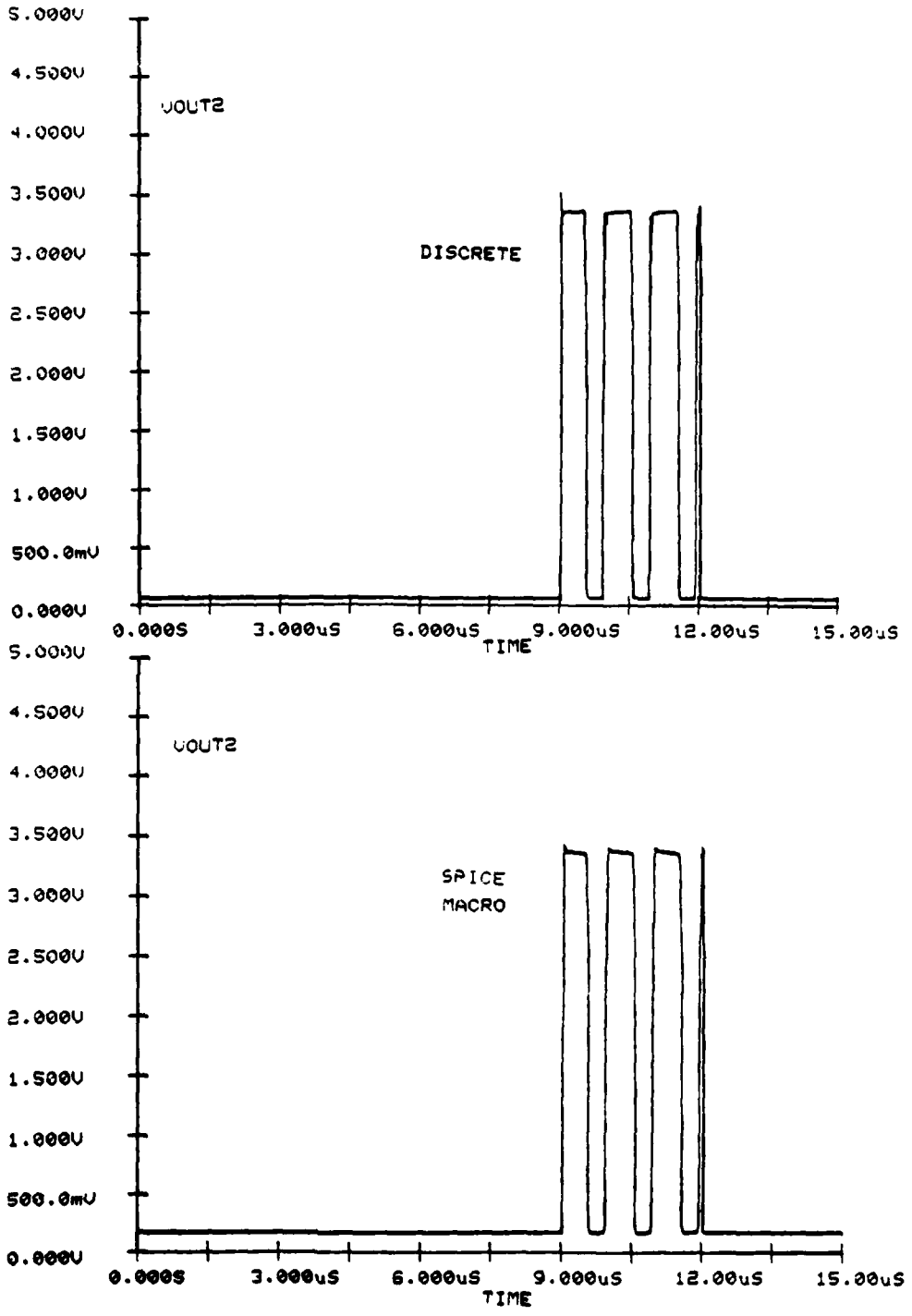


FIGURE 27: Response to Output Interference by Quadrant

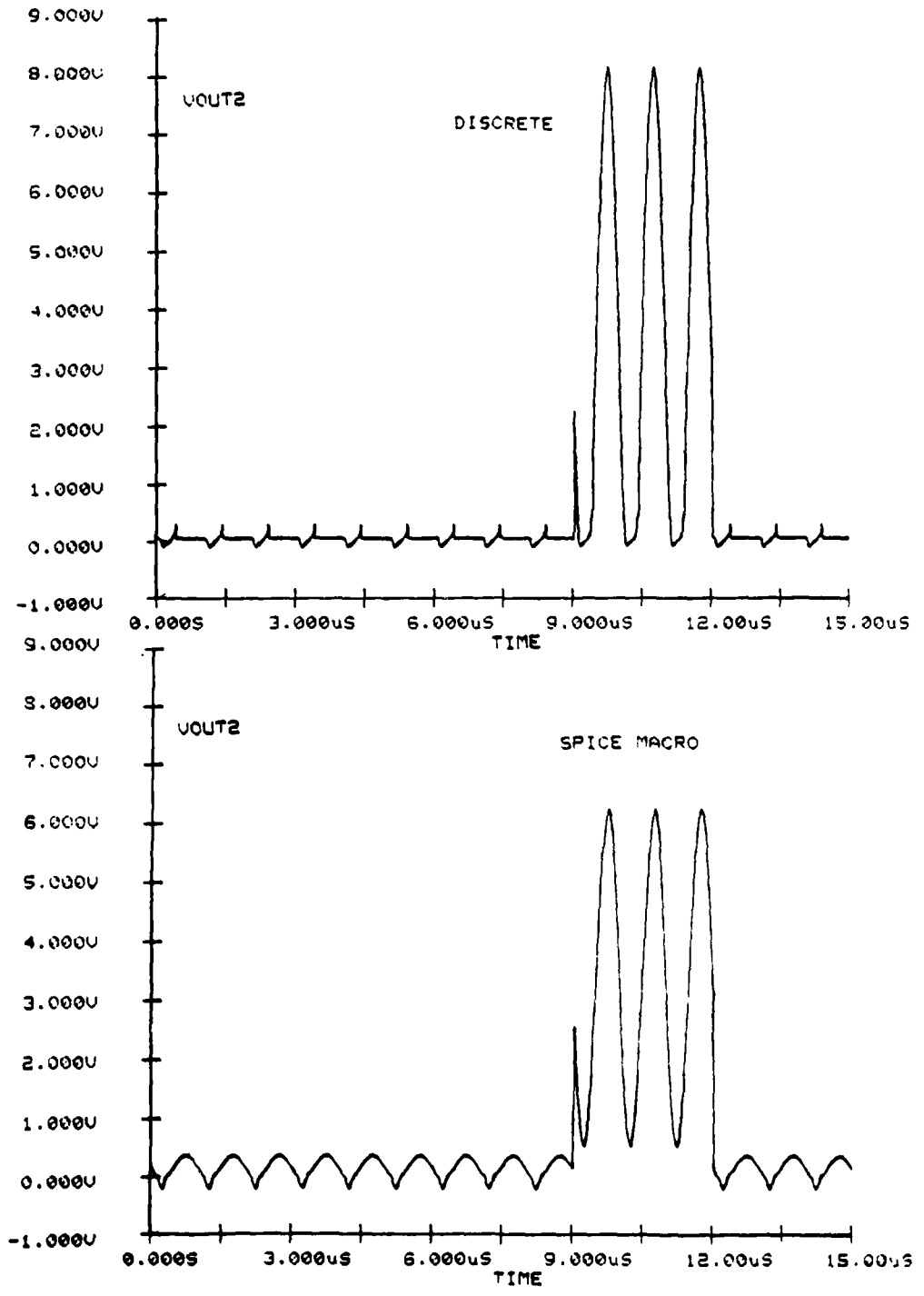


FIGURE 28: Response to Power Supply Interference by Quadrant

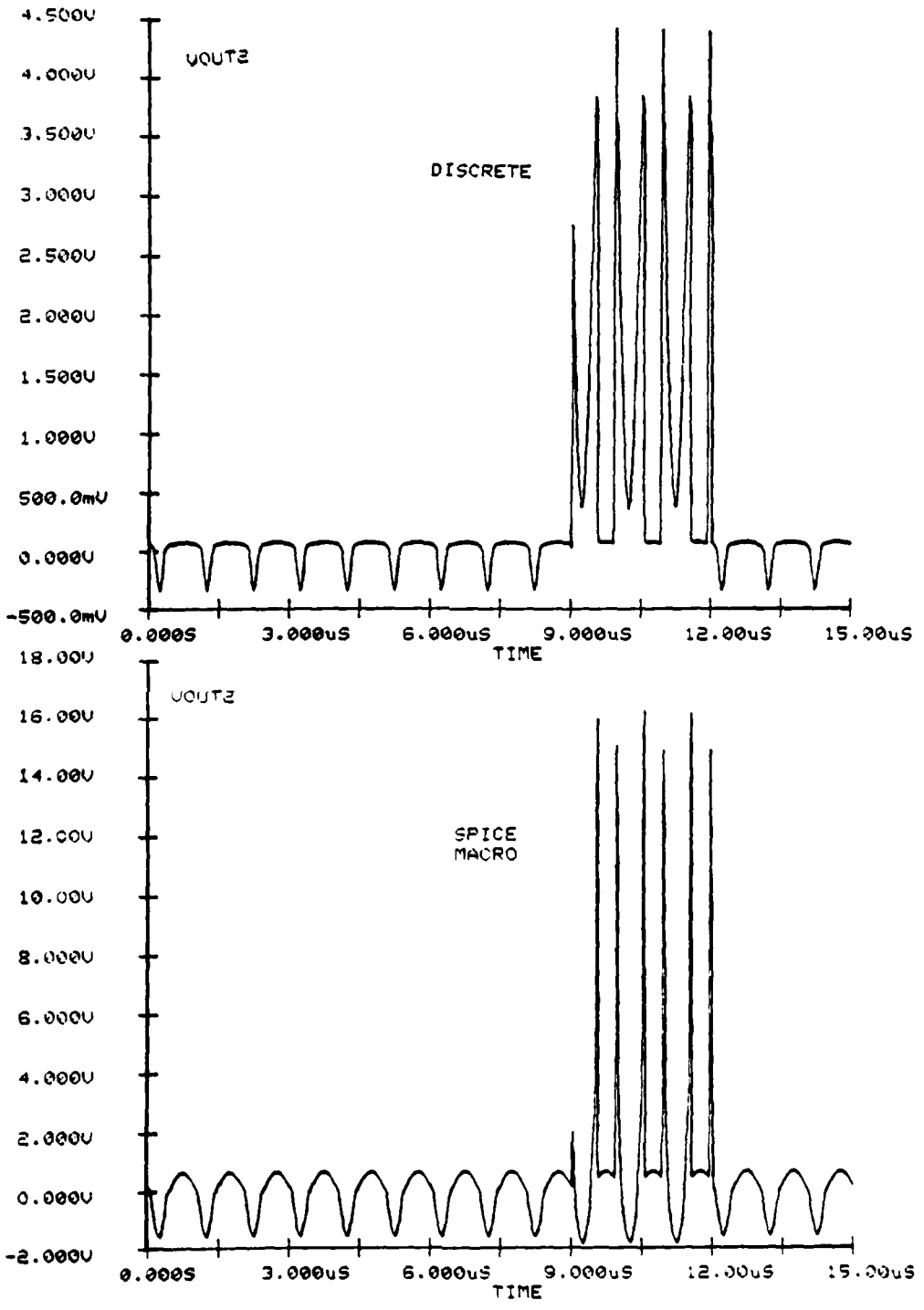


FIGURE 29: Response to Ground Interference by Quadrant

INTERFERENCE AMPLITUDE VS. FREQUENCY

Another response function of interest is the relationship between the frequency of the interfering signal and the magnitude required to cause the output of the second gate to change state. To test the response of the macro-model versus the discrete model, many test runs were performed with the interference signal swept from small to large magnitude at constant frequency (figure 30) by using a polynomial dependent source to multiply a ramp by a unit sinusoid. Using this method, data could be extracted from a single run to show the magnitude of the interference voltage required to cause the output signal to be perturbed from its initial value, into the undefined area (1-2V) and to completely change state (HIGH to LOW).

In figures 31 and 32 are responses VOUT2 for interference at the input to gate 1 at 1MHz and 15MHz, each plotted against the magnitude of the sinusoidal interference, for inputs of VIN1=LOW, VIN2=HIGH. Note that at 1MHz the change is essentially a DC step from LOW to HIGH and back, since at this frequency a half cycle lasts 500ns, much longer than the 10-15ns response of the NAND gate. At 15MHz, however, the half cycle is only 33ns long so the rise and fall times limit the response to a greater degree. In fact, for frequencies over 25MHz, the 20ns half cycle time is insufficient to change the state of the output regardless of the magnitude of the interference.

Figures 33-35 show the results of interference added to the output of gate 1 when both inputs are HIGH, at frequencies of 10, 40, and 100MHz. At 10MHz we see that the output of the second gate (normally HIGH) will toggle from HIGH to LOW for interference of greater than around 1.4V; at 40MHz, the input moves from HIGH to toggling between 4V and 7V; and at 100MHz, around 18V of interference signal are required to initiate toggling, but increase to a 21V signal causes an actual logic error, where the output which should be HIGH actually stays LOW when sufficiently large interferers are present. In all of these cases, the macro-model very faithfully models the responses found in the discrete device.

A 10MHZ interferer injected from the power supply with both inputs LOW is shown in figure 36. The response shows a sharp spiking phenomenon at the output of gate 2, which is reasonably well modeled in the macro-model, although the magnitudes are not quite even.

Finally, interference at 30MHz in the ground line of gate 2 with both inputs HIGH yields the results in figure 37. The macro-model again shows large gain in the signal above 5V, but the critical values where the output drops below 2V and where its state changes to a constant LOW are still well preserved.

Summaries of the critical levels where the output reaches the logic threshold of 1.5V and where it drops to a continuous LOW state for each type of interference is summarized in

figures 38 and 39, showing a very good correlation between the results of the macro-model with the discrete model. This is rather startling when it is recognized that only DC values and delay times were used for computation of the model parameters. Apparently the device's input and output transistors, Q1 and Q4 (which can be nearly fully synthesized from external measurements) are responsible for the dominant high frequency response of the device.

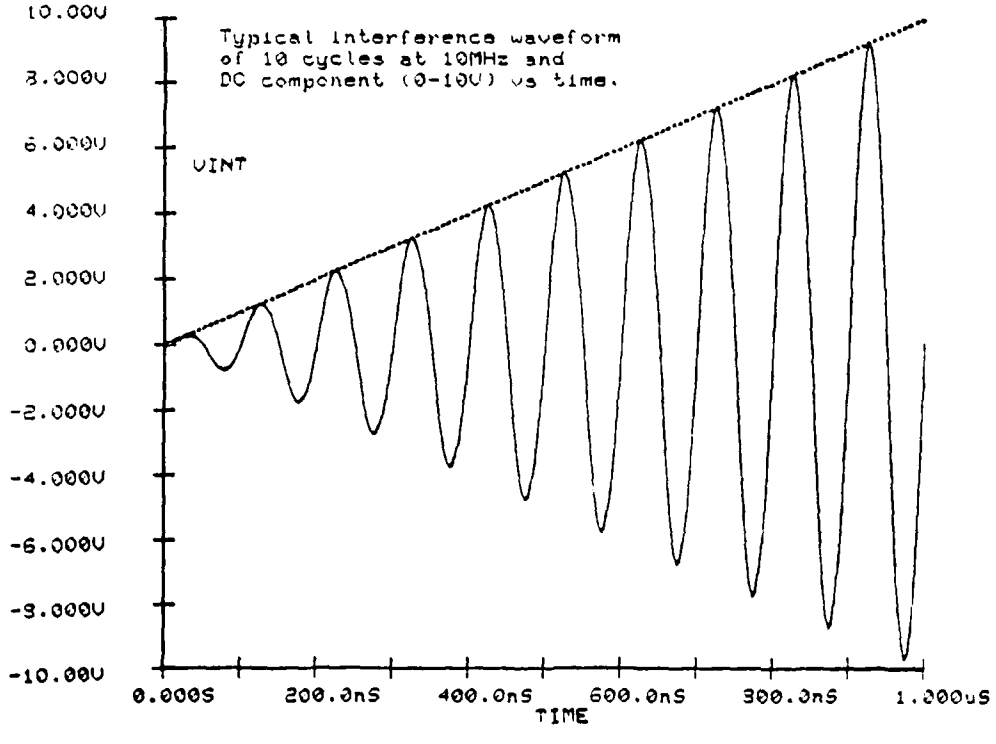


FIGURE 30: Typical Interference Test Input Waveform

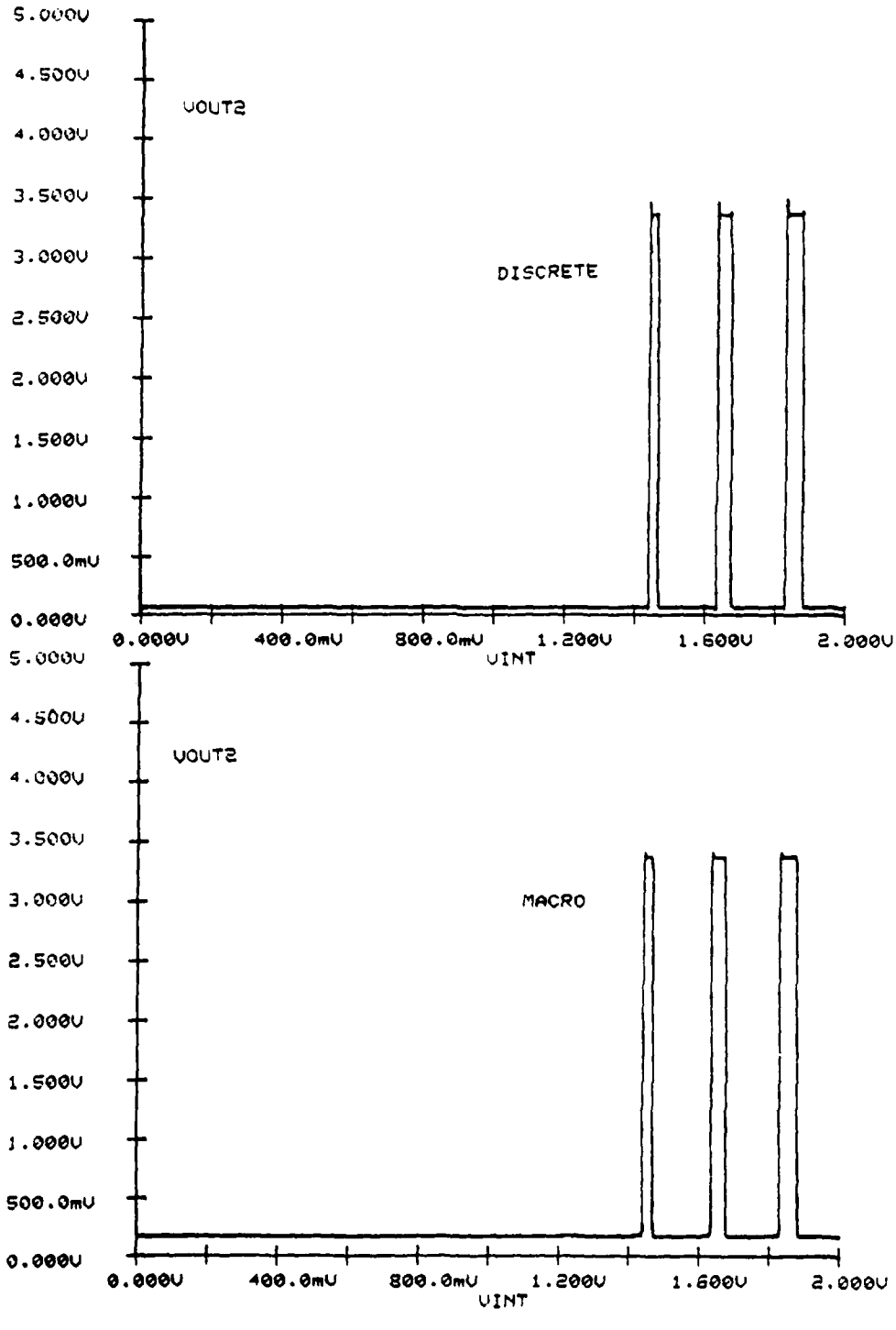


FIGURE 31: Response to Input Interference: 0-2V, 1MHz

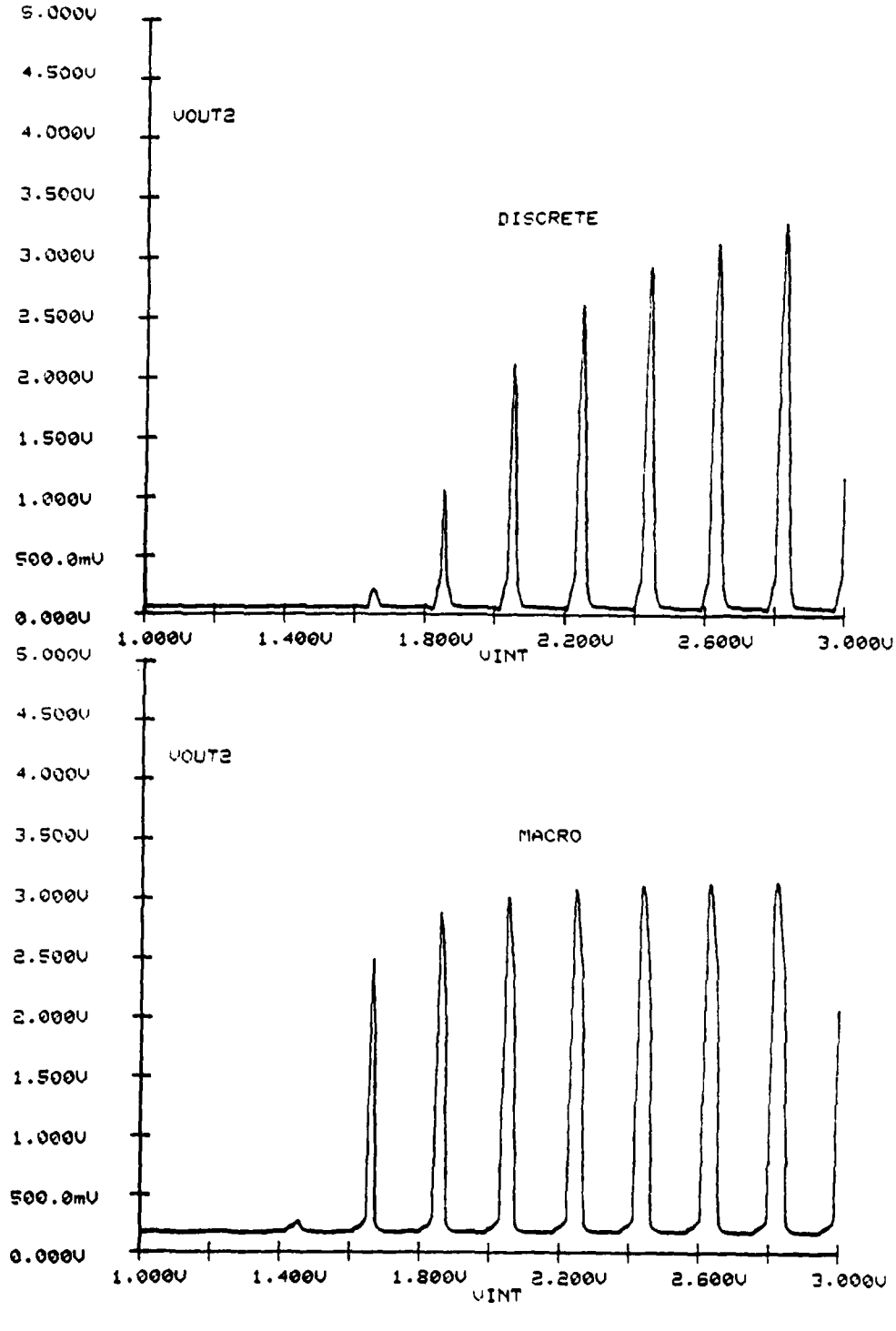


FIGURE 32: Response to Input Interference: 1-3V, 15MHz

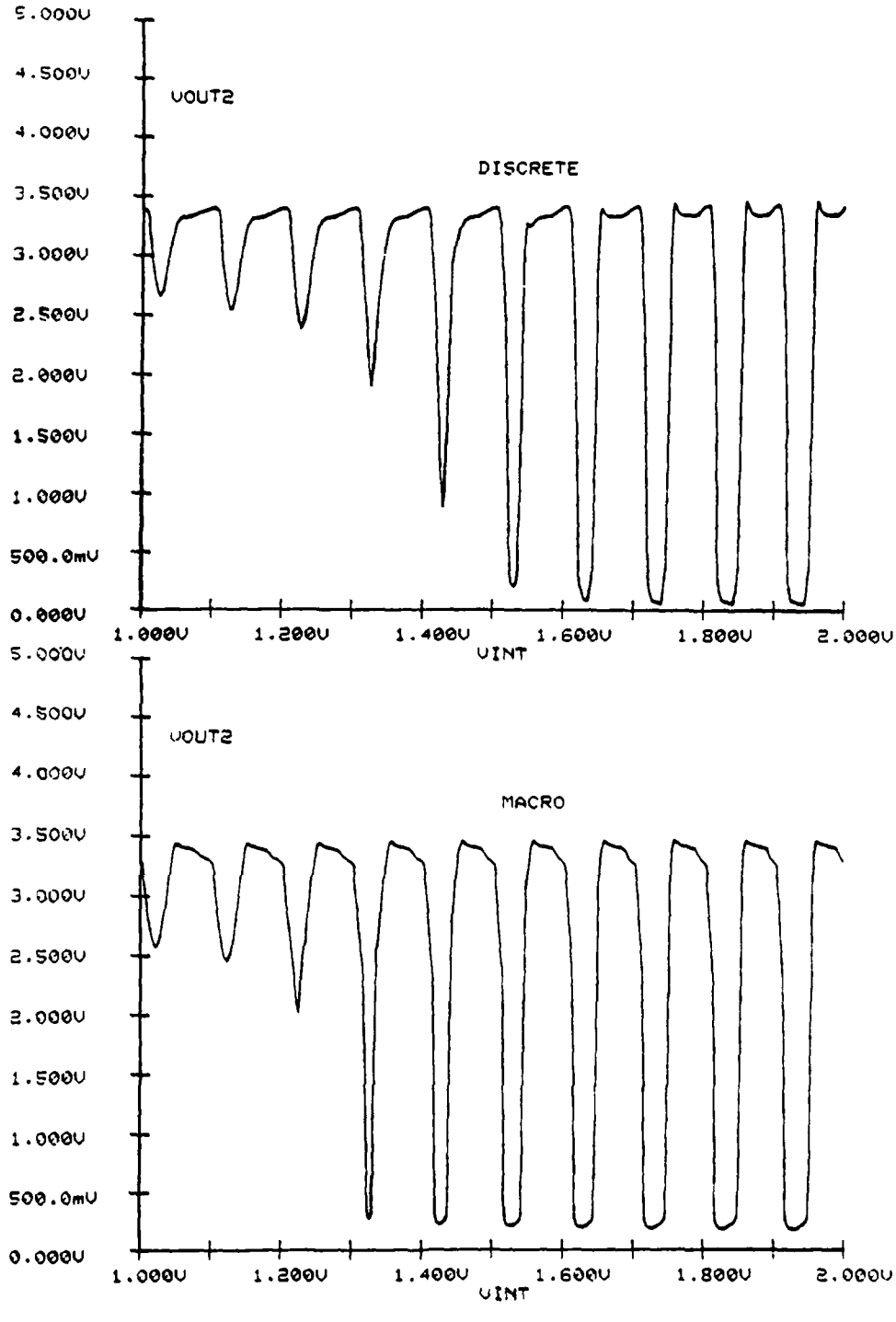


FIGURE 33: Response to Output Interference: 1-2V, 10MHz

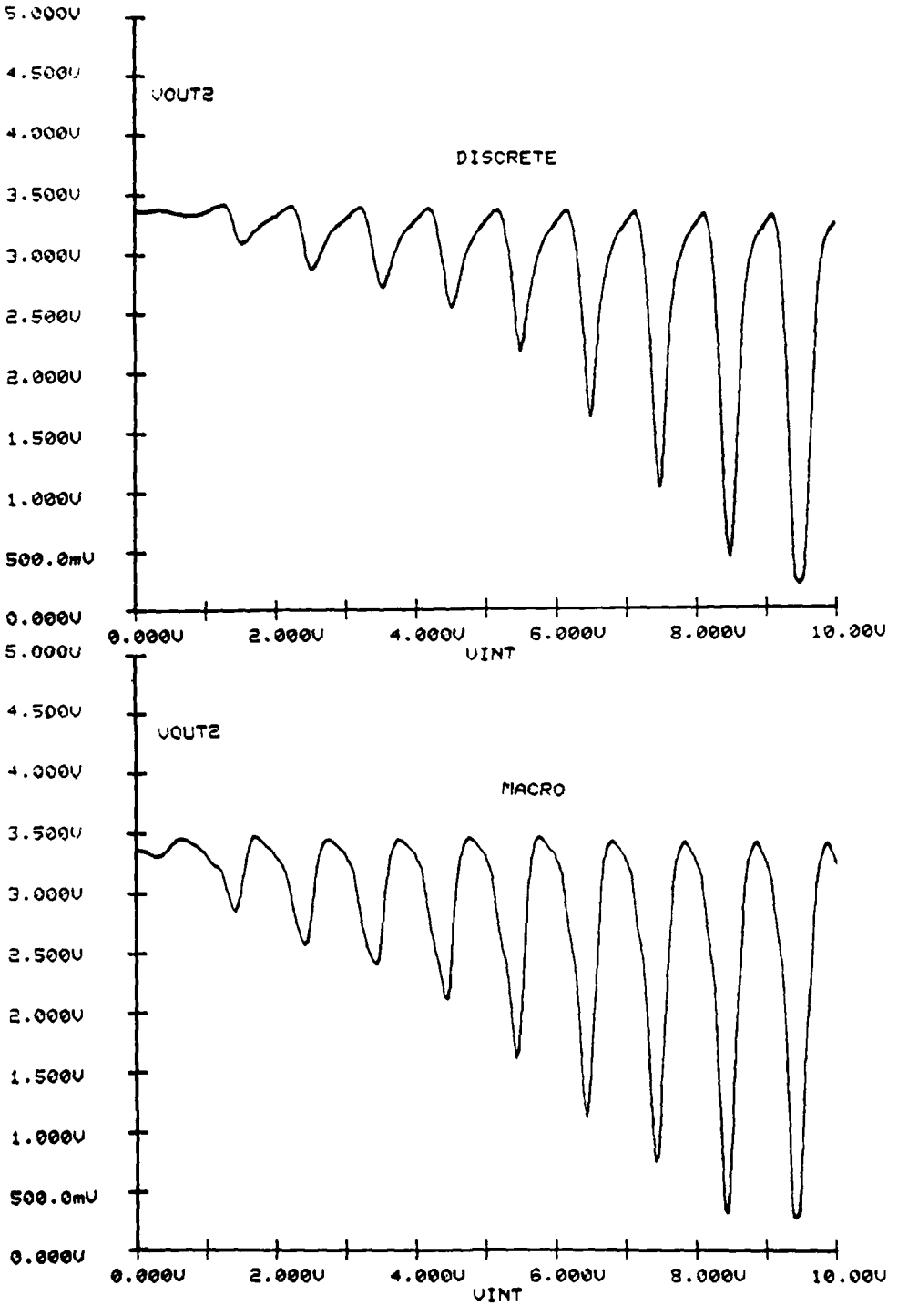


FIGURE 34: Response to Output Interference: 0-10V, 40MHz

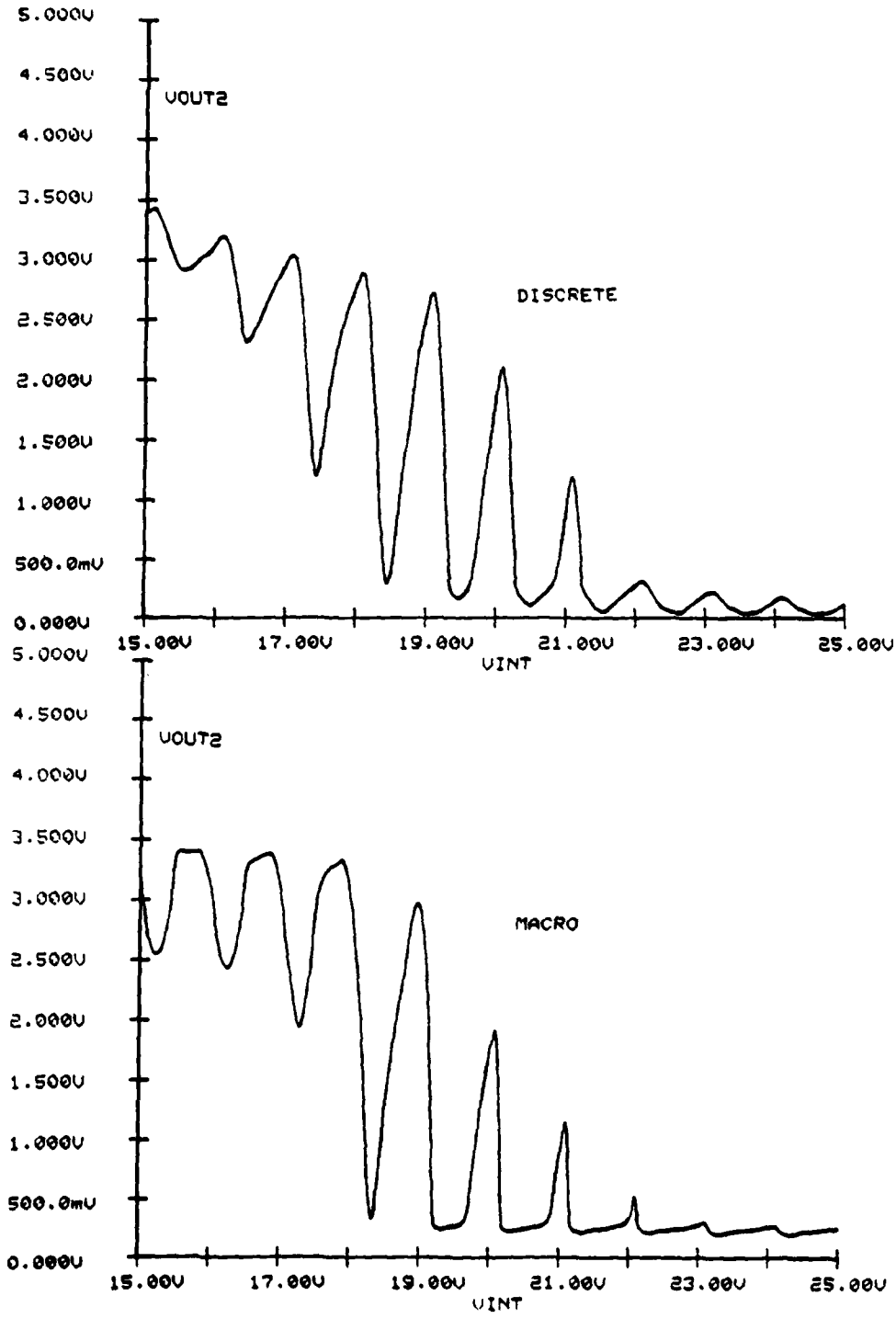


FIGURE 35: Response to Output Interference: 15-25V, 100MHz

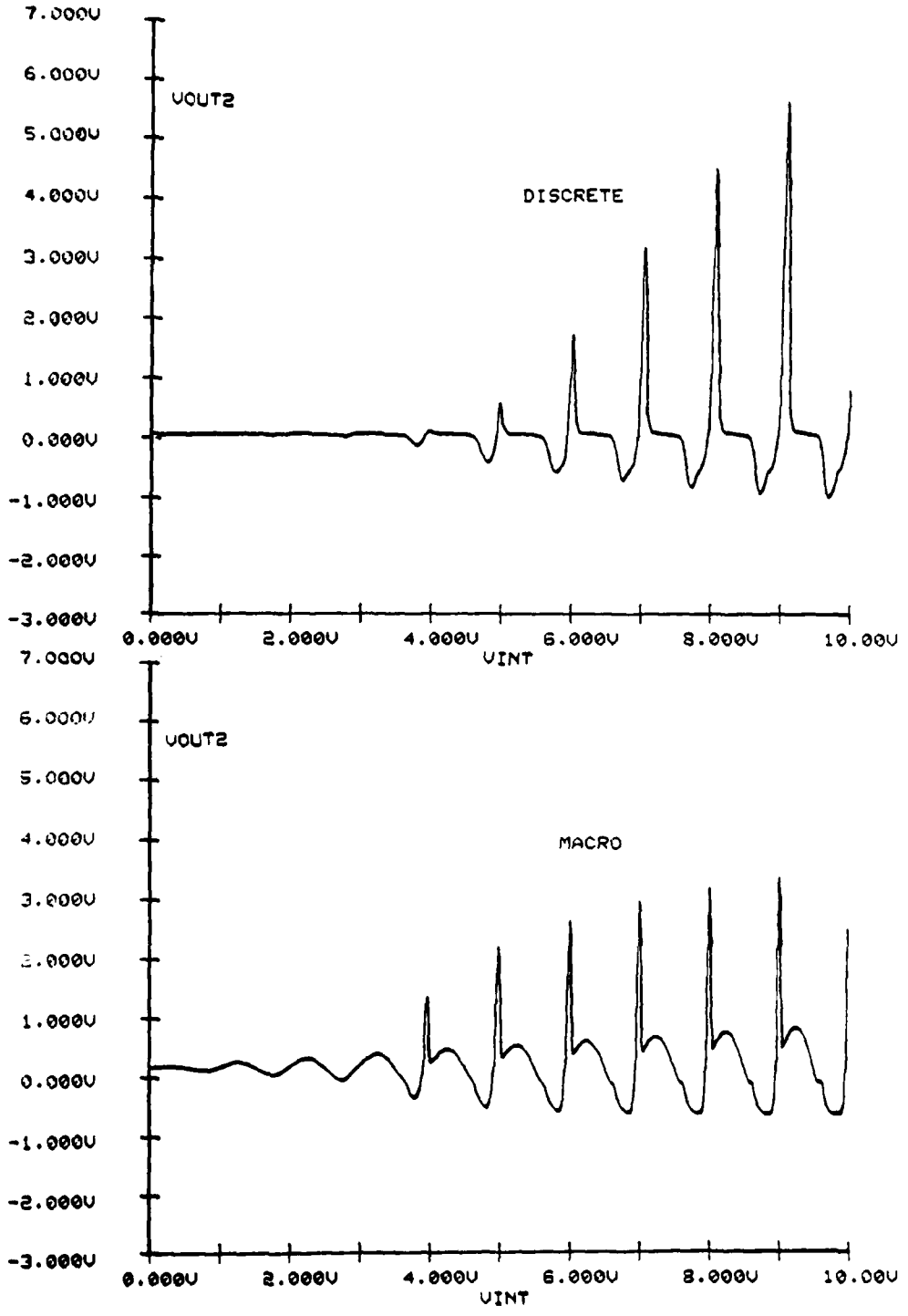


FIGURE 36: Response to Supply Interference: 0-10V, 10MHz

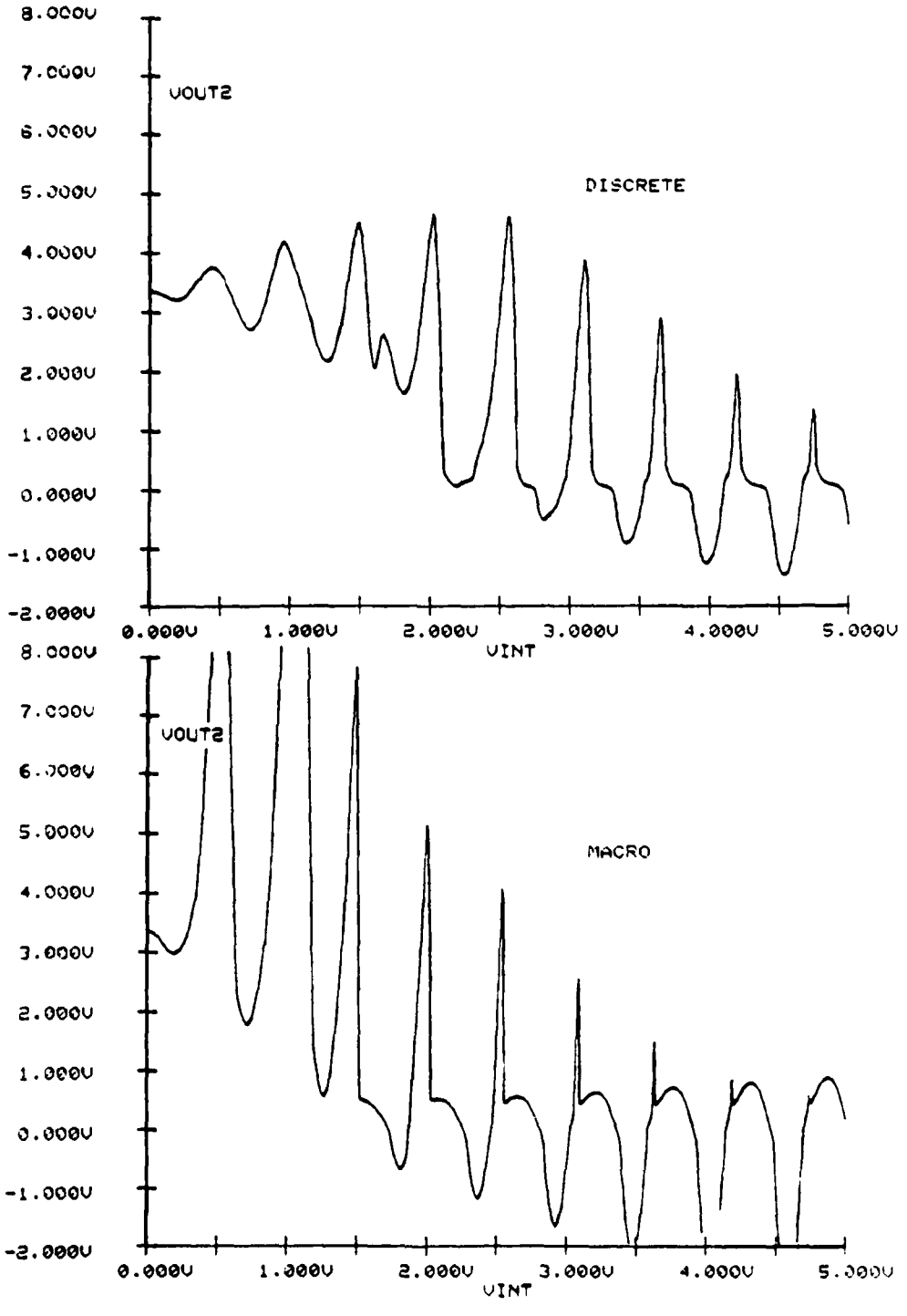


FIGURE 37: Response to Ground Interference: 0-5V, 30MHz

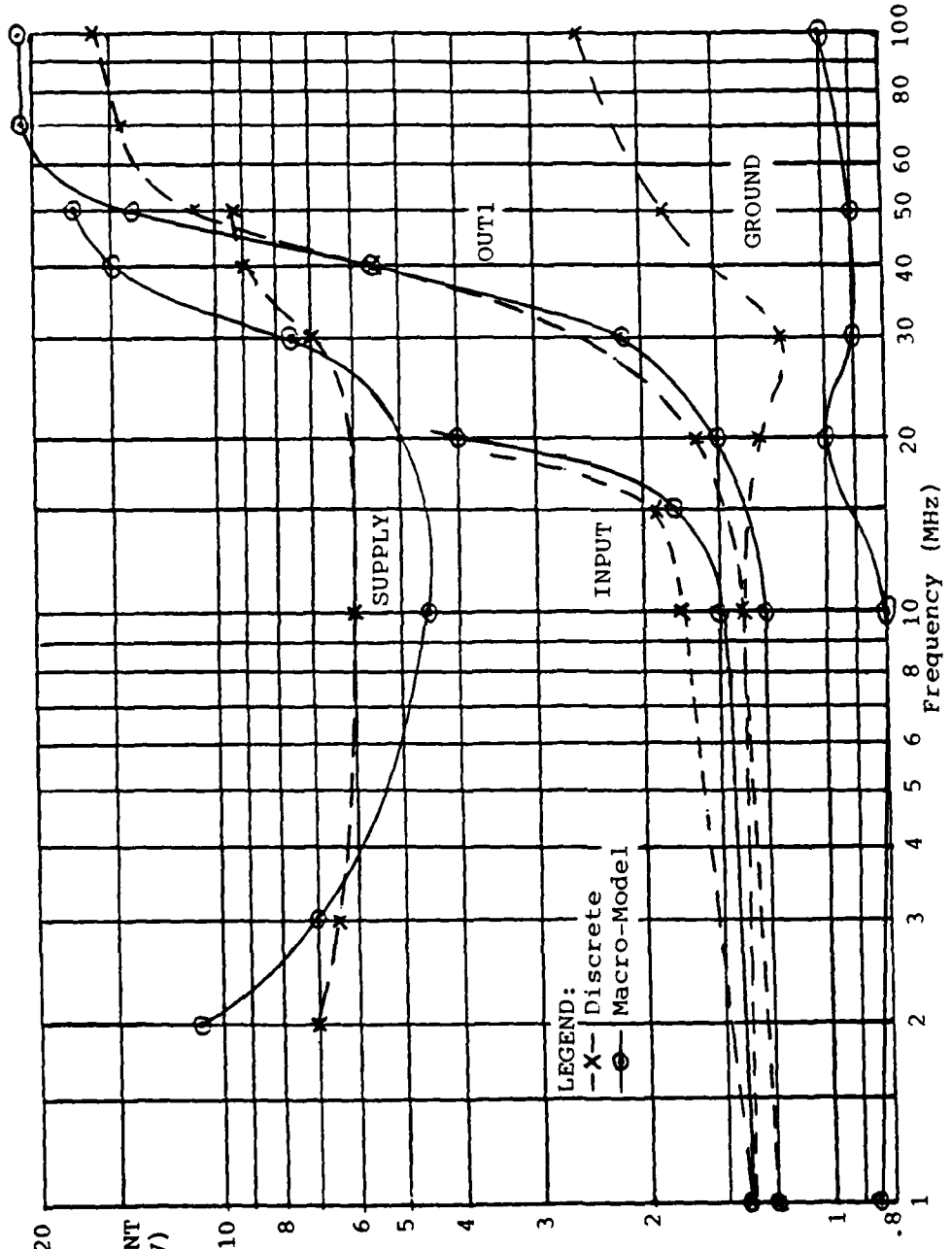


FIGURE 38: Interference Voltage to Produce VOUT2 = 1.5V vs. Frequency

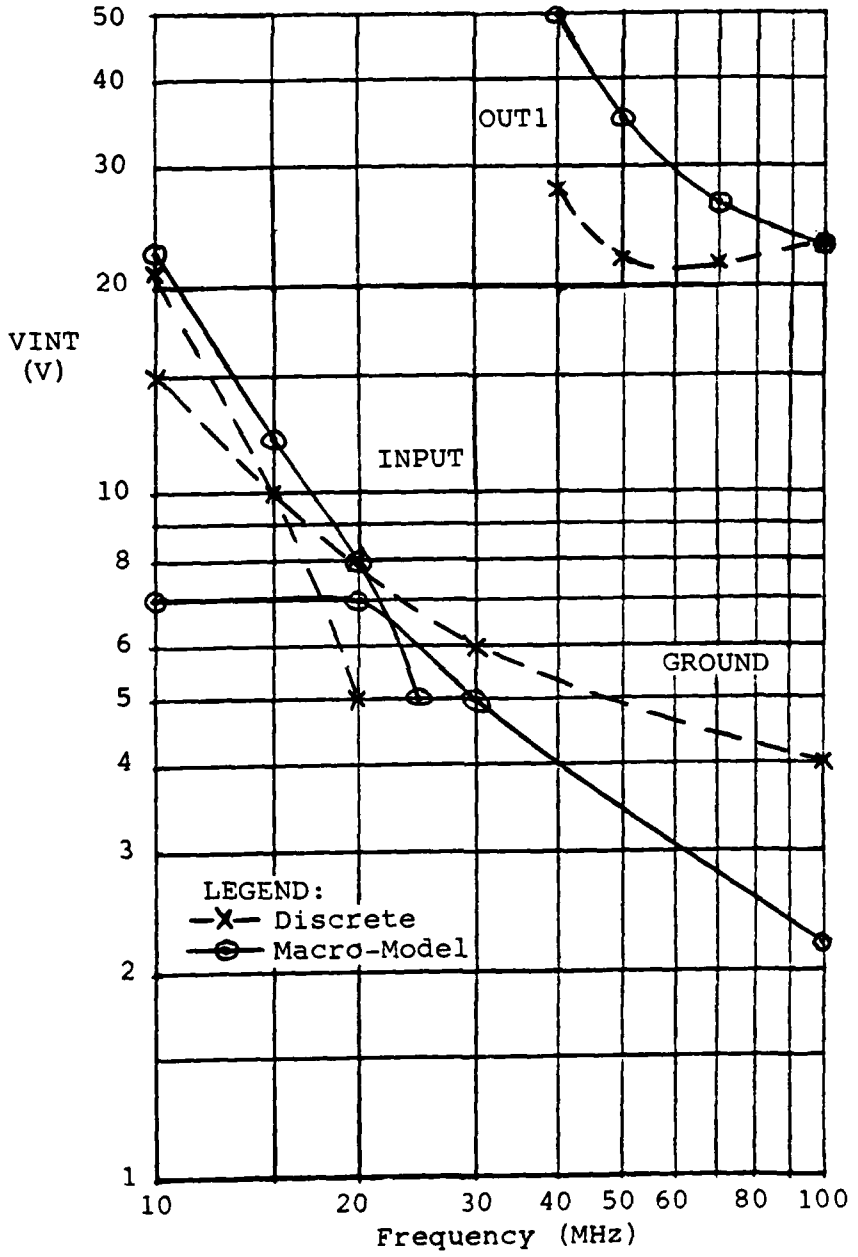


FIGURE 39: Interference Voltage to Produce Continuous VOUT2 < 1.0V vs. Frequency

5. MODELING OF A LARGE LOGIC CIRCUIT

In this chapter, a procedure will be developed to allow the modeling of large logic circuits in a minimum of CPU time within the confines of SPICE. A particular case study on this will be presented here: the modeling of a TTL 5485 four bit comparator[2]. For this purpose, the following requirements will be used as guidelines:

1. Model must be logically correct for any combination of inputs and outputs.
2. Output LOW and HIGH levels and logic threshold must be within the specs.
3. Input and output impedances must be reasonably correct.
4. Propagation delay times must be appropriate for any input-to-output combination.
5. Transient waveform should resemble typical response.

The external terminal connections of the comparator are shown in figure 40. The truth table given in table 5 shows all possible relationships between the 11 inputs and 3 out-

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[2] 'Microcircuits, Digital, TTL, Magnitude Comparators, Monolithic Silicon', USAF Military Specifications, MIL-M-38510/150B, January 1976

puts. The topology in logic format is shown in figure 41, and the associated transistor-level representation in figure 42.

Using figure 41, the comparator can be described in terms of logic elements as containing:

```
        18, 2-input gates
         2, 3-input gates
         2, 4-input gates
         7, 5-input gates
         2, 6-input gates
        ------------------
Total: 97 inputs, 31 gates
```

Since the realization is already in a multilevel sum of products form, logical simplification would not result in a significant decrease in the number of gates present, so a SPICE model will need to be developed which follows the logic diagram as defined while using the minimum complexity which will still fulfill the requirements.

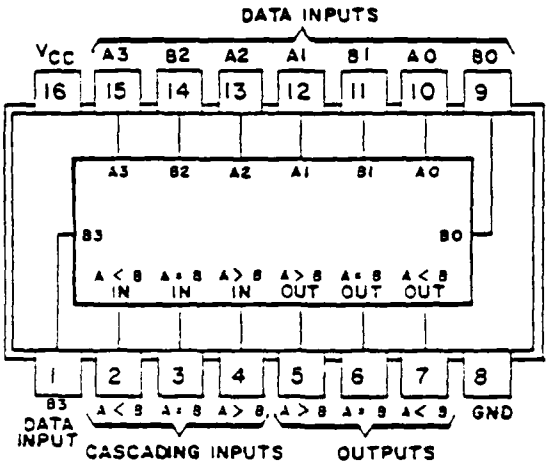

FIGURE 40: External Pinout of Comparator

TABLE 5: Truth Table for Comparator

Comparing Inputs				Cascaded Inputs			Outputs		
A3,B3	A2,B2	A1,B1	A0,B0	A>B	A=B	A<B	A>B	A=B	A<B
A3>B3	X	X	X	X	X	X	H	L	L
A3<B3	X	X	X	X	X	X	L	L	H
A3=B3	A2>B2	X	X	X	X	X	H	L	L
A3=B3	A2<B2	X	X	X	X	X	L	L	H
A3=B3	A2=B2	A1>B1	X	X	X	X	H	L	L
A3=B3	A2=B2	A1<B1	X	X	X	X	L	L	H
A3=B3	A2=B2	A1=B1	A0>B0	X	X	X	H	L	L
A3=B3	A2=B2	A1=B1	A0<B0	X	X	X	L	L	H
A3=B3	A2=B2	A1=B1	A0=B0	H	L	L	H	L	L
A3=B3	A2=B2	A1=B1	A0=B0	L	H	L	L	H	L
A3=B3	A2=B2	A1=B1	A0=B0	L	L	H	L	L	H
A3=B3	A2=B2	A1=B1	A0=B0	X	H	X	L	H	L
A3=B3	A2=B2	A1=B1	A0=B0	H	L	H	L	L	L
A3=B3	A2=B2	A1=B1	A0=B0	L	L	L	H	L	H

LEGEND: H=High level L=Low level X=irrelevant

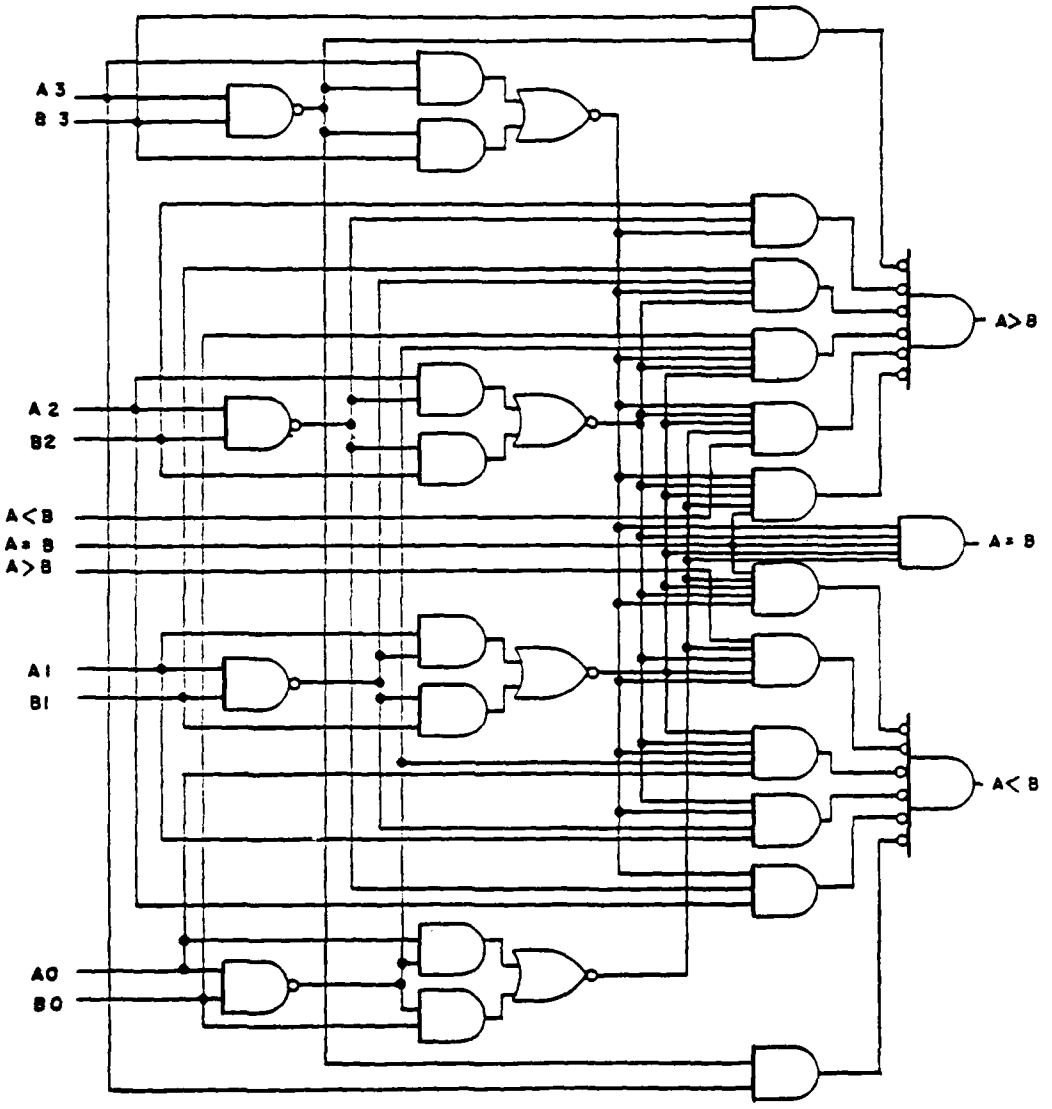

FIGURE 41: Logic Gate Representation

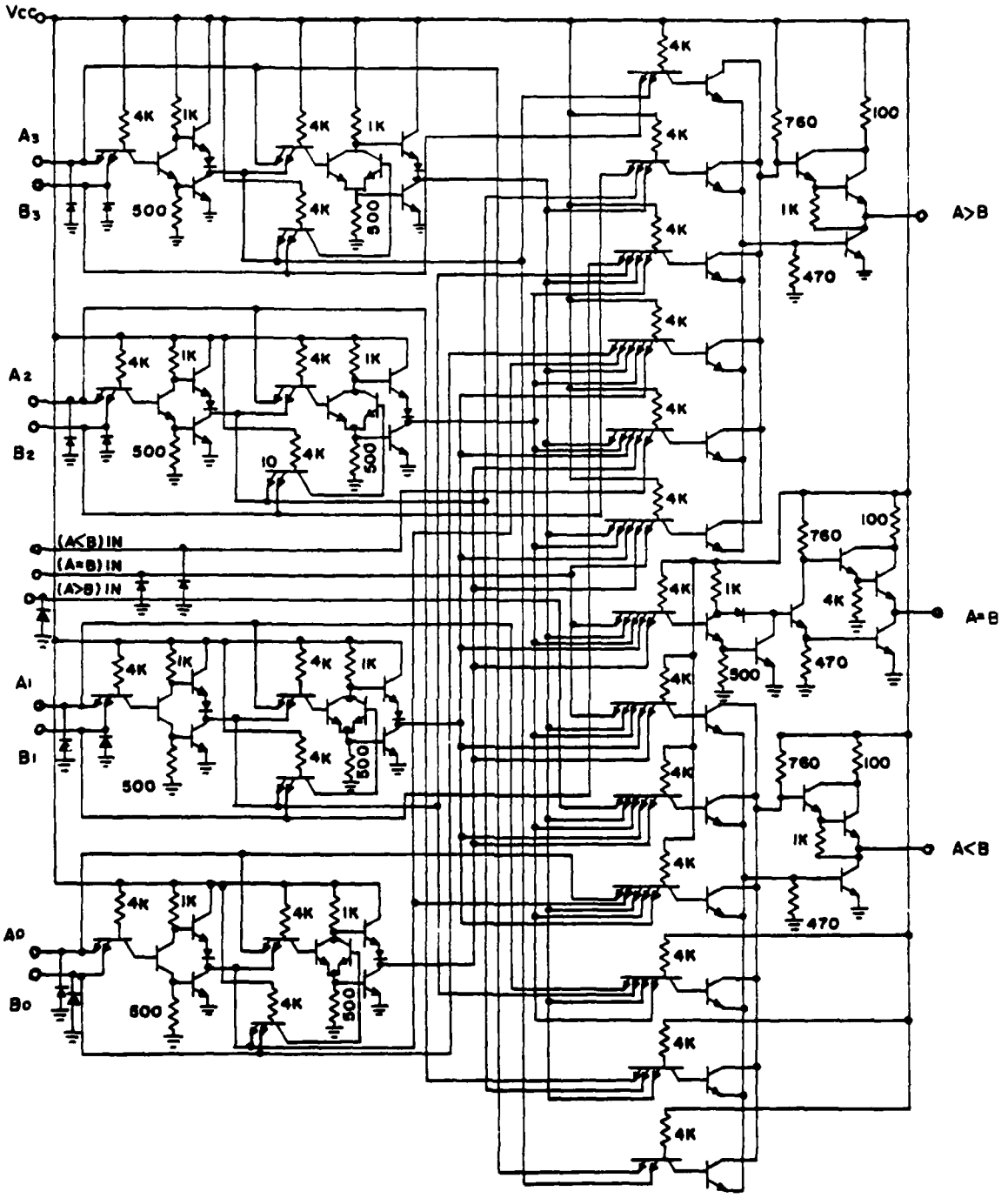

FIGURE 42: Internal Device-Level Schematic

TOPOLOGY DEVELOPMENT CONSIDERATIONS

Developing a procedure to convert such a complicated device into a SPICE model is neither a simple nor straightforward task. There are no logical elements in the SPICE language, only diodes, transistors, resistors, linear dependent sources, and so on. The NAND gate model created in Chapter 1 could of course be reconstructed in the AND-OR-INVERT (AOI) format used in the comparator which would yield a model which essentially parallels the discrete transistor representation in figure 42. While this would certainly give a very accurate model, it would contain around a hundred transistors and similarly large numbers of the other elements, obviously much too complex of a model if it is to be used as just a part of a larger circuit.

On the other hand, there is a limit on the minimum number of active devices which must be used to produce a logic model in SPICE: Each logical gating action is a nonlinear function, which therefore sets a requirement of one active device (diode or transistor) per logic gate, yielding an absolute minimum of 31 active devices for the fourbit comparator.

A simple example of a single diode logic gate is shown in figure 43. In this case, three input voltages, VA, VB, and VC are used as the arguments of linear dependent sources to provide current for diode D. Thus if all inputs are at 0V, no current would flow through the diode, so the output vol-

tage would be 0V. If at least one of the inputs was significantly above 0V, the diode would turn on and the output voltage would be equal to the 'on' voltage of the diode. The function is therefore a logical OR, with the low level at 0V and the high level dependent on the diode parameters and linear gain coefficients specified. This function could be further improved upon by adding a shunt resistance to the diode so that small currents would not immediately turn it on, and a shunt capacitor could add a simple first order time constant to the response to help model the switching delay time.

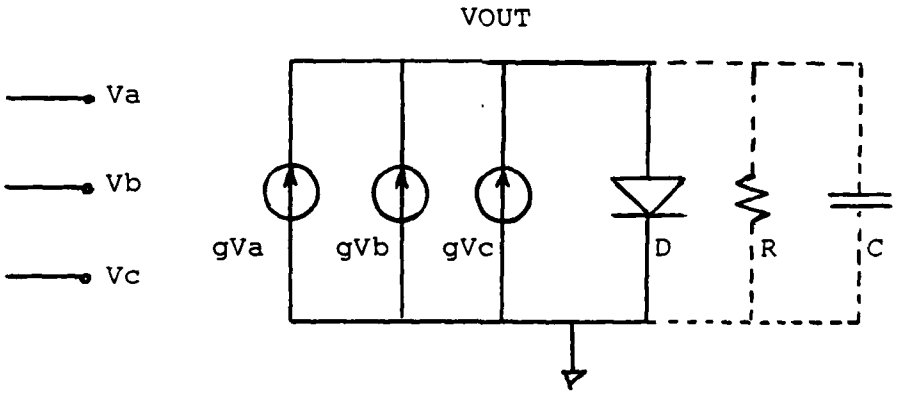

FIGURE 43: Single Diode Logical OR Gate Example

NAND AND AOI EQUIVALENT FUNCTIONS

The greatest single factor that causes the macro-model NAND gate to have so many transistors present when adapted to the four bit comparator is the fact that the NAND model requires a transistor for each input to each gate for the purpose of modeling the input current vs voltage characteristic. However, the current/voltage relationships inside the comparator model are of no interest to the user as long as the external nodes are modeled correctly. The input transistors can be replaced by diodes with little loss of the operating characteristic, but that simply means the 97 input transistors are converted into 97 input diodes, still too many for the simple operation that they are performing.

One method of circumventing this problem is by using a separate buffer circuit on each of the 11 inputs to roughly model the external current/voltage relationship at that point, then replacing all of the diodes within the comparator with linear dependent current sources. A NAND gate built using this methodology is shown in figure 44.

Note the resemblance between this format and the first half of the *NAND model in Chapter 1*: The input current sources represent the base-emitter diode of each input transistor; R1 remains unchanged; C1 represents the collector substrate capacitance, CCS; and D2 is the series connection of the base-collector diode junction and diode D2 of the original macro-model.

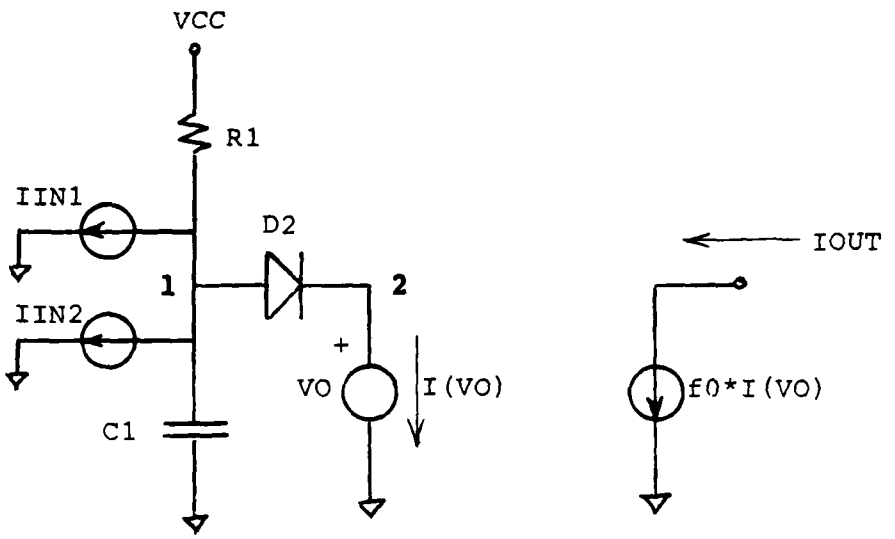

FIGURE 44: NAND Function Using Current-Based Inputs

Using the input transistor analogy, a LOW input voltage would correspond to maximum current flow out of the input of the device, while a HIGH input voltage would correspond to roughly zero input current. Checking figure 44 we see that if all inputs are HIGH (that is, all input currents are zero) then current will flow from VCC through R1 and D2, and into VO, so the output current which is linearly dependent on the current in VO will be at its maximum value, corresponding to a LOW voltage level to the next stage. If any of the inputs are at their LOW state (that is, at least one input with nonzero current) then the current flowing through R1 would sufficiently lower the voltage at node 1 so that

diode D2 would not be turned on. In this case, no current would flow through VO and therefore no output current, corresponding to a HIGH voltage level to the next stage. Thus the NAND function is being realized correctly.

One significant difference does become apparent in this model when more than one input turns on: Since each input current source would pull its current through R1, each one would drop the voltage at node 1 by the same amount, so that when several inputs turn on, the node 1 voltage can drop to a substantial negative value. This does not change the DC input/output characteristic, but during transient analysis capacitor C1 would cause greatly differing delay times, depending on how many inputs turn off together. For this reason, capacitor C1 must be excluded from the circuit in all cases except that of a single-input inverter. The delay characteristics must therefore be added elsewhere.

An AND-OR-INVERT stage can be constructed using several NAND gates as defined above followed by an OR gate similar to the example described previously (the logical function does work out correctly due to the automatic inversion inherent in the output current). This model is shown in figure 45.

To get the capacitive time constant in the OR stage into a symmetric format (regardless of the number of gates switching on or off) and to also keep the output voltage reasonably independent of the number of gates, a choice of

R4 and the parameters of D4 should be made so that, when one of the OR'd inputs is on, most of the current is flowing into the resistor, but any more that turn on will dump their current essentially directly into the diode. In this way, all additional 'on' inputs will be handled immediatly by D4, so that the output voltage is reasonably immune to changes in the number of 'on' inputs, but during discharge just a small drop in the output voltage will cause the diode to turn off, leaving just the R4*C4 time constant for relatively symmetric charging and discharging.

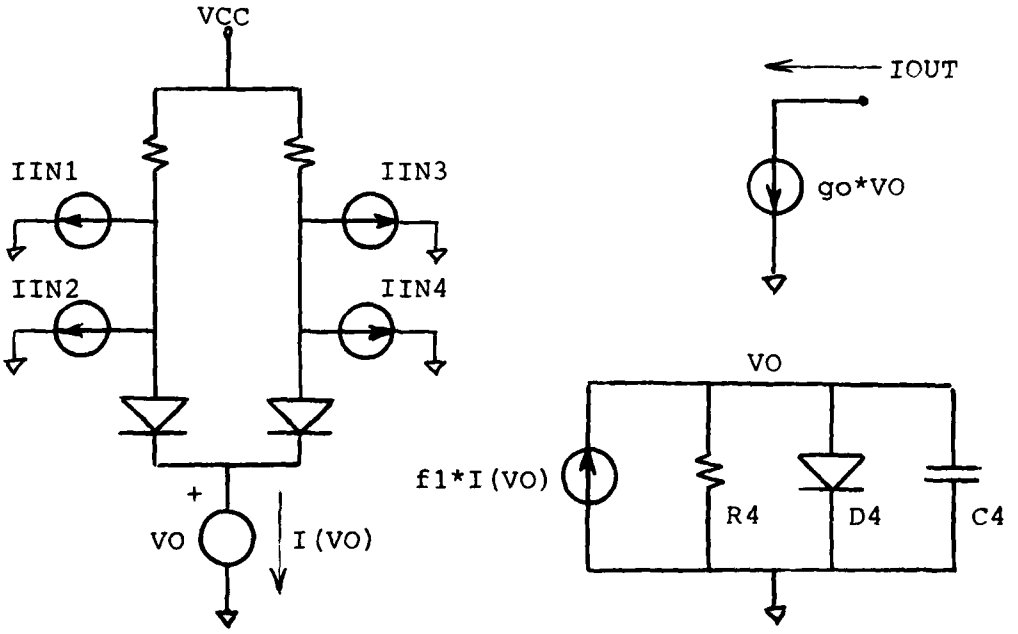

FIGURE 45: AND-OR-INVERT Gate Format

INPUT AND OUTPUT STAGES

Now that the essential logic elements have been defined, the interface stages to the outside world must be specified. In figure 46 is a very simple input stage which uses a single diode to approximate the typical input current/voltage relationship. The approximation used can be seen from the sketch to match the input current fairly well at both low and high voltage levels, while linearly connecting between the two regions so that a multiple diode circuit need not be synthesized to model the curve. Also, capacitor CS is added which helps to simulate the effect of substrate capacitance CCS of the input transistor in the device, which adds unidirectional delay when the input switches from LOW to HIGH.

The output stage shown in figure 47 is essentially the same as the last half of the NAND macro-model. The current drive provided by G1 is analogous to the current which is supplied by D2 in the macro-model, and the linear region which was being defined as the dependence of G3 on Q4's base voltage is not present since the DC transfer relationship no longer needs to be so precisely defined.

This stage provides a fairly sharp turn-on characteristic which is needed to 'square up' the otherwise slow first order time constants produced by the earlier stages in the model. The output transistor and diode are used as they were in the macro-model to give the device separate low and high level output impedances, and diode D3 was retained so

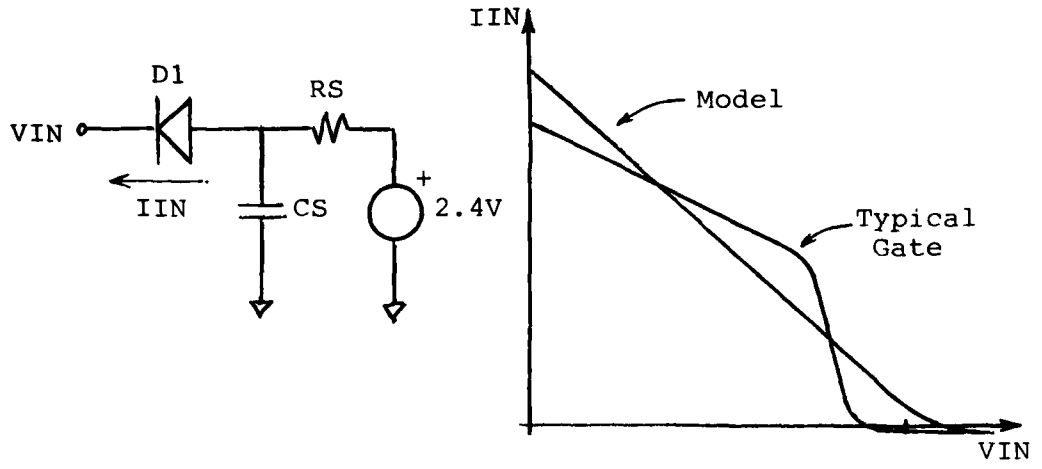

FIGURE 46: Input Buffer and input current approximation used

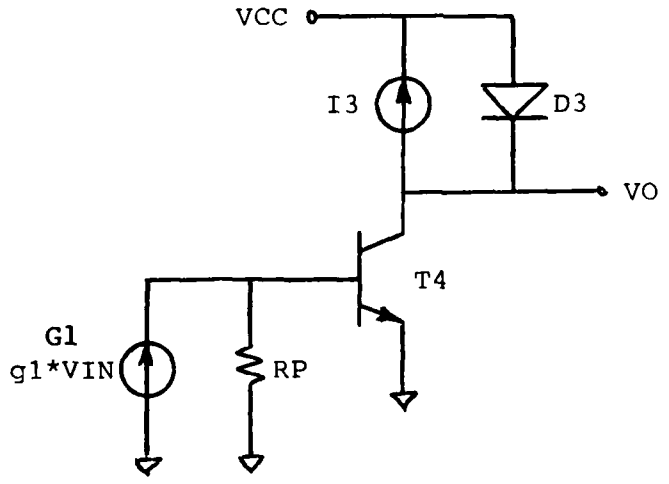

FIGURE 47: Output buffer stage

that positive voltage transients at the output node could turn off the output stage when in the HIGH state. Also, the storage time of the transistor can be used to provide a unidirectional delay on the output voltage low-to-high transition.

The actual parameter determination used will not be presented here, simply because it does not in actuality provide any new information. That is, all of the decisions on element and parameter values can be made by first understanding the relatively simple operation of the basic gates specified in figures 43-45; then choosing low, threshold, and high voltage and current logic levels; and solving for the resistor and diode parameter values. This parameter determination is no more complicated than that of finding the coefficients for a series or parallel combination of a diode and a resistor. The output stage would be analyzed in a manner analogous to that set forth for the macro-model in Chapter 1.

Similarly, the input to output delay characteristics can be matched in just a few iterations by first setting the R-C time constant on the AOI stage (which causes an essentially symmetric delay) to roughly match the minimum delays required by each path through the circuit (differing paths from input to output pass through a different number of gates, causing differing delay times). Then, the unidirectional delay coefficients (the input stage capacitor C1 and

output stage transistor storage time constant TR), can be used to add more delay in the paths with nonsymmetrical delay characteristics.

In Appendix 2 is a summary of each of the subcircuits used to construct the four bit comparator model, and the actual SPICE listing of the model and test circuit are in Appendix 3.

RESULTS OF COMPARATOR SIMULATIONS

In figure 48 is the results of a SPICE DC analysis of the four bit comparator model. All inputs initially started at zero volts (except for a 3V signal on the A=B input), then the most significant bit of the A input, VA3, was swept from zero to 2.5V. The output signal is correctly generated as initially HIGH at the A=B output, signifying equal inputs, then the A=B output switches to LOW and the A>B output switches to HIGH when the input voltage crosses roughly 1.5 volts, around the center of the transition region.

In figure 49 is the input current/voltage relationship generated for one of the data inputs (note, the A<B and A>B inputs would have only one-third of this current, since they have a fanout of one rather than the fanout of three for the rest of the gates). The current level was matched so that it is between the spec limits of 2mA to 3.6mA for the LOW range of 0 to 0.8 volts and drops to a small negative value for HIGH inputs of greater than 2.0 volts.

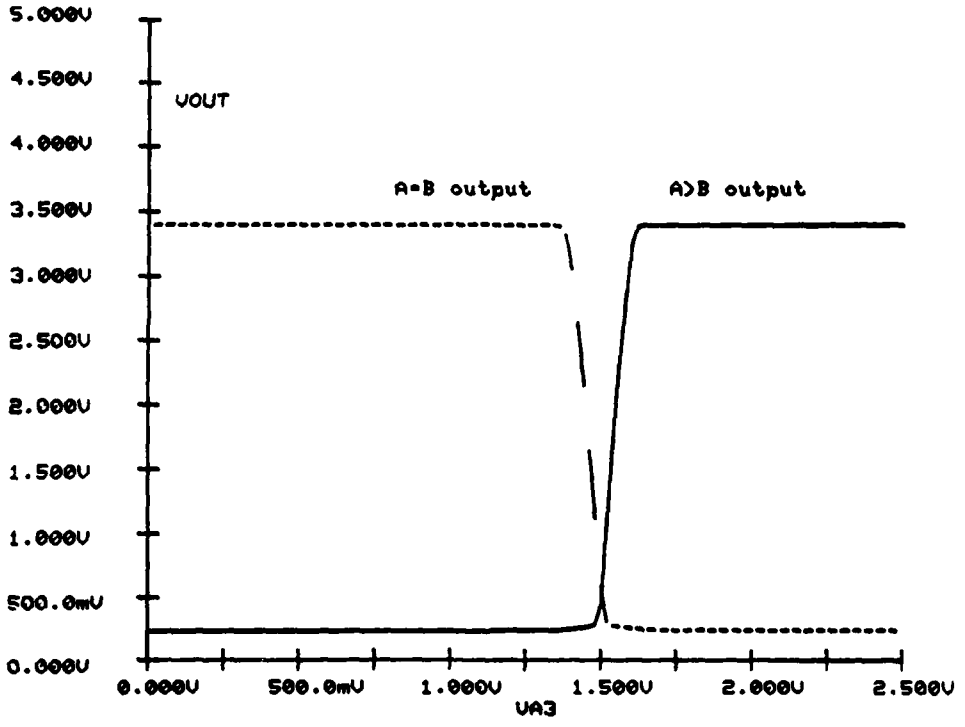

FIGURE 48: Comparator Output vs. Data Input Voltage

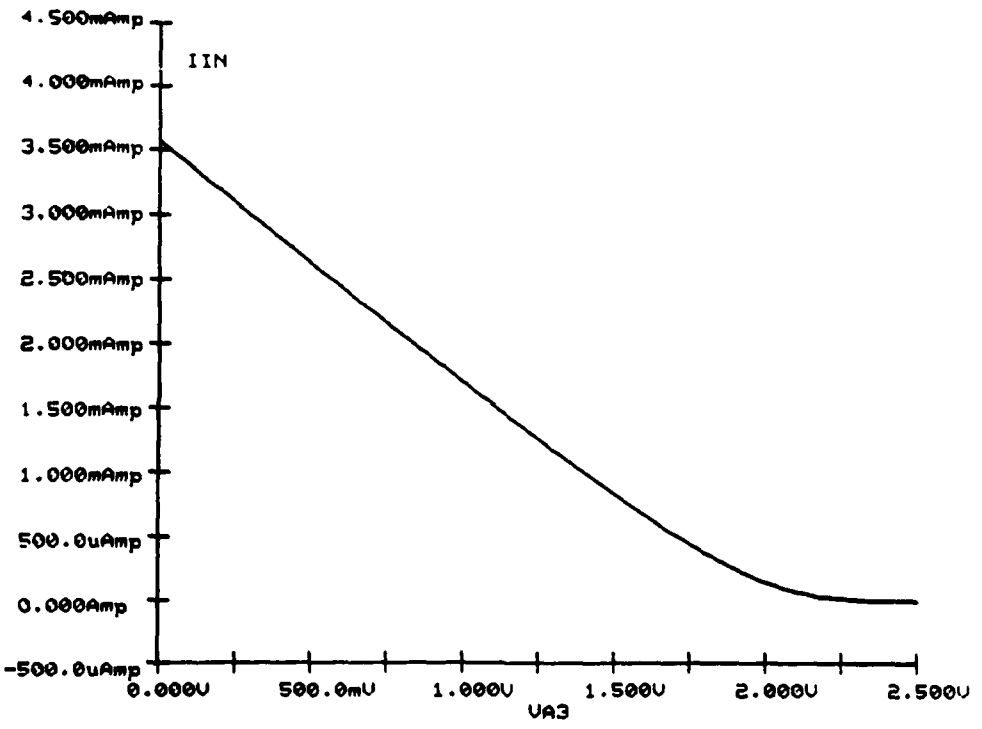

FIGURE 49: Comparator Input Current vs. Voltage

A transient analysis was also performed on the circuit using inputs VA3 and VB3 (the most significant bits of each input), switching from zero to three volts with 200ns pulses staggered by 100ns as shown in figure 50. The response at each of the outputs is shown in figure 51.

Initially both inputs are LOW so that the initial output is HIGH at the A=B output and low at the other two, indicating that the two inputs are equal. During the first 100ns, signal VA3 becomes HIGH so that the A>B signal switches to HIGH after the delay time. In the second 100ns, both inputs are HIGH, so equality is again achieved and the A>B signal drops back to LOW as the A=B output returns to its initial HIGH state. The A input then drops to LOW, so the A<B signal goes HIGH, and finally the B input also goes LOW, so the A=B output is again HIGH during the last interval.

In table 6 is a summary of the results from these and other tests, including propagation times from each data and control input to each of the outputs, compared with the spec sheet typical or maximum values.

The DC low and high output values, VOL and VOH, are well within the specs, as is the input current in the LOW state, IIL, for both the inputs with fanouts of 3 (all data inputs and A=B input) and with fanout of 1 (A<B and A>B inputs). The parameter VIC, which is the input voltage produced when 12mA of current is drawn from the input, is not quite matched due to the absense of the shunt diode on each of the

inputs (see figure 42). If this parameter was important in a particular instance, then that diode could simply be added to the model on the input or inputs desired. Finally, the short circuit output current, IOSC, is also well within specs.

Since only maximum values were specified for the propagation times, model propagation time values were fitted to roughly two-thirds of the maximum value. Actual values all fell within the range of 50% to 83% of the given spec maximum values.

The element count comparison at the bottom of table 6 shows just how much smaller the model is than the discrete representation in figure 42. Since each transistor consists of two diode junctions, two linear dependent sources, and two capacitances, then the model is seen to contain only one-sixth of the diodes junctions, one-third of the dependent sources, and one-eleventh of the number of capacitors, certainly much more favorable numbers than those of the original device. Although a simulation has not been attempted of the device-level circuit, an educated guess based on the ratios above might be that a decrease in computer time required for simulation of roughly a factor of five may be expected.

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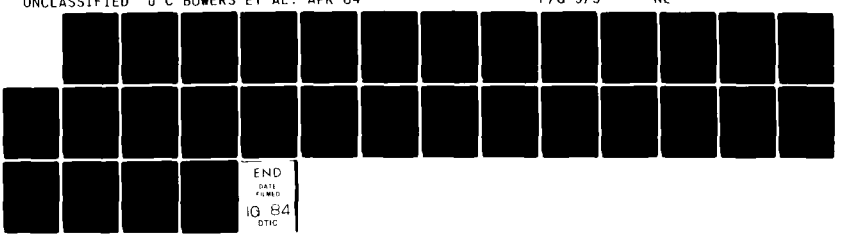

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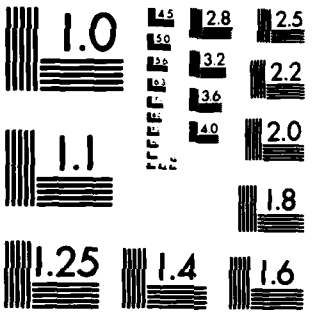

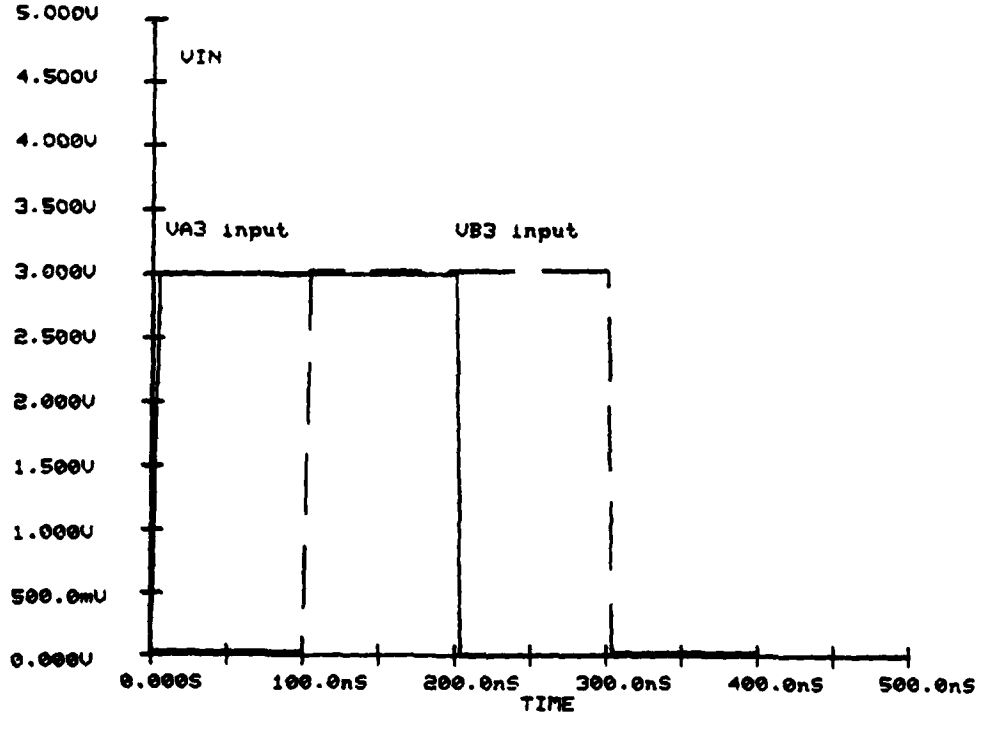

FIGURE 50: Data Input Signals for Transient Response Test

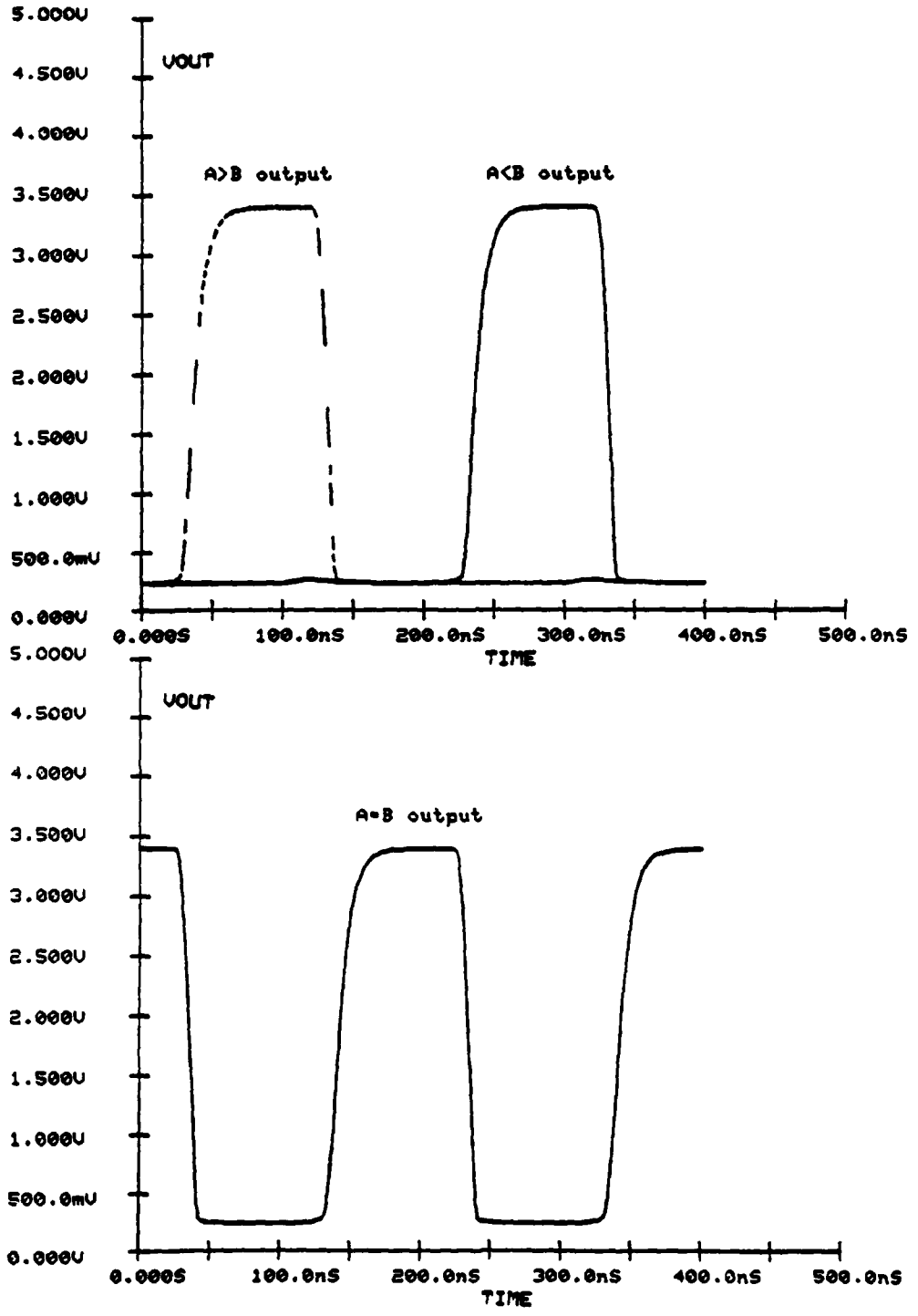

FIGURE 51: Comparator Output Voltages vs. Time

TABLE 6: Four Bit Comparator Results Summary

DC Parameters:

PARM	SPEC	MODEL	CONDITION
VOL	typ 0.2V	0.23V	normal load
	max 0.4V	0.38V	Iout=-16mA
VOH	min 2.4V	3.40V	Iout=400uA
IIL1	2.0 to 4.8mA	2.8mA	VIN=0.4V, all inputs
IIL2	0.7 to 1.6mA	.94mA	VIN=0.4V, <,> inputs
IIH	max 300uA	40uA	VIN=5.0V, all inputs
VIC	min -1.5V	-4V ***	Iin=12mA
IOSC	-20mA to -55mA	-24mA	output shorted

Transient Response Parameters:

		SPEC MAX		MODEL	
INPUT	OUTPUT	Tpd(LH)	Tpd(HL)	Tpd(LH)	Tpd(HL)
Data	<,>	38ns	43ns	29ns	26ns
Data	=	49ns	43ns	33ns	30ns
<,>	<,>	18ns	26ns	15ns	18ns
=	<,>	18ns	26ns	15ns	13ns
=	=	30ns	26ns	20ns	19ns

Element Count Comparison:

TYPE	DEVICE	MODEL	COMMENTS
Transistors	129	3	
Diodes	20	42	
Resistors	55	43	
Nodes	110	70	
Total Diode Junctions	278	48	1/6 of original
Total Dependent Srcs	258	86	1/3 of original
Total Capacitors	311	28	1/11 of original

SUMMARY AND CONCLUSIONS

In the first chapter of this report it has been shown that a well qualified model can be developed for a TTL logic gate from only external DC measurements and logic delay times, given a good knowledge of the internal topology of the gate. Using similar methods, other families of logic elements may be able to be modeled as well, although this may or may not be true based on the complexity of the gate involved. The added bonus of accurate interference effects at all nodes of the SPICE model is certainly a direct benefit of keeping the macro-model as near to the device as possible in all of its dominant modes of behavior.

The key to the SPICE macro-model's construction was in determining what internal devices (transistors Q2 and Q3) were noncritical to its overall response and what parameters were critical to the DC and transient responses so that simplification could be performed. After those discoveries were made, the parameter determination breaks down to an assault from both ends of the device working inward to solve for each of the element values and parameters required.

The SCEPTRE model constructed in Chapter 2, while not nearly as well qualified as the SPICE model, is still fully adequate in logic simulations, and the simplified model used in the last chapter shows that the complexity of the SPICE macro-model is not necessary when large combinational logic circuits need to be simulated, if the interference effects are not required.

Incidentally, if a FORTRAN subroutine capability were present in SPICE,* only the 11 external inputs and 3 outputs of the comparator would need to be modeled. The logic in between could be directly computed by a subroutine without resorting to diode-based logic functions otherwise required, and the delays could be either computed in the routine or added in the input and output stages. Using a model in that format could conceivably decrease the computer time required for simulation by as much as an order of magnitude.

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* This capability is contained, along with other interactive graphics features, in a program called I-GSPICE, commercially available from A. B. Associates, 1348 Eckles Drive, Tampa, Florida 33612. The U.S. Air Force does not recommend this program above other programs which may exist with the same capability.

APPENDIX 1

DIODE AND TRANSISTOR MODEL FORMATS USED FOR SPICE NAND MODEL DERIVATION

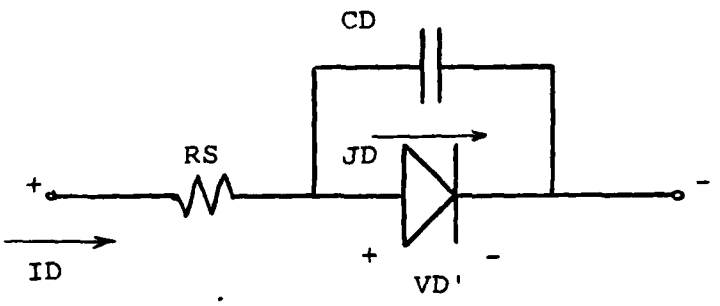

FIGURE A1: Diode Internal Representation

NAME	DEFAULT	DEFINITION
RS	0 ohms	Bulk series resistance
IS	.01 pA	Diode saturation current
N	1.0	Nonideal diode coefficient
CJO	0 pf	Junction capacitance
TT	0 ns	Diffusion capacitance time constant
VT	--	Constant kT/q = 25.85mV, where k=Boltzman's constant, T=Temperature (300K), and q=electron charge.

DEFINING EQUATIONS

```
JD = IS*(exp(VD'/(N*VT))-1)
CD = CJO/(1-VD')**.5 + TT*N*VT*(JD+IS)
```

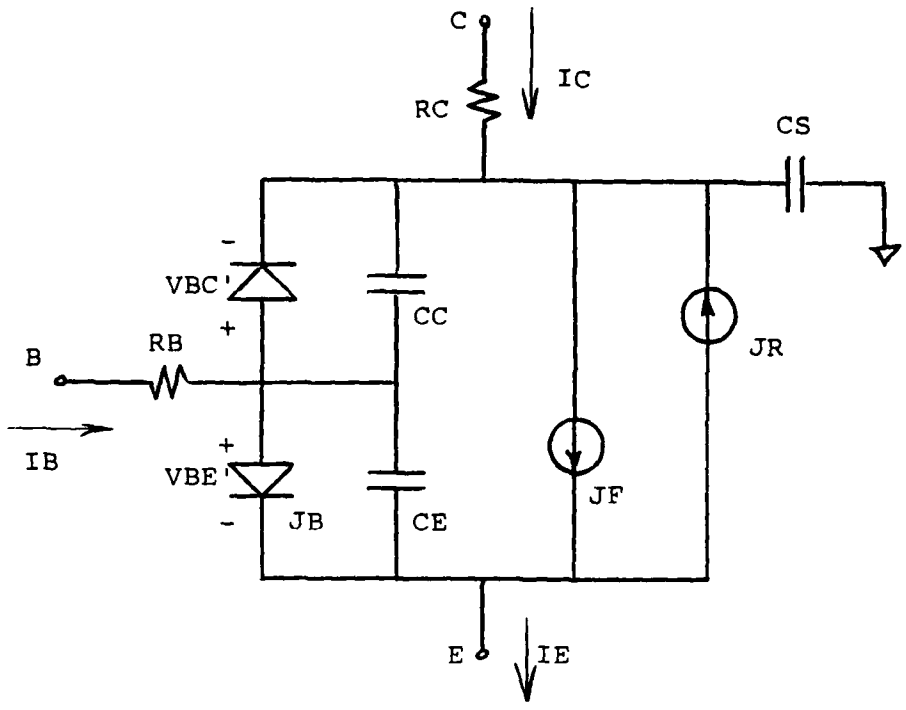

FIGURE A2: Transistor Internal Representation

NAME	DEFAULT	DEFINITION
RB,RC	0 ohms	Bulk base and collector resistances
IS	.01 pA	Intrinsic saturation current
BF,BR	100,1	Forward and reverse current gain
CJE,CJC	0 pF	Zero-bias junction capacitances
TF,TR	0 nS	Diffusion capacitance time constants
CCS	0 pF	Collector-substrate capacitance

DEFINING EQUATIONS

```
JF = BF*JB
JR = BR*JD
JB = (IS/BF)*(exp(VBE'/VT)-1)
JD = (IS/BR)*(exp(VBC'/VT)-1)
CE = CJE/(1-VBE')**.5 + TF*VT*(JB+IS)
CC = CJC/(1-VBC')**.5 + TR*VT*(JR+IS)
```

APPENDIX 2

SUBCIRCUITS USED IN FOUR BIT COMPARATOR MODEL

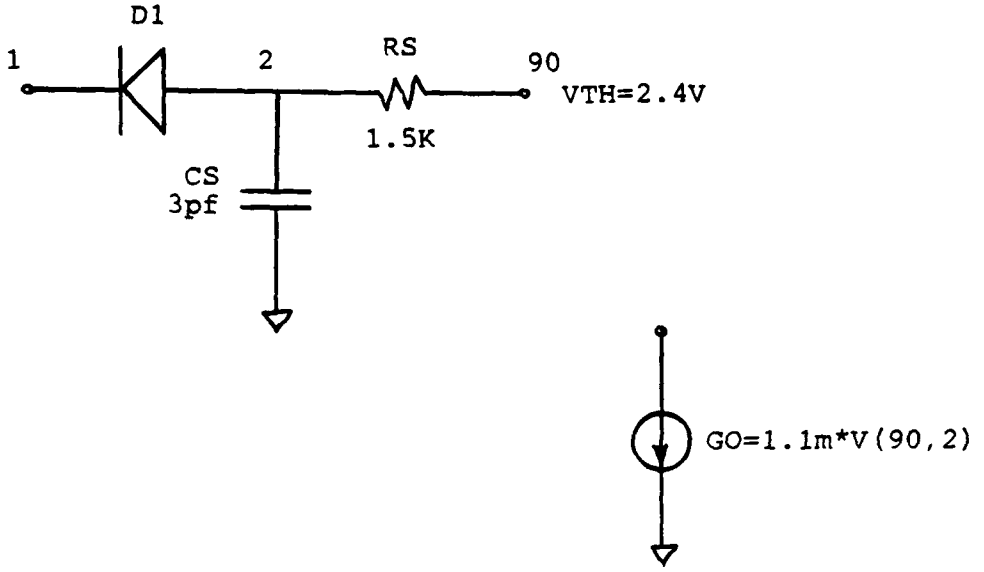

FIGURE A3: Subcircuit INBUF1

INPUT BUFFER - Approximates the input voltage vs. current characteristics and provides dependent current sources to drive following stages. A LOW input of 0.8V will result in a 0.8mA current drive to the next stage, while a HIGH input of at least 2.0V will result in roughly 0mA signal to the next stage.

INBUF3, INBUF3A and INBUF3B - Variants on the input buffer used to simulate inputs with differing fanout conditions.

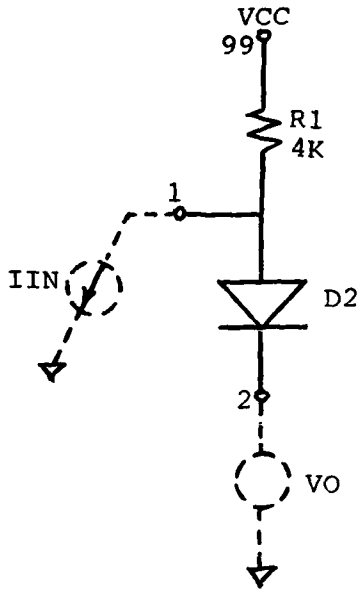

FIGURE A4: Subcircuit NAND

NAND GATE - All inputs (dependent current sources) are connected to node 1. This stage can be used as either a NAND gate, by connecting a zero-valued voltage source to node 2 and using a 1.25X current gain from I(VO) to the next stage, or as an input to an AND-OR-INVERT block, by connecting node 2 of each NAND directly to the AOI input node.

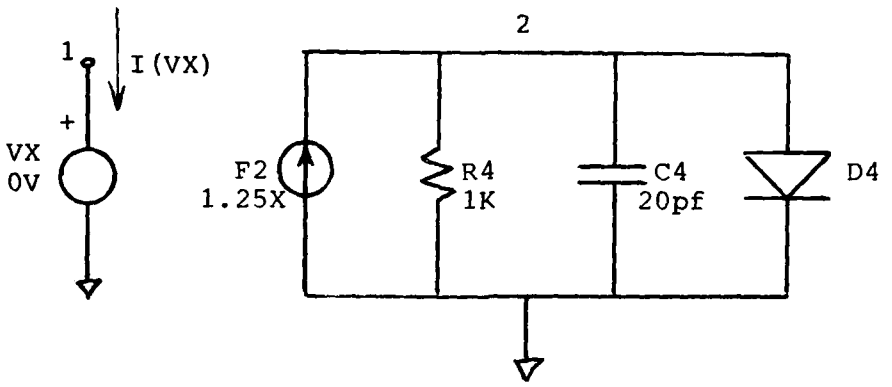

FIGURE A5: Subcircuit AOI

AND-OR-INVERT GATE - Must be driven by several NAND's connected to node 1. Or, if several of the logical-AND stages have the same inputs (see figure 41 -- the AND on the A=B output is identical to the ones just above and below) then only one needs to be simulated. The others can then be driven by unity gain current dependent current sources based on the output current of the one which is simulated. Node 2 voltage levels are 0.8V for LOW output, 0V for HIGH output. A gain of 1.2mmho should then be used to supply current drive to succeeding stages.

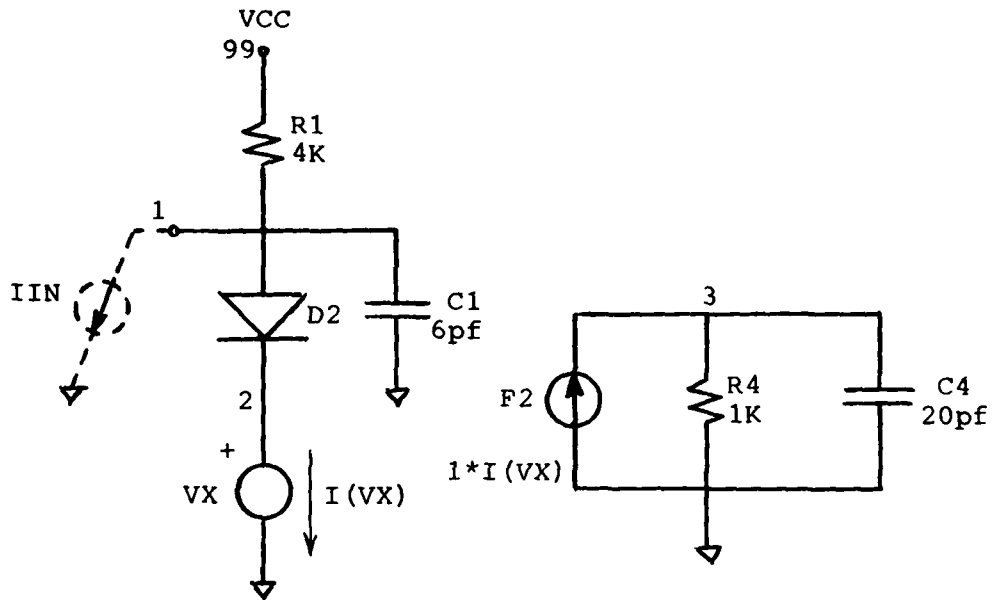

FIGURE A6: Subcircuit INVEQ

INVERT+DELAY - This stage is a logical inverter plus a separate delay stage for use on the A=B output of the device. Capacitor C1 has been added to the invert stage so that an extra unidirectional delay coefficient is available to better fit the A=B output's transient response.

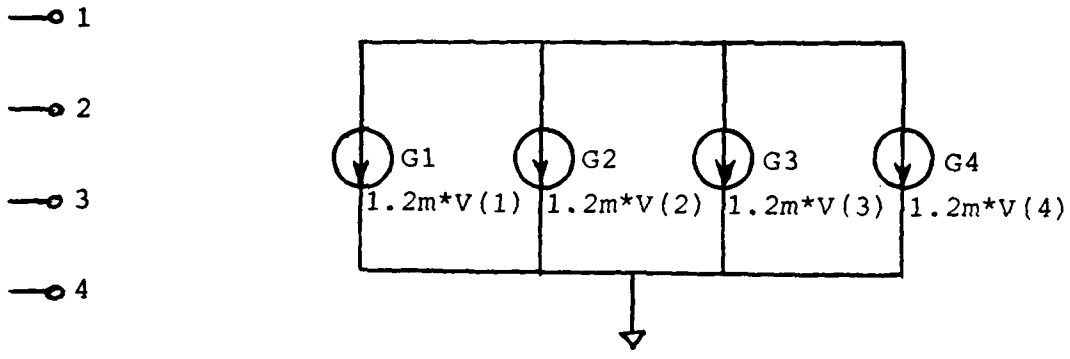

FIGURE A7: Subcircuit ADD4

VOLTAGE SUMMER - This subcircuit is included to simplify the coding of the five-input AND gates in the comparator. Its function is to connect four voltage controlled current sources each with a gain of 1.2mmho to provide the current drive to the individual AND gates in the second level of AOI gates.

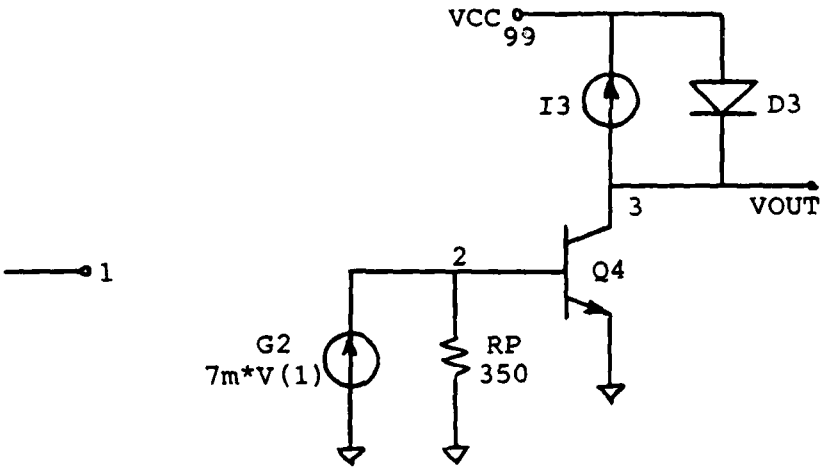

FIGURE A8: Subcircuit OUTBUF

OUTPUT BUFFER - This circuit is designed to switch from HIGH to LOW output states for a change of input voltage from 0.3 to 0.5 volts, which would come from the 0 to 0.8V output of a previous AOI stage. The operation is otherwise analogous to the last half of the macro-model NAND gate.

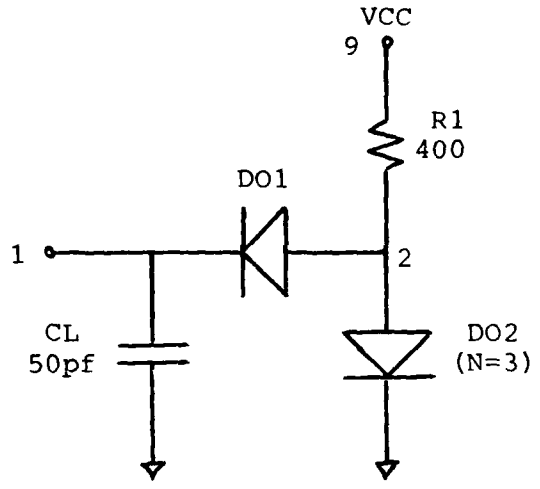

FIGURE A9: Subcircuit LOAD

LOAD STAGE - This is the load stage defined in the spec information. It simulates a fanout of 10 loading the output to which it is connected.

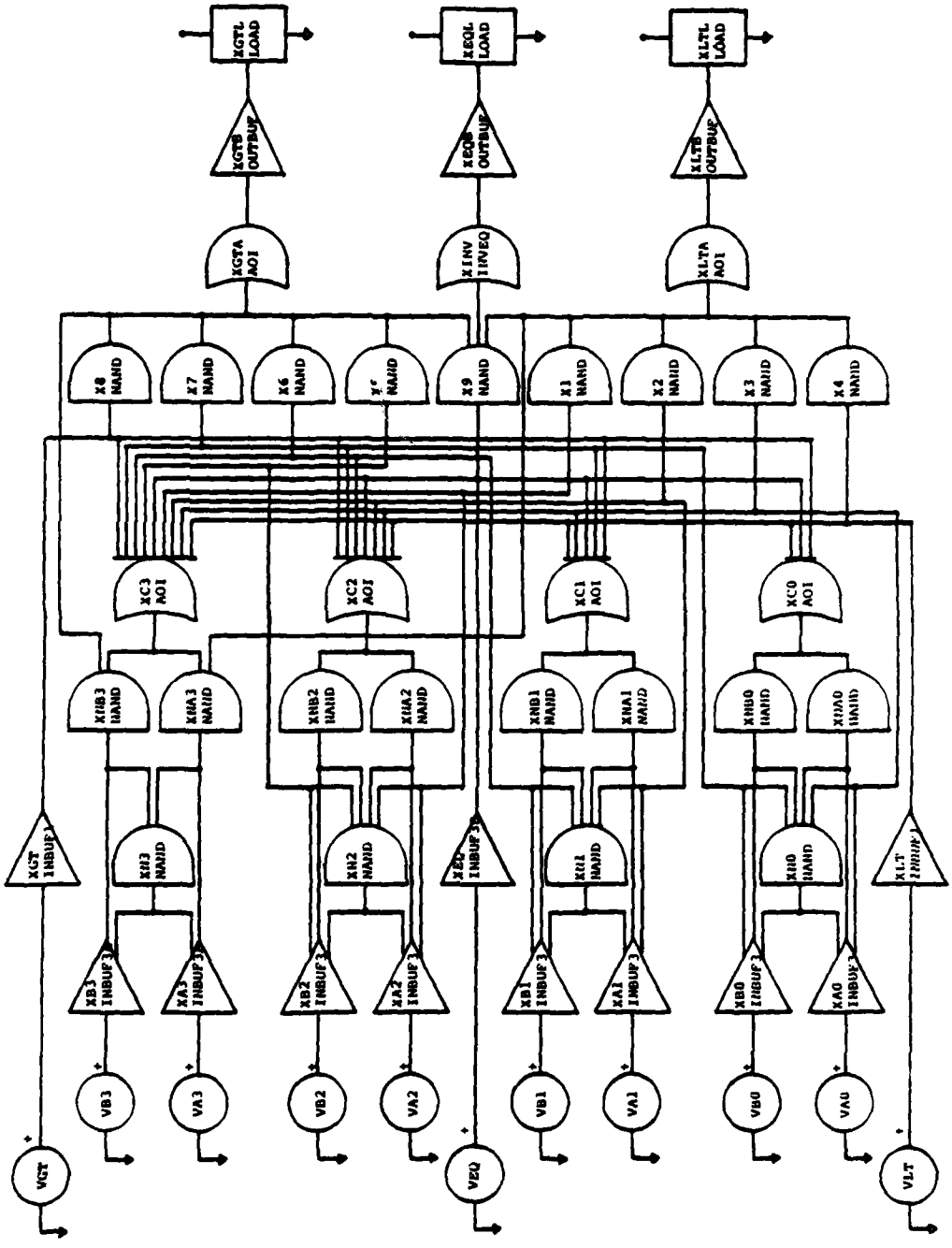

FIGURE A10: Connection Diagram for Subcircuits in the Comparator Model

(Note, the additional dependent current sources used for making connections are not included in this diagram.)

APPENDIX 3

SPICE AND SUPER*SCEPTRE TEST CIRCUIT LISTINGS

TABLE A1: SPICE NAND Gate Macro-Model and Load Stage

```
.MODEL DI    D(IS=1E-16 RS=60 CJO=1PF)
.MODEL T1 NPN(IS=7.52E-17 BF=.3 BR=.02
+              CJE=1PF CJC=1PF CCS=4PF)
.MODEL D2    D(IS=1.67E-18 CJO=.02PF TT=40PS)
.MODEL D3    D(IS=1.08E-16 N=2 RS=119 CJO=1PF)
.MODEL T4 NPN(IS=4.20E-16 BF=865 BR=27 RB=470 RC=10
+              TF=10PS TR=200PS CJE=.02PF)
*
.SUBCKT NAND   10 20  30  40
*7400 TTL GATE: INPUTS OUT VCC
Q1A 2 1 10 T1
Q1B 2 1 20 T1
DIA  0 10  DI
DIB  0 20  DI
R1  40 1   4.3K
D2   2 3   D2
R4   3 0   27.4K
Q4  30 3 0 T4
G3  30 40  (3,0)  10.1MA/V
D3  40 30  D3
.ENDS
*
.SUBCKT NANDL  10 20  30  40  50
*FAN-OUT = 10: INPUTS OUT VCC GND
Q1A 2 1 10 T1  10
Q1B 2 1 20 T1  10
DIA 50 10  DI  10
DIB 50 20  DI  10
R1  40 1   .43K
D2   2 3   D2  10
R4   3 50  2.74K
Q4 30 3 50 T4  10
G3  30 40  (3,50) 101MA/V
D3  40 30  D3  10
.ENDS
```

TABLE A2: SPICE NAND Gate Discrete Model and Load Stage

```
.MODEL DIO D(RS=60 TT=.1NS CJO=2PF PB=.6V BV=40V IS=1E-16)
.MODEL DIO3 D(RS=30 TT=.1NS CJO=2PF PB=.6V BV=40V IS=1E-16)
.MODEL TR1 NPN(BF=.316 BR=.02 RB=68 TF=.39NS TR=100NS RC=10
+ RE=1 VA=200V C2=1000 C4=1 CCS=2PF CJE=1PF PE=.7V ME=.33
+ CJC=.5PF PC=.5V MC=.33 KF=6.6E-16 IS=1E-16)
.MODEL TR2 NPN(BF=19.8 BR=.06 RB=75 TF=.39NS TR=100NS
+ RE=1 VA=200V VB=200V C2=1000 C4=1 CCS=2PF CJE=2PF PE=.7V
+ ME=.33 CJC=1PF PC=.5V MC=.33 KF=6.6E-16 IS=1E-16)
.MODEL TR3 NPN(BF=17.2 BR=.082 RB=70 RC=10 TF=.39NS TR=100N
+ RE=10 VA=200 C2=1000 C4=1 CCS=2PF CJE=2PF PE=.7V ME=.33
+ CJC=1PF PC=.5V MC=.33 KF=6.6E-16 IS=1E-16)
.MODEL TR4 NPN(BF=21.7 BR=.106 RB=80 RC=10 TF=.39NS TR=100N
+ RE=1 VA=200V C2=1000 C4=1 CCS=2PF CJE=2PF PE=.7V ME=.33
+ CJC=1PF PC=.5V MC=.33 KF=6.6E-16 IS=1E-16)
*
.SUBCKT NAND    1 10   8   9
*DEVICE-LEVEL: INPUTS OUT VCC
R1   2 9   4.38K
R2   9 4   1.43K
R3   9 6   .116K
R4   5 0   1.03K
D1   0 1   DIO
D2   0 10  DIO
D3   7 8   DIO3
Q11  3 2 1   TR1
Q12  3 2 10  TR1
Q2   4 3 5   TR2
Q3   6 4 7   TR3
Q4   8 5 0 TR4
.ENDS NAND
*
.SUBCKT NANDL   1 10   8   9   50
*DEVICE-LEVEL: INPUTS OUT VCC GND
R1   2 9   .438K
R2   9 4   .143K
R3   9 6   .0116K
R4   5 50   .103K
D1   50 1   DIO  10
D2   50 10  DIO  10
D3   7 8    DIO3 10
Q11  3 2 1   TR1 10
Q12  3 2 10  TR1 10
Q2   4 3 5   TR2 10
Q3   6 4 7   TR3 10
Q4   8 5 50 TR4 10
.ENDS NANDL
```

TABLE A3: SPICE NAND Gate DC and Transient Response Test Circuit

```
NAND GATE DC AND TRANSIENT RESPONSE - 10X FANOUT LOADING
VIN  90 0  PULSE(.2V 3.4V 8NSD 4NSR 4NSF 46NSPW)
VCC  99 0  5VDC
*
**** MACRO-MODEL TEST CIRCUIT
* LOAD STAGE IS EQUIVALENT OF 10X FANOUT TO NAND GATES
*
XM 10 20 30 99  1 2 3  MACRO
V1  10 90  0V
V2  20 0   3.4V
VO  30 31  0V
XL  31 99 32 99  MACROL
RL  32 0   400
CL  32 0   15PF
*
**** DISCRETE MODEL TEST CIRCUIT
* DISCRETE OUTPUT VOLTAGES CONTAIN "5", I(V)'S CONTAIN "D"
* ALSO, INTERNAL NODES RENUMBERED TO CORRESPOND WITH MACRO.
*
XD 15 25 35 99  51 52 53  DISCRETE
V1D 15 90  0V
V2D 25 0   3.4V
VOD 35 36  0V
XLD 36 99 37 99  DISCRL
RLD 37 0   400
CLD 37 0   15PF
*
**** GENERATE DC CHARACTERISTIC CURVES
*
.DC VIN 0V 2V .01V
.PLOT DC V(30) V(35) I(V1) I(V1D) I(VO) I(VOD)
.PLOT DC V(1) V(51) V(2) V(52) V(3) V(53)
.PLOT DC V(32) V(37)
*
**** TRANSIENT RESPONSE TO INPUT PULSE
*
.TRAN .5NS 100NS
.PLOT TRAN V(30) V(35) I(VO) I(VOD) I(V1) I(V1D)
.PLOT TRAN V(10) V(1) V(51) V(2) V(52) V(3) V(53)
.PLOT TRAN V(32) V(37)
.OPT METHOD=GEAR
.LIBRARY BOTH
.END
```

TABLE A4: Typical Interference Test Circuit

```
NAND INTERFERENCE VOLTAGE:   3OUT-100MEGHZ HI-HI
***TRANSIENT ANALYSIS***
.TRAN 1NS 100NS
.PLOT TRAN V(10,8) V(5) V(21) V(10)
.PLOT TRAN I(VIN1) I(VIN2) I(VCC) I(VO1)
.OPT METHOD=GEAR ITL5=50K LIMPTS=1001
***INTERFERENCE SOURCES***
VXA    21 0  PWL(0 0  1NS 15V 100NS 25V)
VXB    22 0  SIN(0DC 1VAC 100MEGHZ)
RXX    21 22 1
*
V1IN   1 3   0
V2PWR  9 4   0
G3OUT  5 16 POLY(2) (21,0) (22,0) 0 0 0 0 100X
R3OUT  5 16 0.01
V4GND  8 0   0
***INPUT SOURCES***
VIN1   1 0   3.4VDC
VIN2   2 0   3.4VDC
VCC    9 0   5VDC
***CIRCUIT***
XN1    3 2 5  4     NAND
XN2    6 7 10 4 8   NANDL
VO1   16 6   0VPROBE
VL2    7 8   3.4V
RL    10 8   400
CL    10 8   15PF
***MODELS***
.LIBRARY NAND
.LIBRARY NANDL
.END
```

TABLE A5: SUPER*SCEPTRE DC and Transient Response Test Circuit

```
CIRCUIT DESCRIPTION
 TEST OF NAND GATE DC AND AC RESPONSE
ELEMENTS
 EIN, 0-1 = XIN(PDC*TIME + PTRAN*XTABLE(T1,TIME))
 DEIN = XIND(PDC+PTRAN*1E9*XTABLE(T2,TIME))
 ND,  1-2-3-0 = MODEL NAND (PERM,PRINT)
 EHI, 0-2 = 3
 JL,  3-0 = XL(10*XTABLE(TIND,VJL))
 CL,  3-0 = 20E-12
DEFINED PARAMETERS
 PDC=0, PTRAN=0
FUNCTIONS
 TABLE 1 = 0,0, 8E-9,0, 12E-9,3, 58E-9,3, 62E-9,0, 1,
 TABLE 2 = 0,0, 8E-9,0, 8.01E-9,.75, 12E-9,.75,12.01E-9,0,
     58E-9,0, 58.01E-9,-.75, 62E-9,-.75, 62.01E-9,0, 1,0
OUTPUTS
 VJL(VOUT), EIN(VIN), IEIN(IIN), PLOT
 JAND, ICAND, PVND, E1ND, VC1ND, PCND, C1ND, PLOT
RUN CONTROLS
 STOP TIME = 1E-6
 INTEGRATION ROUTINE = IMPLICIT
 IC FOR RERUNS = MASTER RESULTS
 MINIMUM STEP SIZE = 1E-30
 MAXIMUM PRINT POINTS = 0
RERUN DESCRIPTION
 DEFINED PARAMETERS
  PDC=1
 RUN CONTROLS
  STOP TIME = 2
  MAXIMUM STEP SIZE = .02
  MAXIMUM PRINT POINTS = 100
RERUN DESCRIPTION
 DEFINED PARAMETERS
  PTRAN=1
 RUN CONTROLS
  STOP TIME = 100E-9
  MAXIMUM STEP SIZE = 1E-9
  MAXIMUM PRINT POINTS = 200
END
```

TABLE A6: Four Bit Comparator Subcircuits

```
*** SUBCIRCUITS AND MODELS
.MODEL DIO1 D(IS=9NA N=2)
*
.SUBCKT INBUF1  1  3   90
*INPUT BUFFER: VIN IO VTH=2.4VDC
* INPUT IS STANDARD TTL LEVELS
* OUTPUT CURRENT SIMULATES SINK CURRENT TO NAND GATE INPUT:
* 'LO'=0.8MA, THRESHOLD=0.4MA, 'HI'=0MA.
D1  2 1  DIO1
RS  2 90 1.5K
CS  2 0  3PF
GO  3 0  (90,2) 1.1MX
.ENDS
*
.SUBCKT INBUF3  1   3 4 5   90
*INPUT BUFFER: VIN OUTPUTS VTH
* SAME AS INBUF1, BUT FOR INPUT WHICH CONNECTS TO 3 GATES.
D1  2 1  DIO1 3
RS  2 90 0.5K
CS  2 0  1PF
G1  3 0  (90,2) 1.1MX
G2  4 0  (90,2) 1.1MX
G3  5 0  (90,2) 1.1MX
.ENDS
*
.SUBCKT INBUF3A  1  3 4  90
*INPUT BUFFER:  VIN OUT VTH
* SAME AS INBUF3, BUT ONLY TWO DEPENDENT SOURCES.
D1  2 1  DIO1 3
RS  2 90 0.5K
CS  2 0  1PF
G1  3 0  (90,2) 1.1MX
G2  4 0  (90,2) 1.1MX
.ENDS
*
.SUBCKT INBUF3B  1   3   90
*INPUT BUFFER:  VIN OUT VTH
* INBUF3 WITH JUST 1 OUTPUT & DELAY FOR 'EQ' INPUT
D1  2 1  DIO1 3
RS  2 90 0.5K
CS  2 0  6PF
G1  3 0  (90,2) 1.1MX
.ENDS
*
.MODEL DIO2 D(IS=66FA N=3)
.MODEL DIO4 D(IS=0.2PA N=1.5)
```

TABLE A6 (cont'd)

```
.SUBCKT NAND  1  2  99
*NAND GATE:  IN IO VCC
* DRIVE WITH CURRENT SINK: >.8MA='LO', 0MA='HI'
* OUTPUT CURRENT (NODE 2) MUST BE TO GROUND POTENTIAL
* USE DEPENDENT SOURCE OF GAIN 1.2X TO DRIVE FURTHER STAGES
* OR SUM DIRECTLY INTO AND-OR-INVERT (AOI) SUBCIRCUIT.
R1  99 1  4K
D2   1 2  DIO2
.ENDS
*
.SUBCKT AOI      1  2
*AND-OR-INV+RC: IN VO
* DRIVE WITH SUM OF NAND OUTPUTS FLOWING INTO NODE 1
* OUTPUT LEVELS ARE >0.8V='LO', 0V='HI'
* USE DEPENDENT SOURCE GAIN 1MA/V TO DRIVE FURTHER STAGES
VX  1 0  0V
F2  0 2  VX  1.25X
R4  2 0  1K
C4  2 0  20PF
D4  2 0  DIO4
.ENDS
*
.SUBCKT INVEQ  1  3  99
*INVERTER:   IN VO VCC
* INVERT+DELAY STAGE FOR 'EQ' OUTPUT
R1  99 1  4K
C1   1 0  6PF
D2   1 2  DIO2
VX   2 0  0V
F2   0 3  VX  1X
R4   3 0  1K
C4   3 0  20PF
.ENDS
*
.MODEL DIO3 D(IS=43NA N=2 RS=140 CJO=1PF)
.MODEL TR4 NPN(BF=20 BR=4 RC=9 IS=10FA CJE=1PF TR=.5NS)
*
.SUBCKT OUTBUF   1   3   99
*OUTPUT BUFFER: VI VOUT VCC
* INPUT IS VOLTAGE FROM AOI OUTPUT
* OUTPUT IS STANDARD TTL LEVELS
G2  0 2  (1,0) 7MA/V
RP  2 0  350
Q4 3 2 0 TR4
D3 99 3  DIO3
I3  3 99 7MA
.ENDS
```

TABLE A6 (cont'd)

```
.SUBCKT LOAD   1   9
*LOAD STAGE: VOUT VCC
CL   1 0   50PF
D1   2 1   DO1
D2   2 0   DO2
RL   9 2   400
.MODEL DO1 D(N=1 IS=1PA CJO=1PF TT=1NS)
.MODEL DO2 D(N=3 IS=1PA CJO=1PF TT=1NS)
.ENDS
*
.SUBCKT ADD4  1 2 3 4  5
*COMPUTE IOUT=(V1+V2+V3+V4)*1M AS CURRENT SINK.
G1   5 0   (1 0)   1.2MX
G2   5 0   (2 0)   1.2MX
G3   5 0   (3 0)   1.2MX
G4   5 0   (4 0)   1.2MX
.ENDS
```

TABLE A7: Four Bit Comparator Test Circuit

```
FOUR BIT COMPARATOR TEST
*** INPUT VOLTAGE SOURCES
VA0   1 0   0V
VA1   2 0   0V
VA2   3 0   0V
VA3   4 0   PULSE(0V 3V 0NSD 2NSR 2NSF 198NSPW)
VB0   5 0   0V
VB1   6 0   0V
VB2   7 0   0V
VB3   8 0   PULSE(0V 3V 100NSD 2NSR 2NSF 198NSPW)
VLT   9 0   0V
VEQ  10 0   3V
VGT  11 0   0V
*
VCC  99 0   5V
VTH  90 0   2.4V
*
*** INPUT BUFFERS
XA0   1 21 31 53 90   INBUF3
XA1   2 22 32 52 90   INBUF3
XA2   3 23 33 51 90   INBUF3
XA3   4 24 34    90   INBUF3A
XB0   5 21 35 57 90   INBUF3
XB1   6 22 36 56 90   INBUF3
XB2   7 23 37 55 90   INBUF3
XB3   8 24 38    90   INBUF3A
XLT   9 58       90   INBUF1
XEQ  10 59       90   INBUF3B
XGT  11 54       90   INBUF1
*
*** FIRST LEVEL OF NAND GATES
XN0   21 25 99   NAND
XN1   22 26 99   NAND
XN2   23 27 99   NAND
XN3   24 28 99   NAND
VN0   25 0   0V
VN1   26 0   0V
VN2   27 0   0V
VN3   28 0   0V
*
*** NAND2 + AOI2
XNA0   31 41 99   NAND
XNA1   32 42 99   NAND
XNA2   33 43 99   NAND
XNA3   34 39 99   NAND
VNA3   39 44      0V
XNB0   35 41 99   NAND
XNB1   36 42 99   NAND
XNB2   37 43 99   NAND
XNB3   38 40 99   NAND
VNB3   40 44      0V
```

TABLE A7 (cont'd)

```
FIA0   31 0    VN0 1.2X
FIA1   32 0    VN1 1.2X
FIA2   33 0    VN2 1.2X
FIA3   34 0    VN3 1.2X
*
FIB0   35 0    VN0 1.2X
FIB1   36 0    VN1 1.2X
FIB2   37 0    VN2 1.2X
FIB3   38 0    VN3 1.2X
*
XC0   41 45   AOI
XC1   42 46   AOI
XC2   43 47   AOI
XC3   44 48   AOI
*
*** NAND'S FOR A<B
FNA3    0 69    VNA3    1.2X
*
X1     51 69 99  NAND
F1N2   51 0     VN2     1.2X
G1C3   51 0     (48,0)  1.2MX
X2     52 69 99  NAND
F2N1   52 0     VN1     1.2X
G2C3   52 0     (48,0)  1.2MX
G2C2   52 0     (47,0)  1.2MX
X3     53 69 99  NAND
F3N0   53 0     VN0     1.2X
X3G3   48 47 46 0 53  ADD4
X4     54 69 99  NAND
X4G4   48 47 46 45 54 ADD4
*
FLT    99 69      VAND 1.2X
*
*** NAND'S FOR A>B
FNB3    0 71    VNB3    1.2X
*
X5     55 71 99  NAND
F5N2   55 0     VN2     1.2X
G5C3   55 0     (48,0)  1.2MX
X6     56 71 99  NAND
F6N1   56 0     VN1     1.2X
G6C3   56 0     (48,0)  1.2MX
G6C2   56 0     (47,0)  1.2MX
X7     57 71 99  NAND
F7N0   57 0     VN0     1.2X
X7G3   48 47 46 0 57  ADD4
X8     58 71 99  NAND
X8G4   48 47 46 45 58 ADD4
*
FGT    99 71    VAND   1.2X
```

TABLE A7 (cont'd)

```
*** NAND+INVERT FOR A=B
X9     59 62 99  NAND
X9G4   48 47 46 45 59 ADD4
*
VAND   62 0      0V
*
XINV   63 75 99  INVEQ
FINV   63 0      VAND   1.25X
*
*** AOI+BUFFER+LOAD FOR OUTPUTS
XLTA   69 74     AOI
XLTB   74 79 99  OUTBUF
XLTL   79 99     LOAD
*
XEQB   75 80 99  OUTBUF
XEQL   80 99     LOAD
*
XGTA   71 76     AOI
XGTB   76 81 99  OUTBUF
XGTL   81 99     LOAD
*
*** DC TRANSFER CURVE
.DC VA3 0V 2.5V .02V
.PLOT DC V(79) V(80) V(81) (0,4V)
.PLOT DC V(74) V(75) V(76) (0,1V)
.PLOT DC V(48) V(47) V(46) V(45) (0,1V)
.PLOT DC I(VA3) (-2M,6M) I(VN3) I(VNA3) I(VNB3) I(VAND)
*
*** TRANSIENT ANALYSIS
.TRAN 2NS 400NS
.PLOT TRAN V(79) V(80) V(81) (0,4V)
.PLOT TRAN V(74) V(75) V(76)(-.5,1.5V)
.PLOT TRAN V(45) V(46) V(47) V(48) I(VA3)
.PLOT TRAN I(VN0) I(VN3) I(VNA3) I(VNB3) I(VAND)
.OPTIONS METHOD=GEAR ITL5=10K  ACCT
.END
```

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