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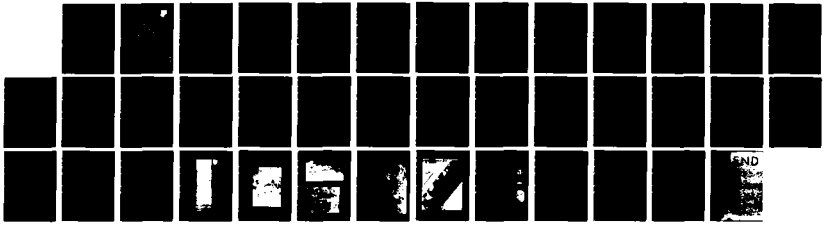

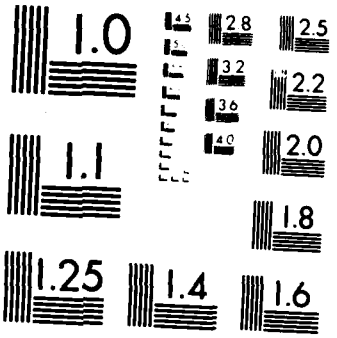

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PREPARATION AND EVALUATION OF ZnSe AND ZnS_xSe_{1-x} EPITAXIAL LAYERS ON Ge SUBSTRATES FOR APPLICATIONS IN SURFACE PASSIVATION AND HETEROJUNCTION DEVICES

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This report summarizes a detailed study of ZnSe and ZnS_xSe_{1-x} epitaxial growth on germanium and gallium arsenide substrates, for application in surface passivation and heterojunction devices. These layers were prepared by a novel low pressure, low temperature organometallic chemical vapor deposition (OM-CVD) process. Both nominally undoped, intrinsic ZnSe and Al-doped, highly conductive n-type ZnSe were prepared by this method.

Excellent epitaxial growth was achieved as indicated by the large intensity in the near bandgap photoluminescence and the rather weak intensity in the self-activated luminescence spectra. This indicates a low concentration of intrinsic and extrinsic defects and a low compensation ratio. An important relationship was observed between reproducibility of layer characteristics and substrate and reactor preparation. Also, deep center luminescence revealed that ZnSe layers deposited on both GaAs and Ge (100) surfaces have luminescence

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properties superior to those deposited on other substrate orientations.

This study revealed a large disparity in the electrical conductivity depending on substrate orientation, of Al-doped, n-type ZnSe layers deposited both on GaAs and Ge Substrates. The conductivity of layers deposited on (100) substrates is usually at least one order of magnitude larger than the conductivity of layers grown on (110) or (111) substrates. As a result of SIMs and mobility measurements, we conclude that this anisotropy is related to the growth morphology and the defect structure observed in our high resolution TEM work.

During the course of this work, the defect structure of ZnSe layers grown on (100), (110), and (111)B GaAs, and on (100) and (111) Ge substrates were imaged for the first time by high resolution transmission electron microscopy. It was found that ZnSe grows in epitaxial fashion on all substrates orientations. The defect structures are also similar. Surprisingly, fewer defects are seen in ZnSe grown on Ge (111) than in ZnSe grown on GaAs (111)B. This effect is most likely due to the slight misorientation of the Ge substrate which facilitates nucleation.

ZnSe-Ge heterojunctions were successfully fabricated and reflect the orientation dependence of interface properties and layer resistivity in their current - voltage characteristics. Heterojunctions formed on (100) p-Ge, show a much reduced dark saturation current and a better diode behavior, when compared with heterojunctions formed on (111) p-Ge. By measuring the turn-on voltage V_T in the MIS capacitance curve, the interface state density at the ZnSe-Ge (100) interface was estimated to be in the order of $\sim 10^{11}$ cm^{-2}.

17. Cosati Codes (Continued)

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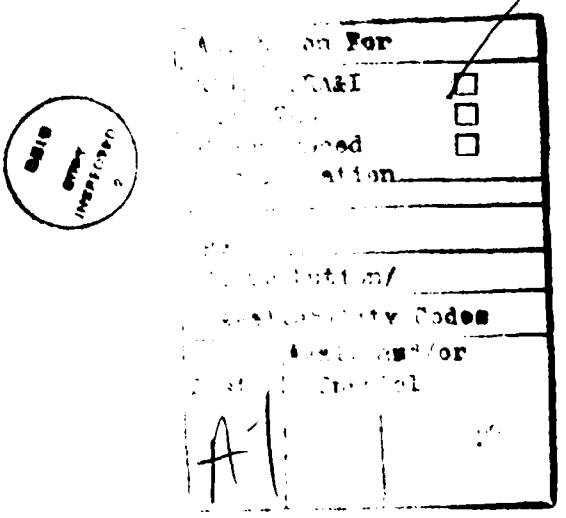

Report Summary

The work during the duration of this contract focused on the deposition and evaluation of ZnSe and ZnS_xSe_{1-x} layers deposited on gallium arsenide and germanium substrates for applications in surface passivation and heterojunction devices. These layers were prepared by a novel low pressure, low temperature organometallic chemical vapor deposition (OM-CVD) process. Both nominally undoped, intrinsic ZnSe and Al-doped, highly conductive n-type ZnSe were prepared by this method. The large intensity in the near bandgap photoluminescence and the rather weak intensity in the self-activated luminescence spectrum of the as-grown layers indicate a low concentration of intrinsic and extrinsic defects and a low compensation ratio.

We have found that in order to achieve reproducible physical properties, extreme care has to be exercised in cleaning the substrates and maintaining a water- and oxygen-free atmosphere in the reactor. We have investigated the relationship between substrate cleaning, substrate orientation, and deep center luminescence in great detail and have found that ZnSe layers deposited on both GaAs and Ge (100) surfaces have luminescence properties superior to those deposited on other substrate orientations.

We have also investigated the large anisotropy in the electrical conductivity, depending on substrate orientation, on Al-doped, *n*-type ZnSe layers deposited both on GaAs and Ge substrates. The conductivity of layers deposited on (100) substrates is usually more than one order of magnitude larger than the conductivity of layers grown on (110) substrates. The dark conductivity of *n*-ZnSe grown on (111) substrates is consistently too small to be measured. SIMS measurements have confirmed that the dopant concentration is independent of the substrate orientation and corresponds closely to the observed electron concentration indicating a low compensation ratio. The measured electron mobility, on the other hand, exhibits a strong dependence on substrate orientation. We conclude that the anisotropy in the electrical conductivity is related to the growth morphology and the defect structure observed in our high resolution TEM work; a correlation with typical features in the photoluminescence spectra has been established.

During the course of this work, the defect structure of ZnSe layers grown on (100), (110) and (111)B GaAs, and on (100) and (111) Ge substrates has been imaged for the first time by high resolution transmission electron microscopy. The defects were imaged in cross section, both near the interface and in the bulk about 1 μm away from the interface. It was found that ZnSe grows indeed epitaxially on all substrates. The defect structure is also similar. Surprisingly, however, fewer defects are seen in ZnSe grown on Ge (111) than in ZnSe grown on GaAs (111)B. This effect is most likely due to the slight misorientation of the Ge substrate which facilitates nucleation.

ZnSe – Ge heterojunctions reflect the orientation dependence of the interface properties and of the electrical resistivity in their current – voltage chracteristics. Heterojunctions formed on (111) *p*-type Ge substrates exhibit a non-ideal diode behavior with a large dark saturation current dominated by tunnelling through interface states, possibly by a multistep tunnelling process. Heterojunctions formed on (100) *p*-Ge, on the other hand, show a much reduced dark saturation current and a better diode behavior; the current transport was found to be to be thermally activated.

By measuring the turn-on voltage V_T in the MIS capacitance curve, the interface state density at the ZnSe-Ge (100) interface was estimated to be in the order of $\sim 10^{11}$ cm^{-2}.

2.0 Objective of this investigation

ZnSe is a semiconductor with a large direct bandgap of ~2.7 eV at room temperature and has potential applications for light emitting devices emitting in the visible part of the spectrum. Because of its wide bandgap, it is transparent from ~5000 Å to the infrared and is a standard IR window material. Furthermore, ZnSe with a lattice constant of 5.667 Å is closely lattice matched to GaAs (5.6534 Å) and to Ge (5.658 Å) and is therefore attractive for heterojunction devices and for the surface passivation of GaAs and Ge which lack native oxides. The remaining small lattice mismatch between the GaAs or Ge substrates and the ZnSe layers can be overcome by adding a small amount of sulfur to form ZnS_xSe_{1-x}. The exact lattice match to GaAs occurs for $x = 0.052$ and to Ge for $x = 0.035$. Photoluminescence (PL) studies of epitaxial layers of ZnS_xSe_{1-x} lattice matched to GaAs suggest that the interface between ZnS_xSe_{1-x} and the GaAs substrates is much improved near the lattice matched composition [1]. This is evident from the width of the near-bandgap PL peak and the intensity of the self-activated (SA) PL which both have a minimum near $x = 0.05$ signifying a relief of the strain and a reduced number of defects at the interface. A similar improvement in the interface properties is expected for ZnS_xSe_{1-x} layers deposited on Ge substrates. The properties of ZnSe and of lattice matched ZnS_xSe_{1-x} deposited on germanium were the topic of this investigation and are reviewed in this report.

3.0 Technical results and important findings

In the following section, we will discuss the organometallic CVD process and the growth of undoped and doped, n-type ZnSe and ZnS_xSe_{1-x} layers on GaAs and Ge substrates and their physical properties. The investigation of the defect structure by high resolution transmission electron microscopy will provide insight into the role that defect play in the luminescent and electrical transport properties of the layers.

3.1 The organometallic CVD process

The feasibility of using organometallic compounds for the growth of II-VI semiconductors materials was first demonstrated by Manasevit and Simpson [2]. Not before 1978, however, was further work reported in the literature, although numerous groups were working during this time on wide bandgap semiconductors and the problems associated with doping. In 1978 two articles decribing the growth of ZnSe by OMCVD appeared [3,4], using relatively low growth temperatures of 340°C and 520°C, respectively, which should help reduce the degree of self compensation. The OMCVD process is inherently simple and lends itself to the preparation of large area devices at low cost.

A schematic of the reactor is shown in Fig. 1 and will be briefly described here. The reactor is a vertical reactor. The quartz tube has a diameter of 54 mm. The substrates sits on a SiC-coated graphite susceptor which is cut at an angle of ~45°. The susceptor is heated with quartz iodine lamps; the temperature during deposition is monitored with a chromel – alumel thermocouple inside a sealed stainless steel tube which also serves as a support for the susceptor. The reactor is evacuated using a Leybold-Heraeus Trivac pump suitable for corrosive service. The gases are introduced at the top of the reactor in a manner similar to the arrangement reported by Manasevit et al. [2]. The center tube carrying the organometallic zinc compound [dimethylzinc (DMZn)] and the dopant [triethylaluminum (TEAl)] extends inside the reator tube to about 2 cm above the substrate. This arrangement was found necessary in order to avoid deposition of reaction products forming in the gas phase. Hydrogen was used as a carrier gas. Hydrogen selenide was diluted to 10% in hydrogen.

Before a typical deposition run for a ZnSe epitaxial layer on GaAs, the GaAs substrate is first cleaned in trichlorethylene, then in acetone, followed by a rinse in deionized (DI) water. The substrate is then etched in a mixture of 5:1:1 H_2SO_4:H_2O_2:H_2O for about 1 min in order to remove surface damage resulting from cutting and polishing of the wafer. Finally, a potentially present oxide layer is removed by an etch in boiling HCl followed by a rinse in deionized (DI) water. The Ge substrate wafers are cleaned in the same fashion, except that the etching step in sulfuric acid is omitted. The substrate wafer is then positioned on the susceptor, the reactor is pumped down and leak tested using an *in situ* mass spectrometer. During that time, the flow rates are set up with the reactant gases bypassing the reactor. After the deposition temperature is reached, the various gases or gas mixtures are introduced either simultaneously or sequentially into the reactor at separate ports at the top in order to avoid unwanted chemical reactions between the gases before they reach the heated reaction zone. A layer with a typical thickness of ~5 μm is deposited in about one hour with the substrate temperature being held at ~350°C. The pressure in the reactor during the deposition is ~100 mTorr. Typical flow rates are ~3 ml/min of hydrogen through the bubbler containing the DMZ at 0°C, between 5 and 20 ml/min of hydrogen through the bubbler containing the TEAl, and 30 ml/min of 10% H_2Se in H_2. The dopant concentration is adjusted by varying the flow rate of H_2 through the TEAl cylinder and the temperature of the cylinder between 0 and 20°C. The flow rates are controlled using *Tylan* mass flow controllers (FC in Fig.1). The actual mass flow rates of the organometallic compounds are determined by metering the H_2 flow in front of the bubblers, assuming that the carrier gas is saturated with the organometallic compounds at its partial pressure. The total pressure in the bubblers is maintained at ~760 Torr during the deposition via a pressure controller (PC in Fig.1) which automatically adjusts the flow through a needle valve. After the desired layer thickness is reached, the heater is turned off and the sample is allowed to cool down in a H_2Se ambient in order to avoid loss of selenium.

The substrate preparation just before the growth was found to have a profound effect on the photoluminescence (PL) properties of the ZnSe layers, as shown in Fig.2. The PL was excited with a 10 mW He-Cd laser emitting at 3250 Å and

measured at 77 K. If the substrate was only cleaned in an organic solvent before growth, the near-bandgap PL peak is small compared with the self-activated luminescence. Etching in acid, as outlined above, improves the PL response, and the best PL response, at least for GaAs substrates, was obtained after in-situ etching in HCl gas at about 550°C.

3.2 The preparation of n-type ZnS_xSe_{1-x}

ZnSe layers prepared by OM-CVD without intentional doping are highly resistive. From capacitance-voltage measurements of ZnSe layers deposited on *n*-GaAs and from van der Pauw resistivity and Hall effect measurements of ZnSe layers deposited on Cr-doped semi-insulating GaAs substrates, we concluded that the electrical resistivity of these layers is greater than 10^5 Ω·cm.

Most recently, low-resistivity *n*-type ZnSe (ρ<0.05 Ω·cm) has been grown epitaxially on (100) GaAs substrates by OM-CVD.[5] Triethylaluminum was used as a dopant. Carrier concentrations at room-temperature range between 10^{15} and 10^{18} cm^{-3}, and mobilities between 200 and 400 $cm^2/(V·sec)$ have been measured. The layers exhibit a smooth surface morphology, and the PL spectra are dominated by the near-bandgap peak. Notably absent in the PL spectra are donor-acceptor pair bands, and the self-activated PL intensity arising from deep centers is weak. Because of these excellent properties of the layers, and since no further treatment is required after deposition, *n*-type ZnSe prepared by OM-CVD has advantages over *n*-type ZnSe prepared by other methods.

For the electrical measurements, *n*-type ZnSe layers with various doping levels of Al were deposited on semi-insulating Cr doped GaAs substrates having a resistivity of >10^7Ω·cm. A typical thickness of the ZnSe layers was 5 μm; the GaAs wafers were 0.5-mm thick. This sets an upper limit for the resistivity of the ZnSe that can be measured without shunting by the substrate of ~10^5Ω·cm. The electrical conductivity and the Hall constant were measured between liquid-helium temperature and room temperature in a van der Pauw configuration. Ohmic contacts to the ZnSe layers were made by depositing drops of a Hg-In alloy followed by an annealing step in forming gas at 280 °C. The contacts remained ohmic to liquid-helium temperatures .

The results of the electrical transport measurements as a function of temperature are shown in Fig.3 for three different layers, with carrier concentrations at 77 K ranging from $4.5 \cdot 10^{15}$ cm^{-3} for sample No. 6 to $5 \cdot 10^{17}$ cm^{-3} for sample No. 10. The room-temperature values for the carrier concentration are in good agreement with the values derived from capacitance-voltage measurements.[6] The conductivity appears to be thermally activated with an activation energy of between 24 meV for sample No. 6 and 6 meV for sample No. 10. These values for the activation energy are taken from the steepest part of the σ vs 1/T curves. The corresponding activation energy for the electron concentration is less that the activation energy for the conductivity, since the carrier mobility is strongly temperature dependent [see Fig.3(c)]. Using nondegenerate statistics, we obtain an activation energy of ~9 meV for the electrons on sample No. 6. This value is considerably smaller than both the activation energy of 21 meV measured for melt-grown, *n*-type ZnSe and the activation energy of 26.3 meV for isolated Al donors derived from optical spectroscopy.[7] The layer No. 10 with the largest carrier concentration is degenerate.

3.3 The anisotropy in the electrical conductivity of *n*-type ZnSe

A novel and very interesting phenomenon has been observed in the conductivity of deliberately doped, *n*-type ZnSe: the conductivity of ZnSe layers grown on semiinsulating, Cr-doped GaAs substrates depends strongly on the substrate orientation [8]. The conductivity of *n*-ZnSe layers grown on Cr-doped, semiinsulating (100) GaAs was found to be more than one order of magnitude larger than that of *n*-ZnSe layers grown on (110) GaAs substrates. The dark conductivity of ZnSe on (111)B GaAs was consistently too low to give a reliable reading. The temperature dependence of the electron concentration and the electron mobility of two samples of *n*-type ZnSe deposited during the same deposition run on Cr-doped, semiinsulating GaAs substrates with (100) and (110) orientation, respectively, are shown in Fig. 4. Data reported in the literature on bulk ZnSe [9] and on unintentionally doped ZnSe layers grown by MBE [10] are also shown for comparision. It is evident that the electron concentration of the layers grown by OM-CVD is $\sim 2 \cdot 10^{16}$ cm^{-3} and does not significantly depend on the substrate orientation. The electron mobility, on the other hand, is reduced by more than two orders of magnitude in the (110)

ZnSe layer compared to the (100) orientation.

SIMS measurements have confirmed that the dopant concentration is independent of the substrate orientation, in agreement with the analysis of the electrical transport data. A similar dependence on substrate orientation has been observed in the PL spectra. (see Fig. 5) Whereas the layers deposited on (100) GaAs or (100) Ge substrates exhibit strong bandgap luminescence and very little intensity in the self-activated part of the spectrum, the situation is just the opposite for the (111) substrate orientation. This larger intensity in the self-activated luminescence is indicative of a larger concentration of deep trapping states, and we will show below that electronic levels associated with the defect structure observed in our high resolution TEM work are responsible for the observed anisotropic properties.

We like to mention that the electron mobility in the (100) layers is not quite reproducible from deposition run to deposition run (it ranges from ~300 $cm^2/(V \cdot sec)$ to ~1500 $cm^2/(V \cdot sec)$ at room temperature) and seems to be associated with the defect structure which will be discussed below. We have also observed that the C-V and I-V characteristics of ZnSe-GaAs and ZnSe-Ge heterojunction devices depend on the substrate orientation. Their properties will be discussed in Section 3.6.

3.4 The lattice structure at ZnSe-GaAs interfaces

The defect structure of ZnSe epitaxial layers grown by OM-CVD and of their interface with the GaAs and Ge substrates has been studied using high resolution transmission electron microscopy [11,12]. This work was done in collaboration with Dr. F. A. Ponce, Hewlett-Packard Laboratories, Palo Alto, CA. Distinct differences in the defect structure were observed depending on substrate orientation and on the kind of substrate used.

3.4.1 The structure of ZnSe(100)/GaAs(100)

Fig. 6 shows a low magnification bright field micrograph of a ZnSe layer grown on GaAs(100). The observed large density of faults is typical of the ZnSe layers grown on (100) substrates that we have studied. More details of the structural characteristics are observed in Fig. 7, which is a multibeam lattice

image of the region about the ZnSe-GaAs interface. The lattice is viewed on a [110] projection. Two of the four sets of {111} lattice planes appear edge on, while the other two sets are oblique to the plane of the figure. These images were obtained under axial illumination, with an instrumental resolution of about 2.5 Å.

The faults in the bulk of the ZnSe layer consist to a large extent of interstitial Frank loops, with diameters between 30 and 120 Å. These loops lie in {111} planes and have a density of about 5 X 10^{17} cm^{-3}, which varies little with position away from the substrate interface. These loops involve an extra {111} plane and are associated with an extrinsic stacking fault. Only half of the loops are visible edge on; these are the loops which lie on the two sets of {111} planes normal to the image plane. The other half of the loops are oblique to the image plane and give rise to circular regions of moiré fringes.

The ZnSe-GaAs interface itself is seen delineated throughout the material. In some regions we observed some amorphous inclusions of about 20 Å in length. We feel that this delineation has two possible causes: (a) absorbed surface impurities (*e.g.*, carbon, oxygen, OH^-, chlorine) which are remnants of the original surface preparation and (b) intermixing of ZnSe and GaAs which are completely miscible. The lattice is very coherent, which means that there is continuity of lattice planes across the interface. Very few misfit dislocations have been directly imaged at the interface, and the large majority of faults at the interface is due to intercepting faulted loops. The measured density of these faulted loops at the interface is an order of magnitude higher than the expected density of misfit dislocations due to lattice mismatch.

3.4.2 The structure of ZnSe(111)/GaAs(111)B

The structure of ZnSe layers grown on GaAs(111)B sustrates is quite different from that of layers grown on (100) substrates. The predominant characteristic of growth in the [111] direction is the existence of high densities of twins and stacking faults. Fig. 8 shows a lattice image of the ZnSe-GaAs interface; the interface is planar and along the [111] direction. The absence of faulted loops is striking. The right-hand side of the figure is twinned with respect to the substrate whereas the left-hand side is not. The boundary where these two

regions meet is severely distorted. Fig. 9 shows the defect structure in the bulk of the film, about 1 μm away from the interface; micrographs such as Fig. 9 strongly suggest lateral step layer growth. The formation of large vertical faulted boundaries as observed in the middle of this figure could be due to an offset or step in the growth.

3.4.2 The structure of ZnSe(110)/GaAs(110)

The best interface with the lowest concentration of defects was observed for the (110) orientation; a defect-free section of such an interface is shown in Fig.10. Occasionally we have observed twinning at the interface, with the boundary of the twinned section originating at a defect directly at the substrate interface. Fig.11 shows the defect structure in the bulk of the layer, about 1 μm from the interface. It is striking that *all* stacking faults are planar in the [111]B direction only; *no* faults are observed in the [111]A direction. This observation supports the fact that the [111]B planes are the natural growth planes for crystals with the zincblende and wurtzite structure.

3.5 The lattice structure at ZnSe-Ge interfaces

3.5.1 The structure of ZnSe(100)/Ge(100)

The structural characteristic of a region about the ZnSe(100)/Ge(100) interface as observed in a multibeam lattice image is shown in Fig.12. The lattice is viewed on a [110] projection; two of the four sets of {111} lattice planes appear edge on, while the other two are oblique to the plane of the figure. Some of the observed faults are similar in nature to those observed on (100)ZnSe – (100)GaAs interfaces. They consist of interstitial Frank loops (indicated by a in Fig.12), with diameters between 30 A and 200 A. These loops involve an extra {111} plane and are associated with an extrinsic stacking fault. In addition we have also observed large intrinsic stacking faults (indicated by b) originating at the interface and probably caused by slip. The latter could be caused by lateral stresses that appear after the growth, possibly due to a) the presence of native oxides and other impurities at the interface of the Ge substrate, and b) the larger difference in thermal expansion coefficient between ZnSe ($7.0 \cdot 10^{-6}$/°C) and Ge ($5.9 \cdot 10^{-6}$/°C) compared with ZnSe and GaAs ($6.8 \cdot 10^{-6}$/ C).

The ZnSe - Ge interface itself appears delineated throughout the material. This delineation could be caused by native oxides and/or impurities absorbed at the substrate surface before the growth or by intermixing of Ge and ZnSe. The lattice is very coherent, i.e., the lattice planes are continuous across most of the interface, and the ZnSe layers grow truly epitaxial. The density of misfit dislocations is expected to be low because of the good lattice match between Ge and ZnSe.

3.5.2 The structure of ZnSe(111)/Ge(111)

Fig. 13 shows the defect structure at the ZnSe(111)/Ge(111) interface. In contrast to the structure observed on (100) substrates, the predominant characteristic of growth in the (111) direction is the existence of intrinsic stacking faults (indicated by a in Fig. 13) and microtwins across a large portion of the interface. Away from the interface, the defect density of the ZnSe layer is relatively low when compared to the defect density observed in layers grown on [111]B GaAs. This characteristic is due to the slight misorientation of the Ge substrate (~3° off the {111} crystalline planes). This misorientation leads to an increased number of nucleation sites for lateral growth of the ZnSe layer. In the absence of these nucleation sites, the growth of large microtwins and stacking faults, as observed in the [111]B GaAs case (see Fig. 9), would be expected. The ZnSe(111)/Ge(111) interface shown in Fig. 13 is not planar. In some regions it follows the (111) Ge planes, whereas in other planes it is inclined. The microtwins and stacking faults are associated with the interface regions parallel to the [111] Ge, whereas the inclined regions do not exhibit any faults at the interface. This observation leads to the conclusion that the quality of the epilayer for growth on (111) substrates is improved by a slight misorientation of the substrates of ~3° which causes overgrowth of the stacking faults. We can expect that the defect structure of ZnSe layers grown on perfectly oriented (111) Ge substrates is identical to the one observed on ZnSe layers grown on (111)B GaAs substrates.

3.6 Properties of ZnSe-GaAs and ZnSe-Ge heterojunction devices

As part of the characterization of ZnSe layers on Ge substrates we have employed essentially three different junction structures on (100) and (111)

oriented Ge substrates. The three types of junctions yield information about the ZnSe bulk properties, the doping of the ZnSe, and the interface between ZnSe and the Ge substrates.

1) Au/*i*-ZnSe/*n*-Ge and Au/*i*-ZnSe/*p*-Ge MIS junctions
2) Au/*n*-ZnSe/*n*-Ge Schottky barriers
3) *n*-ZnSe/*p*-Ge and *n*-ZnSe/*n*-Ge heterojunctions

(1) *The metal/insulator/semiconductor (MIS) junctions* serve as a tool to investigate the nature of ZnSe acting as a dielectric. Diodes have been prepared both on n-type and on p-type Ge using thick layers (> 3 μm) of ZnSe. Capacitance-voltage measurements have confirmed the dielectric nature of the ZnSe.

By using thin layers of ZnSe (d < 0.1 μm) on low-doped Ge and GaAs substrates, the dielectric nature of ZnSe and the properties of the ZnSe/Ge and ZnSe/GaAs interfaces can be investigated. The difference in defect structure depending on the substrate orientation was found to have a significant influence on the C-V characteristics.

Ideally, the MIS structure has a total capacitance, C, given by [13]

$$C = C_i C_D/(C_i + C_D)$$

where C_i is the insulator capacitance and C_D is the semiconductor depletion-layer capacitance which is voltage dependent. The total capacitance C is illustrated in Fig. 14 for an ideal MIS diode. In accumulation (forward bias) the total capacitance approaches C_i, which is given by $C_i \simeq \varepsilon_i/d$ with ε_i being the permittivity of the insulator and d its thickness. In inversion (reverse bias) the total capacitance approaches C_{min}, which is given by $C_{min} \simeq \varepsilon_i/(d + W)$ with W being the width of the semiconductor depletion layer. Only when d and W are of the same magnitude will there be any noticeable effect on the total capacitance C as the voltage is altered. W is determined by the doping of the semiconductor and for values of W of about 0.1 μm the doping should not exceed 10^{16} cm^{-3}. Consequently, the film thickness d should also be of the order of 0.1 μm. This ideal theory neglects the presence of any interface states. If such interfacial trap states do exist, there will be a shift in the turn-on

voltage V_T in the MIS capacitance curve by $V_T = Q_F/C_i$, where Q_F is the interface state density. By measuring V_T it is therefore possible to estimate of the total trapped interface charge. We have prepared undoped ZnSe layers ranging in thickness from less than 1000 Å to ~5000 Å and measured the C-V curve at a frequency of 1 MHz. Although we were not able to drive the device into accumulation due to excess leakage current, we estimated V_T to be in the order of 0.1 to 0.2 V corresponding to an interface state density of $\sim 10^{11}$ cm^{-2}. This density of interface states is low enough to make ZnSe potentially useful for the passivation of GaAs and Ge based FET's.

(2) *Au/n-ZnSe/n-Ge Schottky barriers* have been prepared using Al-doped, n-type ZnSe and have yielded information about the dopant concentration in the ZnSe. The n-type Ge substrate serves in this case mainly as a contact to the n-ZnSe film; the barrier has been verified to occur at the Au/n-ZnSe interface. The dopant concentration determined from these C – V and I – V measurements agrees with Van der Pauw studies of the electrical resistivity of n – type ZnSe deposited on semiinsulating GaAs substrates.[6] Appreciable differences in the behavior of diodes formed on (100) and (111) oriented substrates were again observed and can be linked to the anisotropy in the electrical resistivity discussed above.

(3) *N-ZnSe/p-Ge and n-ZnSe/n-Ge heterojunctions* have been prepared. The substrate orientation has been found to play a major role in the properties of the heterojunctions, most likely reflecting the observed differences in the defect structure at the interface and in the bulk of the ZnSe layer away from the interface. The thickness of the ZnSe layers used in the current – voltage measurements was 4.3 μm for the (100) orientation and 3.5 μm for the (111) orientation.

For *n*-ZnSe – *p*-Ge heterojunctions formed on the (100) Ge substrates, the current – voltage characteristic is found to follow the Shockley expression for a simple diode model:

$$J = J_0 [\exp(qV/(A \cdot k_B T)) - 1] \qquad (1)$$

where J_0 is the dark saturation current, q the electron charge, V the applied voltage, A the diode factor, and T the temperature in degrees Kelvin (see

Fig.15). For a typical *n*-ZnSe – *p*-Ge heterojunction formed on a (100) Ge substrate, A is 1.1 - 1.2 and remains constant over a temperature range from 250 K to 350 K. J_0 is $1 \cdot 10^{-11}$ A/cm^2 at 300 K and is thermally activated with an activation energy of 0.75 eV, which is considerably larger than expected from a simple energy band diagram based on the Anderson model shown in Fig. 12. However, if the current is limited by diffusion of minority carriers injected into the *p*-Ge from the *n*-ZnSe, then J_0 is given by

$$J_0 = qD_n n_i^2/(L_n N_A) \qquad (2)$$

where D_n is the diffusion constant, L_n is the minority carrier diffusion length, n_i is the intrinsic carrier concentration, and N_A is the acceptor concentration. The temperature dependence of J_0 in equation (2) is dominated by the temperature dependence of n_i^2, which is proportional to E_G/k_BT. A plot of J_0 vs 1/T should therefore have a slope of $E_{G(Ge)}$ (0.7 eV). The observed temperature dependence agrees reasonably well with the diffusion mechanism, but our observed J_0 values are lower than expected. However, the passage of current at the ZnSe/Ge interface may be limited by a minority carrier build up at the edges of the depletion region due to a discontinuity in the conduction bands (see Fig.16).

Heterojunctions formed on the (111) Ge substrates, on the other hand, exhibit a non-ideal diode behavior with diode factors larger than 3 and a dark saturation current of $4 \cdot 10^{-8}$ A/cm^2 (see Fig. 15). Temperature-dependent measurements have not been successful, mostly due to the high resistivity of the (111)ZnSe layer. However, the large diode factors observed indicate a current transport mechanism dominated by a recombination process through interface states, which are most likely a result of the structural defects observed at the (111)ZnSe/Ge interface. Since the ZnSe is relatively resistive ($> 10^2$ Ω·cm), the diode current at higher voltages may be limited by space charge processes in the ZnSe.

4.0 Work sponsored by this contract

4.1 Manpower

Dr. Wolfgang Stutius, principal investigator, was supported in part by the contract. The salary of Dr. Jan G. Werthen was paid entirely by the contract.

4.2 Talks

1.) "Lattice structure at ZnSe-GaAs heterojunction interfaces prepared by organometallic CVD." F. A. Ponce, Hewlett-Packard Laboratories, Palo Alto, CA 94304, and W. Stutius and J. G. Werthen, Xerox Palo Alto Research Centers, Palo Alto, CA 94304.
Paper presented at Symposium C of the Materials Research Society, Boston, MA., Nov.1-4, 1982.

2.) "Interface properties of *n*-ZnSe – *p*-Ge heterojunctions grown by organometallic chemical vapor deposition" by J. G. Werthen and W. Stutius, Xerox Palo Alto Research Center, Palo Alto, CA 94304, and F. A. Ponce, Hewlett-Packard Laboratories, Palo Alto, CA 94304.
Paper presented at the 10th Annual Conference on the Physics and Chemistry of Compound Semiconductor Interfaces (PCSI), Santa Fe, NM, January 24-27, 1983.

3.) "Properties of ZnSe grown by organometallic CVD" by W. Stutius, Xerox Palo Alto Research Center, Palo Alto, CA 94304.
Seminar presented at the North American Philips Research Laboratory, Briarcliff Manor, NY, June 13, 1983.

4.) "Properties of ZnSe grown by organometallic CVD" by W. Stutius, Xerox Palo Alto Research Center, Palo Alto, CA 94304.
Seminar presented at the GTE Laboratory, Waltham, MA, June 16, 1983.

5.) "Anisotropy of the electrical conductivity in epitaxial *n*-type ZnSe prepared by organometallic CVD" by W. Stutius and J.G. Werthen, Xerox Palo Alto Research Center, Palo Alto, CA 94304, and F. A. Ponce, Hewlett-Packard Laboratories, Palo Alto, CA 94304.

Paper presented at the 23rd Annual Electronic Materials Conference, Burlington, VT, June 22-24, 1983.

4.3 Publications

1.) "Lattice structure at ZnSe-GaAs heterojunction interfaces prepared by organometallic chemical vapor deposition." F. A. Ponce, Hewlett-Packard Laboratories, Palo Alto, CA 94304, and W. Stutius and J. G. Werthen, Xerox Palo Alto Research Centers, Palo Alto, CA 94304.
Thin Solid Films, **104** (1983), pp.133-143.

2.) "Interface properties of *n*-ZnSe – *p*-Ge heterojunctions grown by organometallic chemical vapor deposition" by J. G. Werthen and W. Stutius, Xerox Palo Alto Research Center, Palo Alto, CA 94304, and F. A. Ponce, Hewlett-Packard Laboratories, Palo Alto, CA 94304.
J.Vac.Sci.Technology, **B 1** (1983), pp.656-660.

3.) "Anisotropy of the electrical conductivity in epitaxial *n*-type ZnSe prepared by organometallic CVD" by W. Stutius and J.G. Werthen, Xerox Palo Alto Research Center, Palo Alto, CA 94304, and F. A. Ponce, Hewlett-Packard Laboratories, Palo Alto, CA 94304.
Paper to be published in the Journal of Electronic Materials (1984).

4.4 Inventions

Xerox invention proposal entitled: " GaAs FET's with ZnSe or ZnS_xSe_{1-x} dielectric insulator" by W. Stutius and J.G. Werthen.

5.0 References

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6.0 Figure captions

Fig.1 Schematic of the OM-CVD reactor

Fig.2 Dependence of the photoluminescence on the substrate cleaning procedure for GaAs (100) substrates: (a) organic cleaning only; (b) cleaned in organic solvents followed by acid cleaning; and (c) same as (b), but with careful control of GaAs surface (hydrophobic) and low oxygen and water partial pressure in the reactor.

Fig.3 Electrical properties of aluminum doped, n-type ZnSe on GaAs(100) substrates: (a) electrical conductivity; (b) electron concentration; and (c) electron mobility.

Fig.4 Electron concentration and mobility for ZnSe(100)/GaAs(100) (full circles) and ZnSe(110)/GaAs(110) (open circles) showing the anisotropy of the electron mobility caused by the defect structure. For comparision, results obtained on bulk crystals and on a layer grown by MBE are also shown.

Fig.5 PL spectra of (a) undoped ZnSe on GaAs(100) and (b) undoped ZnSe on GaAs(111)B (t = 77K). The strong luminescence peak at 4454 Å in (a) corresponds to the I_2 bound exciton line.

Fig.6 Bright field transmission electron micrograph of a ZnSe(100) layer taken in cross section. The highly faulted nature of the ZnSe layer, when compared with the GaAs substrate, should be noted.

Fig.7 Lattice image of ZnSe(100)/GaAs(100). The interface is coherent and appears delineated. Dislocations do not propagate into the GaAs substrate.

Fig.8 Lattice image of ZnSe(111)/GaAs(111)B. The interface is abrupt and coherent. The presence of twinned regions is indicated.

Fig.9 Structure of the bulk of the epitaxial layer grown on GaAs(111)B.

Fig.10 Lattice image of ZnSe(110)/GaAs(110). The interface is perfect without any faults.

Fig.11 Structure of the bulk of the epitaxial layer grown on GaAs(110). Note that all the stacking faults are parallel to the {111}B planes and that no faults are observed in the {111}A planes.

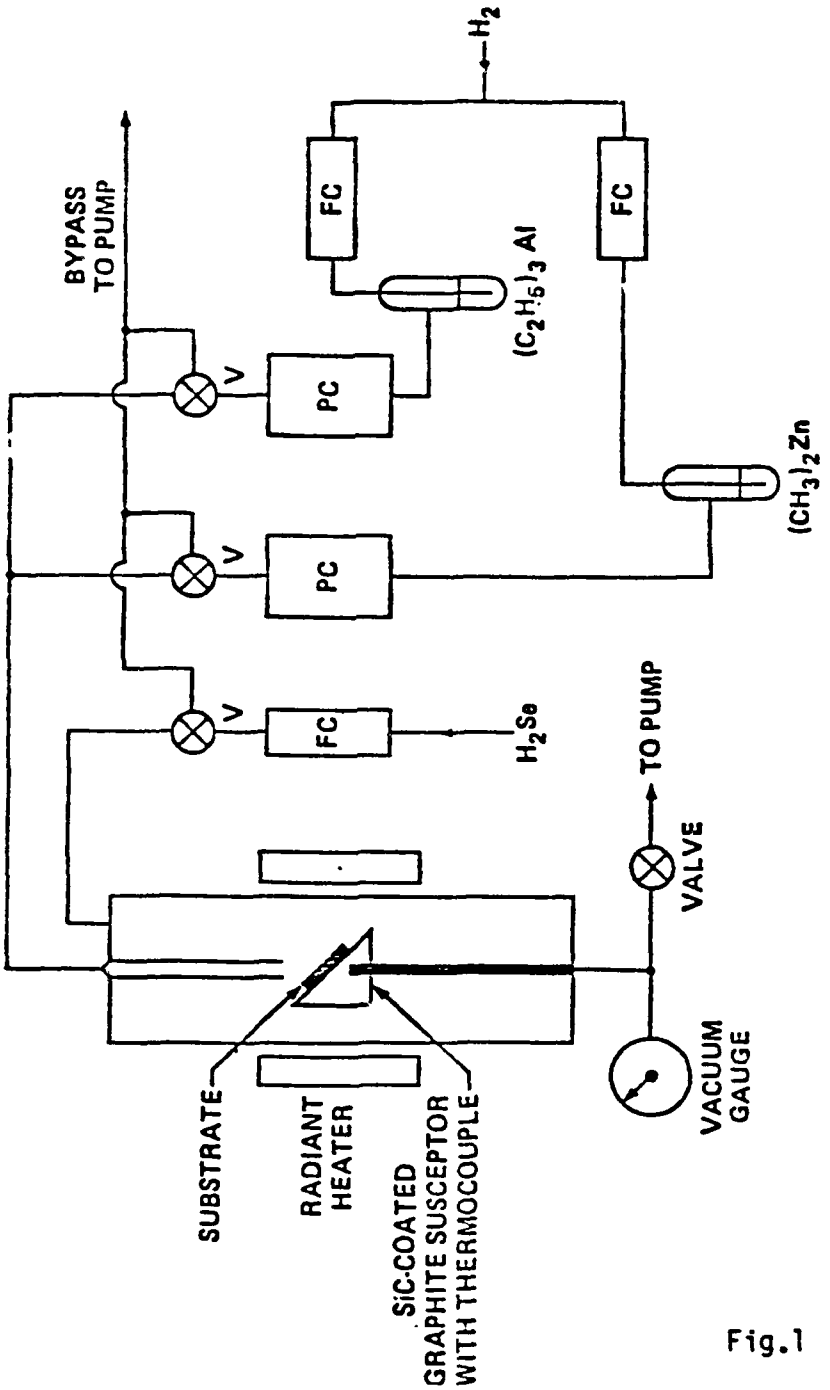
Fig.12 Lattice image of ZnSe(100)/Ge(100). The interface is coherent and appears delineated. Interstitial dislocation (Frank) loops (a) and intrinsic stacking faults (b) are present in the ZnSe layer.

Fig.13 Lattice image of ZnSe(111)/Ge(111). Intrinsic stacking faults (a) cover a large part of the interface.

Fig.14 Capacitance vs voltage for an ideal MIS diode (from Ref.13).

Fig.15 Current – voltage characteristics of (100) and (111) *n*-ZnSe – *p*-Ge heterojunctions. The thickness of the ZnSe layer was 4.3 μm for the (100) orientation and 3.5 μm for the (111) orientation, respectively.

Fig.16 Energy band diagram for the *n*-ZnSe – *p*-Ge heterojunction based on the Anderson model. ΔE_C = 0.04 eV and ΔE_V = 1.9 eV.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FC
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V
PC
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V
PC
V
FC
H_2Se
TO PUMP
VALVE
SUBSTRATE
RADIANT HEATER
SiC-COATED GRAPHITE SUSCEPTOR WITH THERMOCOUPLE
VACUUM GAUGE

Fig.1

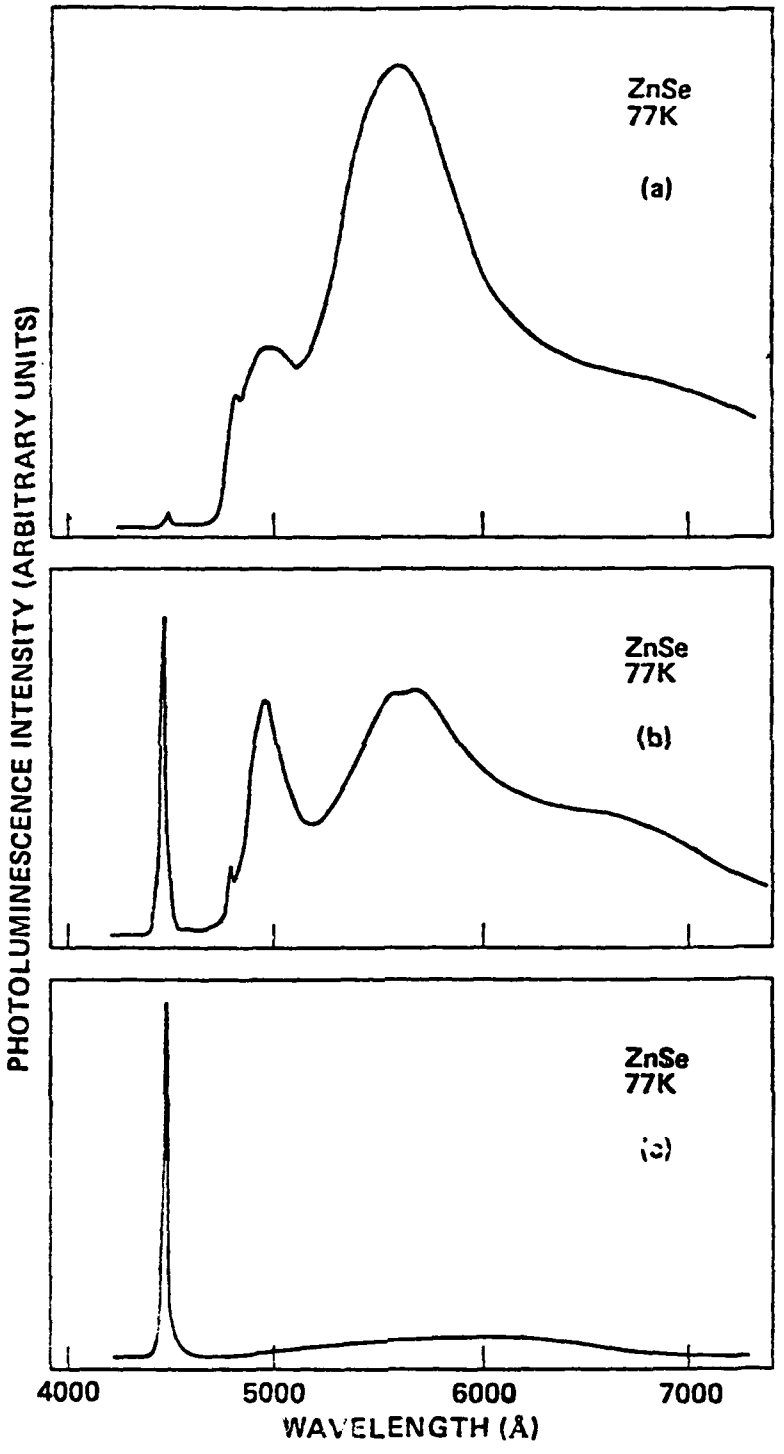

ZnSe
77K
(a)
ZnSe
77K
(b)
ZnSe
77K
(c)
PHOTOLUMINESCENCE INTENSITY (ARBITRARY UNITS)
4000
5000
6000
7000
WAVELENGTH (Å)

Fig.2

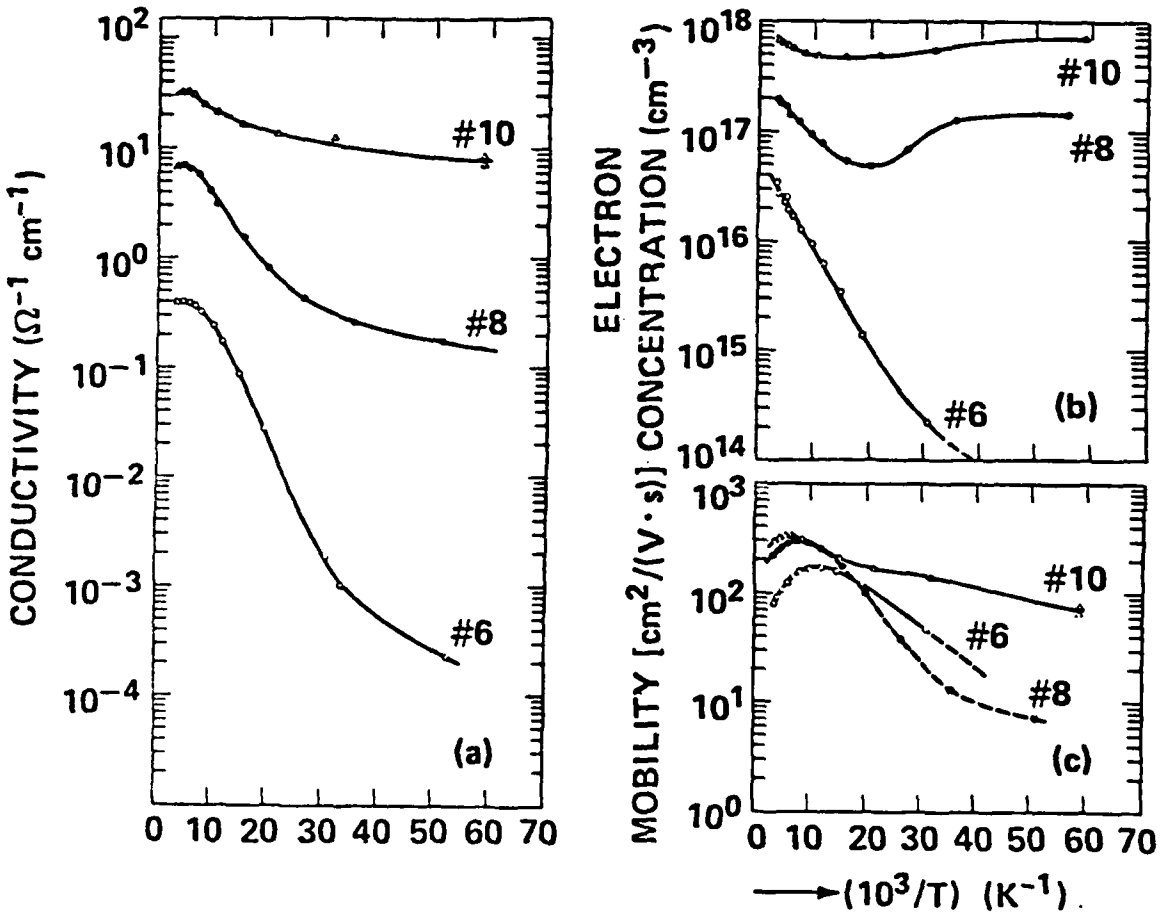
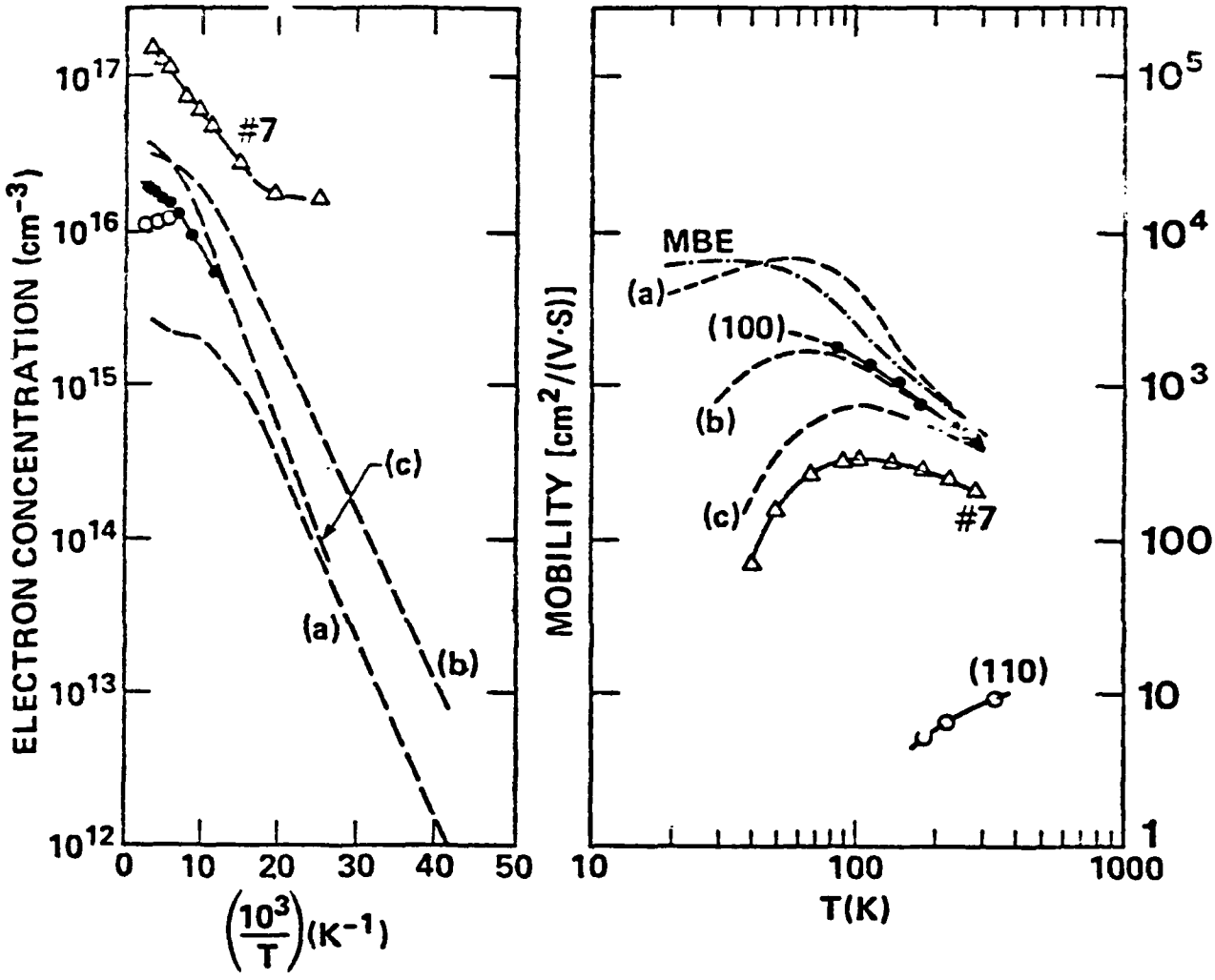

CONDUCTIVITY (Ω^{-1} cm^{-1})
10^2
10^1
10^0
10^{-1}
10^{-2}
10^{-3}
10^{-4}
#10
#8
#6
(a)
0 10 20 30 40 50 60 70
ELECTRON MOBILITY [cm^2/(V·s)] CONCENTRATION (cm^{-3})
10^{18}
10^{17}
10^{16}
10^{15}
10^{14}
#10
#8
#6
(b)
10^3
10^2
10^1
10^0
#10
#6
#8
(c)
0 10 20 30 40 50 60 70
→(10^3/T) (K^{-1})

Fig.3



n – ZnSe ON (100) GaAs (#7, heavily doped)
n – ZnSe ON (100) GaAs
n – ZnSe ON (110) GaAs
} BY OM-CVD

ZnSe ON (100) GaAs BY MBE (T. YAO ET.AL.)

n – ZnSe CRYSTALS (AVEN AND KENNICOTT, 1964)
(a) $N_D = 0.34$; $N_A = 0.13$
(b) $N_D = 3.5$, $N_A = 0.5$ [$\times 10^{16}$ cm^{-3}]
(c) $N_D = 7.4$, $N_A = 3.4$

Fig.4

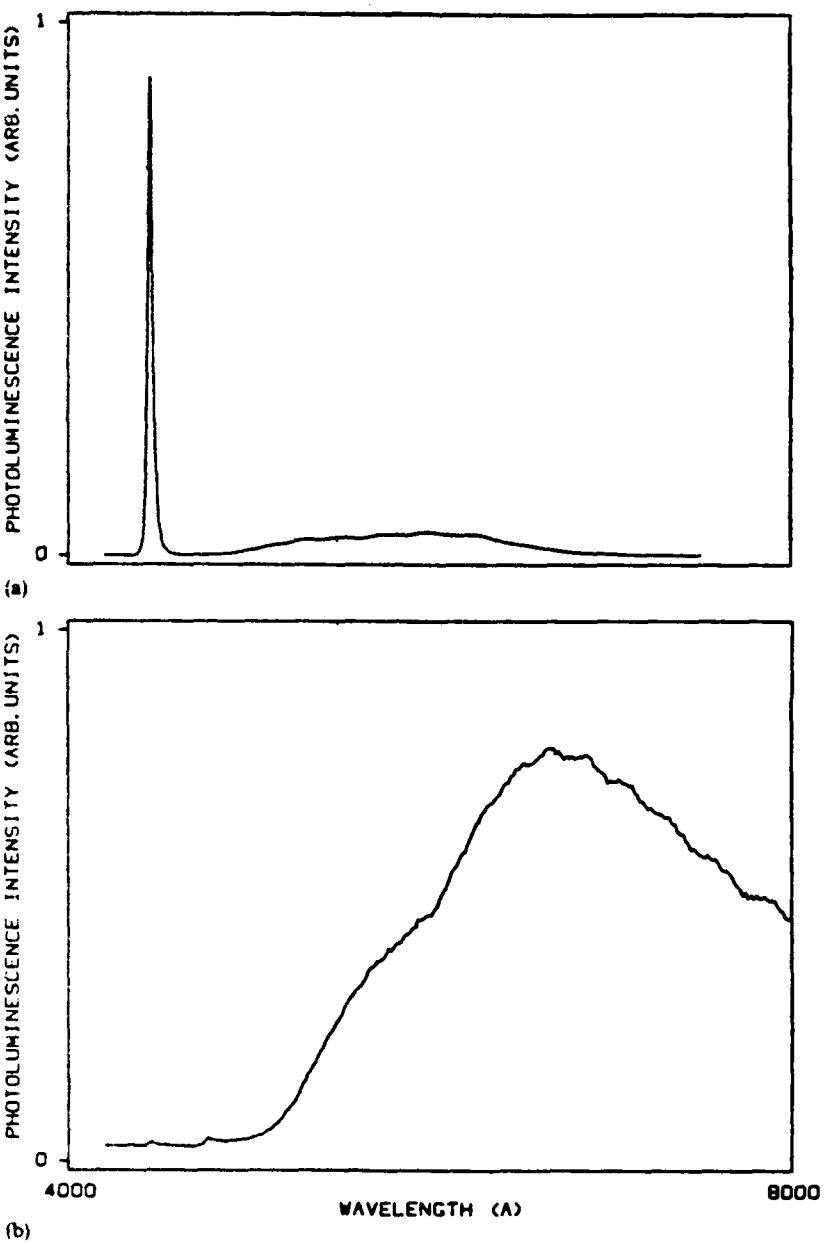


Fig.5 PL spectra of (a) ZnSe on GaAs(100) and (b) ZnSe on GaAs(111)B (T = 77 K). The strong luminescence peak at 4454 Å in (a) corresponds to the I_2 bound exciton line.

Fig.5

Fig.6

Fig. Lattice image of ZnSe(100) GaAs(100). The interface is coherent and appears delineated. Dislocations do not propagate into the GaAs substrate

Fig.7

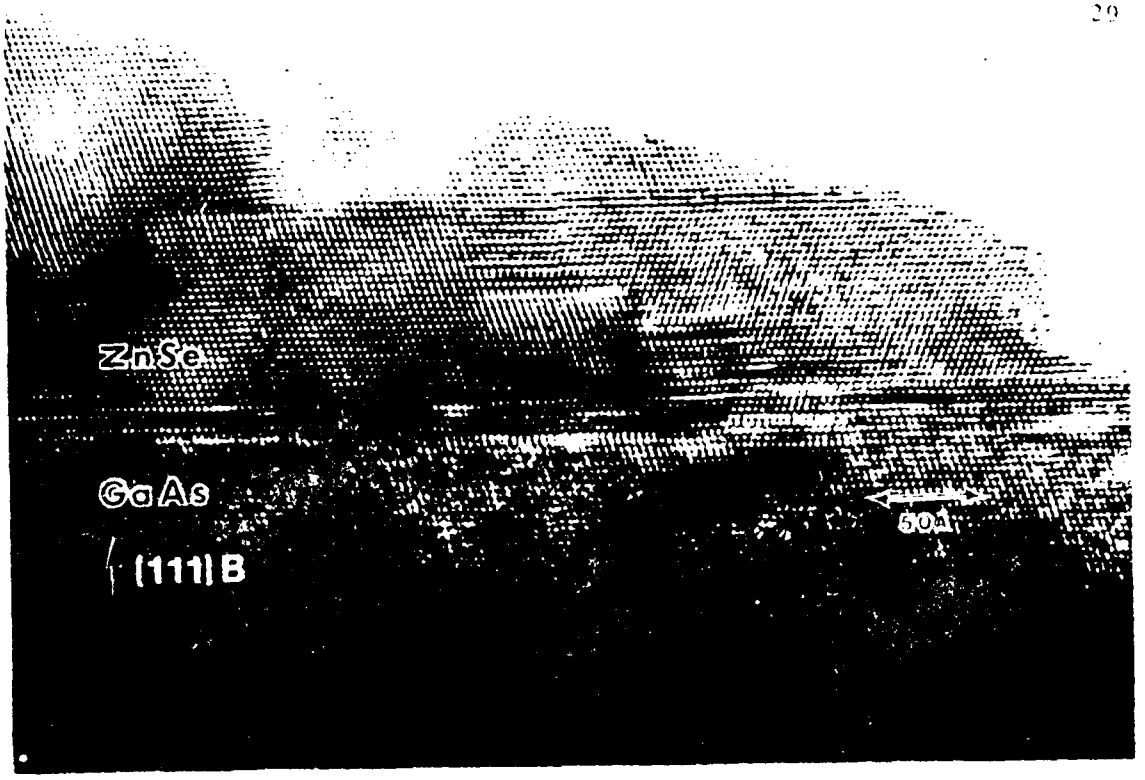


Fig. 1. Lattice image of ZnSe[111]/GaAs[111]B. The interface is abrupt and coherent. The presence of twinned regions is indicated to suppress the lattice mismatch.

Fig. 2. Structure of the bulk of the ZnSe epitaxial layer grown on GaAs[111]B.

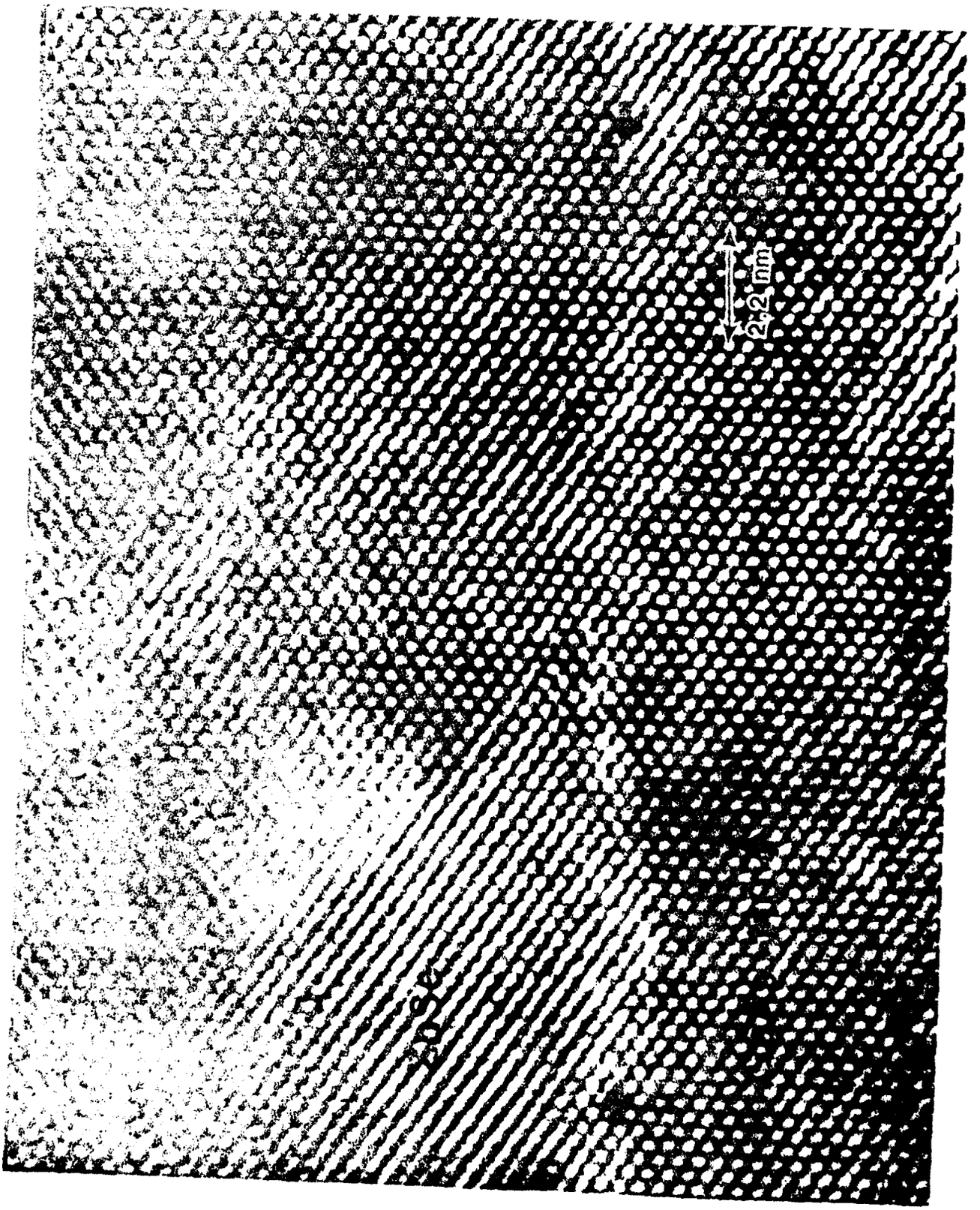
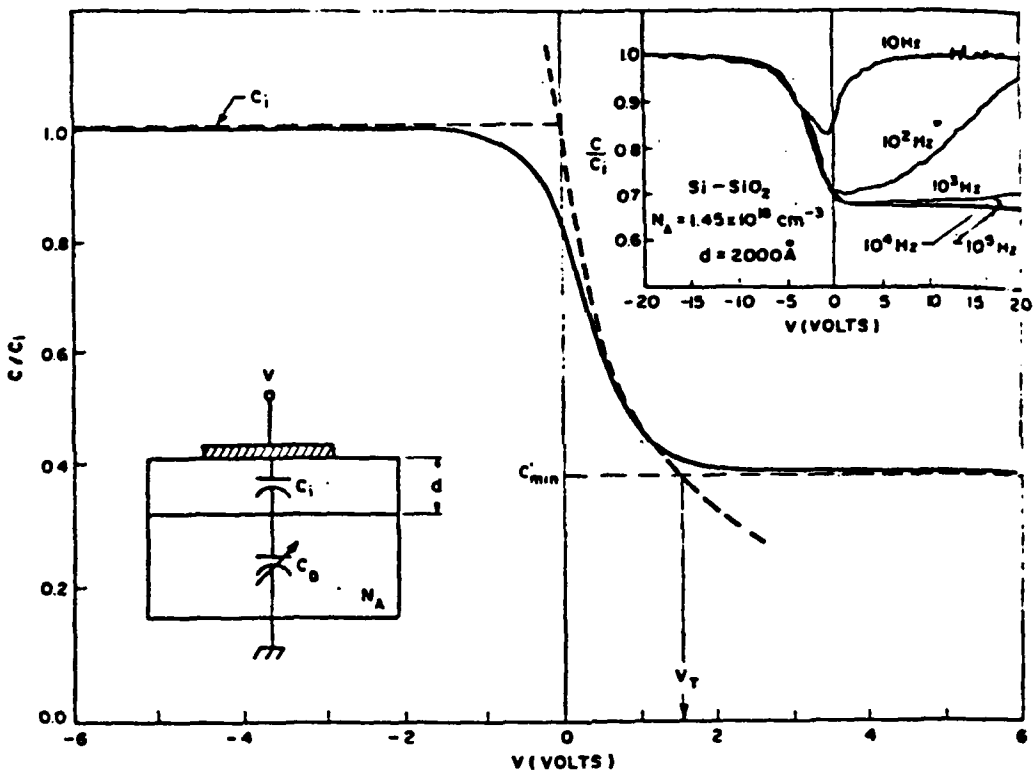


Fig.10

Fig.11

Fig.12

Fig.13



High-frequency MIS capacitance-voltage curve showing its approximated segments (dotted lines). The inset shows the frequency effect.

Fig.14

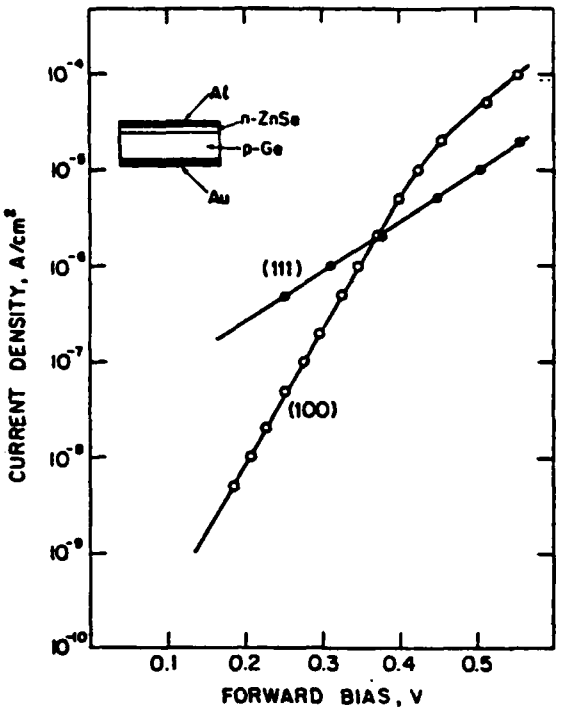


FIG. Current–voltage characteristics of (100) and (111) *n*-ZnSe–*p*-Ge heterojunctions. The thickness of the ZnSe layer was 4.3 μm for the (100) orientation and 3.5 μm for the (111) orientation, respectively.

Fig.15

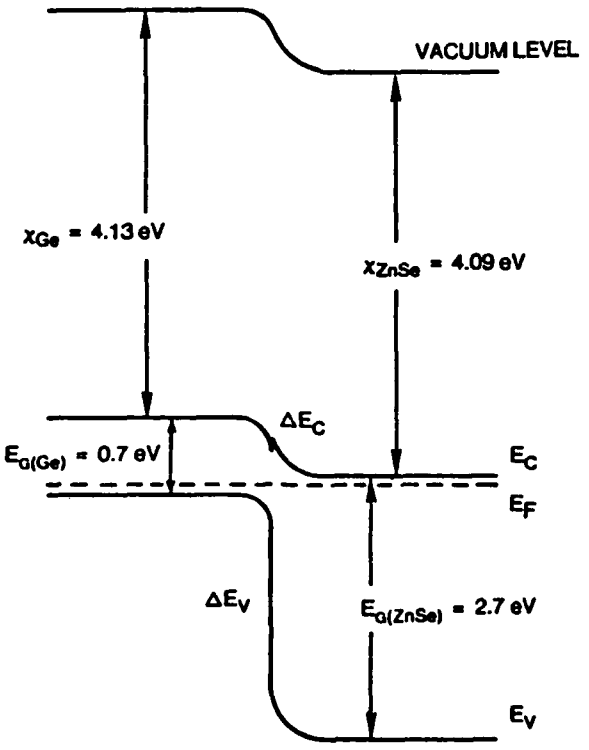


FIG. Energy band diagram for the *n*-ZnSe–*p*-Ge heterojunction based on the Anderson model (Ref. 9). $\Delta E_C = 0.04$ eV and $\Delta E_V = 1.9$ eV.

Fig.16

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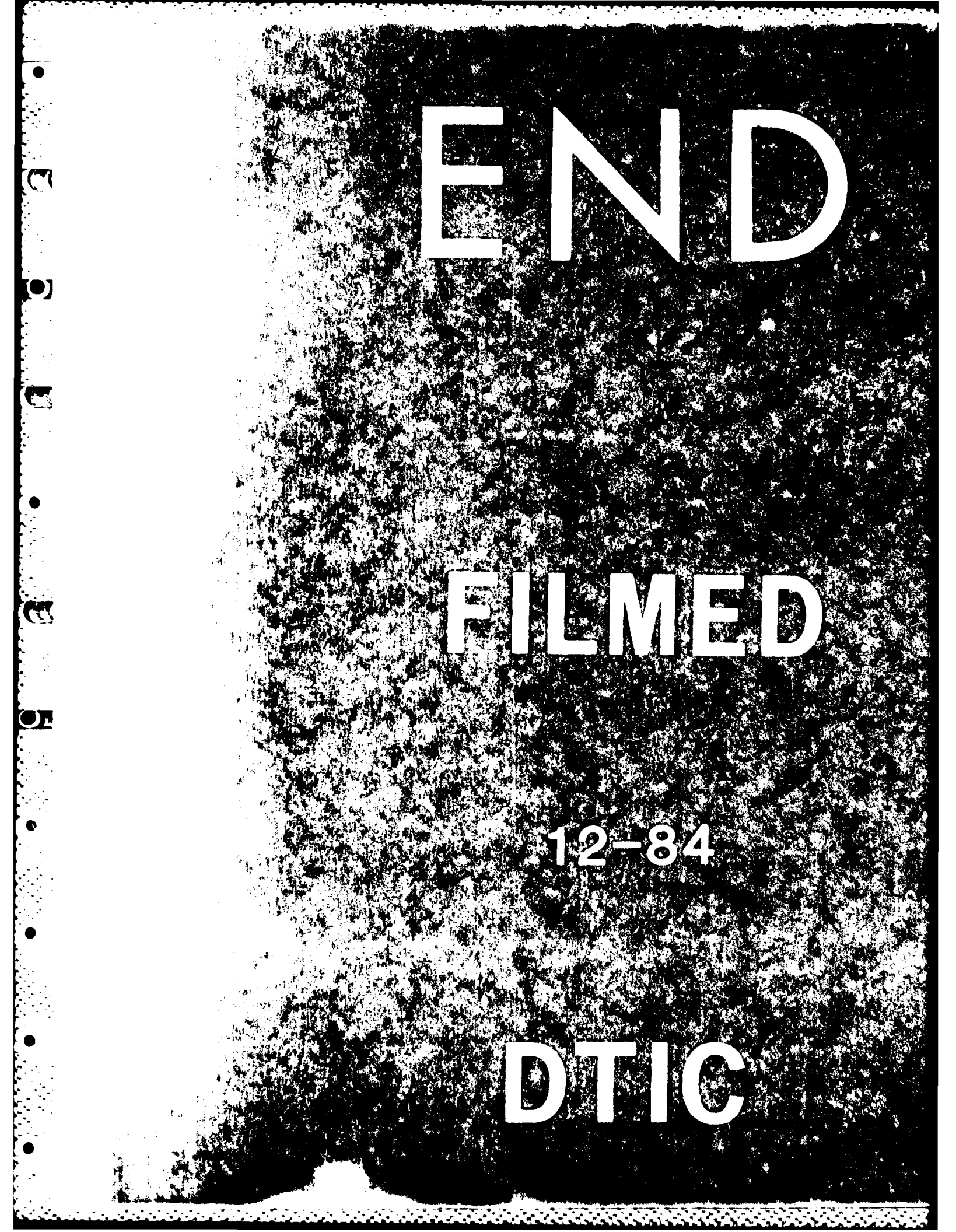
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