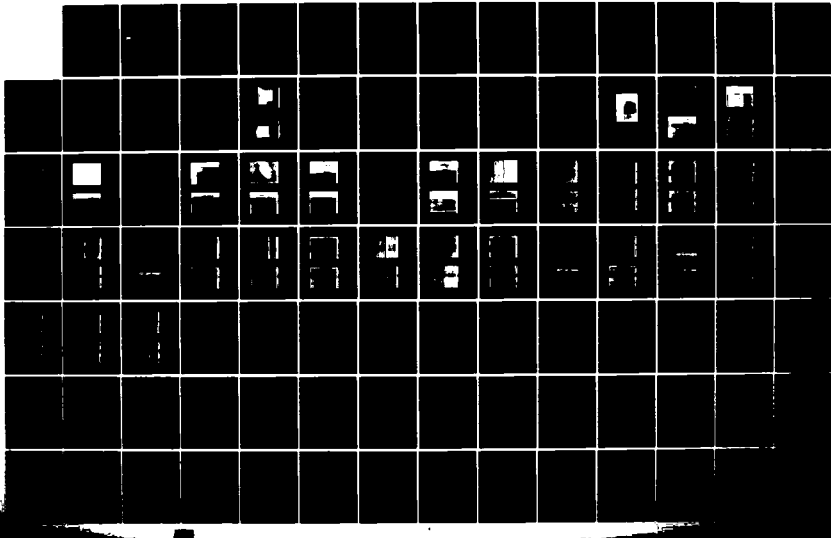
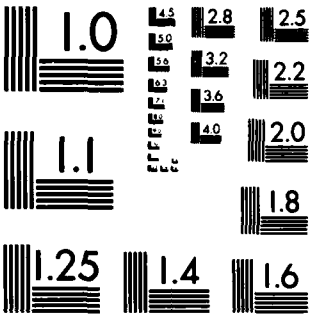
AD-A150 356 SEM (SCANNING ELECTRON MICROSCOPE) INVESTIGATION OF SILICON DIODES USING T..(U) AIR FORCE WEAPONS LAB KIRTLAND AFB NM M E SNYDER DEC 84 AFWL-TR-84-13 1/1

UNCLASSIFIED F/G 9/1 NL





AFWL-TR-
84-13

(2)

SEM INVESTIGATION OF SILICON DIODES USING THE ELECTRON BEAM INDUCED CURRENT METHOD

1Lt Mark E. Snyder

December 1984

Final Report

Approved for public release; distribution unlimited.

AIR FORCE WEAPONS LABORATORY
Air Force Systems Command
Kirtland Air Force Base, NM 87117

This final report was prepared by the Air Force Weapons Laboratory, Kirtland Air Force Base, New Mexico, under Job Order ILIR8219. First Lieutenant Mark E. Snyder (NTAT) was the Laboratory Project Officer-in-Charge.

When Government drawings, specifications, or other data are used for any purpose other than in connection with a definitely Government-related procurement, the United States Government incurs no responsibility or any obligation whatsoever. The fact that the Government may have formulated or in any way supplied the said drawings, specifications, or other data, is not to be regarded by implication, or otherwise in any manner construed, as licensing the holder, or any other person or corporation; or as conveying any rights or permission to manufacture, use, or sell any patented invention that may in any way be related thereto.

This report has been authored by an employee of the United States Government. Accordingly, the United States Government retains a nonexclusive, royalty-free license to publish or reproduce the material contained herein, or allow others to do so, for the United States Government purposes.

This report has been reviewed by the Public Affairs Office and is releasable to the National Technical Information Services (NTIS). At NTIS, it will be available to the general public, including foreign nations.

If your address has changed, if you wish to be removed from our mailing list, or if your organization no longer employs the addressee, please notify AFWL/NTAT, Kirtland AFB, NM 87117-6008 to help us maintain a current mailing list.

This report has been reviewed and is approved for publication.

Mark E. Snyder

MARK E. SNYDER
First Lieutenant, USAF
Project Officer

FOR THE COMMANDER

Roger S. Case

ROGER S. CASE, JR
Lt Colonel, USAF
Chief, Aircraft & Missile Division

James A. Kee

JAMES A. KEE
Major, USAF
Chief, Technology Branch

DO NOT RETURN COPIES OF THIS REPORT UNLESS CONTRACTUAL OBLIGATIONS OR NOTICE ON A SPECIFIC DOCUMENT REQUIRES THAT IT BE RETURNED.

UNCLASSIFIED

SECURITY CLASSIFICATION OF THIS PAGE

AD-A150356

REPORT DOCUMENTATION PAGE

1a. REPORT SECURITY CLASSIFICATION: Unclassified	1b. RESTRICTIVE MARKINGS
2a. SECURITY CLASSIFICATION AUTHORITY	3. DISTRIBUTION/AVAILABILITY OF REPORT: Approved for public release; distribution unlimited.
2b. DECLASSIFICATION/DOWNGRADING SCHEDULE	
4. PERFORMING ORGANIZATION REPORT NUMBER(S): AFWL-TR-84-13	5. MONITORING ORGANIZATION REPORT NUMBER(S)
6a. NAME OF PERFORMING ORGANIZATION: Air Force Weapons Laboratory; 6b. OFFICE SYMBOL (If applicable): NTAT	7a. NAME OF MONITORING ORGANIZATION
6c. ADDRESS (City, State and ZIP Code): Kirtland Air Force Base, NM 87117-6008	7b. ADDRESS (City, State and ZIP Code)
8a. NAME OF FUNDING/SPONSORING ORGANIZATION; 8b. OFFICE SYMBOL (If applicable)	9. PROCUREMENT INSTRUMENT IDENTIFICATION NUMBER
8c. ADDRESS (City, State and ZIP Code)	10. SOURCE OF FUNDING NOS.

PROGRAM ELEMENT NO.	PROJECT NO.	TASK NO.	WORK UNIT NO.
61101F	ILIR	82	19

11. TITLE (Include Security Classification): SEM INVESTIGATION OF SILICON DIODES USING THE ELECTRON BEAM INDUCED CURRENT METHOD

12. PERSONAL AUTHOR(S): Snyder, Mark E.

13a. TYPE OF REPORT	13b. TIME COVERED	14. DATE OF REPORT (Yr., Mo., Day)	15. PAGE COUNT
Final	FROM _____ TO _____	1984, December	100

16. SUPPLEMENTARY NOTATION

17. COSATI CODES			18. SUBJECT TERMS (Continue on reverse if necessary and identify by block number)
FIELD	GROUP	SUB. GR.	SEM, EBIC, Silicon Diodes, Device Failure
09	01		
20	06		

19. ABSTRACT (Continue on reverse if necessary and identify by block number)

This report details the development and utilization of the Scanning Electron Microscope in the electron beam induced current mode method at the Air Force Weapons Laboratory, Material Sciences Laboratory. This method in conjunction with secondary electron imaging, is used to perform a nondestructive testing of a set of specially designed diodes to demonstrate this method's general ability to determine failure modes of semiconductor devices.

20. DISTRIBUTION/AVAILABILITY OF ABSTRACT: UNCLASSIFIED/UNLIMITED ☒ SAME AS RPT. ☐ OTIC USERS ☐	21. ABSTRACT SECURITY CLASSIFICATION: Unclassified

22a. NAME OF RESPONSIBLE INDIVIDUAL	22b. TELEPHONE NUMBER (Include Area Code)	22c. OFFICE SYMBOL
Mark E. Snyder, 1LT, USAF	(505) 844-9758	NTAT

DD FORM 1473, 83 APR EDITION OF 1 JAN 73 IS OBSOLETE.

UNCLASSIFIED

SECURITY CLASSIFICATION OF THIS PAGE

CONTENTS

ILLUSTRATIONS

ILLUSTRATIONS

I. INTRODUCTION

Semiconductor device failure due to an electrical overstress is a primary concern in the nuclear hardening of strategic weapon systems. To acquire the postmortem knowledge necessary to determine the device failure mode, a reliable diagnostic basis in semiconductor physics is necessary. Efforts to achieve a comprehensive understanding of device failure have been hampered by a lack of adequate diagnostic tools and methods of study. This project's primary goal is to develop an experimental tool to study device failure, incorporating the scanning electron microscope (SEM) operated in the electron beam induced current (EBIC) mode. This technique, in conjunction with secondary electron imaging, will provide researchers with a diagnostic tool to qualitatively study the type of failure that occurs in semiconductor devices.

Although SEM operation in the EBIC mode has been recognized as an excellent diagnostic tool for device investigators (Ref. 1 through 5), the Air Force Weapons Laboratory (AFWL) does not possess this basic expertise. The addition of this tool will augment many aspects of ongoing research at the AFWL. To demonstrate the utility of EBIC, this effort will use EBIC and simple auxiliary measurements to determine the failure states of a twin set of specially designed semiconductor diodes.

Both types of diodes were constructed in the same manner (i.e. in terms of mask layout and diffusion methods) except for the addition of one extra P-type diffusion layer. This extra diffusion alters one set of diodes' reverse bias characteristics to exhibit soft avalanche breakdown at less than half the twin diodes' avalanche voltage (-55 V). As of these diodes' production date, it was not known why this additional diffusion drastically altered these devices reverse bias characteristics, or what type of failure states these devices would exhibit under an overstress.

II. EXPERIMENT DESCRIPTION

DIODE CONSTRUCTION AND ELECTRICAL CHARACTERISTICS

A special run of 100 identical N+P+ and N+P diodes was produced for this research project by the Sandia National Laboratories Microelectronics Department*. The diodes were constructed to provide a large peripheral area for SEM examination (Fig. 1). The N+P+ diode's diffusion structure consisted of a P+ and N+ diffusion into a P wafer (Fig. 2) that results in a diode with a low avalanche breakdown voltage (around 18 V) and variable avalanche knee characteristics. The N+P diode's structure consists of a N+ diffusion into a P wafer (Fig. 3) yielding an avalanche voltage of 55 V. Both diode structures were constructed with the same diffusion processes and mask layouts. Thus, the only differences incurred between the two types of devices result from the one additional diffusion to produce the N+P+ diodes. For ease of viewing, the units were mounted in 16 pin flat packs, with the covers unattached. Figures 4 and 5 show characteristic I-V curves for both types of diodes under reverse and forward bias. As the illustrations show, diode 034 (N+P+) has a higher forward current than device 093 (N+P). This was apparently due to diode 034's higher leakage current. The forward characteristics for all diodes were found to be consistent. Additionally, diode 093's reverse characteristics were identical to diodes 051 through 100. This accomplishment testifies to the consistency of the process which produced these diodes. Diode 034's initial reverse bias characteristics do not reflect diode 093's somewhat ideal electrical character.

* Sandia National Laboratories, Albuquerque, New Mexico.

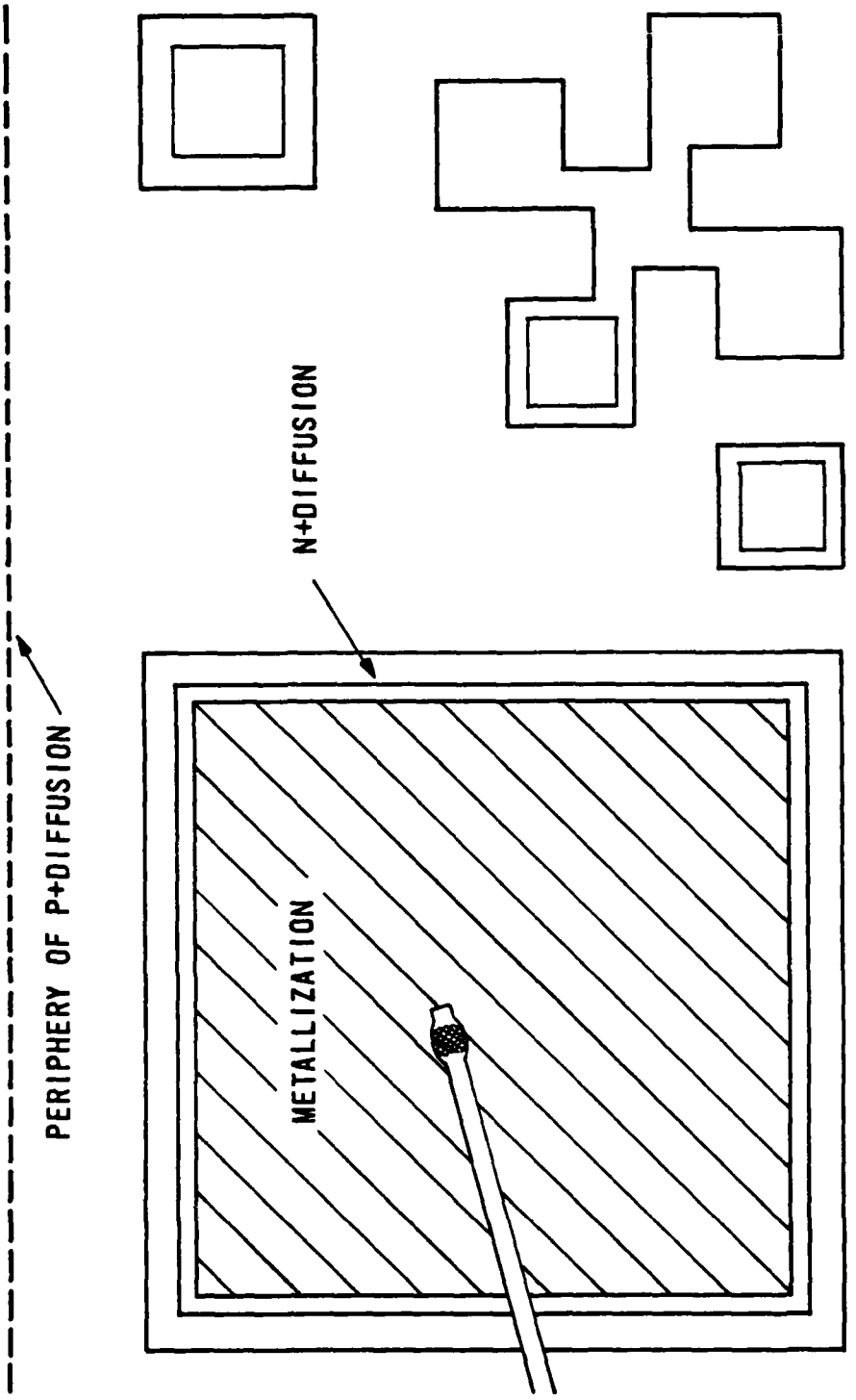


Figure 1. Diode test pattern on a P-type wafer with a doping of 3×10^{15} carriers/cm^3.

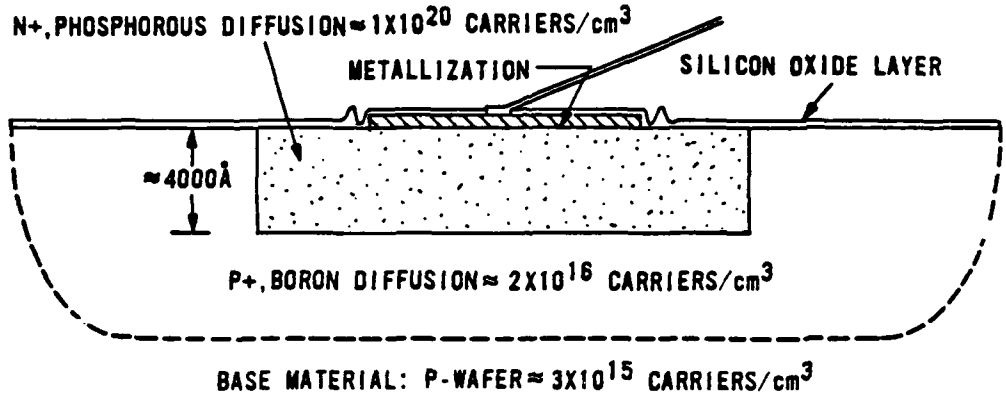


Figure 2. Sideview of the N+P+ silicon diode structure, double diffused (ion implanted) in a P-wafer.

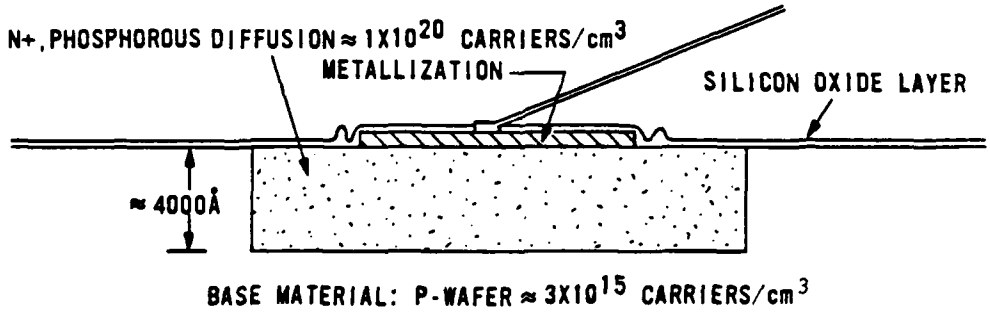
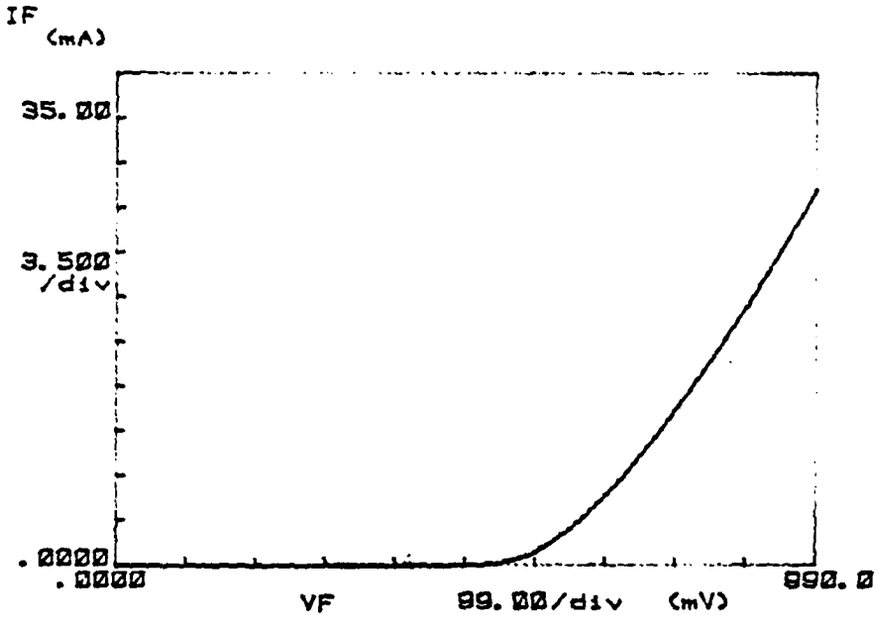
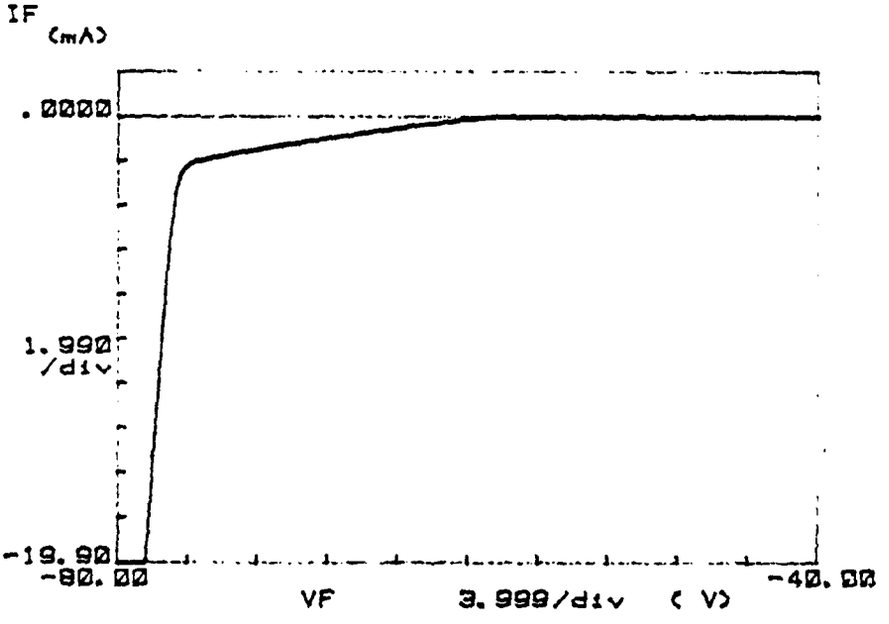


Figure 3. Sideview of the N+P diode silicon structure, single diffused (ion implanted) in a P-wafer.

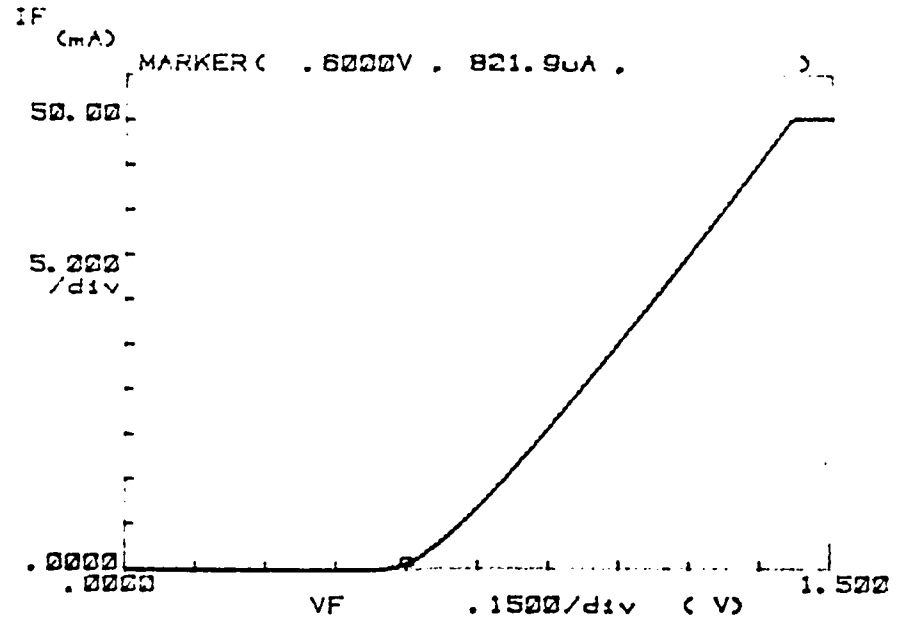


(a) Forward bias characteristics

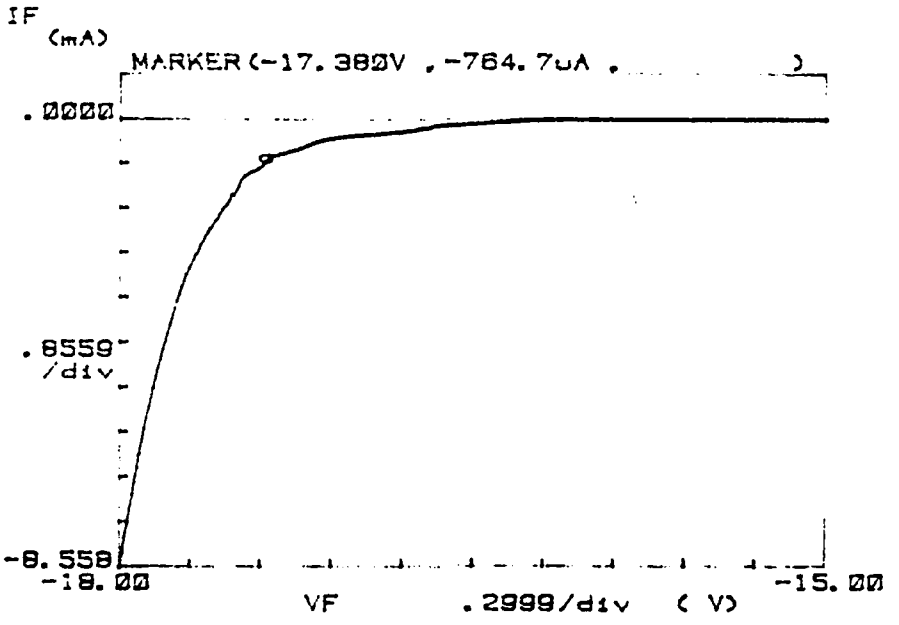


(b) Reverse bias characteristics

Figure 4. Current-voltage characteristics for diode 093.

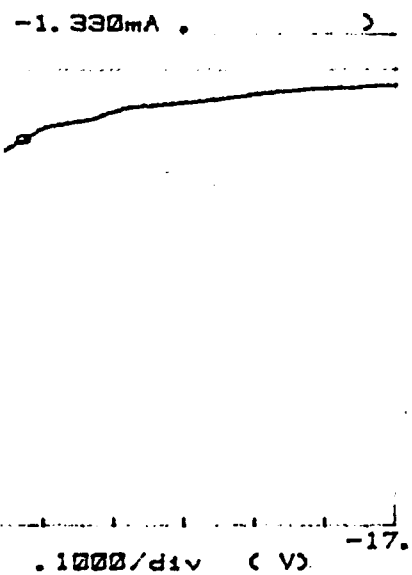


(a) Forward bias Characteristics



(b) Reverse bias characteristics

Figure 5. Current-voltage characteristics for diode 034.



alanche knee in Fig. b

Concluded.

The avalanche voltage of diode 034 is g
the addition of a soft breakdown knee w
formation (Fig. 5c). These formations
characterization runs when diodes 001 t
the avalanche knee--that were not stabl
Examination of diodes 001 through 050 a
avalanche breakdown voltage (despite th
was at reverse currents which varied be
diodes went through the same production
al P+ diffusion may be the source of th
characteristics. It was also determine
for both sets of devices were greatly r
one-sided step junction (Fig. 6). Thus
does not appear to be solely dependent

SCANNING ELECTRON MICROSCOPE OPERATION

The scanning electron microscope ca
of any inert object at extremely high m
resolution. This is accomplished by sca
narrow beam of electrons controlled by
the beam scans across the surface, seco
by a detector which provides input to a
ray tube (CRT). In a general sense, th
adjusted to the appropriate brightness,
microscope's apertures, stops, beam cur

Under normal viewing a semiconducto
secondary electron emission. But, by e

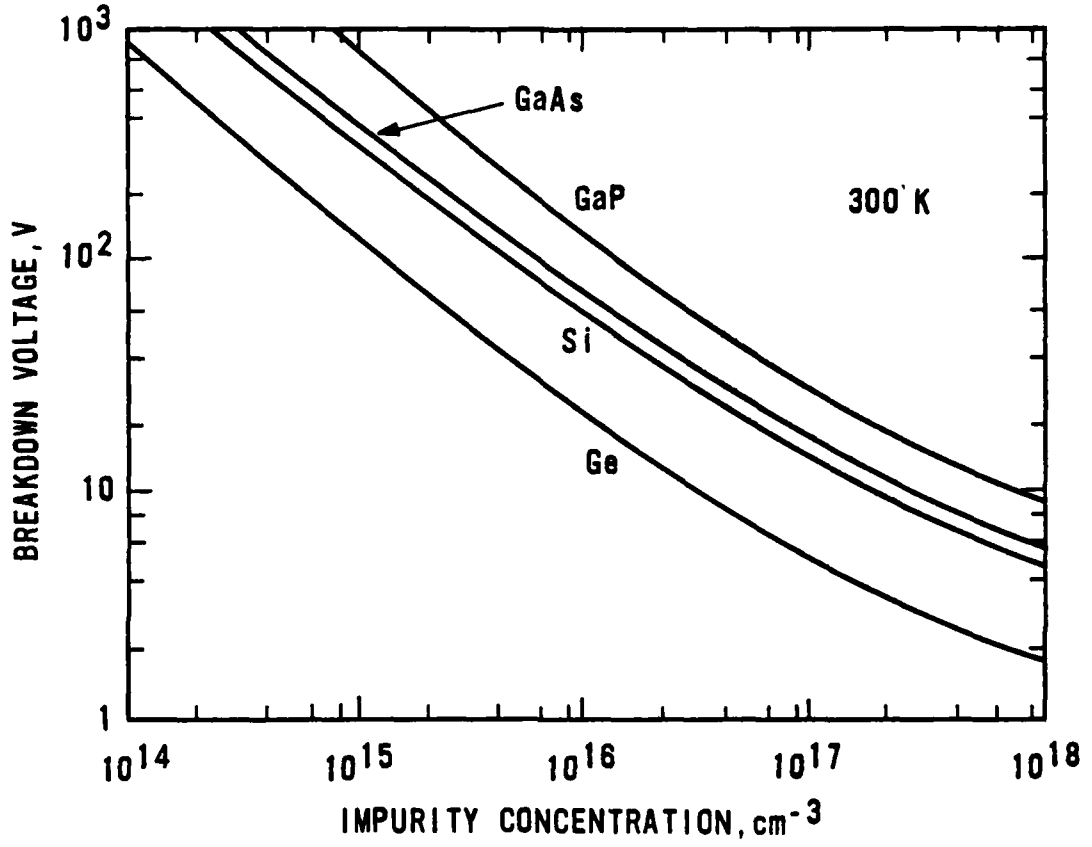


Figure 6. Calculated avalanche breakdown voltage of a one-sided step junction as a function of impurity concentration in the lightly doped side (after Ref. 6).

minute changes in the secondary emission, due to recombination processes inside the semiconductor, can be detected. The resultant image reveals areas of varying contrast, hence, the name voltage contrast imaging. Lighter regions represent areas with little bulk recombination while dark regions are areas with a great deal of bulk recombination. By applying a voltage to the semiconductor, these contrasting regions can be greatly enhanced allowing a fairly accurate determination of the electrically active areas of a semiconductor device.

This procedure can be used to provide practical methods for tracing active circuit paths in integrated circuits. But, this procedure is inadequate for viewing detailed individual device phenomena.

Observation of the specially constructed diodes under voltage contrast imaging (Figs. 7 and 8) reveals active regions, but it appears to be relatively insensitive to individual differences in defect density, and device construction. Thus, this method of viewing seems inadequate to determine microscopic effects in devices.

To derive more detailed electrical information through the SEM requires the use of the EBIC method. This procedure is similar to voltage contrast, except that the input to the imaging CRT comes from an electrometer connected across the sample. The EBIC mode method differs from voltage contrast primarily due to the source of input to the imaging CRT. Voltage contrast uses the secondary electrons emitted from the device by the interaction of the electron beam with the material as a source of imaging. The EBIC mode method incorporates the induced current in the device as the imaging source. By placing the electrometer in a fast mode of operation, and reading a current level on the same order of magnitude as the beam current, an image with light and dark regions appears which corresponds to areas of high and low current concentrations.

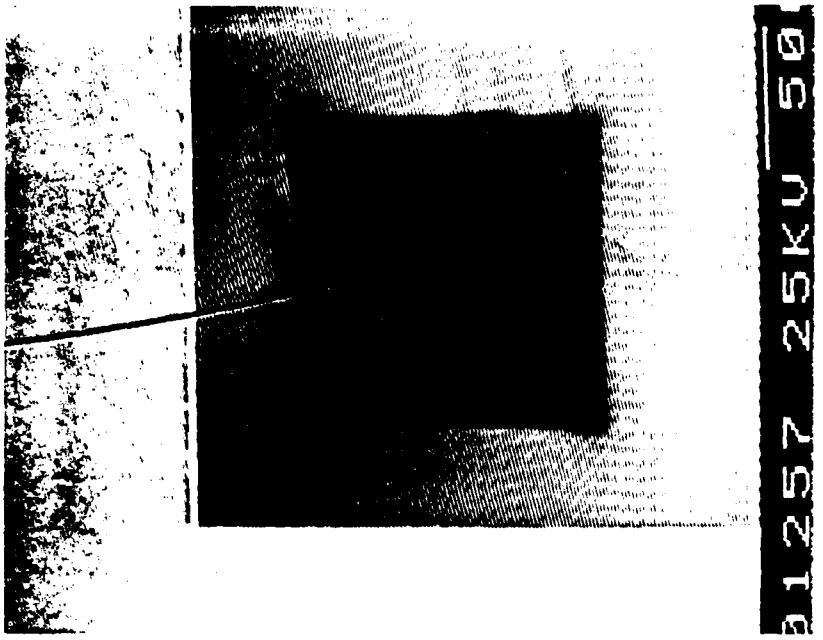


Figure 8. Voltage contrast imaging of device 100.

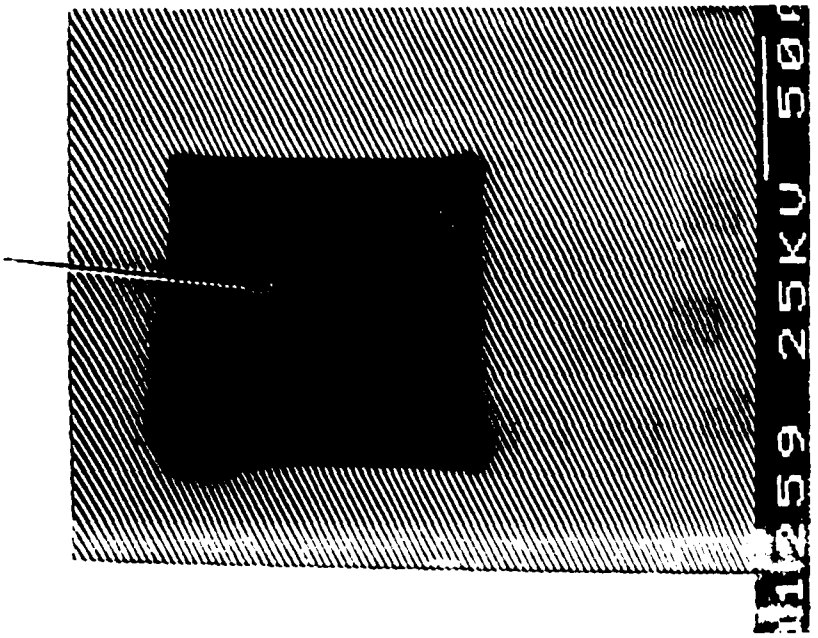


Figure 7. Voltage contrast imaging of device 001.

The advantage of this method over voltage contrast lies in its ability to examine a device's depletion region in detail. In particular, this method will allow for the accurate determination of a device's electrical activity.

As in voltage contrast, a voltage can be applied to the device to expand the electrically active regions (Ref. 7) to obtain more detailed information on avalanche breakdown, electrical activation of defects, and second breakdown (SB) (Ref. 8).

EXPERIMENTAL PROCEDURE AND SET-UP

The Materials Science Laboratory at the AFWL possesses a Hitachi model S500 SEM which has not been used before in the EBIC mode. The first part of the experimental procedure will thus involve an extensive exploration of this microscope's capabilities under EBIC operation, without extensive modification. Once this has been accomplished, attention will be given to determining the mode of failure of the two different sets of diodes. One set may contain a large number of defects due to a P+ diffusion into the P wafer, while the second set contains no P+ diffusion and possibly a smaller number of defects. These two sets will have a select few diodes exposed to various electrical overstresses to induce internal damage which alters their I-V curves significantly.

Upon degrading the devices they will be examined under the SEM in both secondary emission and EBIC modes to discern any physical or electrical change in the diodes. This analysis will be combined with normal electrical measurments to help determine the source of device degradation.

Finally, these diodes will be examined using EBIC and a variable DC and AC voltage across the diodes. This will provide information on the extent to which internal damage has changed the diode's normal operational characteristics.

III. EXPERIMENTAL RESULTS

The initial check-out of the test diodes was accomplished with a HP 4145A Semiconductor Parameter Analyzer using the dual in-line package of the HP 16058A test fixture. For the remainder of this report, diodes 001 through 050 represent the N+P+ diode structure. Diodes 051 through 100 reflect the N+P diode structure. As discussed previously, diodes 001 to 050 exhibit I-V curves that generally reflect those of Fig. 5. Individual differences in the shape of the breakdown knee were quite common, resulting in a varying current level at the measured breakdown voltage. These variations are possibly due to defect activation and consequent unstable microplasma formation (Ref. 9).

Devices 051 to 100 were tested via the same equipment as described. Figure 4 shows the I-V characteristics for device No. 093, which accurately reflects the I-V curves for diodes 51 to 100. Note that these curves do not possess any of the possibly defect-related characteristics exhibited by the N+P+ diodes. In addition the avalanche breakdown voltage and turnover voltage in the forward directions between both sets of diodes is quite different.

It is possible that this unexpected lowering of the breakdown voltage for both the N+P+ and N+P diodes is due to breakdown at the curved regions of the device's depletion region (Ref. 10). It is also possible that defects in the N+P+ diodes may have effectively lowered the breakdown voltage further due to defect activation (Ref. 9). This same effect may also account for some of the differences in reverse bias leakage current between the two sets of diodes.

Thirteen devices were chosen at random to be used in the experiment. Those devices were: 001, 008, 009, 011, 018, 028, 042, 046, 081, 086, 088, 097, and 100. Devices 001 and 100 were chosen for voltage contrast measurements only, with the rest to be used primarily in the EBIC mode of observation. Excitation

of the devices will be performed by the HP 6827A power supply/amplifier operating in the constant current mode, while under EBIC and voltage contrast examination.

VOLTAGE CONTRAST RESULTS

After initial setup of the SEM, a voltage is applied to bias the device in the forward or reverse direction. Contrast controls are set to amplify differences in the image's shading as various voltages are applied.

Using this method, initial investigation of devices 001 and 100 did not reveal a great deal of fine structure in the diodes' depletion regions. Figures 7 and 8 show devices 001 and 100 with a DC reverse bias of 30 and 100 V, respectively. It should be noted that portions of the image may be affected by device heating. This results in a blooming of the image which is a good sign of degradation. Retesting of these devices showed a definite electrical degradation in the reverse bias direction.

Normally, voltage contrast is successful in indicating differences in semiconductor devices without damaging them. These devices display characteristics (due to device construction) that severely limit this method of observation. For example, the dopant concentrations in the N+P and N+P+ diodes create a depletion region that is extremely hard to resolve, even under high magnification SEM observation. This drawback may hamper efforts to observe detailed electrical effects, since the majority of electrical activity occurs in and around the depletion region.

As Figs. 7 and 8 reveal, voltage contrast does not yield a high degree of resolution for the devices tested. Thus, continued work with the voltage contrast method appears to present a very limited method of collecting information.

EBIC MODE METHOD RESULTS

Operation of the SEM in the EBIC mode is well documented in a number of references (Refs. 1 through 5). Many of these articles do not describe the initial setup of the SEM alone. The EBIC method is a simple concept to understand and apply; but, the actual experimental characterization of a device using the EBIC method is an intimate function of the SEM's capabilities and construction. The SEM in operation at the Material Sciences Laboratory of the AFWL has never been used in the EBIC mode of operation. Thus, a prenascent knowledge of using the Hitachi S500 SEM in the EBIC mode did not exist in industry or academia and had to be developed for this research effort. After a great deal of trial and error, a basic set of guidelines has been developed to aid in using EBIC on other SEMs besides the Hitachi S500 SEM.

Primary to any EBIC mode operation is the amount of SEM beam current striking the device under test. Too much current will swamp any imaging ability of an electrometer connected in series to the device, while too little current will barely register any visual difference.

It was also apparent for this set of experiments, that the electrometer type had a strong influence on the optimum SEM beam current. This conjecture is based on the idea that an electrometer's reaction time when connected to the SEM's video amplifier is usually optimal at certain spans of measured current and SEM scan speed. For example, at small current scales where the meter deflection is large (for a certain SEM scan speed and beam current) the visual image is swamped out. This is especially acute for device surfaces exhibiting large differences in induced current. Initial trial and error testing for this effort demonstrated that the beam current had to be set at about 75 μA--much

lower than the normal operating level (as compared to normal SEM secondary imaging).

Additional concern must be taken in EBIC mode operation to remove, or open, all apertures in the SEM column. This activity visually increases the resolution of the EBIC mode signal. The one drawback incurred due to open apertures is a small loss of image quality at high magnification (dependent on SEM design).

One final consideration is the speed of response and type of electrometer used to pick current off the device under test. Normally, the experimenter will have to adjust the SEM scan rate across the device to optimize the electrometer reaction time and, thus, image resolution (later photographs show how a slow electrometer can add artifacts to photographs that represent lost data (Fig. 11b). Thus, the faster the electrometer the better the resolution. Another consideration concerns measuring device current when it is biased by a power supply. This study found that operation of the electrometer in the same circuit with the diode and power supply created an additional ground loop between the supply and the SEM video amplifier.

To overcome this problem, an ungrounded power supply (such as batteries) or a battery operated electrometer should be used. This effort could not study this aspect, since a battery operated electrometer or batteries sufficient to bias the devices were not available.

Diodes 088 and 042 were the first devices examined. Trial and error during a long period of experimentation resulted in the first recorded EBIC images of a device at the AFWL (Figs. 9, 10, and 11).

Device 088 was photographed (Fig. 11) when the EBIC image first appeared, and graphically shows the presence of active regions in the device. The glowing rectangular band in the picture represents the electrically active region below the N diffusion. The fuzzy region on the edge of the rectangular

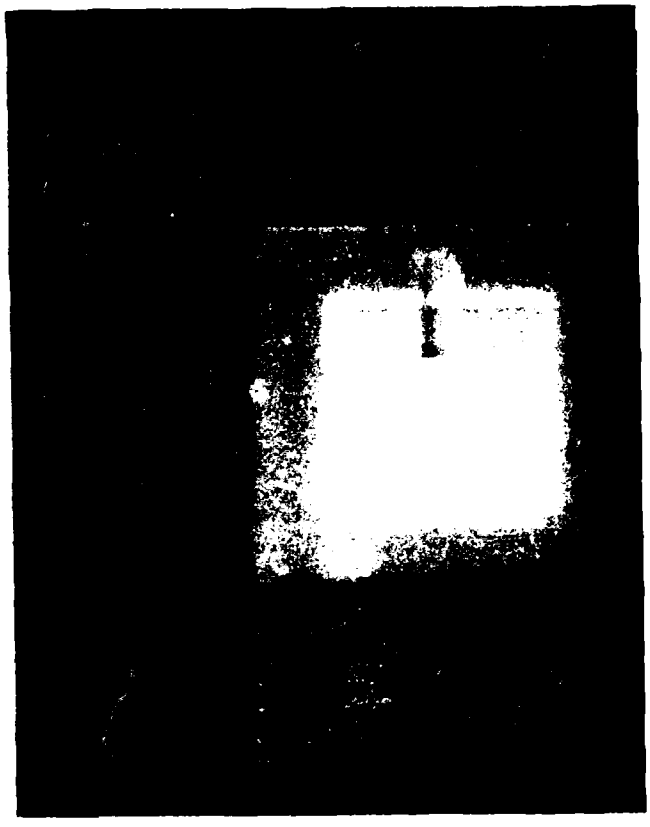
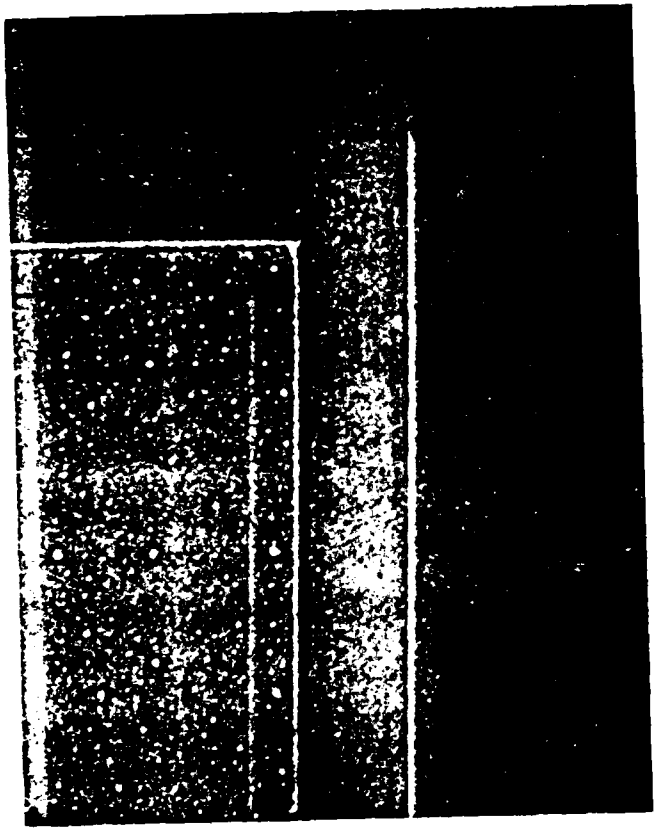
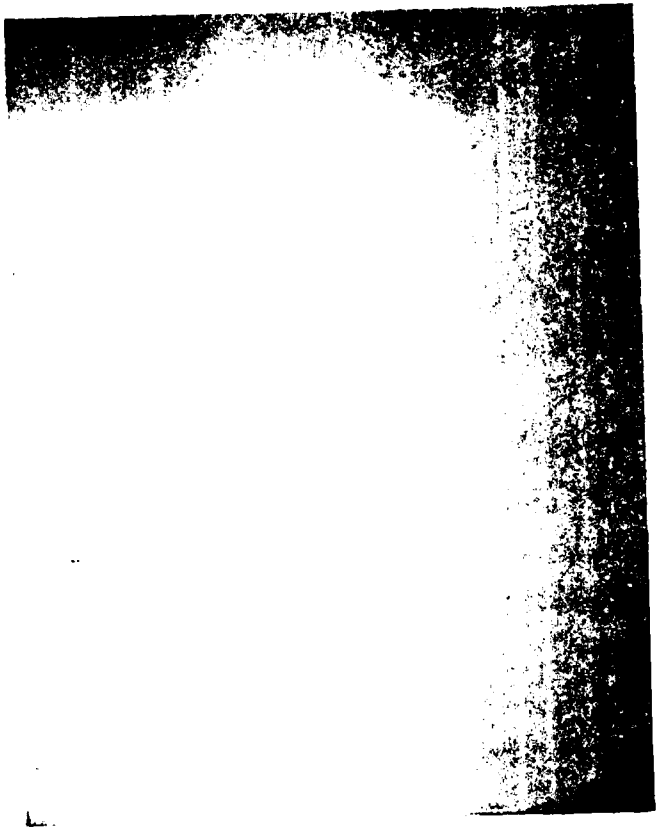


Figure 9. First recorded EBIC image taken at the AFWL Material Sciences Laboratory using device 088.



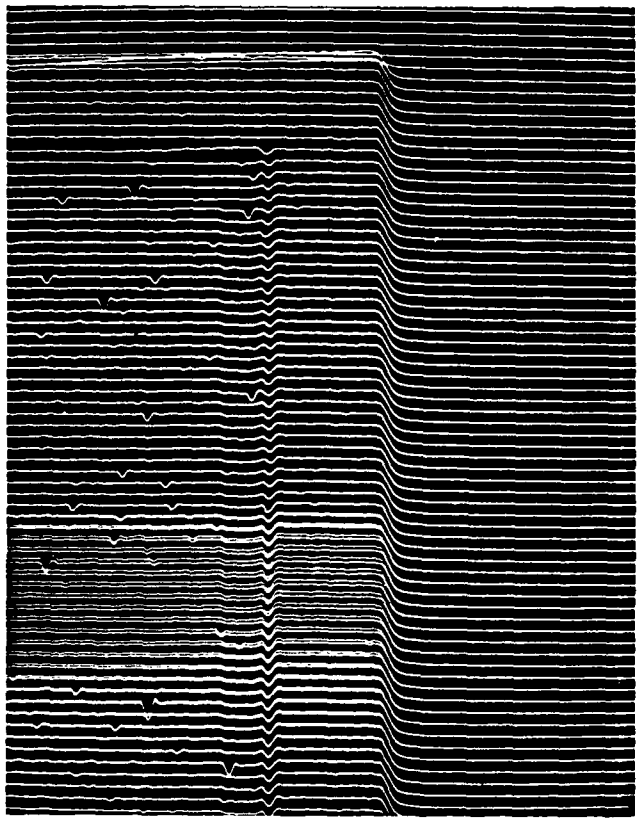
(a) Secondary electron image



(b) EBIC image

Figure 10. The SEM image of the upper right-hand corner of device 088, 300x magnification.

(a) EBIC image of device 042. The dark area to the right of the depletion region is an artifact generated by the electrometer's insufficient reaction time.



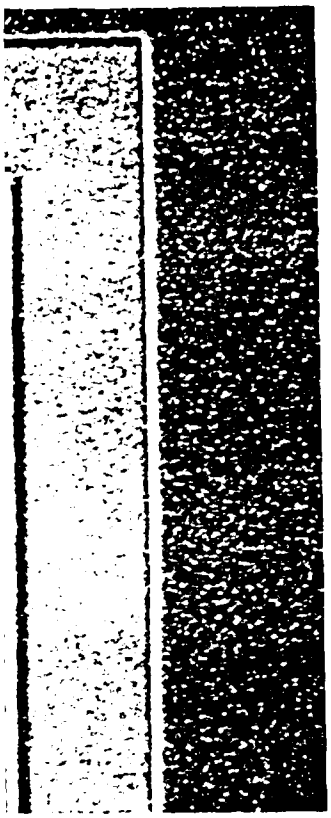
(b) Inverted line scan topography of device 042

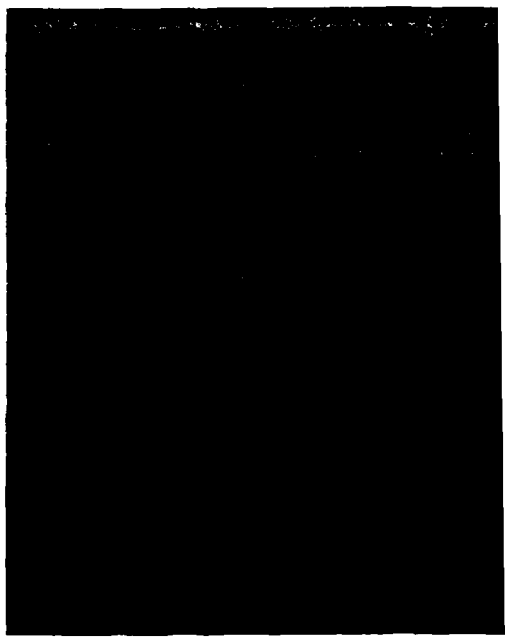
Figure 11. The SEM image of device 042, 300x magnification.

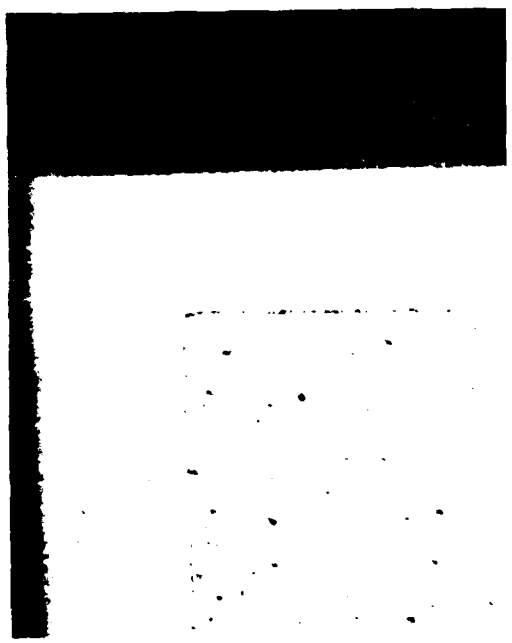
band shows the depletion regions extension into the P region of the device. Figure 10 shows a close-up of the upper righthand corner of the device in secondary and EBIC mode. The depletion region is clearly defined in this EBIC mode photograph but, since the accelerating voltage of the SEM (20 kV) drives the electrons deep into the device, the depletion region appears bright throughout the N region and fairly diffuse into the P region. This effect will be noticeable on all forthcoming EBIC mode photographs and can be adjusted by decreasing the accelerating voltage. These diodes are relatively thin so even at a low accelerating voltage the electrons are driven down the entire depth of the device. Also, decreasing the accelerating voltage by too large an amount makes the EBIC mode image difficult to observe.

Figure 11 shows device 042 in EBIC mode image and inverted line scan topography. The most noticeable aspect is the differences that depict it from device 088. In particular, the depletion region of device 042 seems closely restricted to the N region of the device with little diffusion into the P region. This may be attributable to the heavy doping level of the diodes P+ side. For these diodes, the amount of trapped charge on both sides of the metallurgic junction are the same (since the doping level is so high [$> 10^{16}$ carriers/cm^3] only a small volume of charge is required to provide neutralization of the device's built-in voltage) thus, the depletion region is much smaller for the N+P+ diodes as the EBIC mode image shows.

Device 001 had been exposed to high voltages when photographs were taken under voltage contrast imaging. Thus, it was suspected that the device may have been damaged although an extensive survey of the surface showed no perceptible damage. Figure 12 shows the upper right-hand corner of device 001 in secondary image with a large number of white grains covering the surface. The metallization also shows pits and large globules of unknown origin. Figure 13





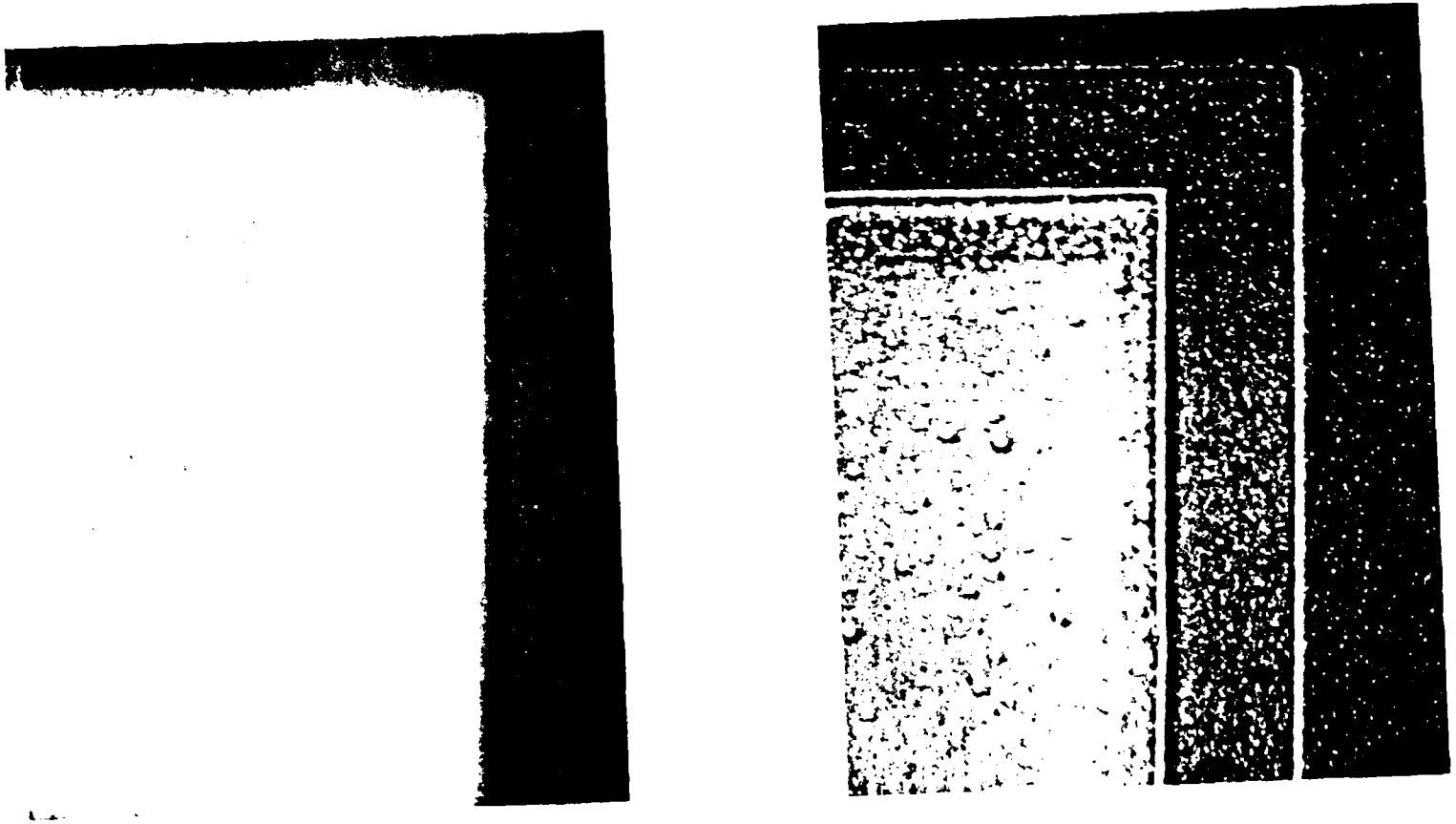


liode 001 at 400x magnification.

shows the EBIC mode images of Fig. 12, in normal white contrast and reverse dark contrast. This reverse image is produced by reversing the electrometer leads to the device. Depending on the surface, a reverse image may provide more information on device characteristics than a positive polarity photograph. These photographs show a depletion region that is more extensive than seen on diode 042. This may imply some change in the static I-V characteristics due to a larger depletion region.

Device 008 was exposed to large voltages in an attempt to reproduce EBIC mode images early in the research effort. At the time, no images were obtained but preliminary checks prior to actual EBIC mode imaging showed the diode's characteristics had changed somewhat. A search of the device surface showed no perceptible damage. The EBIC mode image (Fig. 14) looks similar to Fig. 11, in the respect that the depletion region's extent looks the same. Also, the granulation and metallization pitting are similar to that found on device 001.

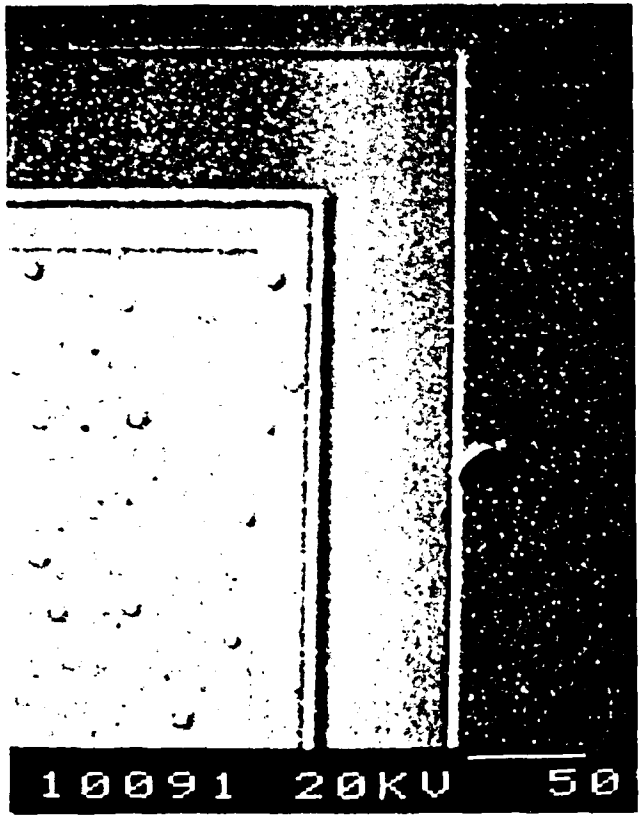
Device 009 had also experienced high voltage while attempting to achieve EBIC mode imaging. Preliminary checks before successful EBIC mode imaging did reveal some I-V changes, and a close examination of the surface revealed several possible abnormalities. Once again the surface granulation was readily apparent, but, observation of the right-hand side of this diode revealed an extrusion between the N+ and P+ regions of the diode (Fig. 15). This secondary imaging shows a definite extrusion that slightly affects EBIC mode imaging of the diode (Fig. 16). This extrusion is possibly an ejected melt due to second breakdown (Refs. 10 and 11). Although this extrusion should have a greater effect on electrical activity in the area (if it was caused by SB) EBIC mode imaging does not demonstrate any effect on local electrical activity.



(a) EBIC image

(b) Secondary image

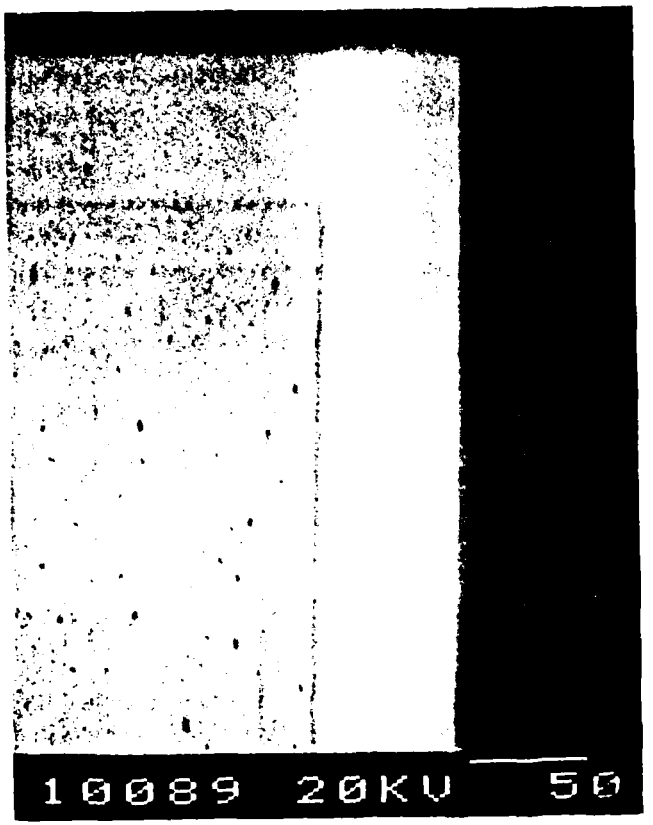
Figure 14. The EBIC and secondary electron images of device 008.



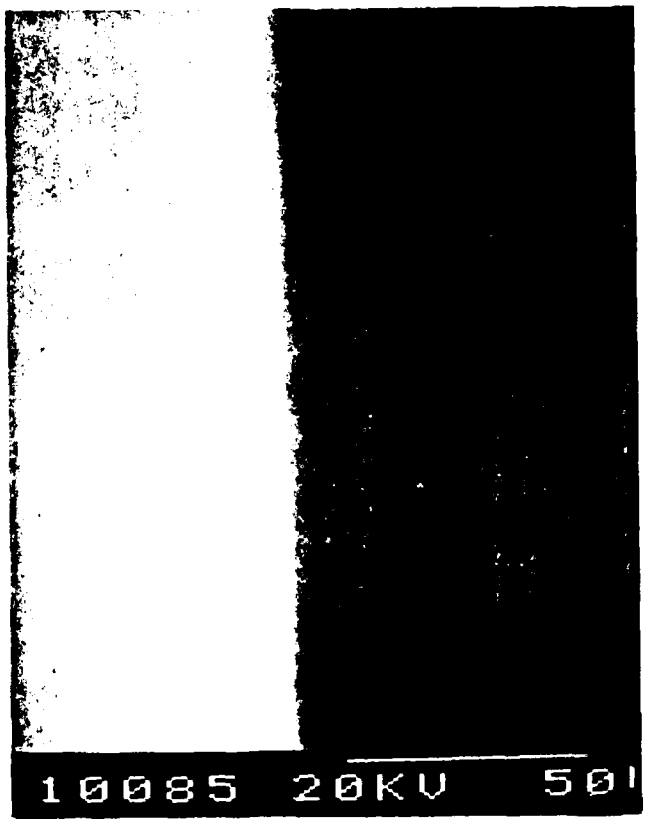
(a) Extrusion at 400x

(b) Extrusion at 4000x

Figure 15. Secondary electron image of device 009.



(a) At 400x



(b) At 4000x

Figure 16. The EBIC image of extrusion found on device 009.

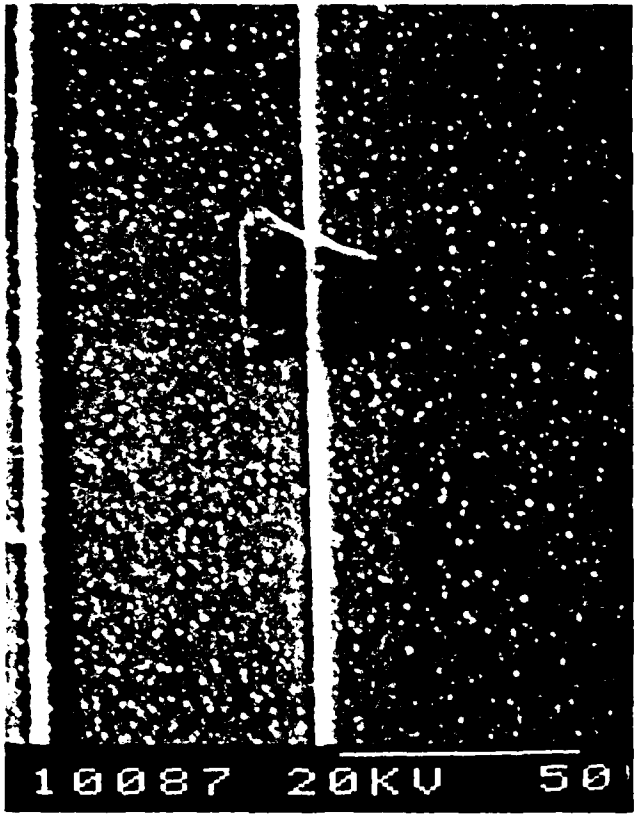
Farther down the diode edge from this extrusion, another extrusion appears (Fig. 17). This abnormality does seem to affect the EBIC mode image. Overdriving the electrometer brings this effect out most dramatically (Fig. 18a). Figures 18b and 19a show a depression that was found on the device's lower edge between the metallization and N+ diffusion. The EBIC imaging of this area showed no electrical abnormalities. The lower left-hand corner of the device metallization showed a distinct pitting between the metallization and N+ diffusion (Fig. 19b). This pitting (which is seen on other predamaged diodes in this report) may be the result of oxide contaminant thermal activation or metallic migration.

Device 011 (also predamaged) showed extreme pitting all along the periphery of the metallization (Fig. 20). Only two photographs of these pits are shown as representative of this effect. The EBIC mode imaging of this diode showed no irregularities (Fig. 21).

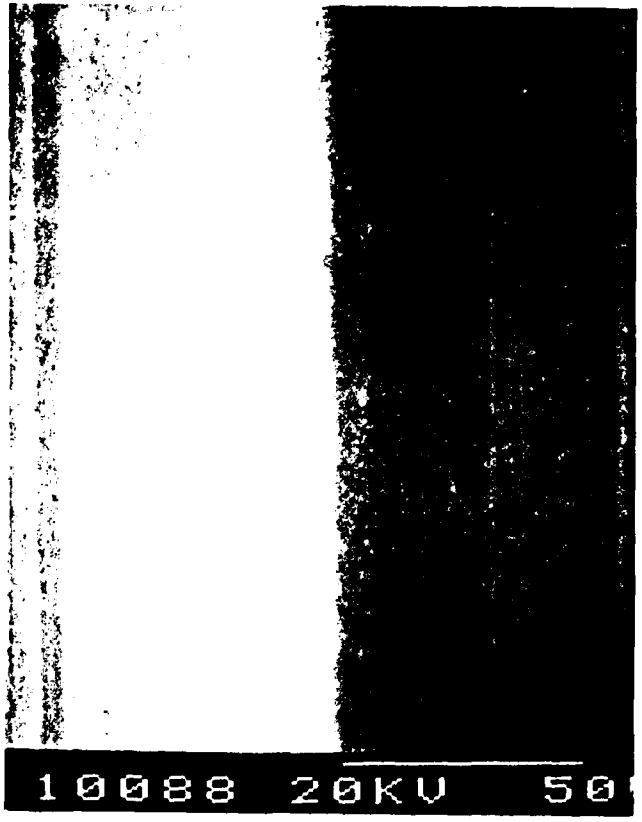
Device 018 (also predamaged) showed no abnormalities in EBIC or secondary mode imaging (Fig. 22).

Device 100 had been viewed using the voltage contrast method discussed earlier in this report. Thus, the device was suspected of being damaged due to the applied voltage. Secondary imaging showed numerous pits along the metallization periphery (Fig. 23); yet, no abnormalities were seen using EBIC mode imaging. Figure 24 shows the upper right-hand corner under EBIC mode imaging which brings out the distinctive depletion region of the device. It was also noted that this diode exhibited a great deal of surface charging. This effect may be caused by surface damage to the diode although this cannot be verified at this time.

Device 097 was an early casualty to poor initial attempts to obtain voltage contrast measurments. Voltages in excess of 75 V were applied to this device in taking unsuccessful voltage contrast images. Observation using secondary

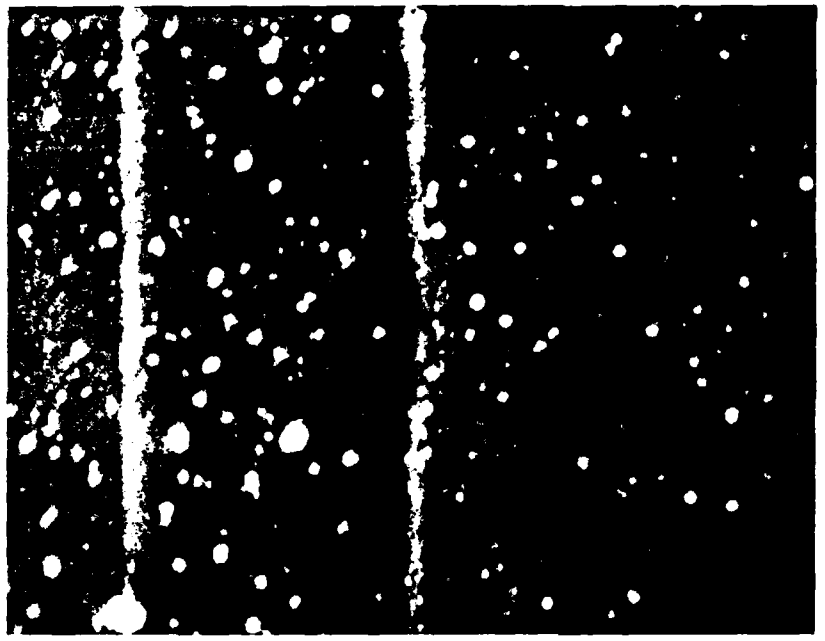


(a) Secondary electron image, 800x

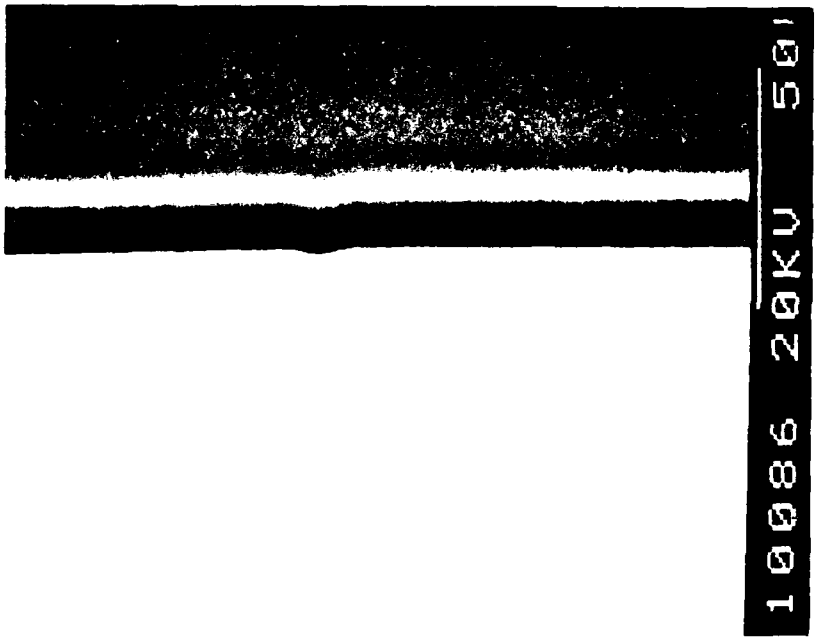


(b) EBIC image of defect at 800x

Figure 17. Secondary and EBIC image of second defect on device 009.

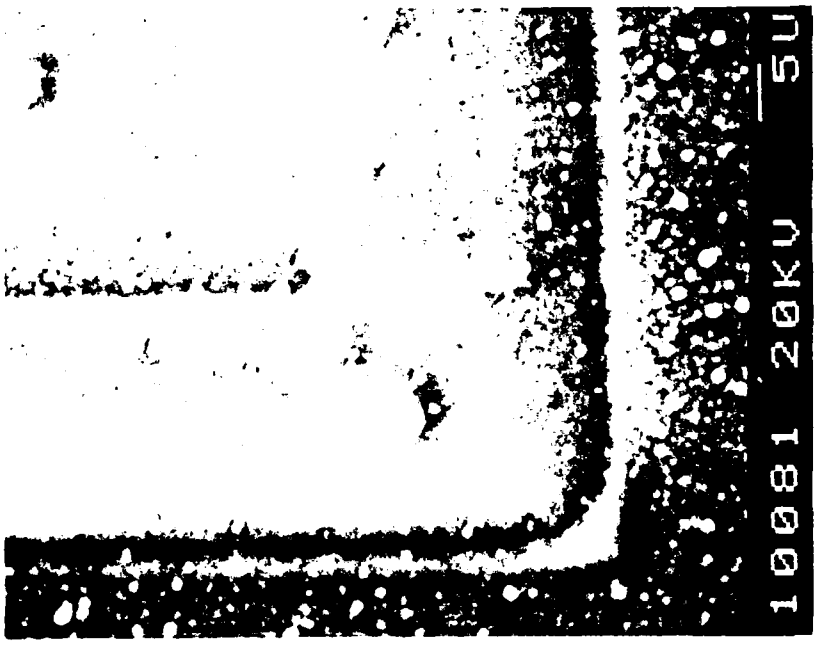


(b)

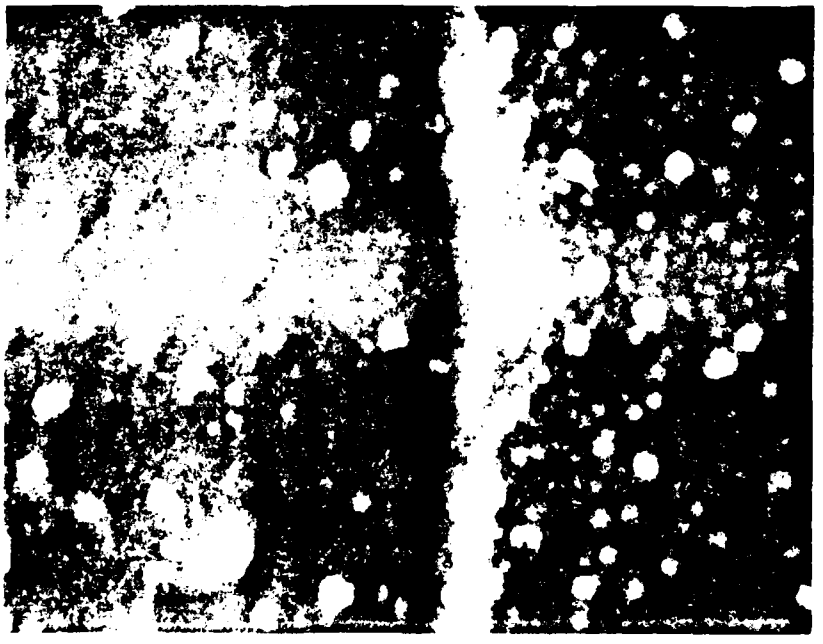


(a)

Figure 18. (a) Intensified EBIC image of second defect, (b) Secondary electron image of third defect on diode 009 at 2000x.



(b)



(a)

Figure 19. (a) Secondary image of the third defect on device 009 at 4000x,
(b) Secondary image of metallization pits on diode 009 at 2000x.

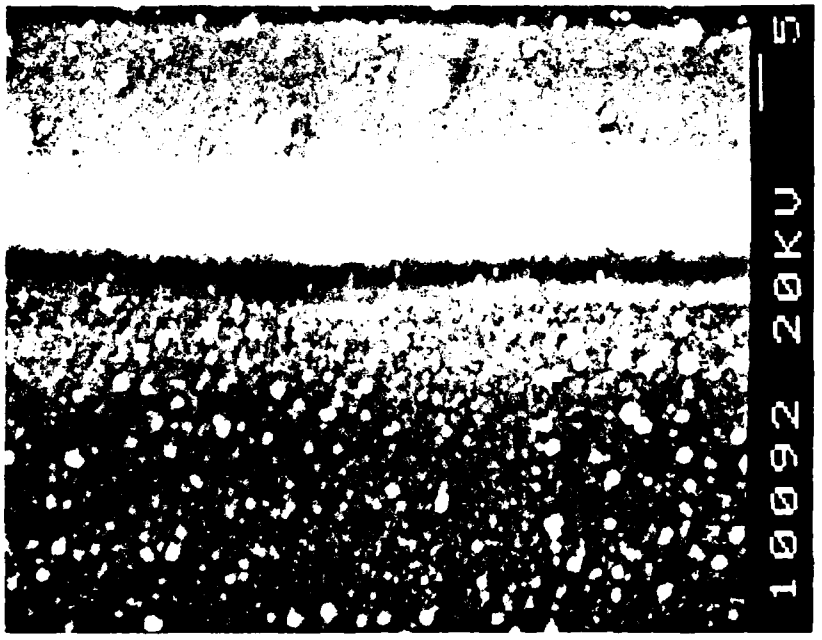
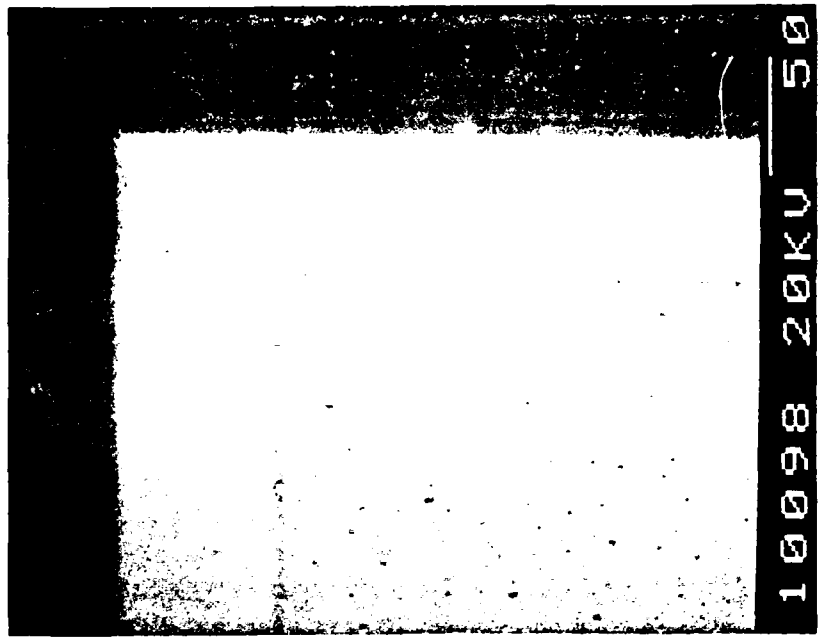
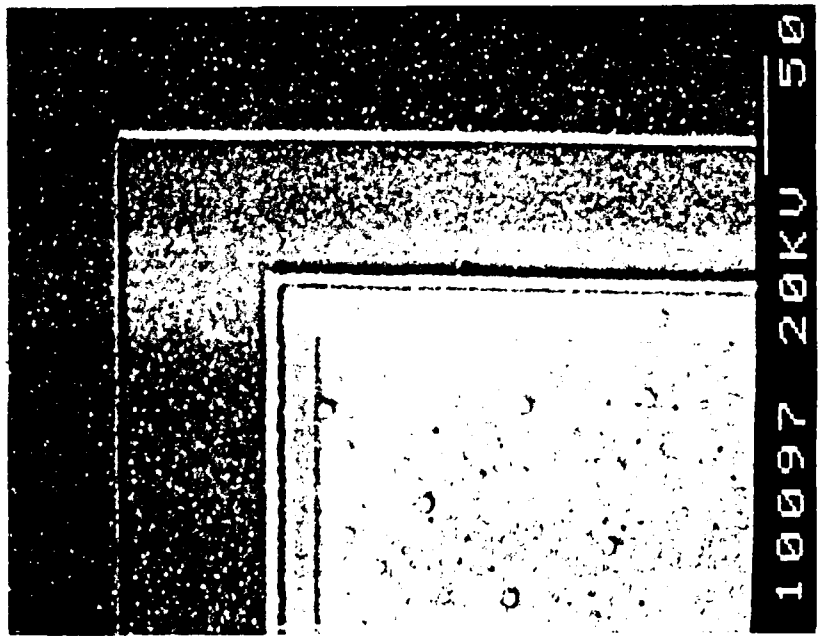


Figure 20. Secondary image of metallization pits on device 011 at 2000x.

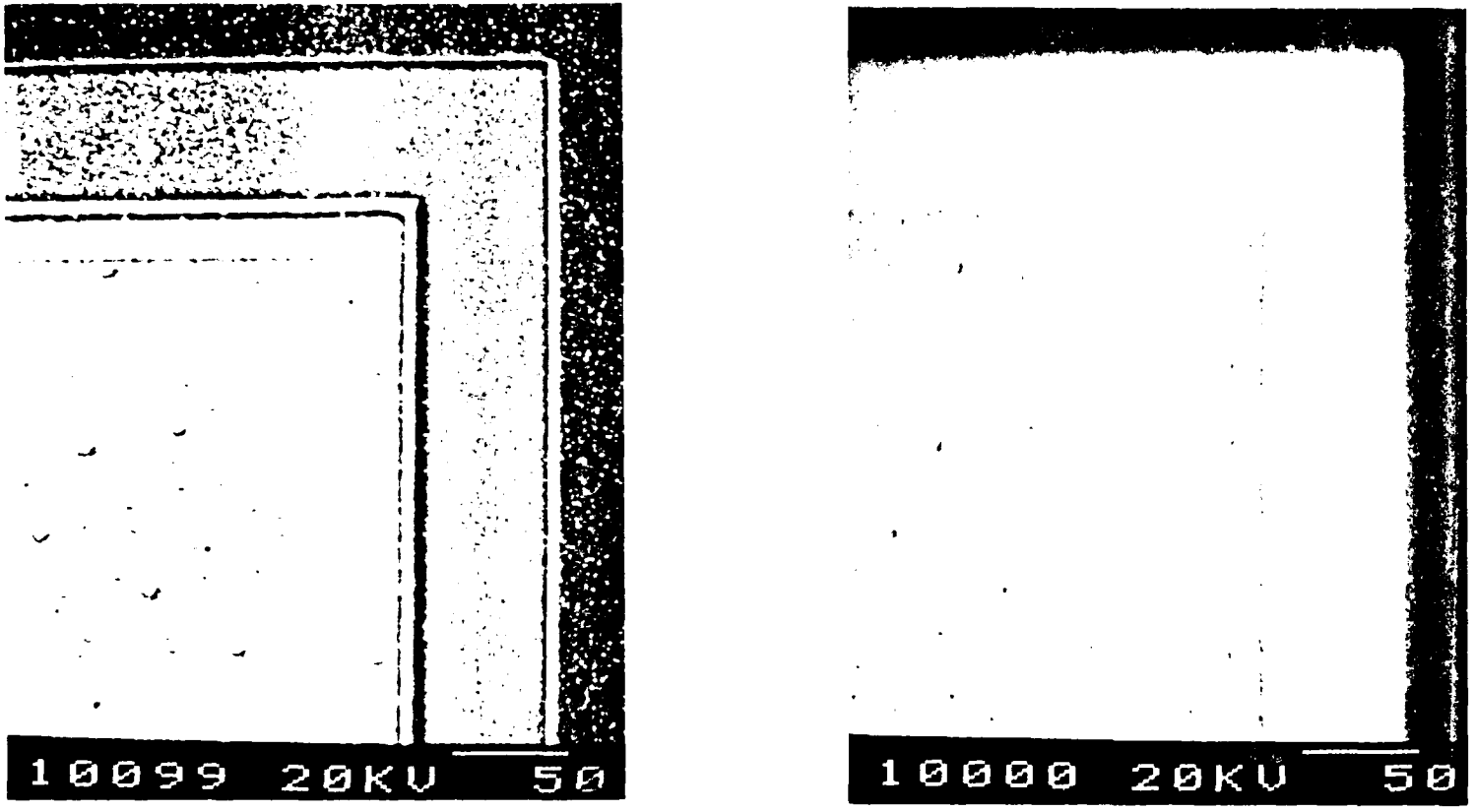


(b)



(a)

Figure 21. (a) Secondary image of diode 011 at 400x. (b) EBIC image of diode 011 at 400x.



(a) (b)

Figure 22. (a) Secondary image of diode 018 at 400x. (b) EBIC image of diode 018 at 400x.

Figure 23. Secondary image of metallization pits on diode 100.

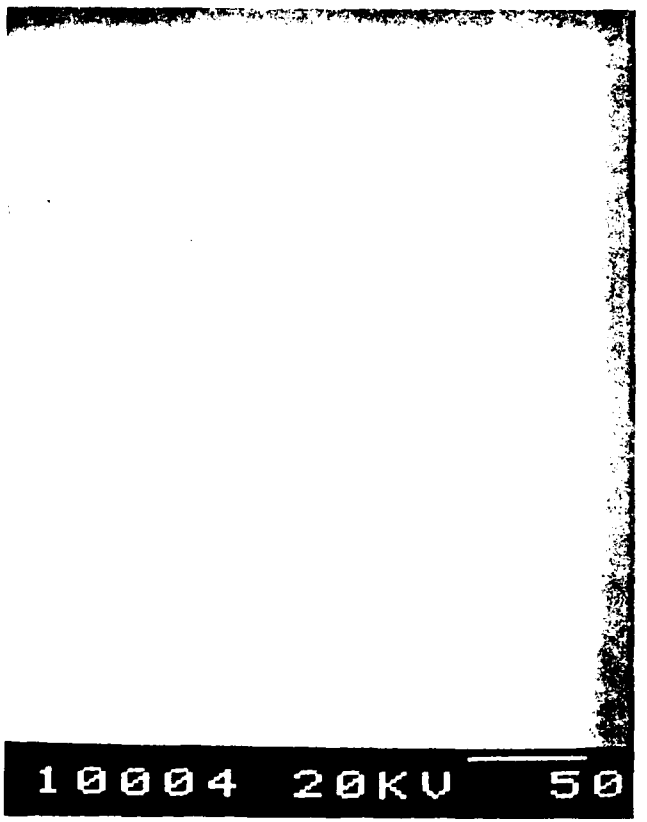


Figure 24. EBIC image of diode 100 at 400x.

ıg the metallization periphery (Figs.
ıt show any distinct abnormalities (Fig.
ı conjecture that the pits observed
l by device damage. To test this con-
·e observed using EBIC and secondary
ːed no overstresses during any part of
ıble to provide an adequate test of this

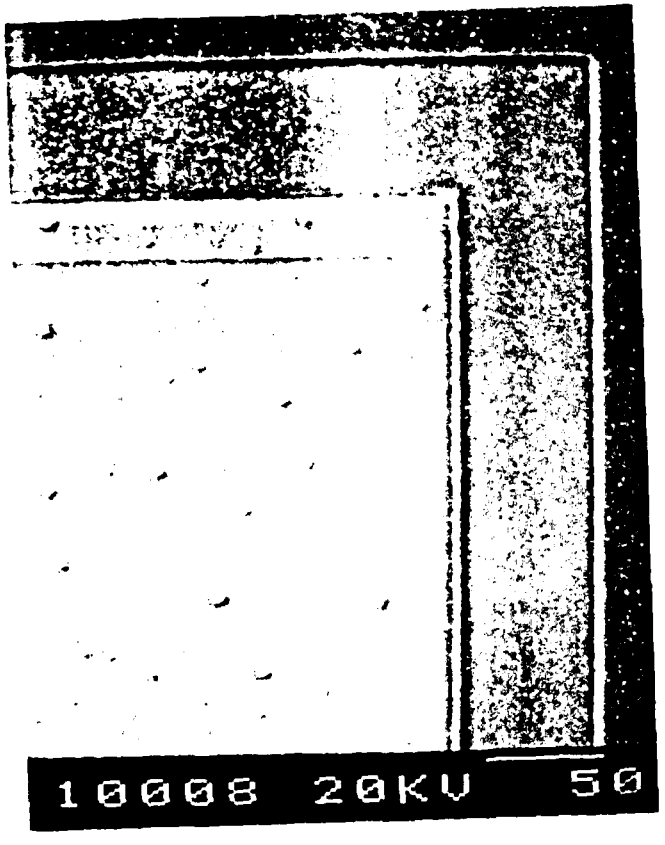
ing did provide some evidence of pits
but, these pits were not as numerous
ɐ EBIC mode imaging showed no distinct

of pits on the metallization periphery
042 (Fig. 30a). Secondary imaging
e diffusion boundary, where a surface
ced EBIC mode photograph of this defect
layer edge (Fig. 31b). This location
e 32 shows the secondary and EBIC mode

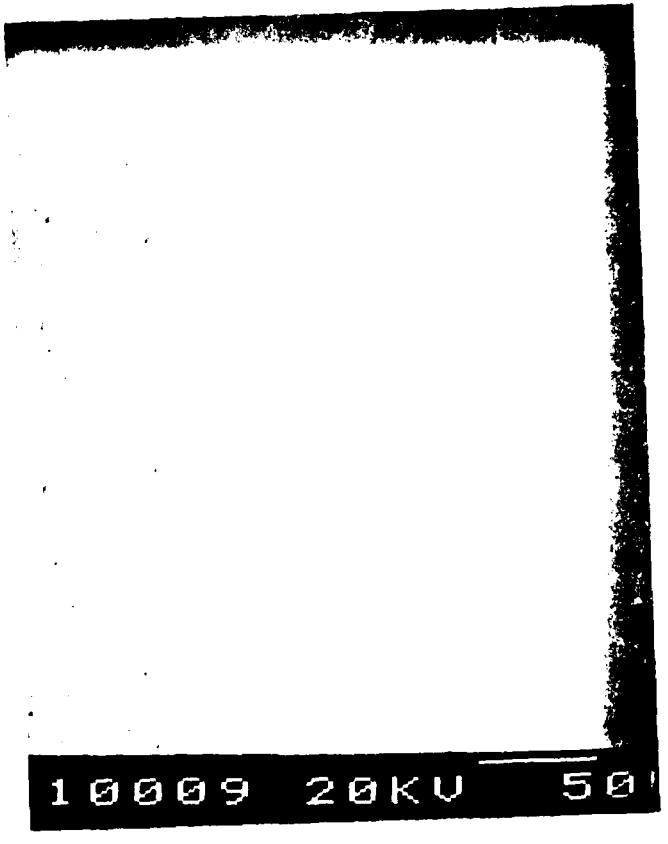
small number of pits similar to devices
ging showed no irregularities for

lly the conjecture that the metalliza-
existence of the pits prior to damaging
d to device fabrication processes.
damage appears to increase the number

Figure 26. Secondary image of metallization pits on diode 097.

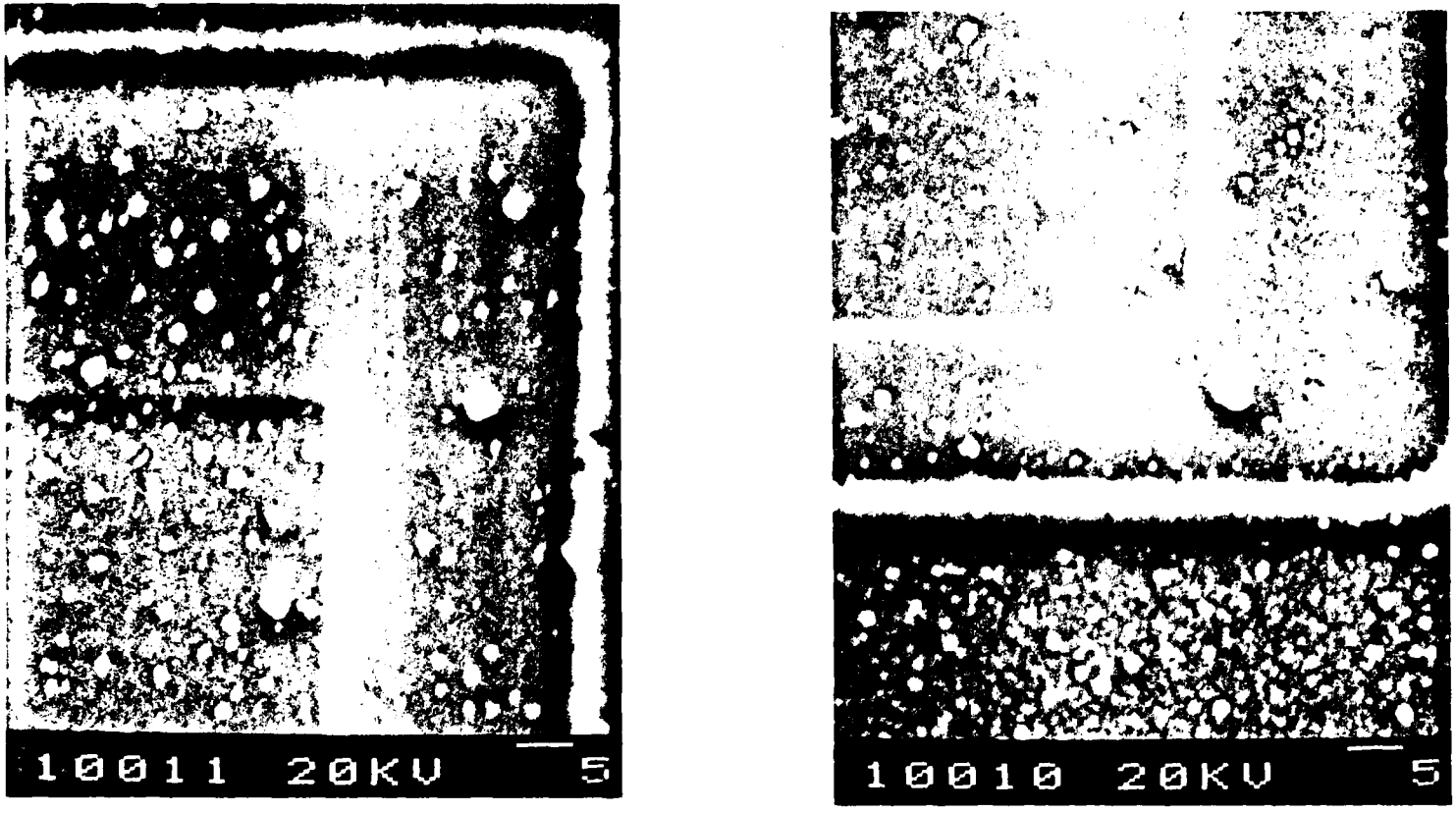


(a)



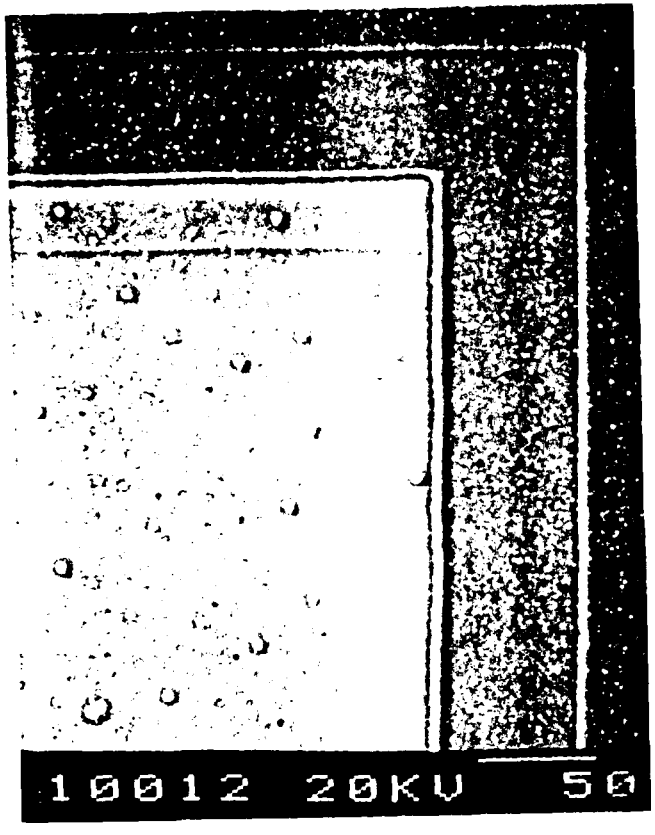
(b)

Figure 27. (a) Secondary and (b) EBIC image of diode 097.

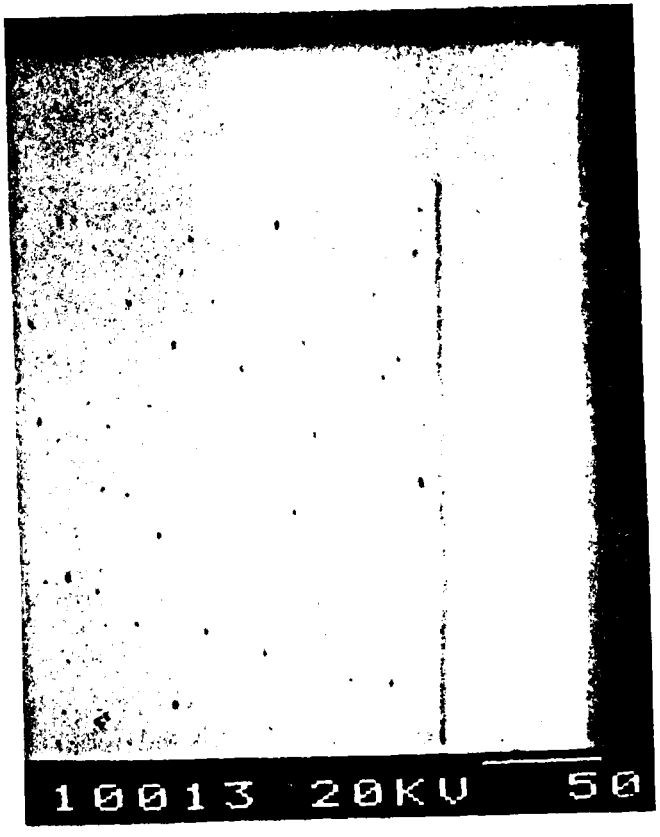


(a) (b)

Figure 28. Secondary image of metallization pits on diode 042 at 2000x.

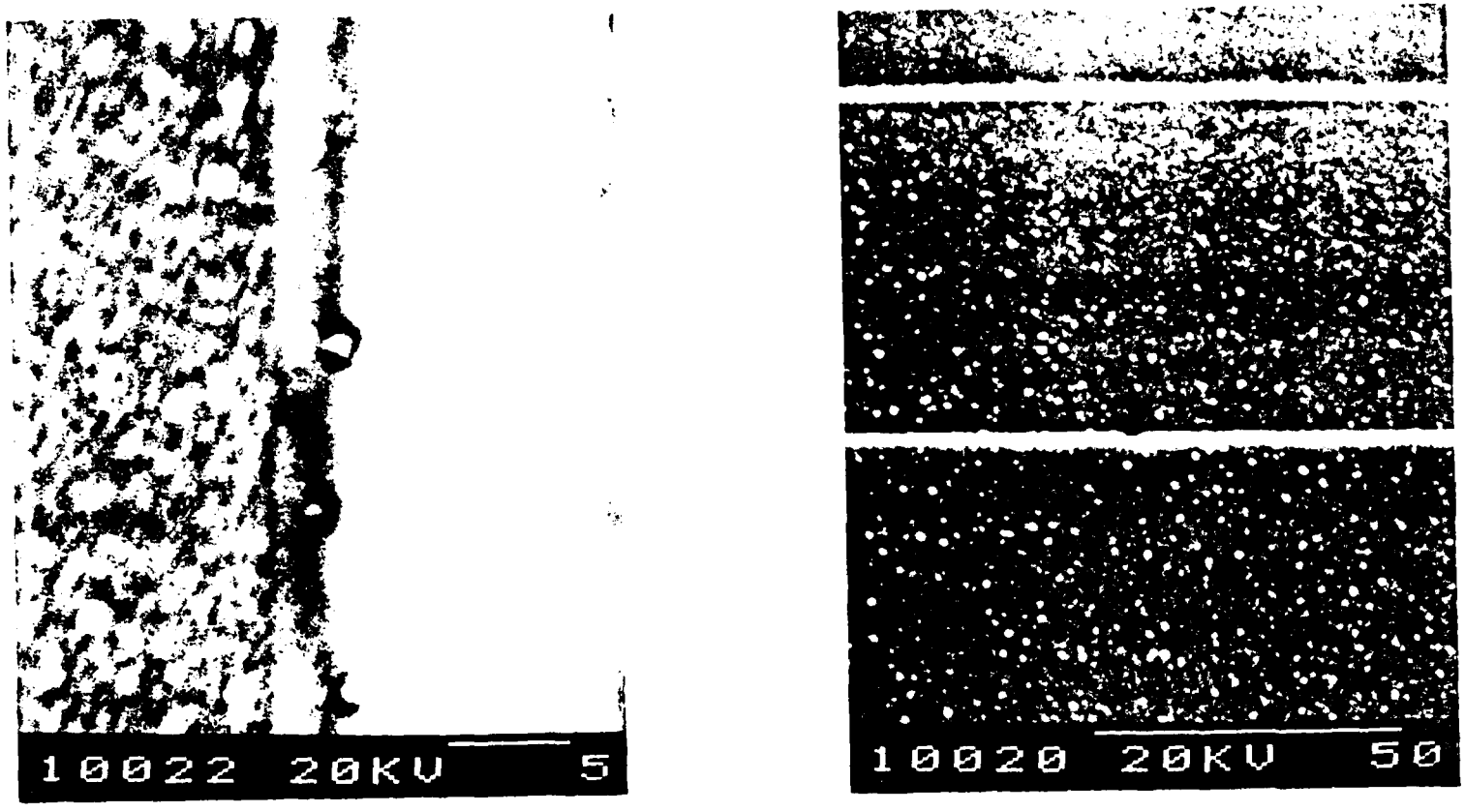


(a)



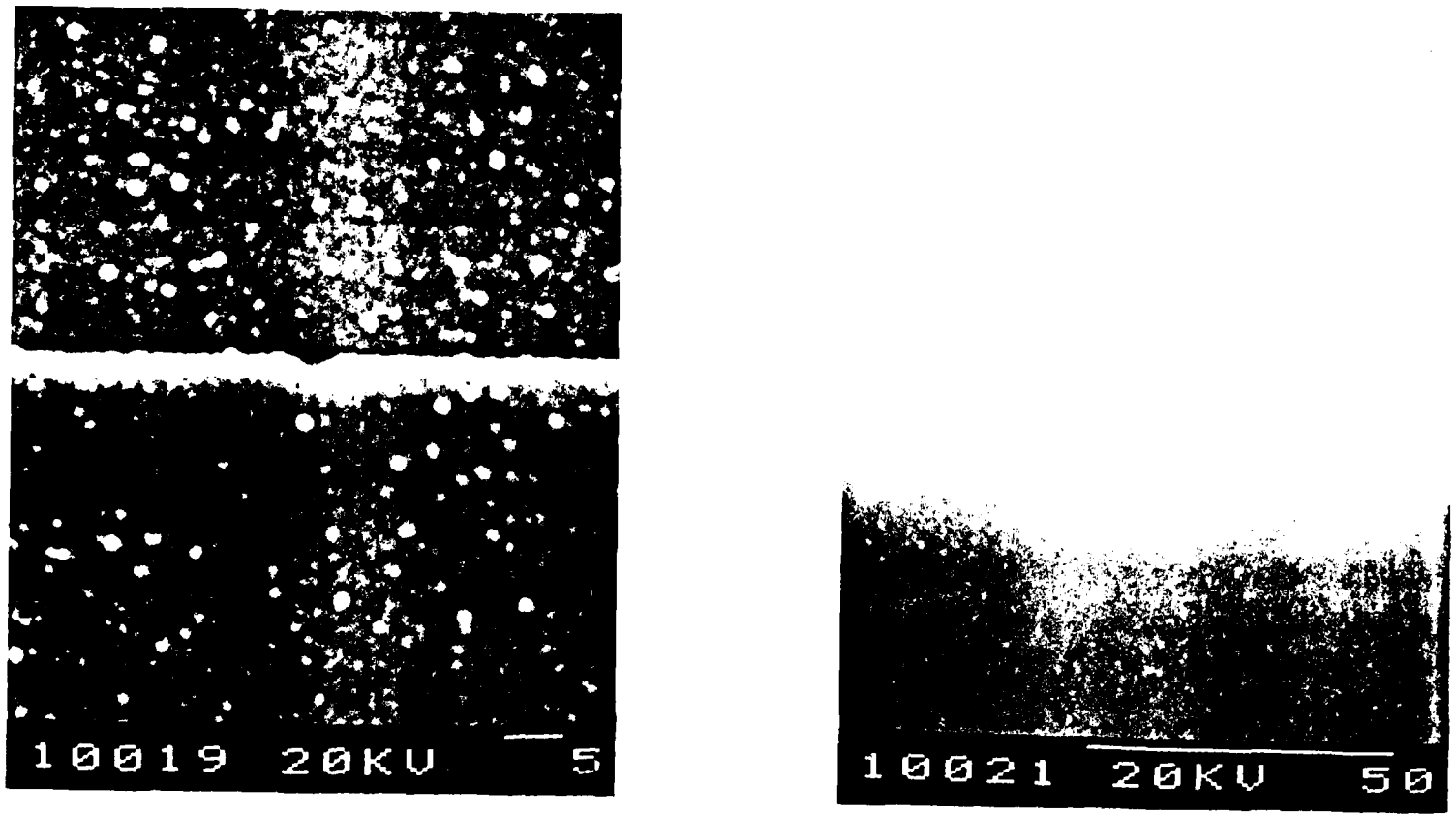
(b)

Figure 29. (a) Secondary and (b) EBIC image of diode 042.



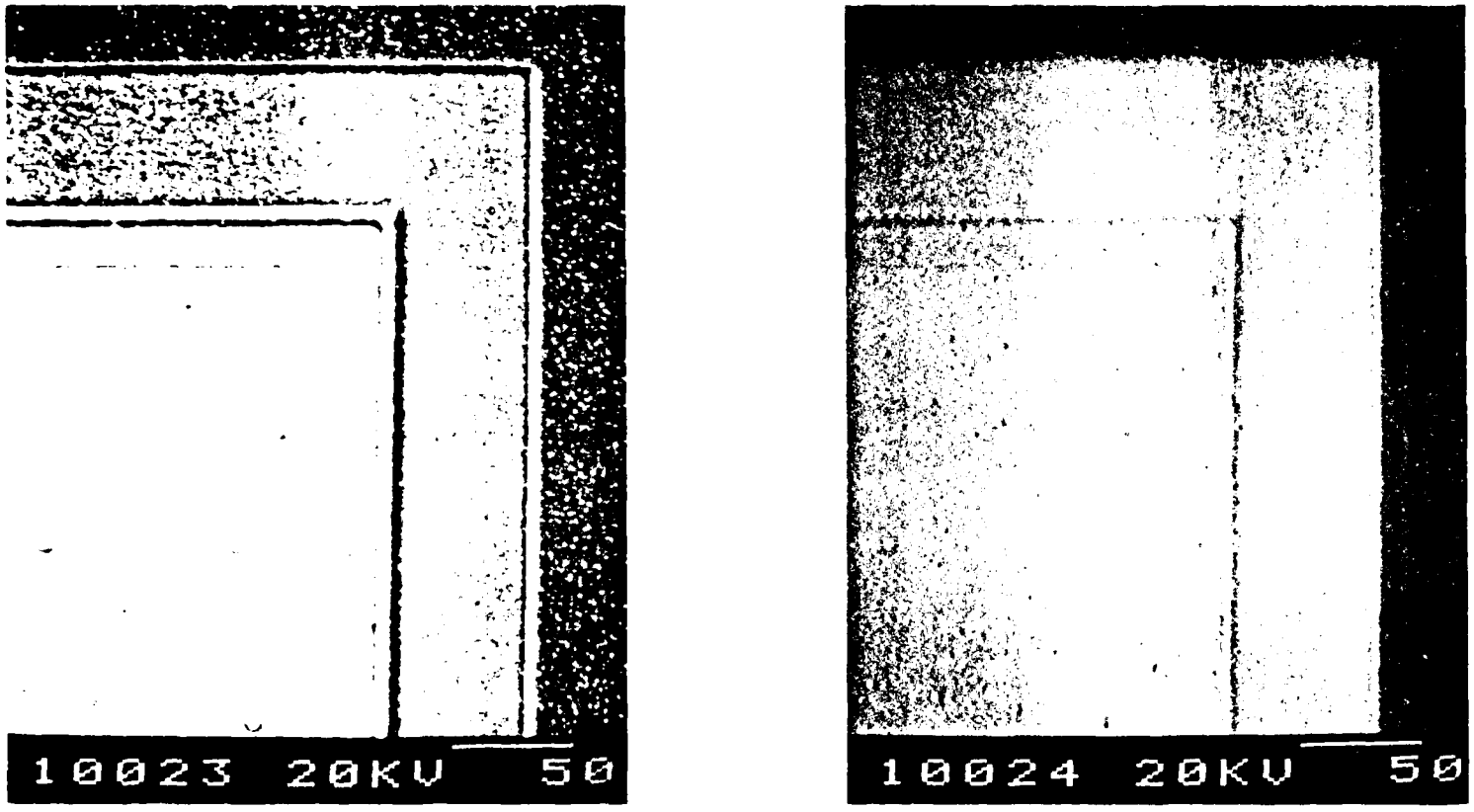
(a) (b)

Figure 30. (a) Secondary image of metallization pits on diode 046 at 4000x.
(b) Secondary image of diffusion edge defect on diode 046 at 1000x.



(a) (b)

Figure 31. (a) Secondary image of diffusion edge defect on diode 046 at 2000x.
(b) Intensified EBIC image of edge defect on diode 046 at 1000x.



(a) (b)

Figure 32. (a) Secondary image of diode 046. (b) EBIC image of diode 046.

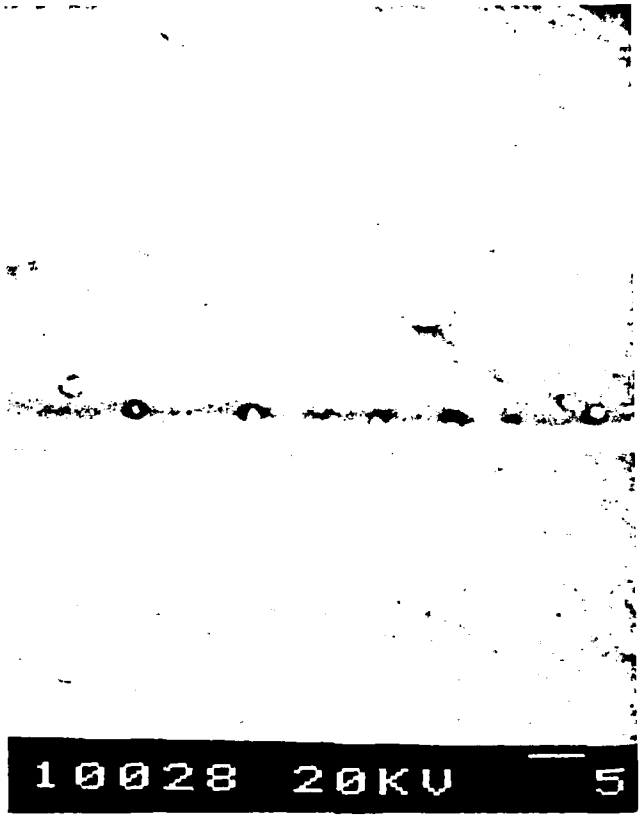
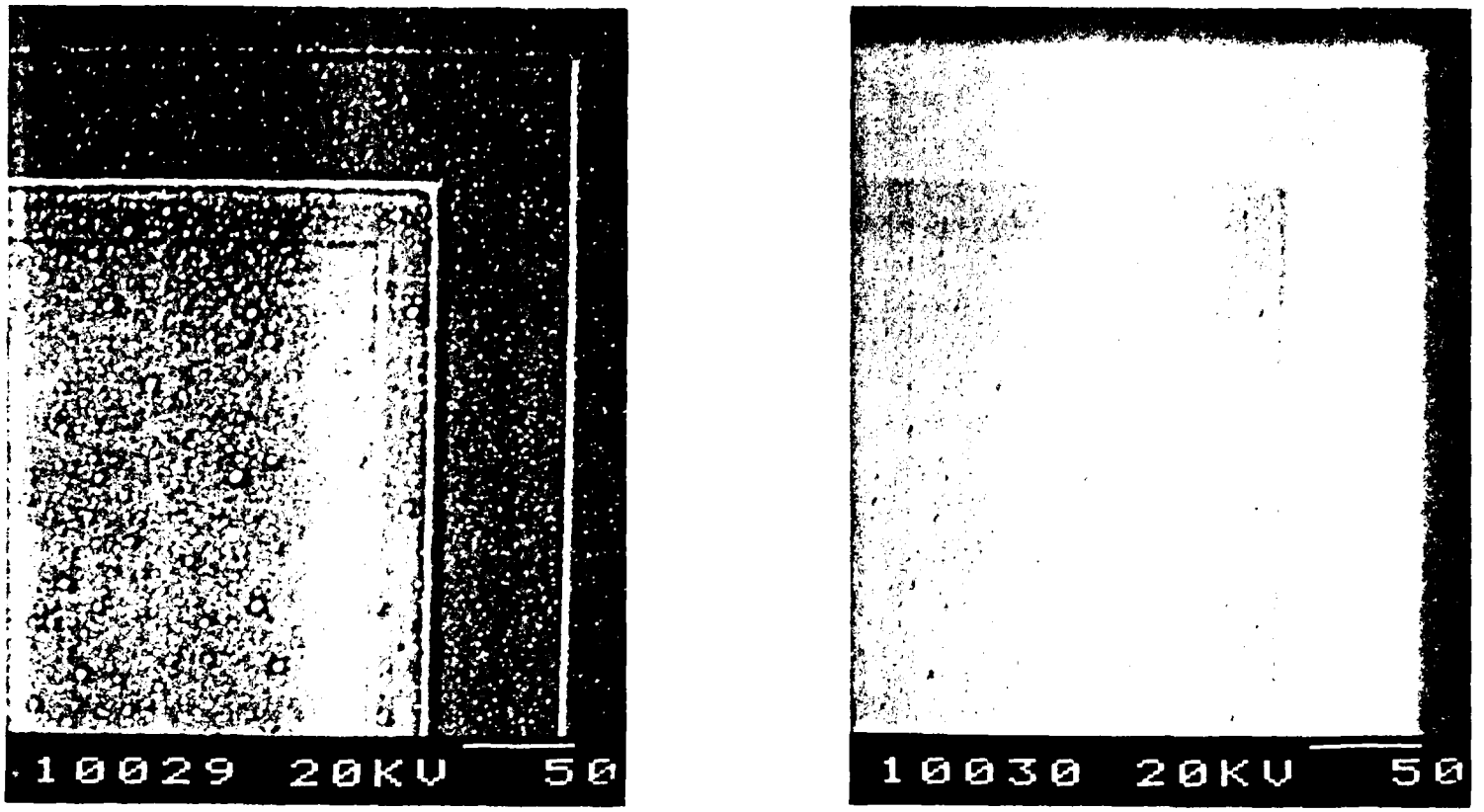


Figure 33. Secondary image of metallization pits on diode 081 at 2000x.



(a) (b)

Figure 34. (a) Secondary image of diode 081 at 400x. (b) The EBIC image of diode 081 at 400x.

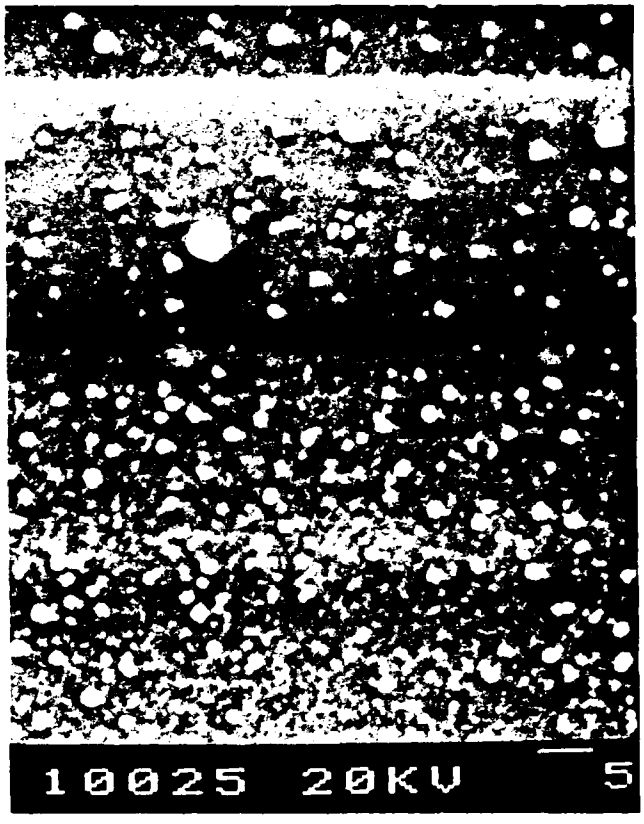
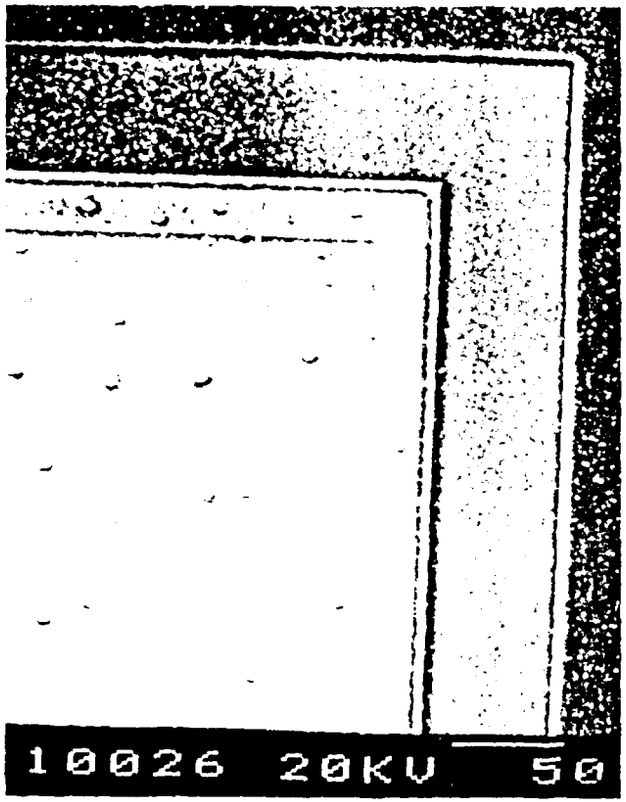
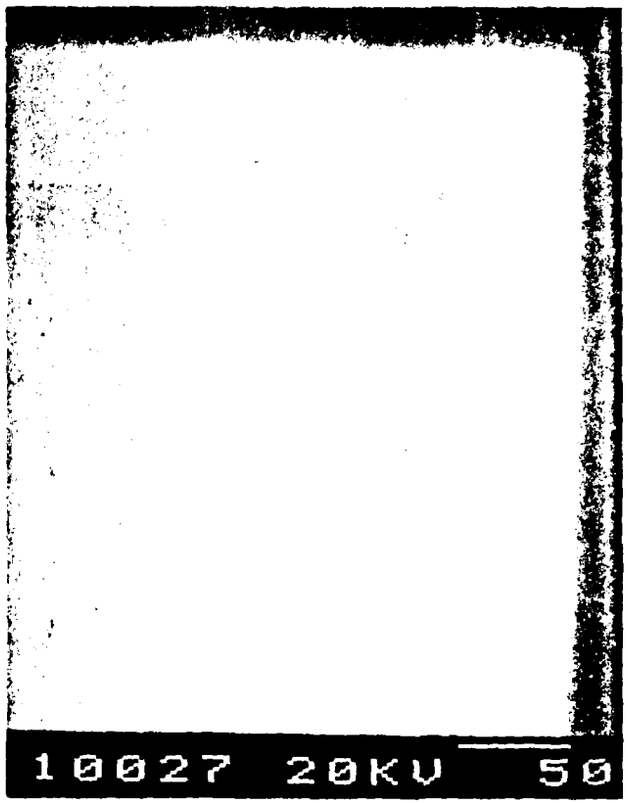


Figure 35. Secondary image of metallization pits on diode 086 at 2000x.



(a)



(b)

Figure 36. (a) Secondary image of diode 086 at 400x. (b) The EBIC image of diode 086 at 400x.

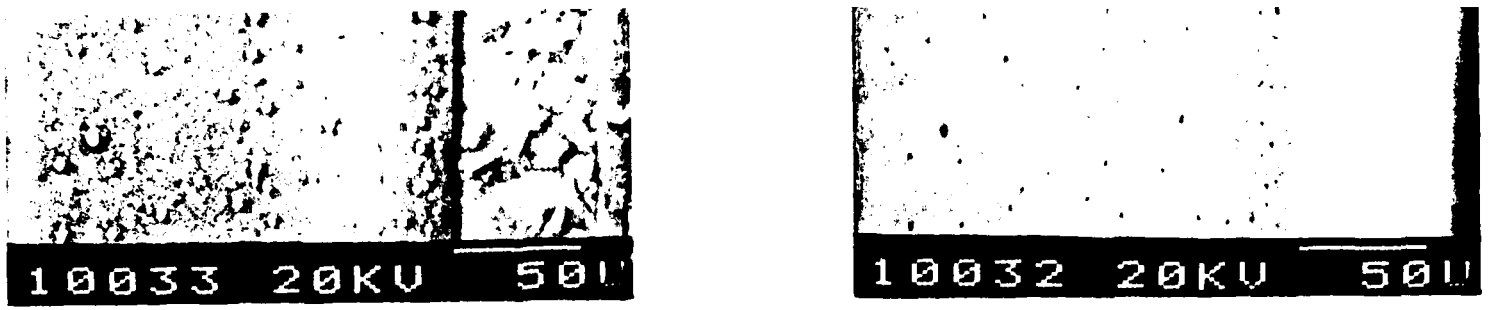
A question still remains as to what damage the pits represent. One possible explanation views the pits as oxide contaminants that become thermally activated when the device heats up due to an electrical overstress. The observed pits could also be explained as metallization migration into the semiconductor. This conjecture can be tested by etching the diode's passivation layer to determine whether the pits extend into the metallization or diffusions.

Devices 008 and 081 were etched with a solution of: 10 ml of ammonium flouride, 10 ml of ethylyne glycol, and 5 ml of hydroflouric acid. This etchant will strip away any glass on the devices' surface.

Device 008 required 20 min to etch the oxide layer away. Observation using secondary imaging showed no pits at the metallization periphery (Fig. 37). The EBIC mode observation showed no distinctive abnormalities from the earlier viewing.

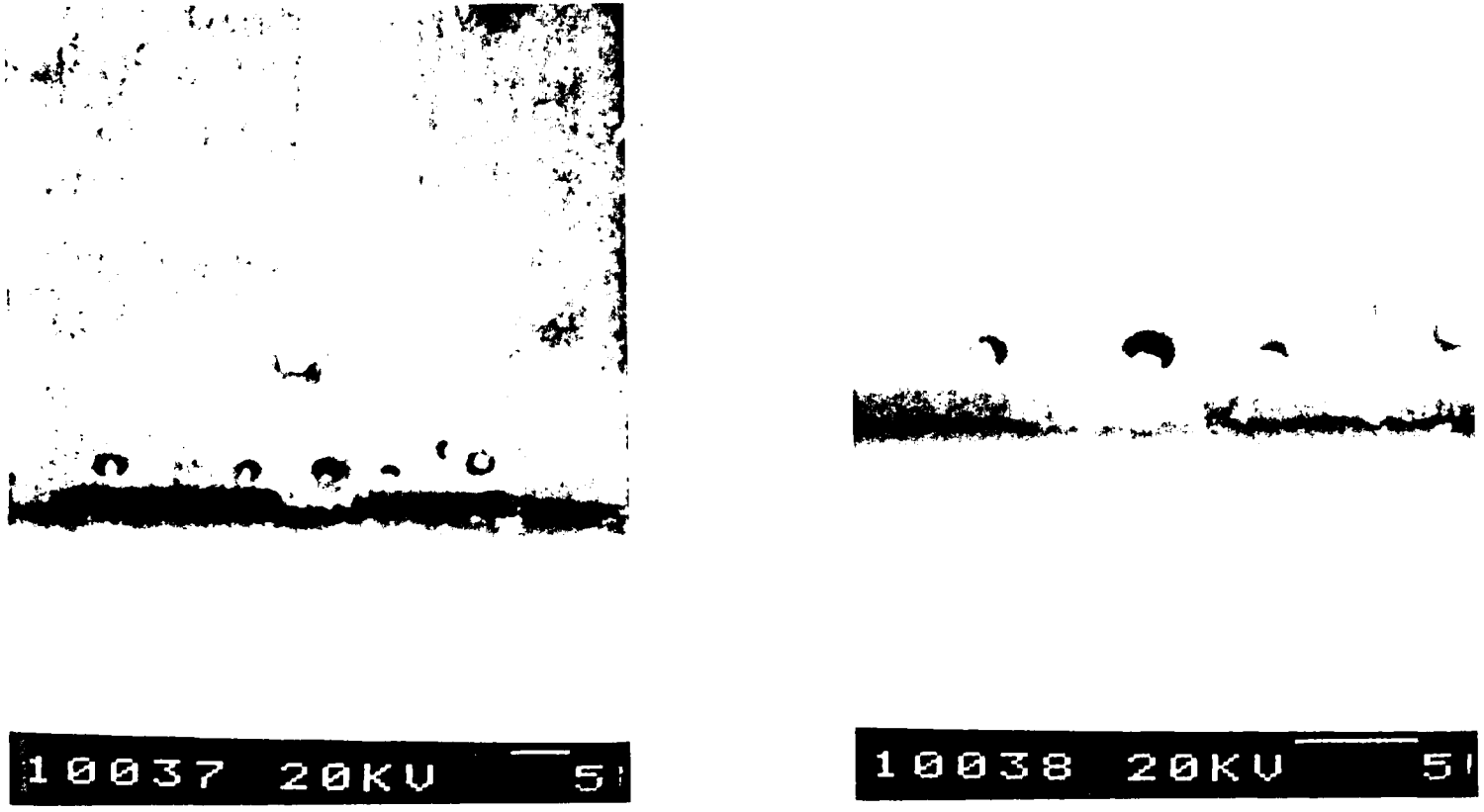
Device 081, after a 20 min etch, still had a lot of surface debris (Fig. 38). In addition, the EBIC mode image was strongly enhanced. After an additional 5 min etch, close examination using secondary imaging showed pits in the lower right-hand corner of the metallization (Fig. 39). These pits seem to correlate with the location of pits seen in Fig. 33 of device 081. No other pits were visible under close observation. The EBIC mode observation of these pits did not show any electrical irregularities.

The information derived from etching devices 008 and 081 show some of the pits are located on the metallization, while others are located in the passivation layer only. Pits that represent oxide contaminants being thermally activated would disappear with removal of the oxide layer as Fig. 39 seems to show. Metallic migration into the semiconductor diffusion would leave pits only in the metallization as the figures of device 081 would seem to indicate.



(a) (b)

Figure 37. (a) Secondary image of diode 008 after a 20 min etch of the surface at a magnification of 400x. (b) EBIC image of diode 008 at 400x.



(a) (b)

Figure 39. (a) Secondary image of metallization pits on diode 081 after a 25 min etching of the surface at 2000x. (b) Secondary image of diode 081 at a magnification of 4000x.

This exploration also raises the possibility that device damage may be occurring at the metal-semiconductor boundary. Such device damage could cause the formation of a rectifying Schottky barrier (Ref. 12) that would also explain the aberrant surface charging problems seen with many of the damaged diodes.

Further evidence for a rectifying Schottky barrier formation can be derived looking at the final I-V characteristics of the viewed devices shown in Appendix B.

IV. DISCUSSION OF POSTTEST DIODE I-V CHARACTERISTICS

The overall characteristics for the damaged diodes showed a distinct change toward a reduced current capacity. Forward bias measurements did show a reduced current capability that was not as severe as the decrease in reverse bias current capacity. Oftentimes the overall reverse characteristics showed no distinct onset of avalanche breakdown. This type of behavior obviously signals a change in the devices' electrically active regions. The types of changes necessary to arrive at these characteristics are difficult to specify. The SEM observations did not show many major depletion region failures. Even so, a major defect at one location would not account for the I-V characteristics found in Appendix B. If the entire depletion region had been damaged, large changes would be apparent in both the forward and reverse bias regimes. Yet, Appendix B's results show major change under only one type of device bias.

Finally, SEM observation did provide evidence that some kind of damage had occurred along the entire periphery of the devices' metallization. This evidence was consistent between predamaged devices and undamaged N+P+ diodes actually tested. The effect of this damage may also account for the undamaged N+P+ diodes' distinctive reverse bias characteristics in the area of the avalanche knee.

Referring to Appendix A, it is apparent that no two N+P+ diodes had the same initial reverse bias characteristics (discounting any large measuring apparatus error) especially in the area of the avalanche knee, while the N+P diodes shown in Appendix A show practically identical reverse bias characteristics.

The possible damage mechanisms involved appear to center around a processing-related parameter that is aggravated by device heating incurred by an electrical overstress. Activation by heating of semiconductor contaminants near the

metallization would result in a diffusion of impurity near the electrode, creating surface states and, hence, a nonohmic boundary between metal and semiconductor. A metal semiconductor boundary, known as a Schottky barrier (Ref. 13) is a common feature of most semiconductor devices. This type of boundary is created by evaporating a metal contact onto a prepared silicon surface to provide an ohmic contact for the device (an ohmic contact is one that will not provide a significant parasitic impedence and drastically change the equilibrium-carrier densities in the base semiconductor material). The contact formed on a device is usually ohmic if the semiconductor doping level is $> 10^{15}$ carriers/cm^3. Such a high doping level in conjunction with a thin oxide layer (that is an unavoidable result of the metallic lay-down process) assures tunneling of carriers across the barrier. Although this oxide layer aids in creating the Schottky barrier, it is also susceptible to permanent electrical changes via impurity diffusion and electromigration of metal, creating surface states in the barrier region.

The conduction process in a rectifing Schottky barrier is by thermonic emission or thermal emmision of carriers (Ref. 13). This type of current flow is carried by majority carriers (electrons in this case) resulting in a saturation current for a rectifying Schottky barrier that is higher than a minority carrier dominated PN junction (Ref. 14). These characteristics give a rectifying Schottky barrier an I-V character similar to that of a PN junction, but with distinct differences due to a Schottky barrier's larger saturation current. As Fig. 41 demonstrates, Schottky diodes possess a lower cut-in voltage and a reverse current that does not saturate and produces a soft breakdown characteristic.

These characteristics seem prominent in the Appendix B I-V curves for damaged and even some undamaged N+P+ diodes. Therefore, it can be inferred

that lowered current levels for damaged and undamaged N+P+ devices appear to be due to the formation of a rectifying Schottky barrier at the insulator interface in series with the PN junction. Direct evidence for this phenomenon is provided by SEM observation, and I-V characteristics measured for the devices. Further evidence was gained when two of the devices' passivation layers were removed and the surfaces examined directly, revealing metallization damage. This evidence also rules out the possibility that the devices' PN junction was bypassed so that only the Schottky barrier is active. The EBIC images show no active surface paths, except the bulk path through the PN junction.

V. DISCUSSION OF DEVICE DAMAGE MECHANISMS

There are many possible damage mechanisms that can be inflicted on a simple diode. Of paramount importance is the damage mechanism known as SB*. This mechanism can occur at the surface or in the bulk of a device (Ref. 16) changing the devices' electrical characteristics drastically. When SB occurs, the remnants of a molten channel should be visible under SEM secondary or EBIC imaging.

Other possible failure mechanisms center around metal-semiconductor interface damage (electromigration or impurity migration) or other bulk semiconductor damage (i.e., impurity diffusion, dislocation growth, etc.). To narrow down the possible damage mechanisms it is helpful to look at how the damage was incurred.

None of the devices tested experienced any systematic pulse testing. This was decided early in this effort because of the inherent unknowns (Ref. 9) in stressing devices with step-stress. Using other types of waveforms for stressing brings the same inherent unknowns to any posttest analysis. Therefore, it was decided that no systematic overstress testing would be accomplished.

In lieu of systematic testing, it was decided that the high steady-state voltages and currents applied to the devices during voltage contrast and EBIC imaging would be sufficient to stress the devices to damage.

Since examination of these devices did not portray extensive SB, only metal-semiconductor interface damage remains as a plausible explanation for the Appendix B I-V characteristics.

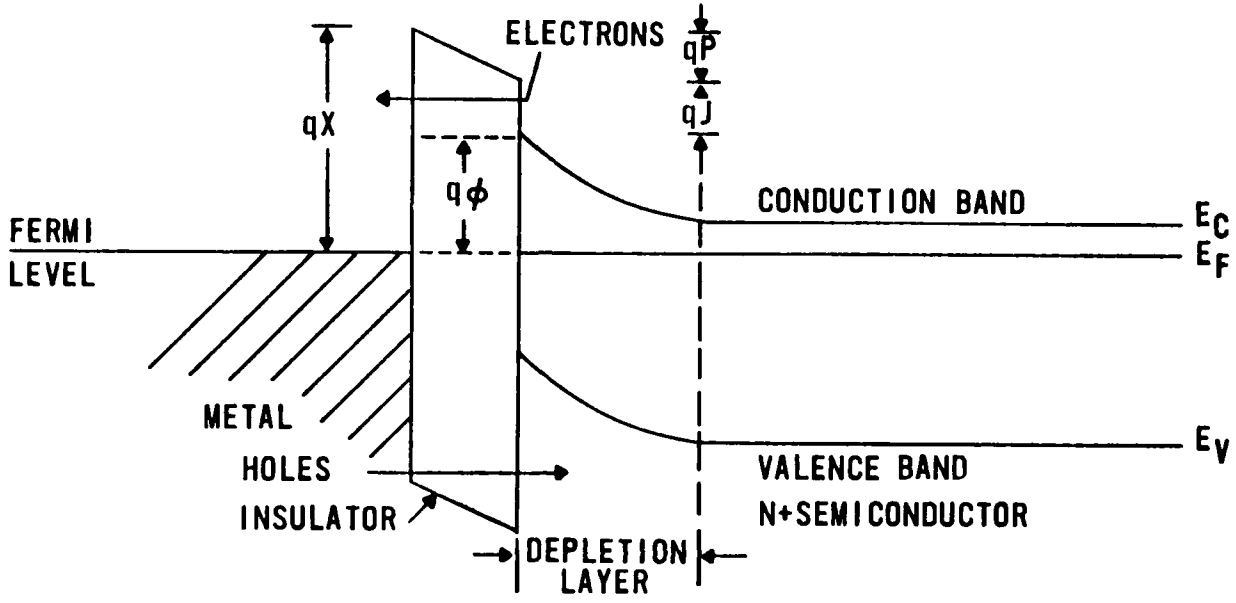
*Second Breakdown (SB) is the term adopted by the International Electrotechnical Commission, IEC Document 47 (Secretariat), 86, 1963.

The extensive amount of damage seen on the metallization periphery clearly implies possible damage to the electrode semiconductor interface. Such damage would induce surface states on the metal and semiconductor surface creating an electrical field in the intervening insulator. To understand why this is detrimental requires a close examination of the physics of Schottky barriers.

SCHOTTKY BARRIERS

When a metal and semiconductor surface are joined together to form a contact, the Fermi level (or chemical potential) of both materials will come to thermal equilibrium and coincide in energy (Fig. 40). This is accomplished in the same manner as a PN junction; i.e., contact is made and carriers pass between the two materials until a potential opposite and equal to the potential difference between the P and N sides is established. The potential differences between doped semiconductors is easily determined by the impurity levels of the two neutral semiconductors prior to contact. Graphically, this built-in potential is measured from the top of the conduction band on the N-side of the material to the top of the conduction band on the P-side (Fig. 42). Carriers diffusing across this junction must traverse this potential to contribute to current generation. The addition of an externally impressed electric field across the junction can then aid or impair carrier movement through the potential.

The barrier potential for a metal-semiconductor contact is determined by the metal's work function and the semiconductor's electron affinity. The difference between these two quantities defines the built-in potential, or barrier, that the carriers must traverse during current flow through the contact (Fig. 40). Normally, the interfacial oxide layer produced by the metallization lay-down is quite thin. If the metal's work function is lower



qX = METAL WORK FUNCTION

qP = POTENTIAL ACROSS OXIDE LAYER

qJ = SEMICONDUCTOR ELECTRON AFFINITY

qφ = BARRIER HEIGHT OF METAL-INSULATOR-SEMICONDUCTOR BARRIER

Figure 40. Energy band structure of a metal-insulator-semiconductor structure (ignoring the small image force lowering of the potential). In this diagram the metal's work function is larger than the semiconductor's electron affinity.

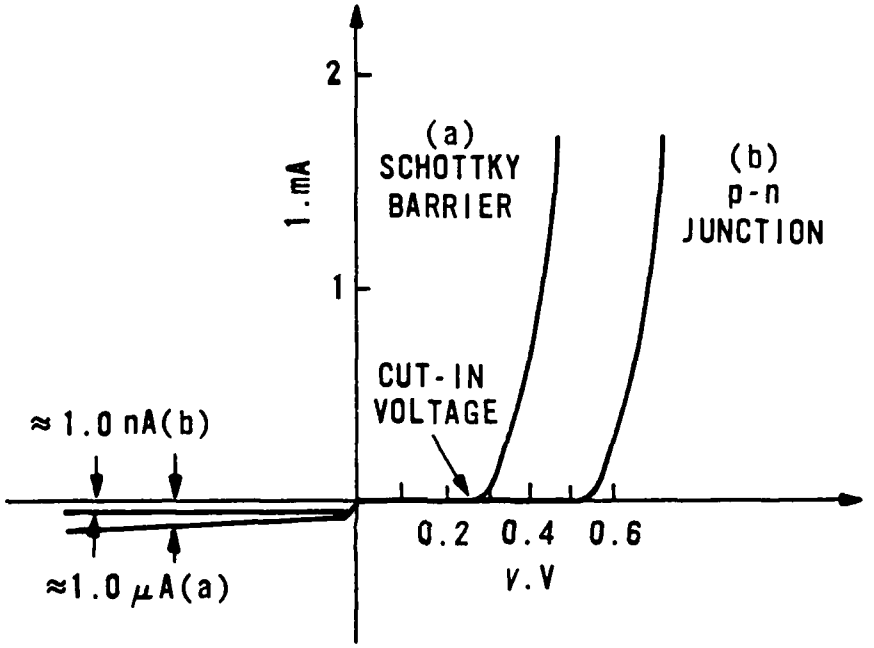


Figure 41. Current-voltage characteristics of a PN junction and a Schottky-barrier diode (after Ref. 15).

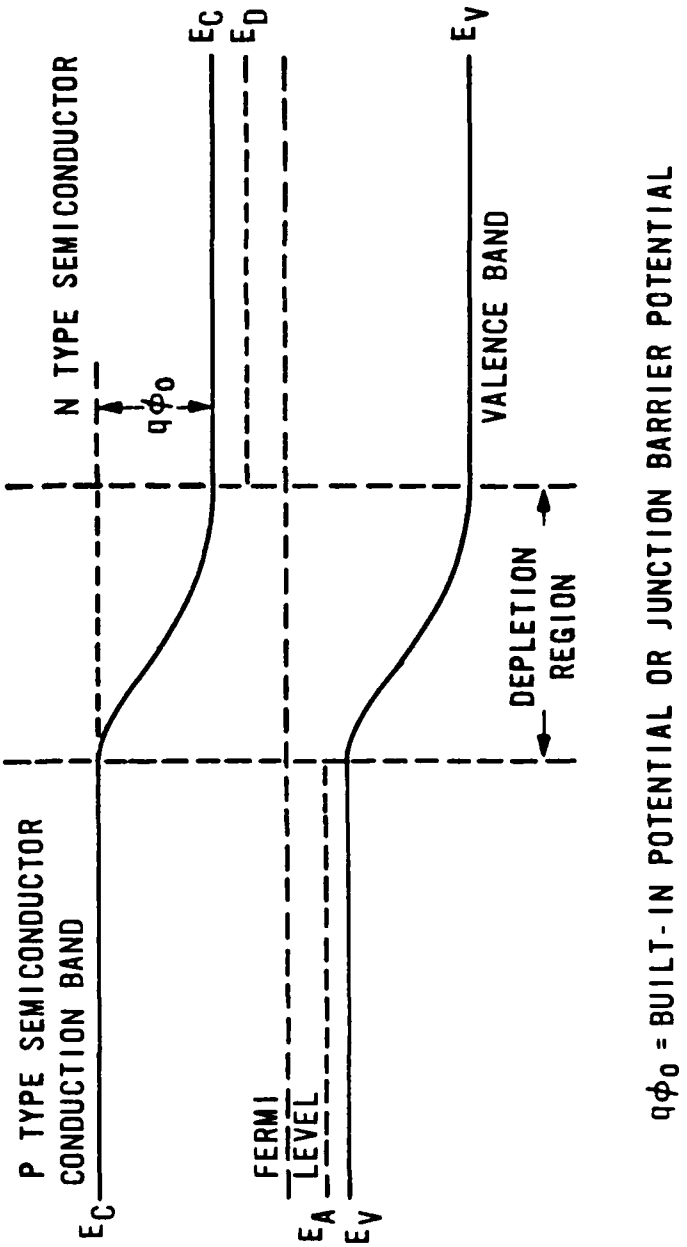


Figure 42. Energy band diagram of a PN junction.

than the semiconductor's electron affinity, an accumulation of electrons occurs on the barrier (Fig. 43) which in combination with the abrupt barrier potential, represents a situation where Boltzmann statistics do not apply within a few Debye lengths of interface (Ref. 18) preventing PN junction like carrier diffusion. Yet, this type of situation provides conditions for the main mode of carrier transport in this area--tunneling (Ref. 19). Therefore, carrier transport across this junction is dominated by majority carrier (electrons for Fig. 43) movement and subsequently, ohmic behavior.

This type of contact is used extensively in industry to make contacts to microscopic semiconductor devices. To assure the tunneling action of the contact, the semiconductor side is normally doped to a high level ($> 10^{19}$ carriers/cm^3). This brings the conduction band close to the Fermi level so that electrons can easily tunnel through the barrier (Fig. 43).

The use of Schottky barriers is altered drastically when surface states occur on the metal or semiconductor side of the contact.

Defects (such as dislocations, dangling bonds or contaminants) located on a surface are by definition thermodynamically unstable, due to the local increase in crystal disorder. When defects are placed in a thermodynamically stable medium, the Fermi level adjusts to provide local thermodynamic equilibrium. Thus, if the number of surface states is large, the energy of the Fermi level will be dependent on the number of surface states, not the impurity level of the bulk material. On the other hand, if the number of surface states is small, the Fermi level will be constant throughout the material. The addition of these defects on a surface also lower the semiconductor's electron affinity.

When two materials are brought into metallurgic contact where one material contains a number of surface states occupied up to and above the Fermi energy, a drop of the Fermi level (equal to the barrier potential) in the defective

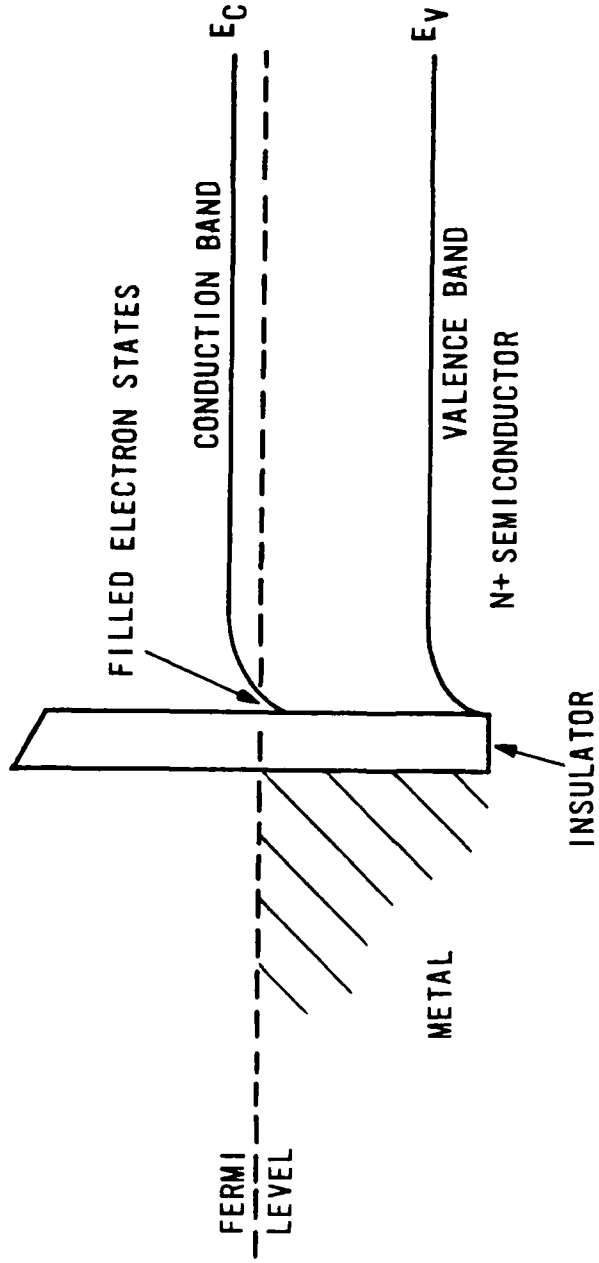


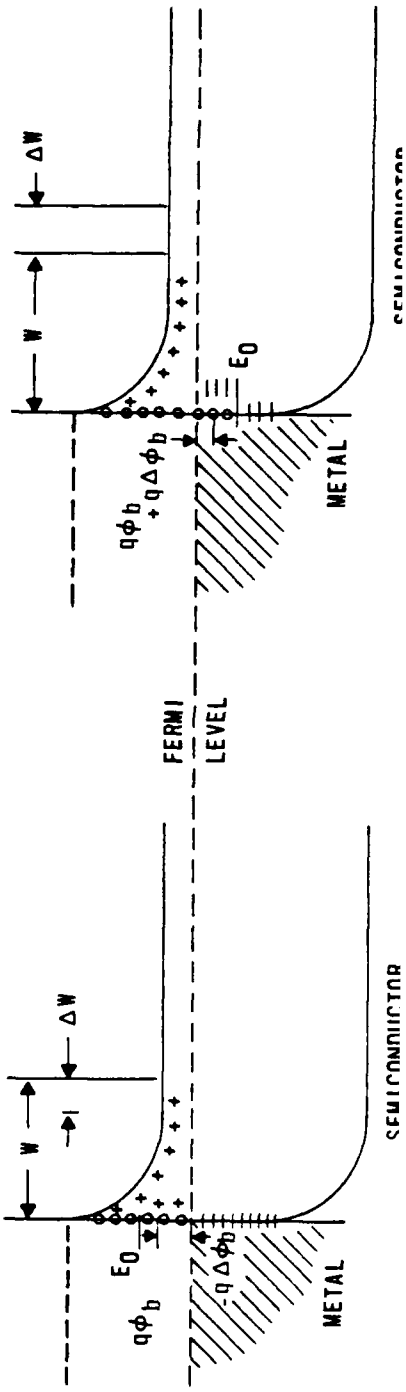
Figure 43. Diagram of a metal-insulator-semiconductor structure with a large doping level on the N-side of the structure. Applying a bias to the structure still alows tunneling across the insulator to the semiconductor's conduction band. This type of contact requires the metal work function to be smaller than the semiconductor's electron affinity.

ield in the interfacial region, due to
states (Fig. 44). If the number of
ced depletion region of the barrier
e exposed surface charge, not the bulk
n alter the potential drastically
e, surface states, not the material
rrier potential.

r experiences an increase in the
ential is lowered, (i.e., the
e metal's work function) allowing an
ditional barrier lowering voltage
ransport mechanism changes from
ffusion (Fig. 40). The result is a
ing contact.

appears that prolonged electrical
e states in the metal-semiconductor
and creating a rectifying Schottky
tate creation appears to be impurity
metal toward the semiconductor.
tress may already possess a sizable
uble diffusion process by which these
erstress increased the surface state
racteristics.

e of initial surface state contami-
degraded the metal-semiconductor
N+P+ diode degradation.



Since the PN junction in both sets of devices would be in series with the rectifying Schottky barrier, the overall current capacity of the devices would be controlled by the Schottky barriers' current capacity at high voltages in the reverse direction. Avalanche breakdown, under this type of situation would require much higher voltages because of the voltage division occurring between the two devices. Forward characteristics appear to reflect a lower cut-in voltage and current than before damage.

Pre- and posttest analyses of the diodes seems to support these conjectures. Indeed, a final pillar of support would be an analytical analysis of lapped diode sections. There are a number of unknowns this nondestructive research effort could not obtain, such as the density of surface states created or impurity changes in the diode bulk. Without this information, any analytical treatment pursued would soon falter.

VI. CONCLUSIONS AND FUTURE WORK

This research effort has endeavored to develop SEM techniques in EBIC mode to be used in the nondestructive analysis of semiconductor devices.

To demonstrate this analytic tool, a set of N+P and N+P+ diodes were constructed to provide an example of the diagnostic capabilities of SEM EBIC mode imaging.

The EBIC mode imaging was compared to voltage contrast imaging for the devices under test. This comparison demonstrated that actual imaging, though simple in theory, is quite diffucult to achieve in practice. A great deal of experimentation finally resulted in the achievement of voltage contrast and EBIC mode imaging for the AFWL's SEM. A set of basic guidelines to be followed in using EBIC mode imaging were derived that will allow its implementation to other types of SEM more simple. The guidelines are:

a. All SEM column apertures must be open.

b. The SEM beam current must be adjusted against decreased resolution caused by opening all SEM column apertures.

c. A fast electrometer (that is battery operated) will provide the best visual resolution.

Application of these guidelines resulted in the first recorded EBIC mode images taken at the AFWL Material Sciences Laboratory.

The EBIC mode and secondary electron images were taken for 13 devices. Some of the devices had been damaged during attempts to perform voltage contrast and EBIC mode imaging and were examined after successful achievement of imaging.

The results of these examinations demonstrated that the main damage mode for these diodes was the formation of a rectifying Schottky barrier at the metal-semiconductor contact of the diodes. Little direct evidence was found to support failure due to SB.

This evidence also appears to explain the initial I-V characteristics for the N+P+ diodes. These diodes' double diffusion construction may have resulted in a contaminated surface prior to metallization lay down, creating a rectifying Schottky barrier that degraded with electrical overstress.

Future work in this area should concentrate on applying EBIC to devices experiencing steady electrical bias. This type of experiment would require a battery operated electrometer to isolate the device measurements from the SEM.

Additionally, efforts should be made toward using variable AC current bias on devices. This type of measurement would greatly increase the amount of information derived from semiconductor devices.

REFERENCES

1. Seidel, T.E., Haszko, S.E., and Maher, D.M., "Electron-Beam-Induced Current and TEM Studies of Stacking Faults Formed by the Oxidation of Boron-Implanted Silicon". J. of Appl. Phys., Vol. 48, No. 12, Dec. 1977, P. 5038.

2. Ashburn, P., et al, "The Use of the Electron-Beam-Induced Current Mode of the SEM for Observing Emitter/Collector Pipes in Bipolar Transistors". J. of Appl. Phys., Vol. 50, No. 5, May 1979, p. 3472.

3. Spivak, G.V. et al, "Scanning Electron Microscopy of Electrical Inhomogeneities in Semiconductors". Sov. Phys. Semicond. Vol. 14, No. 10, Oct. 1980, p. 1151.

4. Bull, C.J. et al, "A Study of Diffused Bipolar Transistors by Electron Microscopy", Solid State Elec., Vol. 23, 1980, p. 953.

5. Nicolas, D. P., "Role of SEM in Microcircuit Failure Analysis", Proc of the 7th Annual Scanning Electron Microscope Symposium , April 8-11, 1974, p. 956.

6. Yang, E.S., Fundamentals of Semiconductor Devices, McGraw-Hill Book Co., St. Louis, Missouri. 1978, p. 118.

7. Crosthwait, D. L. and Ivy, F.P., "Voltage Contrast Methods of Semiconductor Device Failure Analysis", Proc of the 7th Annual Scanning Electron Microscope Symposium, April 8-11, 1974, p. 936.

8. Schick, J.D., "Failure Analysis of Integrated Circuits with SEM-Beam-Induced Currents", IBID, p. 950.

9. Ghandi, S.K., Semiconductor Power Devices, John Wiley and Sons, New York, New York. 1977, p. 290.

10. Cornu, J., "Field Distribution Near the Surface of Beveled P-N Junctions in High Voltage Devices", IEEE Trans. on Elect. Dev., Vol. ED-20, No. 4, April 1973 p. 347.

11. English, A.C., "Mesoplasmas and Second Breakdown in Silicon Junctions", S. S. Elect., Vol. 6, 1963, p. 511.

12. English, A.C., "Physical Investigation of the Mesoplasma in Silicon", IEEE Trans. on Elect. Dev., Vol. ED-13, No. 8/9, Aug/Sept, 1966, p. 682.

13. Yang, E.S., Ref. 6 above p. 134.

14. Yang, E.S., IBID p. 134-136.

15. Yang, E.S., IBID P. 136.

16. Snyder, M.E., The Physics of Second Breakdown, AFWL-TR-83-22, Air Force Weapons Laboratory, Kirtland Air Force Base, NM, Nov. 1983. p. 16.

17. Yee, J.H., et al, "Theoretical Modeling of EMP Effects in Semiconductor Function Devices," AFWL-TR-82-91, Air Force Weapons Laboratory, Kirtland Air Force Base, NM, Feb. 1983. p. 37.

18. Moll, J.L., Physics of Semiconductors, McGraw-Hill Book Comp., San Francisco Calif. 1964, p. 135.

19. Yang, E.S., Ref. 6 above p. 137.

20. Yang, E.S., IBID, p. 128.

APPENDIX A

PRETEST DIODE CURRENT VOLTAGE CHARACTERISTICS

This appendix contains the pretest I-V curves for devices: 008, 009, 011, 034, 042, 046, 081, and 086 in the forward and reverse bias regimes (Figs. A1 through A9).

Prior I-V curves for devices 001, 018, 097, and 100 were not recorded. Pretests determined the I-V curve differences between diodes of the same family (N+P+ or N+P) were relatively small, and it was not deemed necessary to record all the curves. The curves shown in this appendix consistently reflect general characteristics of each family of diodes.

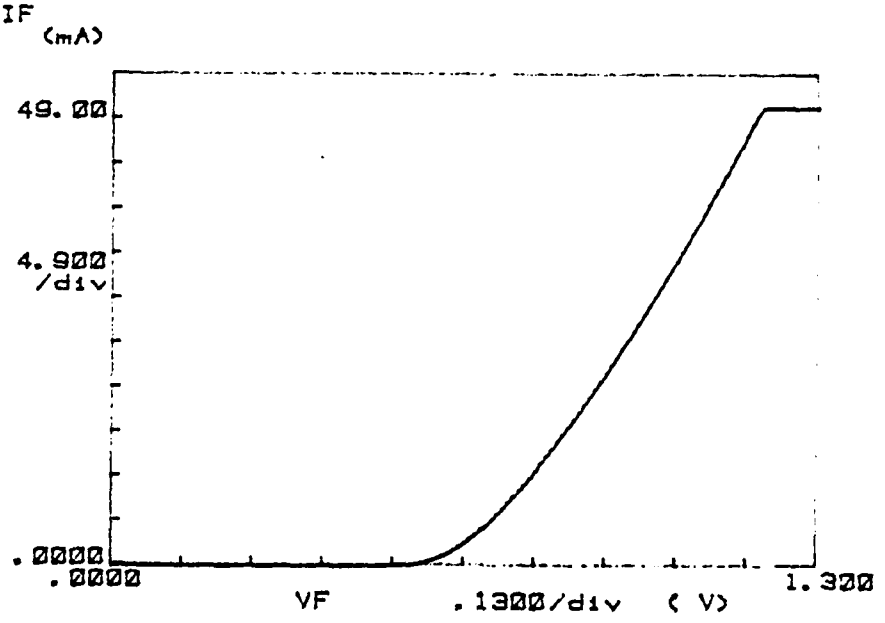
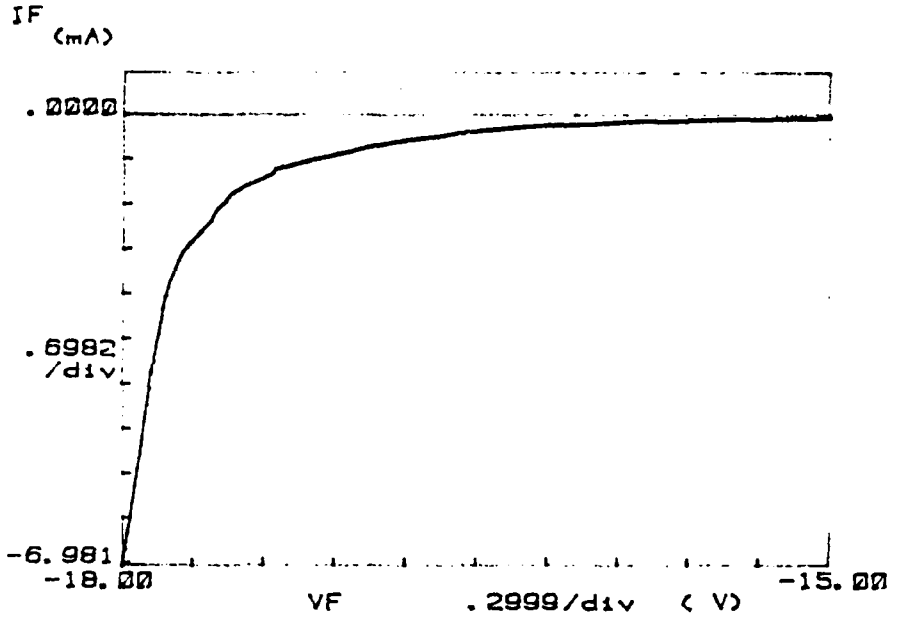
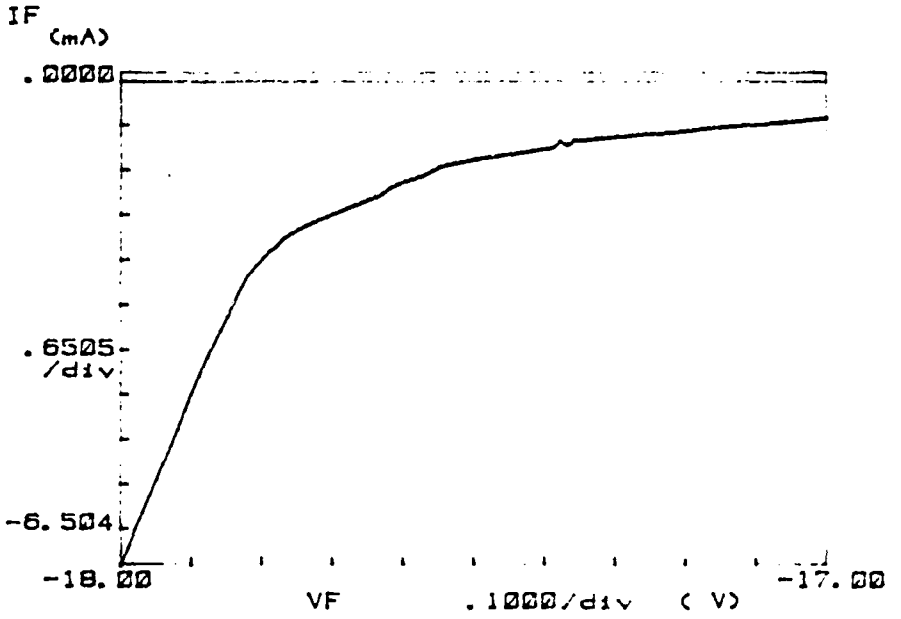


Figure A1. Diode 008 before experiment under forward bias.

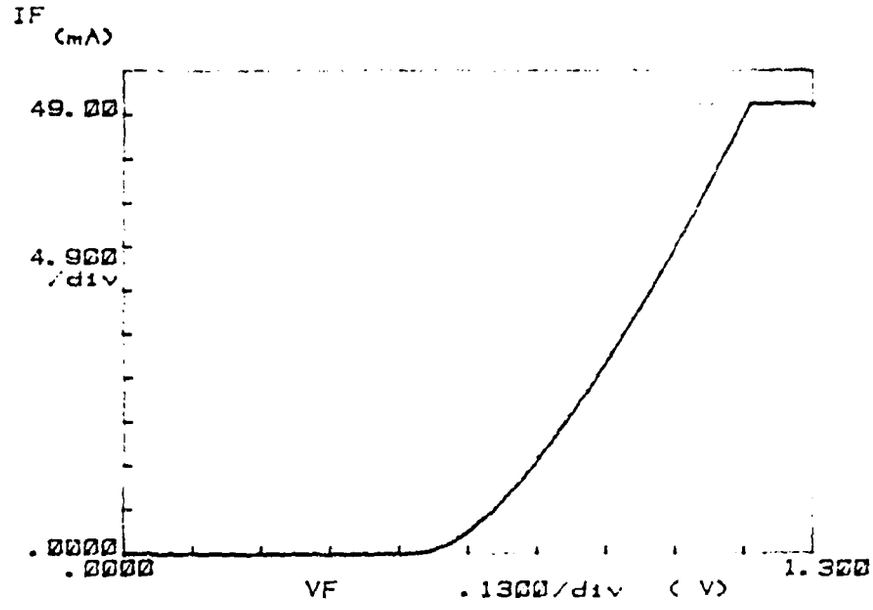


(a) Overall reverse region

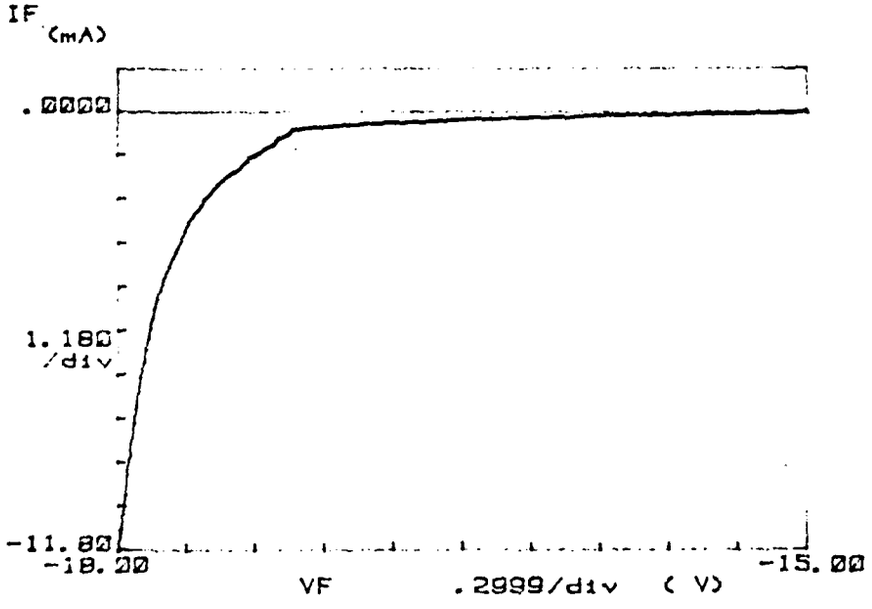


(b) Close-up of the avalanche knee

Figure A2. Diode 008 reverse bias characteristics before testing.

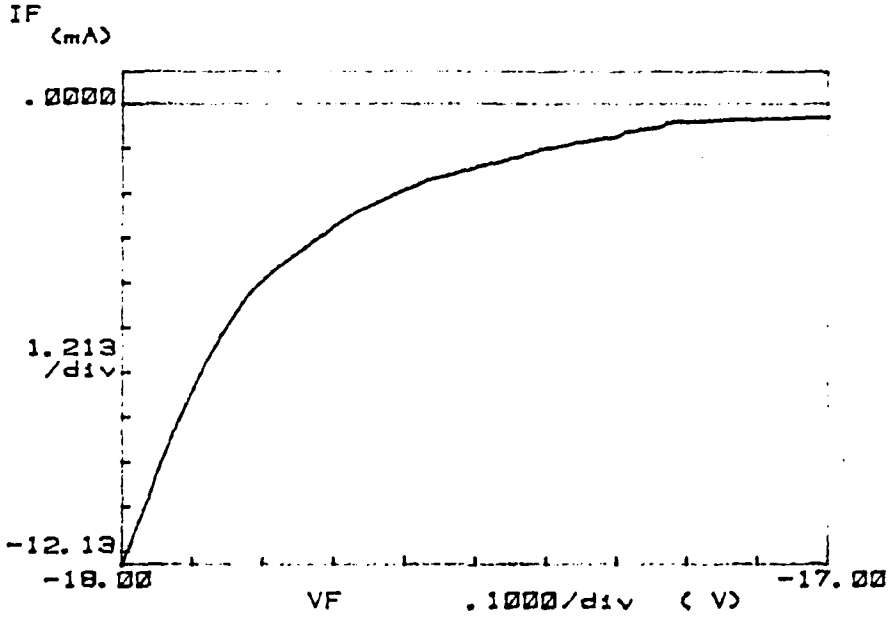


(a) Forward region



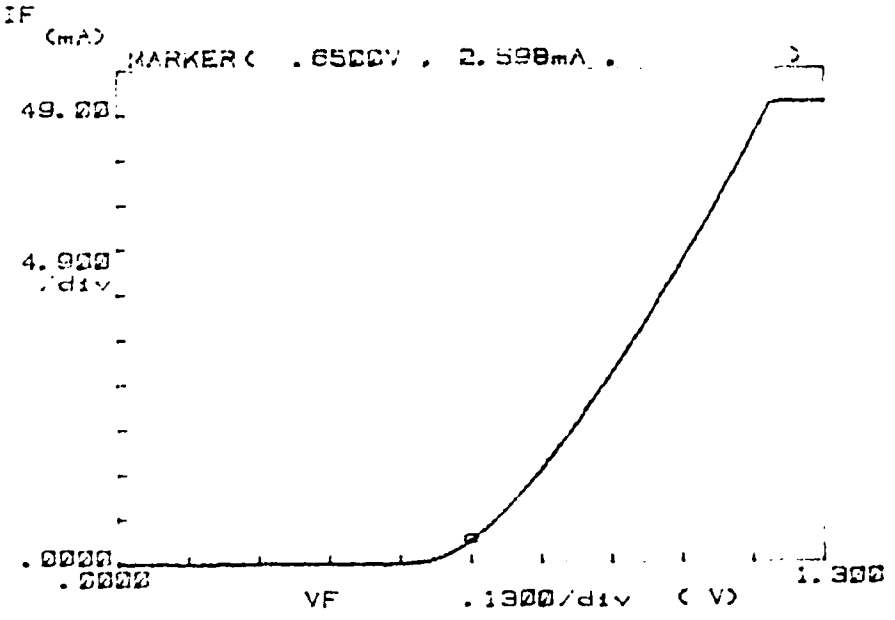
(b) Overall reverse bias region

Figure A3. Diode 009 pretest I-V characteristics.

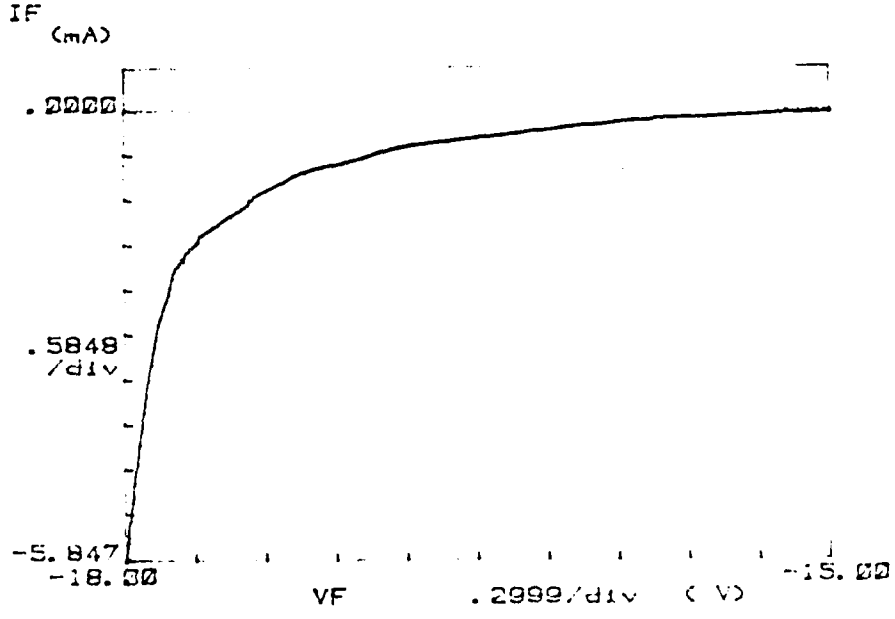


(c) Close-up of the avalanche knee

Figure A3. Concluded.

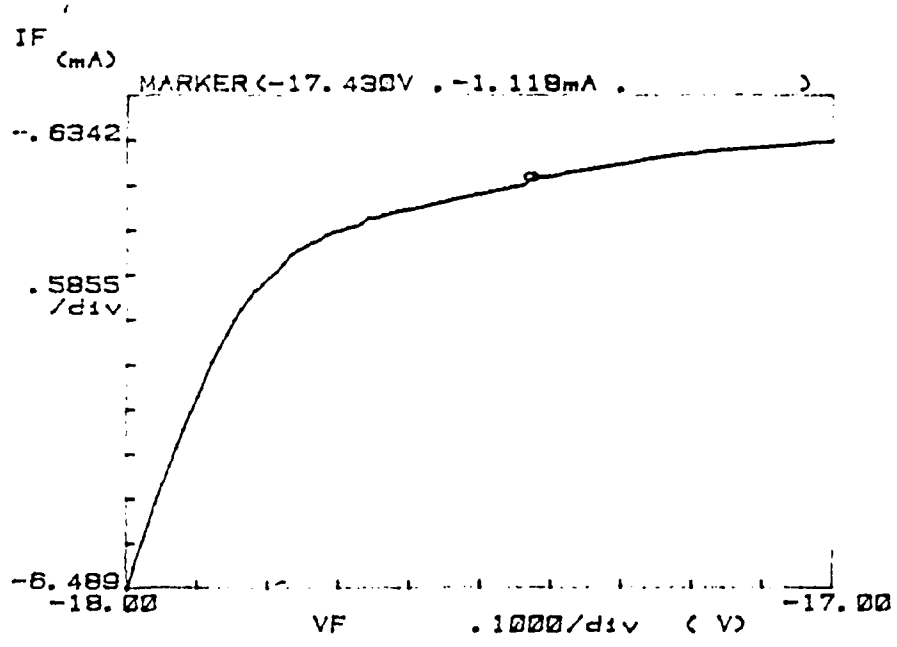


(a) Forward region



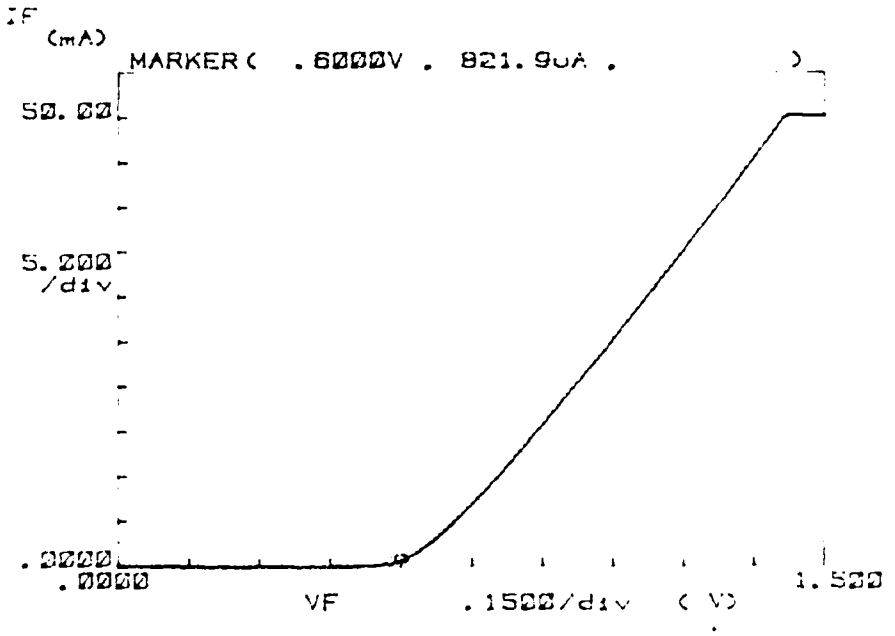
(b) Overall reverse region

Figure A4. Diode 011 pretest I-V characteristics.

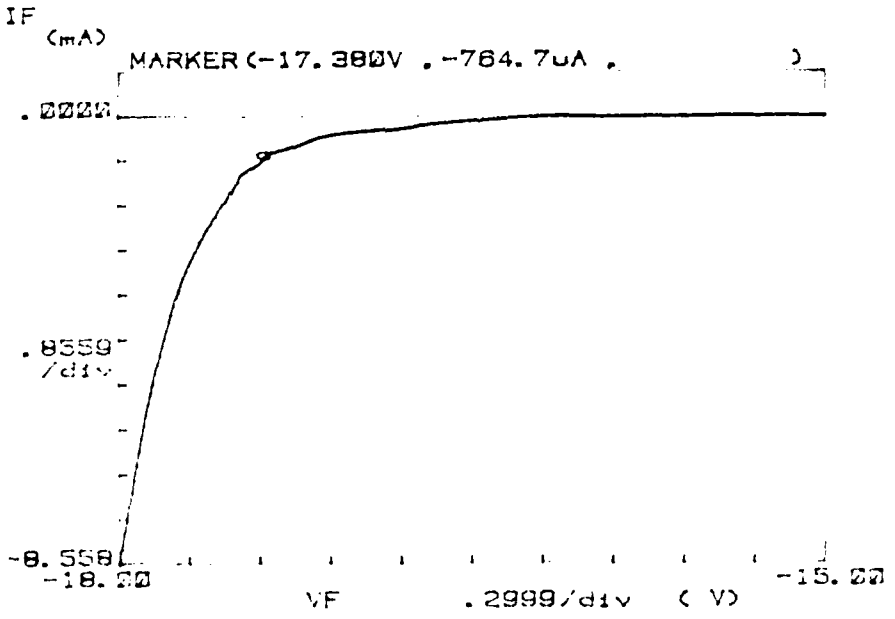


(c) Close-up of avalanche knee

Figure A4. Concluded.



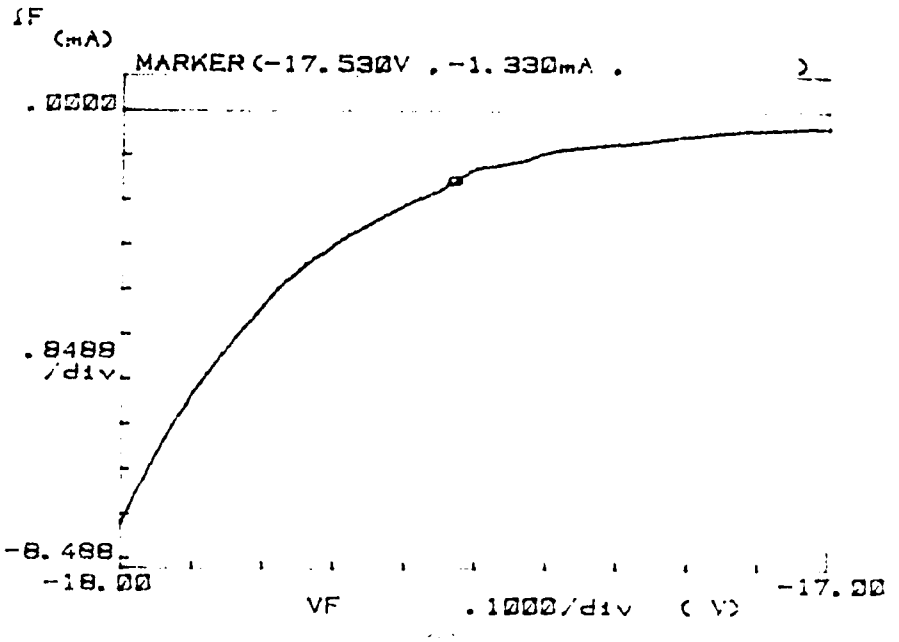
(a) Forward region



(b) Overall reverse region

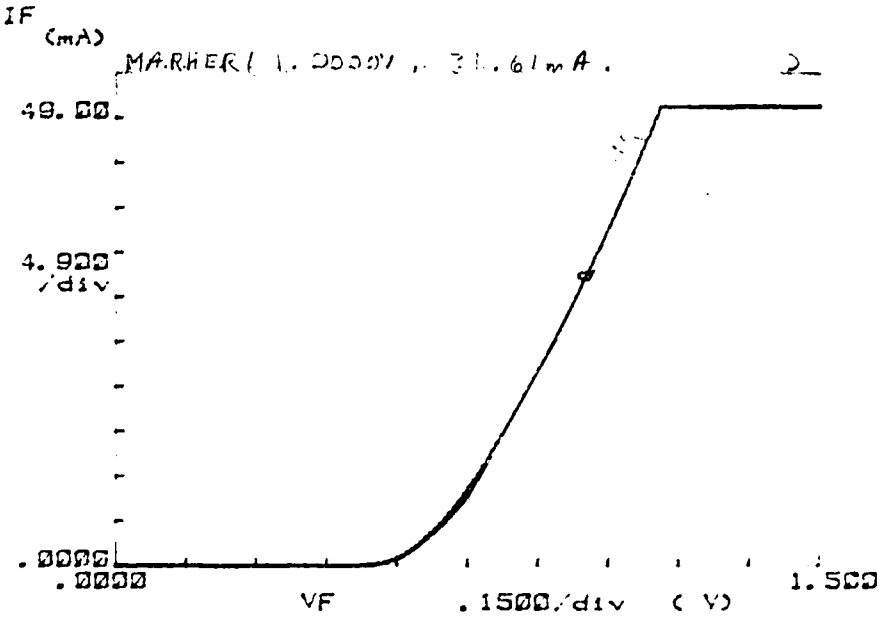
Figure A5. Diode 034 pretest I-V characteristics. Diode 034 is the experiment control diode.

The N+
nation. Ex
interface

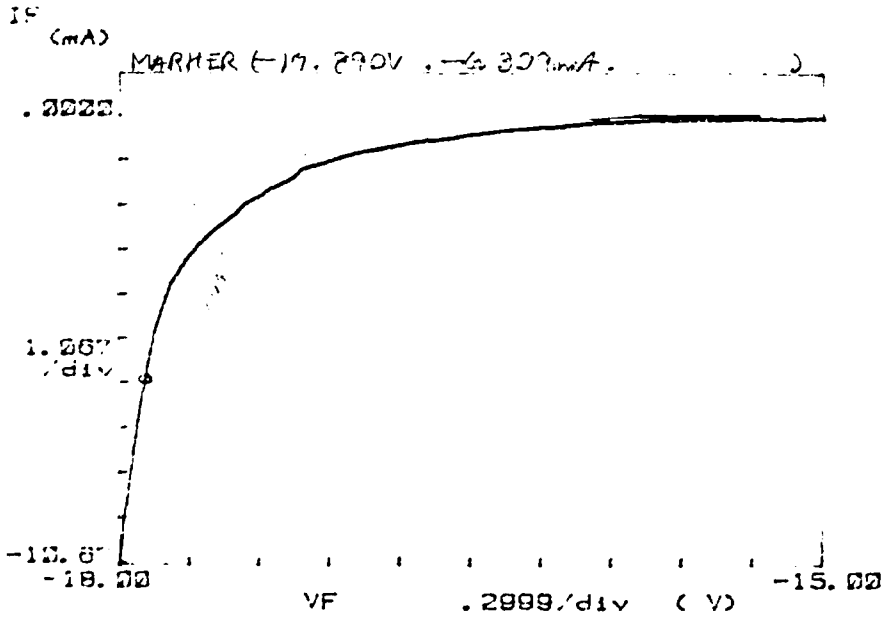


(c) Close-up of avalanche knee.

Figure A5. Concluded.

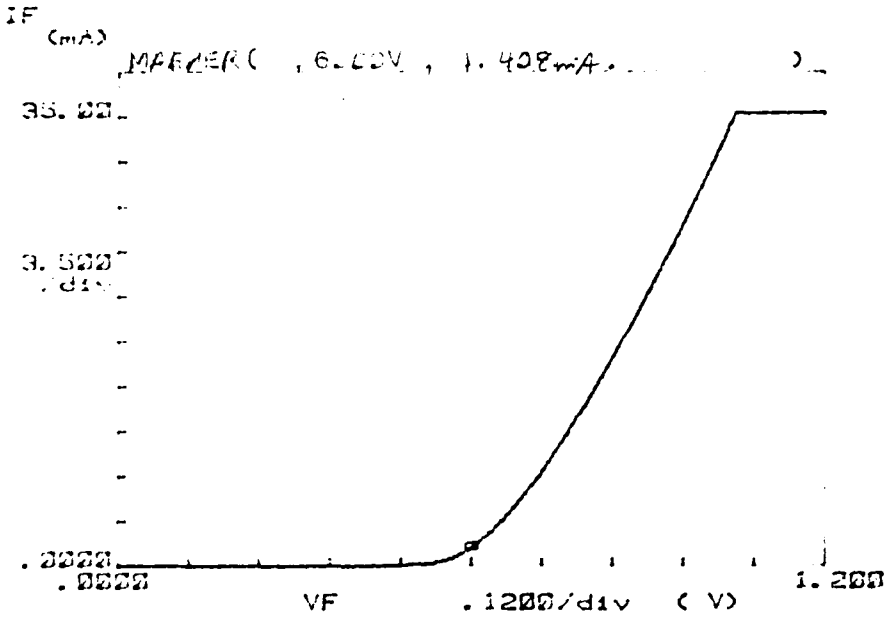


(a) Forward region

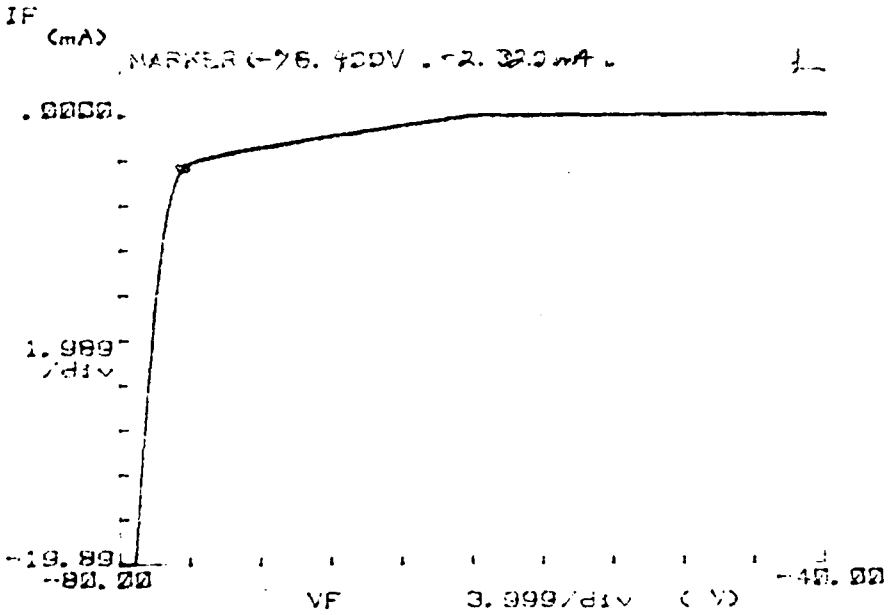


(b) Reverse region

Figure A7. Diode 046 pretest I-V characteristics.



(a) Forward region



(b) Reverse region

Figure A8. Diode 081 pretest I-V characteristics.

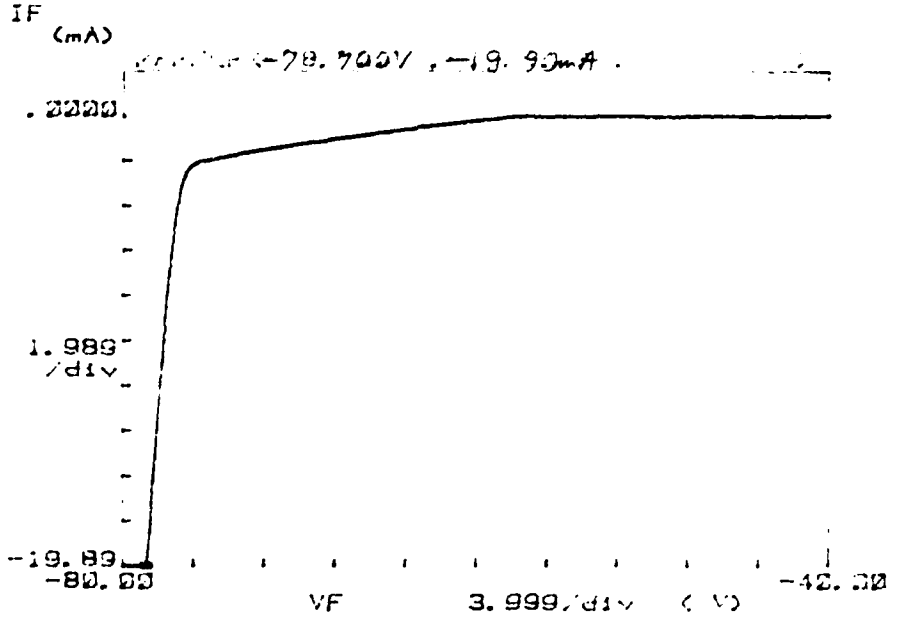


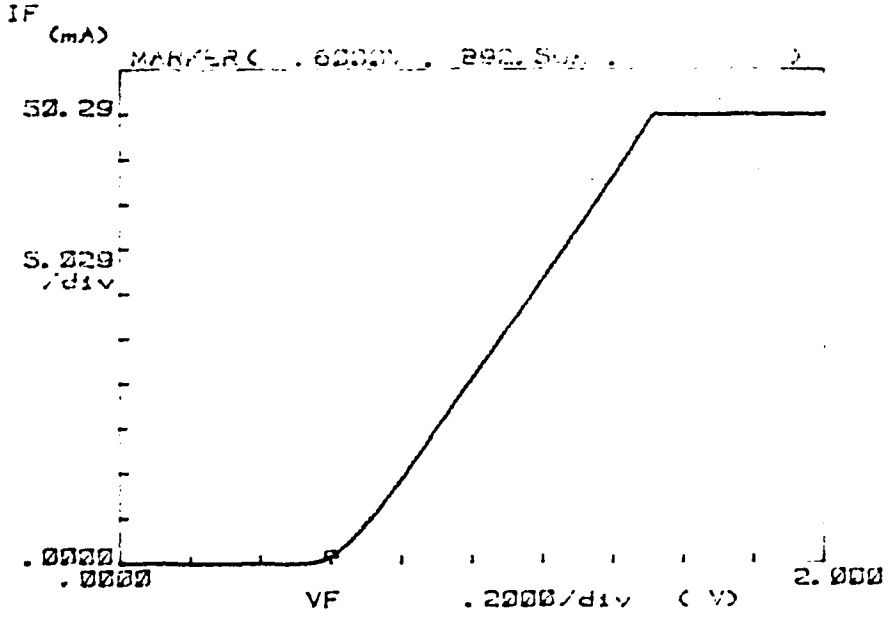
Figure A9. Pretest reverse region I-V characteristics of diode 086.

APPENDIX B

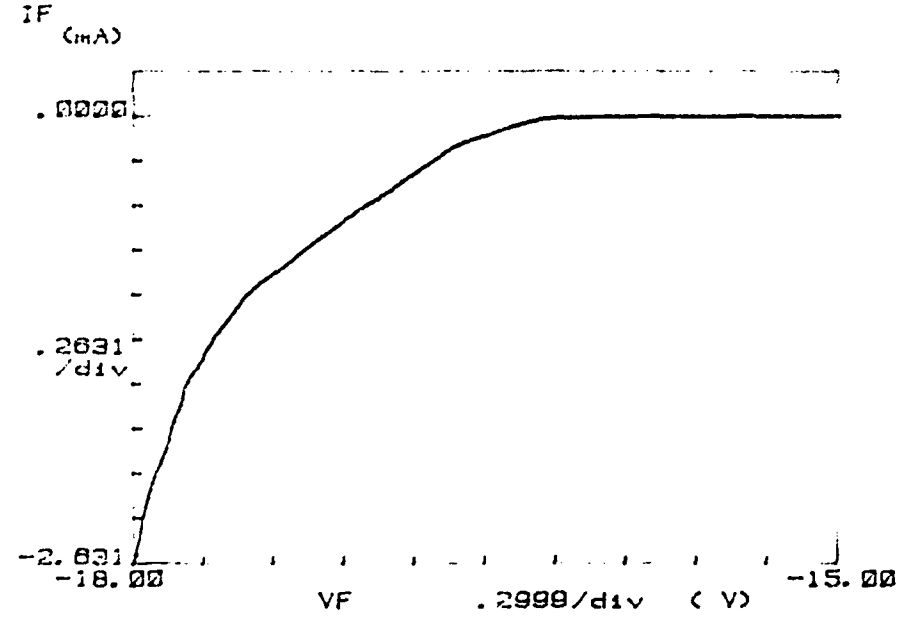
POSTTEST DIODE CURRENT VOLTAGE CHARACTERISTICS

The diodes illustrated in this appendix are: 001, 008, 009, 011, 018, 034, 097, and 100 (Figs. B-1 through B-8).

This appendix does not include curves for diodes 042, 046, 081, and 086. These diodes did not undergo any overstress testing, thus, the characteristics should not have been affected.

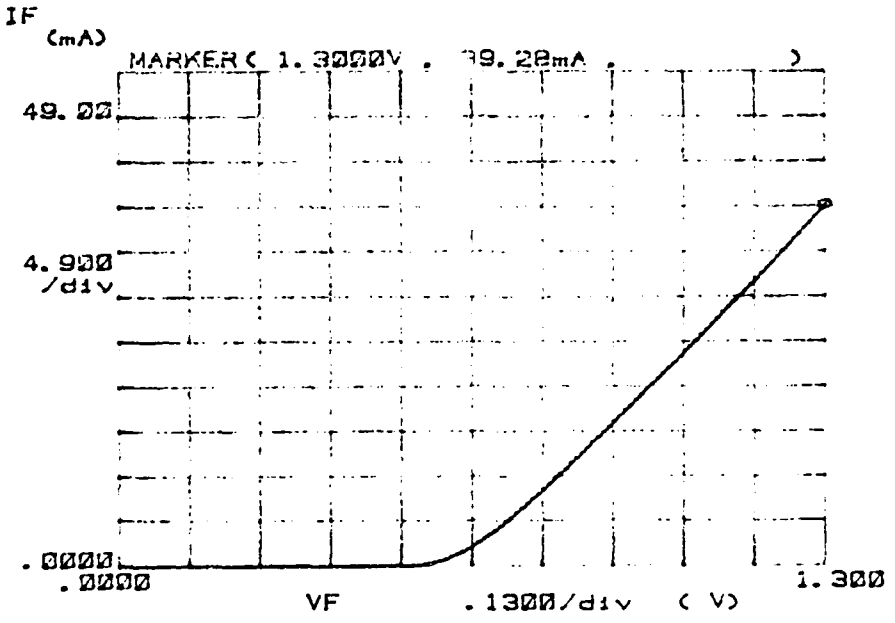


(a) Forward region

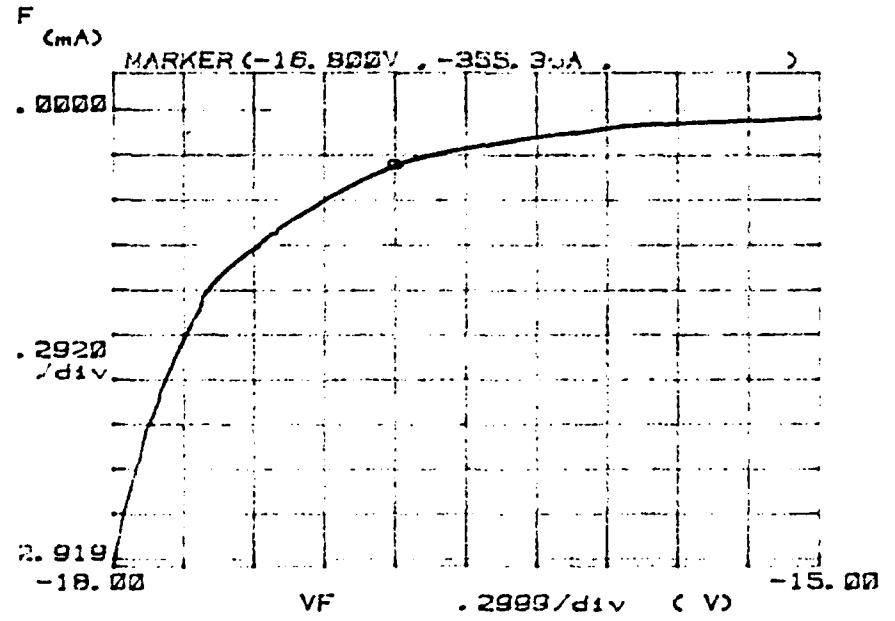


(b) Reverse region

Figure B1. Posttest I-V characteristics for diode 001.

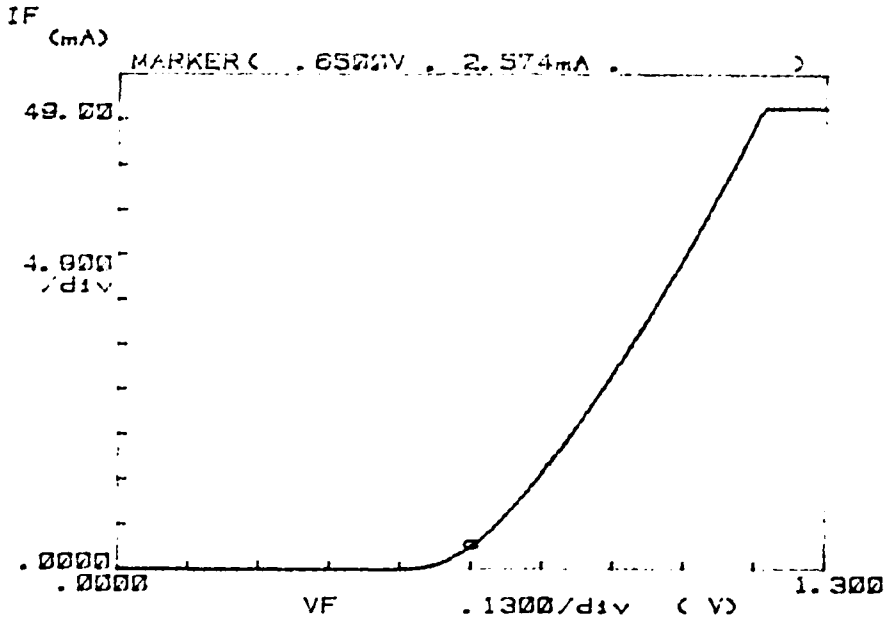


(a) Forward region

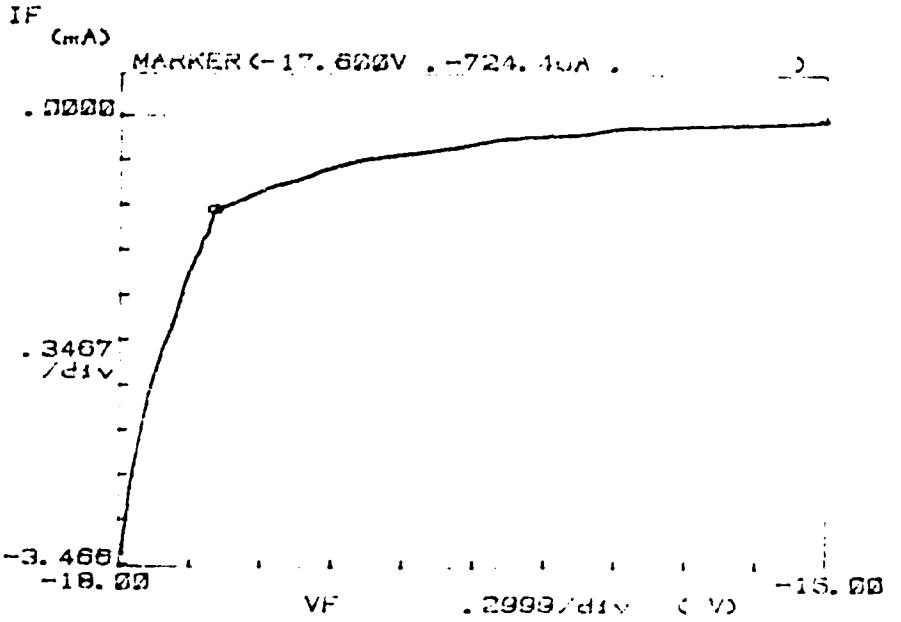


(b) Reverse region

Figure B2. Posttest I-V characteristics for diode 008.

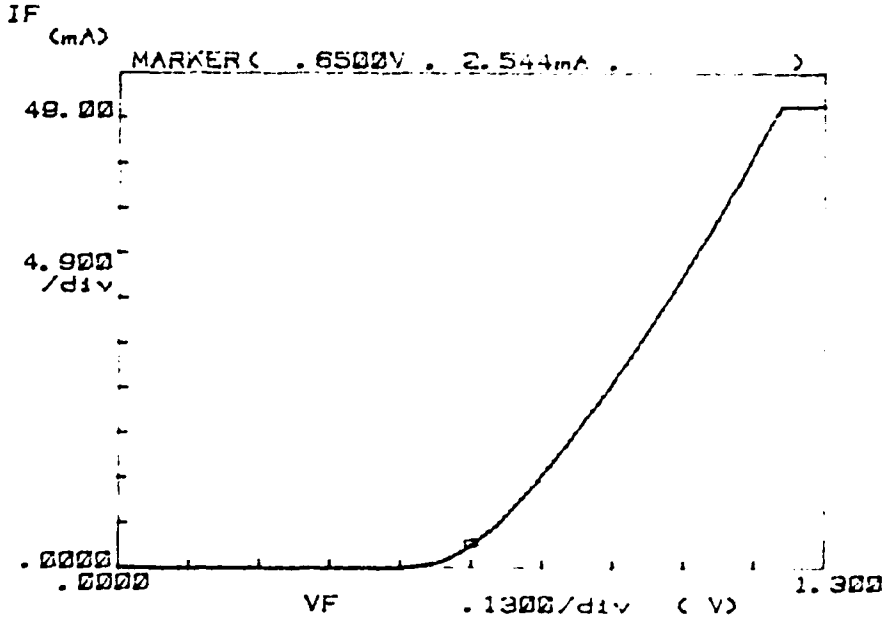


(a) Forward region

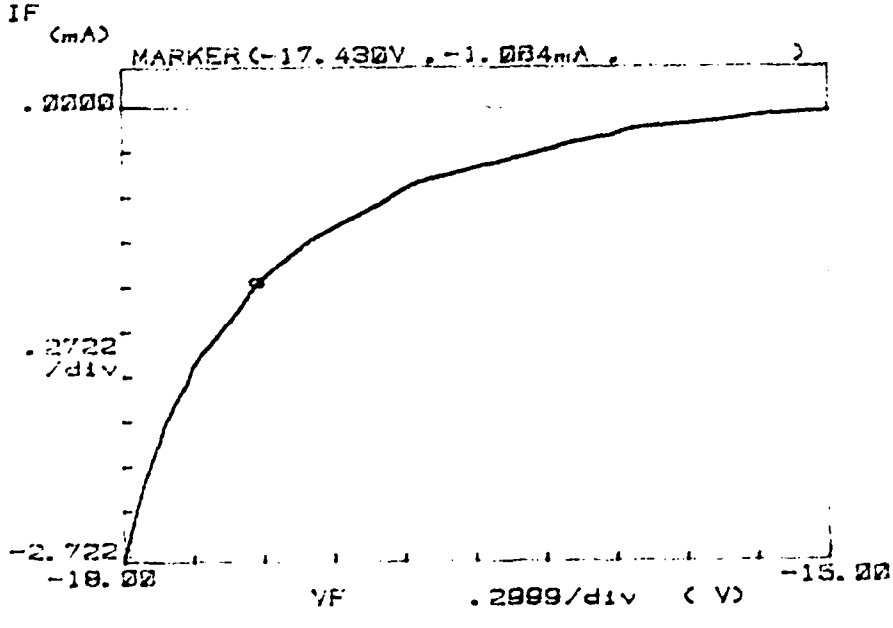


(b) Reverse region

Figure B3. Posttest I-V characteristics for diode 009.

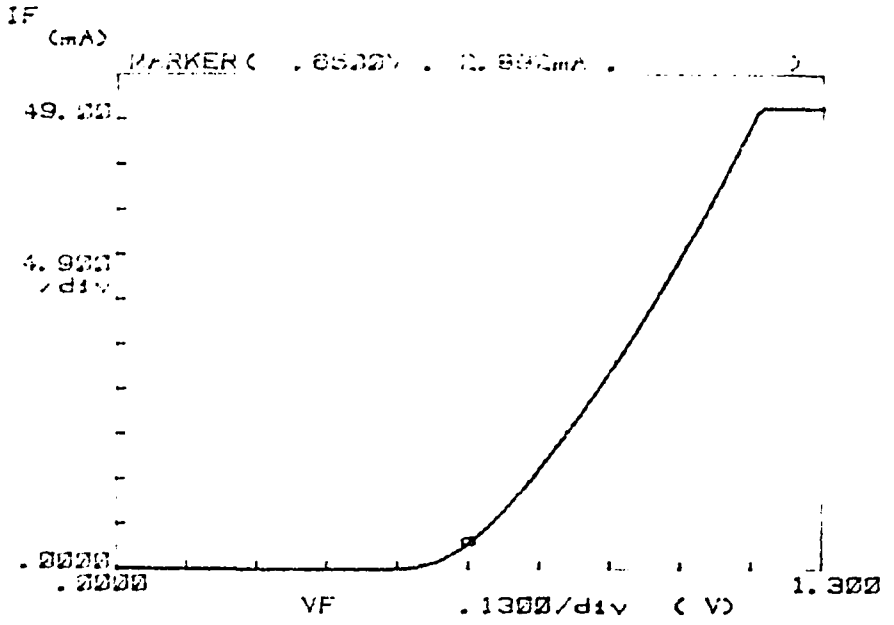


(a) Forward region

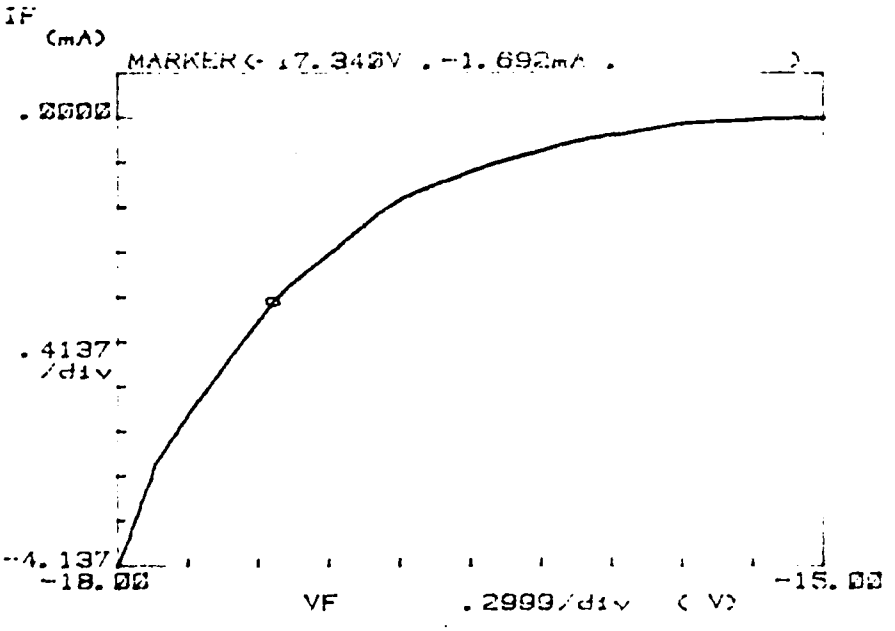


(b) Reverse region

Figure B4. Posttest I-V characteristics for diode 011.



(a) Forward region



(b) Reverse region

Figure B5. Posttest I-V characteristics for diode 018.

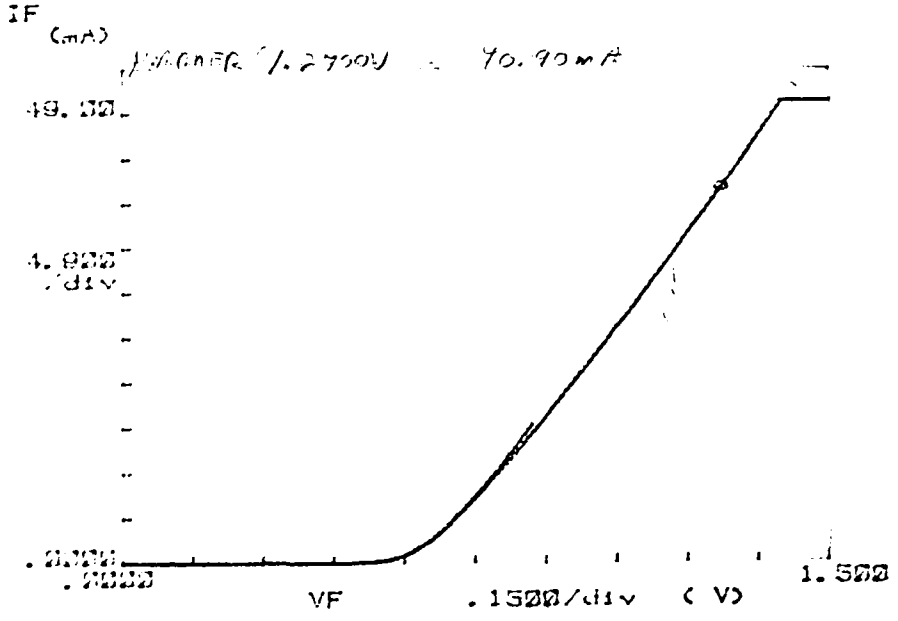
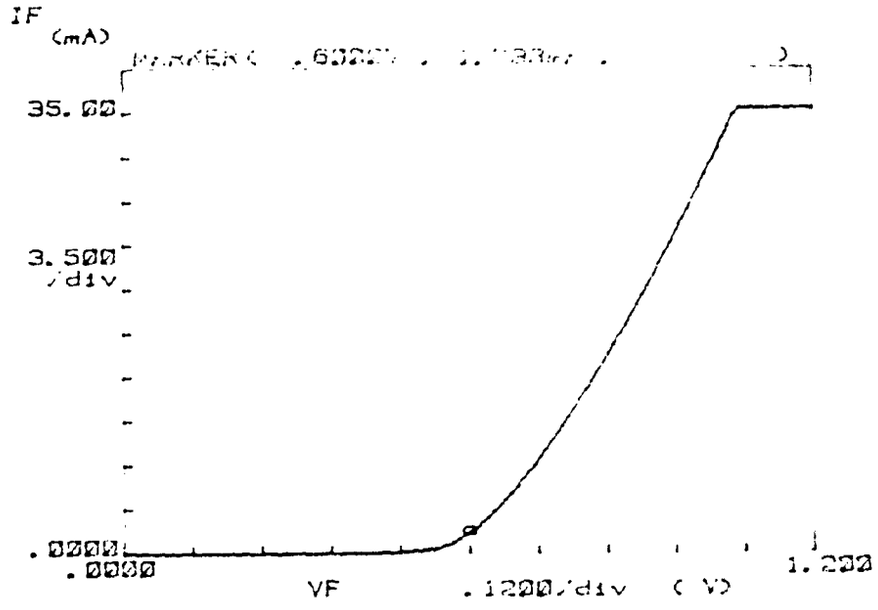
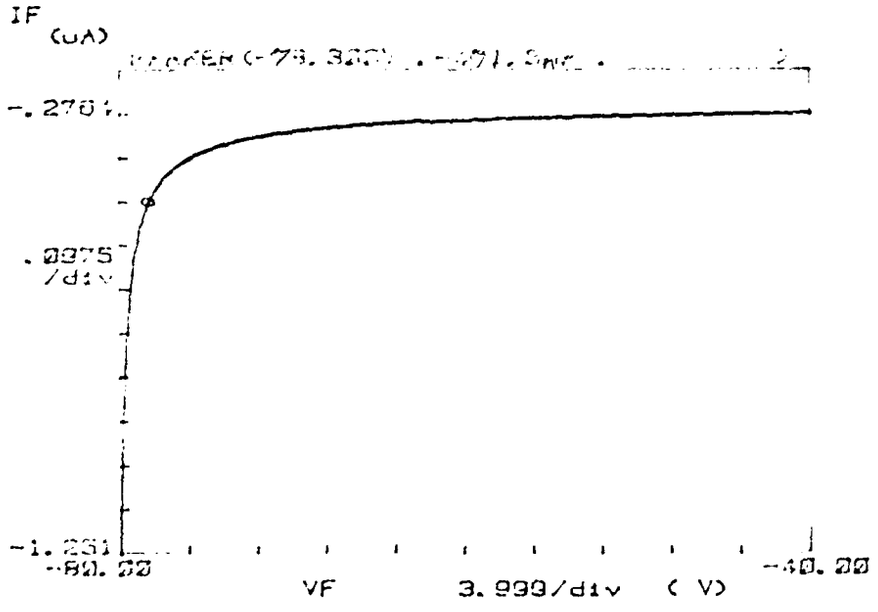


Figure B6. Posttest I-V characteristics for diode 034.



(a) Forward region



(b) Reverse region

Figure B7. Posttest I-V characteristics for diode 097.

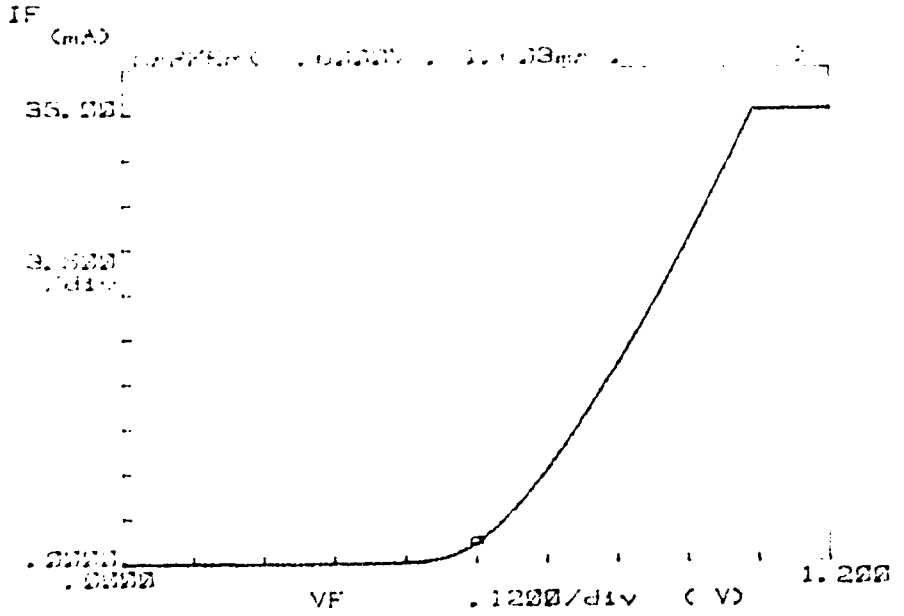


Figure B8. Posttest I-V characteristics for diode 100 in the forward region. The reverse region registers no recordable current flow under any bias of between -17 V and -80 V.