

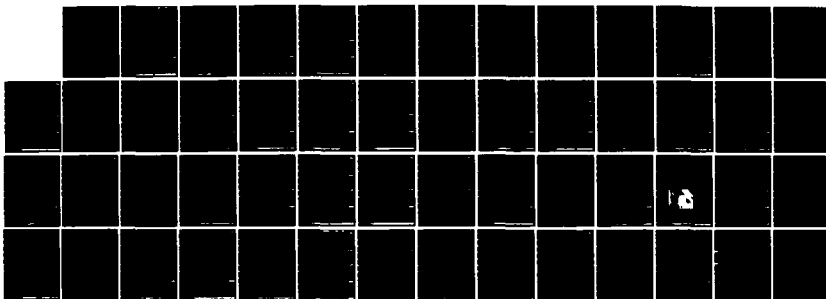
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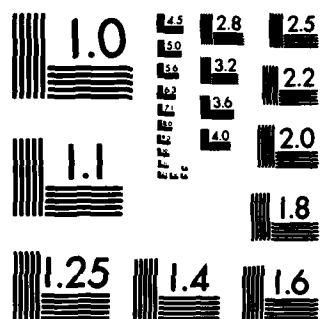
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9TH EUROPEAN SPECIALIST WORKSHOP ON
ACTIVE MICROWAVE SEMICONDUCTOR DEVICES

VELDHOVEN, THE NETHERLANDS

10-12 OCTOBER 1984

PROGRAMME
AND
BOOK OF ABSTRACTS

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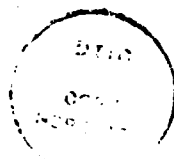
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9th EUROPEAN SPECIALIST WORKSHOP ON ACTIVE MICROWAVE SEMICONDUCTOR DEVICES

Congress Hotel "Koningshof", Veldhoven, 10-12 Oct 1984

P R O G R A M M E

WEDNESDAY 10 OCT

- 8.30 Opening
- 8.45 INV G. Salmer (Un. de Lille)
 MODELING OF SUBMICRONIC DEVICES
- 9.15 K.W.H. Foulds, M.A.R. Al-Mudares (Un. of Guildford, Surrey)
 THE EFFECT OF HIGH TRANSVERSE ELECTRIC FIELDS IN GaAs MESFET'S
- 9.30 D. Lippens, J.R. Nieruchalski, E. Constant (Un. de Lille)
 TIME DOMAIN PARTICLE SIMULATION OF MM WAVE IMPATT DEVICES
- 9.45 S.C. van Someren Gréve, Th.G. van de Roer (Tech. Un. Eindhoven)
 ACCURATE MODELING OF SUBMICRON DEVICE PHYSICS USING
 POLYNOMIAL EXPANSIONS
- 10.00 C. Bacot, A. Scavennec, P. Drouet (CNET Bagneux)
 ORACLE: A PACKAGE FOR INTERPRETATION OF AUTOMATIC
 NETWORK ANALYZER MEASUREMENTS
- 10.15 K. Kazi, I. Mojzes, I. Angelov, L.K. Urshev (Hungarian
 Academy of Sciences, Budapest)
 BROADBAND INVESTIGATION OF TWO TERMINAL PACKAGES FOR MICROWAVE DEVICES
- 10.30 Coffee Break
- 11.00 INV I.G. Eddison (Plessey Caswell Towcester)
 GaAs ANALOGUE MMIC'S
- 11.30 C.M. Snowden (Un. of Leeds)
 MMIC DESIGN BASED ON PHYSICAL DEVICE MODELS
- 11.45 P.R. Shepherd, R.D. Pollard (Un. of Leeds)
 MICROWAVE MEASUREMENT TECHNIQUE FOR GaAs MMIC'S
- 12.00 A. Trasser, H. Schumacher, F. van Raay, H. Beneking (RWTH Aachen)
 A BROADBAND BIAS BLOCK FOR HYBRID GIGABIT LOGIC CIRCUITS
- 12.15 K. Fricke, H.L. Hartnagel (Tech. Un. Darmstadt)
 TRAVELLING-WAVE MESFET'S CHARACTERIZED EXPERIMENTALLY
- 12.30 Lunch

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WEDNESDAY 10 OCT cont.

- 14.00 INV G.T. Brown (RSRE Malvern)
GaAs SUBSTRATE QUALITY: THE CURRENT POSITION WITH RESPECT
TO IC APPLICATIONS
- 14.30 K.-H. Kretschmer, H.L. Hartnagel (Tech. Un. Darmstadt)
INTERELECTRODE BRIDGING WITH GaAs PLANAR STRUCTURES
DEPENDENT ON SEMICONDUCTOR SURFACE CONDITIONS
- 14.45 M. Marengo, M. Cathelin, E. Kohn (Thomson-CSF, Orsay)
A NEW GaAs SELF-ALIGNED GATE TECHNOLOGY BASED ON REFRACTORY METALS
- 15.00 H. Schink (Siemens, München)
INFLUENCE OF THE CHROMIUM CONCENTRATION ON FAT-FET PROFILES
OF ACTIVE LAYERS FOR GaAs MESFET'S
- 15.15 J. Würfl, H.L. Hartnagel (Tech. Un. Darmstadt)
FIELD-ASSISTED INTERDIFFUSION EFFECTS AT THE TRANSITION Al-GaAs
- 15.30 F. Hasegawa, T. Yamate, T. Yamamoto, Y. Mannichi (Un. of Tsukuba,
Sakura-Mura), A. Koukitsu, H. Seki (Tokyo Un. of Agr. & Techn.)
GROWTH AND PROPERTY OF VPE GaAs FOR GaAs FET'S APPLICATIONS
- 15.45 Tea Break
- 16.15 INV E. Kuphal (Deutsche Bundespost, Darmstadt)
LPE MATERIAL FOR InP BASED TRANSISTORS
- 16.45 G. Colomer, M.A. Poisson, C. Brylinsky, S. Hersee (Thomson-CSF)
HIGH POWER HIGH EFFICIENCY MOCVD GROWN InP GUNN DIODES FOR 94 GHz
- 17.00 J. Freyer, X. Zhang (Tech. Un. München)
MILLIMETER WAVE GaAs IMPATT DIODES
- 17.15 J.-F. Luy, W. Behr (AEG-Telefunken, Ulm)
W-BAND IMPATT DIODES MADE FROM Si MBE MATERIAL
- 17.30 Ș. Voinigescu, D. Dascalu (Polytechn. Inst. of Bucharest)
COMPOUND SEMICONDUCTORS FOR MILLIMETRE-WAVE IMPATT DIODES
- 17.45 Late News

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THURSDAY 11 OCT

- 8.30 INV P.J. Tasker, L.H. Camnitz, H. Lee, P.A. Maki, L. Lunardi,
P. Enquist, L.F. Eastman (Cornell Un., Ithaca)
PROGRESS TOWARD PERFORMANCE LIMITS FOR MESFET AND MODFET DEVICES
- 9.00 I. Davies, R. Bennett, D. Brambley, J. Joshi, A. Powell, C. Oxley
(Plessey, Caswell, Towcester)
LOW NOISE K-BAND SUBMICRON FET SHOWING 0.8 dB NOISE FIG. AT 77 K
- 9.15 T. Hariu (Tohoku Un., Sendai)
SOME DESIGN CONSIDERATIONS OF THE OPTIMIZED PERFORMANCE OF
SELF-ALIGNED GaAs MESFET'S
- 9.30 P. Huguet, P. Baudet, C. Venet, M. Iost, M. Pertus, G. Mennechez
(LEP, Limeil-Brévannes)
A 0.5 UM LOW NOISE GaAs FET FOR APPLICATIONS IN THE Ka BAND
- 9.45 M. Laviron, D. Delagebeaudeuf, J.F. Rochette, P.R. Jay,
P. Delescluse, J. Chevrier, Nuyen T. Linh (Thomson-CSF)
ULTRA LOW NOISE AND HIGH FREQUENCY MICROWAVE OPERATION OF
FET'S MADE BY MBE
- 10.00 B.R. Sethi (Un. of Delhi), H.L. Hartnagel (Tech. Un. of Darmstadt)
CHARACTERIZATION OF ELECTRON WIND VOIDING OF GaAs FET
METALIZATION IN VIEW OF DEVICE LIFETIME LIMITATIONS
- 10.15 Coffee Break
- 10.45 INV H. Hasegawa (Un. of Hokkaido, Sapporo)
RECENT JAPANESE DEVELOPMENTS OF HIGH-SPEED DEVICES BY
NON-MESFET APPROACHES
- 11.15 J.R. Wendt, L.F. Eastman (Cornell Un., Ithaca),
E. Kohn (Thomson-CSF, Orsay), U.K. Mishra (Gen. Electric, Syracuse)
VERTICAL HETEROJUNCTION FET STRUCTURE WITH 100 nm
SOURCE TO GATE SPACING
- 11.30 A. D'Ambrosio, G. Fattore (GTE, Milano)
DRIFTING PHENOMENA IN POWER FET'S
- 11.45 D.A. Allan (British Telecom, Ipswich)
TUNGSTEN SILICIDE SCHOTTKY DIODES FOR GaAs MESFET'S
- 12.00 L.R. Dawson (Sandia Labs., Albuquerque)
InGaAs STRAINED LAYER SUPERLATTICES FOR HIGH SPEED FET'S
- 12.15 Late News
- 12.30 Lunch

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FRIDAY 12 OCT

- 8.30 INV P. Greiling (Hughes Res. Labs, Malibu)
HIGH SPEED DIGITAL IC PERFORMANCE OUTLOOK
- 9.00 INV M. Rocchi (LEP, Limeil-Brevannes)
GaAs HIGH SPEED LOW POWER DIGITAL IC'S
- 9.30 R. Zuleeg (McDonnell Douglas Microelectronics, Huntington Beach)
REALIZATION OF COMPLEMENTARY GaAs JFET CIRCUITS
- 9.45 A. Trasser, F. Ponse, H. Schumacher, H. Beneking (RWTH Aachen)
A SYNCHRONIZED CLOCK GENERATOR FOR 6 GBIT/s SIGNAL REGENERATION
- 10.00 R. Schmitt, L.M.F. Kaufmann, K. Heime (Un. Duisburg)
InGaAs JFET'S WITH p^+ GATES MADE BY DIFFUSION FROM SPIN-ON FILMS
- 10.15 Coffee Break
- 10.45 INV D. Fritzsche, H. Kräutle (Deutsche Bundespost, Darmstadt)
OPTOELECTRONIC IC'S BASED ON InGaAsP/InP:
CONCEPTS, PROBLEMS AND PROSPECTS
- 11.15 N. Matsuo, H. Ohno, H. Hasegawa (Hokkaido Un., Sapporo)
INTEGRATED PHOTOCONDUCTIVE DETECTOR/FET GaAs RECEIVERS WITH SIMPLE
OPTICAL COUPLING TO FIBERS FOR INTERCONNECTIONS IN VERY HIGH SPEED IC'S
- 11.30 S. Swaminathan, H.V. Shurmer (Un. of Warwick)
CHARACTERIZATION OF DEVICES EMPLOYING MULTILAYER
QUATERNARY MATERIALS
- 11.45 J. Selders, L. Vescan, M. Maier, H. Beneking (RWTH Aachen)
APPLICATION OF Be ION IMPLANTATION TO GaInAs JUNCTION FET'S
- 12.00 B.R. Singh, H. Jürgensen, M. Heyen, P. Balk (RWTH Aachen)
LOW PRESSURE HALIDE GROWTH OF EPITAXIAL InP FOR MICROWAVE DEVICES
- 12.15 Closing of the Workshop
- 12.30 Lunch

MODELING OF SUBMICRONIC DEVICES

G. SALMER

Centre Hyperfréquences et Semiconducteurs
L.A. C.N.R.S. n° 287 - Bat. P4
Université des Sciences et Techniques de Lille I
59655 VILLENEUVE D'ASCQ CEDEX - FRANCE

SUMMARY :

In high speed digital or microwave integrated circuits, the MESFET is the most commonly used active device. The progress in lithography techniques allows to realize very small device structures, with gate lengths smaller than 0,5 μ m. Moreover, a great number of new structures such as recessed gate or vertical channel MESFET's and TEGFET have been conceived.

More sophisticated models than the classical ones must be used in order to predict the performance of such device. They have to take into account new phenomena :

- non stationary electron dynamics effects ;
- surface and interface influences ;
- exact substrate properties ;
- two dimensional effects : edge effects, injection...

Three different types of models have been conceived for this purpose :

- Monte Carlo particle models and direct resolution of the Boltzman equation ;
- Two dimensional resolution of macroscopic equations (including relaxation equations) ;
- One dimensional resolution of the basic equations.

These models are briefly described. A comparison between them is presented and their respective fields of application are precised.

The Effect of High Transverse Electric Fields in GaAs MESFETS

K.W.H. Foulds and M.A.R. Al-Mudares

Department of Physics, University of Surrey, Guildford, Surrey,
GU2 5XH, U.K.

The paper will deal with the physical interpretation of the results obtained from a Monte Carlo two dimensional simulation of microwave GaAs MESFETS. It will show, in particular, that the effects of the gate are more subtle than would be expected from the simple Shockley model.

In a microwave MESFET the depletion layer boundary between fully depleted and undepleted regions is not abrupt. Because of this, some electrons move under the action not only of the longitudinal field but also of a transverse field. These transverse fields can be very large and exert a dominating influence in whether a current drop back occurs in the I-V characteristic or not. The situation applies both to idealised unsubstrated devices and to practical devices with substrates, and a number of different substrates will be considered.

TIME DOMAIN PARTICLE SIMULATION
OF MILLIMETER-WAVE IMPATT DEVICES

D. LIPPENS, J.L. NIERUCHALSKI, E. CONSTANT

Centre Hyperfréquences et Semiconducteurs
Laboratoire Associé au C.N.R.S. n° 287 - Bat. P4
Université des Sciences et Techniques de Lille I
59655 VILLENEUVE D'ASCQ CEDEX - FRANCE

As IMPATT devices become smaller and are used in ever higher frequency band, it is expected that the relevant temporal and spatial scales become sufficiently small that the classic approach of their operation is no longer valid. The main reason is that the system may undergo subsequent relaxation to a non equilibrium state non involved in traditional treatments.

The aim of this paper is to propose a time domain simulation of millimeter-wave IMPATT devices. The difficulty of incorporating the transient behaviour is overcome by performing a microscopic analysis, the motion of each particle (electron and hole) being studied only in the geometrical space. This model has been applied to the simulation of a 100 GHz Silicon double drift IMPATT diode with an active length of 0.5 μm and a doping density of $2 \cdot 10^{17} \text{ cm}^{-3}$. An efficiency of 0.13 with a diode admittance of $-2567 + j 11635 \text{ S/cm}^2$ was determined for a current density of 29 kA/cm^2 . These results are consistent with experimental ones. This shows that a microscopic description of the impact ionization, restricted at present in the literature to a static one particle Monte Carlo procedure, permits to compute sufficient characteristics in order to comprehensively describe the operation of avalanche devices in the time domain.

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ACCURATE MODELING OF SUBMICRON DEVICE PHYSICS USING POLYNOMIAL EXPANSIONS

S.C. Van Someren Greve, Th. G. Van de Roer,
Eindhoven University of Technology, Dept ET
Eindhoven, The Netherlands

A new method of devices modeling has been developed which is eminently suited for submicron devices in III-V compounds. The carrier distribution function in k -space is represented by a limited number (10-50) of coefficients by expansion in orthogonal Legendre and Hermite polynomials. This number is sufficient to calculate the macroscopic quantities like valley populations and velocities with great accuracy. Boltzmann's equation, including integrals representing the various scattering processes, is thus converted into a set of hydrodynamical equations which is solved by an explicit integration method. The technique has been applied to calculate velocity overshoot in uniform materials, giving excellent agreement with other methods, and to find the current response of plane $n^+ - n - n^+$ diodes to voltage steps and time-harmonic voltages. Phenomena like accumulation layer formation, intervalley transfer and velocity overshoot in devices can be studied in great physical detail and devices like mm wave Gunn diodes can be simulated accurately. Extending the method to two space dimensions will be straight-forward.

ORACLE : A PACKAGE FOR INTERPRETATION OF AUTOMATIC NETWORK
ANALYSER MEASUREMENTS

(C. Bacot, A. Scavennec, P. Drouet)
Centre National d'Etudes des Télécommunications
196 rue de Paris 92220 BAGNEUX - FRANCE

This paper presents a software which allows to interpret micro-wave small signal scattering parameter measurements in terms of equivalent networks ; This type of need in device modelling is generally rather poorly met by commonly used CAD programs.

However some efficient feedback from measurements performed on devices helps the improvement of technological process under maturation.

Our approach involves the description of any equivalent circuit with simple lumped and distributed elements.

The problem is then solved by minimizing a least square error function between currents on the automatic network analyser ports and currents calculated on the equivalent network by a nodal AC analysis routine. Any element may be set or allowed to vary.

Gradient computations are performed with use of the adjoint network theory.

This has been applied to devices involved in optoelectronic IC's MISFETS, J-FETS, LASERS etc.... On the well known case of GaAs MESFETS it is shown that the tabulation of results obtained under various bias conditions may lead to experimental models for large signal operation.

Due to usefulness of such a tool, this program offers facilities such as a simple input language and the use of libraries for measurements and equivalent circuits.

K. Kazi , I. Mojzes , I. Angelov and L.K. Urshev

Broadband investigation of two terminal packages for
microwave devices

In the present work we would show a few experimental results of ceramic-metal packages for Gunn devices in the 6,5-18 GHz frequency band and computed results for the same frequency band. Microwave impedance measurements were made in a coaxial network by computer controlled S-parameter test system. To determine the elements of package equivalent circuit, several packages were prepared without active chip and with "open" and "short" circuit in place of the active chip. The leads e.g. gold wires of diameter 50 μm were made in three configurations: single wire, double parallel wires, double crossed wires. Having made use of experimental results pi-equivalent circuits were computed, e.g. the typical values of the equivalent pi-network elements, the package with single wire were the next:

$$C_A=0.306 \text{ pF} ; \quad C_B=0.096 \text{ pF} ; \quad L_D=0.511 \text{ nH}$$

Accuracy of measured values was better than ± 1 percent.

To show that the inductance of pi-equivalent network depends on the physical dimension and configuration of bonding wire only, a few measurements of this packages without wire were made.

GaAs ANALOGUE MMICs

I.G. Eddison

Plessey Research (Caswell) Ltd., Allen Clark Research Centre,
Caswell, Towcester, Northants. England.

Today, the development of monolithic microwave integrated circuits (MMICs) is at an interesting stage. With the introduction of development and pilot production facilities within many companies worldwide the MMIC is no longer a research laboratory curiosity. Indeed MMICs are now being developed for a variety of military, commercial and consumer systems. Of these applications the most popular are advanced phased array radars and direct broadcast satellite TV receivers (DBS). In both these applications low cost, reliability and reproducibility are crucial to the systems success. These constraints and the potentially high chip production numbers demand a high degree of automation in circuit design, wafer production, chip testing and module assembly. This paper therefore reviews the MMIC from the standpoint of two of the most important automated techniques viz. computer aided design and computer assisted testing.

Following a brief description of MMIC processing technology the problems associated with circuit design are detailed with reference to an X-band LNA circuit development. This case study shows the successful realisation of a 16 dB gain, low noise (<4 dB NF) amplifier chip operating over the 8 to 10 GHz frequency range. In addition further circuit examples are given to show the increasing complexity of MMIC system design.

Having designed and processed the MMIC wafer the question of chip evaluation and selection becomes vital. To minimise production costs and timescales the d.c. and microwave characteristics of the IC chips have to be ascertained before the as-processed wafer is diced. This approach avoids the excess costs and times of bonding and testing non-functional chips. The development of a wafer probe ATE system for MMIC production testing is thus described and details of probed phase shifter and amplifier IC measurements are also given.

Acknowledgements

The author acknowledges with pleasure the work of his numerous colleagues in GaAs IC design and fabrication at Plessey Research (Caswell) Ltd.

Part of this work was carried out with the support of Procurement Executive Ministry of Defence sponsored by DCVD.

MMIC DESIGN BASED ON PHYSICAL DEVICE MODELS

Christopher M. Snowden

Solid State Materials, Devices and Applications Group,
Department of Electrical and Electronic Engineering,
University of Leeds,
Leeds. LS2 9JT
United Kingdom

A comprehensive two-dimensional numerical device simulation, capable of modelling MMIC elements both individually and collectively in simple circuits, has been developed to provide a sound basis for the design and characterisation of GaAs MMIC devices operating upto 18GHz. This approach circumvents the problems associated with equivalent circuit modelling techniques frequently encountered when analysing active microwave devices.

The simulation is based on the solution of a time-dependent set of semiclassical carrier transport equations, which include energy and momentum relaxation effects. Rapid finite-difference numerical techniques are used to implement the model, which allow long simulation times to be achieved in moderate amounts of computer time. The simulation allows a variety of devices to be incorporated into simple MMIC circuits and permits the investigation of individual devices as well as the determination of the terminal characteristics of the circuit.

Monolithic circuit elements that are being investigated using this approach include MESFETs, varactor diodes, pin diodes, resistors and TEDs. The simulation has been applied to the design of fixed frequency and voltage controlled oscillators. This simulation plays a particularly important role in the design and development of MMICs at frequencies above 2GHz where equivalent circuit models become increasingly unreliable, and allows devices to be optimised at a pre-fabrication stage.

MICROWAVE MEASUREMENT TECHNIQUE FOR GaAs MMICs

A major problem associated with the design of microwave integrated circuits on gallium arsenide is the verification of designs and design changes from microwave measurements. The problem is fundamentally one of mounting the circuit in such a way as to be able to accurately and reliably measure the r.f. properties or response of the circuit. Inherent in this measurement is a procedure in which the measurement equipment is calibrated using 'known' pieces of circuit (shorts, opens, loads, through lines etc.).

Microwave monolithic circuit measurement philosophies can be divided into two principal categories in which the integrated circuit is either probed directly or is connected into an external circuit or package and the chip performance is de-embedded from data taken on the overall circuit. The method of direct probing requires calibration of the measurement system to be performed 'on-chip', i.e. the calibration pieces have to be manufactured in the same medium as the circuit to be measured. The alternative, more traditional, more traditional technique requires the chip to be bonded into a test circuit or package and the process of de-embedding requires the modelling of such items as adaptors, transitions or launchers as well as bond wires. The modelling of bond wires, especially, is highly suspect at frequencies in excess of 10 GHz and consequently results in large uncertainty in the parameters for the chip which are obtained from the de-embedding process.

The measurement work has concentrated on employing a direct launcher connection to the substrate and a 'semi-redundant' calibration technique where all the 'standards' are fabricated on the same material as the circuit to be tested. The fixtures which are currently in use are designed to accommodate 10 mm x 10 mm samples with microwave connections at up to four ports. Measurements are made using a phase-locked automatic network analyser employing the conventional 12-term error model. The reflection calibration at each port is achieved by means of a series of offset open circuits. The redundancy of the process enables a value to be obtained for the impedance of the open circuit as well as providing a check on the self-consistency of the calibration procedure. Provided that all of the calibration pieces are realized on the same substrate material with identical linewidths, assumptions made about the material properties will not affect accurate calibration of the measurement system and will allow the definition of a reference plane on the medium under test. This technique offers the best means of evaluating the transmission line properties of GaAs substrates whilst making minimal assumptions as well as assessing the repeatability of the technique.

P. R. Shepherd & R. D. Pollard

Department of Electrical and Electronic Engineering,
The University of Leeds,
Leeds, LS2 9JT,
U.K.

A Broadband Bias-Block for Hybrid Gigabit Logic Circuits

A. Trasser, H. Schumacher, F. van Raay and H. Beneking

Institute of Semiconductor Electronics
Technical University Aachen

Microwave broad-band applications, e.g. Gbit/s logic circuits or broadband amplifiers are greatly enhanced by integrating the biasing networks.

Therefore a wide-band bias-block, covering 0.1-18 GHz, has been integrated in microstrip on alumina ceramic substrate.

The bias block basically consists of a spiral inductor in the dc-path and a capacitor for RF coupling. An additional capacitor from the DC-terminal to ground prevents the penetration of residual RF into the DC supply.

The line width of the spiral inductor is tapered towards the 50 Ω stripline, reducing the resonant behaviour always encountered in broadband inductances and keeping the disturbance of the RF path small. The resonance effects have been finally overcome with an integrated damping resistor in thin film technology.

The coupling capacitor should best be realized as an overlay capacitor in thin film technology, however technological problems have to be overcome because of the roughness of the substrates. The low frequency limit requires a large coupling capacitance ($> 70\text{pF}$), leading to large electrode areas and thin dielectric films, suggesting the use of polished semiinsulating semiconductor substrates.

Results of prototypes with chip capacitors, RF insertion loss $< 2\text{ dB}$ at 0.1-18 GHz, DC-path resistance $< 4\Omega$, will be presented.

TRAVELLING-WAVE-MeSFETs CHARACTERISED EXPERIMENTALLY

K. Fricke
H.L. Hartnagel

Institut für Hochfrequenztechnik
Technische Hochschule Darmstadt
Merckstraße 25, 6100 Darmstadt, FRG

✧ In this paper wave-propagation along the electrodes of a travelling-wave-FET is experimentally investigated. This travelling-wave-FET is a GaAs-Schottky-FET with large 'gate width' and connecting pads on both ends of the gate- and drain-electrodes. For this 4-port a set of 16 S-parameters for each frequency was measured using a network-analyser. From the reflection- and transmission-parameters of gate- and drain lines the wave-impedances and propagation constants were calculated. It is shown that the wave-impedance of the gate line is higher and depends much more than the drain line on the gate-voltage due to the depletion layer under the gate. The propagation and attenuation-constants of the gate line are higher than those of the drain line as is expected from the slow wave behaviour of this mode.

From the measured S-parameters the loads on the usually open ends of the gate line and the drain line were calculated so that the MAG of the remaining 2-port becomes maximal. These calculations are in very good agreement with the experimental results obtained by simulating the loads with tunable loads. It is shown that a great improvement of the MAG is possible.

GaAs Substrate Quality - the Current Position with Respect
to IC Applications

G T Brown

RSRE, St Andrews Road, Malvern, Worcs, UK, WR14 3PS

The inhomogeneity of semi-insulating GaAs substrates is a subject of some concern to those interested in fabricating ICs by direct ion implantation. It is well established that the dislocation density can vary markedly across a wafer and there have been a number of studies suggesting that variations in device parameters can be correlated with fluctuations in dislocation density. It is likely that it is not the dislocation itself which creates such effects both the propensity for dislocations to locally perturb the point defect distributions. This paper reviews the current understanding on the distribution of dislocations in semi-insulating substrates and how they may modify the distribution of point defects. Efforts to reduce or homogenise dislocation densities and the concomitant effects are also reviewed. Finally, in view of the interest in integration of electronic and optical components, the effect of substrate quality on optical devices is also briefly discussed.

INTERELECTRODE BRIDGING WITH GaAs PLANAR STRUCTURES DEPENDENT ON
SEMICONDUCTOR SURFACE CONDITIONS

K.-H. Kretschmer

H.L. Hartnagel

Institut für Hochfrequenztechnik
Technische Hochschule Darmstadt
Merckstraße 25, 6100 Darmstadt

XPS measurements and studies of material migration between neighbouring electrodes on GaAs surfaces have shown that there are large differences in the threshold for material transport from one electrode across the GaAs surface to the neighbouring one. For example etchants based on H_2SO_3 exhibited a breakdown voltage less than 30 % of those treated with KOH type etchants. The surface analysis shows that the former case results in a large amount of arsenic oxide whereas the latter case is based on a strongly reduced surface oxygen content. Further details can be derived from the XPS spectra and a great deal of useful information is found on the properties of the types of surfaces used. So far a selection of 5 typical technology conditions as based on various etchants and cleaning solutions have been investigated as commonly employed for the manufacture of GaAs devices.

A NEW GaAs SELF ALIGNED GATE TECHNOLOGY

BASED ON REFRACTORY METALS

M. MARENGO, M. CATHELIN, E. KOHN

Thomson-C.S.F., D.H.M., Domaine de Corbeville, B.P. n° 10, ORSAY (France)

Currently self-aligned gate technology (containing a self-aligned N^+ contacts implantation) is applied in GaAs FETs by using refractory metal systems as TiWSi, WSi, or WAl mixtures. Prime interest is on enhancement mode of operation where high extrinsic transconductances and high switching speeds can be achieved. However there is still a need to overcome the low gate to drain breakdown voltage and to increase gate diode barrier height.

In the new concept presented here, a thin interfacial spacer is inserted between the refractory metal gate (TiW) and the GaAs. This spacer is a nitridized TiWSi film, deposited by reactive sputtering of TiWSi in a N-plasma. This spacer improves the temperature stability of the metal GaAs barrier essentially. Diode characteristics show $n = 1.07$, $\phi_B = 0.85$ V after 850° C, 15 min annealing.

Application in FET technology results in a T-gate structure, where the TiW forms an overhang over the TiWSi (N) spacer. First self-aligned 1 μ m FETs with N^+ contact implants yielded in a $g_m \approx 140$ ms/mm for enhancement mode of operation. Drain breakdown voltages in excess of 5V are achieved.

The spacer layer represents a highly resistive interfacial layer and can thereby act as a dc-gate current limiter. In the dynamic mode this resistance is however short circuited by its dielectric capacitance. This makes the contact attractive for mmW FET structures.

Influence of the Chromium-Concentration on Fat-FET
Profiles of Active Layers for GaAs-MESFET

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The depth dependence of carrier concentration and mobility of implanted layers in semiinsulating GaAs was investigated by Fat-FET measurements for materials with different chromium concentration. The experimental results are discussed in terms of the peak carrier concentration as parameters. It allows to investigate the influence of the chromium concentration on the shape of the doping profile. Static FET data are also presented and compared with the Fat-FET results.

It is shown, that with increasing chromium concentration the peak carrier concentration decreases and the profile gets steeper. This is not an effect of variations in the compensation ratio alone but also of an altered diffusion mechanism. For high chromium concentrations the electron mobility, taken at a doping level of $1 \cdot 10^{17} \text{ cm}^{-3}$ decreases due to the increasing compensation. Homogeneity across the wafer is also influenced by the presence of chromium: for high concentrations an M shape for the diffusion constant and the peak carrier concentration appears. Electrical parameters of $1 \mu\text{m}$ -FET's are clearly correlated to the shape of the doping profile.

By means of Fat-FET measurements it is possible to distinguish between several effects influencing electrical properties of MESFET's. Doping profil and peak carrier concentration on the one hand and mobility on the other.

FIELD-ASSISTED INTERDIFFUSION EFFECTS AT THE TRANSITION Al-GaAs

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Metal contacts on semiconductor devices have to be resistant to interdiffusion and must retain their properties during device operation. The operation conditions are associated with a combination of elevated temperatures, high electric fields and high current densities. A degradation of contacts during device operation results in a corresponding reduced device performance⁽¹⁾. Device lifetime investigations reveal that some of the important degradation mechanisms are bias sensitive and that accelerated lifetime assessment without bias (i.e. using elevated temperatures only) gives erroneously long lifetime projections⁽²⁾.

The influence of high electric fields on the interface properties of the Al-GaAs transition most commonly used in GaAs MeSFET gate metallizations has been studied in our investigations by using XPS-sputter profiling techniques. All test samples were etched in various solutions that are commonly used in GaAs device fabrication. Some of the experimental results can be summarized as follows: Device operation at high electric fields seems to lead to a structural change in the polycrystallinity of the Al-layer that can probably be explained by a field-enhanced material diffusion along grain boundaries in the Al-film⁽³⁾. The amount of oxygen and the Ga to As ratio at the Al-GaAs interface has been found to depend on the electric field applied.

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Growth and Property of VPE GaAs for GaAs FET's Application

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The chloride VPE of GaAs is most widely used for preparation of practical GaAs FET's active layers. However, there are still several problems such as nonuniformity of epi-layer, surface irregularity, and abnormal interface layer, which deteriorate the performance and yield of GaAs FET's.

In this paper, we discuss a new chloride VPE method which can produce uniform and reproducible epitaxial layer. This method utilizes transport of GaCl by helium and reduction of GaCl at the growth region by hydrogen, with uniform temperature of source and growth region.

It was found that epitaxial layers grown on the substrates 2° off from (100) surface toward <110> direction always give lower carrier densities (generally a half) and smoother surface than those grown on (100) just substrates. Abnormal high resistive interface layer was wider but smaller for the 2° off substrates than for just substrates, and was bigger for HB subs. than for LEC substrates.

DLTS measurements revealed that there are many deep acceptor levels due to Cu and Fe at the interface, whose concentrations are proportional to depth of the carrier density dip. This abnormal interface layer affects properties of high purity buffer layer for GaAs FET application. These problems are presented and discussed in this paper.

LPE Material for InP-based Transistors

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This paper describes the preparation and characterization of liquid phase epitaxial (LPE) material used for InP-based high-speed transistors. The structures investigated are

- (I) s.i. InP/ p^- -InP/ n^+ -InP or s.i. InP/ n^+ -InP for InP-MISFETs,
- (II) s.i. InP/ p^- -InGaAs/ n^+ -InGaAs for InGaAs-MISFETs,
- (III) s.i. InP/ n -InGaAs for diffused InGaAs-JFETs and
- (IV) s.i. InP/ n^+ -InP/ n^- -InGaAsP/ p^+ -InGaAsP/ n -InP for quaternary bipolar (photo)-transistors. In the latter case $\lambda = 1.25 \mu\text{m}$ as well as $\lambda = 1.55 \mu\text{m}$ devices have been made.

Our results on the following problems and material properties will be reported:

- 1) Shallow impurities and doping problems in InP and InGaAs.
- 2) Deep levels in InGaAs.
- 3) Phase equilibria in the systems InP, InGaAs and InGaAsP.
- 4) Thickness control of thin InGaAs layers. The diffusion limited growth of ternaries from a melt of finite size is simulated and compared with experiments.
- 5) The growth of InGaAs at very low (500 °C) temperature.
- 6) Restrictions in the growth of InGaAs and InGaAsP caused by the miscibility gap.
- 7) The melt-back problem in the growth of InP on top of InGaAs(P).

It is concluded that LPE is a versatile method but due to limited thickness control (especially for devices III and IV) has to be considered as a laboratory method.



High power high efficiency MOCVD grown

InP Gunn diodes for 94 GHz

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InP Gunn diodes have been fabricated by low pressure metal organic V.P.E.

These diodes were based on a three layer $N^+ N N^+$ structure where Si (from Silane) was used as the dopant. This dopant allows a precise doping control which enabled us to compare various doping profiles.

An integral heat sink technology was developed to produce several well controlled mesa diameters in the 30 or 60 microns range for eventual production type quantities.

Diode chips were mounted in standard W3 packages using several different bounding wire geometries.

The paper describes the effects on device characteristics of the important parameters such as : epitaxial structure, technology, bounding.

Power levels in excess of 50 mw were obtained at 94 GHz with an efficiency of 3 % while an optimized structure up to 75 mw has been obtained with an efficiency of 2.4 %.

Millimeterwave GaAs Impatt diodes

Freyer, J. and Zhang, X. *)

The design and fabrication as well as the performances of $p^{+}nn^{+}$ GaAs single drift Impatt diodes for V-band frequencies are described. The drift velocity of electrons - an important factor in the diode design - has been determined by space charge resistance measurements for highly doped GaAs material ($0.6 - 2.0 \cdot 10^{17} \text{ cm}^{-3}$). It is found that the saturated velocity of $6.5 \times 10^6 \text{ cm/s}$ which has been used successfully at lower frequencies cannot be applied for the mm-wave Impatt diode design. Depending on the doping concentration a velocity between 4.4 and $2.8 \times 10^6 \text{ cm/s}$ has to be taken into account for V-band diodes at an operation temperature of 500 K.

The devices are fabricated using molecular beam epitaxy GaAs material which offers an extremely fine control of the epitaxial layer thickness and doping concentration. The diodes are thermocompression bonded on diamond heat sinks and packaged using quartz stand-offs to obtain low parasitics.

The maximum output power of the single drift devices is 0.7 W at 53 GHz and the maximum conversion efficiency is between 10 and 12.5 % in the V-band. At 72 GHz an output power of 0.35 W with 10 % efficiency could be realized. The diodes exhibit an excellent noise behaviour and a minimum noise measure of less than 24 dB at 60 GHz enables these diodes to be applied as local oscillators.

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W-Band IMPATT Diodes Made From Si-MBE Material

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Single-drift Impatt diodes have been fabricated from Si-MBE material for CW and pulse operation at 90 GHz.

N-layers with doping levels in the range of $1-2 \times 10^{17} \text{ cm}^{-3}$ were grown at growth temperatures ranging from 550 °C to 750 °C on commercially available n^+ -substrates. The p^+ -contact layer was either formed by a shallow diffusion of boron or for comparison also grown by molecular-beam epitaxy.

The IMPATT's are then fabricated in the same way like diodes from LPCVD-material made in our laboratory /1/.

Doping profile was measured for each wafer by Spreading Resistance Probe as well as by C(V)-Method. RF-measurements in a reduced height waveguide circuit allow further characterization and comparison with diodes made from LPCVD-material. Output power and efficiency are given as function of epitaxial layer properties and diode dimensions.

/1/ W. Behr

90 GHz Single-Drift IMPATT Diodes With High Output Power Level
14th EMC 1984, Liege

COMPOUND SEMICONDUCTORS FOR MILLIMETRE-WAVE

IMPATT DIODES

Sorin Voinigescu, Dan Dascălu⁺)

An analysis of GaAs, InP and In_{0.53}Ga_{0.47}As for mm-wave IMPATT diodes fabrication is presented. The focus is set on InP as the best material to compete with Si in the frequency ranges beyond GaAs capabilities. The comparative study of InP and Si is carried out for conventional SDR (Single-Drift-Region) and DDR (Double-Drift-Region) IMPATT diodes as well as for the newly proposed DAR (Double-Avalanche-Region) IMPATT. Promising computer simulation results have been obtained for DAR-IMPATT diodes as compared to those for the DDR structure. The 1.5 times higher merit factor (the $P_m f^2 X_{cl}$ product), usual efficiencies in excess of 45% and flexibility of design forecast an attractive future for Si and InP DARs especially at and around 100 GHz. For the first time, methods based on ion implantation or MBE are suggested for the fabrication of Si and InP DAR-IMPATT diodes. InP is confirmed as having considerably higher (2-3 times) power yields than Si at similar operational frequencies, irrespective of the type of IMPATT diode considered.

Finally a SDR-IMPATT InP-In_{0.53}Ga_{0.47}As heterostructure is proposed. This diode allows for very deep depletion-zone length modulation with a significant gain in efficiency. 90% of the drift zone is made up by an InP layer with the remainder of In_{0.53}Ga_{0.47}As which has higher negative differential mobilities in the lower field range. High power requirements make it imperative that the avalanche region be made of InP. This structure could be very competitive at the lower mm-wave frequencies.

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PROGRESS TOWARDS PERFORMANCE LIMITS FOR MODFET AND HBJT DEVICES

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ABSTRACT

Results on HBJT's and short gate length MODFET's made from AlGaAs/GaAs are reported. The performance of .3 micron gate GaAs MODFET's will be presented, in which state of the transconductances of 400 mS/mm at room temperature and 550 mS/mm at 77K were obtained with enhancement mode devices, which correspond to d.c. saturation velocities of 2.1×10^7 and 3.1×10^7 cm/S respectively. Using the small signal model calculated from the measured s-parameters of these devices, a value of f_T in excess of 70 GHz was calculated. With an AlGaAs buffer layer under a GaAs quantum well of 130 Å, state of the art measured noise temperature of 10.5K at 10K crystal temperature has been obtained at 8 GHz.

In the case of the HBJT, modifications in device processing have produced devices with values of f_{max} in excess of 9 GHz for devices with $f_T = 11$ GHz.

Work supported by AFOSR, ONR, ARO, NRAO of NSF, IBM, GE, McDonnell Douglas, U.S. Siemens, Honeywell and AT&T Bell Laboratory.

LOW NOISE K BAND SUB-MICRON FET SHOWING 0.8 dB NOISE FIGURE AT 77°K

I. Davies, R. Bennett, D. Brambley, J. Joshi, A. Powell and C. Oxley

To achieve optimum high frequency performance of GaAs FETs it is necessary to assess and minimise various parasitic elements associated with the transistor in addition to reducing device gate lengths. These elements within the FET structure are analysed and the design philosophy of a high frequency low noise 0.3µm gate length device will be described in detail. The fabrication of the gate electrode using electron beam lithography is also described. The room temperature performance of these devices indicated noise figures of 2.2 dB with associated gain of >9 dB at 23 GHz, while at 77°K a noise figure of 0.8 dB was obtained with greater than 9 dB of associated gain.

The noise theories of Pucel and Fukui have been used to examine the effects of device structure and fabrication technology on the noise performance of FETs. The major parameters which affect the r.f. performance of a GaAs FET are gate length, gate metallisation, loss source resistance, and source inductance.

For high frequency operation the FT of the transistor requires to be as high as possible and this can be achieved by reducing the gate length of the transistor. The use of electron beam lithographic techniques have provided a high yield process which is capable of reproducibly realising 0.3µm gate features.

The noise contribution from gate metallisation loss is dependent upon gate length, unit gate width, gate metallisation thickness and metal conductivity. The effect of these gate parameters on the noise performance have been studied up to 34 GHz.

In order to minimise the source parasitic resistance a self aligned etched gate technology has been adopted. The use of an n⁺ contact material structure minimises both the contact resistance and the layer resistance in the gate to source gap.

The gain of the device can be increased by raising the transconductance of the transistor. This parameter is a function of both device geometry and material parameters. Devices have been fabricated with transconductances greater than 240 mS/mm. A study of these parameters has been made and a device structure designed with particular attention to minimise source inductance and gate bond pad capacitance.

The r.f. performance of these devices has been measured throughout K band. Associated gains of >9 dB at 23 GHz and >7 dB at 27 GHz with noise figures of 2.2 dB and 3 dB respectively have been measured. The low temperature performance has also been assessed and a noise figure of 0.8 dB with greater than 9 dB of associated gain has been seen.

Some Design Considerations of the Optimized Performance of
Self-Aligned GaAs MESFET's

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There are two important aspects in the design and process of high speed GaAs IC: i) optimized design of GaAs MESFET's for the highest speed operation and ii) minimized spreading of device parameters, particularly the threshold voltage, for the appropriate operation of IC.

In this paper, considering that a particular feature inherent to GaAs MESFET's is the depletion layer under the free surface between source and gate as well as gate and drain, the effect of this depletion layer on series resistance and input capacitance of self-aligned GaAs MESFET's is discussed quantitatively based on a new model.¹⁾ It is then pointed out that an optimized dose and acceleration energy to form the ion-implanted n^+ -layer should be selected for the high speed operation.

A passivation layer deposited over GaAs surface before ion-implantation is sometimes preferred for the stabilized process and for the increase of g_m by shifting the position of maximum doping density toward the surface. The effect of implantation conditions on this structure is also discussed with the effects on the spreading of threshold voltage.

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A 0.5 μ m LOW NOISE GaAs FET FOR APPLICATIONS IN THE KA BAND*

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The device design has been optimized for a maximum gain in the Ka band using the CAD analysis reported in (1). The resulting structure consists of three T-shaped aligned gates, leading to a 75 μ m total gate width. The most important point is a reduced unit gate width of 12.5 μ m, in order to minimize both the input impedance mismatch loss at 30 GHz, and the gate series resistance which is one of the most critical parameters for gain as well as noise figure. Source contacts are connected by air bridges over the gate feeders. This device has been fabricated on both VPE and ion implanted materials in a recessed channel technology. A standard mid-UV photolithography has been used, yielding 0.5 μ m gate length with 80 % efficiency. Two test fixtures with different waveguide to microstrip transitions have been designed to evaluate the device in the Ka band. One consists of an antipodal finline transformer while the other is similar to the common waveguide to coaxial transition. Both have yielded good results. Biased for maximum gain, the amplifier including the VPE device exhibited 8.0 dB gain at 30 GHz. Noise measurements showed 4.6 dB noise figure with 7.1 dB associated gain. These are among the best results ever reported at 30 GHz for 0.5 μ m gate MESFET's.

- (1) P. BAUDET, C. VENET, C. ROCHER, "Optimized Pattern Design for Power GaAs MESFET", Proceedings ESSDERC 83, vol. E7, pp. 77-79

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•• THOMSON-CSF

Laboratoire Central de Recherches

ULTRA LOW NOISE AND HIGH FREQUENCY MICROWAVE OPERATION OF FETs

MADE BY MBE

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Both conventional FET structures and $n\text{-AlGaAs/GaAs}$ TEGFET (Two-dimensional Electron Gas FET) heterostructures have been grown at 600°C by molecular beam epitaxy on two inch diameter wafers.

Using a simple and fast processing technology based on optical and E-beam lithography, TEGFET structures with gatelengths of 0.5 microns have been made.

For 300 microns gatewidth TEGFETs, a 10 GHz noise figure of 1.25 dB with 11 dB of associated gain was obtained. At 17.5 GHz this device gives a noise figure of 1.9 dB at room temperature falling to 0.4 dB at 80K ($G_{\text{ass}} = 9.6$ dB, $MAG = 14.4$ dB).

An optimisation of device geometry with gatewidths of 140 microns improves the room temperature performance to 1 dB noise figure at 10 GHz and 1.5 dB at 17.5 GHz.

Classical FET MBE structures using the optimised 140 micron geometry have given 2 dB noise figure with 10.2 dB of associated gain at 17.5 GHz.

The fabrication of the two types of transistors will be described and the results will be analysed in terms of a comparison of the different structures used.

The TEGFET results for 0.5 μm gatelength devices are comparable with those published for 0.25 μm gatelength MESFETs.

CHARACTERIZATION OF ELECTRON WIND VOIDING OF GaAs FET METALLIZATION IN VIEW
OF DEVICE LIFETIME LIMITATIONS

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An often found lifetime limitation for GaAs FETs is caused by breakage in gate metallizations due to the so-called electron wind effect when high electric current densities are flowing. Experimental results are therefore to be reported here on the characterization of typical narrow thin film gate structures regarding the transport of material.

The two experimental approaches employed are a measurement of the 'Mean Time to Failure' (MTF) based on the statistics of structures failing completely, and the less destructive 'Resistometric Technique' where changes of resistance are monitored between probes.

The results indicate that electrode voiding occurs preferentially at geometric irregularities such as corners or the transitions from bonding pads.

Activation energies of electromigration for Al electrodes with Cr interfaces were obtained for semiinsulating GaAs and glass substrates. Whereas in the former case a low activation energy of 0.14 eV was obtained, the latter system showed a value of 0.37 eV. In the former case the magnitude of material transport was, however, smaller than in the latter one. When the Cr interface was omitted in the latter case the activation energy increased to 0.46 eV.

It can be concluded from these results that the temperature dependence of this detrimental phenomenon is not very strong for the sandwich of Al/Cr/GaAs and that this lifetime process is not only limited to the higher temperature of operation. The inclusion of Cr seems to reduce the activation energy.

Further work is now in progress of evaluating the effect of surface treatment of the GaAs before deposition of the narrow electrode structures.

Recent Japanese Developments of High-Speed Devices
by Non-MESFET Approaches

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Although the self-aligned version of the "classical" MESFET has been extremely successful for integration, achieving LSI complexities, intensive efforts are also being made towards high-speed devices by non-MESFET approaches in order to exploit the potential speed capability in compound semiconductor materials to its fullest extent. This paper reviews the current status of such efforts made in Japan, including HEMTs, MIS-like FETs, HBTs and HETs and InP MISFETs.

HEMTs have now achieved LSI complexity, resulting in a subnanosecond 1kb SRAM with 4kb version being pursued. Process control and photo-induced instability of V_{th} , compatibility with implantation for self-alignment are the major issues. Use of AlAs/GaAs SL reduces DX centers and improves the stability. The MIS-like FET using undoped AlGaAs semi-insulator is an attractive alternative to the HEMT structure for 77K operation.

For realization of high-speeds in LSI complexity, large driving capability of devices is an essential requirement. Thus, the HBT gate is a natural extension of Si ECLs. A discrete device with f_t of 25 GHz has recently been fabricated and its integration is now being pursued. Tunneling HET is expected to achieve subpicosecond operation.

Since the FET current is determined by velocity $\times$ sheet carrier concentration, InP and InGaAs MISFETs can potentially offer advantages of large drivability, less tight control of V_{th} and large N.M. for room temperature operation. Reduced drain current instability with a high channel mobility has recently been obtained.

VERTICAL HETEROJUNCTION FET STRUCTURE WITH 100 nm SOURCE TO GATE SPACING

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To achieve mm-wave performance from GaAs FET's, active device geometries must be of nanometer dimension. These include gate length, channel length and width, source-drain spacing, and gate-to-gate source spacing. The vertical FET has been shown to be particularly suited to obtain these geometries [1]. Additionally, performance at mm-wave frequencies requires enhanced electron velocity such as may be obtained by the use of a GaAs/AlGaAs heterojunction ballistic electron launcher. Again, the vertical FET is particularly amenable to the incorporation of such a source structure.

Previously fabricated vertical FET's incorporating an AlGaAs cathode [2] have utilized a source finger overhang structure consisting of the source ohmic metallization only and in which the gate is defined by a dual-angle shadow evaporation. The fabrication scheme and results obtained for this structure will be reviewed. To date, the performance of these devices has not met expectations due in part to two limitations of the above process: 1) preferential etching of the AlGaAs during the undercut etch degrades source performance, and 2) the angle of the gate evaporation is critical and therefore nanometer source-to-gate spacing cannot be reliably obtained.

A new vertical heterojunction FET structure is proposed which overcomes these limitations. In this structure both the source metallization and the source AlGaAs electron launcher system have been used as the overhang. Gate-to-source spacings of ~ 100 nm are achieved by a self-aligned "rotating" shadow evaporation (Fig. 1). The fabrication scheme developed to obtain the desired finger cross section will be presented along with geometries obtained to date (Fig. 2). Additional device design changes necessitated by the new fabrication scheme will be discussed.

This work was supported by DARPA under contract N66001-83-C-

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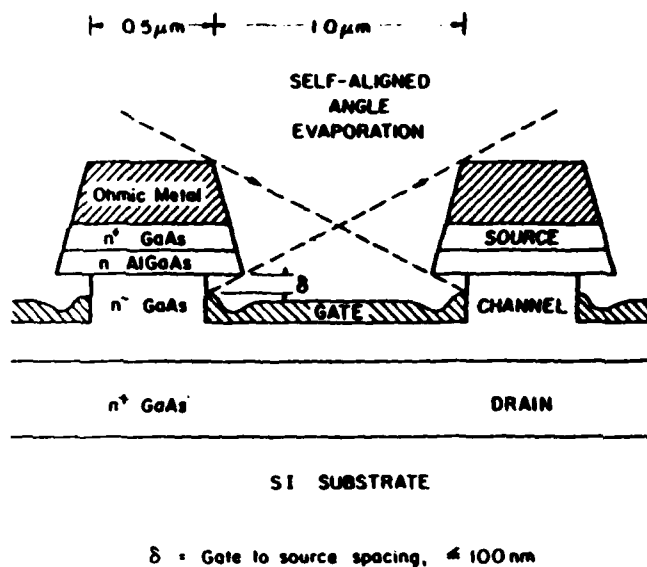


Figure 1. Scale drawing of desired device cross section.



Figure 2. SEM micrograph showing finger cross section.

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DRIFTING PHENOMENA IN POWER FET'S

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A new or at least unknown drifting phenomenon has been detected in medium power (0.5 W) FET's operated as direct oscillators.

The drift characteristics were:

- Frequency drift "upward"
- Drain current decrease
- Gate current increasing in forward direction

The above drift could be induced or not, depending on biasing conditions. Conclusions drawn so far indicate a change in donor concentration between gate and drain to be the cause of said drift.

More details will be provided at Workshop.

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TUNGSTEN SILICIDE SCHOTTKY DIODES FOR GaAs MESFETS

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Tungsten silicide Schottky diodes have been reported¹ to have stable electrical characteristics even after heat treatment at 800°C. This makes them eminently suitable for use as ion implantation masks in a self aligned gate technology for GaAs MESFETS as they will withstand the subsequent implant activation annealing procedure. It is for that reason that we have undertaken an investigation to evaluate their usefulness in an enhancement-depletion MESFET technology. Tungsten silicide of varying composition has been deposited by ion beam and r.f. sputtering using pressed powder or composite elemental targets and a variety of encapsulation techniques (Si_3N_4 , GaAs proximity cap etc.) have been used for the high temperature annealing of the wafers. Schottky diode characteristics have been measured after heat treatment at 800°C with ideality factors of 1.23 and barrier heights of 0.75eV. The main problems have been associated with stress in the films [causing them to peel from the GaAs surface for certain silicide compositions] and the high resistivity of the deposited films. Results will be presented on the optimum composition and annealing procedure and comparisons made with tungsten silicide deposited in a commercial LPCVD reactor. Further work is being carried out to improve the uniformity of the diode characteristics in order to make them suitable for use in an ISL technology.

1 Yokoyama et al., 1983 IEEE International Solid State Circuits Conference paper WAM.3.4

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MBE Growth of Strained-Layer Superlattice Material
for High Speed FETs*

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Strained-layer superlattice (SLS) structures allow the use of mismatched semiconductor alloys without the accumulation of strain energy sufficient to cause the generation of misfit dislocations. This freedom from the need for precise lattice matching of the superlattice components greatly broadens the choice of compatible superlattice alloys, and increases the ability to tailor electronic and optical properties in such structures. Two attractive features of the $\text{In}_x\text{Ga}_{1-x}\text{As}$ SLS system are the ability to tune the energy gap to suitable values and the ability to enhance carrier transport properties by suitable doping profiles. This talk will emphasize recent results in the MBE growth and doping of $\text{In}_{.2}\text{Ga}_{.8}\text{As}/\text{GaAs}$ SLS structures and their incorporation into prototype FET devices.

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High Speed Digital IC Performance Outlook

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To meet the functional throughput requirements of future high speed signal processing systems and commercial computers, GaAs digital integrated circuits are being developed. Applications for frequency counters, correlators, multiplexers, demultiplexers, time interval counters, and A/D converters with on-chip clock frequencies exceeding 1 GHz exist in the near-term. Such circuits are of MSI complexity, several hundred gate equivalents. Future applications for high speed IC's in more complex computational systems, such as radar signal processors, will require static random access memories, read only memories, high density logic arrays, and special purpose chips such as the multiplexers used in fast Fourier transform processors. For these future applications integration levels exceeding 1000 gates per chip are essential. In these advanced signal processors, the required system clock speed will be in the range from 250 MHz to 2.5 GHz.

Logic gates with tens of picosecond gate delay, tens of micro-watts power dissipation, cryogenic to hundreds °C operating temperatures and greater than 10^7 rads radiation tolerance, will provide performance enhancements of one to two orders of magnitude for digital communications, memories and computers. The implementation of this technology in MSI/LSI chips requires stringent control on material and process parameters for tight tolerances on device and circuit characteristics and high yields, and extremely short gate delays with large fanouts and low power dissipation for increased throughput rates.

In order to assess GaAs technology, this talk reviews the device technology and issues related to device/circuit design and fabrication of MSI/LSI complexity circuits operating at gigahertz clock frequencies, discusses limitations of the technology, compares with competing Si technologies, and presents applications where the technology will have a significant impact.

GaAs HIGH SPEED, LOW POWER DIGITAL IC's*

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After ten years of research activity on GaAs digital IC's, basic questions such as : why GaAs, when and for what applications, can now be answered rather accurately. First, the state of the art in GaAs digital IC's is reviewed and then the advantage of GaAs over silicon for digital applications is updated.

Material and process refinements have gradually made N-off DCFL, the most promising GaAs approach for (V)LSI circuits.

For fast interfaces of SSI/MSI complexity such as multiplexers and prescalers up to 10 GHz, N-on GaAs circuits (SDFL, BFL) are still an alternative to DCFL, but at the 1000 gate level and above, DCFL is today almost unchallenged and has enabled to fabricate 3000 gate-16 x 16 bit parallel multipliers (10 ns/1 W) and fast SRAM's (1 K : 1.3 ns/ 300 mW ; 4 K : 3 ns/700 mW and 16 K : 5 ns/2 W).

Simultaneously, new devices, mainly based on heterostructures, have been fabricated (HEMT's, heterobipolar transistor...). These devices are expected to outdo the conventional MESFET in speed performance. For instance a HEMT-1 K SRAM has exhibited 0.9 ns access time at 77°K with 360 mW power consumption.

Scaling down of silicon MOS and bipolar circuits to submicron design rules, has made it possible to evaluate the advantage of GaAs over Si experimentally. For fast, low power ($P \leq 1$ mW/gate, $t_{pd} \leq 250$ ps/gate) LSI applications 0.6 μ m DCFL circuits have been showed to be 2.5 to 3 times as fast as 0.6 μ m channel length silicon NMOS and consume 10 times less power at the maximum speed of the NMOS circuit. These results apply approximately to ECL and CMOS circuits for continuously operated systems.

The power consumption advantage is of prime importance for the near future of GaAs IC's since it addresses a field of applications where a real market already exists and where users have to make do with the high power consumption of today's ECL IC's.

REALIZATION OF COMPLEMENTARY GaAs JFET CIRCUITS

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The purpose of this paper is to report and describe the double ion-implanted GaAs n-channel and p-channel enhancement mode junction field-effect transistor (JFET) and its application to the design of complementary low power integrated circuits. This complementary inverter design is not readily available with MES-FETs because of the difficulty in forming Schottky barriers to the p-type channel material.

In Si complementary circuits the ratio of effective channel electron and hole mobility is about 2 to 3, making complementary circuits more attractive for high speed operation. For GaAs integrated circuits the complementary design with a hole mobility of about $300 \text{ cm}^2/\text{Vs}$ and an electron mobility of $3500 \text{ cm}^2/\text{Vs}$ is primarily useful when a power consumption reduction is required. The application of this new GaAs complementary circuitry to the design of an ultra low-power static 256-bit RAM will be demonstrated. The fully operational and decoded RAM has an access time of 5 ns and a memory stack standby power of 100 nW/cell.

A Synchronized Clock Generator for 6 Gbit/s
Signal Regeneration

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To fully exploit the modulation possibilities of semiconductor lasers at several Gbit/s, data streams have to be multiplexed. Clock pulses have been produced with 6 Gbit/s repetition rate, 53 ps FWHM and 6 V peak in a 50Ω system, improving timing and pulse shape of a 1-to-6 Gbit/s multiplexer.

The clock generator extracts the 6th harmonic from the system's 1GHz synchronization source through a filter that is broadband matched at the input, amplifies this signal in three stages and shapes it by overdriving a final MESFET stage. Hence the output pulses are phase-locked to the bit stream. The subsequent regeneration of the multiplexer's output is done in a dual-gate MESFET acting as a NAND gate.

The circuit is constructed on five $1'' \times 1'' \text{Al}_2\text{O}_3$ substrates. It uses interstage band pass filters suppressing the "sidebands" at 5 and 7 GHz which would show up as a 1 GHz amplitude modulation in the time domain.

Additional stubs provide the matching between subsequent stages.

The system presented can also be used to regenerate time and pulse shape of received data from a fiber link, if synchronisation can be provided.

InGaAs-JFETs with p^+ -Gates made by diffusion from spin-on films.

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In_{0.53}Ga_{0.47}As is a favourable semiconductor for microwave devices and for amplifiers in integrated optoelectronic circuits because of the high electron mobility and the compatibility with optoelectronic devices in the long-wavelength optical communication systems. Because of the low Schottky-barrier, InGaAs MESFETs cannot be fabricated, but MISFETs and JFETs are suitable devices. In this paper the development of a process for making highly doped p^+n -junctions, the properties of the junctions and the characteristics of JFETs using these junctions are described. The highly doped p^+ -regions are obtained by an easy-to-handle open tube diffusion process. A solid diffusion source ($\text{SiO}_2\text{:Zn}$) is formed from a spin-on emulsion. The process is performed in a nitrogen purged open tube at temperatures, which are low enough to prevent any long-range tails in the dopant profiles and substrate conversion. The available hole concentration is controlled by the process temperature and is more than 10^{19}cm^{-3} for diffusion temperatures of 600°C . The electrical properties of the p^+n -diodes are close to theoretical values.

For the fabrication of the JFETs a selective diffusion through a sputter deposited silicon nitride mask forms the p^+ -gates. InGaAs-JFETs with $10\mu\text{m}$ gate length and a channel doping of $N_D=10^{17}\text{cm}^{-3}$ have shown transconductances up to 70mS/mm . By linearly scaling down to $1\mu\text{m}$ gate length and simultaneous optimization of the device, transconductances up to 700mS/mm should be expected. Therefore it is concluded that the diffusion from solid sources is either an attractive, since simple and economic alternative or a complementary process to ion implantation.

Optoelectronic ICs based on InGaAsP/InP:
Concepts, problems and prospects

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While most of the current research on optoelectronic ICs (OEICs) is focussed on GaAs/GaAlAs for applications in local networks, in fast computers and in fiber sensors, similar concepts based on InGaAsP/InP will have an important impact on optical communication systems operating at 1.3 - 1.6 μ m wavelength. Here, the first task will be the integration of the photodetector with the front end amplifier which will lead to reduced parasitics, improved signal interference immunity and reduced cost. A less urgent need is the driver-laser integration which gives advantages in the laser impedance matching. The potential and limitations of such OEIC concepts will be discussed in this contribution.

For the implementation in the integrated photoreceiver, the pin photodiode will be favoured, as the APD has too stringent material requirements and the photoconductive device needs a high light intensity for trap saturation demanding expensive focussing. We will compare the following front end designs: JFET (high g_m/C_g is difficult to obtain), MISFET (sufficient g_m/C_g , low leakage current, but drift problems), selectively doped heterostructure FET (high g_m/C_g) and heterostructure bipolar transistor (high current gain, excellent threshold uniformity and stability, but very demanding in technological aspects). For the driver-laser integration the double heterostructure bipolar transistor is the natural choice considering the material compatibility and the current driving capability.

The most pressing problems for the realization of these OEIC concepts are the lack of self-registration techniques allowing 1 - 2 μ m design rules and the need for mesa structuring. Therefore, the performance of present experimental OEICs is falling far behind their hybrid counterparts. By exploiting techniques using ion implantation combined with flash annealing an essential progress is foreseeable.

**Integrated Photoconductive Detector/FET GaAs Receivers
with Simple Optical Coupling to Optical Fibers
for Interconnections in Very High Speed IC's**

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In order to meet the need for high speed, cross-talk free interconnections in high speed IC's, integration of high-speed GaAs photoconductive detectors and MESFETs with simple coupling to optical fibers is investigated.

Two photoconductive detectors and one FET were integrated on a 0.2 μm thick n-type MOCVD GaAs layer doped to $2 \times 10^{17} \text{ cm}^{-3}$ grown on a semi-insulating GaAs substrate. Photoconductors had width of 200 μm and length of 10 μm . Gate length of the MESFET was 10 μm and width 500 μm .

For simple coupling of optical fibers to the integrated receiver, a single mode fiber was laid directly on one of the detectors and coated with epoxy resin. To enhance the efficiency of distributed coupling between fiber and detector, optical fiber was etched to 5 μm to remove the coating and cladding. The resulting connection loss between fiber and detector was about -1.4 dB with 5 ns overall response time, which is excellent considering the very simple method and structure employed here. The response time is limited by the surface state effect of the detector and can be improved by employing window layers such as GaAlAs.

Monolithic integration of photoconductive detectors with GaAs MESFETs together with a simple and low-loss coupling of optical fibers to the integrated high speed receivers are thus shown to be very promising for optical interconnection in very high speed IC's and systems.

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Characterization of Devices Employing Multilayer Quaternary Materials

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Quaternary alloy semiconductor materials of the form $\text{In}_{1-x}\text{Ga}_x\text{As}_{1-y}\text{P}_y$ are of considerable interest for microwave and opto-electronic devices in that they may be grown on such substrates as InP and permit the independent selection of lattice parameter and energy gap. Devices may benefit from the incorporation of several layers of such materials, epitaxially grown, each of a different specific band gap whilst remaining lattice-matched to the substrates, in order to avoid the creation of mis-fit dislocations. An important requirement has been for the development of a non-destructive technique to evaluate accurately lattice parameter mismatches occurring at the epitaxial layer interfaces.

Such a technique has been established involving an automated double-axis X-ray diffraction method, based on the S.E.R.C. synchrotron beam facility at Daresbury. Rocking curves are obtained for each specimen, which represent the angular variation of reflected radiation intensity from the specimen under defined geometrical conditions. From these curves it is possible to study compositional and thickness variations of the epitaxial layers as well as lattice parameter mismatches of the order 10^{-4} . Work is in hand on the computer simulation of the rocking curves. Comparison of experimental and predicted rocking curves enables growth conditions to be determined.

Application of Be ion implantation to GaInAs junction FETs

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Ga_{0.47}In_{0.53}As junction FETs are of high interest because of the high electron mobility and because of the low barrier height of Schottky contacts to n-material which restricts the application to conventional MESFETs. We fabricated JFETs by ion implantation of 10 or 30 keV Be into n-GaInAs. Usual annealing techniques (typical at 650°C) resulted in considerable diffusion of the Be into the bulk and an outdiffusion into the capping SiO₂ layer. Activations between 10 and 50% of the implanted Be were achieved depending on the implantation and annealing conditions. First JFETs were made on rather low doped GaInAs with an 10 keV Be-implantation and 4 μm gate length. Transconductances of about 25 mS/mm were achieved and the channel mobilities deduced from magneto-transconductance measurements at the complete device were up to 8000 cm²/Vs depending on the applied gate voltage. High frequency measurements made on this not optimized structure with high channel resistance gave a cut off frequency of 2 GHz. The annealing procedure was improved by use of a rapid thermal annealing within seconds. This resulted in very steep profiles with nearly no diffusion, high activation and high hole mobilities. This allows the very controllable application of Be-implantation to GaInAs JFETs with effective gate lengths in the submicron range.

Low Pressure Halide Growth of Epitaxial InP for Microwave Devices

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For the successful fabrication of microwave devices thin layered structures with well defined film thickness and uniform properties are required. It has been shown earlier for the growth of GaAs that thickness control and uniformity can be improved by reducing the total system pressure.

In this paper we will discuss the low pressure growth of InP in the In-HCl-PH₃-H₂ system. The effects of epitaxial parameters on the growth rate are similar to those observed in the case of GaAs deposition. In agreement with model considerations the rate decreases almost linearly with decreasing H₂ pressure. At a pressure of 13 kPa the rate of 2 $\mu\text{m/h}$ can be reproducibly adjusted, thus allowing the controlled growth even of submicron layers at such conditions. An increased phosphorus pressure is required to obtain perfect surface morphology during low pressure growth. Background electron concentrations lower than 10^{15} cm^{-3} could be achieved. For the intentional preparation of n-type material $\text{Te}(\text{C}_2\text{H}_5)_2$ has been used as the doping source. Improved uniformity of Te distribution and thickness of epitaxial layers could be achieved upon pressure reduction as indicated by the saturation current and pinch off voltage data measured at FET structures distributed over layers with an area of $1.5 \times 1.5 \text{ cm}^2$. SIMS data on the abruptness of Te profiles will be presented.

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InGaAs/InP Heterobipolar Transistors on Semiinsulating InP

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For very fast electronic circuits $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ is a promising material due to its high electron mobility and high peak drift velocity. Combined with the wide gap material InP, most favourable devices such as hetero-junction bipolar transistors (HBT's) can be realized.

We report on results of npn-HBT's made from LPE layers grown on semiinsulating (s.i.) InP-substrates. These substrates used here suffer from a very high defect density in comparison to the low resistivity substrates up to now used for the fabrication of InGaAs/InP-HBT's. However, to obtain a maximum flexibility in device and circuit design the use of s.i.-substrates is advantageous.

The design in emitter down configuration enables the straight forward growth of the layer sequence n-InP/p-InGaAs/n-InGaAs without the necessity for an anti-meltback layer. The devices were fabricated in mesa technique using wet chemical etching. The collector areas rang from $20 \times 35 \mu\text{m}^2$ to $40 \times 150 \mu\text{m}^2$. The devices were coated with SiO_2 . Interconnections lead from the ohmic contacts of the mesa device to bond pads on the s.i.-substrate.

The HBT's show stable characteristics without any hysteresis, low values of output conductance, low turn-on voltages and sufficiently high break-through voltages.. Current gains up to 25 are obtained for a fairly thick base of $0.7 \mu\text{m}$. The devices usually have higher gains in the reverse direction. It hints to the necessity of further improvements of the homo- and hetero-junction. Their quality is strongly affected by the high defect density of the s.i. InP-substrates.

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