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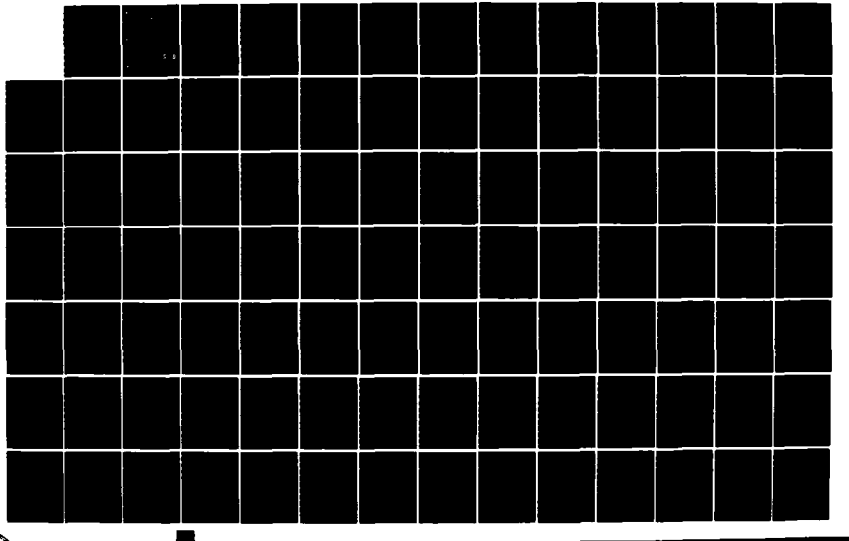

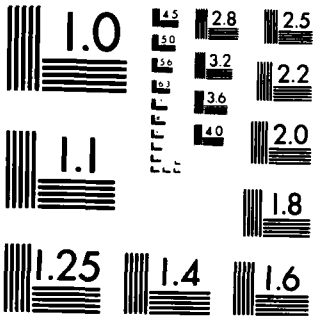

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ANALYSIS OF THE CAPABILITY TO EFFECTIVELY DESIGN COMPLEMENTARY METAL OXIDE SEMICONDUCTOR INTEGRATED CIRCUITS

THESIS

Michael L. McConkey
Second Lieutenant, USAF

AFIT/GE/ENG/84D-44

DEPARTMENT OF THE AIR FORCE
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Wright-Patterson Air Force Base, Ohio

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THESIS

Presented to the Faculty of the School of Engineering
of the Air Force Institute of Technology
Air University
In Partial Fulfillment of the
Requirements for the Degree of
Master of Science in Electrical Engineering

Michael L. McConkey, B.S.
Second Lieutenant, USAF

December 1984

Preface

This project was undertaken with the intent of acquiring a knowledge base of the available tools with which to do CMOS/BULK design work. This knowledge base includes the "how to" of each tool to ease the frustration that a designer might experience (and avoid the frustration that I experienced). The easiest tools to use are the ones that are presented in the pages of this thesis.

The CMOS/BULK library that was put together is by no means complete, but it gives the designer a head start and hopefully will tickle his imagination to add new cells and perhaps better versions of the old ones.

I would like to thank my thesis advisor, Bill Sutton, for his invaluable help, guidance, and draft reviews in completing this project. I would also like to thank Hal Carter and Joe Hamlin for their help in getting BANE up and running on the VAX 11/780.

Special thanks goes to my lovely new wife, Angela, for putting up with all of this.

Michael L. McConkey

Contents

List of Figures

List of Tables

Abstract

A complete CMOS/BULK design cycle has been implemented and fully tested to evaluate its effectiveness as a viable set of computer-aided design tools for the layout, verification, and simulation of CMOS/BULK integrated circuits. This design cycle is good for p-well, n-well, or twin-well structures, although current fabrication techniques available limit this to p-well only. BANE, an integrated layout program from Stanford, is at the center of this design cycle and was shown to be simple to use in the layout of CMOS integrated circuits (it can also be used to layout NMOS integrated circuits).

A "flowchart" was developed showing the design cycle from initial layout, through design verification, and to circuit simulation using NETLIST, PRESIM, and RNL from the University of Washington. A CMOS/BULK library was designed and includes logic gates that were designed and completely tested by following this "flowchart". Also designed was an arithmetic logic unit as a more complex test of the CMOS/BULK design cycle.

ANALYSIS OF THE CAPABILITY TO EFFECTIVELY DESIGN COMPLEMENTARY METAL OXIDE SEMICONDUCTOR INTEGRATED CIRCUITS

I. Introduction

Background

The Department of Defense has always been a major driving force behind the development of new and better technologies, and this is especially true in the field of microelectronics and integrated circuits. The development of integrated circuits and their successful use in military applications has had a great impact on the size, functions, and data processing capabilities of military systems such as aircraft, missiles, and satellites. But integrated circuit technology has been increasing steadily for commercial applications and not for military applications (1:273). Although integrated circuits that are targeted for the commercial market are somewhat reliable, they do not meet Department of Defense requirements in terms of "reliability, testability, immunity to environmental stress, and speed" (1:274). Because of this, the VHSIC program was created.

The VHSIC program (Very High Speed Integrated Circuits) was created in 1978 and was put into affect in 1980. It is a four phase program spanning over seven years. It is designed to meet the objective of developing advanced integrated circuits for use in future military systems

(1:276). The product of the VHSIC program will be integrated circuits with very high switching speeds, low power consumption, and radiation hardening. In order to get the high switching speeds, more and more transistors have to be packed onto the same integrated circuit. VLSI technology is capable of doing this. But increasing the number of transistors on the same circuit also increases the power consumption of the circuit. A trend towards the use of CMOS has developed to obtain both high switching speed and decreased power consumption. Also CMOS technology has a somewhat better radiation resistance than other leading transistor technologies (2:58).

Although CMOS is not the only viable technology for use in the VLSI/VHSIC programs, it is a proven technology. Some of the features that make CMOS desirable are as follows: (3)

1. Static power dissipation is extremely small.
2. Excellent noise immunity.
3. Faster than p-channel MOS.
4. TTL compatible.

Also dynamic CMOS circuits are comparable in speed and design complexity to the same type of circuit implemented in NMOS (4:480).

Currently, CMOS technology is being applied to microprocessors, RAMs, and analog devices such as operational amplifiers and analog-to-digital converters. Very large, 256K, RAMs have been designed by using dynamic

CMOS circuits where many n-channel transistors are used with just a few p-channel transistors, and there exists one design that uses an NMOS memory cell in conjunction with high performance CMOS periphery circuitry (10). In this way, all the benefits of CMOS are obtained with the high switching speed of NMOS. CMOS circuits are also ideally suited for analog applications because of the large voltage swing that CMOS can provide. Thus, analog and digital devices incorporating CMOS circuitry can be fabricated on the same integrated circuit.

Problem Statement

The purpose of this thesis is to provide an analysis of the capability to effectively generate CMOS integrated circuits at AFIT. Currently, only NMOS circuit generation exists, but computer-aided design tools for CMOS have recently arrived and are now on the VAX 11/780.

Scope

Because the CMOS computer-aided design tools are new, they will be studied to determine their effectiveness in generating integrated circuits. These tools include a descriptive chip layout language, a design rule checker, a circuit simulator, and a cell library. Each tool's effectiveness will be determined by actually designing an integrated circuit. This circuit will be a 4-bit arithmetic logic unit (ALU), and it will incorporate cells

from the cell library.

If these tools prove to be too cumbersome or even impossible to use, then the existing NMOS circuit generation techniques will be studied and modified for use in generating CMOS circuits. This study will include using the Stanford CLL (Chip Layout Language) to layout the circuit components, and then modifying the CIF (Cal-Tech Intermediate Form) files that are produced by the Stanford CLL. Also, if this approach is taken, compatibility between the CMOS cell library format and the Stanford CLL will have to be determined. If compatibility does not exist, then a new CMOS cell library will be developed using the Stanford CLL.

To provide some comparisons between CMOS and other technologies in VLSI, the ALU designed in this thesis will be compared to an ALU of the same design using CMOS/SOS technology. This CMOS/SOS ALU was designed by Wayne Sommars GE-83D (5).

To provide the necessary background, one chapter of this thesis will briefly present current CMOS technology plus new developments that are making this technology better. Also, differences between CMOS and CMOS/SOS will be presented. Throughout this thesis, CMOS will refer to bulk CMOS (silicon substrate) while CMOS/SOS (sapphire substrate) references will be made explicit.

Assumptions

In order to complete this thesis work in the time allowed, the following assumptions have to be made:

1. Pads suitable for use in CMOS integrated circuits are available. These pads will include VDD, ground, input, and output pads. The input and output pads should be TTL compatible.

2. The CMOS cell library contains the cells most frequently used in designing CMOS integrated circuits. These cells have been tested and perform according to design conventions.

Summary of Current Research

Much is already known about CMOS. It is a well documented technology that is just now being exploited for use in VLSI designs. Currently, research is being conducted to determine how to avoid an annoying problem called latch-up. Also, research is being conducted on how to increase the speed of CMOS logic to make it more desirable for VHSIC applications. Chapter II presents these items in more detail.

At AFIT, there is no research being conducted in CMOS technology merely because there has been no opportunity to do so. This thesis should open new doors for future researchers.

Approach

The approach of this thesis is straight-forward. A working knowledge of the available CMOS computer-aided

design tools will be assembled. This will include "flowcharts" to show how each tool relates to another in the total CMOS design process. A methodology based on this knowledge and on the design process presented in Mead and Conway (6) will then be produced for future AFIT students. If these tools are unsuitable for use, then a methodology based on the current NMOS computer-aided design tools will be produced. If time allows, then compatibility between these two sets of design tools will be analyzed. For example, using SPICE or MEXTRA (both NMOS analysis tools) on CMOS.

After the design methodology has been developed, then it will be implemented in designing a 4-bit ALU. The steps taken in this design should determine whether the developed design methodology is adequate for generating CMOS integrated circuits. The methodology will be strictly adhered to unless such circumstances dictate otherwise.

Sequence of Presentation

Chapter II presents a brief background and introduction of CMOS technology. Such items as latch-up and precharging are discussed. Comparisons between CMOS and NMOS, and between CMOS and CMOS/SOS are included. The emphasis in this chapter will be on current technological advancements in the area of CMOS.

Chapter III includes an introduction and synopsis of the CMOS computer-aided design tools. The use of each tool

is discussed. Also, the design methodology is presented in this chapter. The intent is for this chapter to be used as a tutorial in CMOS integrated circuit design for future AFIT students.

Chapter IV presents the design of the 4-bit ALU. The initial block diagrams, logic circuits, and circuit plots are included.

Chapter V presents the comparison between the CMOS ALU and the CMOS/SOS ALU designed by Sommars.

Chapter VI presents the recommendations and conclusions based on the research included in this thesis.

II. CMOS Technology

This chapter presents current advancements in the broad area of CMOS. The advancements included in this chapter are latch-up improvements, speed enhancements, design complexity improvements as compared to NMOS and CMOS/SOS, and current advancements in CMOS/SOS at AFIT. Before these advancements can be discussed, a brief overview of CMOS is necessary. The reader may wish to proceed to the next section if he is already familiar with this technology.

The CMOS Process

Complementary metal-oxide-semiconductor technology, CMOS, is currently one of the leading transistor logic families for VLSI design. Its low power consumption and excellent noise immunity make it ideally suited for integrated circuits whose design complexity requires more transistors to be packed on a given piece of substrate.

CMOS technology actually consists of two separate MOS technologies; that of p-channel MOS, PMOS, and n-channel MOS, NMOS. Conventional CMOS is known as bulk CMOS because it has a silicon substrate, as opposed to CMOS/SOS which has a sapphire substrate. There are three different possible structures for a CMOS transistor, and these are shown in Figure II-1. Typically, most CMOS circuits are

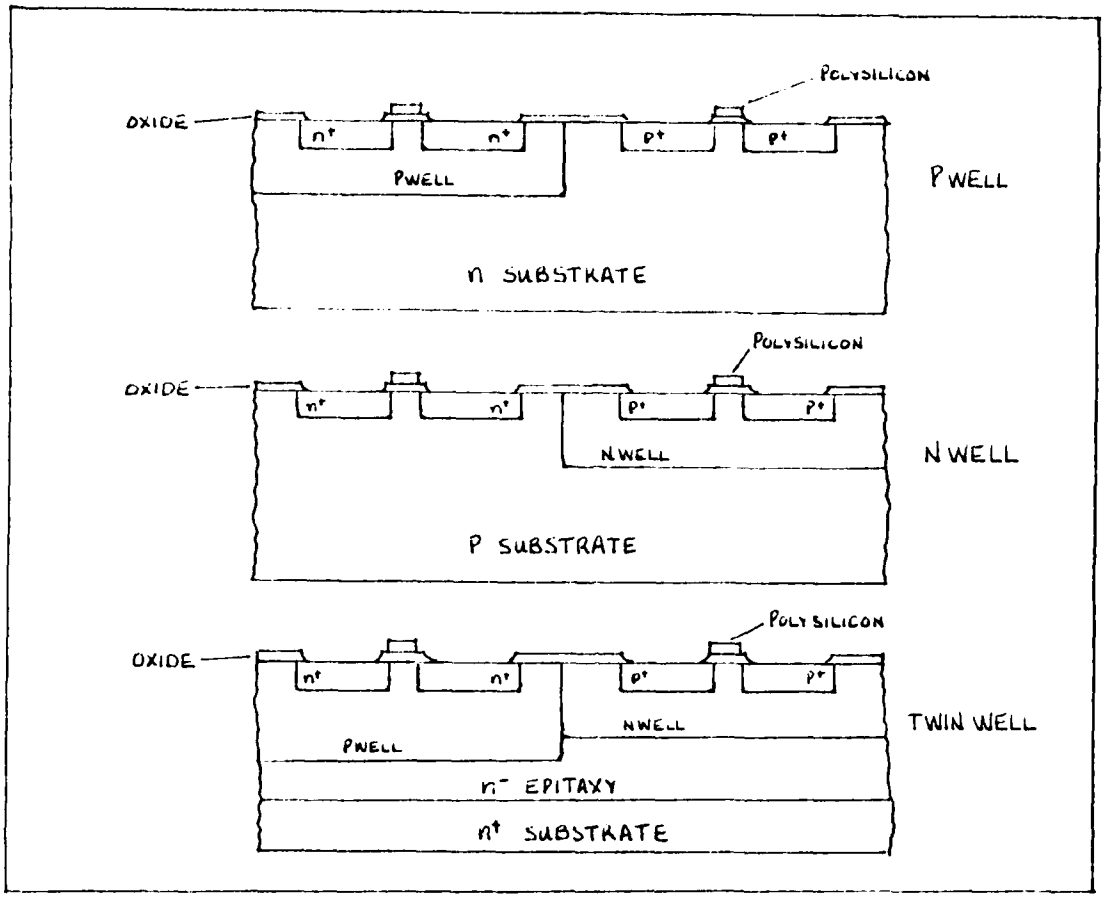


Figure II-1. CMOS Structures (4:483)

constructed using a p-well simply because it was the first method.

All three are claimed to have advantages in enhancing the performance of a CMOS circuit. For the first method, bulk CMOS starts with an n-type substrate into which a p-well is diffused. This well eventually holds the NMOS circuit.

After this diffusion, cuts are made to diffuse in the source and drain for the PMOS circuit which have a higher concentration of p-type material. Next, cuts are made over

the p-well to diffuse in the source and drain of the NMOS circuit. Following this the gates of each transistor are formed. The gate is usually an arrangement of polysilicon sandwiched between silicon dioxide (2). In the last step, metal is laid down to make the appropriate interconnections. Note also in bulk CMOS that there usually is an extra step consisting of etching a groove between each transistor and growing silicon dioxide. This increases the isolation between transistors (2).

Figure II-2 shows a basic CMOS inverter which consists of a PMOS circuit and an NMOS circuit. These two transistors work together to provide the switching, thus the name complementary MOS or CMOS. At any instant of time, only one transistor of the pair is on. What makes CMOS technology so desirable is that in either logic state (0 or 1) negligible power is drawn from the source. Power dissipation only occurs when the logic state switches. This low power dissipation makes CMOS ideally suited for systems that cannot provide a large power supply, such as space vehicles or the new portable microcomputers. Note that both transistors are enhancement mode transistors. This provides active pull-up and active pull-down for the CMOS inverter.

Figure II-2 also shows the typical voltage transfer characteristic for the CMOS inverter. When the input voltage, V_i, is zero, the PMOS transistor is on while the NMOS transistor is off. This is because the PMOS

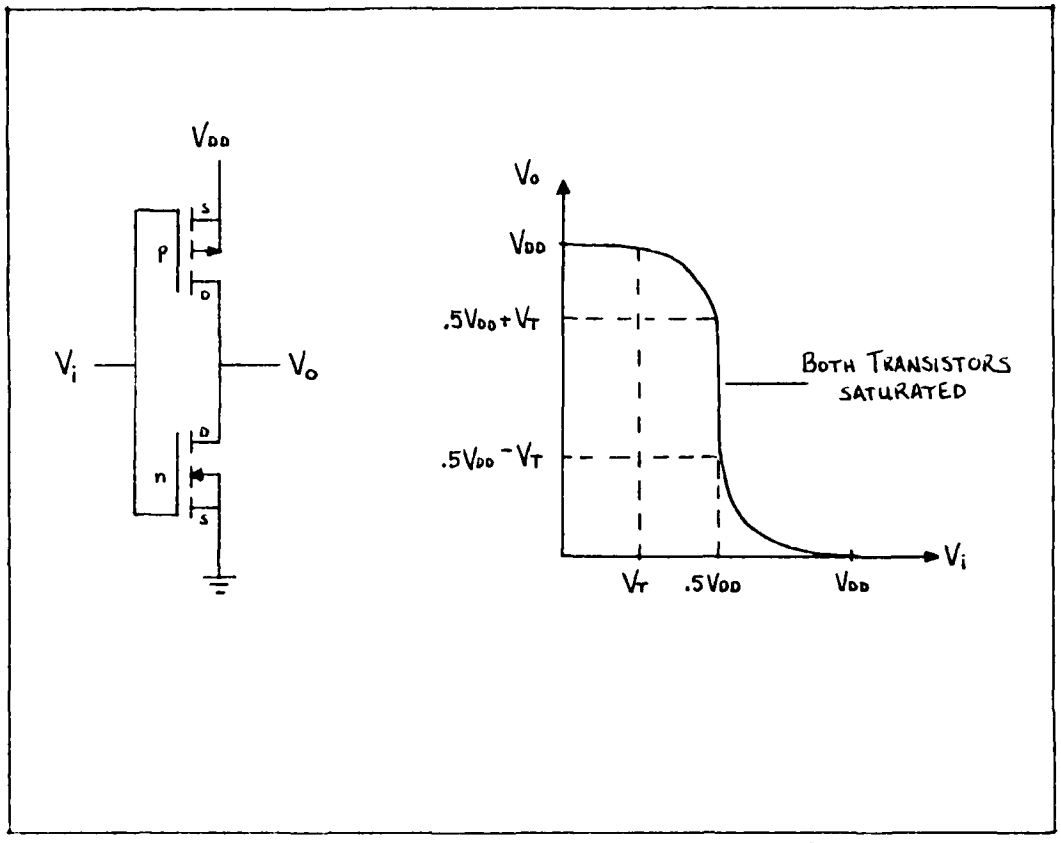


Figure II-2. Typical Inverter and Voltage Transfer Characteristic (7:238,239)

transistor requires negative gate-source and drain-source voltages to cause channel formation while the NMOS transistor requires positive gate-source and drain-source voltages. The output voltage, V_o, is high because it is at the supply voltage potential through the PMOS transistor. As V_i is increased, the NMOS transistor turns on (saturation) causing V_o to drop.

A further increase in V_i causes both transistors to be saturated. It is at this point that the maximum power dissipation of CMOS occurs. Finally, when V_i is

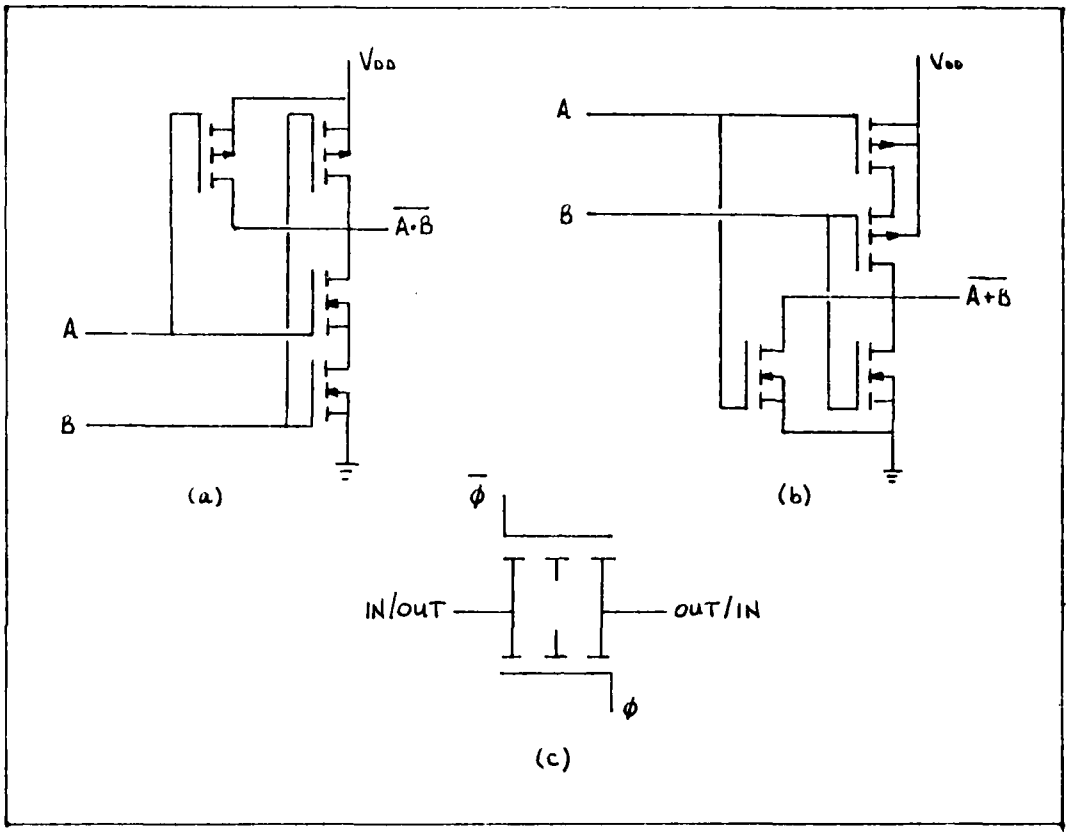


Figure II-3. a) CMOS NAND gate b) CMOS NOR gate
c) CMOS Transmission gate

a threshold voltage (that voltage required for channel formation) below the supply voltage, the NMOS transistor is on and the PMOS transistor is off (7:239). The output voltage is now low because it is at ground potential through the NMOS transistor.

Most CMOS circuits consist of variations of the CMOS inverter. Shown in Figure II-3 are a CMOS NAND gate and a CMOS NOR gate. In the NAND configuration, both n-channel transistor gates must be high to provide a path to ground. Otherwise, the p-channel transistors stay on driving the output to Vdd (normally 5 volts.) In the NOR

configuration, operation is opposite.

Also shown in Figure II-3 is the CMOS transmission gate. This gate is useful in isolating different sections of combinational logic. Current flow through this gate is bi-directional depending on the active phase signal. When the phase signal is high (complement low), current can flow through the transmission gate in either direction because both the p-channel and n-channel transistors are on. When the phase signal is low (complement high), the transmission gate becomes a high impedance device because both transistors are off.

There exist many innovative forms of CMOS technology. All improve or take advantage of certain characteristics of CMOS. High performance CMOS, HiCMOS, uses the twin well structure along with a double layer of polysilicon to increase the speed and density of conventional CMOS (8). Stacked Transistors CMOS, ST-CMOS, stacks the p-channel transistor on top of the n-channel transistor to increase the packing density (9) which makes it comparable to densities achieved with standard NMOS technology. Then there is CMOS on insulating substrate such as CMOS/SOS. More will be said about CMOS/SOS later in this chapter. These are just three of the many forms of CMOS technology that can be used in circuit applications.

Currently, CMOS technology is being applied to microprocessors, RAMs, and analog circuits such as operational amplifiers and analog-to-digital converters.

Very large, 256K, RAMs have been designed by using dynamic CMOS circuits where many n-channel transistors are used with just a few p-channel transistors, and there exists one design that uses an NMOS memory cell in conjunction with high performance CMOS periphery circuitry (10). In this way, all the benefits of CMOS are obtained with the high switching speed of NMOS. CMOS circuits are also ideally suited for analog applications because of the large voltage swing that CMOS can provide. Thus, analog and digital circuits incorporating CMOS circuitry can be fabricated on the same integrated circuit.

CMOS Latchup

CMOS circuits are subject to an undesirable condition called latch-up. When latch-up occurs, the CMOS circuit locks into a logic state and will stay that way until the power is disconnected or the circuit burns out. An electrical transient in the power supply that exceeds the absolute value of either Vdd or Vss (the most negative side of the supply voltage which is usually 0V or ground) is enough to cause latch-up. This transient can be caused by a sudden switching capacitance or it can even be caused by radiation (2).

Latch-up occurs because of the structure of a CMOS circuit. CMOS exhibits parasitic npn and pnp bipolar transistors as shown in Figure II-4. This figure shows a p-well example, but the parasitic transistors exist for the

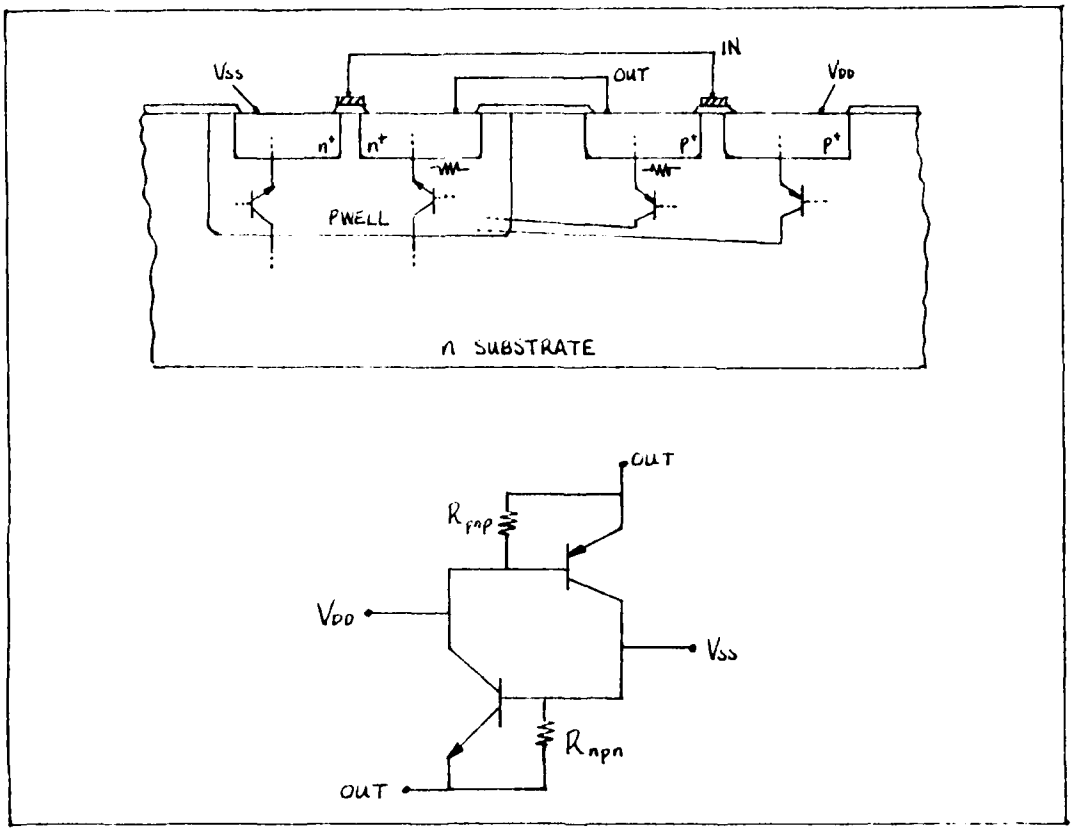


Figure II-4. CMOS Inverter Cross Section Showing Parasitic Bipolar Transistors

n-well and the twin well structures as well.

Notice in the figure that the collector of the npn transistor drives the base of the pnp transistor and vice versa. This forms a pnpn junction which is an SCR, silicon controlled rectifier. The latch-up occurs when the transient voltage is sufficiently large enough to cause an IR drop exceeding 0.7V across either of the emitter-base shunt resistors (4:490). Once one of the transistors turns on, the other will also turn on. Because the collector of each transistor drives the base of the other, both will turn on hard and fast. This quickly causes the power

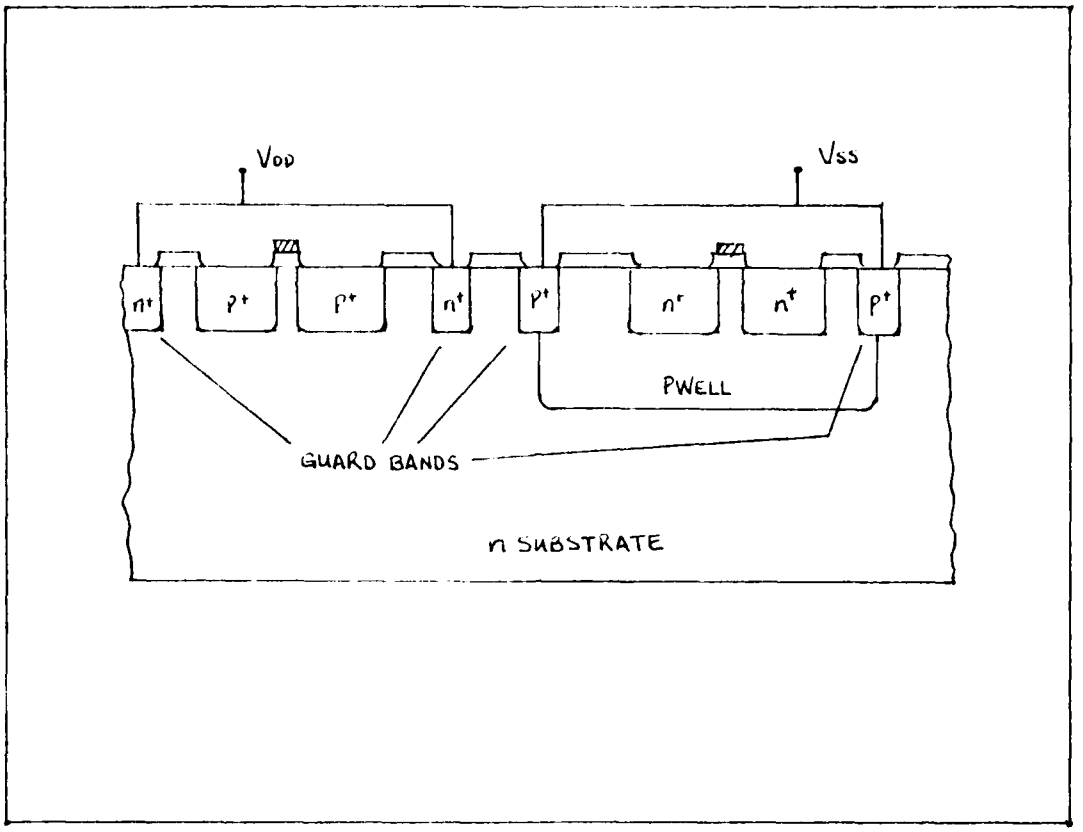


Figure II-5. CMOS Device with Guard Bands (7:243)

supply to be almost completely shorted. A large amount of current flows through this circuit which is why latch-up can be potentially damaging to the CMOS circuit.

Latch-up susceptibility can be reduced or even eliminated in CMOS circuits by careful layout of the CMOS circuits and by either reducing the product of the current gains of the parasitic transistors to be less than one ($h_{FE_{pnp}} \times h_{FE_{npn}} < 1$), or by reducing the emitter-base shunt resistance of the parasitic pnp transistor (11:248), or by using guard bands around the p-channel and n-channel transistors that comprise the CMOS

circuit. The latter method was the first one to be used. Figure II-5 shows how the guard bands are used. The p-channel transistor is surrounded by a continuous n+ ring, and the n-channel transistor is surrounded by a continuous p+ ring (7:243). Guard bands collect the minority carriers before they reach the collectors of the parasitic transistors. Guard bands find the most use in I/O circuitry where input protection from transients is critical (4:490). The major disadvantage of using guard bands is that they increase the dimensions of the CMOS circuit.

One of the more effective ways of reducing latch-up susceptibility is by reducing the product of the current gains of the parasitic transistors. This method is most effective when a p-well is used, and is accomplished by using a p+ buried layer under the p-well (4:490). This method increases the base width of the vertical npn parasitic transistor which decreases its current gain (12:254). Other methods of reducing the product of the current gains is by using a Pt-Si Schottky barrier on the PMOS circuit's source and drain (13), or by using retrograde impurity profiles for the well diffusions (14).

The final method of reducing latch-up susceptibility is by reducing or eliminating the emitter-base shunt resistance of the parasitic pnp transistor. This can be done easily by growing a lightly doped epitaxy over a heavily doped substrate (4:490). If a p-well is used, then

the epitaxy/substrate structure is n/n+, and if an n-well is used, then the structure is p/p+.

Latch-up characterization is dependent on the type of CMOS structure used and influences the choice of substrate material. In the p-well structure, the npn parasitic transistor is formed vertically, and its current gain is dependent on well junction depth and impurity density, while in the n-well structure, the npn parasitic transistor is formed laterally, and its current gain is dependent on circuit alignment and lateral spacing (15:451). But latch-up susceptibility in the p-well and the n-well structures is determined more by the emitter-base shunt resistances and less by the product of the current gains (11, 15, 16, 17). This would make the use of a lightly doped epitaxy critical in hardening against latch-up in CMOS circuits that use either well structure. There is no difference in latch-up immunity between the two structures if an epitaxial layer is not used, while the p-well structure has a better latch-up immunity than the n-well structure if an epitaxial layer is used (16:163).

Latch-up immunity in a twin well structure is also due primarily to a reduction in the emitter-base shunt resistances and not to a reduction in the product of the current gains (17). In this type of structure, though, an epitaxial layer is not used to reduce the shunt resistances, but rather the impurity doping densities of the wells are controlled and kept at 10^{16} cm^{-3}

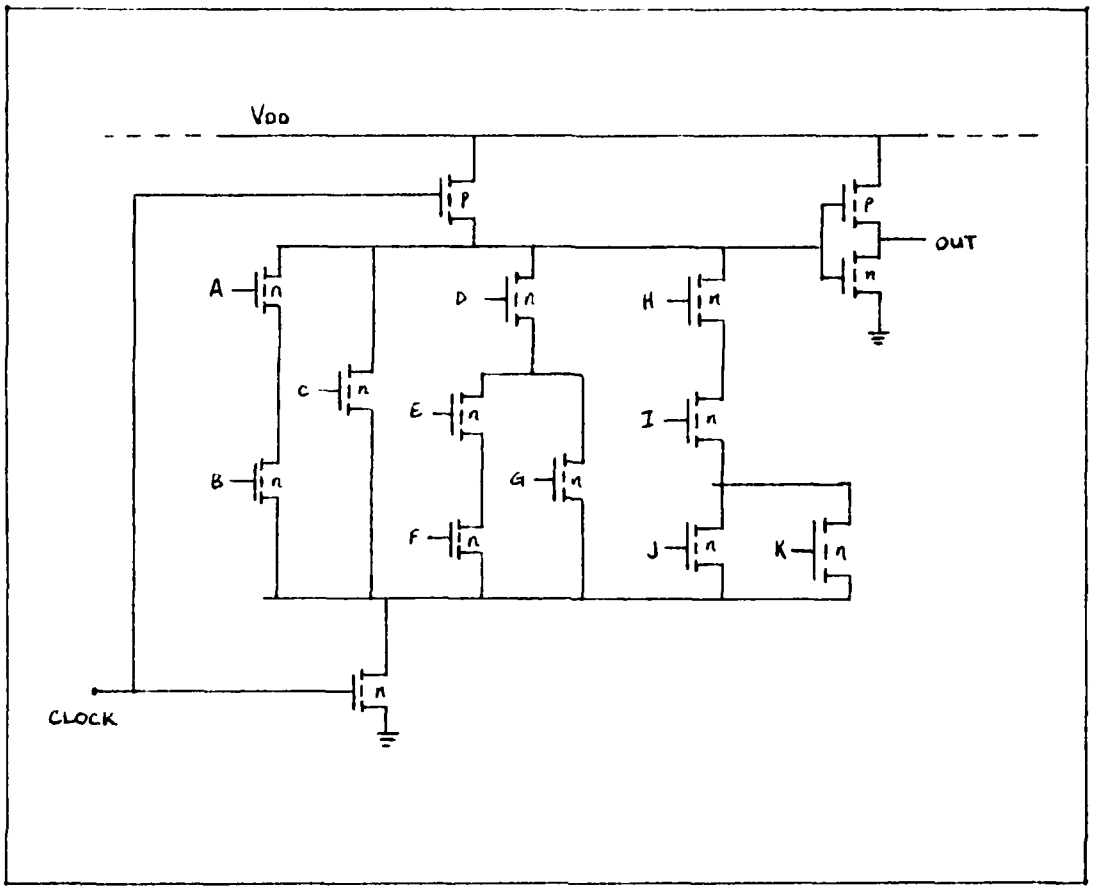


Figure II-6. Domino CMOS (4:481)

(17:171). This high impurity concentration in each well ensures low emitter-base shunt resistances.

CMOS Speed Enhancements

A CMOS circuit is slower than TTL or NMOS, but it is faster than PMOS. The reason why CMCS is slower than NMOS is because of the added gate capacitance on the input due to the parallel connection of the gate of the PMOS transistor to the gate of the NMOS transistor (4:479). The most common way of enhancing the speed of CMOS is by

precharging the bus lines (18). These lines are pulled to a logic 1 during one phase of the clock cycle, and during the next phase, the bus lines are used for the transmission of data. In this way, the CMOS circuit does not have to supply the current necessary to pull the bus lines high which significantly increases the speed of the circuit.

One other way that is currently in wide use of enhancing CMOS circuits is to use many n-channel transistors with very few p-channel transistors (4:480). The speed enhancement comes from the use of a large number of n-channel transistors, yet the power dissipation advantage of CMOS is still present because of the use of the p-channel transistors. This type of arrangement is known as Domino CMOS and an example is shown in Figure II-6.

This type of structure is called dynamic because it is enabled only when the clock pulse is high. When the clock pulse is low, the output remains high. A typical integrated circuit would consist of many of these types of devices in a cascaded connection. The data flows from one device to another, thus the name Domino CMOS (4:480).

There is one other form of CMOS, called Hi-CMOS, that offers improved speed capability over typical CMOS. Hi-CMOS employs the use of a twin well structure with short channel transistors and a double layer of polysilicon for the gate (8:534). It also uses an n/n+ epitaxy/substrate structure to prevent latch-up by reducing the emitter-base

shunt resistances (8:535).

CMOS - NMOS Comparison

The structure of a CMOS circuit and that of an NMOS circuit look similar when compared. The difference is that where the CMOS circuit contains a PMOS transistor, the NMOS circuit contains a depletion mode NMOS transistor with its gate shorted to its drain. This depletion mode transistor provides active pull-up and is always on. This means that the NMOS circuit is always dissipating power while the CMOS circuit is not. An integrated circuit manufactured with thousands of NMOS circuits is going to place a constant load on the power source. This is why CMOS circuits are currently being used in integrated circuits where the power supply is limited.

But a disadvantage of CMOS is that it requires more square area of silicon than does NMOS. Domino CMOS and Hi-CMOS are then used because these two forms not only provide significant speed improvements but they also conserve silicon real estate. Table II-1 shows a more detailed comparison between these two technologies.

Although it appears that NMOS is better, the advantages offered by CMOS can far outweigh any apparent advantages offered by NMOS. The designer must consider the specifications of the system before choosing a technology, especially the power requirements.

Table II-1. CMOS - NMOS Operating Parameters (3)

	NMOS	CMOS
power dissipation per gate (mW)	.1-10	50nW static (freq dependent)
fan-out	25	50
propagation delay per gate (ns)	1-10	10-50
packing density (gates/mm^2)	~150	~70

CMOS - CMOS/SOS Comparison

CMOS/SOS is an emerging technology that seems to offer better performance than bulk CMOS. A CMOS/SOS circuit is similar to a bulk CMOS circuit except that the actual transistors are formed in a silicon island on a sapphire substrate. Figure II-7 shows cross section views of a CMOS and a CMOS/SOS circuit.

There really is no difference between CMOS and CMOS/SOS in the areas of power dissipation, process complexity, and ease of design. There are three important differences between these two technologies and they are parasitic capacitances, latch-up, and floating substrate affects. CMOS exhibits gate-drain, drain-substrate, and source-substrate parasitic capacitances. CMOS/SOS substantially exhibits only a gate-drain capacitance which is lower than that for CMOS (5:II-22).

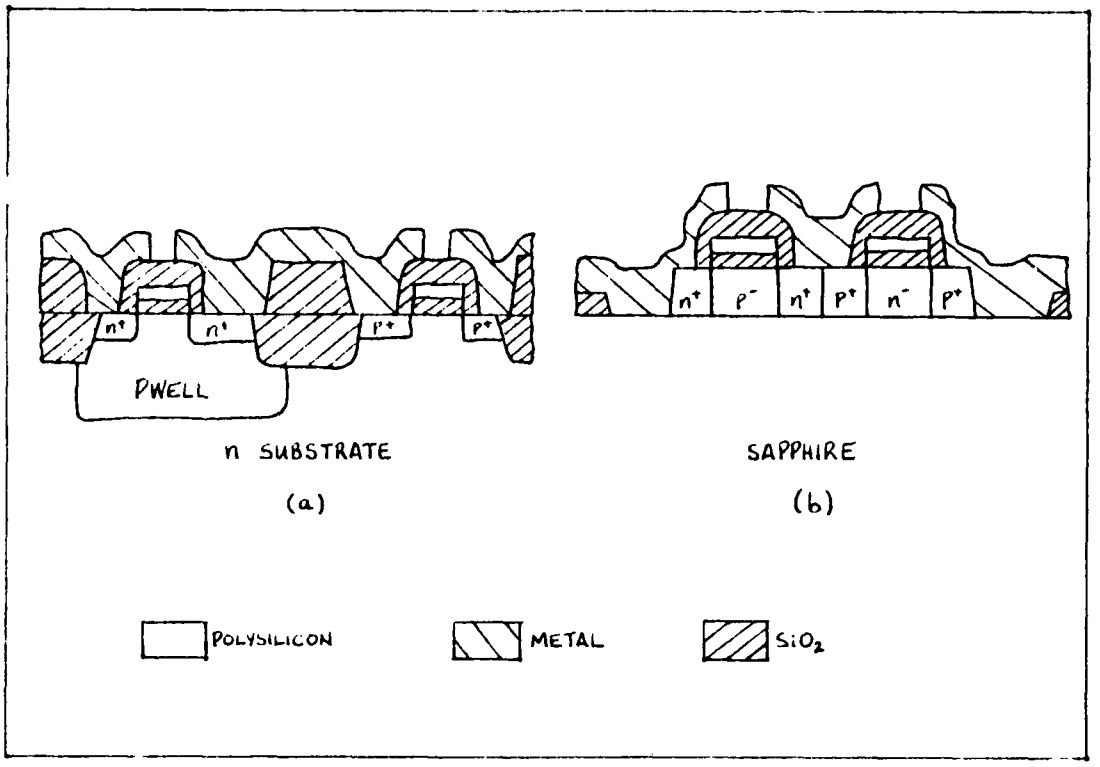


Figure II-7. Cross Section
a) CMOS b) CMOS/SOS (19:247)

The reason for this is that the island diffusions are driven down to the sapphire substrate which is an insulator (5:II-22). Decreasing the parasitic capacitance increases the switching speed for a given supply voltage and power rating. This is why CMOS/SOS enjoys a faster switching speed than CMOS.

CMOS/SOS also does not suffer from latch-up. The sapphire substrate does not permit this condition to occur. There are no possible pnpn junctions in a CMOS/SOS circuit. Although CMOS/SOS does not suffer from latch-up, it does have a floating substrate problem that is not a part of bulk CMOS. This problem causes the potential on the

sapphire substrate to continually rise with repetitive switching of the gates which reduces the drive capability of the CMOS/SOS circuit (19:245).

CMOS/SOS Developments at AFIT

Currently, AFIT has the capability to design and layout CMOS/SOS integrated circuits through the research effort of one of its students (5). A set of CMOS/SOS design rules were established along with a CMOS/SOS cell library that will permit designers to build large scale integrated circuits. Also developed was a CMOS/SOS PLA generator that permits the design and layout of a PLA from the boolean equations that define such a PLA. Finally, a 4-bit ALU was designed and implemented with cells from the cell library. Although no integrated circuits have been fabricated or tested, this capability shows promise for future VLSI designers at AFIT.

III. CMOS Layout and Verification

This chapter presents the current computer-aided design tools that can be used to layout and verify CMOS integrated circuits. Each tool is discussed as it pertains to the CMOS/BULK design methodology. This chapter can possibly be used as a tutorial in CMOS integrated design for future AFIT students.

Design Tools

BANE. A good layout language is vital to design an integrated circuit. This is especially true when the designer cannot depend on an interactive design process but must judiciously place each interconnect through the use of wire and rectangle statements. The BANE process, designed by Stanford, is one of the many layout tools available to the designer.

The BANE process consists of a pipeline that starts with a CLL (Chip Layout Language) file that describes the layout of the circuit and ends with a plot of the circuit. It is an enhanced version of the CLL CAD tool. BANE can also produce a cifout file (".co") or a CIF file (".cif") that is suitable for other CAD tools. BANE can be used for NMOS circuit design or for CMOS circuit design. The emphasis in this thesis is its use in CMOS circuit design. For more information on CLL, the reader should consult the

CLL manual, version 4 produced by Stanford.

To get BANE up and running on the VAX 11/780, a number of changes to the source code had to be made. Most of these changes concerned pathnames, and all the changes are documented in Appendix A for reference. One change that should be noted here is the "lock" procedure of BANE. The designers included this procedure to eliminate the contention of computer resources because the new plotting function takes more time. The "lock" procedure allows only one BANE run per user. In order to study BANE more efficiently, this author eliminated the call to this procedure with the use of comment tokens. The procedure can easily be reinstalled by first deleting the comment tokens and then re-compiling BANE. Appendix A includes the steps necessary to do this.

There are six major differences between BANE and the old CLL program, and these differences are as follows:

-- inclusion of a technology version option (CMOS or NMOS; default is NMOS)

-- inclusion of user defined labels of the form "label: CLL command" in the CLL syntax

-- arguments to options must be separated from the option by a space (ie; "-v cmos" to select CMOS technology)

-- all options must precede the the ".cll" source files

-- any CIF files that are referenced with an external statement from within the ".cll" file must end with a ".cl" and not a ".cif"

-- ability to plot DRC violations on the actual circuit plot

Table III-1. BANE Options

OPTION	RESULT
-v [n/c]mos	selects the technolgy to be used, either NMOS or CMOS; default is NMOS
-o filename	puts any output into filename
-a	supplies a user defined label or a label of the form symname.linenum to all calls in the ".cif" file with user extension 5 (symname is the symbol name in the ".cll" file and linenum is the line number it occurs on in the ".cll" file)
-h	user labels generated for all terminals
-p	display lines containing CLL errors
-u	user defined labels are generated and included in the ".cif" file with user extension 6
-V	use alternate copy of cll2 language processor
-Z	provide extensive diagnostics for debugging BANE
-d #	supplies a ".co" file with a depth corresponding to the level of symbol calls given by the number "#"
-A	plot output on AED terminal (NOT functional)
-r	produce an 8.5 by 11 inch plot
-b	increase the raster plot to 9 feet

One of the primary reasons for developing BANE was to include the capability to design CMOS integrated circuits

by using existing CAD tools for NMOS integrated circuit design. The technology version option allows the designer to select the technology desired for the integrated circuit. Table III-1 summarizes the new options that are included in BANE.

The -a and -u options are not useful for the current implementation of CIFPLOT. Each generates a user extension that is not recognizable by CIFPLOT. Therefore the label feature would not be advantageous to use until CAD tools that can use this extra information can be obtained.

Two useful options included in BANE are the -r and the -p options. The -r option will cause the plot to be drawn on 8.5 x 11 inch paper which will be suitable for reports. But if the plot is very long compared to its height (height being measured along the 11 inch side of the paper) then the plot will not be contained within the allotted 8.5 inches. The -p option will print to the standard output all the lines that contain a CLL error. This greatly improves any debugging in a CLL file.

BANE recognizes nine different layers in the structure of a CMOS integrated circuit. Table III-2 lists these layers. There are four new layers associated with CMOS design. The two layers, pwell and nwell, are used to define the n-channel transistor area and the p-channel transistor area, respectively. Either can be used separately for single-well fabrication processes, or they can be used together for twin-well fabrication processes.

Table III-2. CMOS/BULK Layers

CLL Layer	BANE CIF Layer	MOSIS CIF Layer
metal	UM	CM
poly	UP	CP
diff	UD	CD
contact	UC	CC
glass	UG	CG
pwell	UPW	CW
pplug	UPP	CS
nwell	UNW	---
nplug	UNP	---
---	---	CE
---	---	CC2
---	---	CM2

The other two layers, pplug and nplug, are a p+ layer and an n+ layer, respectively. They are used to create diodes, guard bands, and to provide a good ohmic contact when grounding the p-well or tying the n-well to Vdd.

Also shown in Table III-2 are the layer names that the MOSIS fabricators recognize. Currently MOSIS offers only a standard p-well fabrication process. Before a chip is sent to MOSIS for fabrication, the conversion from the BANE CIF layer names to the MOSIS CIF layer names must be done. Note that MOSIS offers a second level polysilicon (CE), a second level cut (CC2), and a second level metal (CM2). These additional levels are used for creating capacitors, and any design work must be done in CIF since BANE does not support the layers.

DRC. After the circuit has been layed out, the artwork should be verified using the design rule checker. (Design rules are discussed in the next section.) The new DRC program allows the designer to declare the particular technology just like in BANE with the "-v" option.

Besides the standard checks such as minimum width and separation, DRC also provides three additional checks with the "-e" option. With this option, DRC checks for p-wells connected to ground, n-wells connected to Vdd, and that all diodes are shorted. The p-well and n-well checks only consist of ensuring that these wells are connected to the same node; whether it is ground for the p-wells or Vdd for the n-wells the DRC makes no distinction. But because of the way that DRC performs this check and the way that the wells are connected to the supply voltages causes DRC to report that the wells are not connected.

One additional false error will occur when DRC is used. DRC will report "contact cuts without poly or diff underneath" for those contacts used in connecting the wells to their respective sides of the power supply. These false errors should be ignored in these situations only. The "-e" option should not be used unless diodes are being implemented in the circuit.

The ".drc" and ".co" files that are generated by DRC and BANE, respectively, should be kept. BANE permits the designer to "tag" DRC violations on the actual circuit plot.

By typing

bane -v cmos file.drc file.co

the BANE pipeline will produce a plot of the circuit with little black, solid diamonds corresponding to the general area of the DRC violation. This eliminates any confusion by showing exactly where DRC spotted a violation.

Extraction and Simulation. Verification of the circuit should continue through the use of a simulator. This could be an event level simulator or SPICE. Before the simulator can be used, the necessary information must be extracted from the circuit.

MEXTRA can be used for the extraction because it recognizes p-well CMOS. The designer must create a .cadrc file in the home directory with the entry "tech cmos-pw" in it before running MEXTRA with a CMOS CIF file. The designer must also change the CIF layer names to those recognized by MOSIS before running MEXTRA.

SPICE can be run with this output from MEXTRA, but the event level simulator cannot. The current implementation of ESIM cannot be used for CMOS. However, there exists an event level simulator from the University of Washington called RNL. RNL uses the binary output from a program called PRESIM. PRESIM takes for input the extracted information for the circuit. According to the RNL User's Manual, MEXTRA with the "-o" option will produce the extracted information (".sim" file) required by PRESIM. This is not completely true. First, PRESIM does not like

the "n" declaration for n-channel transistors. It would rather have an "e". Second, the node records created by MEXTRA with the "-o" option do not contain all the information that PRESIM requires (PRESIM returns a "bad node record" error).

PRESIM requires the ".sim" file to be in M.I.T. format, but MEXTRA produces the ".sim" file in Berkeley format. There does exist a filter program called SIMFILTER that converts from one format to the other. This program was used but the conversion process did not produce the ".sim" file in the correct format for PRESIM. After conversion, vital information such as the diffusion perimeter, polysilicon perimeter, and metal perimeter in each node record was missing, and four fields in the transistor records were in the wrong positions. PRESIM cannot create an accurate binary file for input to RNL because of these errors.

There is an extraction program from the University of Washington called NETLIST. This program takes a nodal description of the circuit, in LISP-like syntax supplied by the designer, and creates a ".sim" file that is completely suitable for PRESIM. RNL can accurately describe the switching using this output. Using NETLIST will take more time in the overall design cycle because the designer must write a nodal description of the entire circuit and all its transistors, but using macro definitions as described in the NETLIST manual does alleviate some of the design

effort. For additional information on NETLIST, PRESIM, RNL, MEXTRA, SPICE, and ESIM the reader should consult the respective manuals.

Finally, there is a program called EXTRACT that AFIT does not have. This program and a new version of ESIM complement BANE. Their procurement would complete the CMOS design cycle.

Appendix B completely shows the steps needed by the designer to layout and verify a CMOS integrated circuit using the available tools at AFIT. In it is a flowchart that shows the steps. Also included are the editing changes that the designer must do in order to interface to other CAD tools.

Design Methodology

Design Rules. As stated before, MOSIS only offers a standard p-well fabrication process. This process is for 3um (microns) CMOS only. In order to satisfy the MOSIS 3um design rules and the requirements of DRC, a set of design rules were developed. These design rules are listed in Appendix C. Although the final CIF file that is used for fabrication can be scaled, the values presented for lambda in Appendix C represent the best choice to ensure a proper fabrication of the circuit. These values also permit the designer to use DRC without obtaining errors in minimum width and spacing. The final scale value of 75/1 (lambda = 1.5um) for the fabrication CIF file would give the smallest

possible circuit if the values given for lambda in Appendix C are used.

Simple Cells. A cell is a circuit that is used with other circuits like itself or different to make a larger, more complex circuit. Each cell provides a particular function. Simple cells would be classified as those circuits that contain less that 10 transistors. Basic logic gates such as inverters, NAND, NOR, and transmission gates would fall into this classification. A simple cell is relatively straightforward to design, and Appendix D shows designs for a 2-, 3-, and 4-input NAND, a 2-input NOR, an inverter, a double buffer (inverter pair), and a transmission gate. Also included in Appendix D are the SPICE outputs for each cell. Most of these gates will be included in the design of a 4-bit ALU.

Each of the gates shown in Appendix D were designed to allow for the smallest such device without violating any of the design rules established in Appendix C. They were also designed to allow for vertical tessellation, with the power running vertically and the input/output running horizontally. All inputs and outputs are in polysilicon, except for the transmission gate whose output is metal and input is either polysilicon or metal. All of the NAND gates can be tessellated with each other. The inverter, transmission gate, NOR gate, and the double buffer can only be tessellated with themselves. The ratios used were those established by Sommars in his thesis (5:V-8).

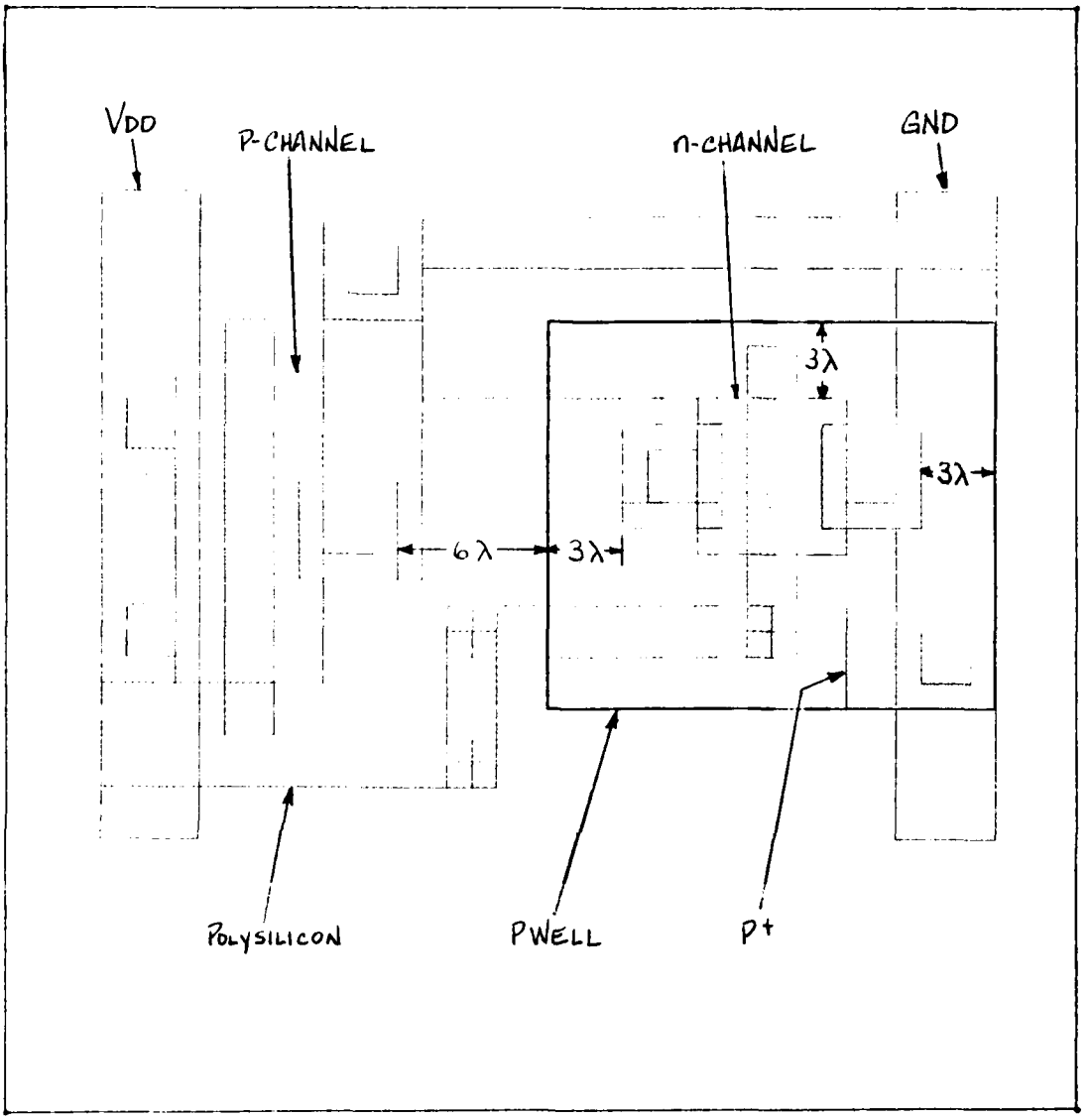


Figure III-1. CMOS Inverter Layout

The p-well is clearly identified in each gate, and therefore the n-channel devices, see Figure III-1 for an example. The rest of the unused real estate of Figure III-1 is n-substrate. Note the contact cuts in the ground wire that overlays the p-well. Below this section of wire is a layer of p+ (pplug) material. The contact cuts and

the p+ material provide a good contact between the p-well and ground. Liberal use of contact cuts to ground p-wells should be implemented to provide better latch-up immunity. Placement of the p-well should be done carefully, and the design rules of Appendix C should be strictly followed to ensure reliable operation.

None of these gates employ guard bands to eliminate latch-up. Guard bands are the only effective way of reducing latch-up because of the fabrication process that is available. MOSIS advises that the only effective way to reduce latch-up susceptibility in this process is to use a large guard band between the internal circuitry and the I/O circuitry. Guard bands could also be used within each cell to prevent spurious channel formation, but the design rules and careful placement of the polysilicon gates help to eliminate this.

From looking at the SPICE output for each gate, the capacitance that is inherent in a CMOS device becomes quite evident. This is especially true when only one input changes while the others remain high as shown in the SPICE outputs for the 3-input NAND and 4-input NAND gates. These two gates had to be modified as shown in Appendix D because of this capacitance.

The switching speeds could be increased by using precharging, or since these designs are basic CMOS gates, they could be eliminated in favor of using Domino CMOS. RNL, an event level simulator, was also used on each of the

gates, and each gate switched correctly.

When designing these cells, especially NAND gates, the designer must be careful in choosing the proper W/L ratios of each transistor. Remember that a CMOS transistor pair contains a relatively large amount of capacitance so that the transistors must be designed large enough to allow an adequate current flow to provide maximum and symmetrical switching. Also the number of inputs of a NAND gate should be limited to four. The reason for this is that in a CMOS gate, the relative resistance of each transistor in the conducting state is about the same (20:203). Consequently, the number of inputs that change simultaneously will influence the voltage transfer characteristic of the gate. The transfer curve will shift, corresponding to the number of inputs that change. This shift causes a decrease in noise immunity, and, hence, the usefulness of the gate.

The designer should also note that because the hole mobility is less than the electron mobility, the width of the p-channel device should be 1.5 to 2 times wider than the width of the n-channel device for a CMOS transistor pair (20:205). The industry standard is 2:1 PMOS to NMOS for transistor pairs (5:II-13).

Complex Cells. Complex cells are those circuits that contain a large number of transistors. The same methodology exists for these types of cells that exists for simple cells. There is one addition, though, and that is the use of guard bands (or channel stops) with shorting

diodes, or Schottky diodes. The guard bands are necessary to prevent spurious channel formation of adjacent transistors in the same substrate area. The shorting diodes are used to short the guard band to the substrate area. This is done by forming a 2x6 lambda contact cut over the guard band-substrate junction (half on one side, half on the other) and then covering it with metal. This ensures that the transistors remain isolated. The I/O pads in the next section can be classified as complex cells.

I/O Pads

A set of CMOS/BULK pads have been obtained from MOSIS. These pads were designed at M.I.T. for minimum susceptiblity to latch-up under the current MOSIS fabrication process. Appendix E shows CIFPLOTS for each pad that is available.

The pads shown in Appendix E are known as the Group 1 pads. They are the only complete set and the most useful. They are also the largest. Each one is 300x640 um, and since they were laid out with 1um equal to 1 lambda, the size of each pad is 300x640 lambda. They include input and output pads, Vdd and GND pads, a tri-state pad, a TTL output pad, a buffered TTL input pad, and a buffered input pad. There is no clock pad included in this group or any other group. Each pad has two Vdd buses and a single ground bus.

The very top and very bottom buses are the Vdd buses.

Table III-3. CMOS/BULK Standard Pad Frames

Frame	Description
28p46x34	28 pins, 4600x3400 um project size 3320x2120 um
40p46x68	40 pins, 4600x6800 um project size 3320x5520 um
40p69x68	40 pins, 6900x6800 um project size 5620x5520 um
64p69x68	64 pins, 6900x6800 um project size 5620x5520 um
64p79x92	64 pins, 7900x9200 um project size 6620x7920 um
84p79x92	84 pins, 7900x9200 um project size 6620x7920 um

The bottom bus (the narrower one) also has a layer of n+ material beneath it and connected to it with contact cuts. This is the guard band that separates the internal circuitry from the I/O circuitry. It is only broken where the connection to the pads must be made by the internal circuitry and where the GND connection must be made to the GND pad.

Also included with these pads are standard pad frames shown in Table III-3. Each pad frame has a full complement of standard input pads. To change pads, the designer just needs to enter the CIF file for the pad frame and replace the call to the input pad with a call to the pad desired.

This eliminates any guess work as to the exact location of placing pads around the perimeter of the frame.

Custom pad frames can be designed by using the desired pads alternating with "padlspace" which is a 300um wide strip of the three bus materials. A custom pad frame is not necessarily reliable because of latch-up susceptibility. The standard pad frames should always be used.

For more information on the other two pad groups available, the reader should consult the CMOS pads doc umentation (21).

Cell Library

Currently, no CMOS/BULK cell library exists. A good cell library contains those cells that are most often used by designers as building blocks. It should contain logic gates that are most often used.

Since no cell library exists, one was created. The logic gates designed by this author are included, as well as the I/O pads, and the standard pad frames. The library is called "libc.lib" and it has a corresponding "c_ext.cll". It is used the same way as the library for NMOS. Appendix F lists the cells available from the library.

IV. ALU Design

To fully test the CMOS design cycle as explained in the previous chapter, a functional circuit incorporating as many components of the cycle as possible was designed and is outlined in this chapter. This functional circuit is a 4-bit ALU.

Preliminary Design

In order to be able to make comparisons between this technology and CMOS/SOS technology, the ALU designed was the one implemented by Sommars and is based on the Motorola MC10181 (5:IV-1). This ALU is only four bits wide and is capable of performing not only arithmetic operations, but also logical operations. This is accomplished through combinational circuitry included before each full adder circuit. This ALU incorporates look-ahead carry adders to increase the speed of the ALU. Figure IV-1 shows the logic diagram of the ALU, Table IV-1 defines the terms of the ALU, and Table IV-2 shows the ALU functions.

As can be seen in Figure IV-1, the ALU consists of 2-, 3-, and 4-input NAND gates, inverters, transmission gates, and double buffers. Clocking is accomplished through the transmission gates; the data and control signals being input on phi1 and data being output on phi2. The double buffers serve as drivers for sending data to other circuit elements.

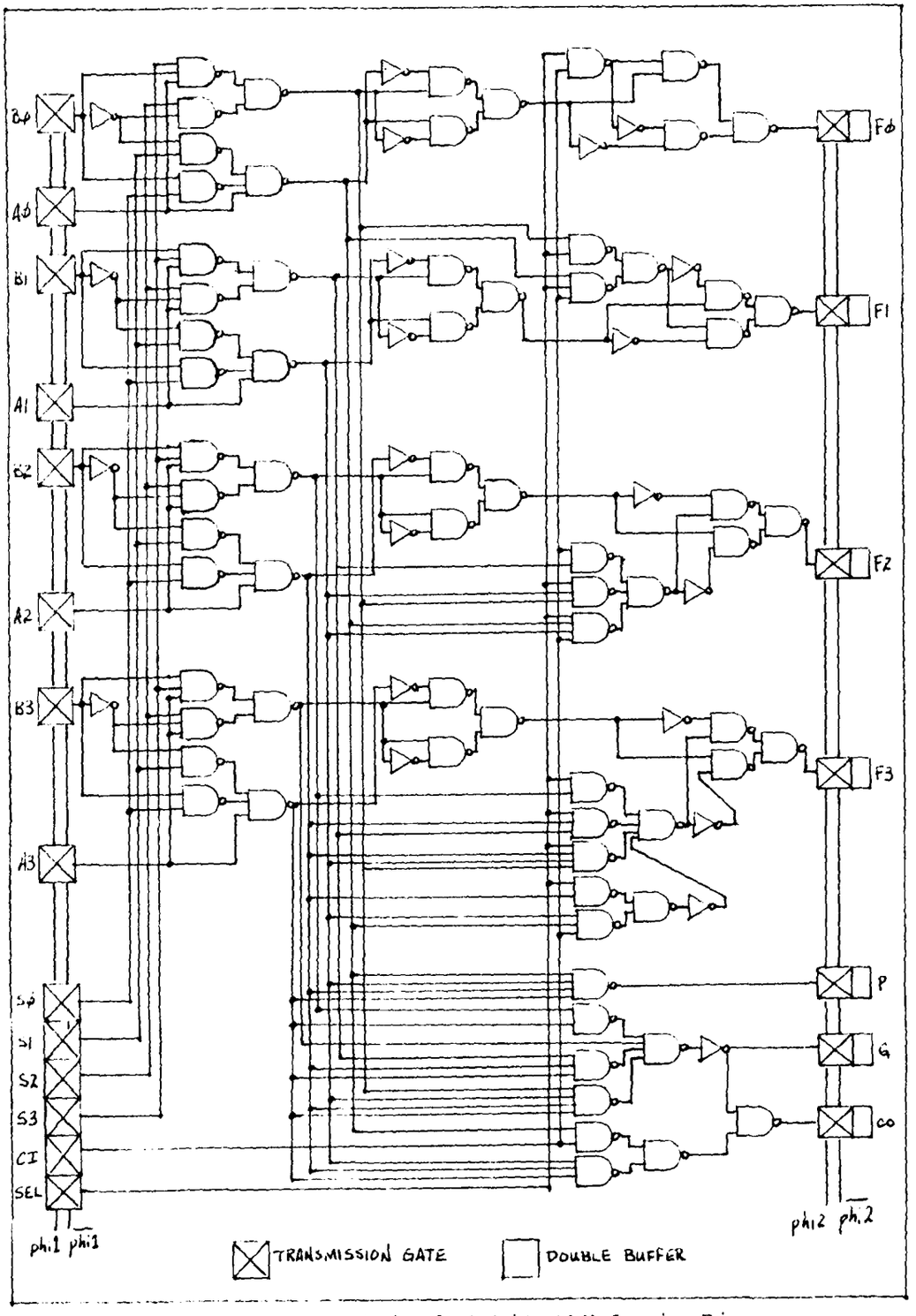


Figure IV-1. Original 4-bit ALU Logic Diagram

Table IV-1. Definition of ALU Terms

Term	Definition
A0 - A3	Operand A
B0 - B3	Operand B
S0 - S3	Function Selection (see Table IV-2)
SEL	when "high" selects logic fcn; when "low" selects arithmetic fcn
F0 - F1	4-bit output
P & G	carry look-ahead output for successive stages
C1	carry in bit
CO	carry out bit

Table IV-2. ALU Arithmetic and Logic Functions (5:V-14)

Fcn Select S3 S2 S1 S0	Logic Fcn SEL is HIGH	Arithmetic Operation SEL is LOW Cn of LSB must be HIGH
L L L L	F = A'	F = A - 1
L L L H	F = (A + B)'	F = A plus (A + B')
L L H L	F = A' • B	F = A plus (A + B)
L L H H	F = logical 0	F = A x 2
L H L L	F = (A • B)'	F = (A • B) - 1
L H L H	F = B'	F = (A • B) plus (A + B')
L H H L	F = A ⊕ B	F = A plus B
L H H H	F = A • B'	F = A plus (A • B)
H L L L	F = A' + B	F = (A • B') - 1
H L L H	F = A ⊙ B	F = A - B - 1
H L H L	F = B	F = (A • B') plus (A + B)
H L H H	F = A • B	F = (A • B') plus A
H H L L	F = logical 1	F = - 1 (2's complement)
H H L H	F = A + B'	F = (A + B') plus 0
H H H L	F = A + B	F = (A + B) plus 0
H H H H	F = A	F = A plus 0

Detailed Design

This ALU was designed in five slices with the first four slices each containing one A and B operand bit and one output bit, and the fifth bit slice containing the control bits, carry-in bit, and the carry outputs. But because each slice is not exactly the same concerning number of cells, each slice had to be designed separately. The difference in each slice is due to the corresponding look-ahead carry circuitry.

There are three main buses in this design, and they run vertically. The first bus, nearest the input transmission gates, transmits the input control signals, S0-S3, to the other four bit slices. These signals go to combinational circuitry that then control how the input operands are manipulated. The second bus consists of eight wires that are staggered in length through the bit slices. It is used to transmit the carry information to the fifth bit slice for calculation of the output carry. The third bus is only two wires wide and is used to transmit the SEL and CI control signals to all the bit slices.

Each bit slice, except for the fifth slice, manipulates only one bit of the operand. Each has a one bit input for the A and B operand, and each has one output for the final product of the manipulation. The fifth bit slice is the largest, and it contains all the control inputs. It also has the carry out information outputs, P, G, and CO.

Because each cell (gate) was designed to tessellate vertically, the cells in each bit slice are stacked to conserve space. Also by careful placement of the cells in each slice, the power connections can easily be made. Consequently, the Vdd and GND connections run vertically with the main Vdd bus at the top of the ALU, and the main GND bus at the bottom of the ALU. The cells were placed to permit the smallest possible dimensions, although the vertical dimension could be shortened by about 50 lambda by moving gates in the first and fifth bit slices and routing wires in a zigzagging pattern. The overall dimensions of the ALU are 864x1238 lambda, including the main Vdd and GND buses. The lower left corner of the ALU is the origin with coordinates of (0,4) lambda.

Verification

DRC was run on the ALU and the expected errors were obtained. These errors were "p-well unconnected to ground" and "contact without poly or diff underneath". These errors were ignored for the reasons stated in Chapter III, page III-5. There were only one or two minimum width errors and these were corrected.

RNL was then used to check the operation of the ALU. The results of this test are inconclusive. The output from MEXTRA with the -o option was used in PRESIM, and a ".net" file describing the ALU was created and used in NETLIST; the output from NETLIST also was used in PRESIM. Both of

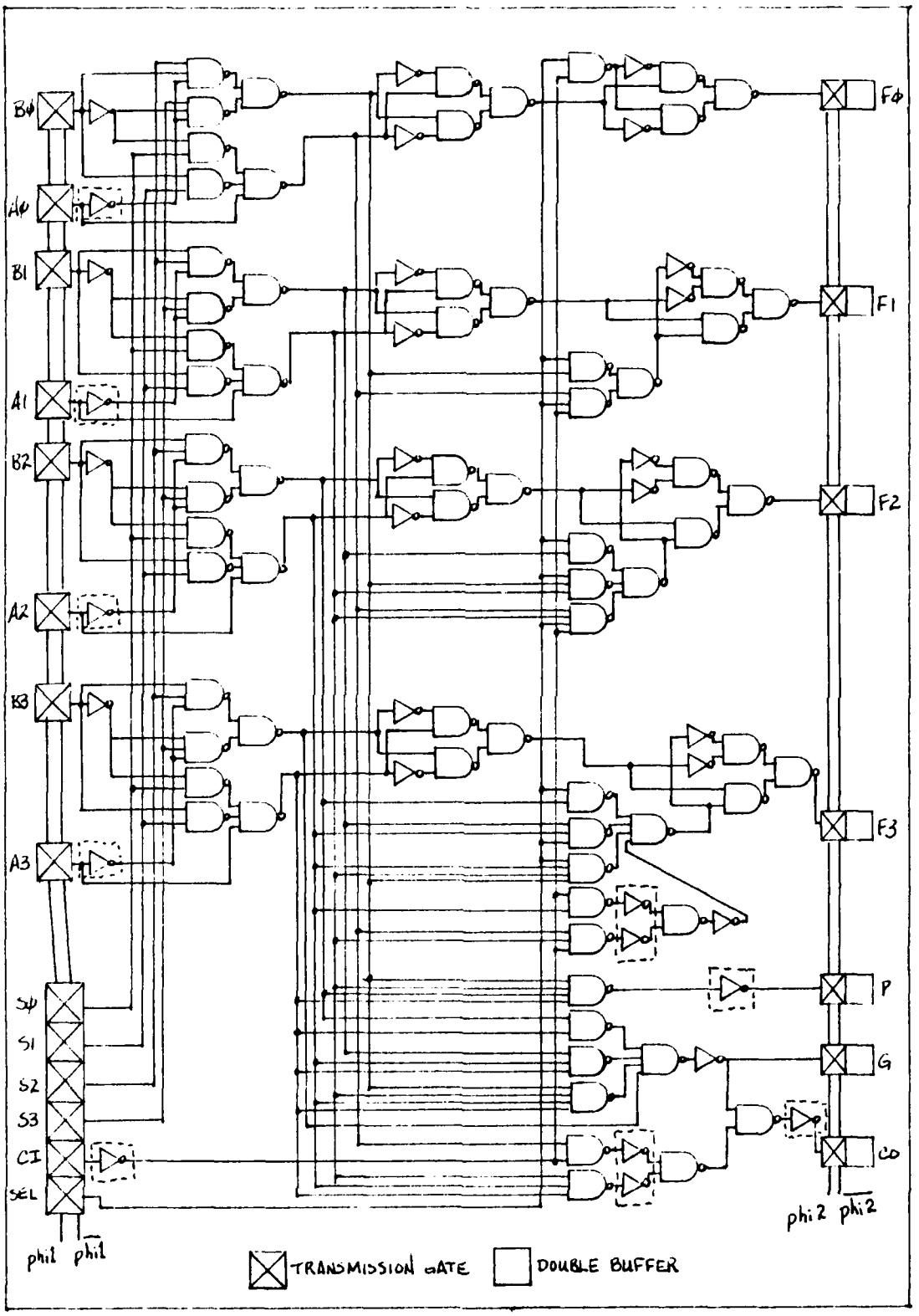


Figure IV-2. Modified ALU Logic Diagram

Table IV-3. Modified ALU Functions

Fcn Select S3 S2 S1 S0	Logic Fcn SEL is LOW	Arithmetic Operation SEL is HIGH Cn of LSB must be HIGH
H H H H	F = A'	F = A - 1
H H H L	F = (A + B)'	F = A plus (A + B')
H H L H	F = A' B	F = A plus (A + B)
H H L L	F = logical 0	F = A x 2
H L H H	F = (A • B)'	F = (A • B) - 1
H L H L	F = B'	F = (A • B) plus (A + B')
H L L H	F = A ⊕ B	F = A plus B
H L L L	F = A • B'	F = A plus (A • B)
L H H H	F = A' + B	F = (A • B') - 1
L H H L	F = A ⊙ B	F = A - B - 1
L H L H	F = B	F = (A • B') plus (A + B)
L H L L	F = A • B	F = (A • B') plus A
L L H H	F = logical 1	F = - 1 (2's complement)
L L H L	F = A + B'	F = (A + B') plus 0
L L L H	F = A + B	F = (A + B) plus 0
L L L L	F = A	F = A plus 0

the binary files created by PRESIM and subsequently used by RNL showed the same results. After loading and setting up RNL, the simulation showed the outputs, F0-F3, to go high and remain that way. No change in inputs changed the state of the outputs.

Subsequent analysis of Sommars' logic diagram and comparison with the original logic diagram for the MC10181 (22:3-196) showed Sommars' design to be in error. In Sommars' design, a NAND gate was substituted for each NOR gate of the original design. This is incorrect, since an AND gate with inverting inputs or a NAND gate with inverting inputs and inverting output must be replaced for each NOR gate. Because of this, the logic diagram and

layout of the ALU was modified. The corrected logic diagram is shown in Figure IV-2 and the CLL layout is shown in Appendix G. The modification consisted of moving some wires and adding 11 inverters as shown by the dotted lines in Figure IV-2. The ALU functions also had to be modified and is shown in Table IV-3. This modification consisted of changing each "high" to "low" and vice versa for the function select inputs, S0-S3, and reversing the role of the SEL input so that when it is "low", the logic functions are selected, and when it is "high", the arithmetic functions are selected. A hardware implementation of this (instead of redefining the function inputs) would be to put an inverter at the inputs of S0-S3 and SEL, then all the previous functions would be valid.

This ALU implementation was then checked using PRESIM/RNL. The ".sim" file used by PRESIM was created by NETLIST using a ".net" file as discussed on page III-8 of Chapter III. The binary output file generated by PRESIM for use by RNL was incorrect. The total number of transistors in the ".sim" file was not being read correctly. The problem was found to be in the transmission gates and the double buffers. For some reason, PRESIM does not like them. These logic gates were then bypassed, and the binary output file was generated properly.

Switching analysis of the modified ALU using RNL was still inconclusive. Although outputs were being generated for different input combinations of S0-S3 and SEL, most of

the outputs generated by the ALU did not correspond to the expected outputs given in Table IV-3. Those outputs that did correspond were most likely coincidental.

V. ALU Comparison

This chapter presents a comparison between the CMOS/SOS ALU designed by Sommars (5:V-12) and the CMOS/BULK ALU designed in Chapter IV of this thesis. A physical comparison of all the logic gates used in the layout of the ALU and the actual ALU is included. Throughout this chapter, references to the CMOS/BULK ALU will be preceded by the word "bulk", and references to the CMOS/SOS ALU will be preceded by the word "sos".

Logic Gates

The logic gates that are used in each ALU design include 2-, 3-, 4-input NAND gates, inverters, transmission gates, and double buffers. As expected, there is a difference in the relative sizes of each. Table V-1 shows the relative sizes of each logic gate for both the bulk and sos versions. Included are the x-length, y-length, area, and percent area difference for each. The percentage shows how much more area the bulk logic gate incorporates over the sos logic gate.

On the average, the bulk logic gates are 39% larger than those of the sos variety. Although the bulk and sos logic gates each have the same W:L ratio for each p-channel and n-channel transistor, respectively, the bulk logic gates require more silicon area because of the p-well.

Table V-1. Relative Dimensions for BULK and SOS Logic Gates

Device	BULK x	BULK y	BULK area	SOS x	SOS y	SOS area	% area diff
2-in NAND	44	28	1232	34	24	816	33.8
3-in NAND	44	46	2024	34	36	1224	39.5
4-in NAND	44	65	2860	34	48	1632	42.9
TX_GATE	38	30	1140	27	14.5	391.5	65.7
INVERTER	36	25	900	23.5	23	540.5	39.9
DBUF	94	90	8460	97	79.5	7711.5	8.8

note: (x and y dimensions in lambda; area in square lambda)

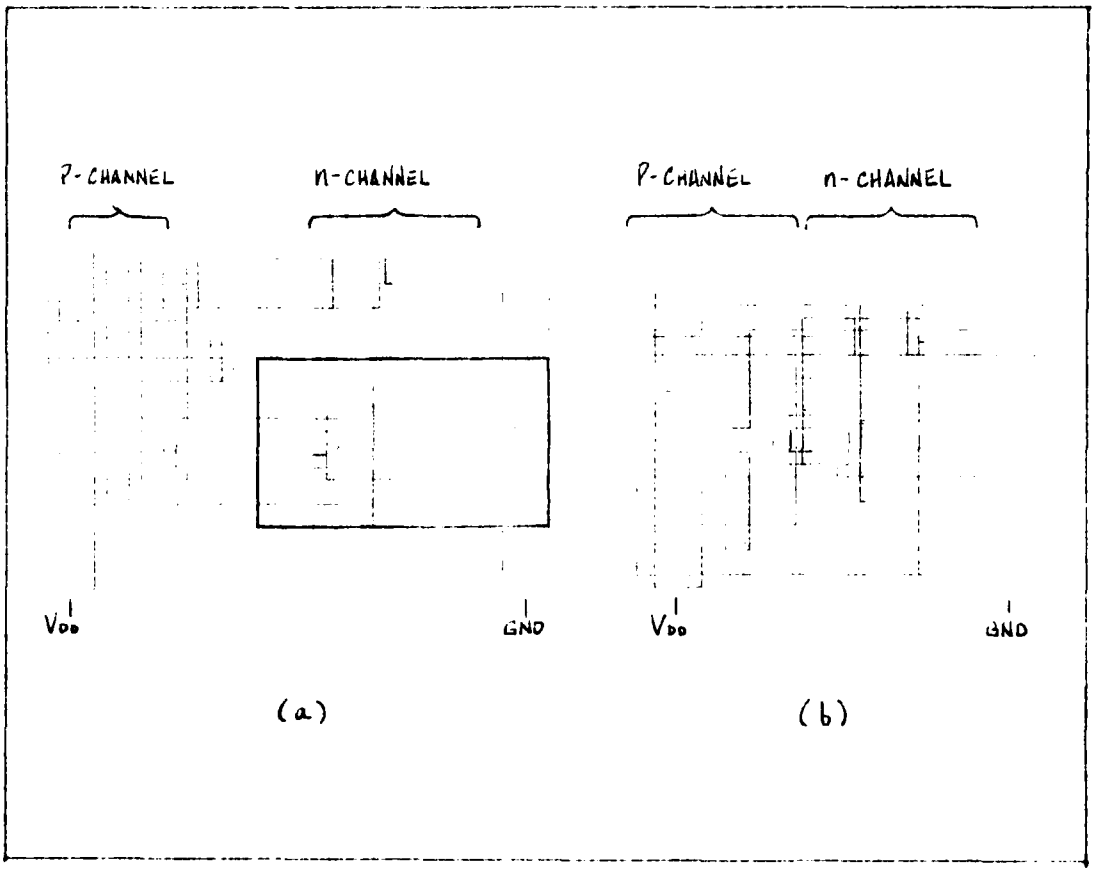


Figure V-1. 2-input NAND Gates
a) BULK b) SOS

Table V-2. ALU Dimensions for BULK and SOS Versions

BULK ALU			SOS ALU			% area
x	y	area	x	y	area	diff
864	1238	1,069,682	707.5	803	568,122.5	46.9

note: (x and y dimensions in lambda; area in square lambda)

The design requirements for the size and placement of the p-well dictate how large the logic gate will be.

Figure V-1 shows how the p-well increases the size of a bulk logic gate. Both are 2-input NAND gates plotted with the same scale. The sos NAND gate is much more compact because its transistors are formed from isolated islands of silicon on a sapphire substrate. The bulk NAND gate requires the p-well to form the n-channel complementary transistor, and it must be large to ensure isolation.

ALU

Each version of the ALU is comprised of 2-, 3-, 4-input NAND gates, inverters, transmission gates, and double buffers. Because of this, the size of the ALU is dependent on these logic gates and any associated interconnecting wires. As shown in the first section of this chapter, the bulk logic gates are larger than the sos logic gates, and, therefore the bulk ALU is larger than the sos ALU. Table V-2 shows the dimensions of each ALU.

The larger size of the bulk ALU has nothing to do with the wiring changes and added inverters that were necessary to correct the design of the logic of the sos ALU (see Chapter IV). There was no change in size of the modified ALU with respect to the original ALU. However, the bulk ALU can be made smaller in the y-dimension by bringing devices closer together and routing interconnect wires in zigzagging patterns. Most of this shrinking can be done in the first and fifth bit slices for a total of approximately 50 lambda. The x-dimension cannot be made smaller.

VI. Conclusions and Recommendations

Conclusions

A complete CMOS/BULK design cycle has been implemented and fully tested to evaluate its effectiveness as a viable set of computer-aided design tools for the layout, verification, and simulation of CMOS/BULK integrated circuits. This design cycle is good for p-well, n-well, or twin-well structures, although MOSIS currently supports just the p-well fabrication process.

BANE was shown to be simple to use in the layout of the CMOS integrated circuits (it can also be used to layout NMOS integrated circuits). The CLL constructs that are employed by BANE make this layout uncomplicated. The added options of BANE are useful (see Table III-1). The one option that does not work is the grid option, -g. The BANE pipeline misinterprets this option and instead of plotting a grid over the circuit, it simply darkens the outline of the circuit. The problem seems to be in the program "concat" of the BANE pipeline.

The design rule verification, DRC, is also useful but is limited because of the nature of the CMOS integrated circuit structures. It is good for checking minimum widths and distances, but it cannot be used for checking "p-well connected to ground" or "n-well connected to Vdd". DRC also produces the errors "diffusion not inside n-well" for

the p-channel transistors, and "contact without poly or diff underneath" for all the contacts that are used to ground the p-well. These errors indicate that DRC would be most useful for the twin-well CMOS structure.

The simulation of a CMOS integrated circuit is accomplished using NETLIST, PRESIM, and RNL. NETLIST produces the ".sim" file for use in PRESIM/RNL. MEXTRA with the -o option cannot be used even when converted with SIMFILTER because of differences in the fields of the transistor and node records within the ".sim" file produced and what PRESIM expects in the fields of each record. RNL was shown to be highly useful and more versatile to use than ESIM.

A CMOS/BULK library was developed, and it contains the integrated circuits that were designed as part of this thesis. All of the gates simulated correctly except for the transmission gate and the double buffer. Although SPICE analysis showed these gates to work properly (see Appendix D), PRESIM would not correctly process these two gates for simulation. Any design work should exclude these two gates when simulating the circuit.

An ALU based on the Motorola MC10181 was designed using the logic gates designed in this thesis. Limited success was accomplished in the simulation runs of the modified ALU presented in Chapter IV. These runs showed the usefulness of RNL, but the bugs in the ALU have not been worked out.

Also included in the library are pads. These pads were designed at M.I.T. for minimum susceptibility to latch-up. They include standard input and output pads, a tri-state pad, and TTL compatible input and output pads. A problem with these pads occur when including them in a ".cll" file with the "external" statement. BANE will not plot the pads, and it gives the error "LAMBDA not gridded". This error occurs because of the scaling factor within the CIF code for the pads. Therefore the pads must be included in the CIF file only for the integrated circuit.

The final CIF file that is sent to fabrication must have the "C-type" layer names that are recognized by MOSIS (see Table III-2). Also the scale factor in the CIF file can be changed to 75/1 to give the minimum size circuit (lambda = 1.5um). This scale factor can be left at 125/1 for a 5um minimum feature size circuit implementation.

Recommendations

The following recommendations are made solely to enhance the CMOS/BULK design cycle:

1. The grid option, -g, of BANE should be corrected. This would entail analyzing the source code of BANE and perhaps discussing the problem with the program's software engineers. This could be done as a special study.

2. The CMOS/BULK ALU should be analyzed, and if necessary discarded in favor of an ALU that does not provide as many functions. The logic of the ALU should be compared to the logic of the original Motorola design. Any changes can then be made and the ALU simulated with RNL. This could also be done as a special study.

3. Procurement of three computer-aided design programs from Berkeley should be made. They are designed to complement BANE and to take full advantage of its capabilities. These programs are EXTRACT, an extraction program; ESIM, the new version which is capable of simulating CMOS circuits; and CIFPLOT, the new version which is capable of plotting the CMOS integrated circuits without having to use the -P option.

4. Procurement of an advanced CMOS/BULK library should be made. Most CMOS design work is done using library cells that are known to be fully operational. An advanced CMOS/BULK library containing complex cells is necessary to design large systems efficiently.

5. A textbook about the design of CMOS integrated circuits should be made available to future VLSI students. A book similar to Mead & Conway (6) is necessary, but one does not exist. Selected articles on Domino CMOS and p-well CMOS, coupled with Chapter II and III of this thesis might be adequate until such a book can be found.

Appendix A. Pathname Changes

Changes to the BANE source code are documented. Most of these changes were pathnames so that proper execution of the BANE pipeline could be accomplished. Also presented are the steps to reinstall the "lock" procedure for BANE. All the changes were done to the source code that exists under the directories /usr/local/cad/lib/stanford/src/DRC83 and /usr/local/cad/lib/stanford/src/PIPELINE83/SRC.

1. For all source files :
   /usr/local/include --> /usr/local/cad/lib/bane
   /usr/local/lib --> /usr/local/cad/lib/bane
   /usr/local/lib/drc --> /usr/local/cad/lib/bane/drc
   /scr/DISTRIBUTIONS/DIST83/LIB -->
   /usr/local/cad/lib/bane

2. For spathnames.h :
   - pathnames for TPLOT, APLOT, and EAPLOT removed
   - /scr/DISTRIBUTIONS/DIST83 -->
     /usr/local/cad/stanford/src/PIPELINE83/SRC

3. For bane.c :
   - pipeline modified to reflect removal of APLOT and TPLOT

4. To reinstall the lock procedure :
   a) Go to the directory
      /usr/local/cad/stanford/src/PIPELINE83/SRC/BANE
   b) Edit Makefile
      - add lock.c to the command line that creates bane, line #56
   c) Edit bane.c
      - remove the comment tokens from the declaration for lock, line #221
      - remove the comment tokens from the call to lock.c, line #276
      - remove the clean up call for lock.c, line #661
   d) Run "make bane"
   e) Move "bane" to /usr/local/cad/bin

Appendix B. CMOS/BULK Design Cycle

The complete CMOS/BULK design cycle is presented. Figure B-1 shows the cycle.

In Figure B-1, the designer must supply the files ".cll" which is the layout of the circuit used by BANE, and ".net" which describes the network of the circuit for use in NETLIST. All the other files are created by the programs shown in the boxes.

Before using MEXTRA, the designer must edit the ".cif" file. The "/" in the scale number (ie, "DS 1000 125/1;") within the file must be deleted and a space inserted, and the layer names must be changed to those recognized by MOSIS, see Table III-2. The file ".cadrc" with the entry "tech cmos-pw" must also be added to the home directory. The ".sim" file produced by MEXTRA cannot be used for the event level simulator, RNL, because the binary file produced by PRESIM for use by RNL cannot be guarenteed to be correct (see the section titled "Extraction and Simulation" in Chapter III of this thesis). NETLIST should be used to create the ".sim" file for PRESIM.

When using CIFPLOT, the option -P must be used with the file upat. This file contains the description of the stipple patterns needed by CIFPLOT.

The following are pathnames to the necessary programs. The designer should create aliases for them in the .cshrc file in the home directory, or simply add the paths to the PATH line in the .login file.

```
bane     -->  /usr/local/cad/bin/bane
cifplot  -->  /usr/local/cad/bin/cifplot
mextra   -->  /usr/local/cad/bin/mextra
newdrc   -->  /usr/local/cad/lib/bane/drc/drc_filter
netlist  -->  /usr/local/cad/uw/bin/netlist
presim   -->  /usr/local/cad/uw/bin/presim
rnl      -->  /usr/local/cad/uw/bin/rnl
spice    -->  /usr/local/cad/bin/spice
```

RNL requires two files to be loaded prior to executing a simulation run. These are loaded after invoking RNL by typing " (load "file") ", where "file" is one of the following:

```
/usr/local/cad/uw/lib/rnl/uwstd.l
/usr/local/cad/uw/lib/rnl/uwsim.l
```

To use the CMOS/BULK cell library, the term

```
#include "/usr/local/cad/lib/bane/c_ext.cll"
```

must be the first term in the ".cll" file. Also, the BANE option "-l" must be used in conjunction with "c" in the BANE command line; ie, "bane -v cmos -l c . . . "

To produce the CIF file that is sent for fabrication, the option "-F" must be used; ie,

"bane -v cmos -F file.cll".

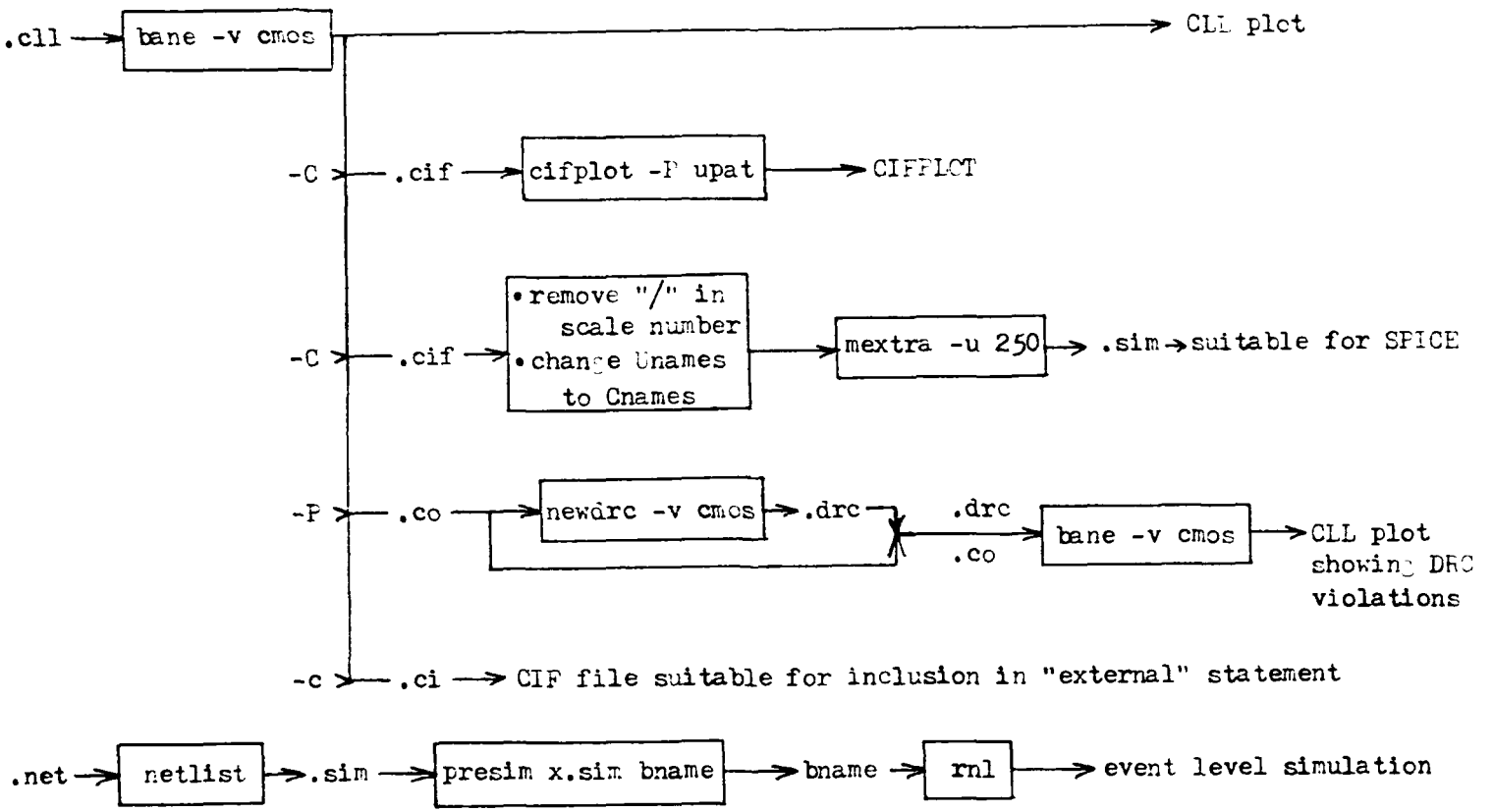


Figure B-1. CMOS/BULK Design Cycle

Appendix C. CMOS/BULK 3um Design Rules

Presented are the design rules developed for CMOS/BULK circuit layout. These rules conform to the MOSIS standard 3um p-well process, (L = lambda).

minimum poly width	2L
poly-poly separation	2L
poly gate extension over active area	2L
minimum metal width	3L (.7uA/um)
metal-metal separation	3L
active area minimum opening	3L
active area separation	3L
poly-diff (active area) separation	2L
minimum contact size	2Lx2L
maximum contact size	2Lx6L
contact-contact separation	2L
Pwell minimum width	5L
Pwell-Pwell separation, same potential	6L
different potential	10L
p+ active area to Pwell edge	6L
p+ mask overlap of Pwell	3L
p+ active area to n+ active area separation inside or outside Pwell	3L
n+ active area in Pwell to Pwell edge	3L
n+ active area in n-sub to Pwell edge	5L

diffusion (active area) cannot cross well boundary

scale in "final.cif" can be no smaller than 75/1
so that L = 1.5um

Appendix D. Description and SPICE Outputs of CMOS/BULK Cells

Presented are the schematics, CLL plots and SPICE outputs for the transimission gate (TX_GATE), 2-, 3-, and 4-input NAND gates (NAND2, NAND3, NAND4, respectively), 2-input NOR gate (NOR2), inverter (INV), and the double buffer (DBUF). These cells were designed to allow for vertical tessellation. They are also cross referenced by CIF ID number for the CMOS/BULK cell library, "libc.lib".

The ratios next to each transistor in the schematic correspond to its width : length ratio. All units are in lambda (L).

The SPICE outputs for the NAND gates correspond to different input conditions. These conditions are marked on each respective SPICE output.

The numbers that are included on both the schematic and the CLL plot are the internal SPICE node numbers. The location of each number on the schematic corresponds to the same location on the CLL plot. This provides clarification of electrical continuity in the CLL plot.

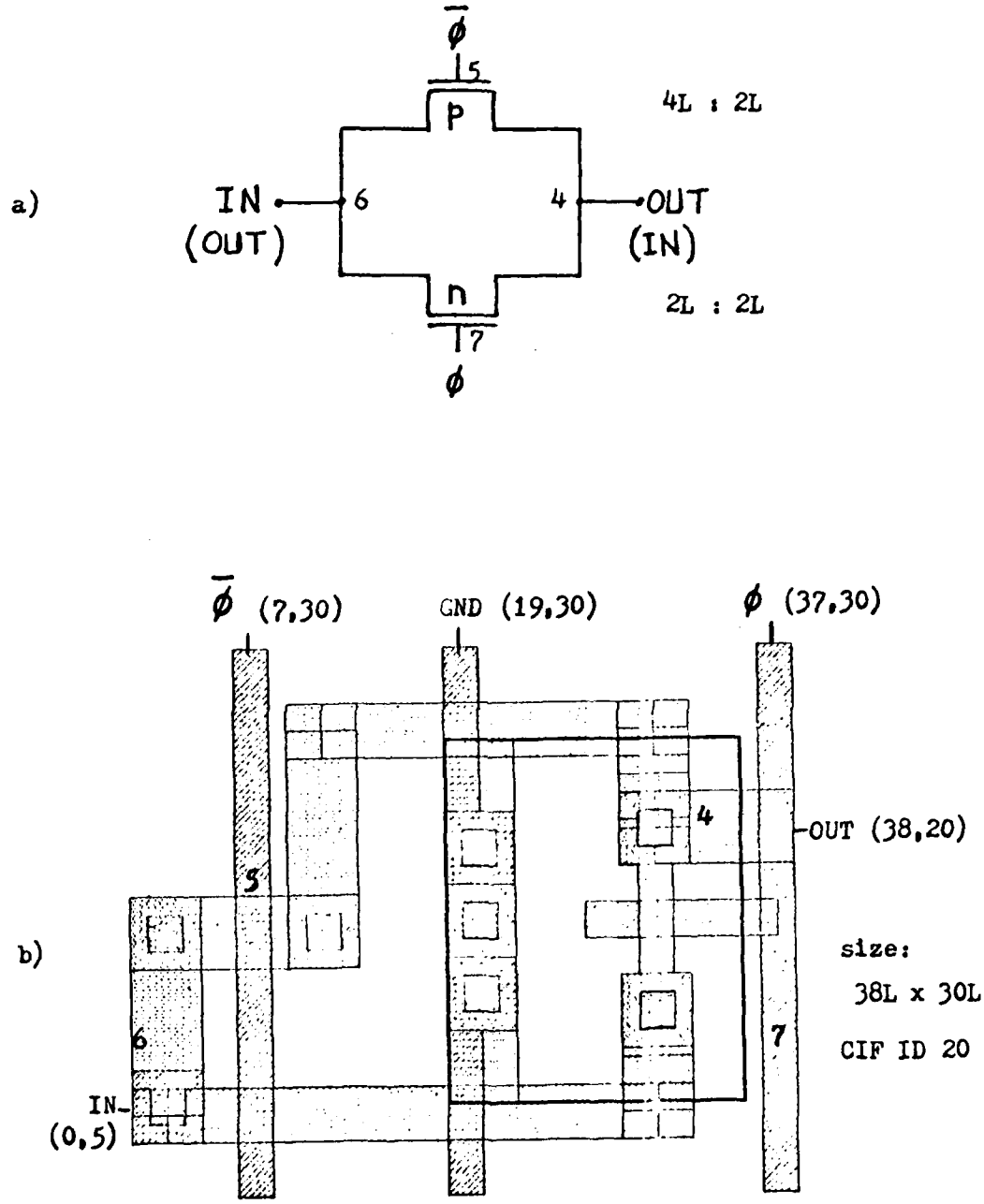
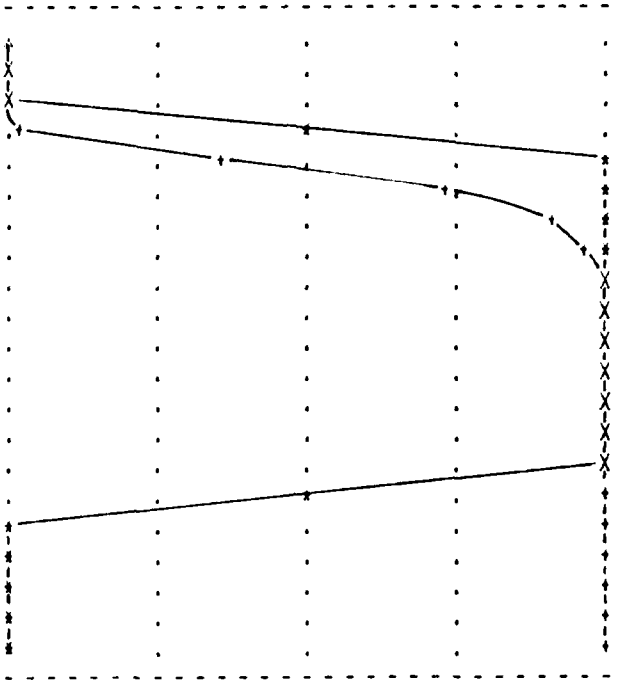


Figure D-1. Transmission Gate

a) schematic b) CLL plot

```
1********07/25/84 ********  SPICE 2G.1 (15OCT80)  ********10:57:50******

0   CMOS/BULK TRANSMISSION GATE TRANSIENT ANALYSIS

0*****     INPUT LISTING                    TEMPERATURE =   27.000 DEG C

0******************************************************************************

 .WIDTH OUT=80
 .IC V(4)=0
 .OPTIONS ITL1=500 ITL5=0
 .MODEL NMOS NMOS (VTO=1V TOX=75NM UO=500 NSUB=1E15 LD=0.7UM)
 +LEVEL=1
 .MODEL PMOS PMOS (VTO=-1V TOX=75NM UO=300 NSUB=2.5E15 LD=0.7UM)
 +LEVEL=1
 VDD 1 0 DC 5V
 M1 6 5 4 0 NMOS L=5.0U W=5.0U
 M2 6 7 4 1 PMOS L=5.0U W=10.0U
 C3 6 0 0.072PF
 C4 4 0 0.065PF
 VIN1 6 0 DC 5V
 VP 5 0 PULSE (0V 5V 1NS 1NS 1NS 5NS)              input high
 VPB 7 0 PULSE (5V 0V 1NS 1NS 1NS 5NS)
 .TRAN 0.5NS 10NS UIC
 .PLOT TRAN V(5) V(4) (0V,5V)
 .END
1********07/25/84 ********  SPICE 2G.1 (15OCT80)  ********10:57:50******

0   CMOS/BULK TRANSMISSION GATE TRANSIENT ANALYSIS

0*****     MOSFET MODEL PARAMETERS          TEMPERATURE =   27.000 DEG C

0******************************************************************************

            NMOS       PMOS
0TYPE       NMOS       PMOS
0LEVEL       1.000      1.000
0VTO         1.000     -1.000
0KP       2.30d-05   1.38d-05
0GAMMA       0.396      0.626
0PHI         0.576      0.624
0CJ       1.02d-04   1.61d-04
0TOX      7.50d-08   7.50d-08
0NSUB     1.00d+15   2.50d+15
0LD       7.00d-07   7.00d-07
0UO        500.000    300.000
1********07/25/84 ********  SPICE 2G.1 (15OCT80)  ********10:57:50******

0   CMOS/BULK TRANSMISSION GATE TRANSIENT ANALYSIS

0*****     TRANSIENT ANALYSIS               TEMPERATURE =   27.000 DEG C

0******************************************************************************
```

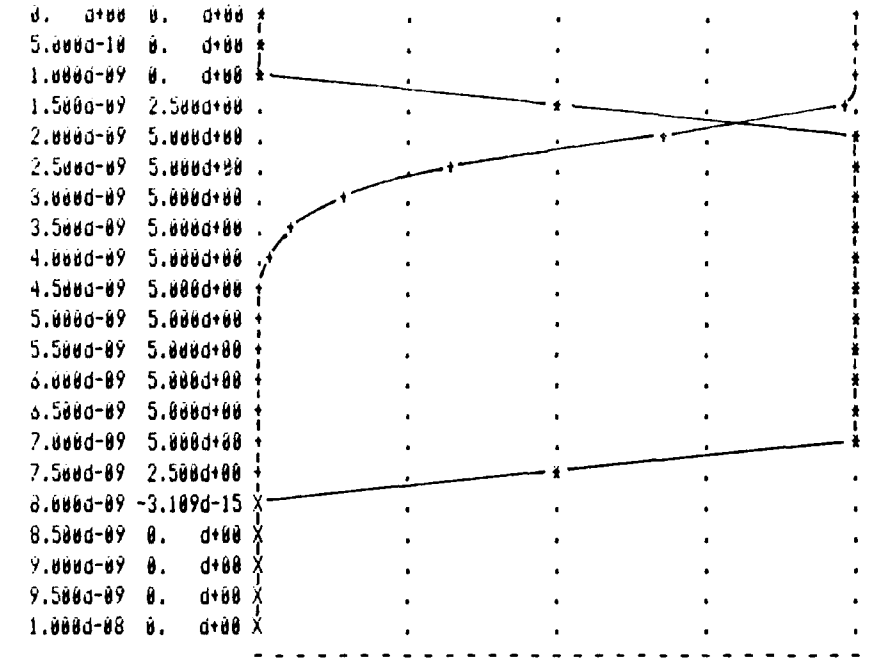
```
LEGEND:

 *: V(5)
 +: V(4)
X
    TIME      V(5)

X(**)---------- 0.   0+00     1.250d+00     2.500d+00     3.750d+00  5.000d+00
```



```
  0.   d+00  0.   d+00
  5.000d-10  0.   d+00
  1.000d-09  0.   d+00
  1.500d-09  2.500d+00
  2.000d-09  5.000d+00
  2.500d-09  5.000d+00
  3.000d-09  5.000d+00
  3.500d-09  5.000d+00
  4.000d-09  5.000d+00
  4.500d-09  5.000d+00
  5.000d-09  5.000d+00
  5.500d-09  5.000d+00
  6.000d-09  5.000d+00
  6.500d-09  5.000d+00
  7.000d-09  5.000d+00
  7.500d-09  2.500d+00
  8.000d-09 -3.109d-15
  8.500d-09  0.   d+00
  9.000d-09  0.   d+00
  9.500d-09  0.   d+00
  1.000d-08  0.   d+00
```

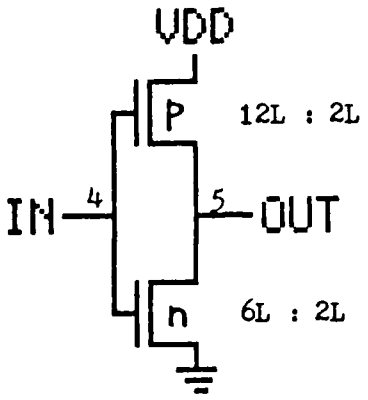
```
1*******07/25/84 ********  SPICE 2G.1 (15OCT8Ø)  ********11:32:26******

Ø   CMOS/BULK TRANSMISSION GATE TRANSIENT ANALYSIS

Ø*****     INPUT LISTING                    TEMPERATURE =   27.ØØØ DEG C

Ø******************************************************************************

 .WIDTH OUT=8Ø
 .IC V(4)=5
 .OPTIONS ITL1=5ØØ ITL5=Ø
 .MODEL NMOS NMOS (VTO=1V TOX=75NM UO=5ØØ NSUB=1E15 LD=Ø.7UM)
 +LEVEL=1
 .MODEL PMOS PMOS (VTO=-1V TOX=75NM UO=3ØØ NSUB=2.5E15 LD=Ø.7UM)
 +LEVEL=1
 VDD 1 Ø DC 5V
 M1 6 5 4 Ø NMOS L=5.ØU W=5.ØU
 M2 6 7 4 1 PMOS L=5.ØU W=1Ø.ØU
 C3 6 Ø Ø.Ø72PF
 C4 4 Ø Ø.Ø65PF
 VIN1 6 Ø DC ØV                                    input low
 VP 5 Ø PULSE (ØV 5V 1NS 1NS 1NS 5NS)
 VPB 7 Ø PULSE (5V ØV 1NS 1NS 1NS 5NS)
 .TRAN Ø.5NS 1ØNS UIC
 .PLOT TRAN V(5) V(4) (ØV,5V)
 .END
1*******07/25/84 ********  SPICE 2G.1 (15OCT8Ø)  ********11:32:26******

Ø   CMOS/BULK TRANSMISSION GATE TRANSIENT ANALYSIS

Ø*****     MOSFET MODEL PARAMETERS          TEMPERATURE =   27.ØØØ DEG C

Ø******************************************************************************

             NMOS       PMOS
ØTYPE        NMOS       PMOS
ØLEVEL        1.ØØØ      1.ØØØ
ØVTO          1.ØØØ     -1.ØØØ
ØKP        2.3ØØd-Ø5  1.38d-Ø5
ØGAMMA        Ø.396      Ø.626
ØPHI          Ø.576      Ø.624
ØCJ        1.Ø2d-Ø4   1.61d-Ø4
ØTOX       7.5Ød-Ø8   7.5Ød-Ø8
ØNSUB      1.ØØd+15   2.5Ød+15
ØLD        7.ØØd-Ø7   7.ØØd-Ø7
ØUO         5ØØ.ØØØ    3ØØ.ØØØ
1*******07/25/84 ********  SPICE 2G.1 (15OCT8Ø)  ********11:32:26******

Ø   CMOS/BULK TRANSMISSION GATE TRANSIENT ANALYSIS

Ø*****     TRANSIENT ANALYSIS               TEMPERATURE =   27.ØØØ DEG C

Ø******************************************************************************
```

```
*: V(5)
+: V(4)
X
    TIME        V(5)

X(**)---------- 0.   0+00     1.250d+00     2.500d+00     3.750d+00  5.000d+00
```



```
 0.   0+00  0.   0+00
 5.000d-10  0.   0+00
 1.000d-09  0.   0+00
 1.500d-09  2.500d+00
 2.000d-09  5.000d+00
 2.500d-09  5.000d+00
 3.000d-09  5.000d+00
 3.500d-09  5.000d+00
 4.000d-09  5.000d+00
 4.500d-09  5.000d+00
 5.000d-09  5.000d+00
 5.500d-09  5.000d+00
 6.000d-09  5.000d+00
 6.500d-09  5.000d+00
 7.000d-09  5.000d+00
 7.500d-09  2.500d+00
 8.000d-09 -3.109d-15
 8.500d-09  0.   0+00
 9.000d-09  0.   0+00
 9.500d-09  0.   0+00
 1.000d-08  0.   0+00
```

a)



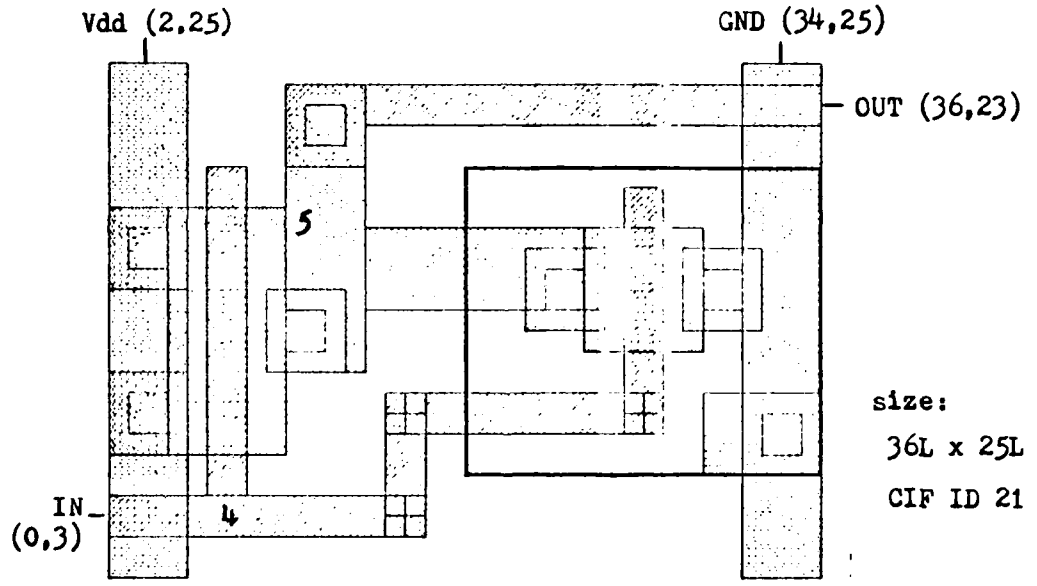
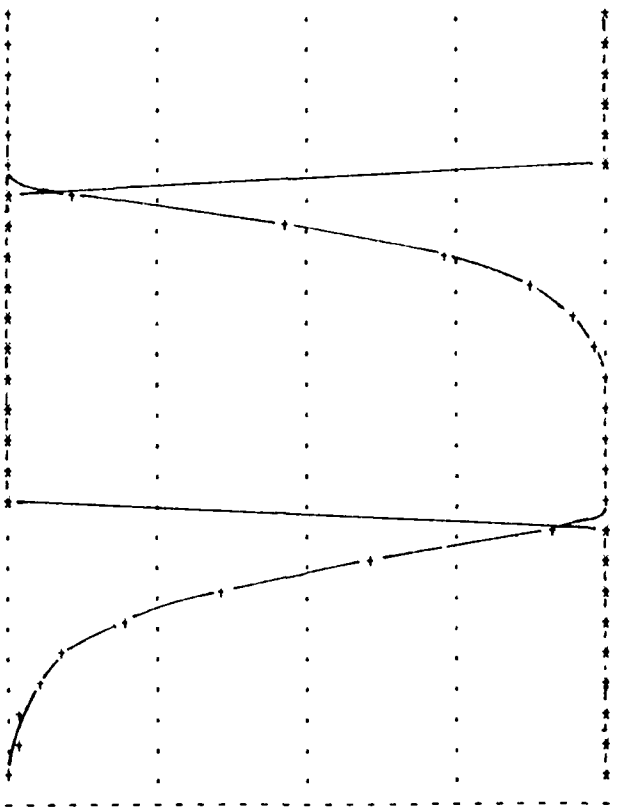


Figure D-2. Inverter
a) schematic b) CLL plot

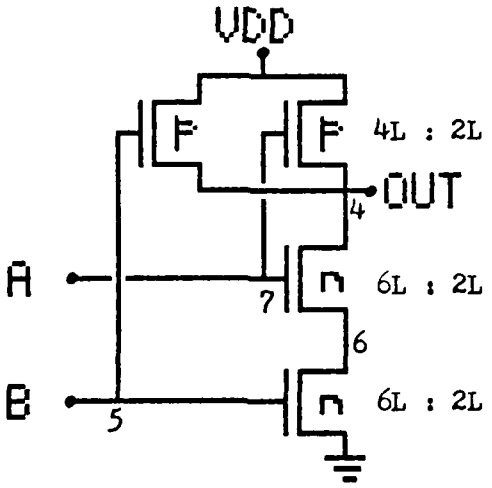
```
1********08/10/84 ********  SPICE 2G.1 (15OCT80)  ********01:23:47*****

0   CMOS/BULK INVERTER TRANSIENT ANALYSIS

0*****     INPUT LISTING                    TEMPERATURE =   27.000 DEG C

******************************************************************************

 .WIDTH OUT=80
 .OPTIONS ITL1=500 ITL5=0
 .MODEL NMOS NMOS (VTO=1V TOX=75NM UO=500 NSUB=1E15 LD=0.7UM)
 +LEVEL=1
 .MODEL PMOS PMOS (VTO=-1V TOX=75NM UO=300 NSUB=2.5E15 LD=0.7UM)
 +LEVEL=1
 VDD 1 0 DC 5V
 M1 5 4 0 0 NMOS L=5.0U W=15.0U
 M2 1 4 5 1 PMOS L=5.0U W=30.0U
 COUT 5 0 0.1PF
 VIN1 4 0 PULSE (5V 0V 1NS 0NS 0NS 2NS)
 .TRAN 0.2NS 5NS
 .PLOT TRAN V(4) V(5) (0V,5V)
 .END
1********08/10/84 ********  SPICE 2G.1 (15OCT80)  ********01:23:47*****

0   CMOS/BULK INVERTER TRANSIENT ANALYSIS

0*****     MOSFET MODEL PARAMETERS          TEMPERATURE =   27.000 DEG C

******************************************************************************

              NMOS       PMOS
0TYPE         NMOS       PMOS
0LEVEL         1.000      1.000
0VTO           1.000     -1.000
0KP         2.30d-05   1.38d-05
0GAMMA         0.396      0.626
0PHI           0.576      0.624
0CJ         1.02d-04   1.61d-04
0TOX        7.50d-08   7.50d-08
0NSUB       1.00d+15   2.50d+15
0LD         7.00d-07   7.00d-07
0UO          500.000    300.000
```

```
1********08/10/84 ********  SPICE 2G.1 (15OCT80)  *********01:23:47*****

0   CMOS/BULK INVERTER TRANSIENT ANALYSIS

0*****     INITIAL TRANSIENT SOLUTION       TEMPERATURE =   27.000 DEG C

0*******************************************************************************

  NODE   VOLTAGE     NODE   VOLTAGE     NODE   VOLTAGE

(  1)    5.0000    (  4)    5.0000    (  5)    0.0000

     VOLTAGE SOURCE CURRENTS

     NAME       CURRENT

     VDD      -6.933d-12

     VIN1      0.   d+00

     TOTAL POWER DISSIPATION   3.47d-11  WATTS

1********08/10/84 ********  SPICE 2G.1 (15OCT80)  *********01:23:47*****

0   CMOS/BULK INVERTER TRANSIENT ANALYSIS

0*****     OPERATING POINT INFORMATION      TEMPERATURE =   27.000 DEG C

0*******************************************************************************
0
0***** MOSFETS

0            M1        M2
0MODEL     NMOS      PMOS
 ID        6.93d-12  0.  d+00
 VGS          5.000     5.000
 VDS          0.000     5.000
 VBS          0.        5.000
1********08/10/84 ********  SPICE 2G.1 (15OCT80)  *********01:23:47*****

0   CMOS/BULK INVERTER TRANSIENT ANALYSIS

0*****     TRANSIENT ANALYSIS               TEMPERATURE =   27.000 DEG C

0*******************************************************************************
```

```
LEGEND:

 *: V(4)
 +: V(5)
X
    TIME      V(4)

X(**)---------- 0.   0+00     1.250d+00     2.500d+00     3.750d+00  5.000d+00
```



a)



b)

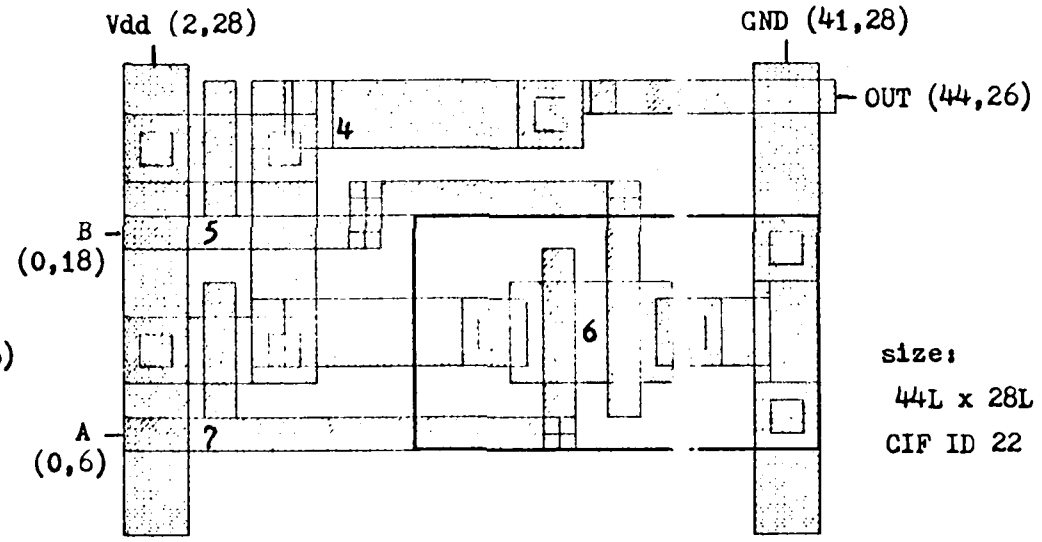
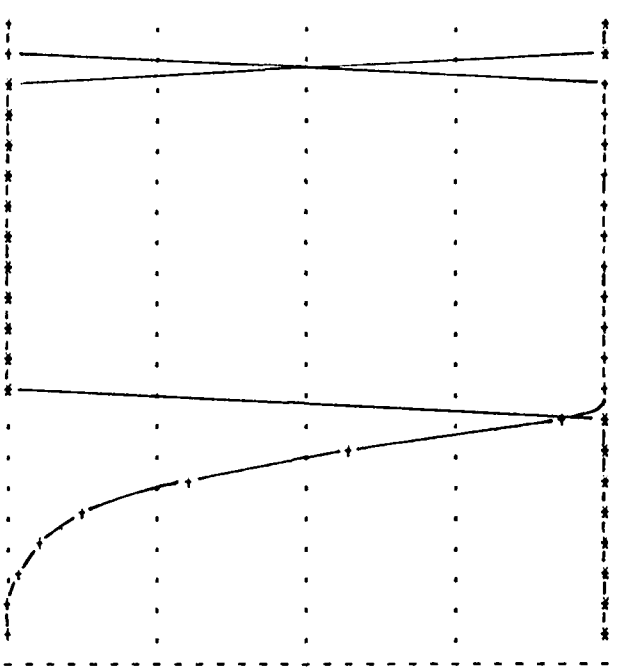


Figure D-3. 2-Input NAND Gate
a) schematic b) CLL plot

```
1********06/10/84 ********  SPICE 2G.1 (15OCT8d)  *********01:12:18*****

0          CMOS/BULK 2-IN NAND TRANSIENT ANALYSIS

0****     INPUT LISTING                    TEMPERATURE =   27.000 DEG C

0******************************************************************************

 .WIDTH OUT=8d
 .OPTIONS ITL1=5dd ITL5=d
 .MODEL NMOS NMOS (VTO=1V TOX=75NM UO=5dd NSUB=1E15 LD=d.7UM)
 +LEVEL=1
 .MODEL PMOS PMOS (VTO=-1V TOX=75NM UO=3dd NSUB=2.5E15 LD=d.7UM)
 +LEVEL=1
 VDD 1 d DC 5V
 M1 1 5 4 1 PMOS L=5.dU W=1d.dU
 M2 6 5 d d NMOS L=5.dU W=15.dU
 M3 4 7 6 d NMOS L=5.dU W=15.dU
 M4 1 7 4 1 PMOS L=5.dU W=1d.dU
 COUT 4 d d.2PF
 VIN1 7 d PULSE (5V dV 1NS dNS dNS 1dNS)    A & B pulse high-low-high
 VIN2 5 d PULSE (5V dV 1NS dNS dNS 1dNS)
 .TRAN 1NS 2dNS
 .PLOT TRAN V(7) V(4) (dV,5V)
 .END
1********08/10/84 ********  SPICE 2G.1 (15OCT8d)  *********01:12:18*****

0          CMOS/BULK 2-IN NAND TRANSIENT ANALYSIS

0****     MOSFET MODEL PARAMETERS          TEMPERATURE =   27.000 DEG C

0******************************************************************************

             NMOS       PMOS
0TYPE        NMOS       PMOS
0LEVEL        1.ddd      1.ddd
0VTO          1.ddd     -1.ddd
0KP        2.3dd-d5   1.3dd-d5
0GAMMA        d.396      d.626
0PHI          d.576      d.624
0CJ        1.d2d-d4   1.d1d-d4
0TOX       7.5dd-d8   7.5dd-d8
0NSUB      1.ddd+15   2.5dd+15
0LD        7.ddd-d7   7.ddd-d7
0UO         5dd.ddd    3dd.ddd
```

```
1********06/10/84 ********  SPICE 2G.1 (15OCT80)  *********01:12:16*****

0           CMOS/BULK 2-IN NAND TRANSIENT ANALYSIS

0*****     INITIAL TRANSIENT SOLUTION       TEMPERATURE =   27.000 DEG C

0******************************************************************************

  NODE   VOLTAGE     NODE   VOLTAGE     NODE   VOLTAGE     NODE   VOLTAGE

(  1)    5.0000    (  4)    0.0000    (  5)    5.0000    (  6)    0.0000

(  7)    5.0000

     VOLTAGE SOURCE CURRENTS

     NAME       CURRENT

     VDD      -1.387d-11

     VIN1       0.   d+00

     VIN2       0.   d+00

     TOTAL POWER DISSIPATION   6.93d-11  WATTS

1********06/10/84 ********  SPICE 2G.1 (15OCT80)  *********01:12:18*****

0           CMOS/BULK 2-IN NAND TRANSIENT ANALYSIS

0*****     OPERATING POINT INFORMATION      TEMPERATURE =   27.000 DEG C

0******************************************************************************
0
0***** MOSFETS

0             M1         M2         M3         M4
0MODEL      PMOS       NMOS       NMOS       PMOS
 ID         0.  d+00  1.39d-11  1.39d-11  0.  d+00
 VGS          5.000      5.000      5.000      5.000
 VDS          5.000      0.000      0.000      5.000
 VBS          5.000      0.        -0.000      5.000
1********08/10/84 ********  SPICE 2G.1 (15OCT80)  *********01:12:18*****

0           CMOS/BULK 2-IN NAND TRANSIENT ANALYSIS

0*****     TRANSIENT ANALYSIS               TEMPERATURE =   27.000 DEG C

0******************************************************************************
```

```
LEGEND:

*: V(7)
+: V(4)
X
     TIME        V(7)

X(**)---------- 0.   d+00      1.250d+00      2.500d+00      3.750d+00  5.000d+00
```

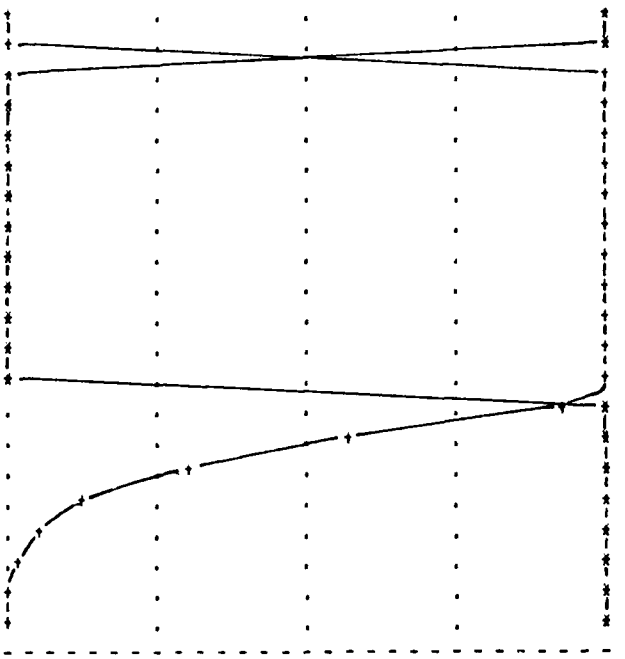


```
  0.   d+00  5.000d+00
  1.000d-09  5.000d+00
  2.000d-09  0.   d+00
  3.000d-09  0.   d+00
  4.000d-09  0.   d+00
  5.000d-09  0.   d+00
  6.000d-09  0.   d+00
  7.000d-09  0.   d+00
  8.000d-09  0.   d+00
  9.000d-09  0.   d+00
  1.000d-08  0.   d+00
  1.100d-08  0.   d+00
  1.200d-08  0.   d+00
  1.300d-08  5.000d+00
  1.400d-08  5.000d+00
  1.500d-08  5.000d+00
  1.600d-08  5.000d+00
  1.700d-08  5.000d+00
  1.800d-08  5.000d+00
  1.900d-08  5.000d+00
  2.000d-08  5.000d+00
```

```
1********08/10/84 ********  SPICE 2G.1 (15OCT80)  ********01:11:2o*****

0          CMOS/BULK 2-IN NAND TRANSIENT ANALYSIS

0***     INPUT LISTING                    TEMPERATURE =   27.000 DEG C

0******************************************************************************

 .WIDTH OUT=80
 .OPTIONS ITL1=500 ITL5=0
 .MODEL NMOS NMOS (VTO=1V TOX=75NM UO=500 NSUB=1E15 LD=0.7UM)
 +LEVEL=1
 .MODEL PMOS PMOS (VTO=-1V TOX=75NM UO=300 NSUB=2.5E15 LD=0.7UM)
 +LEVEL=1
 VDD 1 0 DC 5V
 M1 1 5 4 1 PMOS L=5.0U W=10.0U
 M2 o 5 0 0 NMOS L=5.0U W=15.0U
 M3 4 7 6 0 NMOS L=5.0U W=15.0U
 M4 1 7 4 1 PMOS L=5.0U W=10.0U
 COUT 4 0 0.2PF
 VIN1 7 0 PULSE (5V 0V 1NS 0NS 0NS 10NS)     A pulses high-low-high
 VIN2 5 0 DC 5V                              B remains high
 .TRAN 1NS 20NS
 .PLOT TRAN V(7) V(4) (0V,5V)
 .END
1********08/10/84 ********  SPICE 2G.1 (15OCT80)  ********01:11:2o*****

0          CMOS/BULK 2-IN NAND TRANSIENT ANALYSIS

0*****     MOSFET MODEL PARAMETERS          TEMPERATURE =   27.000 DEG C

0******************************************************************************

             NMOS       PMOS
0TYPE        NMOS       PMOS
0LEVEL        1.000      1.000
0VTO          1.000     -1.000
0KP        2.30d-05   1.38d-05
0GAMMA        0.396      0.626
0PHI          0.576      0.624
0CJ        1.02d-04   1.61d-04
0TOX       7.50d-08   7.50d-08
0NSUB      1.00d+15   2.50d+15
0LD        7.00d-07   7.00d-07
0UO         500.000    300.000
```

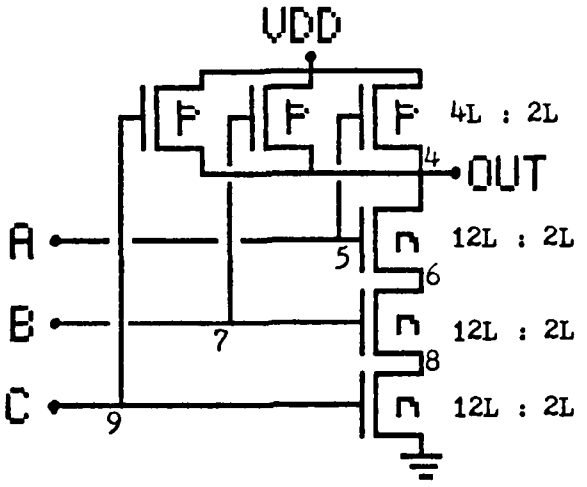
```
1********08/10/84 ********  SPICE 2G.1 (15OCT80)  ********01:11:26*****

0          CMOS/BULK 2-IN NAND TRANSIENT ANALYSIS

0****     INITIAL TRANSIENT SOLUTION       TEMPERATURE =   27.000 DEG C

0*****************************************************************************

  NODE   VOLTAGE     NODE   VOLTAGE     NODE   VOLTAGE     NODE   VOLTAGE

(  1)    5.0000    (  4)    0.0000    (  5)    5.0000    (  6)    0.0000

(  7)    5.0000

    VOLTAGE SOURCE CURRENTS

    NAME       CURRENT

    VDD      -1.387d-11

    VIN1       0.   d+00

    VIN2       0.   d+00

    TOTAL POWER DISSIPATION   6.93d-11  WATTS

1********08/10/84 ********  SPICE 2G.1 (15OCT80)  ********01:11:26*****

0          CMOS/BULK 2-IN NAND TRANSIENT ANALYSIS

0****     OPERATING POINT INFORMATION      TEMPERATURE =   27.000 DEG C

0*****************************************************************************
0
0**** MOSFETS

0            M1        M2        M3        M4
0MODEL     PMOS      NMOS      NMOS      PMOS
 ID        0.  d+00  1.39d-11  1.39d-11  0.  d+00
 VGS          5.000     5.000     5.000     5.000
 VDS          5.000     0.000     0.000     5.000
 VBS          5.000     0.       -0.000     5.000
1********08/10/84 ********  SPICE 2G.1 (15OCT80)  ********01:11:26*****

0          CMOS/BULK 2-IN NAND TRANSIENT ANALYSIS

0****     TRANSIENT ANALYSIS               TEMPERATURE =   27.000 DEG C

0*****************************************************************************
```

```
LEGEND:

 *: V(7)
 +: V(4)
X
     TIME        V(7)

X(**)---------- 0.   d+00      1.250d+00      2.500d+00      3.750d+00  5.000d+00
```



```
  0.   d+00  5.000d+00
  1.000d-09  5.000d+00
  2.000d-09  0.   d+00
  3.000d-09  0.   d+00
  4.000d-09  0.   d+00
  5.000d-09  0.   d+00
  6.000d-09  0.   d+00
  7.000d-09  0.   d+00
  8.000d-09  0.   d+00
  9.000d-09  0.   d+00
  1.000d-08  0.   d+00
  1.100d-08  0.   d+00
  1.200d-08  0.   d+00
  1.300d-08  5.000d+00
  1.400d-08  5.000d+00
  1.500d-08  5.000d+00
  1.600d-08  5.000d+00
  1.700d-08  5.000d+00
  1.800d-08  5.000d+00
  1.900d-08  5.000d+00
  2.000d-08  5.000d+00
```

a)



b)

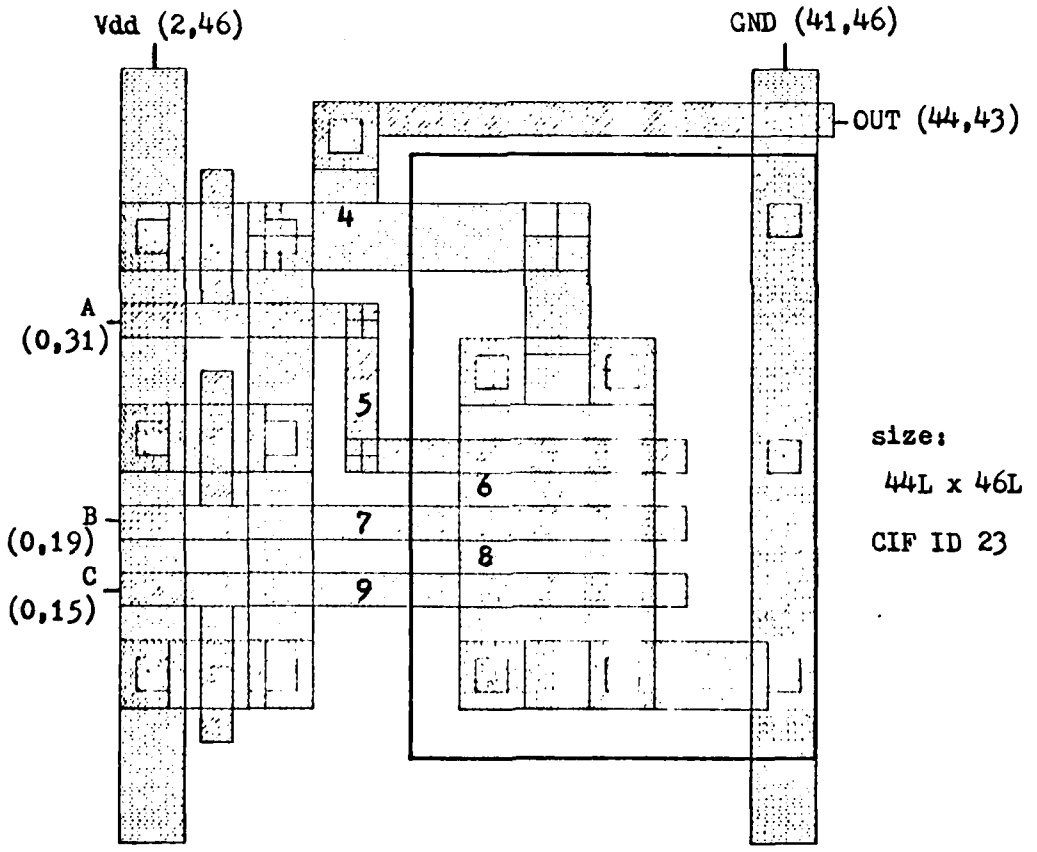
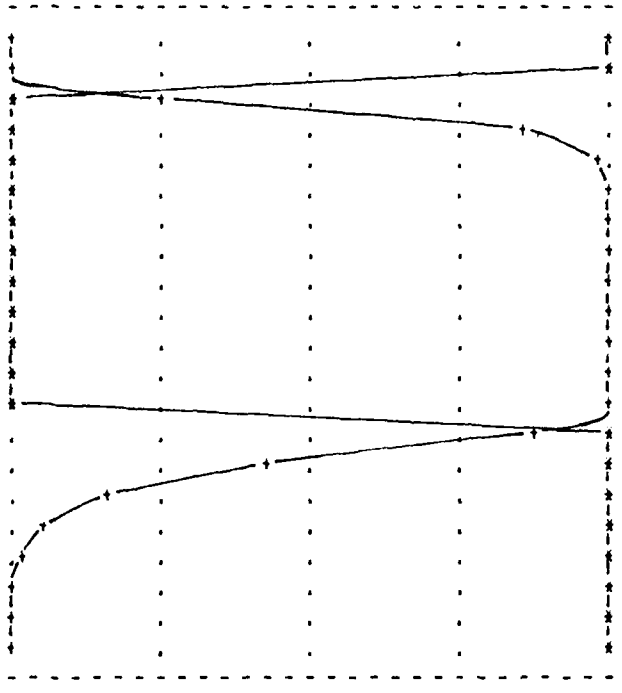


Figure D-4. 3-Input NAND Gate
a) schematic b) CLL plot

```
1********08/10/84 ********  SPICE 2G.1 (15OCT80)  *********01:09:15*****

0           CMOS/BULK 3-IN NAND TRANSIENT ANALYSIS

0*****     INPUT LISTING                    TEMPERATURE =   27.000 DEG C

0******************************************************************************

 .WIDTH OUT=80
 .OPTIONS ITL1=500 ITL5=0
 .MODEL NMOS NMOS (VTO=1V TOX=75NM UO=500 NSUB=1E15 LD=0.7UM)
 +LEVEL=1
 .MODEL PMOS PMOS (VTO=-1V TOX=75NM UO=300 NSUB=2.5E15 LD=0.7UM)
 +LEVEL=1
 VDD 1 0 DC 5V
 M1 1 5 4 1 PMOS L=5.0U W=10.0U
 M2 6 5 4 0 NMOS L=5.0U W=30.0U
 M3 1 7 4 1 PMOS L=5.0U W=10.0U
 M4 8 7 6 0 NMOS L=5.0U W=30.0U
 M5 0 9 8 0 NMOS L=5.0U W=30.0U
 M6 1 9 4 1 PMOS L=5.0U W=10.0U
 COUT 4 0 0.2PF
 VIN1 9 0 PULSE (5V 0V 1NS 0NS 0NS 10NS)     A, B, & C pulse high-low-high
 VIN2 7 0 PULSE (5V 0V 1NS 0NS 0NS 10NS)
 VIN3 5 0 PULSE (5V 0V 1NS 0NS 0NS 10NS)
 .TRAN 1NS 20NS
 .PLOT TRAN V(9) V(4) (0V,5V)
 .END
1********08/10/84 ********  SPICE 2G.1 (15OCT80)  *********01:09:15*****

0           CMOS/BULK 3-IN NAND TRANSIENT ANALYSIS

0*****     MOSFET MODEL PARAMETERS          TEMPERATURE =   27.000 DEG C

0******************************************************************************


              NMOS       PMOS
0TYPE         NMOS       PMOS
0LEVEL         1.000      1.000
0VTO           1.000     -1.000
0KP         2.30d-05   1.38d-05
0GAMMA         0.396      0.626
0PHI           0.576      0.624
0CJ         1.02d-04   1.61d-04
0TOX        7.50d-08   7.50d-08
0NSUB       1.00d+15   2.50d+15
0LD         7.00d-07   7.00d-07
0UO          500.000    300.000
```

```
1********08/10/84 ********  SPICE 2G.1 (15OCT80)  ********01:09:15*****

0          CMOS/BULK 3-IN NAND TRANSIENT ANALYSIS

0*****     INITIAL TRANSIENT SOLUTION       TEMPERATURE =   27.000 DEG C

0******************************************************************************

  NODE   VOLTAGE     NODE   VOLTAGE     NODE   VOLTAGE     NODE   VOLTAGE

(  1)    5.0000    (  4)    0.0000    (  5)    5.0000    (  6)    0.0000

(  7)    5.0000    (  8)    0.0000    (  9)    5.0000

     VOLTAGE SOURCE CURRENTS

     NAME       CURRENT

     VDD      -2.000d-11

     VIN1      0.   d+00

     VIN2      0.   d+00

     VIN3      0.   d+00

     TOTAL POWER DISSIPATION   1.04d-10  WATTS

1********08/10/84 ********  SPICE 2G.1 (15OCT80)  ********01:09:15*****

0          CMOS/BULK 3-IN NAND TRANSIENT ANALYSIS

0*****     OPERATING POINT INFORMATION      TEMPERATURE =   27.000 DEG C

0******************************************************************************
0
0***** MOSFETS

0            M1        M2        M3        M4        M5        M6
0MODEL      PMOS      NMOS      PMOS      NMOS      NMOS      PMOS
 ID        0.  d+00 -2.00d-11  0.  d+00 -2.00d-11 -2.00d-11  0.  d+00
 VGS          5.000     5.000     5.000     5.000     5.000     5.000
 VDS          5.000    -0.000     5.000    -0.000    -0.000     5.000
 VBS          5.000    -0.000     5.000    -0.000    -0.000     5.000
1********08/10/84 ********  SPICE 2G.1 (15OCT80)  ********01:09:15*****

0          CMOS/BULK 3-IN NAND TRANSIENT ANALYSIS

0*****     TRANSIENT ANALYSIS               TEMPERATURE =   27.000 DEG C

0******************************************************************************
```

```
LEGEND:

 *: V(9)
 +: V(4)
X
     TIME        V(9)

X(**)---------- 0.   d+00     1.250d+00     2.500d+00     3.750d+00  5.000d+00
```

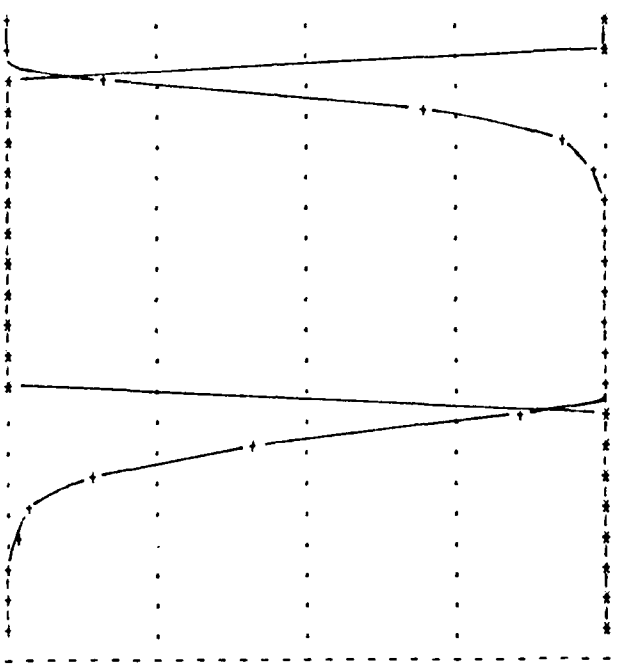


```
 0.   d+00  5.000d+00
 1.000d-09  5.000d+00
 2.000d-09  0.   d+00
 3.000d-09  0.   d+00
 4.000d-09  0.   d+00
 5.000d-09  0.   d+00
 6.000d-09  0.   d+00
 7.000d-09  0.   d+00
 8.000d-09  0.   d+00
 9.000d-09  0.   d+00
 1.000d-08  0.   d+00
 1.100d-08  0.   d+00
 1.200d-08  0.   d+00
 1.300d-08  5.000d+00
 1.400d-08  5.000d+00
 1.500d-08  5.000d+00
 1.600d-08  5.000d+00
 1.700d-08  5.000d+00
 1.800d-08  5.000d+00
 1.900d-08  5.000d+00
 2.000d-08  5.000d+00
```

```
1********08/10/84 ********  SPICE 2G.1 (15OCT80)  ********01:09:47*****

0           CMOS/BULK 3-IN NAND TRANSIENT ANALYSIS

0*****     INPUT LISTING                    TEMPERATURE =   27.000 DEG C

0******************************************************************************

 .WIDTH OUT=80
 .OPTIONS ITL1=500 ITL5=0
 .MODEL NMOS NMOS (VTO=1V TOX=75NM UO=500 NSUB=1E15 LD=0.7UM)
 +LEVEL=1
 .MODEL PMOS PMOS (VTO=-1V TOX=75NM UO=300 NSUB=2.5E15 LD=0.7UM)
 +LEVEL=1
 VDD 1 0 DC 5V
 M1 1 5 4 1 PMOS L=5.0U W=10.0U
 M2 6 5 4 0 NMOS L=5.0U W=30.0U
 M3 1 7 4 1 PMOS L=5.0U W=10.0U
 M4 8 7 6 0 NMOS L=5.0U W=30.0U
 M5 0 9 8 0 NMOS L=5.0U W=30.0U
 M6 1 9 4 1 PMOS L=5.0U W=10.0U
 COUT 4 0 0.2PF
 VIN1 9 0 PULSE (5V 0V 1NS 0NS 0NS 10NS)   A & C pulse high-low-high
 VIN2 7 0 DC 5V                            B remains high
 VIN3 5 0 PULSE (5V 0V 1NS 0NS 0NS 10NS)
 .TRAN 1NS 20NS
 .PLOT TRAN V(9) V(4) (0V,5V)
 .END
1********08/10/84 ********  SPICE 2G.1 (15OCT80)  ********01:09:47*****

0           CMOS/BULK 3-IN NAND TRANSIENT ANALYSIS

0*****     MOSFET MODEL PARAMETERS          TEMPERATURE =   27.000 DEG C

0******************************************************************************

             NMOS       PMOS
0TYPE        NMOS       PMOS
0LEVEL        1.000      1.000
0VTO          1.000     -1.000
0KP        2.30d-05   1.36d-05
0GAMMA        0.396      0.626
0PHI          0.576      0.624
0CJ        1.02d-04   1.61d-04
0TOX       7.50d-08   7.50d-08
0NSUB      1.00d+15   2.50d+15
0LD        7.00d-07   7.00d-07
0UO         500.000    300.000
```

```
1********08/10/84 ********  SPICE 2G.1 (15OCT8Ø)  *********01:09:47*****

Ø          CMOS/BULK 3-IN NAND TRANSIENT ANALYSIS

Ø*****     INITIAL TRANSIENT SOLUTION       TEMPERATURE =   27.ØØØ DEG C

Ø********************************************************************************

  NODE   VOLTAGE     NODE   VOLTAGE     NODE   VOLTAGE     NODE   VOLTAGE

(  1)    5.ØØØØ    (  4)    Ø.ØØØØ    (  5)    5.ØØØØ    (  6)    Ø.ØØØØ

(  7)    5.ØØØØ    (  8)    Ø.ØØØØ    (  9)    5.ØØØØ

    VOLTAGE SOURCE CURRENTS

    NAME        CURRENT

    VDD       -2.Ø8ØØe-11

    VIN1        Ø.    e+ØØ

    VIN2        Ø.    e+ØØ

    VIN3        Ø.    e+ØØ

    TOTAL POWER DISSIPATION   1.Ø4e-1Ø  WATTS

1********08/10/84 ********  SPICE 2G.1 (15OCT8Ø)  *********01:09:47*****

Ø          CMOS/BULK 3-IN NAND TRANSIENT ANALYSIS

Ø*****     OPERATING POINT INFORMATION      TEMPERATURE =   27.ØØØ DEG C

Ø********************************************************************************
Ø
Ø***** MOSFETS

Ø            M1         M2         M3         M4         M5         M6
ØMODEL      PMOS       NMOS       PMOS       NMOS       NMOS       PMOS
 ID        Ø.  e+ØØ -2.Ø8e-11  Ø.  e+ØØ -2.Ø8e-11 -2.Ø8e-11  Ø.  e+ØØ
 VGS          5.ØØØ      5.ØØØ      5.ØØØ      5.ØØØ      5.ØØØ      5.ØØØ
 VDS          5.ØØØ     -Ø.ØØØ      5.ØØØ     -Ø.ØØØ     -Ø.ØØØ      5.ØØØ
 VBS          5.ØØØ     -Ø.ØØØ      5.ØØØ     -Ø.ØØØ     -Ø.ØØØ      5.ØØØ
1********08/1Ø/84 ********  SPICE 2G.1 (15OCT8Ø)  *********01:09:47*****

Ø          CMOS/BULK 3-IN NAND TRANSIENT ANALYSIS

Ø*****     TRANSIENT ANALYSIS               TEMPERATURE =   27.ØØØ DEG C

Ø********************************************************************************
```

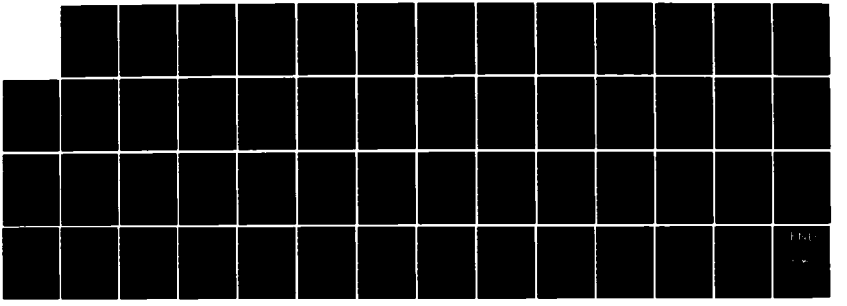
```
0LEGEND:

 *: V(9)
 +: V(4)
X
     TIME       V(9)

X(**)---------- 0.   0+00      1.250D+00      2.500D+00      3.750D+00  5.000D+00
```

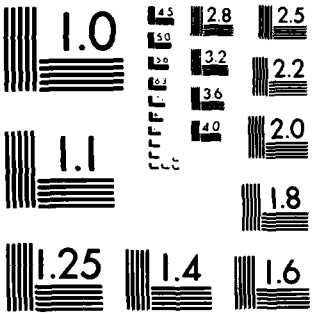


```
  0.   0+00  5.0000+00
  1.0000-09  5.0000+00
  2.0000-09  0.   0+00
  3.0000-09  0.   0+00
  4.0000-09  0.   0+00
  5.0000-09  0.   0+00
  6.0000-09  0.   0+00
  7.0000-09  0.   0+00
  8.0000-09  0.   0+00
  9.0000-09  0.   0+00
  1.0000-08  0.   0+00
  1.1000-08  0.   0+00
  1.2000-08  0.   0+00
  1.3000-08  5.0000+00
  1.4000-08  5.0000+00
  1.5000-08  5.0000+00
  1.6000-08  5.0000+00
  1.7000-08  5.0000+00
  1.8000-08  5.0000+00
  1.9000-08  5.0000+00
  2.0000-08  5.0000+00
```

AD-A151 832 ANALYSIS OF THE CAPABILITY TO EFFECTIVELY DESIGN COMPLEMENTARY METAL OXID..(U) AIR FORCE INST OF TECH WRIGHT-PATTERSON AFB OH SCHOOL OF ENGI.. M L MCCONKEY 2/2

UNCLASSIFIED DEC 84 AFIT/GE/ENG/84D-44 F/G 9/5 NL

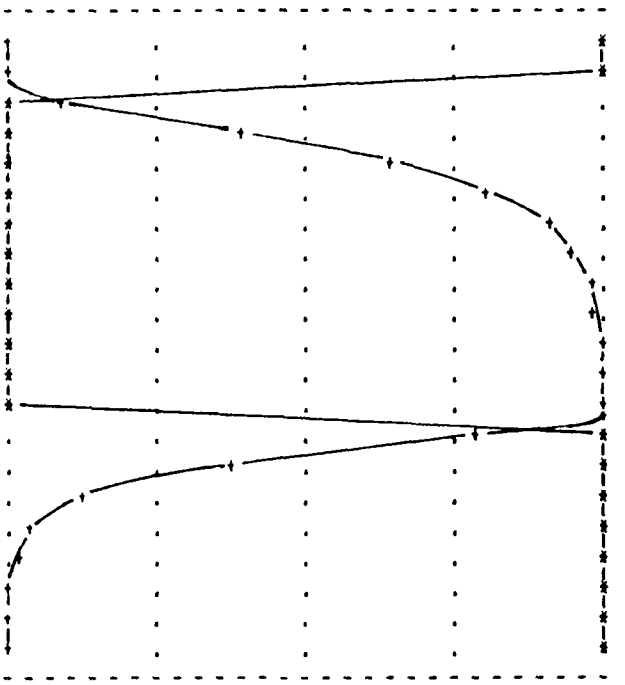




```
1********08/10/84 ********  SPICE 2G.1 (15OCT80)  ********01:10:23*****

0          CMOS/BULK 3-IN NAND TRANSIENT ANALYSIS

0****     INPUT LISTING                    TEMPERATURE =   27.000 DEG C

0******************************************************************************

 .WIDTH OUT=80
 .OPTIONS ITL1=500 ITL5=0
 .MODEL NMOS NMOS (VTO=1V TOX=75NM UO=500 NSUB=1E15 LD=0.7UM)
 +LEVEL=1
 .MODEL PMOS PMOS (VTO=-1V TOX=75NM UO=300 NSUB=2.5E15 LD=0.7UM)
 +LEVEL=1
 VDD 1 0 DC 5V
 M1 1 5 4 1 PMOS L=5.0U W=10.0U
 M2 6 5 4 0 NMOS L=5.0U W=30.0U
 M3 1 7 4 1 PMOS L=5.0U W=10.0U
 M4 8 7 6 0 NMOS L=5.0U W=30.0U
 M5 0 9 8 0 NMOS L=5.0U W=30.0U
 M6 1 9 4 1 PMOS L=5.0U W=10.0U
 COUT 4 0 0.2PF
 VIN1 9 0 PULSE (5V 0V 1NS 0NS 0NS 10NS)      A pulses high-low-high
 VIN2 7 0 DC 5V                               B & C remain high
 VIN3 5 0 DC 5V
 .TRAN 1NS 20NS
 .PLOT TRAN V(9) V(4) (0V,5V)
 .END
1********08/10/84 ********  SPICE 2G.1 (15OCT80)  ********01:10:23*****

0          CMOS/BULK 3-IN NAND TRANSIENT ANALYSIS

0****     MOSFET MODEL PARAMETERS          TEMPERATURE =   27.000 DEG C

0******************************************************************************

               NMOS       PMOS
0TYPE          NMOS       PMOS
0LEVEL          1.000      1.000
0VTO            1.000     -1.000
0KP          2.30d-05   1.38d-05
0GAMMA          0.396      0.626
0PHI            0.576      0.624
0CJ          1.02d-04   1.61d-04
0TOX         7.50d-08   7.50d-08
0NSUB        1.00d+15   2.50d+15
0LD          7.00d-07   7.00d-07
0UO           500.000    300.000
```

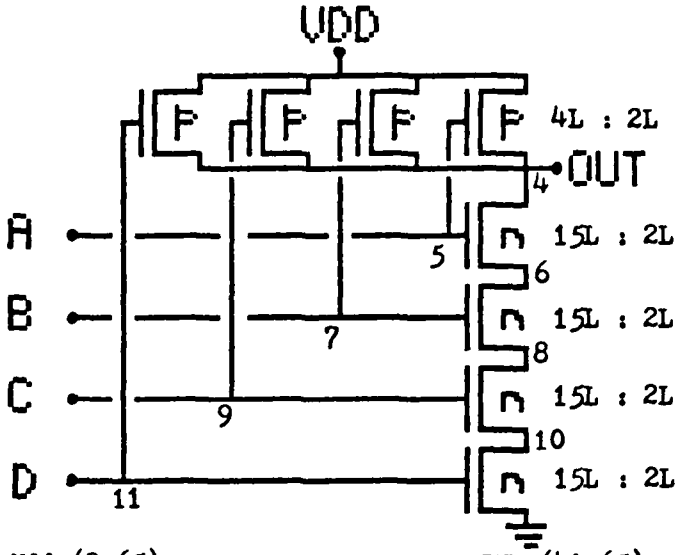
```
1********08/10/84 ********  SPICE 2G.1 (15OCT80)  *********01:10:25*****

0          CMOS/BULK 3-IN NAND TRANSIENT ANALYSIS

0****     INITIAL TRANSIENT SOLUTION       TEMPERATURE =   27.000 DEG C

0*****************************************************************************

  NODE   VOLTAGE     NODE   VOLTAGE     NODE   VOLTAGE     NODE   VOLTAGE

(  1)    5.0000    (  4)    0.0000    (  5)    5.0000    (  6)    0.0000

(  7)    5.0000    (  8)    0.0000    (  9)    5.0000

    VOLTAGE SOURCE CURRENTS

    NAME       CURRENT

    VDD      -2.080d-11

    VIN1      0.   d+00

    VIN2      0.   d+00

    VIN3      0.   d+00

    TOTAL POWER DISSIPATION   1.04d-10  WATTS

1********08/10/84 ********  SPICE 2G.1 (15OCT80)  *********01:10:25*****

0          CMOS/BULK 3-IN NAND TRANSIENT ANALYSIS

0****     OPERATING POINT INFORMATION      TEMPERATURE =   27.000 DEG C

0*****************************************************************************
0
0**** MOSFETS

0           M1        M2        M3        M4        M5        M6
0MODEL     PMOS      NMOS      PMOS      NMOS      NMOS      PMOS
 ID        0.  d+00 -2.08d-11  0.  d+00 -2.08d-11 -2.08d-11  0.  d+00
 VGS         5.000     5.000     5.000     5.000     5.000     5.000
 VDS         5.000    -0.000     5.000    -0.000    -0.000     5.000
 VBS         5.000    -0.000     5.000    -0.000    -0.000     5.000
1********06/10/84 ********  SPICE 2G.1 (15OCT80)  *********01:10:23*****

0          CMOS/BULK 3-IN NAND TRANSIENT ANALYSIS

0****     TRANSIENT ANALYSIS               TEMPERATURE =   27.000 DEG C

0*****************************************************************************
```

```
@LEGEND:

 *: V(9)
 +: V(4)
X
    TIME      V(9)

X(**)---------- 0.   d+00     1.250d+00     2.500d+00     3.750d+00  5.000d+00
```



```
 0.   d+00  5.000d+00
 1.000d-09  5.000d+00
 2.000d-09  0.   d+00
 3.000d-09  0.   d+00
 4.000d-09  0.   d+00
 5.000d-09  0.   d+00
 6.000d-09  0.   d+00
 7.000d-09  0.   d+00
 8.000d-09  0.   d+00
 9.000d-09  0.   d+00
 1.000d-08  0.   d+00
 1.100d-08  0.   d+00
 1.200d-08  0.   d+00
 1.300d-08  5.000d+00
 1.400d-08  5.000d+00
 1.500d-08  5.000d+00
 1.600d-08  5.000d+00
 1.700d-08  5.000d+00
 1.800d-08  5.000d+00
 1.900d-08  5.000d+00
 2.000d-08  5.000d+00
```

a)



b)

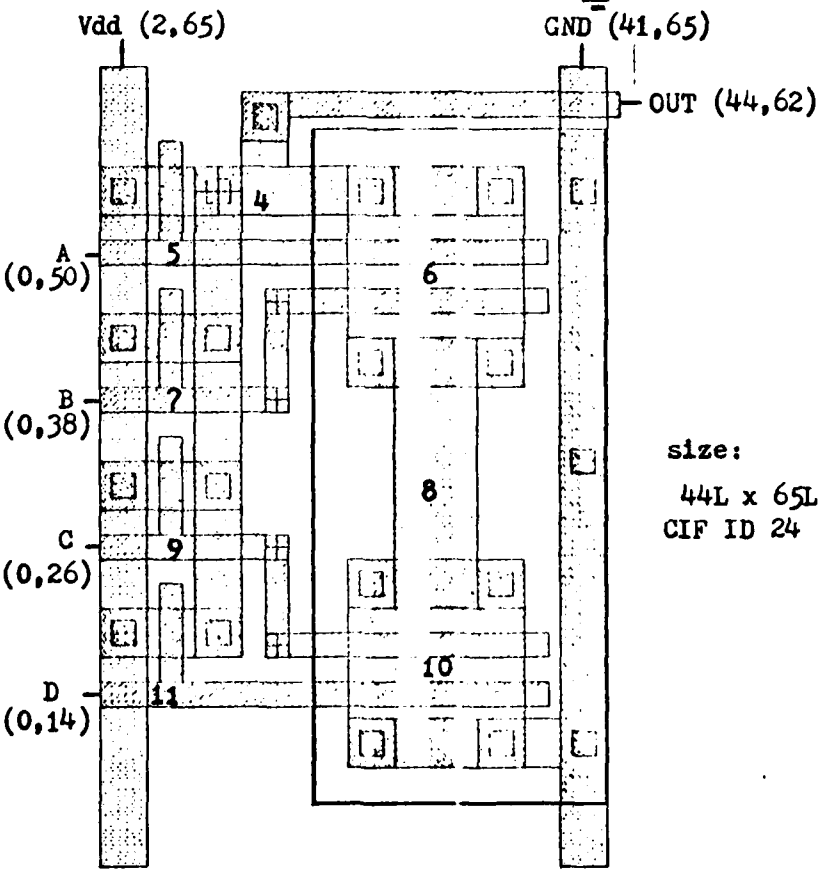
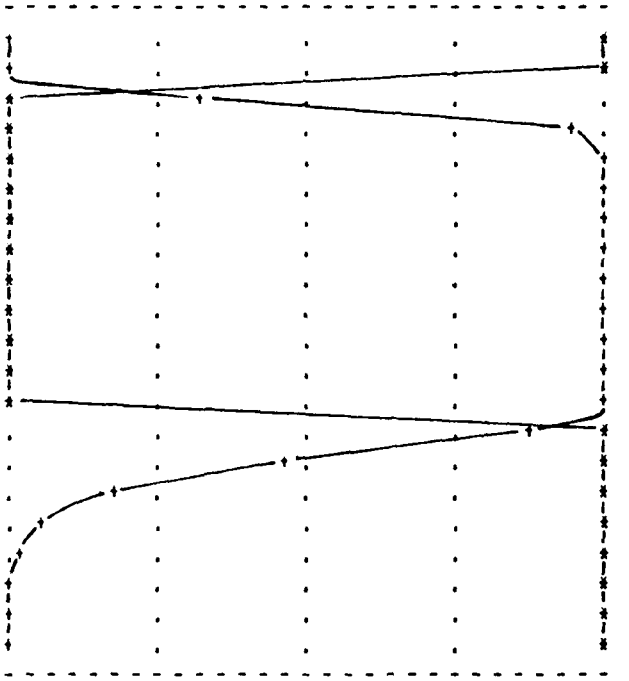


Figure D-5. 4-Input NAND Gate
a) schematic b) CLL plot

```
1********06/10/84 ********  SPICE 2G.1 (15OCT80)  ********01:17:12*****

0          CMOS/BULK 4-IN NAND TRANSIENT ANALYSIS

0*****     INPUT LISTING                    TEMPERATURE =   27.000 DEG C

0******************************************************************************

 .WIDTH OUT=80
 .OPTIONS ITL1=500 ITL5=0
 .MODEL NMOS NMOS (VTO=1V TOX=75NM UO=500 NSUB=1E15 LD=0.7UM)
 +LEVEL=1
 .MODEL PMOS PMOS (VTO=-1V TOX=75NM UO=300 NSUB=2.5E15 LD=0.7UM)
 +LEVEL=1
 VDD 1 0 DC 5V
 M1 1 5 4 1 PMOS L=5.0U W=10.0U
 M2 6 5 4 0 NMOS L=5.0U W=37.5U
 M3 8 7 6 0 NMOS L=5.0U W=37.5U
 M4 1 7 4 1 PMOS L=5.0U W=10.0U
 M5 1 9 4 1 PMOS L=5.0U W=10.0U
 M6 10 9 8 0 NMOS L=5.0U W=37.5U
 M7 1 11 4 1 PMOS L=5.0U W=10.0U
 M8 0 11 10 0 NMOS L=5.0U W=37.5U
 COUT 4 0 0.2PF
 VIN1 11 0 PULSE (5V 0V 1NS 0NS 0NS 10NS)   A-D pulse high-low-high
 VIN2 9 0 PULSE (5V 0V 1NS 0NS 0NS 10NS)
 VIN3 7 0 PULSE (5V 0V 1NS 0NS 0NS 10NS)
 VIN4 5 0 PULSE (5V 0V 1NS 0NS 0NS 10NS)
 .TRAN 1NS 20NS
 .PLOT TRAN V(11) V(4) (0V,5V)
 .END
1********06/10/84 ********  SPICE 2G.1 (15OCT80)  ********01:17:12*****

0          CMOS/BULK 4-IN NAND TRANSIENT ANALYSIS

0*****     MOSFET MODEL PARAMETERS          TEMPERATURE =   27.000 DEG C

0******************************************************************************

             NMOS       PMOS
0TYPE        NMOS       PMOS
0LEVEL        1.000      1.000
0VTO          1.000     -1.000
0KP        2.3ad-05   1.38d-05
0GAMMA        0.396      0.626
0PHI          0.576      0.624
0CJ        1.02d-04   1.61d-04
0TOX       7.50d-08   7.5ad-08
0NSUB      1.00d+15   2.50d+15
0LD        7.00d-07   7.00d-07
0UO         500.000    300.000
```

```
1********08/10/84 ********  SPICE 2G.1 (15OCT80)  ********01:17:12*****

0          CMOS/BULK 4-IN NAND TRANSIENT ANALYSIS

0****     INITIAL TRANSIENT SOLUTION       TEMPERATURE =   27.000 DEG C

0*****************************************************************************

  NODE   VOLTAGE     NODE   VOLTAGE     NODE   VOLTAGE     NODE   VOLTAGE

(  1)    5.0000    (  4)    0.0000    (  5)    5.0000    (  6)    0.0000

(  7)    5.0000    (  8)    0.0000    (  9)    5.0000    ( 10)    0.0000

( 11)    5.0000

    VOLTAGE SOURCE CURRENTS

    NAME       CURRENT

    VDD      -2.773d-11
    VIN1      0.   d+00
    VIN2      0.   d+00
    VIN3      0.   d+00
    VIN4      0.   d+00

    TOTAL POWER DISSIPATION   1.39d-10  WATTS

1********08/10/84 ********  SPICE 2G.1 (15OCT80)  ********01:17:12*****

0          CMOS/BULK 4-IN NAND TRANSIENT ANALYSIS

0*****     OPERATING POINT INFORMATION      TEMPERATURE =   27.000 DEG C

0*****************************************************************************
0
0**** MOSFETS

0            M1        M2        M3        M4        M5        M6        M7
0MODEL     PMOS      NMOS      NMOS      PMOS      PMOS      NMOS      PMOS
 ID        0.  d+00 -2.74d-11 -2.74d-11  0.  d+00  0.  d+00 -2.77d-11  0.  d+00
 VGS          5.000     5.000     5.000     5.000     5.000     5.000     5.000
 VDS          5.000    -0.000    -0.000     5.000     5.000    -0.000     5.000
 VBS          5.000    -0.000    -0.000     5.000     5.000    -0.000     5.000

0            M8
0MODEL     NMOS
 ID       -2.77d-11
 VGS          5.000
 VDS         -0.000
 VBS         -0.000
1********08/10/84 ********  SPICE 2G.1 (15OCT80)  ********01:17:12*****

0          CMOS/BULK 4-IN NAND TRANSIENT ANALYSIS

0*****     TRANSIENT ANALYSIS               TEMPERATURE =   27.000 DEG C

0*****************************************************************************
```

```
0LEGEND:

 *: V(11)
 +: V(4)
X
    TIME      V(11)

X(**)---------- 0.   d+00     1.250d+00     2.500d+00     3.750d+00  5.000d+00
```

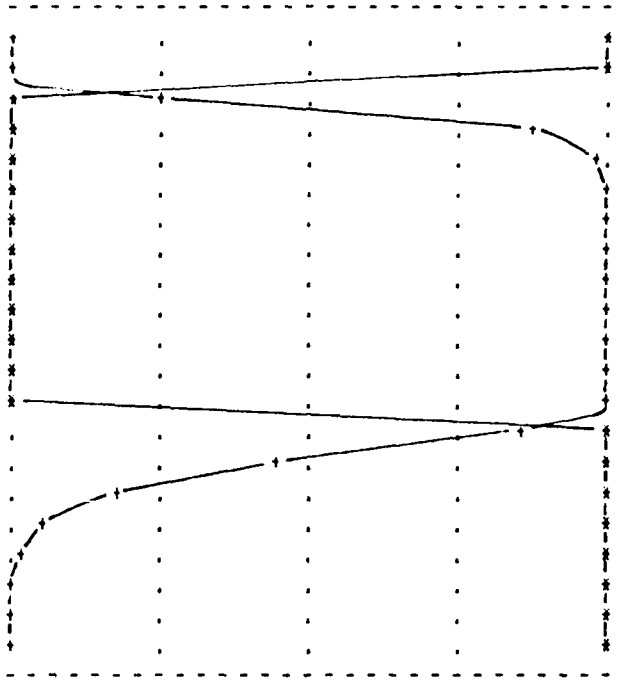


```
  0.   d+00  5.000d+00
  1.000d-09  5.000d+00
  2.000d-09 -1.388d-17
  3.000d-09  0.   d+00
  4.000d-09  0.   d+00
  5.000d-09  0.   d+00
  6.000d-09  0.   d+00
  7.000d-09  0.   d+00
  8.000d-09  0.   d+00
  9.000d-09  0.   d+00
  1.000d-08  0.   d+00
  1.100d-08  0.   d+00
  1.200d-08  0.   d+00
  1.300d-08  5.000d+00
  1.400d-08  5.000d+00
  1.500d-08  5.000d+00
  1.600d-08  5.000d+00
  1.700d-08  5.000d+00
  1.800d-08  5.000d+00
  1.900d-08  5.000d+00
  2.000d-08  5.000d+00
```

```
1********08/10/84 ********  SPICE 2G.1 (15OCT80)  ********01:16:31*****

0          CMOS/BULK 4-IN NAND TRANSIENT ANALYSIS

0*****     INPUT LISTING                    TEMPERATURE =   27.000 DEG C

*******************************************************************************

 .WIDTH OUT=80
 .OPTIONS ITL1=500 ITL5=0
 .MODEL NMOS NMOS (VTO=1V TOX=75NM UO=500 NSUB=1E15 LD=0.7UM)
 +LEVEL=1
 .MODEL PMOS PMOS (VTO=-1V TOX=75NM UO=300 NSUB=2.5E15 LD=0.7UM)
 +LEVEL=1
 VDD 1 0 DC 5V
 M1 1 5 4 1 PMOS L=5.0U W=10.0U
 M2 6 5 4 0 NMOS L=5.0U W=37.5U
 M3 8 7 6 0 NMOS L=5.0U W=37.5U
 M4 1 7 4 1 PMOS L=5.0U W=10.0U
 M5 1 9 4 1 PMOS L=5.0U W=10.0U
 M6 10 9 8 0 NMOS L=5.0U W=37.5U
 M7 1 11 4 1 PMOS L=5.0U W=10.0U
 M8 0 11 10 0 NMOS L=5.0U W=37.5U
 COUT 4 0 0.2PF
 VIN1 11 0 PULSE (5V 0V 1NS 0NS 0NS 10NS)      A-C pulse high-low-high
 VIN2 9 0 PULSE (5V 0V 1NS 0NS 0NS 10NS)       D remains high
 VIN3 7 0 PULSE (5V 0V 1NS 0NS 0NS 10NS)
 VIN4 5 0 DC 5V
 .TRAN 1NS 20NS
 .PLOT TRAN V(11) V(4) (0V,5V)
 .END
1********08/10/84 ********  SPICE 2G.1 (15OCT80)  ********01:16:31*****

0          CMOS/BULK 4-IN NAND TRANSIENT ANALYSIS

0*****     MOSFET MODEL PARAMETERS          TEMPERATURE =   27.000 DEG C

*******************************************************************************

              NMOS       PMOS
0TYPE         NMOS       PMOS
0LEVEL         1.000      1.000
0VTO           1.000     -1.000
0KP         2.30d-05   1.38d-05
0GAMMA         0.396      0.626
0PHI           0.576      0.624
0CJ         1.02d-04   1.01d-04
0TOX        7.50d-08   7.50d-08
0NSUB       1.00d+15   2.50d+15
0LD         7.00d-07   7.00d-07
0UO          500.000    300.000
```

```
1********08/10/84 ********  SPICE 2G.1 (15OCT80)  *********01:16:31*****

0          CMOS/BULK 4-IN NAND TRANSIENT ANALYSIS

0*****     INITIAL TRANSIENT SOLUTION       TEMPERATURE =   27.000 DEG C

0******************************************************************************

  NODE   VOLTAGE     NODE   VOLTAGE     NODE   VOLTAGE     NODE   VOLTAGE

(  1)    5.0000    (  4)    0.0000    (  5)    5.0000    (  6)    0.0000

(  7)    5.0000    (  8)    0.0000    (  9)    5.0000    ( 10)    0.0000

( 11)    5.0000

    VOLTAGE SOURCE CURRENTS

    NAME       CURRENT

    VDD      -2.773d-11
    VIN1      0.   d+00
    VIN2      0.   d+00
    VIN3      0.   d+00
    VIN4      0.   d+00

    TOTAL POWER DISSIPATION   1.39d-10  WATTS

1********08/10/84 ********  SPICE 2G.1 (15OCT80)  *********01:16:31*****

0          CMOS/BULK 4-IN NAND TRANSIENT ANALYSIS

0*****     OPERATING POINT INFORMATION      TEMPERATURE =   27.000 DEG C

0******************************************************************************
0
0***** MOSFETS

0           M1        M2        M3        M4        M5        M6        M7
0MODEL     PMOS      NMOS      NMOS      PMOS      PMOS      NMOS      PMOS
 ID        0.  d+00 -2.74d-11 -2.74d-11  0.  d+00  0.  d+00 -2.77d-11  0.  d+00
 VGS          5.000     5.000     5.000     5.000     5.000     5.000     5.000
 VDS          5.000    -0.000    -0.000     5.000     5.000    -0.000     5.000
 VBS          5.000    -0.000    -0.000     5.000     5.000    -0.000     5.000

0           M8
0MODEL     NMOS
 ID       -2.77d-11
 VGS          5.000
 VDS         -0.000
 VBS         -0.000
1********08/10/84 ********  SPICE 2G.1 (15OCT80)  *********01:16:31*****

0          CMOS/BULK 4-IN NAND TRANSIENT ANALYSIS

0*****     TRANSIENT ANALYSIS               TEMPERATURE =   27.000 DEG C

0******************************************************************************
```

```
LEGEND:

 *: V(11)
 +: V(4)
X
    TIME      V(11)

X(**)---------- 0.   0+00     1.250d+00     2.500d+00     3.750d+00  5.000d+00
```

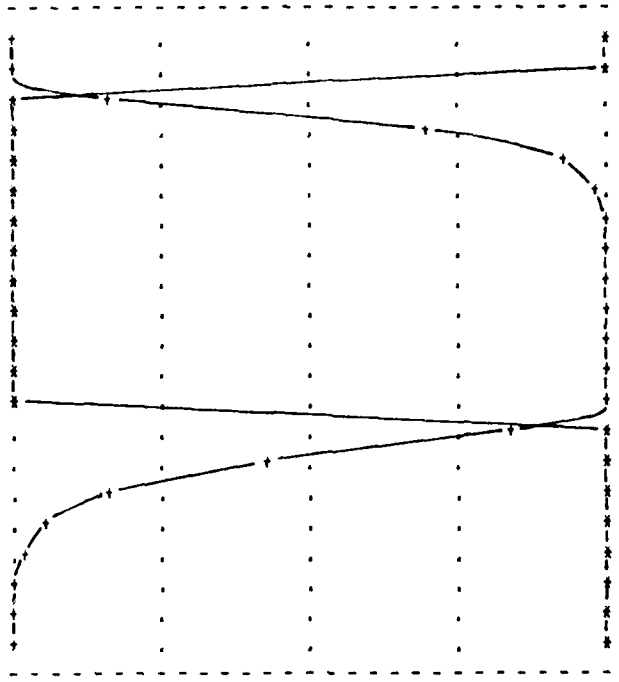


```
  0.   0+00  5.000d+00
  1.000d-09  5.000d+00
  2.000d-09  0.   d+00
  3.000d-09  0.   d+00
  4.000d-09  0.   d+00
  5.000d-09  0.   d+00
  6.000d-09  0.   d+00
  7.000d-09  0.   d+00
  8.000d-09  0.   d+00
  9.000d-09  0.   d+00
  1.000d-08  0.   d+00
  1.100d-08  0.   d+00
  1.200d-08  0.   d+00
  1.300d-08  5.000d+00
  1.400d-08  5.000d+00
  1.500d-08  5.000d+00
  1.600d-08  5.000d+00
  1.700d-08  5.000d+00
  1.800d-08  5.000d+00
  1.900d-08  5.000d+00
  2.000d-08  5.000d+00
```

```
1********08/10/84 ********  SPICE 2G.1 (15OCT80)  *********01:15:45*****

0           CMOS/BULK 4-IN NAND TRANSIENT ANALYSIS

0*****     INPUT LISTING                    TEMPERATURE =   27.000 DEG C

0******************************************************************************

 .WIDTH OUT=80
 .OPTIONS ITL1=500 ITL5=0
 .MODEL NMOS NMOS (VTO=1V TOX=75NM UO=500 NSUB=1E15 LD=0.7UM)
 +LEVEL=1
 .MODEL PMOS PMOS (VTO=-1V TOX=75NM UO=300 NSUB=2.5E15 LD=0.7UM)
 +LEVEL=1
 VDD 1 0 DC 5V
 M1 1 5 4 1 PMOS L=5.0U W=10.0U
 M2 6 5 4 0 NMOS L=5.0U W=37.5U
 M3 8 7 6 0 NMOS L=5.0U W=37.5U
 M4 1 7 4 1 PMOS L=5.0U W=10.0U
 M5 1 9 4 1 PMOS L=5.0U W=10.0U
 M6 10 9 8 0 NMOS L=5.0U W=37.5U
 M7 1 11 4 1 PMOS L=5.0U W=10.0U
 M8 0 11 10 0 NMOS L=5.0U W=37.5U
 COUT 4 0 0.2PF
 VIN1 11 0 PULSE (5V 0V 1NS 0NS 0NS 10NS)  A & B pulse high-low-high
 VIN2 9 0 PULSE (5V 0V 1NS 0NS 0NS 10NS)   C & D remain high
 VIN3 7 0 DC 5V
 VIN4 5 0 DC 5V
 .TRAN 1NS 20NS
 .PLOT TRAN V(11) V(4) (0V,5V)
 .END
1********08/10/84 ********  SPICE 2G.1 (15OCT80)  *********01:15:45*****

0           CMOS/BULK 4-IN NAND TRANSIENT ANALYSIS

0*****     MOSFET MODEL PARAMETERS          TEMPERATURE =   27.000 DEG C

0******************************************************************************

               NMOS       PMOS
0TYPE          NMOS       PMOS
0LEVEL          1.000      1.000
0VTO            1.000     -1.000
0KP          2.30d-05   1.38d-05
0GAMMA          0.396      0.626
0PHI            0.576      0.624
0CJ          1.02d-04   1.61d-04
0TOX         7.50d-08   7.50d-08
0NSUB        1.00d+15   2.50d+15
0LD          7.00d-07   7.00d-07
0UO           500.000    300.000
```

```
1********08/10/84 ********  SPICE 2G.1 (15OCT80)  ********01:15:45*****

0          CMOS/BULK 4-IN NAND TRANSIENT ANALYSIS

0*****     INITIAL TRANSIENT SOLUTION       TEMPERATURE =   27.000 DEG C

0******************************************************************************

  NODE   VOLTAGE     NODE   VOLTAGE     NODE   VOLTAGE     NODE   VOLTAGE

(  1)    5.0000    (  4)    0.0000    (  5)    5.0000    (  6)    0.0000

(  7)    5.0000    (  8)    0.0000    (  9)    5.0000    ( 10)    0.0000

( 11)    5.0000

    VOLTAGE SOURCE CURRENTS

    NAME        CURRENT

    VDD       -2.773d-11
    VIN1       0.   d+00
    VIN2       0.   d+00
    VIN3       0.   d+00
    VIN4       0.   d+00

    TOTAL POWER DISSIPATION   1.39d-10  WATTS

1********08/10/84 ********  SPICE 2G.1 (15OCT80)  ********01:15:45*****

0          CMOS/BULK 4-IN NAND TRANSIENT ANALYSIS

0*****     OPERATING POINT INFORMATION      TEMPERATURE =   27.000 DEG C

0******************************************************************************
0
0***** MOSFETS

0            M1         M2         M3         M4         M5         M6         M7
0MODEL      PMOS       NMOS       NMOS       PMOS       PMOS       NMOS       PMOS
 ID        0.  d+00 -2.74d-11 -2.74d-11  0.  d+00  0.  d+00 -2.77d-11  0.  d+00
 VGS          5.000      5.000      5.000      5.000      5.000      5.000      5.000
 VDS          5.000     -0.000     -0.000      5.000      5.000     -0.000      5.000
 VBS          5.000     -0.000     -0.000      5.000      5.000     -0.000      5.000

0            M6
0MODEL      NMOS
 ID       -2.77d-11
 VGS          5.000
 VDS         -0.000
 VBS         -0.000
1********08/10/84 ********  SPICE 2G.1 (15OCT80)  ********01:15:45*****

0          CMOS/BULK 4-IN NAND TRANSIENT ANALYSIS

0*****     TRANSIENT ANALYSIS               TEMPERATURE =   27.000 DEG C

0******************************************************************************
```

```
0LEGEND:

 *: V(11)
 +: V(4)
X
     TIME       V(11)

X(*+)------------ 0.   d+00      1.25ad+00      2.500d+00      3.75a0+00  5.000d+00
```

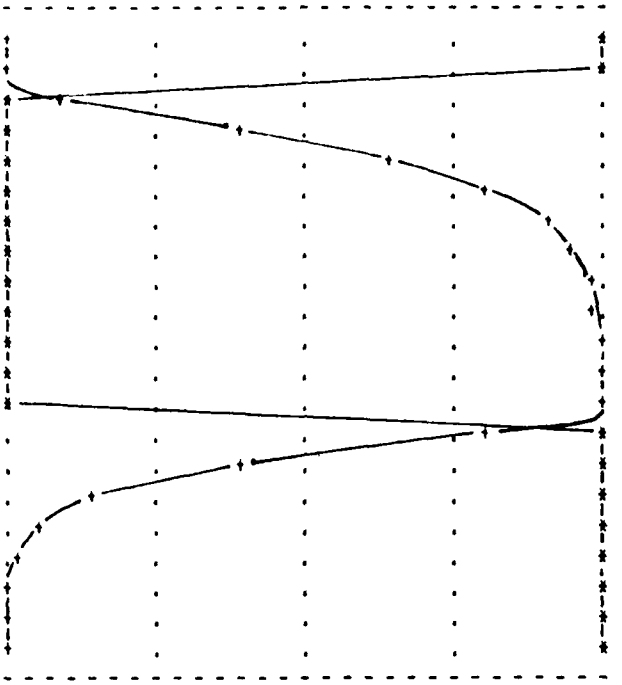


```
  0.   d+00  5.000d+00
  1.000d-09  5.000d+00
  2.000d-09  0.   d+00
  3.000d-09  0.   d+00
  4.000d-09  0.   d+00
  5.000d-09  0.   d+00
  6.000d-09  0.   d+00
  7.000d-09  0.   d+00
  8.000d-09  0.   d+00
  9.000d-09  0.   d+00
  1.000d-08  0.   d+00
  1.100d-08  0.   d+00
  1.200d-08  0.   d+00
  1.300d-08  5.000d+00
  1.400d-08  5.000d+00
  1.500d-08  5.000d+00
  1.600d-08  5.000d+00
  1.700d-08  5.000d+00
  1.800d-08  5.000d+00
  1.900d-08  5.000d+00
  2.000d-08  5.000d+00
```

```
1********08/10/84 ********  SPICE 2G.1 (15OCT80)  ********01:14:28*****

0          CMOS/BULK 4-IN NAND TRANSIENT ANALYSIS

0*****     INPUT LISTING                    TEMPERATURE =   27.000 DEG C

0******************************************************************************

 .WIDTH OUT=80
 .OPTIONS ITL1=500 ITL5=0
 .MODEL NMOS NMOS (VTO=1V TOX=75NM UO=500 NSUB=1E15 LD=0.7UM)
 +LEVEL=1
 .MODEL PMOS PMOS (VTO=-1V TOX=75NM UO=300 NSUB=2.5E15 LD=0.7UM)
 +LEVEL=1
 VDD 1 0 DC 5V
 M1 1 5 4 1 PMOS L=5.0U W=10.0U
 M2 6 5 4 0 NMOS L=5.0U W=37.5U
 M3 8 7 6 0 NMOS L=5.0U W=37.5U
 M4 1 7 4 1 PMOS L=5.0U W=10.0U
 M5 1 9 4 1 PMOS L=5.0U W=10.0U
 M6 10 9 8 0 NMOS L=5.0U W=37.5U
 M7 1 11 4 1 PMOS L=5.0U W=10.0U
 M8 0 11 10 0 NMOS L=5.0U W=37.5U
 COUT 4 0 0.2PF
 VIN1 11 0 PULSE (5V 0V 1NS 0NS 0NS 10NS)     A pulses high-low-high
 VIN2 9 0 DC 5V                               B, C, & D remain high
 VIN3 7 0 DC 5V
 VIN4 5 0 DC 5V
 .TRAN 1NS 20NS
 .PLOT TRAN V(11) V(4) (0V,5V)
 .END
1********08/10/84 ********  SPICE 2G.1 (15OCT80)  ********01:14:28*****

0          CMOS/BULK 4-IN NAND TRANSIENT ANALYSIS

0*****     MOSFET MODEL PARAMETERS          TEMPERATURE =   27.000 DEG C

0******************************************************************************

             NMOS       PMOS
0TYPE        NMOS       PMOS
0LEVEL         1.000      1.000
0VTO           1.000     -1.000
0KP         2.30d-05   1.38d-05
0GAMMA         0.396      0.626
0PHI           0.576      0.624
0CJ         1.02d-04   1.61d-04
0TOX        7.50d-08   7.50d-08
0NSUB       1.00d+15   2.50d+15
0LD         7.00d-07   7.00d-07
0UO          500.000    300.000
```

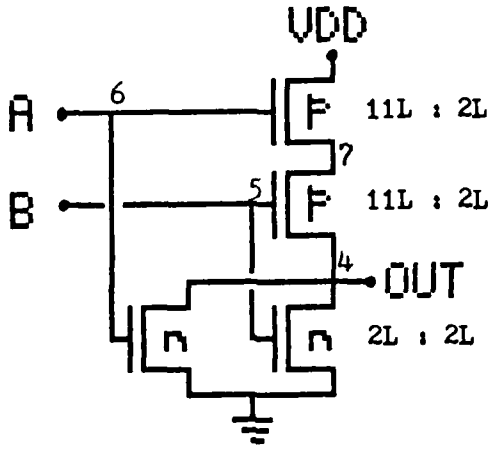
```
1********08/10/84 ********  SPICE 2G.1 (15OCT80)  ********01:14:28*****

0          CMOS/BULK 4-IN NAND TRANSIENT ANALYSIS

0*****     INITIAL TRANSIENT SOLUTION       TEMPERATURE =   27.000 DEG C

0********************************************************************************

  NODE   VOLTAGE     NODE   VOLTAGE     NODE   VOLTAGE     NODE   VOLTAGE

(  1)    5.0000    (  4)    0.0000    (  5)    5.0000    (  6)    0.0000

(  7)    5.0000    (  8)    0.0000    (  9)    5.0000    ( 10)    0.0000

( 11)    5.0000

    VOLTAGE SOURCE CURRENTS

    NAME       CURRENT

    VDD      -2.773d-11
    VIN1      0.   d+00
    VIN2      0.   d+00
    VIN3      0.   d+00
    VIN4      0.   d+00

    TOTAL POWER DISSIPATION   1.39d-10  WATTS

1********06/10/84 ********  SPICE 2G.1 (15OCT80)  ********01:14:28*****

0          CMOS/BULK 4-IN NAND TRANSIENT ANALYSIS

0*****     OPERATING POINT INFORMATION      TEMPERATURE =   27.000 DEG C

0********************************************************************************
0
0***** MOSFETS

0           M1        M2        M3        M4        M5        M6        M7
0MODEL     PMOS      NMOS      NMOS      PMOS      PMOS      NMOS      PMOS
 ID        0.  0+00 -2.74d-11 -2.74d-11  0.  0+00  0.  0+00 -2.77d-11  0.  0+00
 VGS         5.000     5.000     5.000     5.000     5.000     5.000     5.000
 VDS         5.000    -0.000    -0.000     5.000     5.000    -0.000     5.000
 VBS         5.000    -0.000    -0.000     5.000     5.000    -0.000     5.000

0           M8
0MODEL     NMOS
 ID       -2.77d-11
 VGS         5.000
 VDS        -0.000
 VBS        -0.000
1********08/10/84 ********  SPICE 2G.1 (15OCT80)  ********01:14:28*****

0          CMOS/BULK 4-IN NAND TRANSIENT ANALYSIS

0*****     TRANSIENT ANALYSIS               TEMPERATURE =   27.000 DEG C

0********************************************************************************
```

```
0LEGEND:

 *: V(11)
 +: V(4)
X
     TIME       V(11)

X(**)---------- 0.   0+00      1.25E0+00      2.500E+00      3.75E0+00  5.000E+00
```



```
  0.   0+00  5.000E+00
 1.000E-09  5.000E+00
 2.000E-09  0.   0+00
 3.000E-09  0.   0+00
 4.000E-09  0.   0+00
 5.000E-09  0.   0+00
 6.000E-09  0.   0+00
 7.000E-09  0.   0+00
 8.000E-09  0.   0+00
 9.000E-09  0.   0+00
 1.000E-08  0.   0+00
 1.100E-08  0.   0+00
 1.200E-08  0.   0+00
 1.300E-08  5.000E+00
 1.400E-08  5.000E+00
 1.500E-08  5.000E+00
 1.600E-08  5.000E+00
 1.700E-08  5.000E+00
 1.800E-08  5.000E+00
 1.900E-08  5.000E+00
 2.000E-08  5.000E+00
```

a)



b)

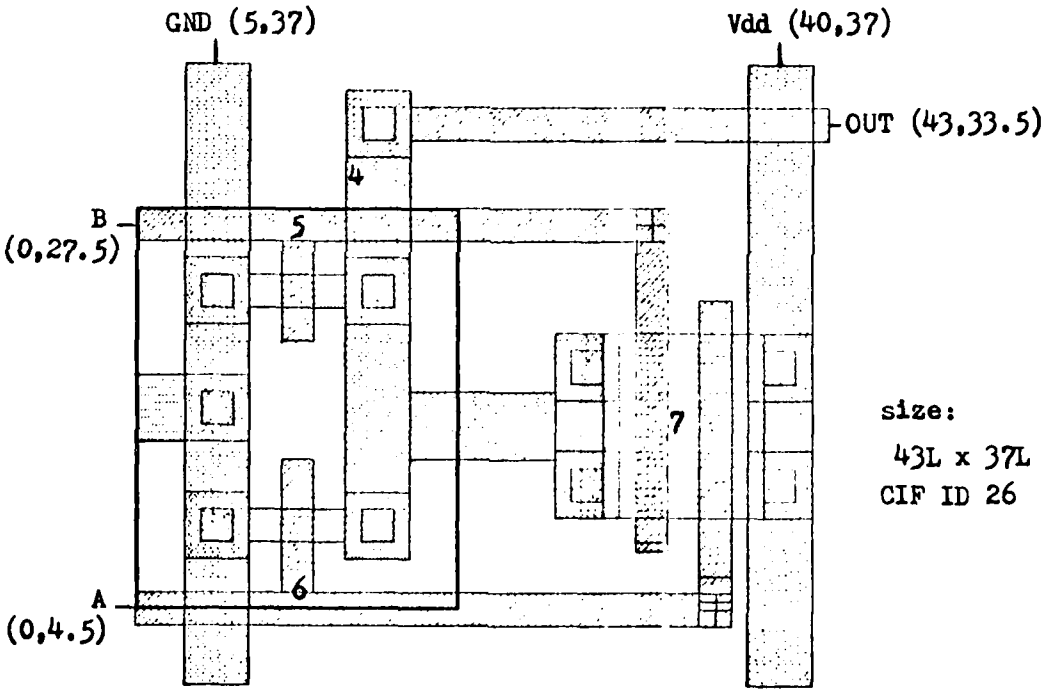
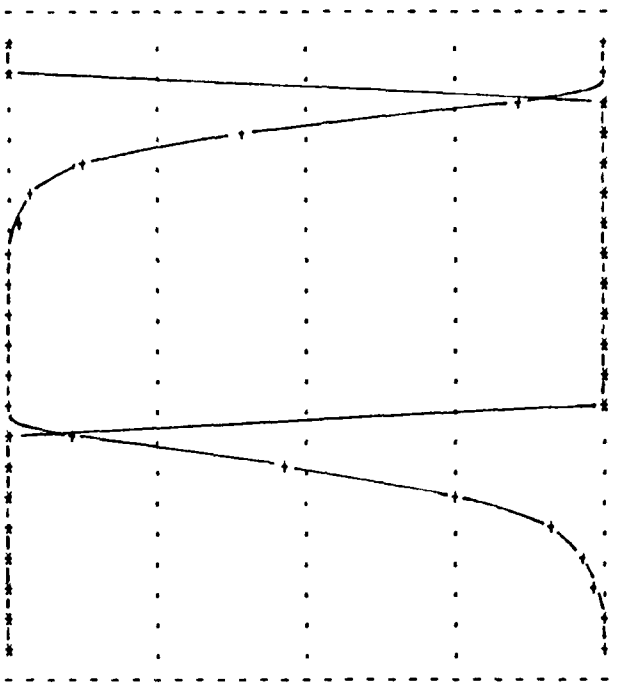


Figure D-6. 2-Input NOR Gate
a) schematic b) CLL plot

```
1********08/10/84 ********  SPICE 2G.1 (15OCT8Ø)  ********01:47:27*****

Ø   CMOS/BULK 2-IN NOR TRANSIENT ANALYSIS

Ø*****     INPUT LISTING                    TEMPERATURE =   27.ØØØ DEG C

Ø******************************************************************************

 .WIDTH OUT=8Ø
 .OPTIONS ITL1=5ØØ ITL5=Ø
 .MODEL NMOS NMOS (VTO=1V TOX=75NM UO=5ØØ NSUB=1E15 LD=Ø.7UM)
 +LEVEL=1
 .MODEL PMOS PMOS (VTO=-1V TOX=75NM UO=3ØØ NSUB=2.5E15 LD=Ø.7UM)
 +LEVEL=1
 VDD 1 Ø DC 5V
 M1 Ø 5 4 Ø NMOS L=5.ØU W=5.ØU
 M2 7 6 1 1 PMOS L=5.ØU W=27.5U
 M3 4 5 7 1 PMOS L=5.ØU W=27.5U
 M4 Ø 6 4 Ø NMOS L=5.ØU W=5.ØU
 COUT 4 Ø Ø.2PF
 VIN1 6 Ø PULSE (ØV 5V 1NS ØNS ØNS 1ØNS)   A & B pulse low-high-low
 VIN2 5 Ø PULSE (ØV 5V 1NS ØNS ØNS 1ØNS)
 .TRAN 1NS 2ØNS
 .PLOT TRAN V(6) V(4) (ØV,5V)
 .END
1********08/10/84 ********  SPICE 2G.1 (15OCT8Ø)  ********01:47:27*****

Ø   CMOS/BULK 2-IN NOR TRANSIENT ANALYSIS

Ø*****     MOSFET MODEL PARAMETERS          TEMPERATURE =   27.ØØØ DEG C

Ø******************************************************************************

             NMOS       PMOS
ØTYPE        NMOS       PMOS
ØLEVEL        1.ØØØ      1.ØØØ
ØVTO          1.ØØØ     -1.ØØØ
ØKP        2.3Ød-Ø5   1.38d-Ø5
ØGAMMA        Ø.396      Ø.626
ØPHI          Ø.576      Ø.624
ØCJ        1.Ø2d-Ø4   1.61d-Ø4
ØTOX       7.5Ød-Ø8   7.5Ød-Ø8
ØNSUB      1.ØØd+15   2.5Ød+15
ØLD        7.ØØd-Ø7   7.ØØd-Ø7
ØUO         5ØØ.ØØØ    3ØØ.ØØØ
```

```
1********08/10/84 ********  SPICE 2G.1 (15OCT80)  *********01:47:27*****

0   CMOS/BULK 2-IN NOR TRANSIENT ANALYSIS

0*****     INITIAL TRANSIENT SOLUTION       TEMPERATURE =   27.000 DEG C

0******************************************************************************

  NODE   VOLTAGE     NODE   VOLTAGE     NODE   VOLTAGE     NODE   VOLTAGE

(  1)    5.0000    (  4)    5.0000    (  5)    0.        (  6)    0.

(  7)    5.0000

     VOLTAGE SOURCE CURRENTS

     NAME       CURRENT

     VDD      -1.387d-11

     VIN1      0.   d+00

     VIN2      0.   d+00

     TOTAL POWER DISSIPATION   6.93d-11  WATTS

1********08/10/84 ********  SPICE 2G.1 (15OCT80)  *********01:47:27*****

0   CMOS/BULK 2-IN NOR TRANSIENT ANALYSIS

0*****     OPERATING POINT INFORMATION      TEMPERATURE =   27.000 DEG C

0******************************************************************************
0
0***** MOSFETS

0            M1         M2         M3         M4
0MODEL     NMOS       PMOS       PMOS       NMOS
 ID        0.  d+00 -1.38d-11 -1.39d-11  0.  d+00
 VGS        -5.000     -5.000     -5.000     -5.000
 VDS        -5.000     -0.000     -0.000     -5.000
 VBS        -5.000      0.         0.000     -5.000
1********08/10/84 ********  SPICE 2G.1 (15OCT80)  *********01:47:27*****

0   CMOS/BULK 2-IN NOR TRANSIENT ANALYSIS

0*****     TRANSIENT ANALYSIS               TEMPERATURE =   27.000 DEG C

0******************************************************************************
```

```
LEGEND:

 *: V(6)
 +: V(4)
X
     TIME       V(6)

X(**)---------- 0.   d+00      1.25ad+00      2.5ad+00      3.75ad+00  5.ad+00
```



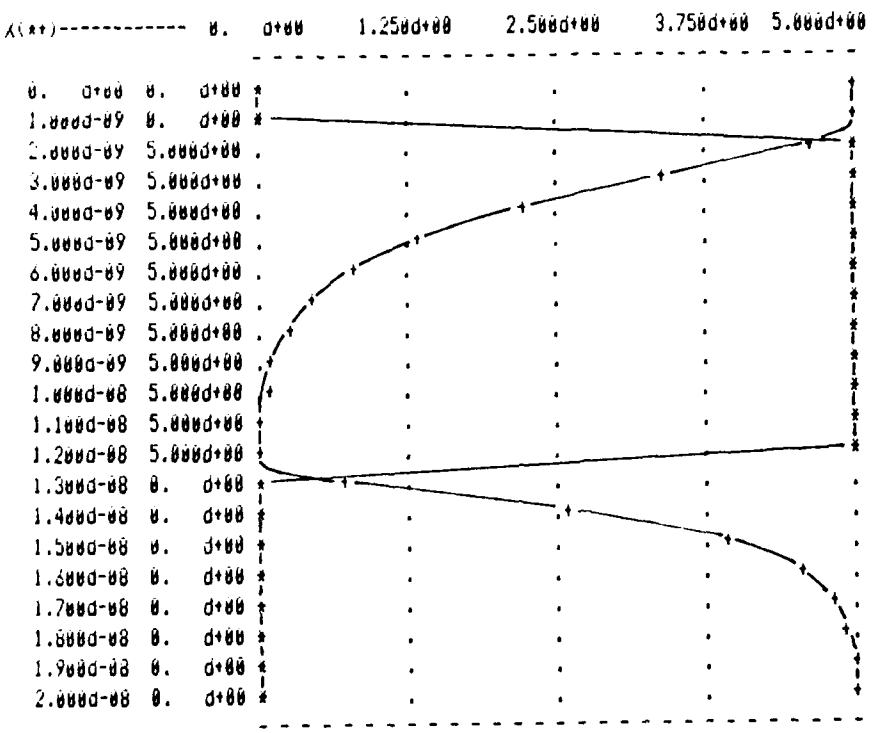
```
  0.   d+00  0.   d+00
  1.ad-09    0.   d+00
  2.ad-09    5.ad+00
  3.ad-09    5.ad+00
  4.ad-09    5.ad+00
  5.ad-09    5.ad+00
  6.ad-09    5.ad+00
  7.ad-09    5.ad+00
  8.ad-09    5.ad+00
  9.ad-09    5.ad+00
  1.ad-08    5.ad+00
  1.1ad-08   5.ad+00
  1.2ad-08   5.ad+00
  1.3ad-08   0.   d+00
  1.4ad-08   0.   d+00
  1.5ad-08   0.   d+00
  1.6ad-08   0.   d+00
  1.7ad-08   0.   d+00
  1.8ad-08   0.   d+00
  1.9ad-08   0.   d+00
  2.ad-08    0.   d+00
```

```
1********08/10/84 ********  SPICE 2G.1 (15OCT80)  ********01:48:02*****

0    CMOS/BULK 2-IN NOR TRANSIENT ANALYSIS

0*****     INPUT LISTING                    TEMPERATURE =   27.000 DEG C

0******************************************************************************

 .WIDTH OUT=80
 .OPTIONS ITL1=500 ITL5=0
 .MODEL NMOS NMOS (VTO=1V TOX=75NM UO=500 NSUB=1E15 LD=0.7UM)
 +LEVEL=1
 .MODEL PMOS PMOS (VTO=-1V TOX=75NM UO=300 NSUB=2.5E15 LD=0.7UM)
 +LEVEL=1
 VDD 1 0 DC 5V
 M1 0 5 4 0 NMOS L=5.0U W=5.0U
 M2 7 6 1 1 PMOS L=5.0U W=27.5U
 M3 4 5 7 1 PMOS L=5.0U W=27.5U
 M4 0 6 4 0 NMOS L=5.0U W=5.0U
 COUT 4 0 0.2PF
 VIN1 6 0 PULSE (0V 5V 1NS 0NS 0NS 10NS)     A pulses low-high-low
 VIN2 5 0 DC 0V                              B remains low
 .TRAN 1NS 20NS
 .PLOT TRAN V(6) V(4) (0V,5V)
 .END
1********08/10/84 ********  SPICE 2G.1 (15OCT80)  ********01:48:02*****

0    CMOS/BULK 2-IN NOR TRANSIENT ANALYSIS

0*****     MOSFET MODEL PARAMETERS          TEMPERATURE =   27.000 DEG C

0******************************************************************************

             NMOS       PMOS
0TYPE        NMOS       PMOS
0LEVEL        1.000      1.000
0VTO          1.000     -1.000
0KP        2.30d-05   1.38d-05
0GAMMA        0.396      0.626
0PHI          0.576      0.624
0CJ        1.02d-04   1.61d-04
0TOX       7.50d-08   7.50d-08
0NSUB      1.00d+15   2.50d+15
0LD        7.00d-07   7.00d-07
0UO         500.000    300.000
```

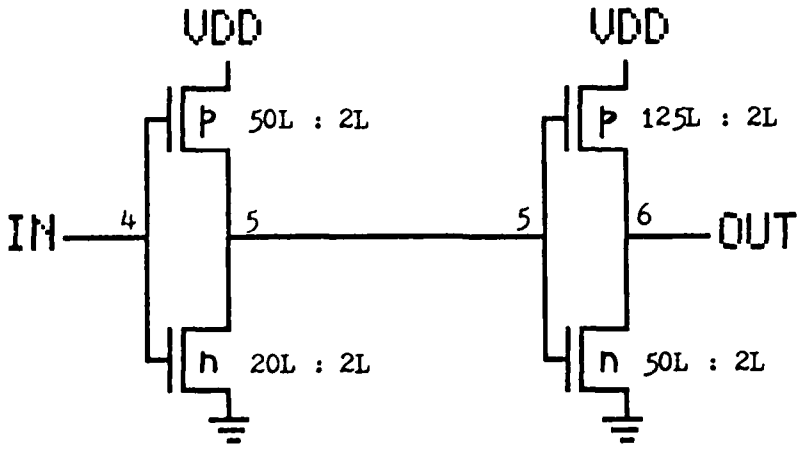
```
1********08/10/84 ********  SPICE 2G.1 (15OCT80)  ********01:48:02*****

0    CMOS/BULK 2-IN NOR TRANSIENT ANALYSIS

0****     INITIAL TRANSIENT SOLUTION       TEMPERATURE =   27.000 DEG C

0*****************************************************************************

  NODE   VOLTAGE     NODE   VOLTAGE     NODE   VOLTAGE     NODE   VOLTAGE

(  1)    5.0000    (  4)    5.0000    (  5)    0.        (  6)    0.

(  7)    5.0000

    VOLTAGE SOURCE CURRENTS

    NAME        CURRENT

    VDD       -1.587d-11

    VIN1       0.   d+00

    VIN2       0.   d+00

    TOTAL POWER DISSIPATION   6.93d-11  WATTS

1********08/10/84 ********  SPICE 2G.1 (15OCT80)  ********01:48:02*****

0    CMOS/BULK 2-IN NOR TRANSIENT ANALYSIS

0****     OPERATING POINT INFORMATION      TEMPERATURE =   27.000 DEG C

0*****************************************************************************
0
0**** MOSFETS

0             M1         M2         M3         M4
0MODEL      NMOS       PMOS       PMOS       NMOS
 ID         0.  d+00 -1.38d-11 -1.39d-11  0.  d+00
 VGS          -5.000     -5.000     -5.000     -5.000
 VDS          -5.000     -0.000     -0.000     -5.000
 VBS          -5.000      0.         0.000     -5.000
1********08/10/84 ********  SPICE 2G.1 (15OCT80)  ********01:48:02*****

0    CMOS/BULK 2-IN NOR TRANSIENT ANALYSIS

0****     TRANSIENT ANALYSIS               TEMPERATURE =   27.000 DEG C

0*****************************************************************************
```

0LEGEND:

*: V(6)
+: V(4)
X
TIME V(6)



a)



b)

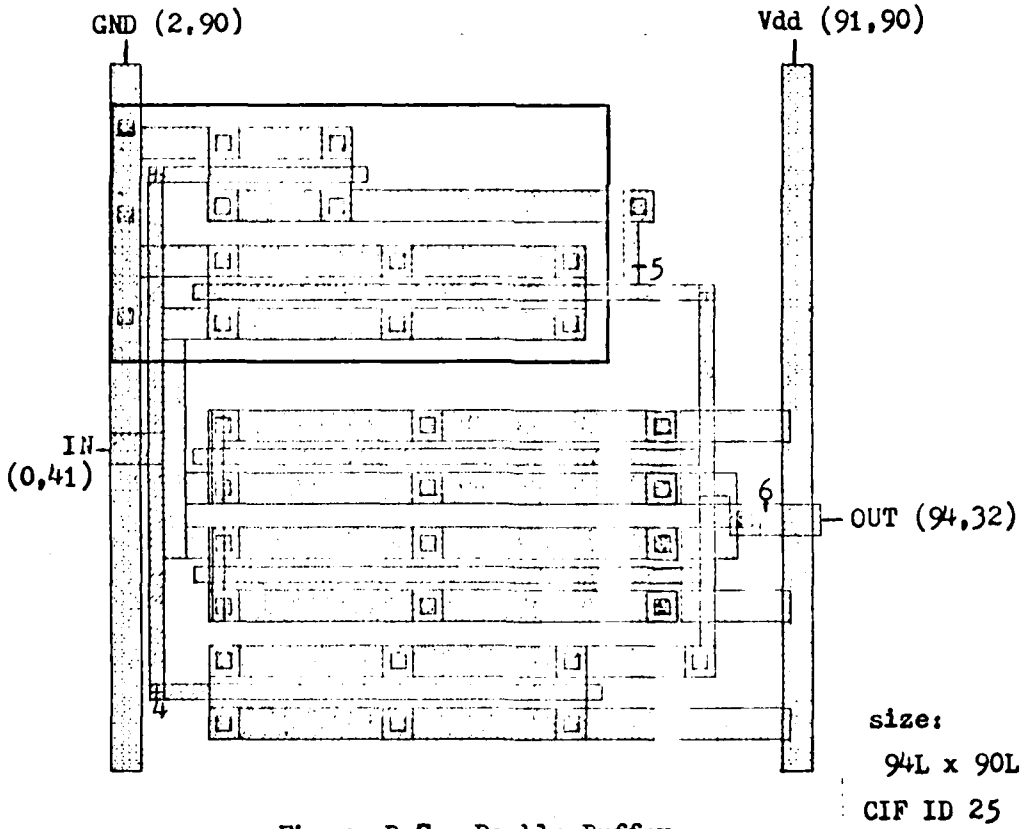


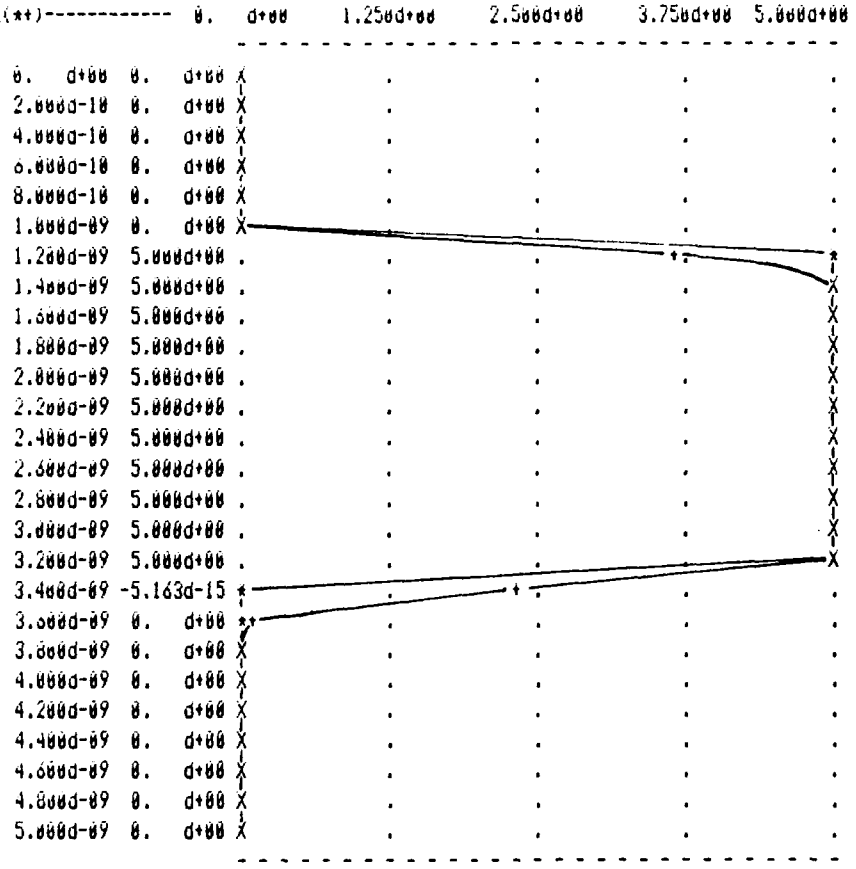
Figure D-7. Double Buffer
a) schematic b) CLL plot

cat *.spout

```
1********08/10/84 ********  SPICE 2G.1 (15OCT80)  ********14:19:58*****

0   CMOS/BULK DOUBLE BUFFER TRANSIENT ANALYSIS

0*****     INPUT LISTING                    TEMPERATURE =   27.000 DEG C

******************************************************************************

 .WIDTH OUT=80
 .OPTIONS ITL1=500 ITL5=0
 .MODEL NMOS NMOS (VTO=1V TOX=75NM UO=500 NSUB=1E15 LD=0.7UM)
 +LEVEL=1
 .MODEL PMOS PMOS (VTO=-1V TOX=75NM UO=300 NSUB=2.5E15 LD=0.7UM)
 +LEVEL=1
 VDD 1 0 DC 5V
 M1 5 4 0 0 NMOS L=5.0U W=47.5U
 M2 6 5 0 0 NMOS L=5.0U W=125.0U
 M3 6 5 1 1 PMOS L=5.0U W=156.3U
 M4 1 5 6 1 PMOS L=5.0U W=156.3U
 M5 1 4 5 1 PMOS L=5.0U W=125.0U
 COUT 6 0 0.2PF
 VIN1 4 0 PULSE (0V 5V 1NS 0NS 0NS 2NS)
 .TRAN 0.2NS 5NS
 .PLOT TRAN V(4) V(6) (0V,5V)
 .END
1********08/10/84 ********  SPICE 2G.1 (15OCT80)  ********14:19:58*****

0   CMOS/BULK DOUBLE BUFFER TRANSIENT ANALYSIS

0*****     MOSFET MODEL PARAMETERS          TEMPERATURE =   27.000 DEG C

******************************************************************************

             NMOS       PMOS
0TYPE        NMOS       PMOS
0LEVEL        1.000      1.000
0VTO          1.000     -1.000
0KP        2.30d-05   1.38d-05
0GAMMA        0.396      0.626
0PHI          0.576      0.624
0CJ        1.02d-04   1.01d-04
0TOX       7.50d-08   7.50d-08
0NSUB      1.00d+15   2.50d+15
0LD        7.00d-07   7.00d-07
0UO         500.000    300.000
```

```
1********08/10/84 ********  SPICE 2G.1 (15OCT80)  ********14:19:58******

0   CMOS/BULK DOUBLE BUFFER TRANSIENT ANALYSIS

0*****     INITIAL TRANSIENT SOLUTION       TEMPERATURE =   27.000 DEG C

0*******************************************************************************

  NODE   VOLTAGE     NODE   VOLTAGE     NODE   VOLTAGE     NODE   VOLTAGE

(  1)    5.0000    (  4)    0.        (  5)    5.0000    (  6)    0.0000

     VOLTAGE SOURCE CURRENTS

     NAME        CURRENT

     VDD       -2.080d-11

     VIN1       0.   d+00

     TOTAL POWER DISSIPATION   1.04d-10  WATTS

1********08/10/84 ********  SPICE 2G.1 (15OCT80)  ********14:19:58******

0   CMOS/BULK DOUBLE BUFFER TRANSIENT ANALYSIS

0*****     OPERATING POINT INFORMATION      TEMPERATURE =   27.000 DEG C

0*******************************************************************************
0
0***** MOSFETS

0             M1         M2         M3         M4         M5
0MODEL      NMOS       NMOS       PMOS       PMOS       PMOS
 ID        1.93d-12  1.39d-11 -1.93d-12  0.  d+00  6.93d-12
 VGS          0.        5.000     -0.000     5.000     -5.000
 VDS          5.000     0.000     -5.000     5.000      0.000
 VBS          0.        0.         0.        5.000      0.000
1********08/10/84 ********  SPICE 2G.1 (15OCT80)  ********14:19:58******

0   CMOS/BULK DOUBLE BUFFER TRANSIENT ANALYSIS

0*****     TRANSIENT ANALYSIS               TEMPERATURE =   27.000 DEG C

0*******************************************************************************
```

```
@LEGEND:

 *: V(4)
 +: V(6)
X
    TIME      V(4)

X(**)---------- 0.   d+00     1.250d+00     2.500d+00     3.750d+00  5.000d+00
```



```
  0.   d+00  0.   d+00 X           .             .             .          .
  2.000d-10  0.   d+00 X           .             .             .          .
  4.000d-10  0.   d+00 X           .             .             .          .
  6.000d-10  0.   d+00 X           .             .             .          .
  8.000d-10  0.   d+00 X           .             .             .          .
  1.000d-09  0.   d+00 X           .             .             .          .
  1.200d-09  5.000d+00 .           .             .             .          *
  1.400d-09  5.000d+00 .           .             .             .          X
  1.600d-09  5.000d+00 .           .             .             .          X
  1.800d-09  5.000d+00 .           .             .             .          X
  2.000d-09  5.000d+00 .           .             .             .          X
  2.200d-09  5.000d+00 .           .             .             .          X
  2.400d-09  5.000d+00 .           .             .             .          X
  2.600d-09  5.000d+00 .           .             .             .          X
  2.800d-09  5.000d+00 .           .             .             .          X
  3.000d-09  5.000d+00 .           .             .             .          X
  3.200d-09  5.000d+00 .           .             .             .          X
  3.400d-09 -5.163d-15 *           .             .             .          .
  3.600d-09  0.   d+00 *+          .             .             .          .
  3.800d-09  0.   d+00 X           .             .             .          .
  4.000d-09  0.   d+00 X           .             .             .          .
  4.200d-09  0.   d+00 X           .             .             .          .
  4.400d-09  0.   d+00 X           .             .             .          .
  4.600d-09  0.   d+00 X           .             .             .          .
  4.800d-09  0.   d+00 X           .             .             .          .
  5.000d-09  0.   d+00 X           .             .             .          .
```

Appendix E. CIFPLOTS of Group 1 Pads

Presented are the CIFPLOTS for the Group 1 pads that are available for CMOS/BULK design work. All units shown in the figures are in lambda (L). The coordinates for the Vdd and GND buses are not given because they are not necessary for any design work. The pad frames should be used.

A description of the CIF layer names is as follows:

CLL Layer	CIF Layer
poly	UP
metal	UM
diff	UD
contact	UC
glass	UG
pwell	UPW
nwell	UNW
pplug	UPP
nplug	UNP
---	XP

A more complete description of the different layers can be found on page III-5 of chapter III of this thesis.

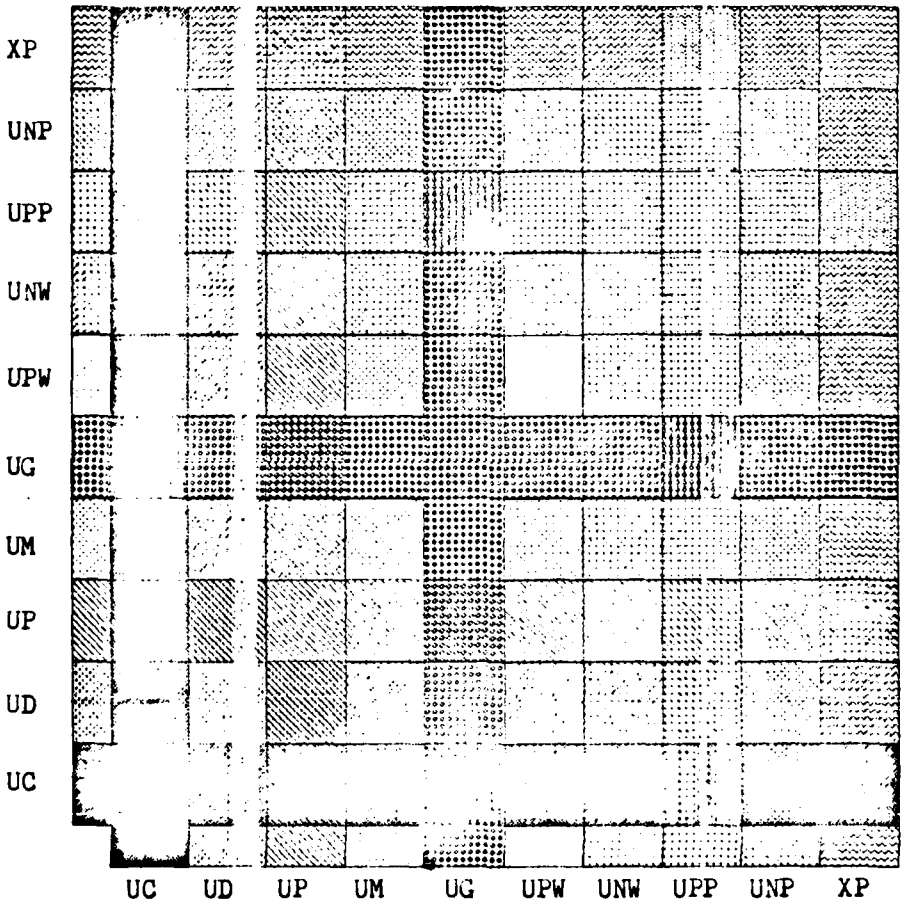
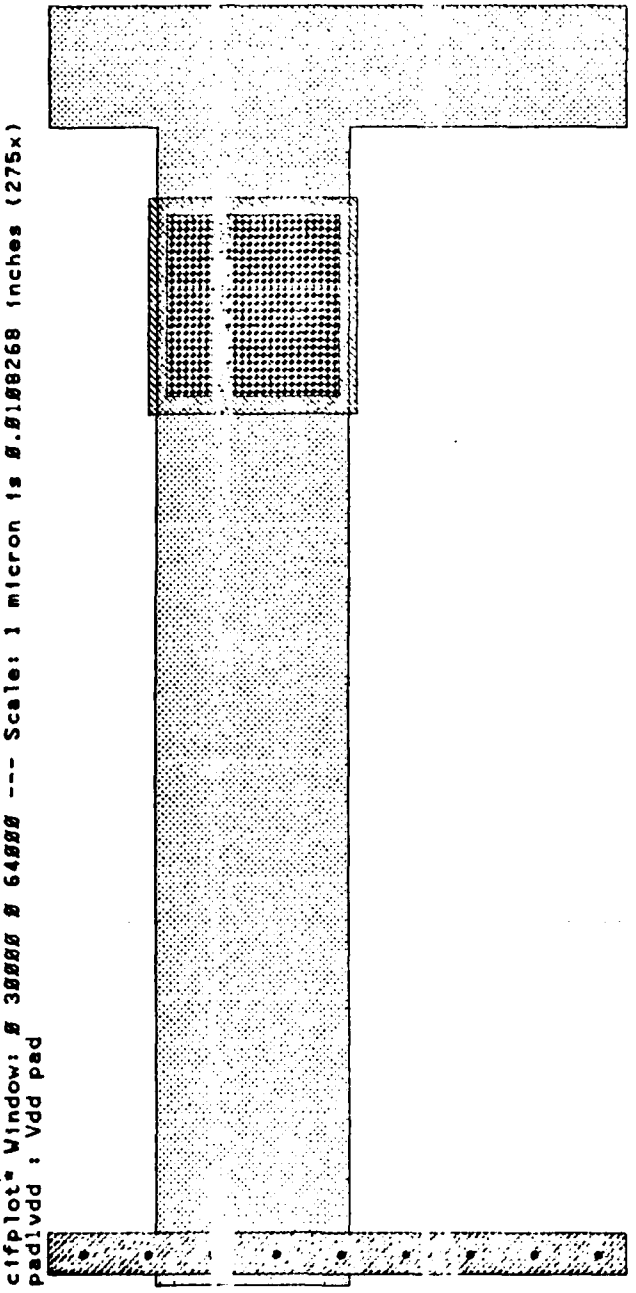
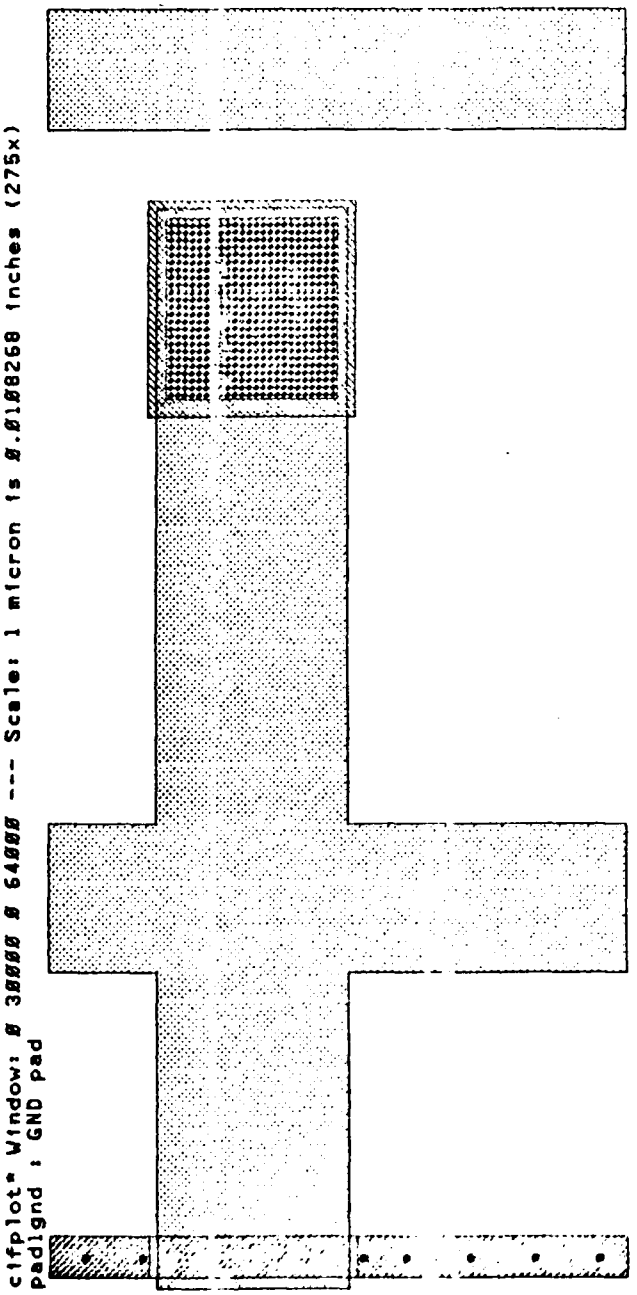


Figure E-1. CMOS/BULK CIF Layers



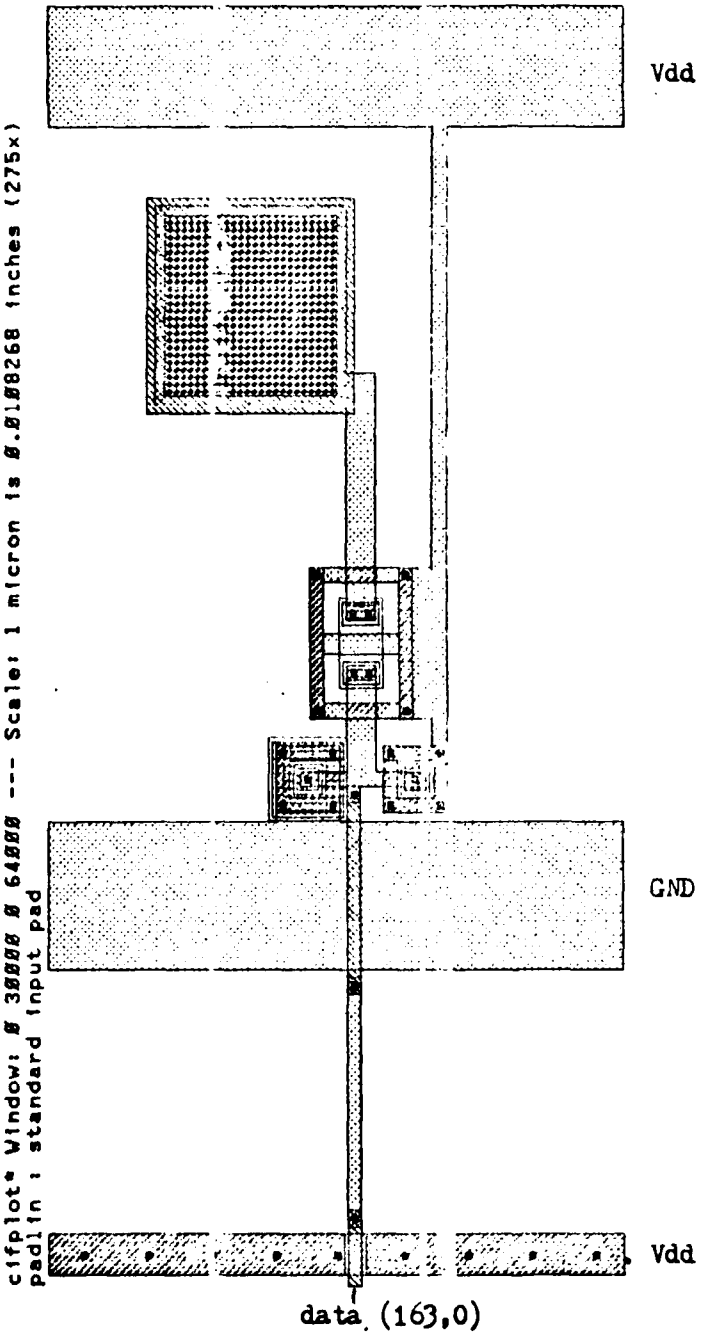
CIF ID 823

Figure E-2. pad1vdd



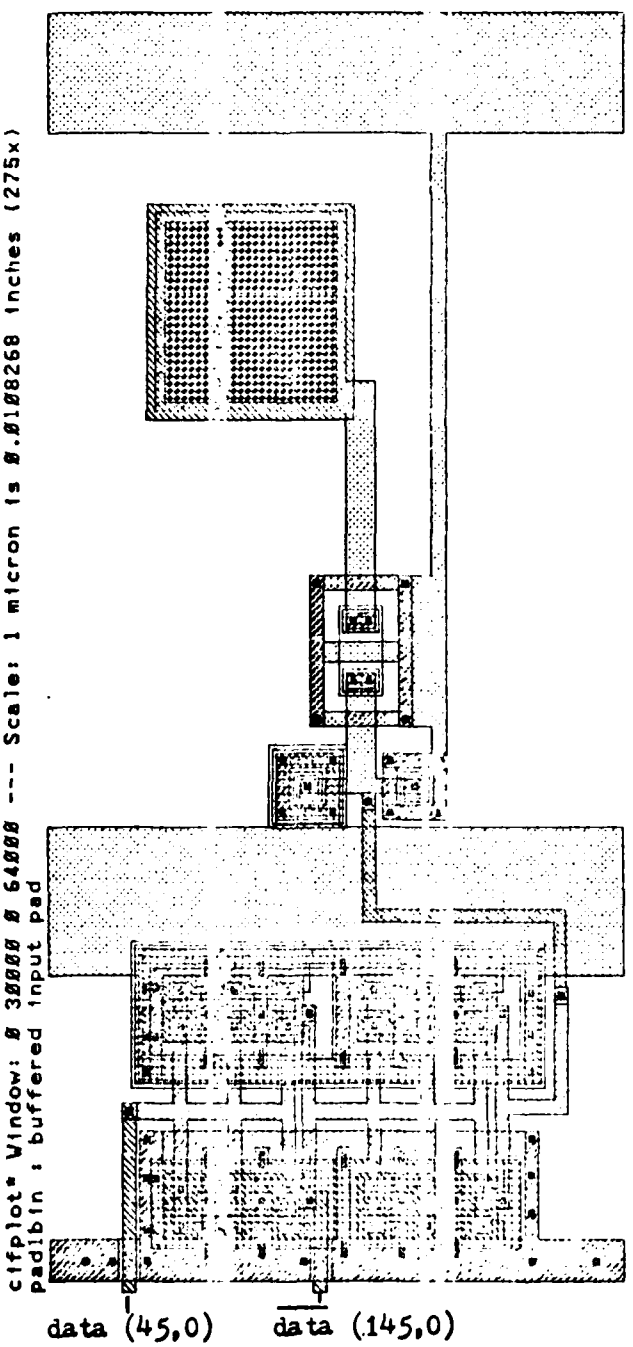
CIF ID 824

Figure E-3. padlgnd



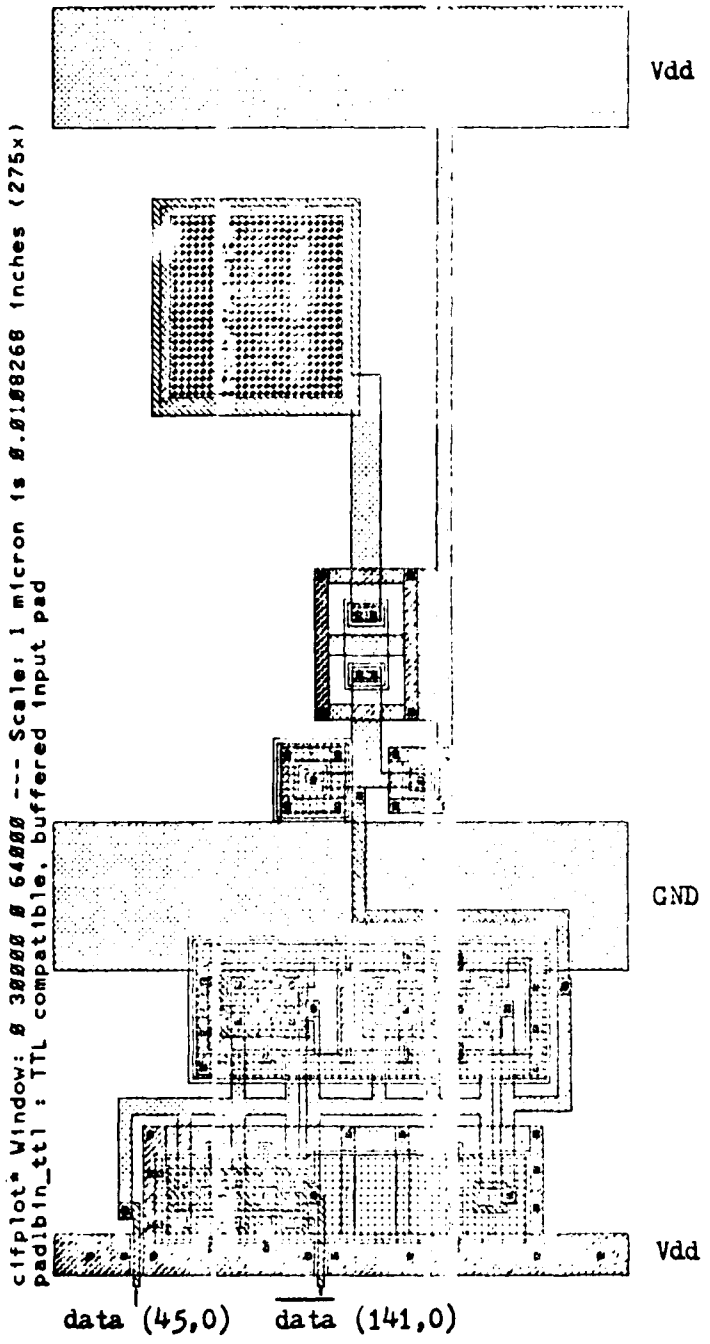
CIF ID 819

Figure E-4. padiin



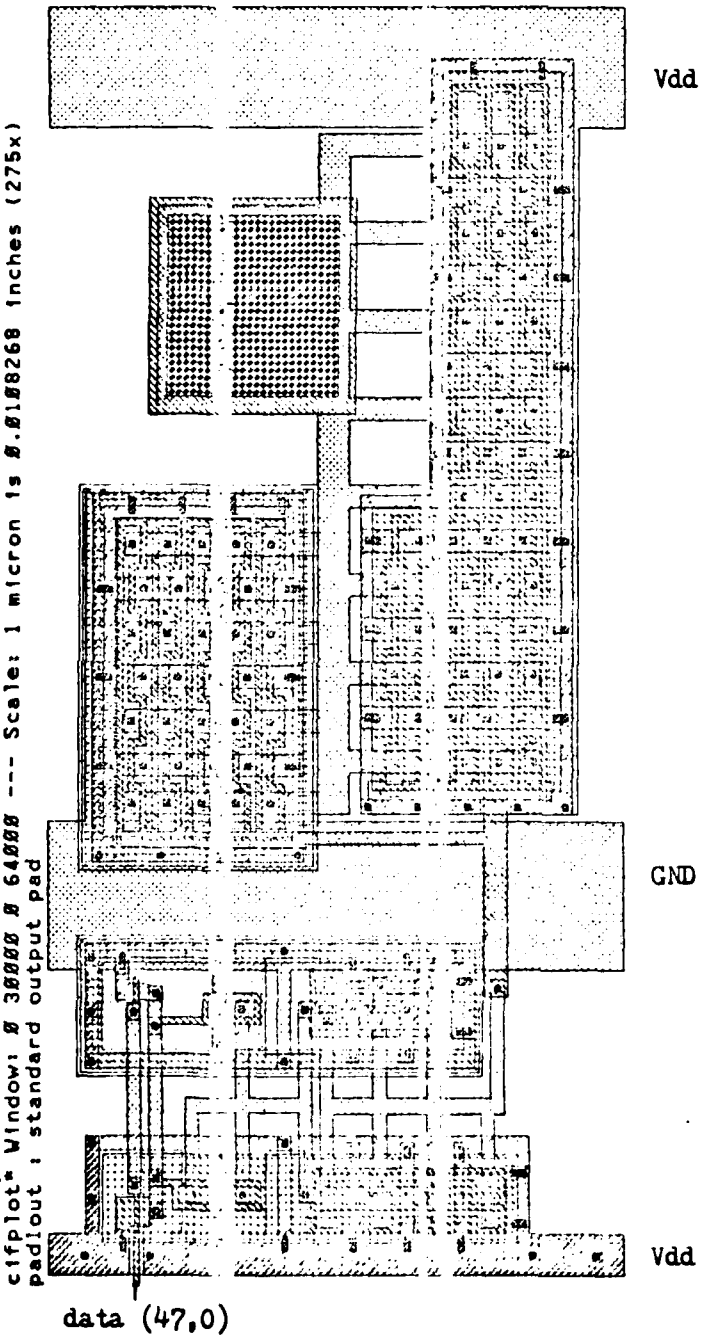
CIF ID 822

Figure E-5. padibin



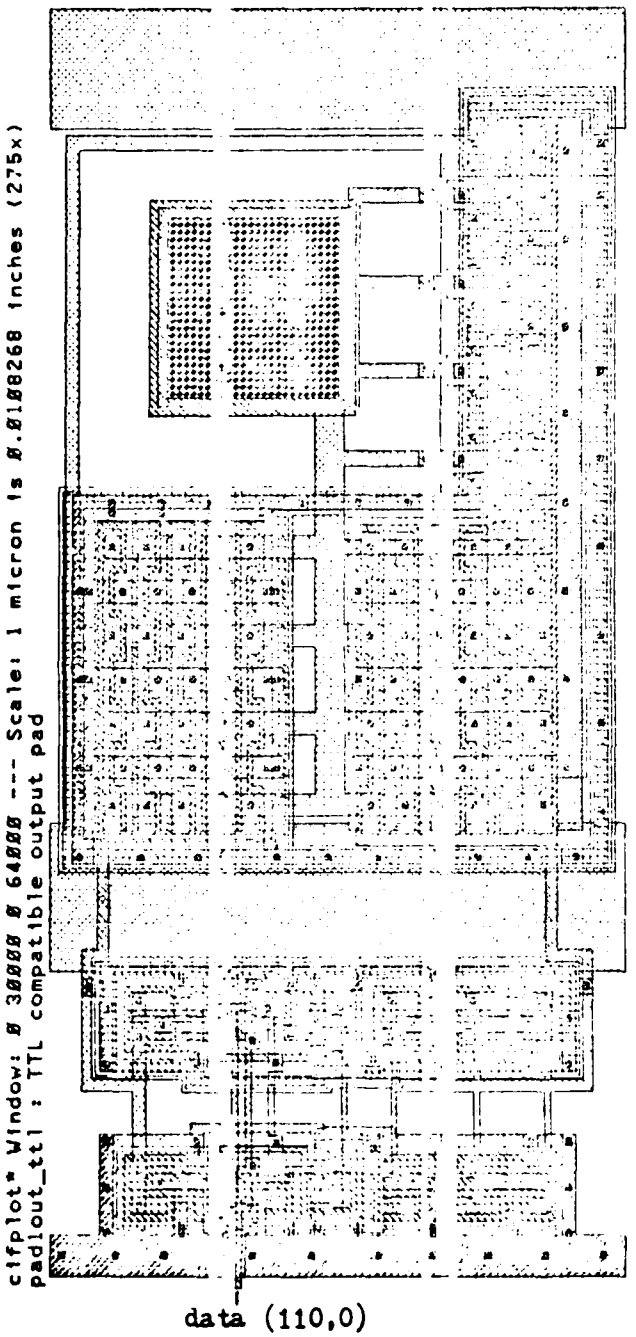
CIF ID 829

Figure E-6. padibin_ttl



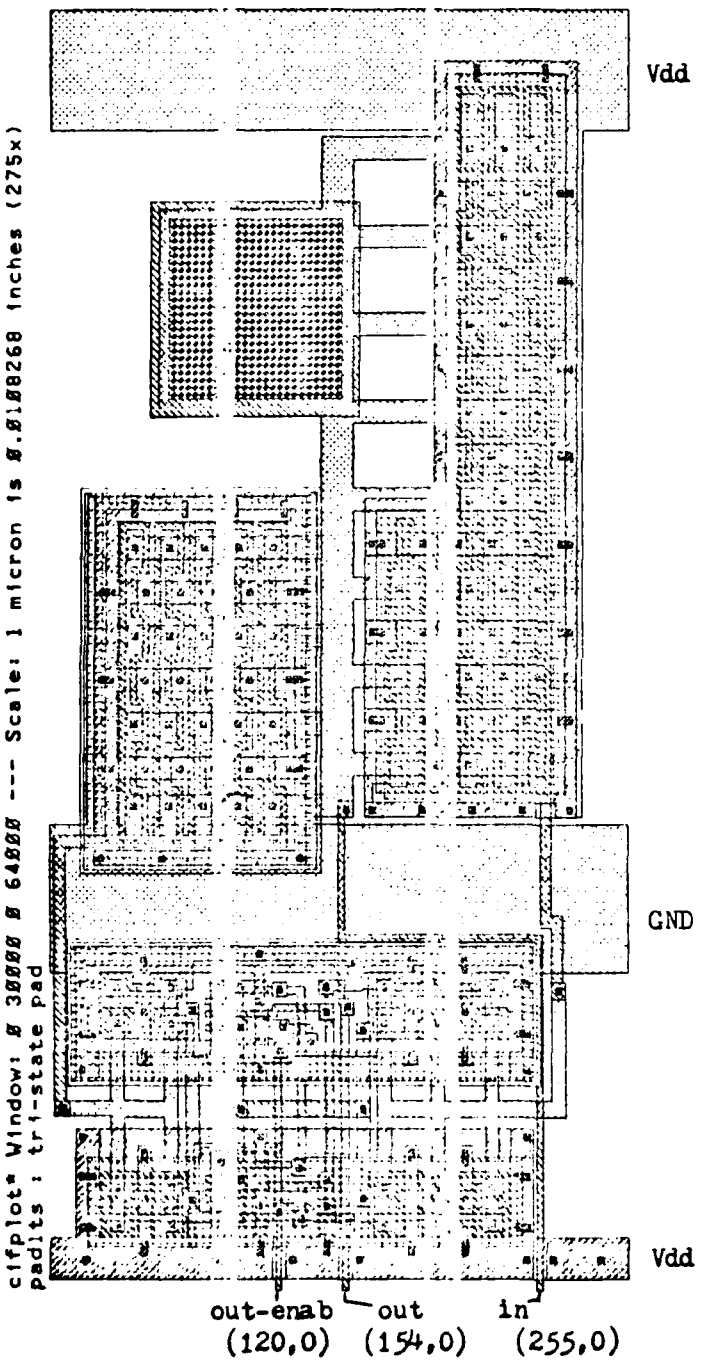
CIF ID 818

Figure E-7. padlout



CIF ID 836

Figure E-8. padlout_ttl



CIF ID 825

- out-enab low, pad is input and signal appears at "in"
- out-enab high, pad is output and signal appears at pin and at "in"

Figure E-9. padits

Appendix F. CMOS/BULK Cell Library

Presented is a listing of the file "c_ext.cll" which shows the available cells in the CMOS/BULK library "libc.lib". To use the library, the designer must include the following line in the ".cll" file:

```
#include "/usr/local/cad/lib/bane/c_ext.cll"
```

To invoke the library, the -l option must be used in the BANE command line as follows:

```
bane -v cmos -l c . . .
```

```
#ifndef STANDARD_LIBRARY_DEFINED
#define STANDARD_LIBRARY_DEFINED
external Shortguard (cif 812 bounds 0,0 40,20)
external padlout (cif 818 bounds 0,0 300,640)
external padlin (cif 819 bounds 0,0 300,640)
external padlbin (cif 822 bounds 0,0 300,640)
external padlvdd (cif 823 bounds 0,0 300,640)
external padlgnd (cif 824 bounds 0,0 300,640)
external padlts (cif 825 bounds 0,0 300,640)
external Longguard (cif 826 bounds 0,0 300,640)
external padlspace (cif 827 bounds 0,0 300,640)
external padlbin_ttl (cif 829 bounds 0,0 300,640)
external padlout_ttl (cif 836 bounds 0,0 300,640)
external pad2in (cif 843 bounds 0,0 200,430)
external pad2bin (cif 843 bounds 0,0 200,430)
external pad2gnd (cif 848 bounds 0,0 200,430)
external pad2vdd (cif 849 bounds 0,0 200,430)
external pad2space (cif 850 bounds 0,0 200,430)
external pad3vdd (cif 838 bounds 0,0 200,306)
external pad3in (cif 839 bounds 0,0 200,306)
external pad3gnd (cif 840 bounds 0,0 200,306)
external pad3space (cif 841 bounds 0,0 200,306)
external padlexample (cif 837 bounds 0,0 2400,640)
external pad2example (cif 851 bounds 0,0 1800,430)
external pad3example (cif 842 bounds 0,0 600,306)
external pf_28p46x34 (cif 865 bounds 0,0 4600,3400)
external pf_40p46x68 (cif 854 bounds 0,0 4600,6800)
external pf_40p69x68 (cif 857 bounds 0,0 6900,6800)
external pf_64p69x68 (cif 858 bounds 0,0 6900,6800)
external pf_64p79x92 (cif 862 bounds 0,0 7900,9200)
external pf_84p79x92 (cif 867 bounds 0,0 7900,9200)
external TX_GATE (cif 20 bounds 0,0 38,30)
external INV (cif 21 bounds 0,0 36,25)
external NAND2 (cif 22 bounds 0,0 44,28)
external NAND3 (cif 23 bounds 0,0 44,45)
external NAND4 (cif 24 bounds 0,0 44,65)
external DBUF (cif 25 bounds 0,0 94,90)
external NOR2 (cif 26 bounds 0,0 43,37)
#endif
```

Figure F-1. Listing of "c_ext.cll", available cells in CMOS/BULK library "libc.lib"

Appendix G. CLL Plot of CMOS/BULK ALU

Presented are the CLL plots for the ALU. The entire ALU is shown in Figure G-1, and the four quarters of it are shown in Figures G-2 through G-5. The quarters permit closer inspection of the ALU.

The definition of terms are as follows:

A0 - A3	Operand A
B0 - B3	Operand B
S0 - S3	Function selection, see Table IV-1
SEL	When "high" selects logic functions, when "low" selects arithmetic functions
F0 - F1	4-bit output
P & G	Carry look-ahead outputs for successive stages
CI	Carry in bit
CO	Carry out bit

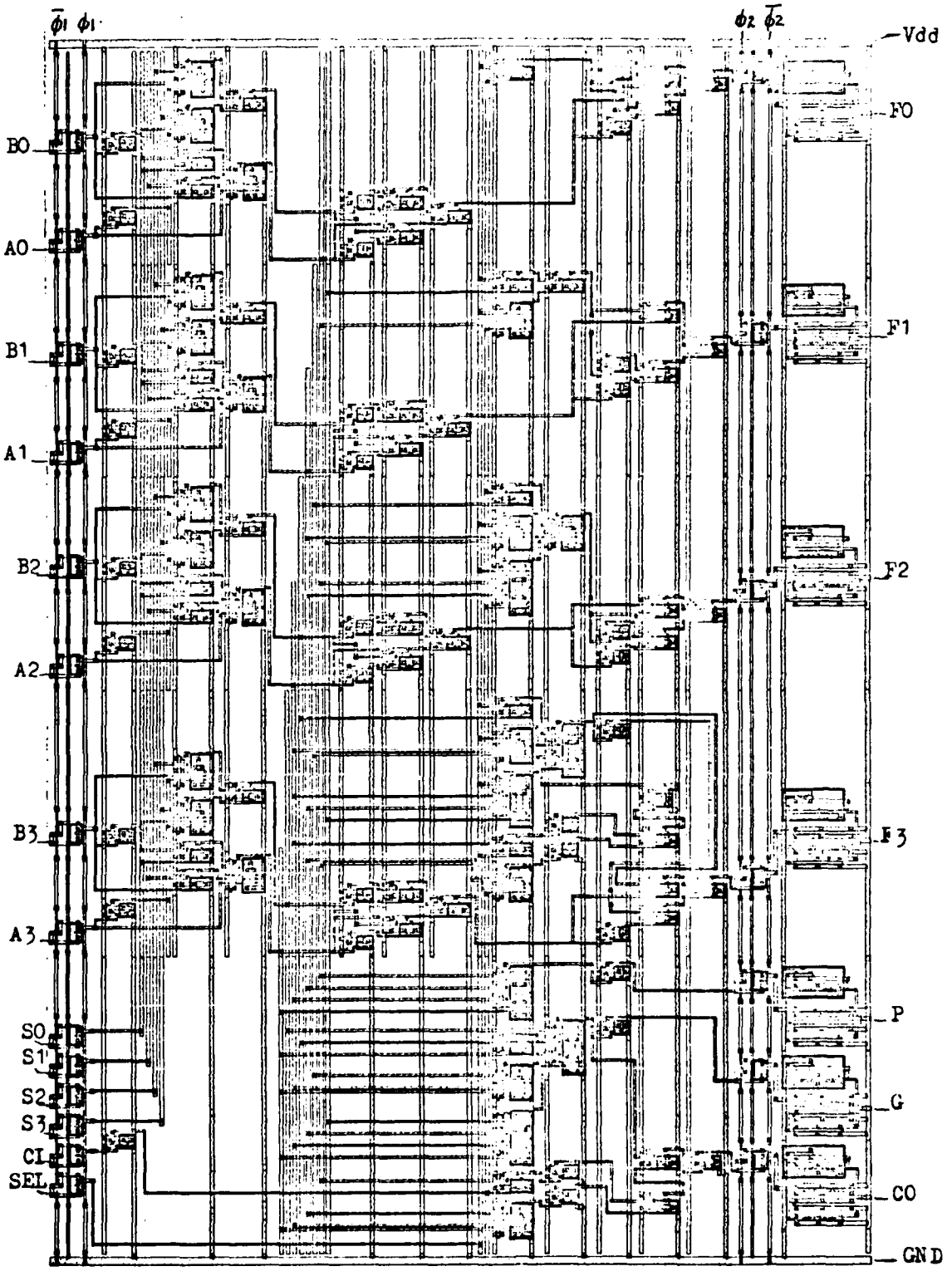


Figure G-1. CMOS/BULK ALU

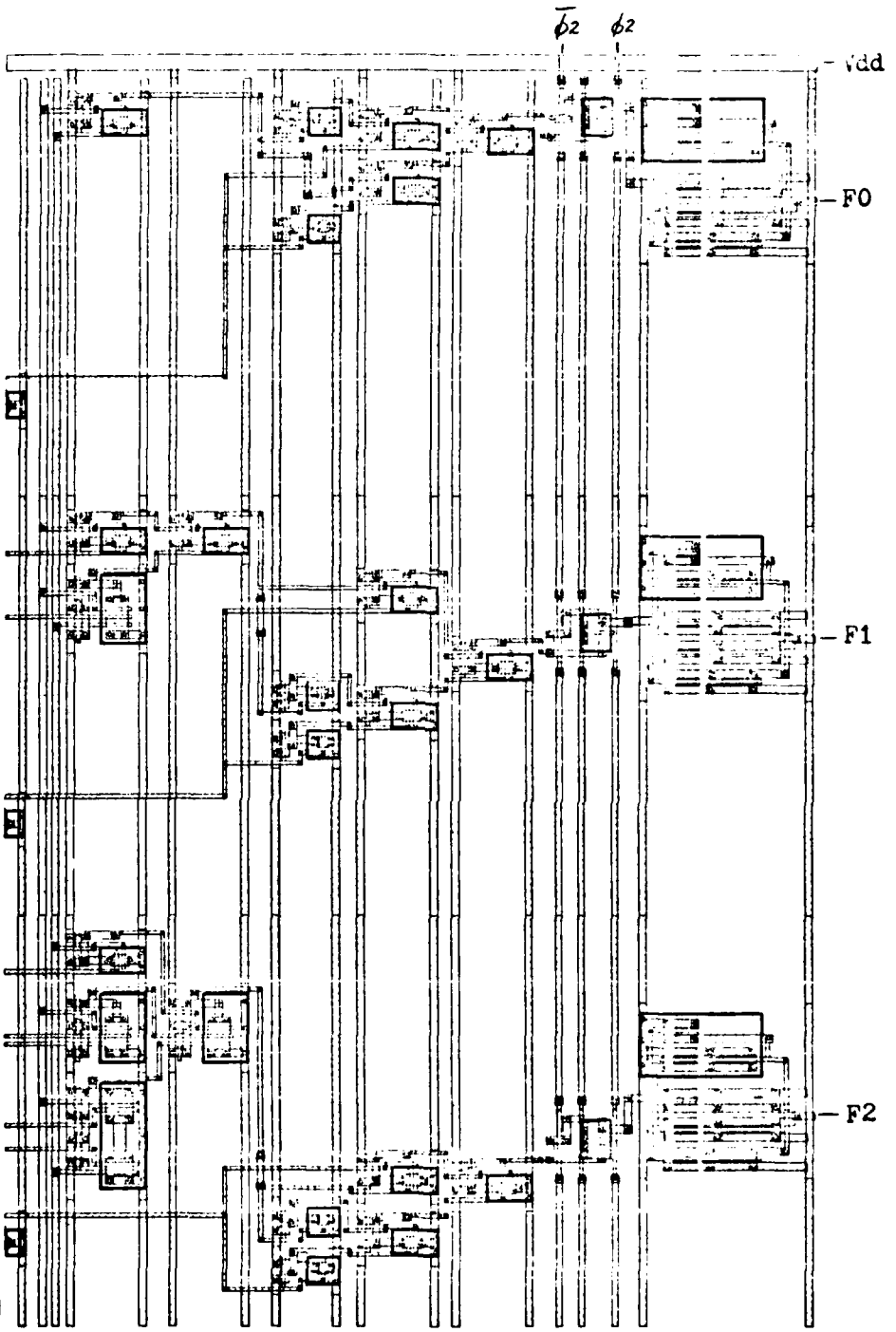


Figure G-2. Upper right corner of ALU

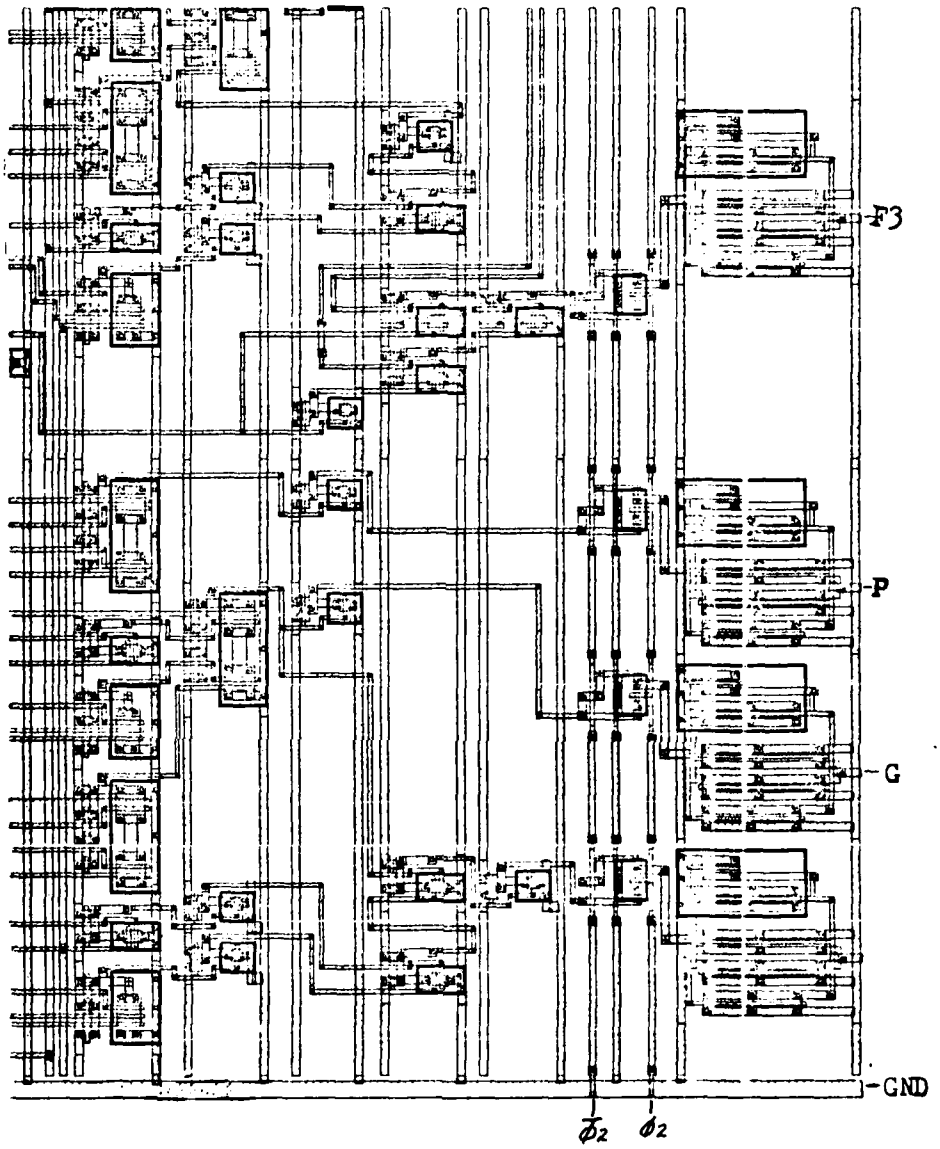


Figure G-3. Lower right corner of ALU

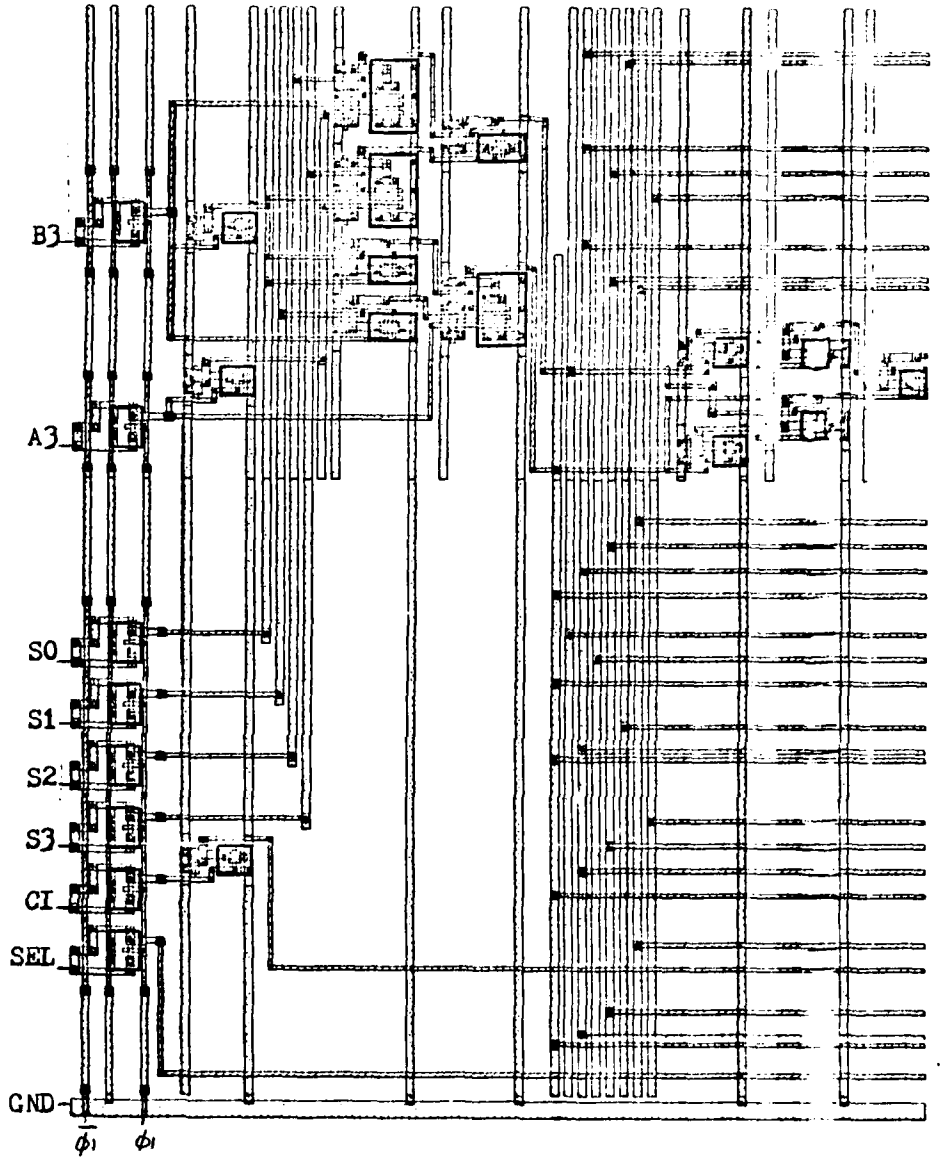


Figure G-4. Lower left corner of ALU

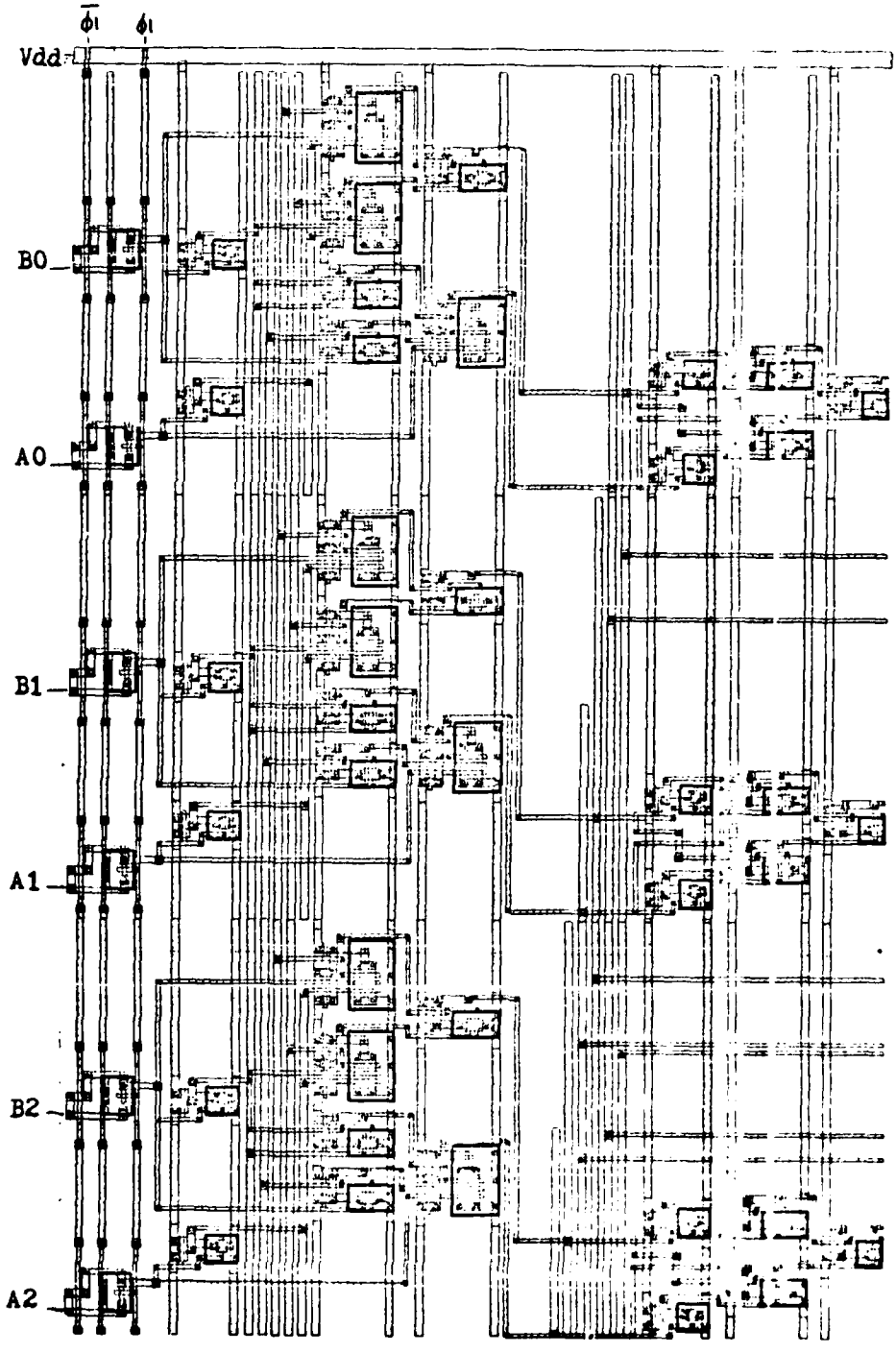


Figure G-5. Upper left corner of ALU

Glossary

ALU	Arithmetic Logic Unit. Combinational circuitry that performs arithmetic and logic operations on two binary numbers.
BANE	A computer-aided-design tool used to layout and plot NMOS or CMOS integrated circuits using CLL, Chip Layout Language. It also generates files that can be used in other computer-aided-design tools such as CIFPLOT and MEXTRA.
CIFPLOT	A computer-aided-design tool used to layout and plot integrated circuits using CIF, Cal-Tech Intermediate Format. CIF is more complex to use than CLL, although final fabrication files are sent in CIF.
CLL	A computer-aided-design tool used to layout and plot NMOS integrated circuits using CLL, Chip Layout Language. It also generates files that can be used in other computer-aided-design tools such as CIFPLOT and MEXTRA. BANE is a new version of CLL.
CMOS	Complementary-Metal-Oxide-Semiconductor. A transistor technology that uses an n-channel field effect transistor (NMOS) and a p-channel field effect transistor (PMOS) in a complementary switching action. CMOS can be used for digital or analog applications.
DRC	A computer-aided-design tool used to verify the layout of an integrated circuit by comparing the actual layout to a set of design rules.
ESIM	An event-level simulator used to verify the switching of an NMOS digital integrated circuit. It requires the simulation file supplied by MEXTRA.

HiCMOS	A subgroup of the CMOS family that uses a twin-well fabrication process with a double layer of polysilicon. It increases the speed and density of conventional CMOS.
MEXTRA	A computer-aided-design tool that extracts information about the nodes, transistors, and capacitors of an NMOS or CMOS (p-well only) integrated circuit. The extraction creates a simulation file suitable for ESIM (for NMOS) and SIMFILTER/PRESIM/RNL (for CMOS p-well).
NETLIST	A computer-aided-design tool that takes a network description of the entire integrated circuit, supplied by the designer, and performs an extraction on it. It creates a simulation file suitable for PRESIM/RNL.
NMOS	N-channel Metal-Oxide-Semiconductor. A field effect transistor that uses n-type doped silicon to form the conducting channel between the source and drain.
PMOS	P-channel Metal-Oxide-Semiconductor. A field effect transistor that uses p-type doped silicon to form the conducting channel between the source and drain.
PRESIM	A computer-aided design tool that converts the simulation file supplied by NETLIST into a binary file suitable for use in RNL.
RNL	An event level simulator that requires the binary output file of PRESIM to do the simulation of the integrated circuit. RNL supports NMOS and CMOS.
SIMFILTER	A computer-aided-design tool that converts a Berkeley formatted simulation file into an M.I.T. formatted simulation file and vice versa.

SOS	A subgroup of the CMOS family that uses silicon on a sapphire substrate (Silicon On Sapphire). The transistors are formed on islands of silicon grown on a sapphire substrate. This particular subgroup is not susceptible to latch-up.
VHSIC	Very-High-Speed-Integrated-Circuits. This is a DoD sponsored program designed to push the development of integrated circuits that can be dependably used in military, hostile, or space environments.
VLSI	Very-Large-Scale-Integrated (circuits). This is a term used to characterize integrated circuits that contain tens of thousands of transistors on a single substrate.

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REPORT DOCUMENTATION PAGE

1a. REPORT SECURITY CLASSIFICATION

UNCLASSIFIED

2a. SECURITY CLASSIFICATION AUTHORITY

2b. DECLASSIFICATION/DOWNGRADING SCHEDULE

3. DISTRIBUTION/AVAILABILITY OF REPORT

Approved for Public Release;
Distribution Unlimited

4. PERFORMING ORGANIZATION REPORT NUMBER(S)

AFIT/GE/ENG/84D-44

5. MONITORING ORGANIZATION REPORT NUMBER(S)

6a. NAME OF PERFORMING ORGANIZATION

School of Engineering

6b. OFFICE SYMBOL (If applicable)

AFIT/ENG

7a. NAME OF MONITORING ORGANIZATION

6c. ADDRESS (City, State and ZIP Code)

Air Force Institute of Technology
Wright-Patterson Air Force Base, OH 45433

7b. ADDRESS (City, State and ZIP Code)

8a. NAME OF FUNDING/SPONSORING ORGANIZATION

8b. OFFICE SYMBOL (If applicable)

9. PROCUREMENT INSTRUMENT IDENTIFICATION NUMBER

8c. ADDRESS (City, State and ZIP Code)

10. SOURCE OF FUNDING NOS.

PROGRAM ELEMENT NO.	PROJECT NO.	TASK NO.	WORK UNIT NO.

11. TITLE (Include Security Classification)

See Box 19

12. PERSONAL AUTHOR(S)

Michael F. [illegible], B.S., 2d Lt, USAF

13a. TYPE OF REPORT

MS Thesis

15. PAGE COUNT

146

16. SUPPLEMENTARY NOTATION

17. COSATI CODES

18. SUBJECT TERMS

[illegible] COMPUTER [illegible] PROGRAMS,
[illegible] SEMICONDUCTORS.

19. ABSTRACT

TITLE: ANALYSIS OF THE CAPABILITY TO [illegible] COMPLEX [illegible] FIELD EFFECT SEMICONDUCTOR [illegible] Circuits

THESIS ADVISOR: William C. Sutton, Major, USAF

[illegible] AFR 190-17
LYNN E. WOLAVER
Dean for Research and Professional Development
Air Force Institute of Technology (ATC)
Wright-Patterson AFB OH 45433

20. DISTRIBUTION/AVAILABILITY OF ABSTRACT

UNCLASSIFIED/UNLIMITED

21. ABSTRACT SECURITY CLASSIFICATION

22a. NAME OF RESPONSIBLE INDIVIDUAL

William C. Sutton, Major, USAF

22b. TELEPHONE NUMBER

22c. OFFICE SYMBOL

DD FORM 1473, 83 APR

A complete [illegible] design cycle has been established and tested to evaluate the effectiveness of [illegible] design tools for the layout, verification, and [illegible] integrated circuits. This design cycle is used for p-well, n-well, or twin-well structures, although current fabrication facilities limit this to p-well only. PIKE, an interactive layout program from Stanford, is at the center of this design cycle and has been shown to be simple to use in the layout of CMOS integrated circuits (it can also be used to layout NMOS integrated circuits).

A "[illegible]" was developed for using the design cycle from initial layout, through design verification, and to circuit simulation using NETLIST, PRESIM, and ESIM from the University of California. A CMOS cell library was designed and [illegible] that were designed and completely tested by [illegible]. Also, a [illegible] arithmetic logic unit as a [illegible] test of the [illegible] design cycle.

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