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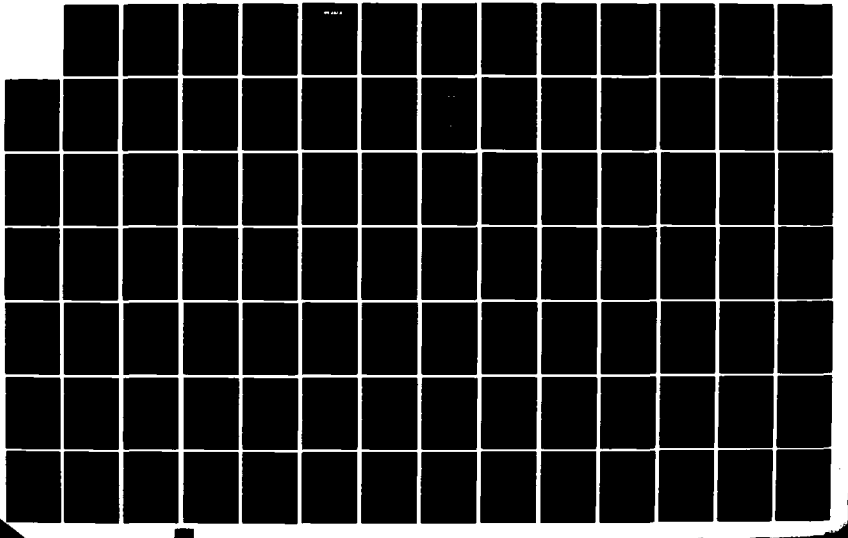

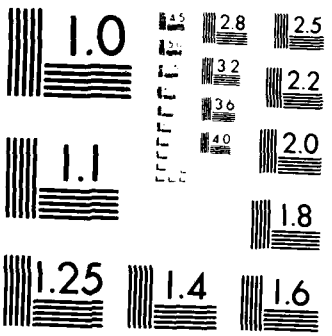

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HYBRID INTEGRATED COMPUTER AIDED DESIGN AND MANUFACTURING

HUGHES AIRCRAFT COMPANY
TUCSON MANUFACTURING DIVISION

Prepared for:
U.S. ARMY MISSILE COMMAND
System Engineering Directorate
ATTN: DRSMI - RHS/Bldg 5400
Redstone Arsenal, AL 35898

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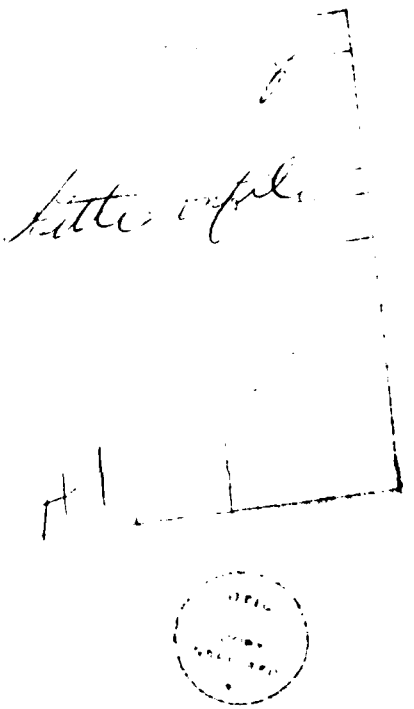
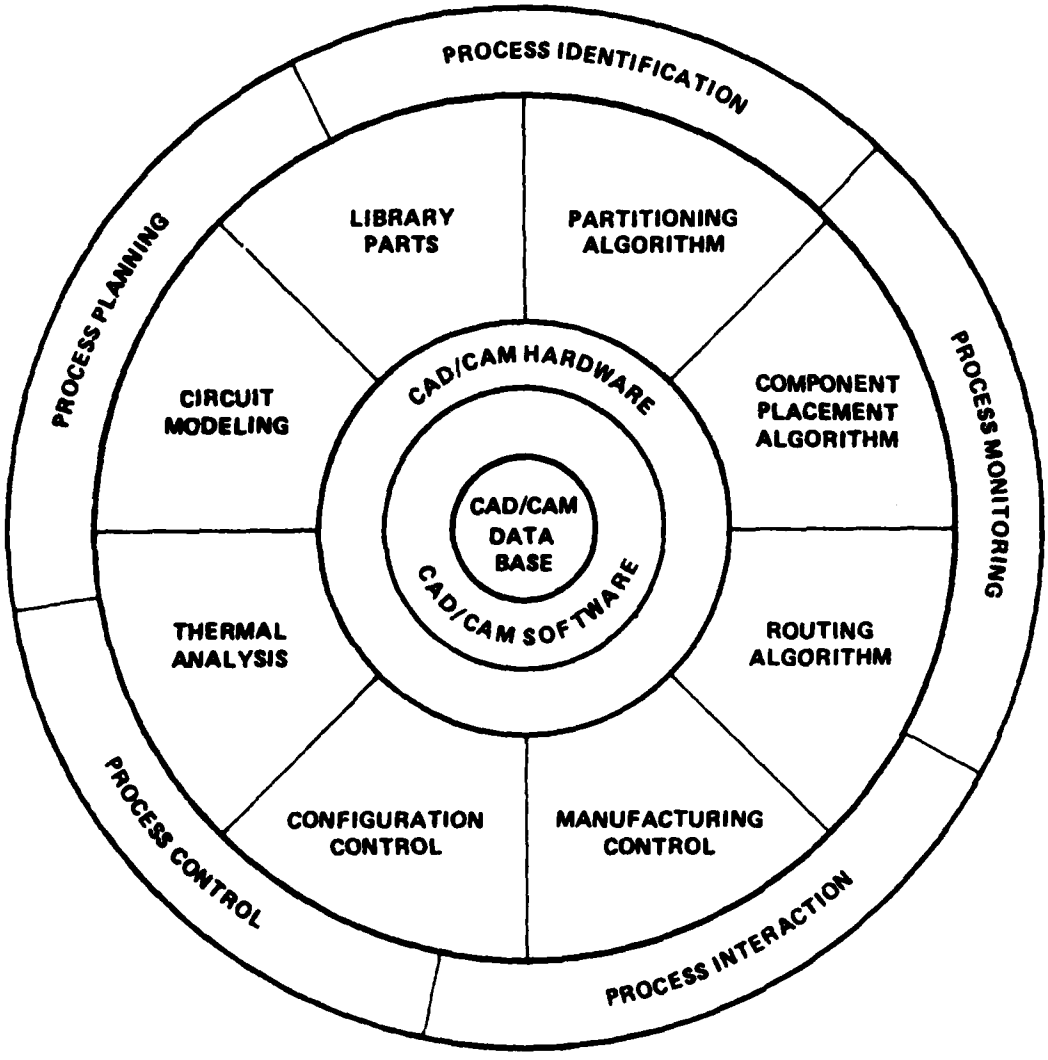


HICADAM

HYBRID INTEGRATED COMPUTER AIDED DESIGN AND MANUFACTURING



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- ABSTRACT -

An overview of the design and manufacturing life cycle of a hybrid has been compiled. CAD/CAM interfaces are discussed. Database specifications and types are highlighted. Current and planned MAN TECH programs in the area of hybrid microelectronics technology are summarized. An industry survey has been conducted and analyzed to ascertain those areas where manufacturing technology advancements will have the maximal cost reduction. A HICADAM Systems architecture is proposed utilizing the ICAM modeling methodology of $IDEF_0$.

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- INTRODUCTION -

The design and manufacture of a hybrid microelectronics circuit requires the interfacing of diverse technologies on the leading edge of materials sciences, equipment advancements, and the advent of computer controlled manufacturing processes. Hybrids offer distinct advantages in weight, volume, performance, power, and reliability considerations. They are an efficient interconnect and packaging technology which is cost effective only when their inherent advantages outweigh their relative design and manufacturing costs.

An analysis of the design & manufacturing life cycle of a hybrid has revealed areas where manufacturing technology advancements will reduce the cost of hybrid microelectronics circuits. These advancements may flow from new materials, new processes, and from the introduction of computer integrated manufacturing. Current and planned manufacturing technology enhancement projects are discussed and related to a systems architecture. Projects are proposed for those identified areas where no scheduled projects occur.

Computer integrated manufacturing entails the interfacing of CAD, CAM, CAT, and MIS systems. This interfacing will ensure a closed loop system to design and manufacture hybrids. An architecture which shows these interfaces has been developed.

- HYBRID DESIGN PROCESS -

The design process of a hybrid circuit is influenced by many factors. These include the origin of the design stimulus, the extent of the design effort to be undertaken, and the technological constraints. Design evolution, from its conceptualization through its finalization, is a continual tradeoff between these various factors.

The market niche which a firm seeks determines the extent of its design effort. A firm which designs and produces custom hybrids may delve into specific component fabrication. Other firms may use off-the-shelf components exclusively because hybrids are one item in an end product. Military applications generally tend more toward the specialty component markets.

Technological constraints flow from material areas and manufacturing processes. Material constraints include cost, reliability, and physical characteristics. The physical characteristics of certain materials (such as beryllia use in substrates) may dictate extreme environmental controls. The constraints from manufacturing processes include repeatability and mechanical considerations (such as the precise positioning of a large XY table).

The design process of a hybrid is more art than science. The process is very iterative and each subset of activities are strongly interrelated. The three general functions which occur during design are:

- technology selection
- detailed design
- detailed documentation

Technology Selection

Technology selection begins the design process for a hybrid. The designing entity must balance competing forces so that a cost effective hybrid design with the necessary performance characteristics may be realized. A list of factors to be considered includes:

- requirements (performance,reliability,specifications)
- capabilities (equipment,facilities,labor force)
- producibility (component density,yield/design margins)
- material (lead times,number of sources)
- costs (material,equipment,burdened labor,pricing factors)

The interplay of these decision factors will result in the establishment of boundaries to the conceptualization process.

Hybrid conceptualization may be instituted as a result of a stimulus to create a new product or to modify an existing product. This process can be described as a mixture of direct synthesis, approximate synthesis, and intuitive innovation.

Direct synthesis is the process of using a historical design as a basis for the new design. This is an evolutionary development of a hybrid design.

Approximate synthesis is the process of using two or more historical designs as the basis for the new design. This is a combinatorial evolution of existing designs.

Intuitive innovation is the art and science of developing a completely new circuit design. This is usually the result of a new breakthrough in materials sciences but may result from the advancement of manufacturing technologies.

Detailed Design

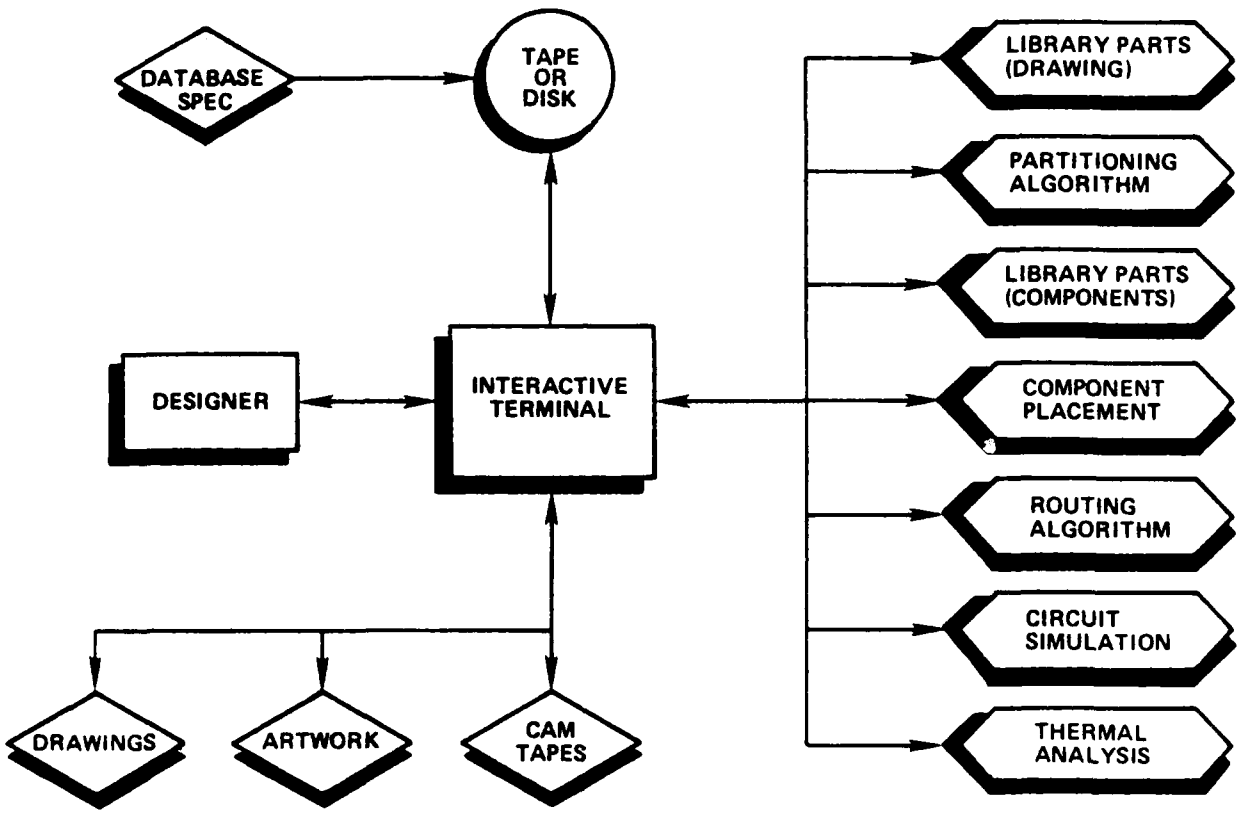
The detailed design process flows from the technology selection decisions. The product is defined logically, electrically, and then physically. This phase of the design process is the most interrelated. Throughout the design steps a designer can use a CAD/CAM system to aid in relating such factors as physical limitations, circuit testability, circuit producibility, and circuit performance specifications. A CAD/CAM system is illustrated in figure 1.

Logical design integrates the conceptual signal flow with the interface requirements generated from circuit partitioning. The logic diagrams can be generated in two fashions. The first features the interaction of a designer and a CAD library of logic symbols. The second uses Boolean Algebra circuit descriptions with a computer to generate the logic diagram. As circuit complexities increase the second procedure becomes more important.

The next step in the design process is the generation of a detailed electrical schematic. The effort involved here is dependent on the detail of the logic diagram. In the best case, the designer needs only to specify part numbers, to add in power/ground requirements, to add signal conditioning circuitry, and to develop a parts list. In the case of a high level block diagram, the designer must develop detailed logic statements to describe each block. These, in turn, will be used in creating the complex schematic. In complex circuits design verification can often only occur through the building of a prototype circuit. In the case of a circuit which uses very large scale integrated devices a macroscopic circuit simulation may be the only viable verification tool.

FIGURE 1.

CAD/CAM SYSTEM ATTRIBUTES



The output of the electrical design consists of documentation, test program information, physical design data, and data for computerized circuit analyses. At this time a schematic may be generated from the CAD database as part of the deliverable documentation. Routing and component placement data is extracted from the CAD system, or manually compiled, and utilized in the physical design process. Crucial test information to be considered includes signal levels, signal types, and the identification of critical test nodes. An illustrative test program generation flow is given in figure 2.

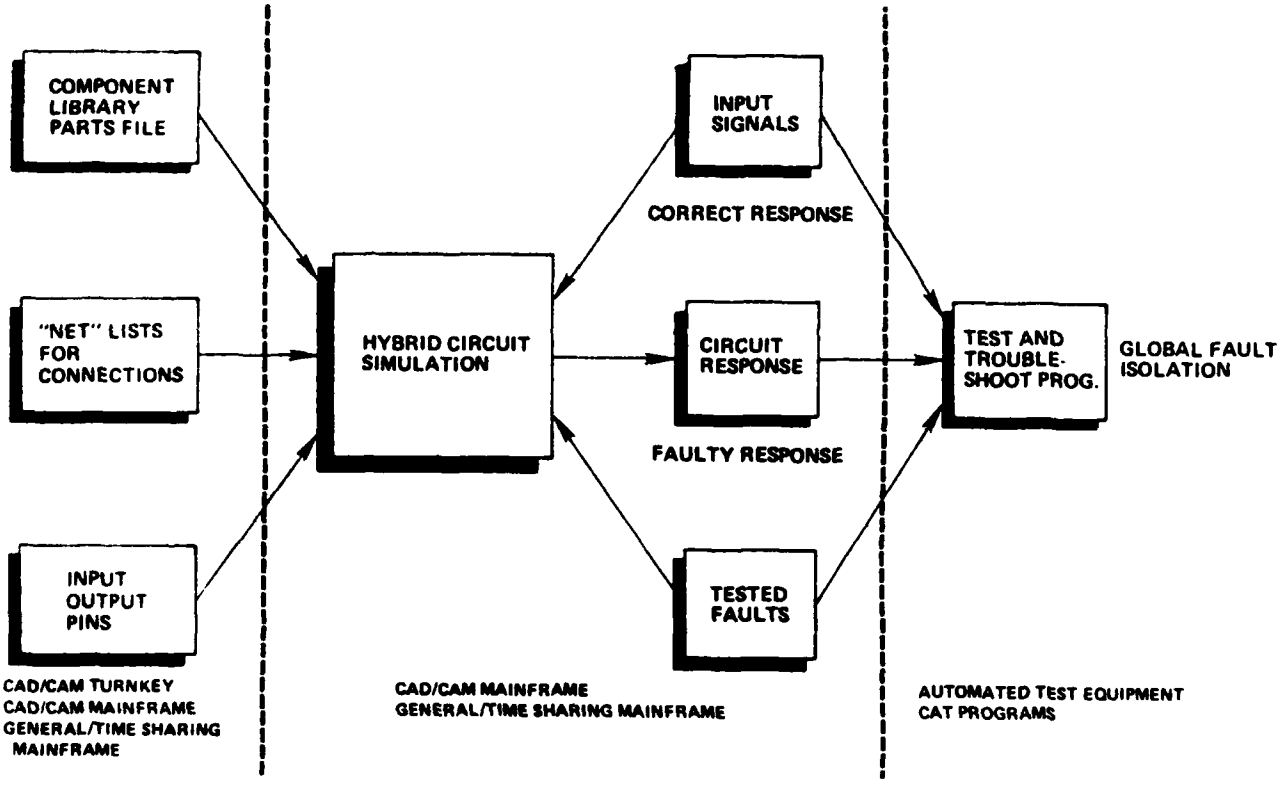
A detailed discussion of circuit design and analysis programs is beyond the scope of this report. The following brief discussion on possible program attributes is included only to add a degree of robustness to the analysis of hybrid microelectronic circuit design.

Circuit design and analysis programs are varied both in their applications and in their complexity. Statistical analyses, such as for component tolerances , may be useful (an example is ASTAP). They may be used to perform AC, DC, and transient analyses (as does ASTAP as well as SPICE2). Design verification and fault simulation for digital circuits is becoming more important as the complexities of circuits increases. TEGAS provides useful tools in these respects. Specialty programs (such as COMPACT for microwave circuits) may be useful in optimizing specific types of circuits. The future for circuit design and analysis programs lies in providing a mixed bag of tools to aid the designer as opposed to the generation of one all-encompassing analysis program.

The hybrid circuit can now be defined on a physical basis. The preliminary bill of materials, the preplacement criteria, and the physical

FIGURE 2.

ILLUSTRATIVE TEST PROGRAM GENERATION



size limitations are now intermeshed. This information is supplied to the designer in the form of extracted databases from previously generated CAD databases or from manual compilation efforts. The physical design phase may use a CAD system to determine two types of information. First, placement information is generated consisting of the locations of the various component parts that make up the circuit. Second, based upon this placement of components upon the substrate, the pin-to-pin connections (using the netlist generated by the logic and electrical schematics) for each component are made.

Placement algorithms are complex and often designed to perform most efficiently with a particular routing algorithm. Constraints that placement algorithms must face are diverse and complex. Placement must not only consider which components are to be interconnected but also which components are to be connected to external connectors. They must account for component orientation (to aid the automation of pick and place equipment) , the ultimate circuit configuration, and circuit densities so as to guard against plating difficulties.

Routing the hybrid requires four different types of inputs. The first inputs are the geometrical boundaries of the substrate. These are bounds beyond which no routed signals may exist. The second inputs are general constraints under which the router will be forced to operate. Typical of these constraints are conductor widths and spacings, the number of layers, via sizes, and maximum flywire lengths. The third set of inputs are extracted from the electrical schematic and are the netlists. This is the pin to pin connection list and specifies which pin of each device is to connected to which pin of any other device or an outside connector.

The fourth type of data is perhaps the most difficult to obtain, particularly for hybrids. This is the physical description of the individual component parts that make up any given hybrid. It includes the exact geometrical location of pins within that part and the component outline. These data vary depending on whether the hybrid is to be chip and wire, TAB/BTAB, chip carrier, or some combination of these techniques. In addition, certain components might be designed with the routed circuitry itself. When this is done the router must be sophisticated enough to automatically incorporate these components into the circuitry or, as is more often the case, the designer must design these devices before the routing process and treat them as component parts. The routing complexity increases dramatically when chip and wire techniques are used and the router must consider the possibility of differing topographies for the various components.

Current component placement and routing algorithms in use for hybrid circuits are modified printed wiring board or VLSIC routing algorithms. The lack of widespread success of these routing algorithms results from important circuit differences which include line spacing, vias which do not pass through the entire substrate, component topography, and external connection requirements.

After placement of components, routing of interconnects, and final gate assignments, sufficient information is available for further circuit analysis. Verification of thermal characteristics, fan out/in power requirements, stray capacitance, testability, and general design rules can be verified. The results of this analysis may dictate changes in the electrical schematic, physical layout, or the design algorithms.

Detailed Product Documentation

The last phase of the design process is to detail the product documentation. The test programs, circuit schematics, drawings, artwork masters, and other design documentation are collated and verified. The compilation of the test program is the main task of this phase.

The generation of a precise test program is accomplished to satisfy specific program requirements. Data on circuit response to an input stimulus is tabulated. The input nodes for the test signals are generated such that the confidence interval selected for the test is achieved (minimal alpha and beta errors for a selected confidence interval).

For analog hybrids testing is accomplished by simulating the actual useage in an end-product application. A computer generates the input and monitors the resultant output. While analog hybrid troubleshooting is currently an art, work is being conducted on a guided probe approach for analog troubleshooting.

Digital hybrids may be tested the same way as analog hybrids but testing is more commonly done on a fault simulation basis. In very complex digital hybrids testing is usually done on a global basis. Specific path sensitization, fault libraries, and guided probes are aids to the troubleshooting of digital hybrids.

There is a continual management review process during the design of a hybrid. Included in this process are program progress, cost tracking, and documentation reviews. The design engineering database will undergo a final review as a complete package prior to being released to the manufacturing engineering functions.

- HYBRID MANUFACTURING PROCESS -

The manufacture of hybrid microelectronics has two main generic activities which are substrate fabrication and hybrid assembly. Substrates are typically fabricated through a thin film or a thick film process. The cofiring of ceramics, the use of mid-film technologies, and the use of exotic materials are alternatives to thin and thick film processes. Hybrid assembly consists of the mounting, interconnecting, and packaging of active and passive devices on these substrates. For military applications MIL-STD-833b is used to specify quality and test constraints.

Thin Film Processes

Thin film substrate fabrication has two main functional activities. These are photolithography and circuit delineation. Photolithography defines the desired circuit pattern. Circuit delineation creates the actual film layers. (Refer to figure 3 & figure 4)

Photolithography is the task of applying and developing the resist coating to form the circuit pattern. The resist is applied (via spinning and baking, or lamination) and then exposed. The master artwork (created from a pattern on rubylith) is used to expose a specific pattern upon the resist. The resist is developed and washed leaving only the exposed resist pattern on the base substrate. The substrate with the exposed resist is then baked to insure the integrity of the resist pattern.

Circuit delineation can now occur. This process occurs via an additive or a subtractive technigue. In an additive process, evaporated material is placed on the substrate by a vacuum deposition technigue. The exposed pattern (resist or mask) covers those areas where layering is not to occur. When the deposition process is completed the resist pattern is

FIGURE 3.

ILLUSTRATIVE THIN FILM PROCESS FLOW

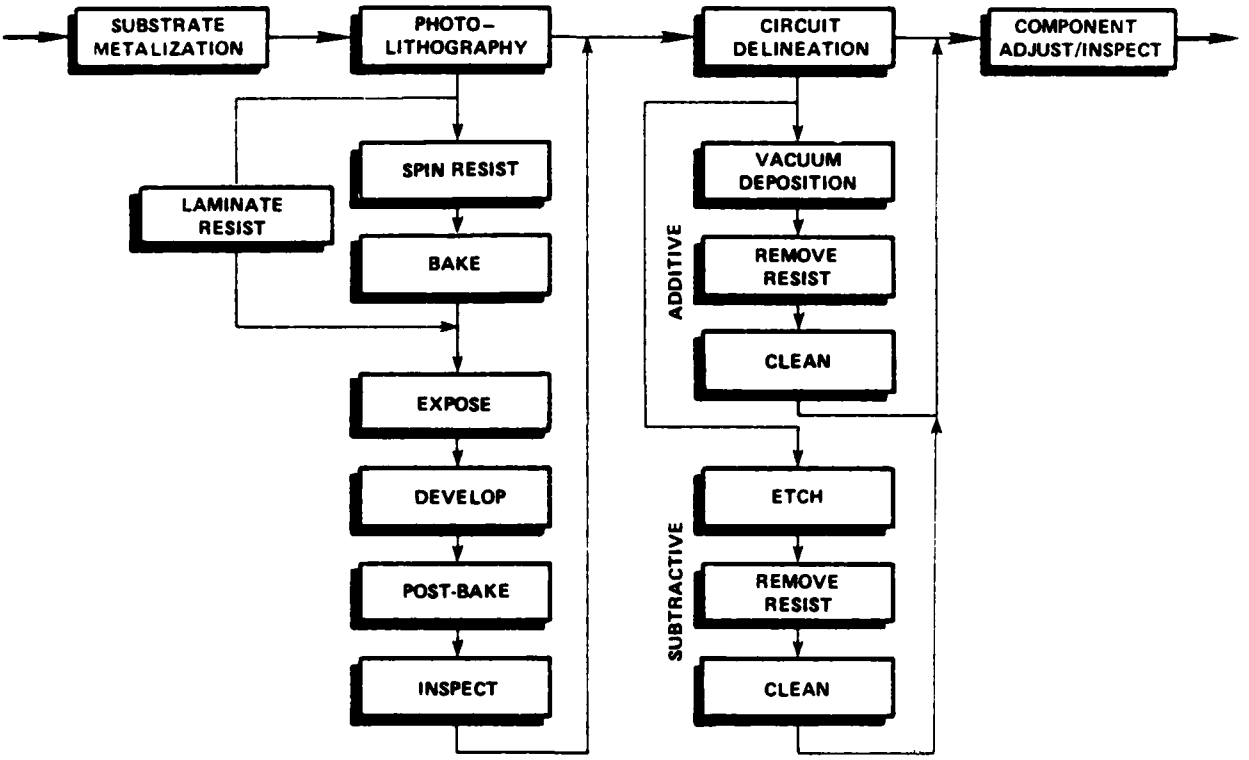
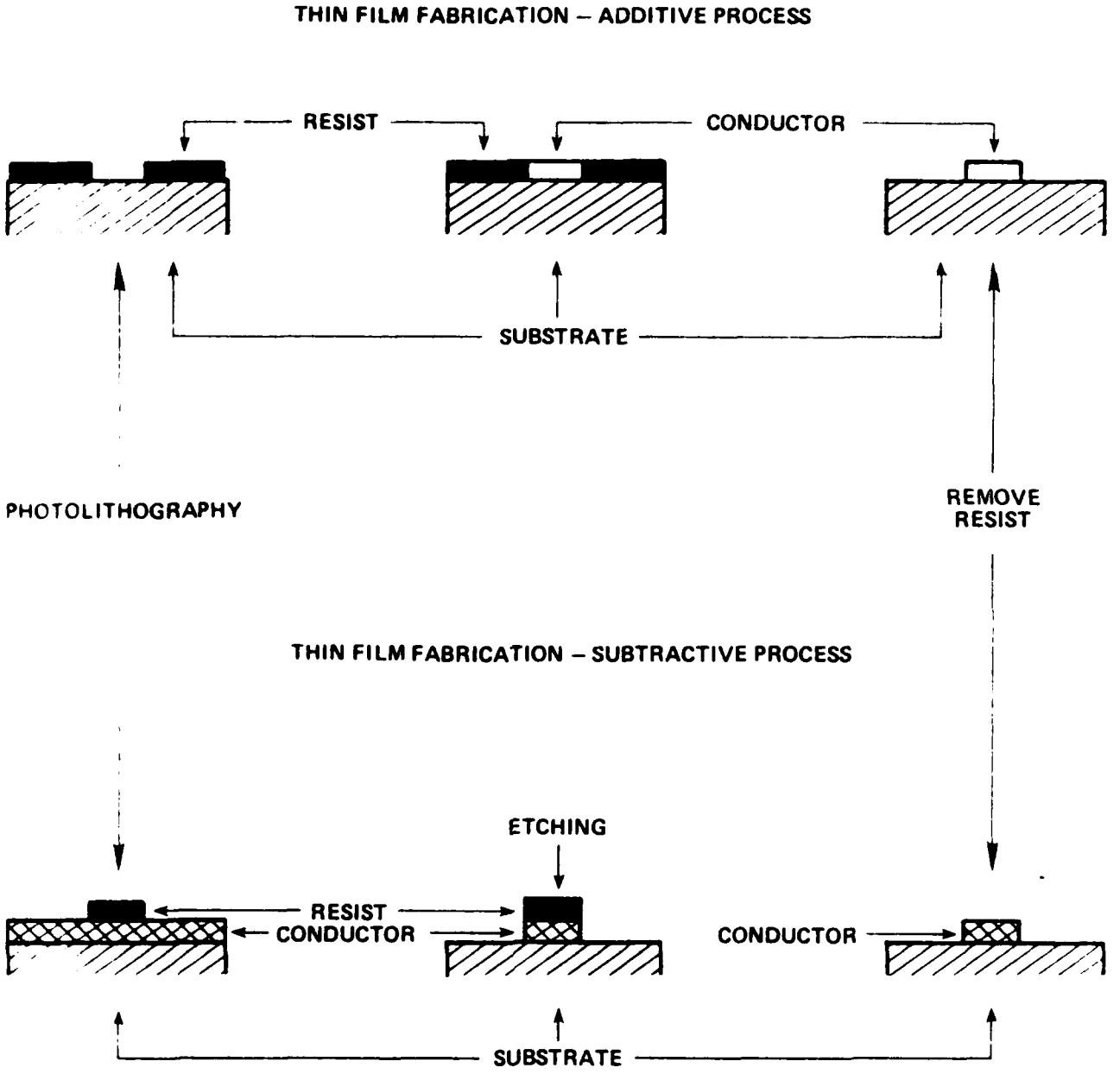


FIGURE 4.

THIN FILM FABRICATION



removed, the substrate is cleaned, and then it is inspected.

In a subtractive process the exposed resist pattern covers those areas which are to remain as part of the circuit. The substrate is placed in an etching solution. This causes the removal of the material on the uncovered surface area. When this process is complete the resist pattern is removed, the substrate is cleaned, and then it is inspected.

Numerous techniques are being used to provide the energy needed to cause the evaporation of the material to be deposited. These include electron beams, ion beams, lasers, heating techniques, and sputtering. The specific film characteristics sought by the user will determine the type of process selected.

Manufacturing constraints (environmental concerns, increased circuit densities, etc.) have fostered the advent of new manufacturing technologies. Examples are the dry etching techniques. Plasma etching (a reactive dry etching) offers reduced chemical hazards but has the problems of repeatability caused by uneven gas flow and thermal gradients. Ion beam milling (a non-reactive dry etching) has enhanced flexibility (angular milling, control of plasma potential,etc.) but suffers from a low etch rate and poor selectivity.

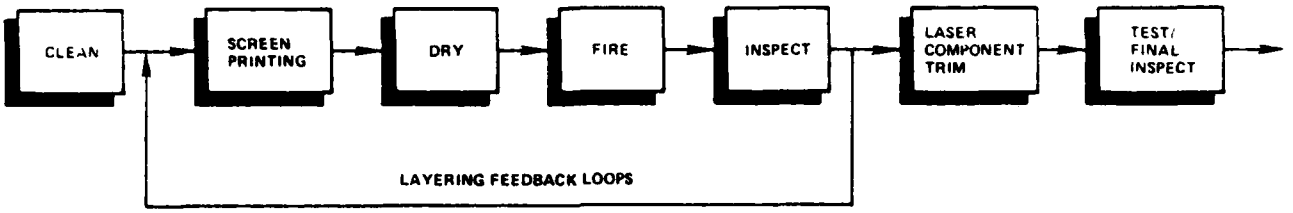
Thick Film Processes

Thick film technology involves the layering of a resistive, a conductive, or a dielectric paste (ink) using a screen printing process. (Refer to figure 5) The paste (ink) is a composition of minute poly-crystalline particles in a thixotropic carrier.

The screen printing process entails the application of a paste through a fine mesh stencil screen onto the substrate. The printed surface

FIGURE 5.

ILLUSTRATIVE THICK FILM PROCESS FLOW



is then dryed and fired. The conductor layers are inspected and may be tested prior to the continuation of the layering process. Multilayer substrates require the fabrication of vias to serve as interconnects between the conductor layers.

Thick film resistors undergo a trimming operation. This fine adjustment of the resistance values may be done using abrasives or a microprocessor controlled laser.

Substrate testing is generally limited to a continuity test of the conductor layers. Manual probes, a bed-of-nails test head, or a capacitance test may be used to verify continuity.

Numerous factors affect the success, or the failure, of the thick film screen printing process. These include paste rheology, stencil/screen mask fabrication, and the printing technique. To date the screen printing process has not been significantly automated.

Cofired Ceramics Process

The cofired ceramics technology may use a sandwiching of tungsten conductor layers between green ceramic sheets. The layers are fabricated, pressed together, and then fired. (Refer to figure 6)

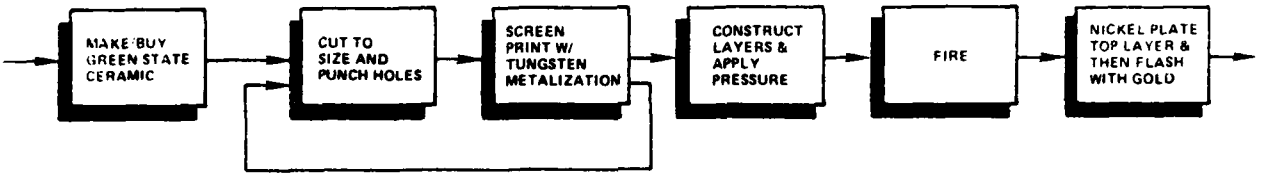
The main problem lies in the shrinkage and the non-repeatability of this shrinkage caused by the firing of the green ceramic. Shrinkages of 12 to 20% are not uncommon. With the advent of tighter spaced lines due to increasing circuit densities , this lack of ability to control the shrinkage prevents the widespread usage of cofired ceramic technology.

Alternate Materials and Technologies

Alternate materials and technologies exist. Porcelanized steel and organic materials can be used as a base for the substrate. A new

FIGURE 6.

ILLUSTRATIVE COFIRE CERAMICS PROCESS FLOW



mid-film technology can be used to deposit conductor material.

A general overview of the mid-film technique is as follows. Resist is applied to a substrate (by spraying or dipping), a conductor pattern is exposed, and the unexposed resist is washed off. The remaining pattern has a 'sticky' consistency. A conductive powder is applied to this pattern and the substrate is baked. During baking the resist pattern evacuates from the substrate leaving a hardened conductor layer bonded to the substrate.

Hybrid Assembly

Hybrid circuits may be assembled under a mixture of line flow and batch mode production operations. The processes described below are illustrative and not definitive.

For a chip and wire assembly the first operations occur in a die attach area. The substrate is cleaned, the die are attached, cured, and the substrate is then inspected for die positioning and integrity. Wire-bonding is used for the necessary interconnections. (Refer to figure 7)

The wirebond activities may include the bonding of 2.0 mil, 1.0 mil, and 0.7 mil flywires. The wires are bonded thermosonically (using heat and a 'sonic' scrubbing motion) or by thermocompression (using heat and pressure). A sample and/or a 100% non-destructive wirepull may then be conducted. (Refer to figure 8)

Alternatives to the chip and wire technology are to utilize tape automated bonding/bumped tape automated bonding or chip carrier techniques. (Refer to figure 9) The TAB/BTAB and chip carrier technologies have advantages and disadvantages. Each offers the ability to prescreen the devices prior to attachment to the substrate which will improve yields.

FIGURE 7.

ILLUSTRATIVE CHIP ATTACHMENT

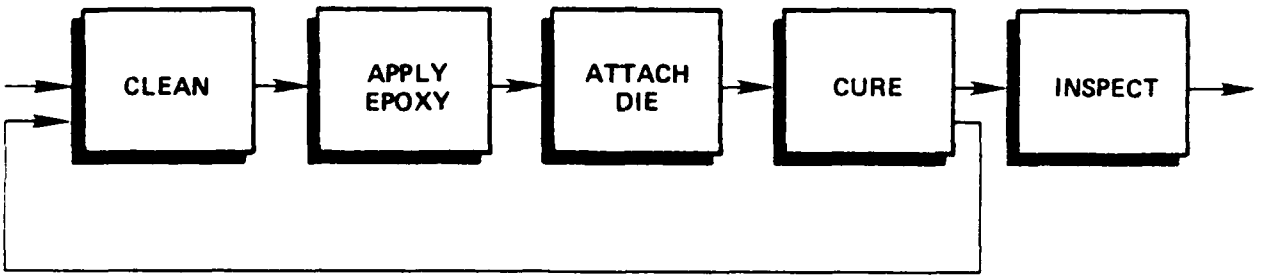


FIGURE 8.

ILLUSTRATIVE WIREBOND PROCESS FLOW

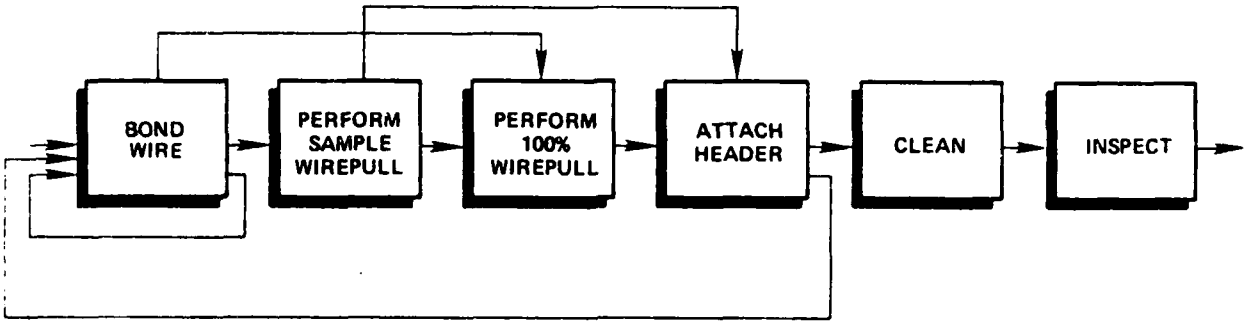
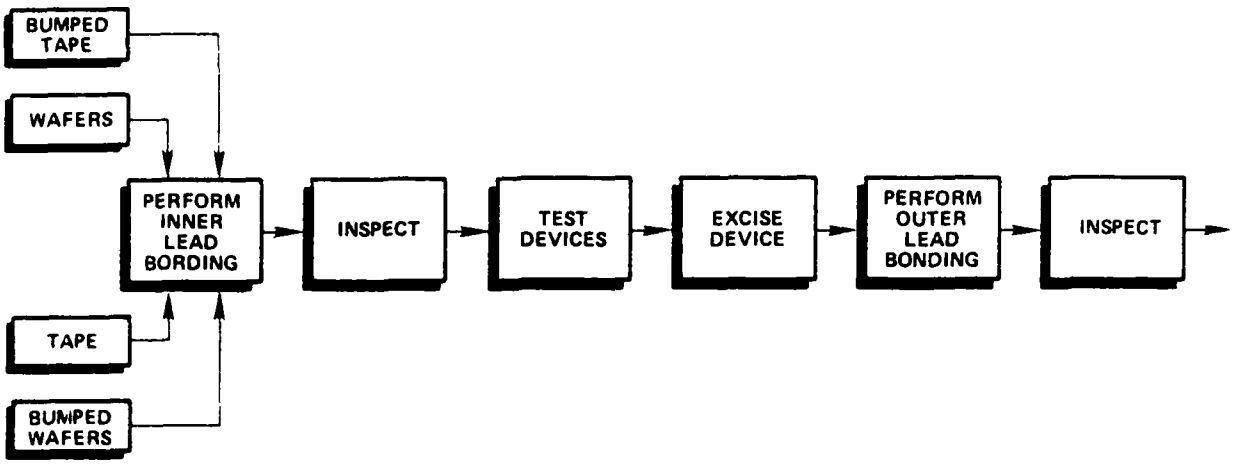


FIGURE 9.

TAB/BTAB ILLUSTRATIVE PROCESS FLOWS



TAB TAPE AUTOMATED BONDING
BTAB BUMPED TAPE AUTOMATED BONDING

The major disadvantages are the loss of in process design flexibility, the availability and standardization of materials, and the increased demand for surface area to connect TAB/BTAB and chip carriers to the substrate.

After mounting the header the hybrid is ready to be packaged. The leads are attached to the outside connectors and a package configuration is selected. The hybrid may be hermetically sealed in a metal case, it may be plastic encapsulated, or a conformal coating may be applied.

The hybrid (as a component or as a circuit) will undergo a certain degree of testing. This testing occurs on a functional basis and on an environmental basis. A functional test is a check on the actual electrical performance of the hybrid whereas an environmental test checks the hybrid under various operating conditions. The environmental tests (also known as screening tests) include the following;

- particle impact noise detection
- stabilization bake
- temperature cycle
- fine leak/gross leak
- burn-in
- acceleration/shock

Hybrids which fail the tests are fault isolated. This process may be manual (as in bench box test positions) or highly automatic (as in digital fault simulation).

A major contributor to hybrid failures are the active devices themselves. Hence, a prescreening program will increase hybrid yields. TAB, BTAB, and chip carrier technologies offer this aspect. A statistical sample plan can offer the same advantage for a chip/wire technology firm.

Computer Aided Manufacturing

Computer aided manufacturing for hybrid microelectronics can be used as a production tool in two basic modes. These are production support and in production automation. Process identification, process monitoring, process interaction, process control, and process planning are examples in these areas. (Refer to figure 10)

The bulk of computer aided manufacturing lies between the process interaction mode and the process control mode. As material handling, equipment automation, and automated test/inspect processes become more advanced and cost effective,the process control mode will become more widespread.

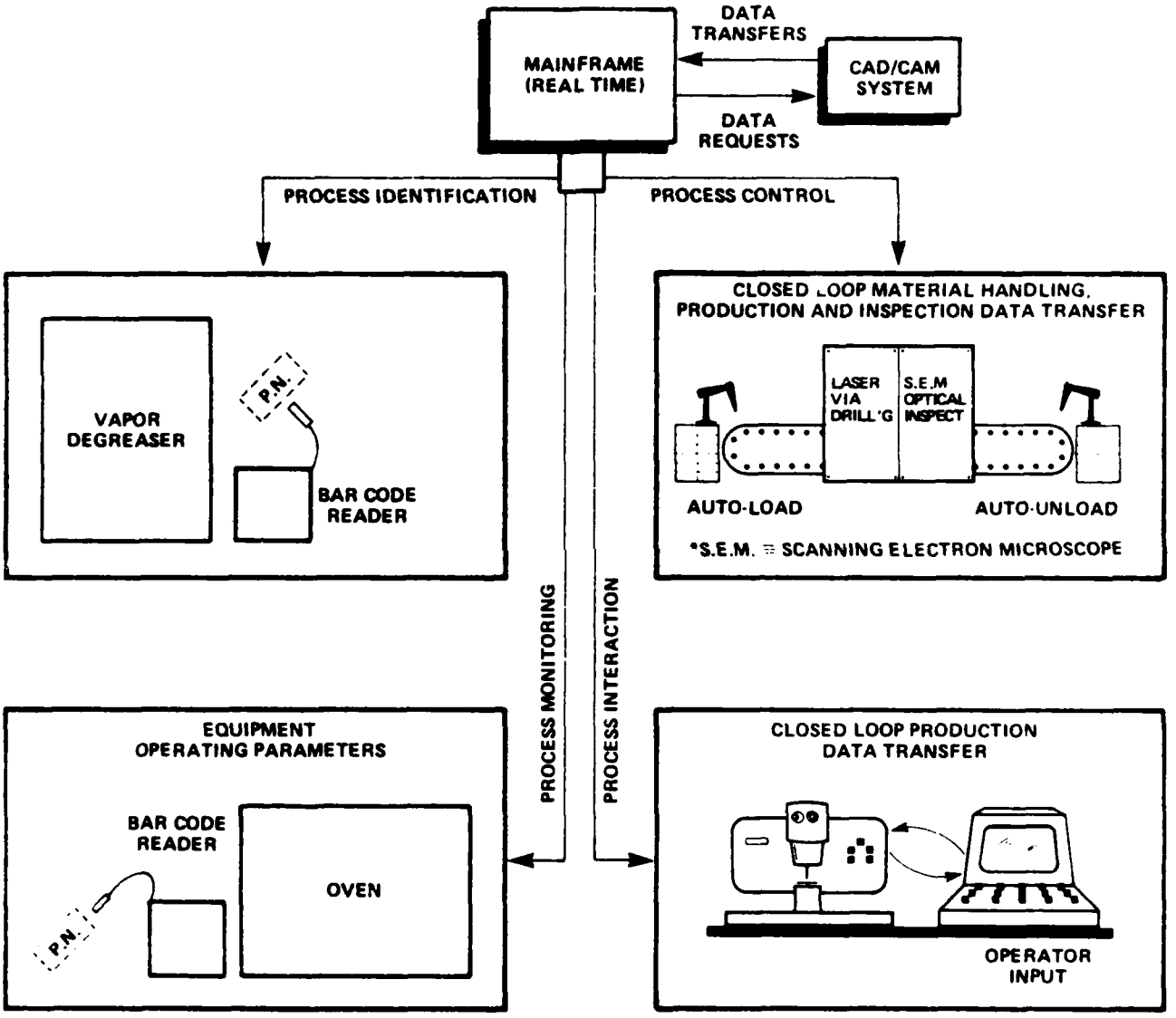
Certain concepts of group technology can be applied in interfacing the design and manufacture of hybrid circuits. Areas of interest include the compilation of component part characteristics, the performance of manufacturing flow analysis, and the generation of planning.

The compilation of part characteristics (via a library parts file) serves a function analogous to that of a coding and classification scheme. The library parts files identify various distinguishing factors (such as die topography, wirebond geographies,costs,wire sizes, etc) which can be used as inputs to a production planning and production operations system as well as the design process.

A manufacturing flow analysis can be utilized to achieve an optimal facilities layout. The component characteristics, when combined with the component counts and equipment specifications, can be used in determining co-location requirements to minimize production costs and times.

FIGURE 10.

ILLUSTRATIVE USES OF COMPUTER AIDED MANUFACTURING



Process planning and operator work instructions have been traditionally generated by manual methods, often consisting only of engineering drawings and handwritten instructions. As production levels and hybrid complexities increase these types of documentation and planning are no longer sufficient to accurately produce hybrids. The problem is intensified in the high mix-low volume environment where an operator rarely works on the same module long enough to realize learning curve benefits.

Use of a CAD database to generate process planning and to drive the automated manufacturing operations dictates that the design and manufacturing functions develop a mutual database specification. (Refer to figure 11) Computer generated planning is created interactively and offers significant advantages.

These advantages include variablity in the mode of presentation (traditional paper medium, CRT terminals, video displays, etc.), work instructions which accurately reflect the product engineering, and the automation of certain manufacturing operations and configuration control. One distinct advantage of using computerized planning is the accomodation of die topography variations.

Variations in different vendors' die topographies for electrically equivalent die provides a unique problem, especially in the low volume-high mix environment. This problem is intensified when contractual obligations force 'second source' requirements for unencapsulated chips. These variations in device topographies become particularly onerous at three points in the hybrid life cycle. These points are at constructing the library parts files, at component placement and routing, and in process automation.

Composite library parts may offer a solution to some of the

FIGURE 11.
SAMPLE OF COMPUTER GENERATED ROUTING SHEETS

[illegible] PLANNING - ASSEMBLY
SEQUENCE & INSTRUCTION SHEET

SHEET 1 OF 4

PROGRAM --
UNIT CODE --
PART NAME --
ASSEMBLY NUMBER --
DSG. CHG. LTR. --
PLANNING REVISION --
UNIT ITEM NAME --
MODEL --
S/N EFF. --
LOT EFF. CONTROL NO. --

ASSY. ENGR.

PROD. ASSUR. ENGR.

PROCESS ENGR.

PROJECT ENGR.

SAFETY ENGR.

NEXT ASSEMBLIES --

STANDARD HOURS
UNIT Y/Y CHG.

PLANNING ENGR.
DATE Y/Y CHG.

NOTE 1: THIS ITEM MUST BE ASSEMBLED IN AN AREA THAT MEETS THE REQUIREMENTS OF MP210.

NOTE 2: HANDLE PARTS PER MP238 AND MP240.

OPER. NO.	REV. NO.	ITEM NO.	WORK STA.	OPERATION DESCRIPTION	STANDARD HOURS SET-UP/100 PC
10		7746	H010	ISSUE MATERIAL PER MAPL.	
16		8231	8503	INSPECT KIT PER MAPL AND PIIM MCA-001.	
20		6213	H020	IDENTIFY S/N PER COMPOSITE GRAPHICS.	
25		8231	8504	LASER CUT PER DIG.	

FIGURE 11.
- continued -

ASSY NAME
ASSY NO.

OPER. NO.	REV. NO.	DEPT NO	WORK CTR.	OPERATION DESCRIPTION	STD. HOURS SET-UP/100 PC
30		6213	HH30	CLEAN SUBSTRATE PER MP211	
35		6213	HH35	INSTALL TAPER PATCHES PER MP233 & COMPOSITE GRAPHICS.	
50		6213	HH50	CONDUCTIVE DIE ATTACH PER MP233 & COMPOSITE GRAPHICS.	
50A		6213	HH50	CONDUCTIVE DIE ATTACH PER MP237 & COMPOSITE GRAPHICS.	
67		6213	HH70	NON-CONDUCTIVE DIE ATTACH PER MP238 & COMPOSITE GRAPHICS.	
75		6213	HH75	CURE PER MP224.	
77		8131	M503	INSPECT DIE PER FILM MCA-001 AND COMPOSITE GRAPHICS.	
100		6214	H100	1 MIL WIREBOND PER MP217 AND COMPOSITE GRAPHICS.	
100A		6214	H100	1 MIL WIREBOND PER MP244 AND COMPOSITE GRAPHICS.	
110		6214	HJ 0	0.7 MIL WIREBOND PER MP217 AND COMPOSITE GRAPHICS.	
120		6214	H150	NON-DESTRUCTIVE SAMPLE WIRE PULL PER MP234 & COMPOSITE GRAPHICS	
130		6214	H150	100% NON-DESTRUCTIVE WIRE PULL PER MP234 & COMPOSITE GRAPHICS.	
210		8131	M503	INSPECT WIREBOND AFTER VISUAL PER FILM MCA-001 AND COMPOSITE GRAPHICS.	
212		6233	H099	CLEAN HEADER PER MP211 AND HEATER ATTACH PER MP216 AND COMPOSITE GRAPHICS. CURE PER MP224.	

ASSY NAME --
ASSY NO.

FIGURE 11.
- continued -

SHEET 3 OF 4

OPER. NO.	REV. NO.	DEPT. NO.	WORK STA.	OPERATION DESCRIPTION	SYS. HOURS SET-UP/100 PC
214		6214	H180	2 MIL WIREBOND PER MP[illegible] AND COMPOSITE GRAPHITE	
214A		6214	H180	2 MIL WIREBOND PER MP[illegible] AND COMPOSITE GRAPHITE	
216		6214	H190	100% NON-DESTRUCTIVE SEAL PER MP[illegible] & COMPOSITE GRAPHITE.	
216		6214	H190	NON-DESTRUCTIVE SAMPLE SEAL PER MP[illegible] & COMPOSITE GRAPHITE.	
230		8271	8504	FUNCTIONAL TEST.	
240		6213	H240	CLEAN LID/MODULE PER MP[illegible].	
250		8231	8504	INSPECT PRECAP PER PIN 6CA-001.	
260		6213	H260	SEAL PER MP[illegible]	
270		6213	H270	IDENTIFY PER MP[illegible] AND DP 27[illegible]	
280		8231	8504	STABILIZATION BAKE.	
290		8231	8504	TEMPERATURE CYCLE.	
300		8231	8504	ACCELERATION.	

FIGURE 11.
- continued -

ASSY NAME --
ASSY NO. --

SHEET 3 OF 3

OPER. NO.	REV. NO.	DEPT. NO.	WORK STA.	OPERATION DESCRIPTION	STD. HOURS SET UP 100 PC
310		8231	8504	FINE LEAK.	
320		8231	8504	GROSS LEAK.	
330		8231	8504	PINCH.	
340		8231	8504	FUNCTIONAL TEST.	
350		8231	8504	BURN IN.	
360		8231	8504	FUNCTIONAL TEST.	
370		8231	9503	INSPECT FINAL PER PIM MIL-883. HOLD FOR QAE.	
380		7246	H380	MOVE TO NEXT ASSYSTEP.	

problems designers, placement algorithms, and routing algorithms face. A composite library part is one that is made up of electrically equivalent devices with very similar topographies. The similarities are rarely great enough to provide meaningful information for wirebonding and die attachment automation. The similarities are sufficient to ensure that when a hybrid is designed using composites, any die of that composite family may be used in the manufacturing process without violating standard manufacturing guidelines specifying chip fit on the pad, maximum wirebond length, wirebond egress angles from the chip,etc. Composite library parts are not a panacea for all problems caused by using multiple vendors for each die, but they do offer a solution to some of the problems. The creation of an 'artifical' intermediate does not come free. Composite libraries endure the same control and maintenance problems common to all library parts. The decision as to which composite a particular venders die belongs to must also be addressed.

Material Handing

Hybrid manufacturing involves very specialized and tenacious material handling problems. The size of microelectronic devices and their inherent fragility are two examples of these problems. As the military hybrid uses the most advanced state-of-the-art technology,and thus is the most uniquely configured,standardization is not a viable alternative.

Initial problems are encountered at the device attachment stage. Currently available pick and place mechanisms are not equipped to handle extremely small devices (less than 0.025 inches). Once the device is captured, the same pick and place mechanisms cannot rotate to insure the proper device orientation. This necessitates an extra material handling

step to repackage the devices to the new orientation prior to the pick and place step of device attachment.

Handling substrates during device attachment and wirebonding but prior to sealing represents another problem area. Automated substrate handlers are usually designed to accept one size of substrate. This inflexibility, when combined with the die fragility and the exposed flywires, leads to increased chances for damaging the work in process substrate.

Once sealed, the various package types represent unique handling difficulties. The automation of loading, unloading, and test head fixturing for automation are not feasible at current functional test, screening test, and fault isolation work stations due to package physical characteristics variations.

An ideal material handling system would have several characteristics which apply to most hybrid manufacturing operations. A list of these would include:

- three dimensional movement
- angular motion and circular motion
- very sensitive contact grippers/sensors
- optical character recognition
- interfaced with a CAD/CAM and MIS system
- self-correcting displacement compensation capability

- CAD/CAM DATABASE SPECIFICATIONS -

One of the greatest values of a CAD database is that, if properly constructed, it may also serve as the CAM database. Before significant automated use can be made of a database, its contents must be formally defined and structured. The vehicle for this task is the database specification. The hybrid database specification must provide efficiency for design activities as well as sufficiency for automated manufacturing tasks. Such a specification can not be derived without equal input from both the design and the manufacturing activities. A robust database specification must interface between controlling data types, subfigure data types, and the formal layering scheme (Refer to figure 12).

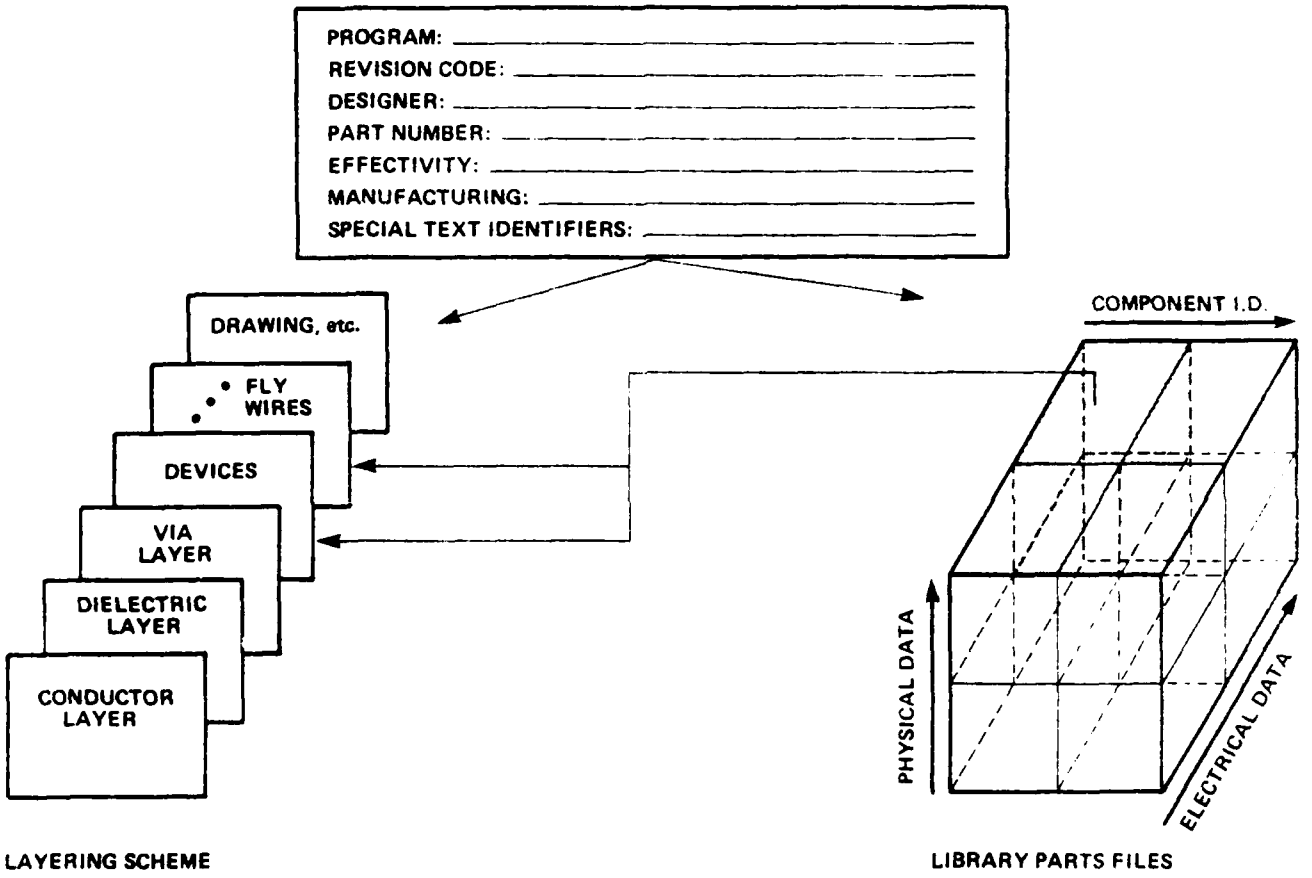
Controlling data represents an information subset which uniquely identifies the generated database of a particular hybrid circuit. This subset of the global database includes information such as part number, effectivity data, revision data, and part-peculiar engineering text.

Subfigure data are inseperable mappings of graphic and non-graphic entities within an engineering database (the intelligence of the database). This subfigure data is usually referred to as library parts files but may be known as cells. As these library parts files will be used throughout the CAD/CAM life cycle of numerous hybrids their integrity must be strictly maintained. The number and types of library parts files used vary from manufacturer to manufacturer. They generally contain data which includes logical, electrical, physical, and management oriented information.

Logical information includes net lists, pad numbers, signal nomenclature, and other signal flow data. This data will be used in verifying the electrical accuracy of the physical layout, as an input to the drawing

FIGURE 12.

ILLUSTRATIVE DATABASE INTERFACES



LAYERING SCHEME

LIBRARY PARTS FILES

of the electrical schematic, and in test program generation.

Physical information is used to generate the artwork, to drive automated manufacturing processes, and as input to the automatic test program. The physical database includes information on component size, length/width of circuit runs, device locations, device orientation, and such things as bond pad locations.

Electrical information kept in library parts files includes operating device characteristics and cross-references to electrically equivalent devices. This database is used as an input to circuit analyses, to the test program generation, to fault isolation programs, and as an aid to in-process design changes.

Management data includes information on production costs, on materials costs, on vender names, supplier names, and inspection criteria. This management database is useful in configuration tracking, cost tracking, pricing determinations, and other management associated activities.

The layering scheme represents the skeleton of the CAD process. It is a structured hierarchy of information storage and presentation and it establishes the mapping between physical reality and the computer data storages. An example of a layering scheme is detailed in figure 13. Care must be taken to avoid mixing hybrid circuitry layers with software layers.

Work on a macroscopic database management system is being conducted under the Integrated Program for Aerospace-Vehicle Design (IPAD). The IPAD software being developed would augment existing CAD/CAM and MIS systems. Relational and codasyl database management systems are being reviewed.

FIGURE 15.

ILLUSTRATIVE LAYERING SCHEME

GRAPHICS SYSTEM LAYER	DESCRIPTION	ENTITY TYPE
1 - 4	1st LAYER CIRCUITRY	LINE
5 - 9	1st LAYER DIELECTRIC	LINE
10 - 14	1st LAYER VIAS	LINE
15 - 19	2nd LAYER CIRCUITRY	LINE
20 - 24	2nd LAYER DIELECTRIC	LINE
25 - 29	2nd LAYER VIAS	LINE
30 - 154	OTHER LAYERS	LINE
155 - 159	LOWEST OHM INK PATTERN	LINE
160 - 164	NEXT HIGHEST OHM INK PATTERN	LINE
165 - 174	OTHER OHM INK PATTERNS	LINE
175 - 179	DEVICES – UNENCAPSULATED	SUBFIGURE
180 - 184	.0007 FLY WIRES	LINE
185 - 189	.001 FLY WIRES	LINE
190 - 194	.002 FLY WIRES	LINE
195 - 199	DEVICES – TAPE AUTOMATED BONDS	SUBFIGURE
200 - 204	DEVICES – CHIP CARRIER	SUBFIGURE
205 - 214	DRAWING FORMAT	SUBFIGURE
215 - 224	CONFIGURATION CONTROL FORMAT	TEXT
225 - END	DRAWING IDENTIFICATION DATA	TEXT

IPAD software developements are being directed at:

- executive software
- data management software
- geometry & graphics utility software

A relational database management system (Refer to figure 14) uses a series of 'key' accessed files to track and retrieve information. The success to this type of system lies in the querying structure. This method is easier to comprehend, easier to code but it creates an excess of duplication in the database and consistency problems may occur.

A codasyl database management system (Refer to figure 15) uses pointers at the end of each information location to direct the system to the next data point. This type of system is difficult to code, is difficult for a non-technical user to comprehend, but is computationally faster and reduces data duplication.

IPIP is the IPAD Information Processor. This is an N-level data architecture which uses logical, internal, and mapping schemas. IPIP will permit database access from either a navigational data manipulation (a codasyl based system) or a relational data manipulation (a relational based system). Further information on IPIP is available under NASA contract NAS1-14700, technical plan D6-IPAD-70002-P, subtask D6-IPAD-70038-D, "Manufacturing Data Management Requirements", Boeing Commercial Airplane Company, Seattle, Washington.

FIGURE 14.

ILLUSTRATIVE RELATIONAL DATABASE MANAGEMENT SYSTEM

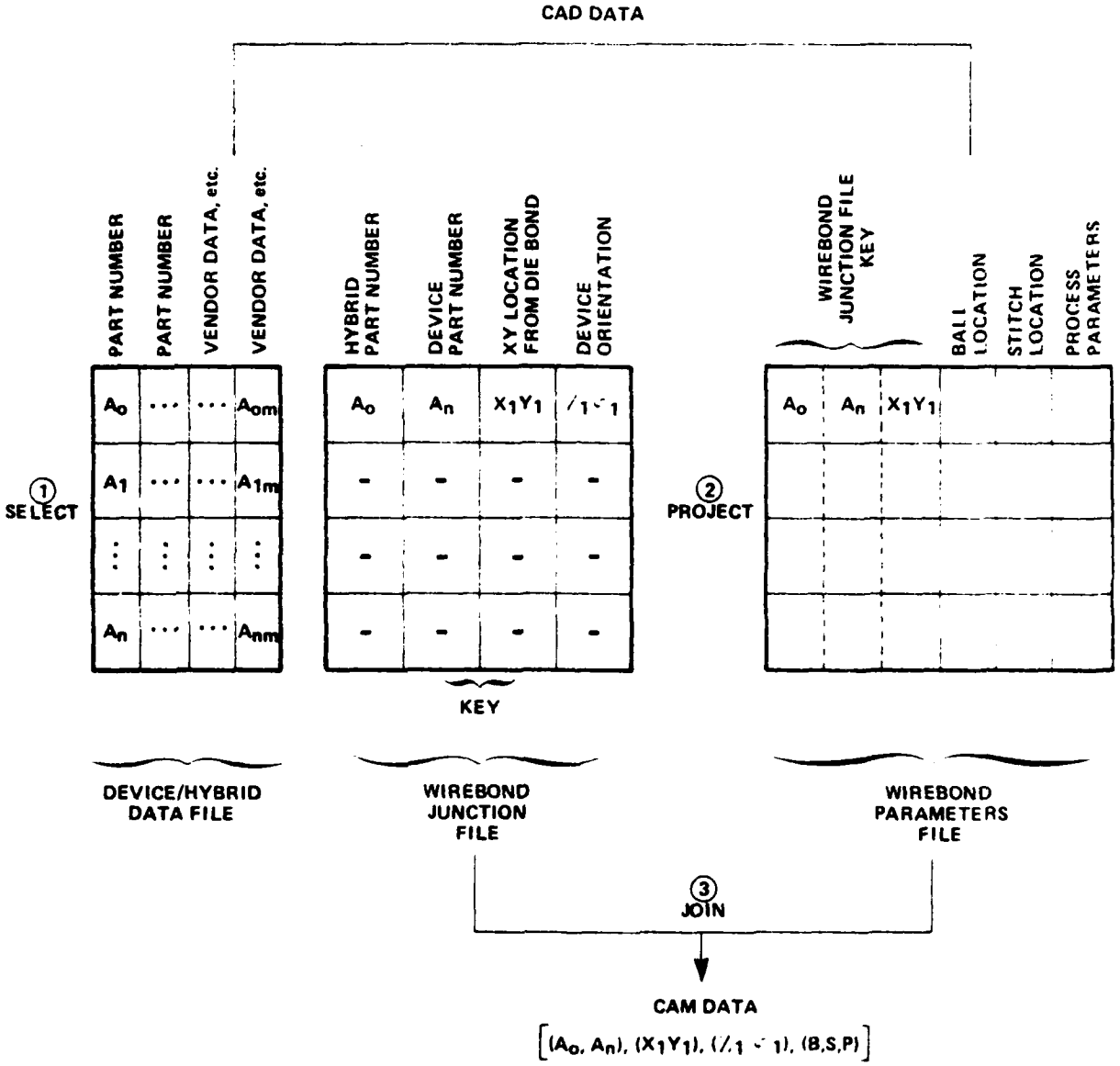
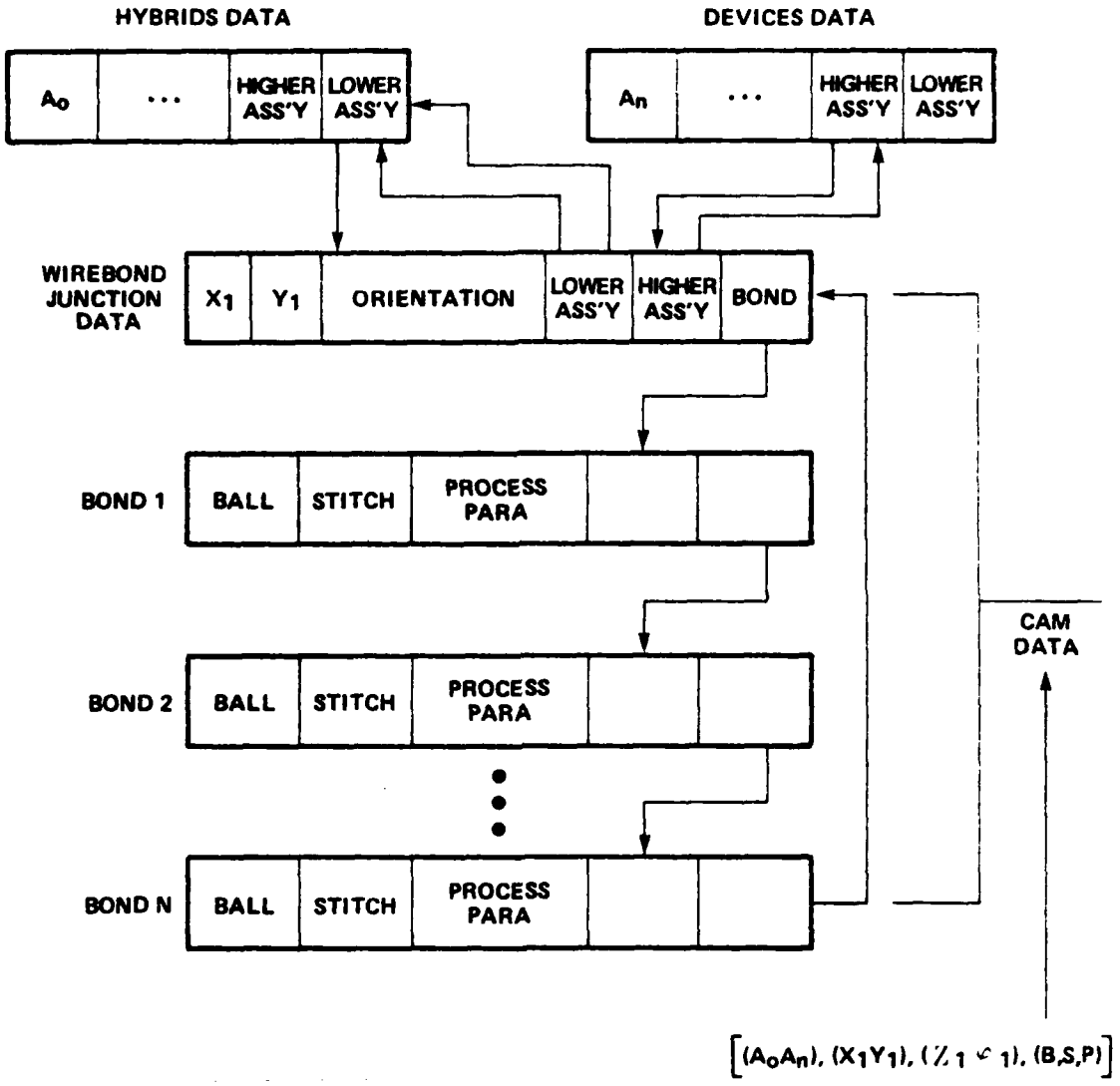


FIGURE 15.

ILLUSTRATIVE CODASYL DATABASE MANAGEMENT SYSTEM



- CURRENT/PLANNED MAN TECH PROJECTS -

A review of current and planned Army, Navy, and Air Force manufacturing methods and technology projects for hybrid circuits has been undertaken. A list of these projects with a cross-reference to the HICADAM architecture is attached as figure 16. As the MAN TECH programs are under a continuous revision process the timeliness of this list should be verified prior to its use. Where possible the listed projects include the project number, or the contract number, the responsible agency, and the estimated year for funding.

A description of each project is beyond the scope of this report. Numerous sources of information on these projects exist. The most current description of these MAN TECH projects exists in the following reference:

> "Overview of Current and Planned Army, Navy, and Air Force MMT Contracts for Hybrid Circuit Technology", Charles E. McBurney, Manufacturing Technology Division, Industrial Base Engineering Activity, Rock Island, Illinois.

This paper will be presented at the Proceedings of the International Society for Hybrid Microelectronics which takes place on October 12 through 14, 1981.

Hughes Aircraft is currently working on several MAN TECH projects in support of a new missile system. Information on these projects will be made available after a contract award occurs.

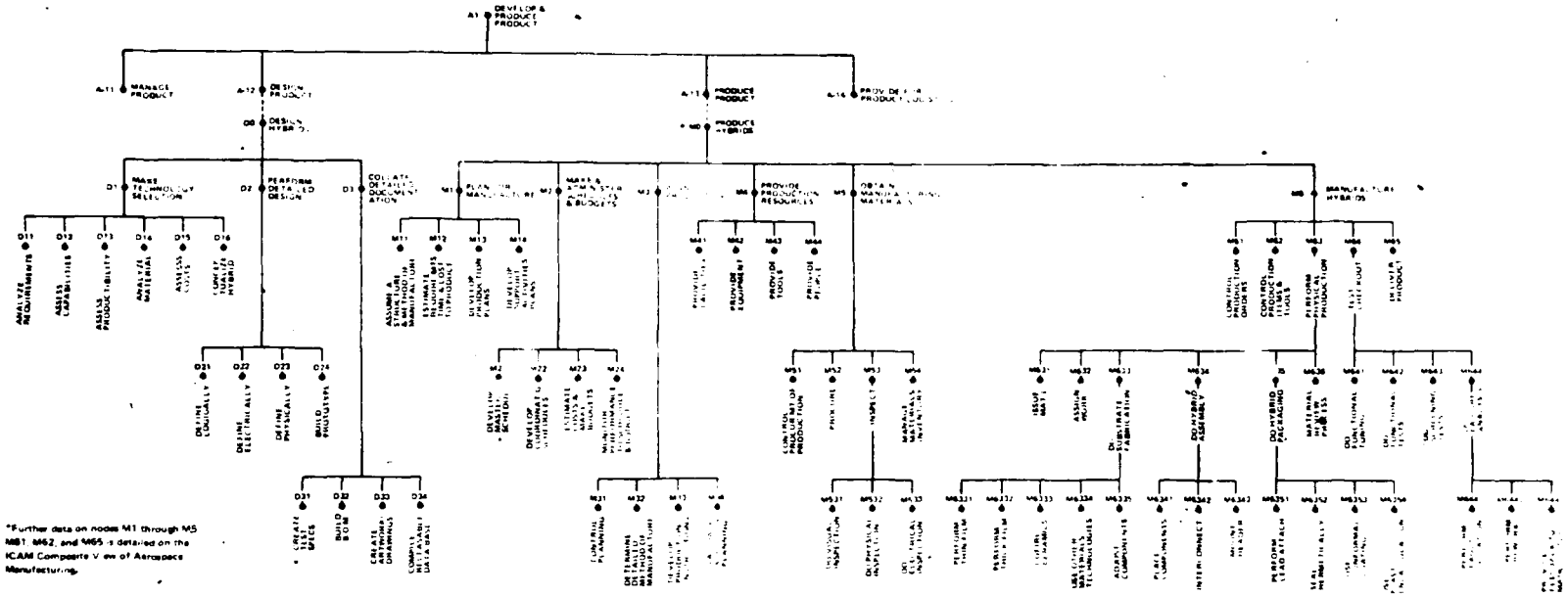
FIGURE 16.

HYBRID MAN TECH PROJECTS

ARCH. NODE	NODE TITLE	MAN TECH NUMBER	YEAR	RESP. AUTH.	MAN TECH TITLE
D-0 M-0	DESIGN & MANUFACTURE HYBRIDS	3-80-1071	1980	ARMY	HYBRID INTEGRATED COMPUTER AIDED DESIGN & MANUFACTURING
		3-81-1071	1981	ARMY	HYBRID INTEGRATED COMPUTER AIDED DESIGN & MANUFACTURING
		18-E-572-1X086101	1981	USAF	MT FOR ELECTRONICS CAD/CAM (ECAM)
		3-82-1075	1982	ARMY	ELECTRONICS COMPUTER AIDED MANUFACTURING (ECAM)
		18-E-572-1X086101	1983	USAF	MT FOR ELECTRONICS CAD/CAM (ECAM)
M5	OBTAIN MATERIALS	3-81-1060	1981	ARMY	ELECTRICAL SCREENING AND TEST OF CHIPS
		3-82-1091	1982	ARMY	ELIMINATION OF PRECIOUS METALS IN MICROCIRCUITS
		3-81-1059	1981	ARMY	ELECTRICAL VERIFICATION & BURN-IN OF HYBRID CHIPS
M633	DO SUBSTRATE FABRICATION	DNA-81016	1981	NAVY	AUTOMATIC MICROSTRIP CIRCUIT BOARD FABRICATION
		DNE-00137	1981	NAVY	MICROWAVE STRIPLINE CIRCUITRY PROCESSES
		3-82-1092	1982	ARMY	AUTOMATIC TESTING OF SUBSTRATES
M6331	PERFORM THIN FILM	DNA-00675	1979	NAVY	HIGH OHMS PER SQUARE THIN FILM RESISTORS
		F-81-9835	1981	ARMY	INTEGRATED THIN FILM TRANSISTOR DISPLAY
		F-82-9835	1982	ARMY	INTEGRATED THIN FILM TRANSISTOR DISPLAY
		DNA-00674	1982	NAVY	MULTIPLE SHEET RESISTANCE THIN FILMS
		DNA-006XX	1982	NAVY	MICROBRIDGE CROSSOVERS FOR THIN FILM HYBRIDS
		DNA-006ZZ	1983	NAVY	MONOMER FILMS FOR THIN FILM HYBRIDS
		DNE-034YY	1983	NAVY	EXTRA HIGH FREQUENCY IC's (THIN & THICK FILM CIRCUITRY)
M6332	PERFORM THICK FILM	3-79-3146	1979	ARMY	HIGH DENSITY MULTILAYER THICK FILM HYBRID MICROCIRCUITS
		DNA-00053	1979	NAVY	COMPUTERIZED THICK FILM PRINTER
		3-80-3435	1980	ARMY	SIMPLIFICATION OF HIGH POWER THICK FILM HYBRIDS
		H-81-9552	1981	ARMY	THICK FILM CONDUCTIVE NETWORKS
		DNE-034YY	1983	NAVY	EXTRA HIGH FREQUENCY IC's (THIN & THICK FILM CIRCUITRY)
M6341	PLACE COMPONENTS	3-79-3219	1979	ARMY	AUTOMATIC POLYMER ATTACHMENT PRODUCTION METHODS
		3-80-3219	1980	ARMY	AUTOMATIC POLYMER ATTACHMENT PRODUCTION METHODS
		F33615-80-C-5053	1980	USAF	MT FOR SUBSTRATE ASSEMBLY WITH HERMETIC CHIP CARRIERS
		3-81-1076	1981	ARMY	PATTERN RECOGNITION OF COMPONENTS FOR HYBRIDS
		3-82-1076	1982	ARMY	PATTERN RECOGNITION OF COMPONENTS FOR HYBRIDS
M6342	INTERCONNECT	DNS-00481	1977	NAVY	BUMPED TAPE AUTOMATIC BONDING
		F33615-77-C-5283	1977	USAF	MT FOR HERMETIC CHIP CARRIER PACKAGING (HUGHES)
		F33615-77-C-5158	1977	USAF	MT FOR HERMETIC CHIP CARRIER PACKAGING (RCA)
		F33615-78-C-5158	1978	USAF	MT FOR HERMETIC CHIP CARRIER PACKAGING (TI)
		F33615-78-C-5147	1978	USAF	MT FOR LOW COST CHIP CARRIERS
		DNS-00712	1980	NAVY	HERMETIC CHIP TAPE CARRIER
		F-33615-80-C-5010	1980	USAF	MT FOR HI-RELIABILITY WIREBONDING IN HYBRID CIRCUITS
		08-E-504-1B084130	1981	USAF	SUBSTRATE ASSEMBLY WITH HERMETIC CHIP CARRIERS
		H-82-5005	1982	ARMY	SEALED CHIP TAPE CARRIER FOR HYBRIDS
M635	DO HYBRID PACKAGING	F33615-80-C-XXXXX	1980	USAF	HIGH SPEED DIGITAL PROCESSOR PACKAGING TECHNIQUES
		11-E-503-1A084260	1981	USAF	HIGH SPEED DIGITAL PROCESSOR PACKAGING TECHNIQUES
		11-E-503-1A084260	1983	USAF	HIGH SPEED DIGITAL PROCESSOR PACKAGING TECHNIQUES
		28-E-583-2A08XXXX	1982	USAF	HIGH RELIABILITY PACKAGING
		28-E-583-2A08ZZZZ	1983	USAF	HIGH RELIABILITY PACKAGING
M6351	PERFORM LEAD ATTACH	DNA-00679	1977	NAVY	AUTOMATED HYBRID LEAD ASSEMBLY
M6352	SEAL HERMETICALLY	3-82-1095	1982	ARMY	AUTOMATIC SEALING OF HYBRIDS
M6441	PERFORM FAULT ISOLATION	3-80-1023	1980	ARMY	DIGITAL FAULT ISOLATION FOR HYBRIDS
M6442	PERFORM REWORK	3-79-3438	1979	ARMY	DELIDDING PARALLEL SEAM SEALED HYBRID PACKAGES
		DNA-00253	1980	NAVY	DELIDDING & RESEALING OF HYBRID MICROCIRCUITS
OTHER		3-79-3410	1979	ARMY	PRODUCTION METHODS FOR HEAT PIPES FOR HYBRIDS/LSI
		3-80-3436	1980	ARMY	DEVELOPEMENT OF CERAMIC CIRCUIT BOARDS & LARGE AREA HYBRIDS
		3-80-1024	1980	ARMY	RF STRIPLINE HYBRID COMPONENTS
		3-80-7319	1980	ARMY	DIGITALLY ADDRESSABLE MULTI-LEGEND DISPLAY SWITCH
		3-81-1066	1981	ARMY	ADDITIVE SINGLE & MULTILAYER HYBRID CIRCUITRY
		3-81-7319	1981	ARMY	DIGITALLY ADDRESSABLE MULTI-LEGEND DISPLAY SWITCH
		N62269-81-C-0067	1981	NAVY	BROADBAND SOLID STATE HIGH POWER RF AMPLIFIERS
		3-82-3081	1982	ARMY	RADAR MONOPULSE SEEKER USING PC & STRIPLINE TECHNIQUES
		3-82-1066	1982	ARMY	ADDITIVE SINGLE & MULTILAYER HYBRID CIRCUITRY
		1-82-7319	1982	ARMY	DIGITALLY ADDRESSABLE MULTI-LEGEND DISPLAY SWITCH
		H-82-5114	1982	ARMY	MINI-LASER TRANSMITTER MODULE
OTHER		3-83-1024	1983	ARMY	RF STRIPLINE HYBRID COMPONENTS

HICADAM SYSTEMS ARCHITECTURE

FIGURE 1A.
- supplement -



*Further data on nodes M1 through M5 M81, M62, and M65 is detailed on the ICAM Composite View of Aerospace Manufacturing.

Figure 17.

1. What is your primary end product application ?

5 responses	☒	aerospace
3 responses	☒	communication
1 response	☒	computer
	☐	consumer
	☐	industrial
	☐	instrumentation, test equipment
1 response	☒	other, please specify :

2. What is your primary involvement with hybrid circuits ?

	☐	semiconductor products
1 response*	☒	production equipment for hybrid circuits
6 responses*	☒	custom hybrid design/manufacture
5 responses*	☒	general hybrid design/manufacture to support end product
	☐	other, please specify :

* one firm responded to doing each thing

3. What type of system do you use to support the design and manufacture of hybrid circuits ?

	Computer Aided Design	Computer Aided Manuf.
turnkey system	5 responses	4 responses
dedicated mainframe	-	-
general time sharing mainframe	3 responses	-
other, please specify :	-	1 response (test)
MANUAL	2 responses	5 responses

4. Is your CAM database generated from :

5 responses	☒	a released CAD database
	☐	a separate CAM database formulation
5 responses	☒	a CAM database is not generated
	☐	other, please specify:

Figure 18.

If you have a computer system to support the design of hybrid circuits please check the capabilities which you use & the system where they reside.

capability	CAD/CAM turnkey	CAD/CAM mainframe	general TS mainframe	other
library parts (drawing symbols)	5	2	0	0
library parts (component specs.)	5	1	0	1
partitioning algorithm	0	0	1	1
component placement algorithm	0	1	2	1
routing algorithm	1	2	1	1
circuit simulation	1	0	5	1
thermal analysis	0	1	4	1
test program generation	1	0	1	3
configuration control	1	1	2	1
other, please specify : Artwork & Design Rules Check	3	0	0	0

NO RESPONSE : 2

Please check the appropriate box for the following data.

algorithm	internally developed	commercially avail.	other
partitioning	4	0	1
component placement	4	1	1
routing	3	2	1
circuit simulation	2	6	1
circuit analysis	3	4	1
test program generation	3	1	2
other, please specify :	3	2	0

NO RESPONSE : 2

numbers inside the boxes represent the respondents (total) who answered that question or checked a box

Figure 19.

. Please rate the percentage of total design time dedicated to each task.

capability	less than						
	20%	40%	60%	80%	90%	95%	100%
schematic generation	7	3	0	0	0	0	0
partitioning	6	0	0	0	0	0	0
component placement	5	1	2	0	0	0	0
routing	5	3	0	0	0	0	0
test program generation	5	1	0	0	0	0	0
configuration control	7	0	0	0	0	0	0
other, please specify :	4	0	0	0	0	0	0

. Please rate the effectiveness of those capabilities as to degree of task accomplished automatically.

capability	- less than -						
	20%	40%	60%	80%	90%	95%	100%
schematic generation	0	0	1	1	1	1	0
partitioning	1	0	0	1	0	0	0
component placement	2	0	3	0	0	0	0
routing	1	0	0	1	2	0	0
test program generation	1	2	0	0	0	0	0
configuration control	2	0	0	1	0	0	0
other, please specify :	0	0	0	0	1	1	2

NO RESPONSE : 4

. Please rate the percentage of design time per task required to manually complete the task.

capability	less than						
	20%	40%	60%	80%	90%	95%	100%
schematic generation	7	1	0	0	0	0	2
partitioning	5	0	0	0	0	0	2
component placement	5	1	1	1	0	0	2
routing	7	0	0	1	0	0	2
test program generation	2	2	3	0	0	0	1
configuration control	5	0	1	0	0	0	1
other, please specify :	4	0	0	0	0	0	0

. numbers inside the boxes represent the total boxes checked by the respon

Figure 20.

-actual numerical responses are inside the boxes-

1). Please rank the following processes for cost contribution from 1 to 12 with process #1 having the greatest cost contribution.

	equipment	material	process
photolithography	3,6,5	4,2,6	1,11,10,7
additive circuit delineation	4,7	4,1	7,12
subtractive circuit delineation	5,11,7	3,5	8,10,4,8
screen printing	2,7,6,6,6	1,2	6,7,5,5
laser trimming	1,1,2,7	8	5,9,8,11
device attachment(TAB,BTAB,CC,etc)	2,8,8,4,2	3,8,3	5,4,6,3,4
wirebonding	3,9,4,3,4,3	1,5,4	6,3,5,2,3
wirepulling	2,11,9,5	1,7,10	3,12,3,7,10
inspection	5,10,10,8,1,4	// 1,6,12	5,9,2,9,9,2
functional testing	6,2,2,1,1	1,10,7	7,2,4,1,2
fault isolation	4,3,3,1,3,5	2,11,9	4,11,1,1,1
material handling	2,12,12	2,9,11	10,10,8,6,6

2). Please rank the following factors for possible technological advancement from manufacturing technology developements with 1 being the most promising and 12 being the least promising.

	equipment	material	process
photolithography	6,12,7,12	4,5,2	4,12,4
additive circuit delineation	7,11,5,11	5,2,3	6,11,1
subtractive circuit delineation	8,9,6,10	6,6,4	10,10,10
screen printing	4,5,10,4,4,6	// 3,1,1,1	2,3,8,5
laser trimming	2,8,12,7	7,8	5,9,12
device attachment(TAB,BTAB,CC,etc)	2,3,4,1,1	8,3,3	4,11,3,3
wirebonding	10,4,5,2,2,2	5//6,2,4,5	8,7,4,2
wirepulling	7,12,6,11,8	12,9	5,12,6,11
inspection	3,9,2,3,1,3	2// 11,11,12	//6,1,2,9,2
functional testing	4,1,7,9,1,9	1,9,7	5,2,7,6
fault isolation	3,10,1,1,10	//11,10,10	4,9,1,7
material handling	1,11,3,8,4	8,8,11	1,8,5,8

Figure 21.

data entry format : response average (number of respo

Please rank the following processes for cost contribution from 1 to 12 with process #1 having the greatest cost contribution.

	equipment	material	process
photolithography	4.67(3)	4.00(3)	3.25(
additive circuit delineation	5.50(2)	2.50(2)	9.25(
subtractive circuit delineation	7.67(3)	4.00(2)	7.50(
screen printing	5.40(5)	1.50(2)	5.75(
laser trimming	2.75(4)	8.00(1)	8.25(
device attachment(TAB,BTAB,CC,etc)	4.80(5)	4.67(3)	4.40(5)
wirebonding	4.33(6)	3.33(3)	3.80(5)
wirepulling	6.75(4)	6.00(3)	7.00(5)
inspection	6.00(6)	6.33(3)	6.00(6)
functional testing	2.40(5)	6.00(3)	3.20(5)
fault isolation	3.80(5)	7.33(3)	3.60(5)
material handling	8.67(3)	7.33(3)	8.00(5)

Please rank the following factors for possible technological advancement from manufacturing technology developements with 1 being the most promising and 12 being the least promising.

	equipment	material	process
photolithography	9.25(4)	3.67(3)	6.67(3)
additive circuit delineation	8.50(4)	3.33(3)	6.00(3)
subtractive circuit delineation	8.25(4)	5.33(3)	10.00(3)
screen printing	5.50(6)	1.50(4)	4.50(4)
laser trimming	7.25(4)	7.50(2)	8.67(3)
device attachment(TAB,BTAB,CC,etc)	2.20(5)	4.67(3)	5.25(4)
wirebonding	4.29(7)	4.25(4)	5.25(4)
wirepulling	8.80(5)	10.50(2)	8.50(4)
inspection	3.29(7)	11.33(3)	4.00(5)
functional testing	5.16(5)	6.00(3)	5.00(4)
fault isolation	4.67(6)	10.33(3)	5.25(4)
material handling	5.40(5)	9.00(3)	5.50(4)

Figure 22.

MANUAL RESPONSES ONLY !

12. Please denote the degree of automation used for the following processes:

M = manual; S = semi-automatic; A = automatic:

	monitoring	load, unload	positioning	process control	inspect	test
photoresist application	1	3	3	2	2	2
photoresist exposure	1	3	2	2	3	–
photoresist develop.	1	3	3	3	3	1
vacuum system- vapor	–	1	1	–	1	–
vacuum system- sputter	–	2	1	–	2	1
etching system	3	4	4	4	–	
screen printing	6	4	3	7	3	–
laser trimming	1	5	–	1	4	–
continuity tester	–	4	2	1	–	1
die attach	5	6	5	6	–	
tape carrier bonding	–	1	–	–	1	–
bump tape auto. bonding	–	–	–	–	1	–
chip carrier bonding	1	2	1	–	3	2
inner lead bonding	–	1	–	1	1	
outer lead bonding	–	–	–	–	1	1
wirebond-for chip/wire	3	4	2	1	4	–
autopull	3	5	5	3	4	–
inspection	6	5	4	5	7	–
sealing	3	5	2	3	–	2
functional test	4	6	3	3	2	1
burn in/isolation-analog	4	4	4	4	4	
burn in/isolation-digital	2	2	2	2	2	
leak test	3	7	4	3	3	3
temperature cycle	1	6	2	1		–
stabilization bake	3	7	3	2	3	
burn-in test	1	7	3	2	3	
other, please specify:	–	–	–	–	–	–

Figure 23.

SEMI-AUTOMATIC RESPONSES ONLY !

12. Please denote the degree of automation used for the following processes.

M - manual; S = semi-automatic; A = automatic:

	monitoring	load/ unload	positioning	process control	inspect	test
photoresist application	2	-	-	1	-	-
photoresist exposure	2	-	1	1	-	
photoresist develop.	1	-	-	-	1	-
vacuum system- vapor	-	1	-	-	1	1
vacuum system- sputter	1	-	1	1	1	1
etching system	-	-	-	-	-	-
screen printing	1	4	2	-	2	1
laser trimming	1	1	1	1	1	
continuity tester	-	-	-	-	1	-
die attach	1	2	2	1	-	1
tape auto. bonding	-	-	-	-	-	-
bump tape auto. bonding	-	-	-	-	-	-
chip carrier bonding	2	-	1	1	-	1
inner lead bonding	1	1	1	1	-	-
outer lead bonding	1	1	1	1	-	-
wirebond-for chip/wire	1	1	-	2	1	1
wirepull	2	2	2	3	1	1
inspection	-	-	1	-	-	-
sealing	4	2	4	3	2	2
functional test	-	-	-	1	2	-
fault isolation-analog	-	-	-	-	1	2
fault isolation-digital	-	-	-	-	-	1
leak tests	1	-	1	1	1	
temperature cycle	2	1	-	-		
stabilization bake	1	-	-	1	-	-
burn-in test	2	-	-	2	-	
other, please specify:	-	-	-	-	-	-

Figure 24.

AUTOMATIC RESPONSES ONLY !

12. Please denote the degree of automation used for the following processes.

M = manual; S = semi-automatic; A = automatic:

	monitoring	load/ unload	positioning	process control	inspect	test
photoresist application	–	1	1	–	–	–
photoresist exposure	–	1	1	1	–	–
photoresist develop.	1	1	1	1	–	–
vacuum system– vapor	1	–	1	2	–	–
vacuum system– sputter	1	1	1	2	–	–
etching system	–	–	–	–	–	–
screen printing	–	–	3	1	–	–
laser trimming	4	1	6	4	1	4
continuity tester	4	1	3	2	3	3
die attach	–	–	1	–	–	–
tape auto. bonding	1	1	2	1	–	1
bump tape auto. bonding	1	1	1	1	–	1
chip carrier bonding	–	1	1	2	–	–
inner lead bonding	–	–	2	–	–	–
outer lead bonding	–	–	1	–	–	–
wirebond–for chip/wire	2	2	6	4	–	–
wirepull	–	–	–	–	–	–
inspection	–	–	–	–	–	–
sealing	–	–	1	1	–	–
functional test	2	1	2	1	1	2
fault isolation–analog	–	–	–	–	–	1
fault isolation–digital	–	–	–	–	–	1
leak tests	1	–	–	2	1	2
temperature cycle	2	–	3	4	1	3
stabilization bake	–	–	1	2	–	1
burn–in test	1	–	1	2	–	1
other, please specify:	–	–	–	–	–	–

Figure 25.

13. How is the following data compiled/generated ? Check the appropriate box.

	CAD/CAM turnkey	CAD/CAM mainframe	general/TS mainframe	other
vendor die topography	2	1	1	4
production planning	1	1	4	1
programs for laser trimming	2	1	-	3
programs for device attach.	2	-	2	2
programs for wirebonding	1	-	2	-
configuration control	1	1	1	3
other, please specify :	-	-	-	-

1 sel- tea

14. How is this data transfered between systems ? Check the appropriate box.

	on line	off line	MANUAL
vendor die topography	-	4	1
production planning	2	2	1
programs for laser trimming	-	3	1
programs for device attach.	-	3	1
programs for wirebonding	-	2	1
configuration control	-	3	1
other, please specify :	-	-	-

NO RESPONSE : 3

15. Briefly describe a problem whose solution would be of significant benefit in the areas of hybrid design and manufacture.

NO RESPONSE : 6

1. team work between divisions
2. automated inspection
3. automated parts identification
4. standardize to chip carriers
5. develop solid encapsulation to avoid hermetic sealing
6. replacement for gold metalliza-
7. eliminate wirebonding
8. higher value thin film resist- better temperature coefficient-

16. Would you like to see the results of this survey? yes no

Would you consider discussing this survey over the phone? yes no

If the answer is yes please include your name and phone number.

- SURVEY SUMMARY -

The response to the industry survey was very limited. Forty questionaires were mailed out. Ten responses were received back The compilation of the ten responses is detailed in figures 17 through 25. The compiled data is not statistically significant. The identified problems from question 15 were addressed in the Future MAN TECH area of this report if they were of significant depth. The lack of response to the survey may be attributed to industry disinterest, a natural desire not to disclose a percieved competitive advantage, and the length of the survey itself. The Proceedings of the Fourth MTAG Hybrid Workshop-Conference indicates that only 24% of the attendents viewed HICADAM as a high priority MAN TECH project, which supports the lack of response to the survey.

-FUTURE MAN TECH AREAS -

A roadmap for future MAN TECH efforts is presented. The candidate tasks identified are directed towards the cost effective advancement of an integrated and automated hybrid microelectronics manufacturing facility. Each task represents an integral building block in achieving the automated factory yet does not have any current or planned MAN TECH expenditures. The majority of these tasks are directed at integration aspects for interfacing the design and manufacture of hybrids.

The tasks were identified as follows. An overview of current design and manufacturing activities was developed. Problem areas were identified through this overview, through an industry survey (which may not be statistically significant), and through discussions with design and manufacturing personnel. These areas were compared with a compilation of future and ongoing MAN TECH projects. The candidate tasks were selected where no funding was planned for an identified problem. (refer to figure 36 for compilation)

Current and planned MAN TECH projects are directed at materials and equipment advancements or at specific end item technologies. These expenditures will reduce production costs and lead towards an automated factory. The current and planned funding programs will not lead to the viable integration of this automated factory. While the automation of the specific processes is sought the ability for these automated machines to communicate with each other and with other computers is not assured.

The proposed roadmap has two added thrusts. First, the integration of the CAD database and the CAM database is pursued. Second, the ability for inter-machine/computer communication is pursued. Integration is not as glamorous as automation but its lack can eliminate the synergy of automation.

Hybrid Microelectronics Database Specifications

The hybrid database specification is the framework for establishing a CAM database during the design phase in the life cycle of a hybrid. This database structure can be viewed as being empty at the start of the design process. As the hybrid is designed this structure becomes populated with information (electrical, physical, and logical) about the hybrid. The structure, when fully populated, contains the information required to support automated production facilities and the information is filed to provide the efficiency required for real time applications.

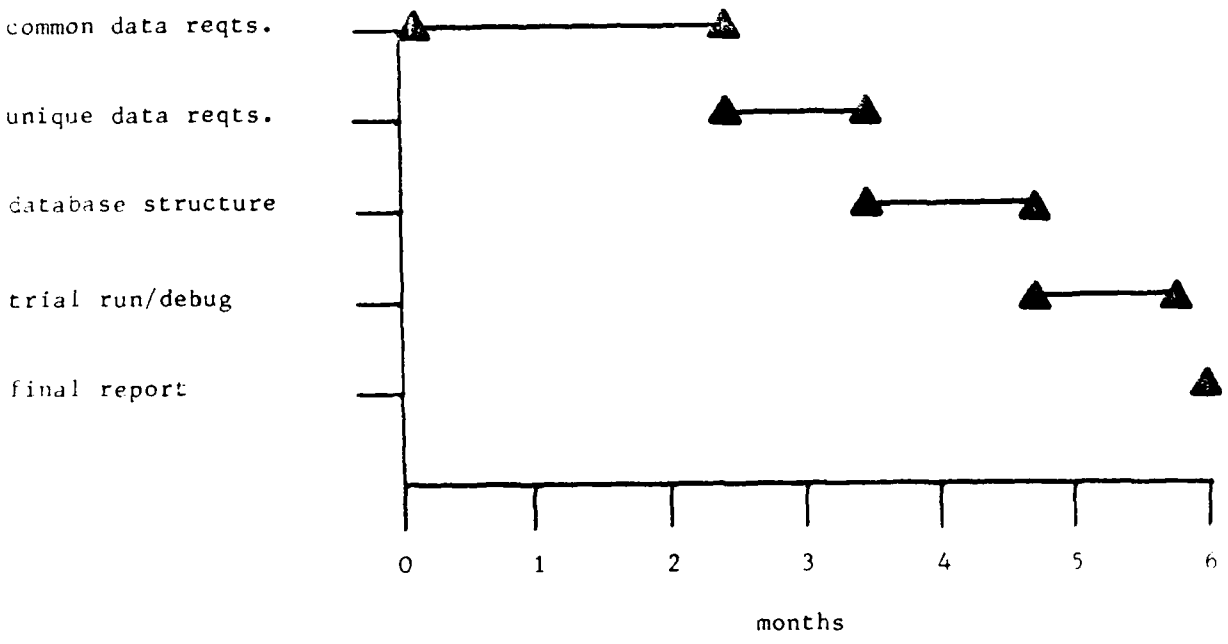
The first step is to map the data needs, both common and unique, required by specific manufacturing processes and support functions. This mapping specifies data content, where this data is required, and where this data is generated. This analysis aids in defining input and output requirements.

The database structure can then be established. This structure must permit the efficient filing of common and unique data. The type of structure (hierarchical, network, or relational), the field lengths, and data formats must be selected. The files should be organized around IGES (interim graphics exchange specifications) formats.

Finally, the documentation for this database specification must be developed. This documentation should contain sufficient written and pictorial information so that the end user can understand the database structure and its applications.

Future MAN TECH projects would be approached so that this database specification could be used to support the automation of manufacturing processes. This will ensure that automated equipment can interrogate the same database and will ensure the transportability of automated processes.

FIGURE 26.
HYBRID DATABASE SPECIFICATIONS



Estimated Budget :

labor.....	$67,200	*
computer time..	22,500	#
travel.....	3,300	
total costs....	$93,000	

* one man year

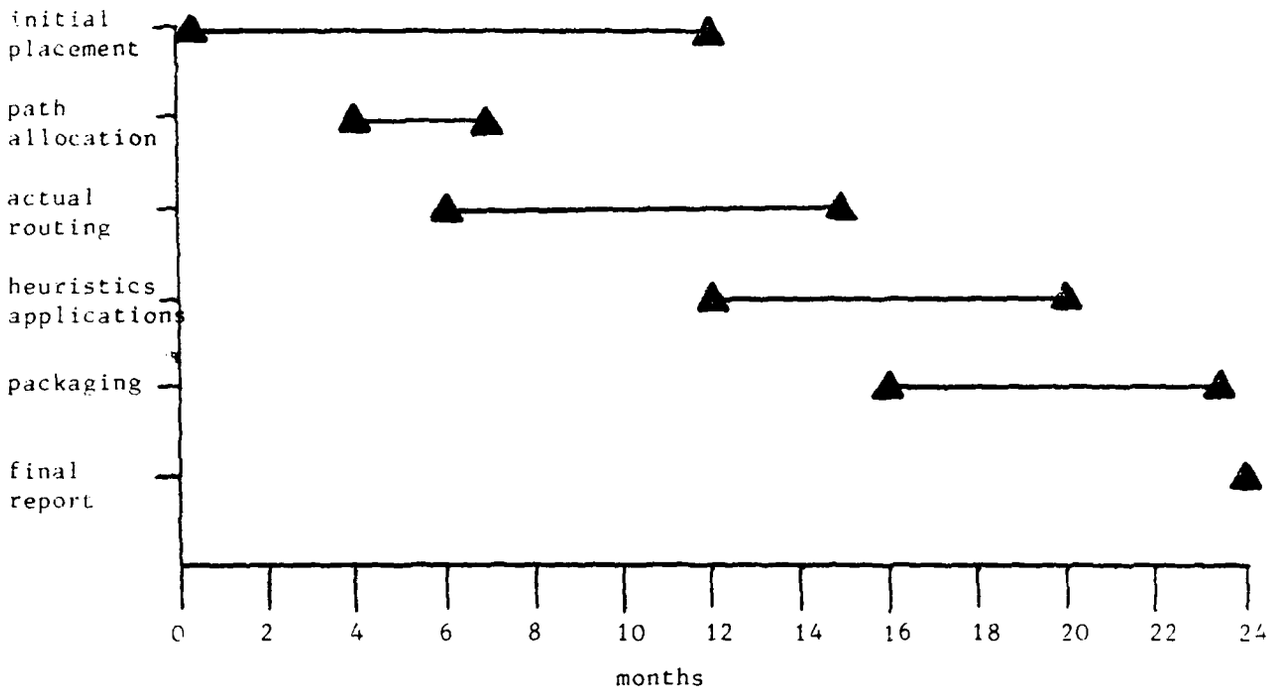
150 hours (not CPU time, bid rate at $150/hr)

Component Placement and Routing Algorithm

As circuit densities increase placement and routing algorithms become very important. They become important from a design efficiency and from a producibility standpoint. Current component placement and routing algorithms are either modified printed wiring board or modified integrated circuit algorithms. These are altered, albeit suboptimally, to consider such factors as maximum flywire lengths, edge connections, vias which do not traverse completely through the substrate, and other important physical characteristics of a hybrid. As routing algorithms operate more efficiently when used with a specific placement algorithm they should be developed simultaneously.

This candidate task will establish a routing algorithm, in tandem with a placement algorithm, which specifically addresses hybrid circuits. It must consider parameters such as those mentioned above as well as cross-overs, components that are designed into the circuit layers, and multi-layer hybrids. These algorithms must deliver a database which is complete and consistent enough to support automated manufacturing, inspection, and test equipment. These algorithms must also be compatible with several types of computer support systems.

FIGURE 27.
COMPONENT PLACEMENT AND ROUTING ALGORITHMS



Estimated Budget :

labor.....	$560,000 *
computer time..	140,000
travel.....	5,000
total cost.....	$565,000

* initial placement... 2 man years
path allocation..... 1/2 man year
actual routing..... 1 1/2 man years
heuristic applications ... 2 man years
packaging..... 2 man years

Physical Communications Interfaces

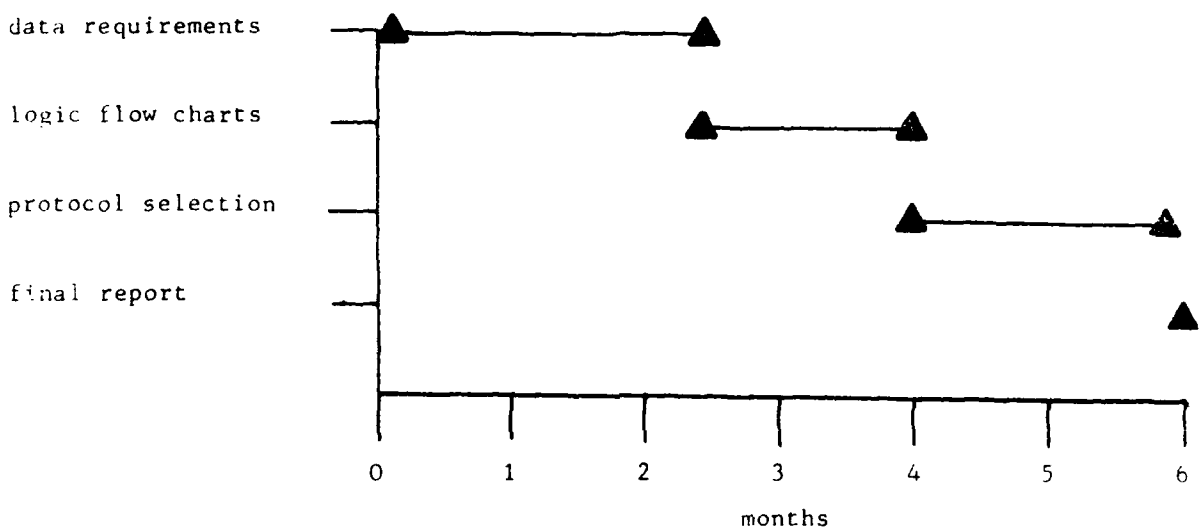
The purpose of this candidate task is to develop the specifications required for communications within an integrated manufacturing environment. This communication would occur between the digital engineering systems, the manufacturing information systems, and the specific computer aided manufacturing processes.

Several entities would be addressed. First, the data needs for each specific manufacturing operation must be defined (as per the database specification). Then these data needs must be melded into a generic logical flow of information. Protocol aspects must then be addressed. Protocol is the formal data transfer specifications (examples are RS232, RS449, IEEE488, BISYNC, X2.5, etc.). Parameters such as physical distance, serial or parallel transmission, noise and interference tradeoffs, the desired rate of data transmittal, error checking algorithms, and costs need to be defined.

The output from this project would be twofold. First, a generic logical information flow for computer aided hybrid manufacturing will be defined. Secondly, a suitable protocol will be established. This will ensure that future MAN TECH efforts are transportable and can be integrated into an automated factory in a timely and cost effective manner.

FIGURE 28.

PHYSICAL COMMUNICATION INTERFACES



Estimated Budget :

labor.....	$67,200
travel.....	2,800
total cost..	$70,000

Automatic Parts Identification

Automated substrate and module identification are important and necessary requirements if the high mix-low volume hybrid manufacturing facilities are to become significantly automated. The automation of the identification activity will accomplish several objectives. It will allow the automatic download of process control software to the specific manufacturing, inspection, or test work station. It will ensure a real time update of the associated MIS systems, such as production control and part history tracking. It will eliminate operator induced errors from manually entering identification data. It will serve as an integral subset of a closed loop, self checking automated material handling system.

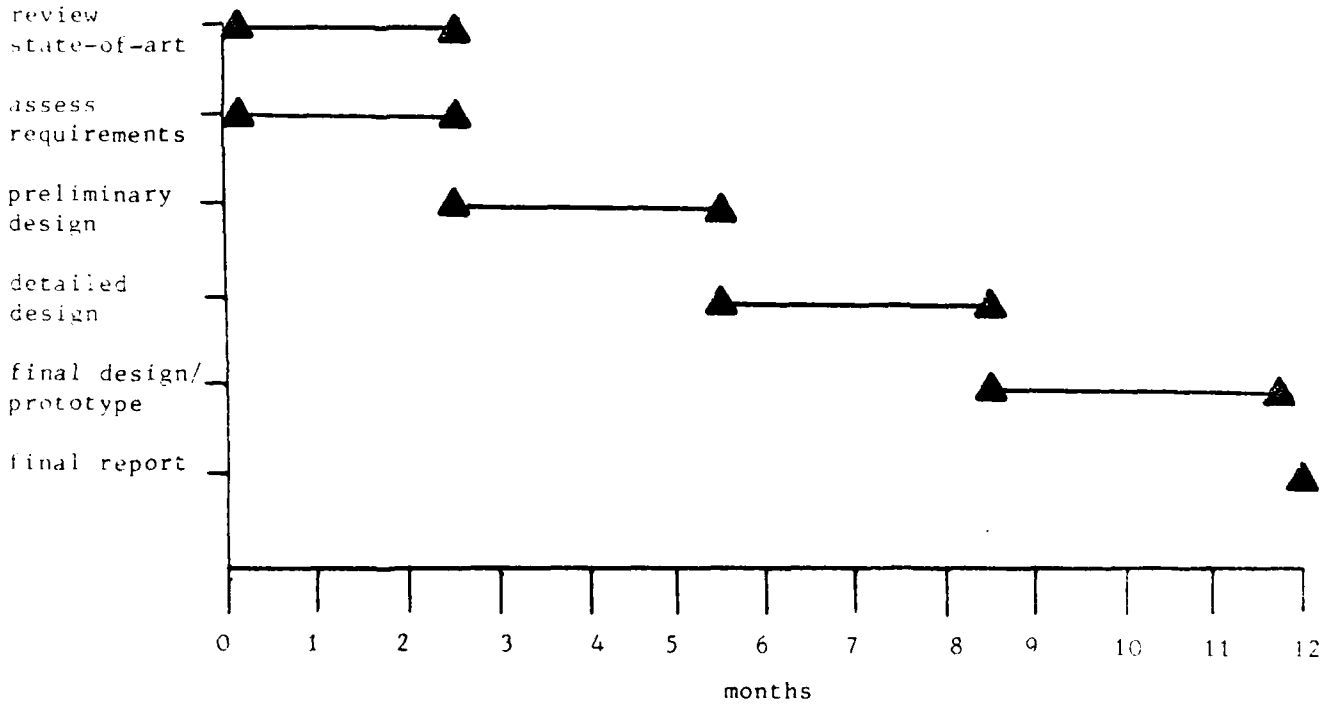
Characteristics of an automated parts identification system are to include :

- compatibility between substrate and module identification
- compatibility with the manufacturing processes for hybrids
- useable by work stations and material handling equipment
- versatile communications interface with host computing systems

The automation of parts identification is an important building block in support of an automated factory. It will reduce indirect labor costs, eliminate operator error, and can be used in monitoring and controlling an automated material handling system.

FIGURE 29.

AUTOMATIC PARTS IDENTIFICATION SYSTEM



Estimated Budget*:

labor.....	$140,000
travel.....	10,000
total cost..	$150,000

* prototype equipment costs not included

Automated Material Handling System

Automation of material handling activities in hybrid circuit manufacturing is one of the major milestones in achieving an automated factory. An undertaking in this area should be an integrated, multi-facted effort. Specific activities to be addressed are :

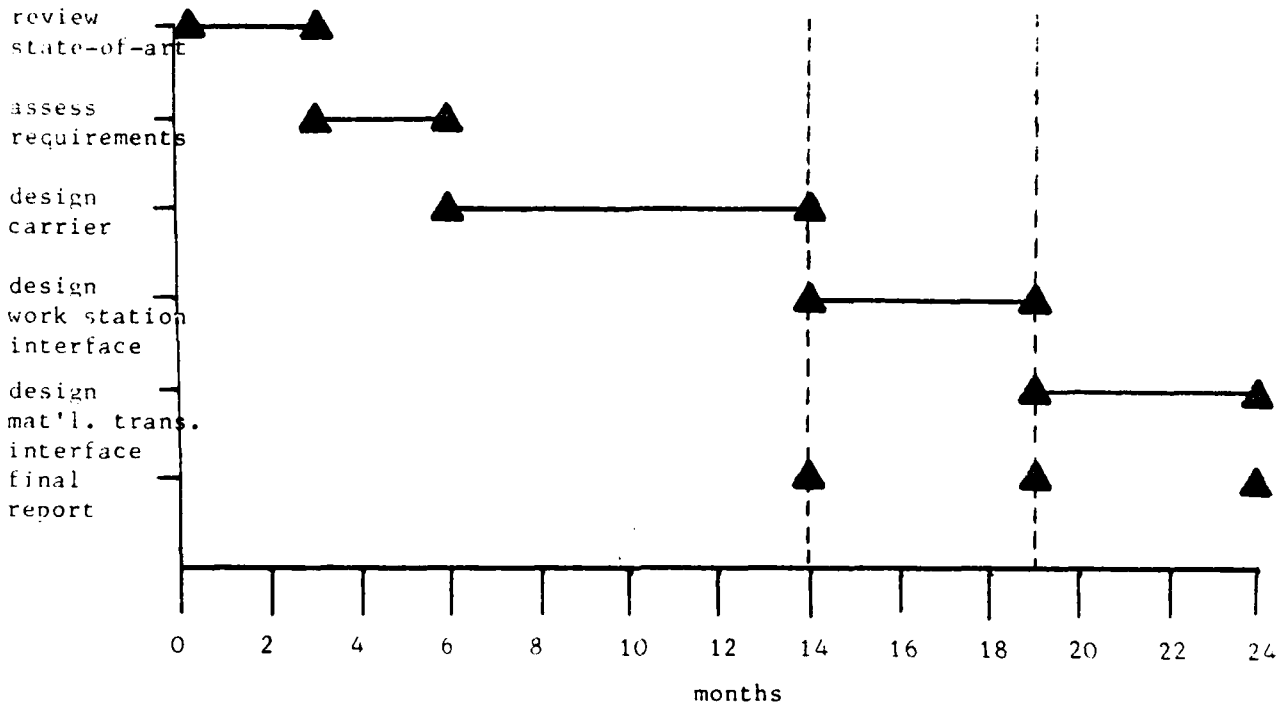
- material handling between work stations
- material handling between work station and the material handler
- material handling at each specific work station

The first milestone will be to develop a substrate/module carrier system. This system must offer protection to work-in-process items, must be compatible with all work stations, must be impervious to damage from the hybrid manufacturing processes, and must interface with the automatic parts identification systems.

Once the carrier system has been designed a two-pronged effort can be undertaken to integrate the carrier system with an automated transfer system for movement between work stations and to integrate the carrier with material handling requirements at each specific work station. This integration effort will ensure the transportability of the automated material handling system. Future MAN TECH equipment advancements would be designed around the use of the carrier system.

FIGURE 30.

AUTOMATED MATERIAL HANDLING SYSTEM



Estimated Budget*:

labor	$168,000
travel	4,000
phase 1 cost	$172,000
labor	$44,800
travel	1,200
phase 2 cost	$46,000
labor	$56,000
travel	2,000
phase 3 cost	$58,000
total project cost	$276,000

*prototype equipment not included

Automated Substrate Inspection

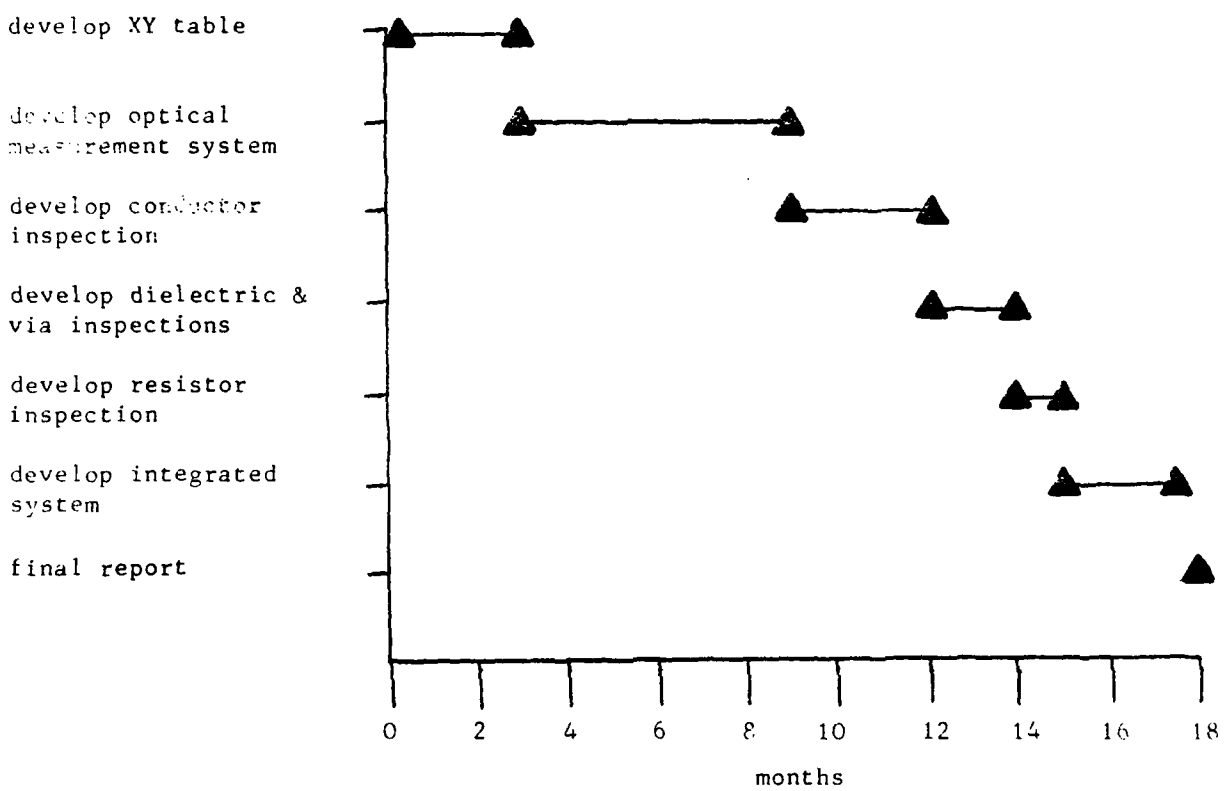
The current practice of manually inspecting the substrates for hybrids is very operator dependent for success. The operator must track the substrate movement, and make a subjective judgement as to pass/fail conditions. As circuit densities increase and multi-layer hybrids become more common this manual process will not adequately perform its task.

This candidate task would automate this process. The substrate would be mounted on an XY table which is programmable. As the substrate is cycled through an automatic sequence of movements an optical measurement system would compare the actual topography with the topography of a digitized database. This comparison would result in a pass or fail decision which would be printed out with the XY coordinate of the discrepant area.

This project would increase the uniformity and consistency of the substrate inspection process. Automation would also decrease the time spent undergoing an inspection. The equipment should be made compatible with future automation projects which address the screen printing process.

FIGURE 31.

AUTOMATIC SUBSTRATE INSPECTION



Estimated Budget*:

labor.....	$210,000
travel.....	5,000
total cost..	$215,000

*prototype equipment costs are not included

Microbridge Production Technology

The traditional bonding of gold wire or ribbon via thermocompression or ulrasonic techniques does not compliment the fine line spacings offered by the use of thin film fabrication technologies. This type of interconnection technology does not adequately support the advent of very high speed hybrid circuits.

The purpose of this future MAN TECH project is to develop and demonstrate the microbridge technology applications as an interconnection technique on thin film substrates in a mass production environment. (reference to the unbudgeted Navy project DNA-006XX) Microbridges are thin film plated crossovers. They may be fabricated as below:

]) create the interconnection bridge structure

2) plate the bridge structure with a conductive material

3) remove the bridge structure, leaving the conductor bridge

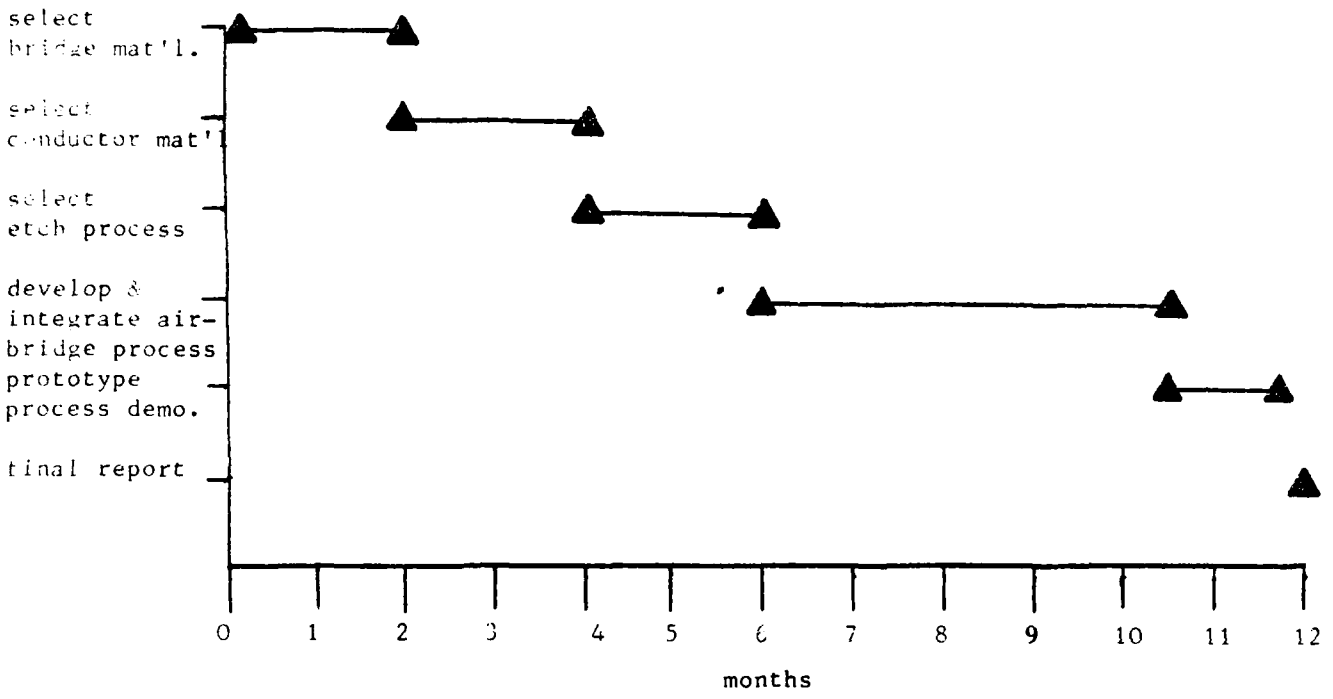
This process will be more complex to control but will utilize the equipment available for additive thin film processing.

The additional costs and complexities of microbridge technologies are outweighed by the advantages it offers. These include:

- batch processing as opposed to bonding one wire at a time
- the process will result in very uniform interconnections
- the interconnection fabrication will be more consistent
- total costs will be reduced
- enable the interconnection of very fine thin film lines
- provides better and more controllable interconnection techniques to support very high speed hybrids

FIGURE 32.

MICROBRIDGE PRODUCTION TECHNOLOGY



Estimated Budget*:

labor.....	$140,000
travel.....	3,000
materials...	25,000
total cost..	$168,000

*prototype equipment costs are not included

Thick Film Ink Characterization for IR Furnaces

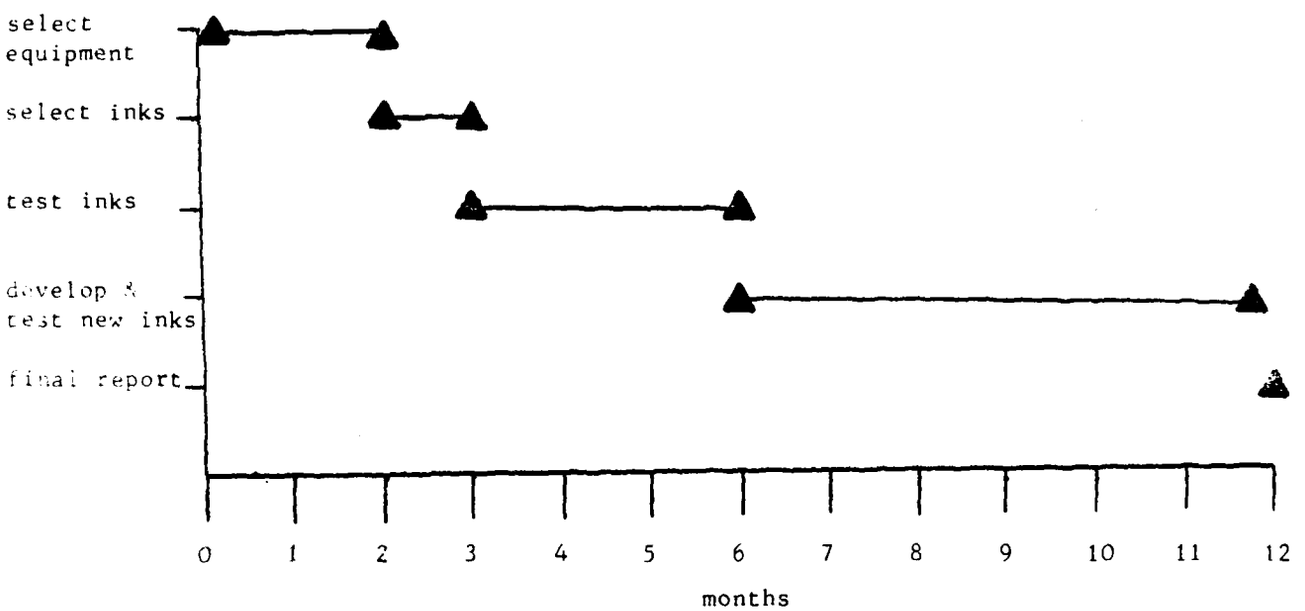
The purpose of this candidate task is to analyze, characterize, and, if necessary, develop thick film inks to be used in conjunction with IR furnaces. The development of thick film inks which are compatible with the IR firing environment will result in a production process which has:

- a faster throughput rate
- lower equipment costs
- reduced floor space requirements
- reduced power consumptions

Thick film inks from various manufacturers will be screened at different levels of thicknesses and then subjected to a 1,000 hour test. The results will then be tabulated and analyzed. The strengths and weaknesses of currently available inks will be assessed. Compatible inks and their applications will be presented. The development of thick film inks, or recommendations for ink improvements,will be conducted as required.

FIGURE 33.

THICK FILM INK CHARACTERISTICS



Estimated Budget :

labor.....	$140,000
materials...	60,000
travel.....	4,000
total costs.	$204,000

Semi-Automatic Die Probe System for Prescreening Tests

The final cost of a hybrid circuit is greatly influenced by the manufacturing expenses incurred in producing it. Rework caused by the failure of inadequately pre-tested die can be a major cost contributing factor. The purpose of this future MAN TECH project is to develop a semi-automated probe test system for prescreening die.

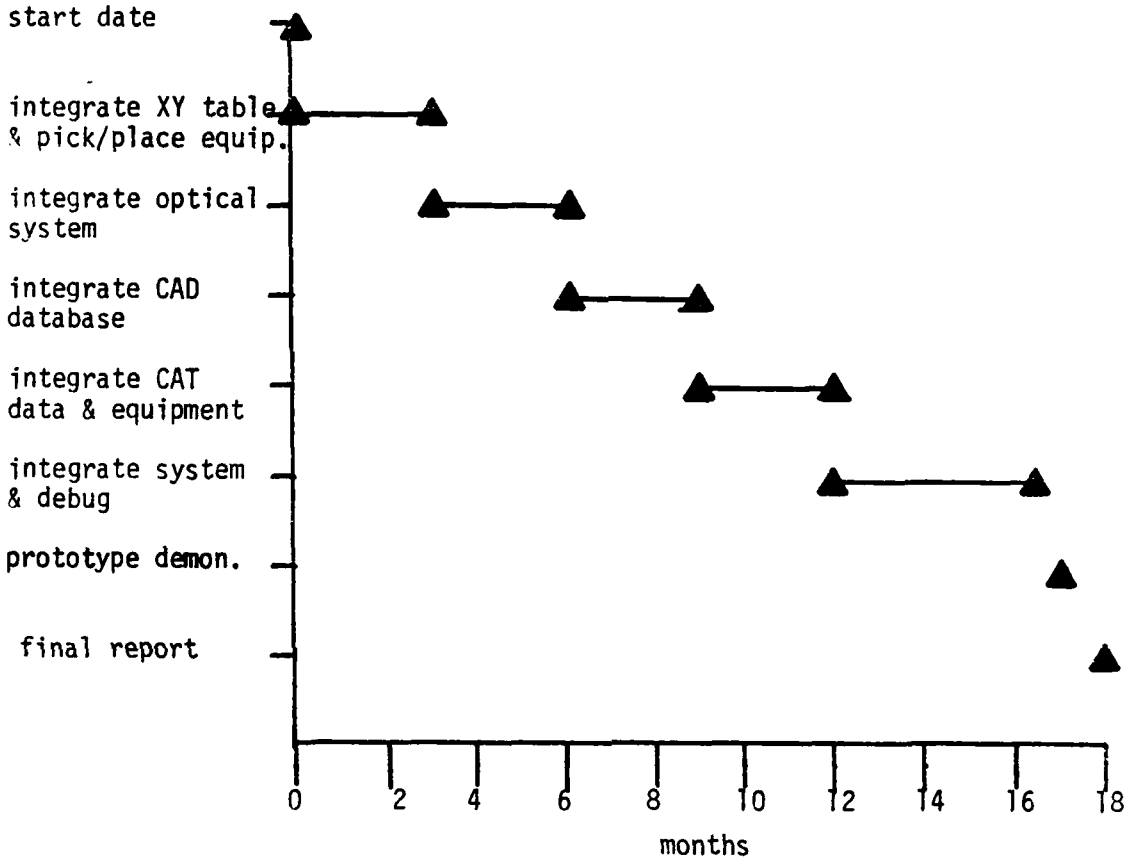
This system would incorporate several modifications to a manual probe test station. These modifications include:

- automatic pick and place mechanisms
- automatic XY table system
- optical alignment system
- CAD database interfaces
- CAT database interfaces
- test equipment and data recording equipment integration

This automated system would test die directly from waffle packs. As such this system would have maximum transportability among manufacturers. The ability to prescreen die via probing at elevated temperatures will insure the maximum benefits from automating the assembly processes for hybrid microelectronics.

FIGURE 34.

SEMI-AUTOMATIC PROBE TEST SYSTEM



Estimated Budget :

labor.....	$212,000
travel.....	3,000
material....	30,000
total cost..	$245,000

Automated Camera and Test Probe Configuration

Existing fault isolation methods typically involve manual probing of the assembled substrate. The very delicate nature of the assembled substrate, especially when chip and wire technology is used, and the small area available for probing make this process slow and expose the substrate to increased chances of damage.

The output of this project would be an automated probe integrated with a video camera machine. This machine would be driven with information from several sources which are:

- the results of prior functional tests
- specific fault isolation programs
- geometric information derived from the engineering database

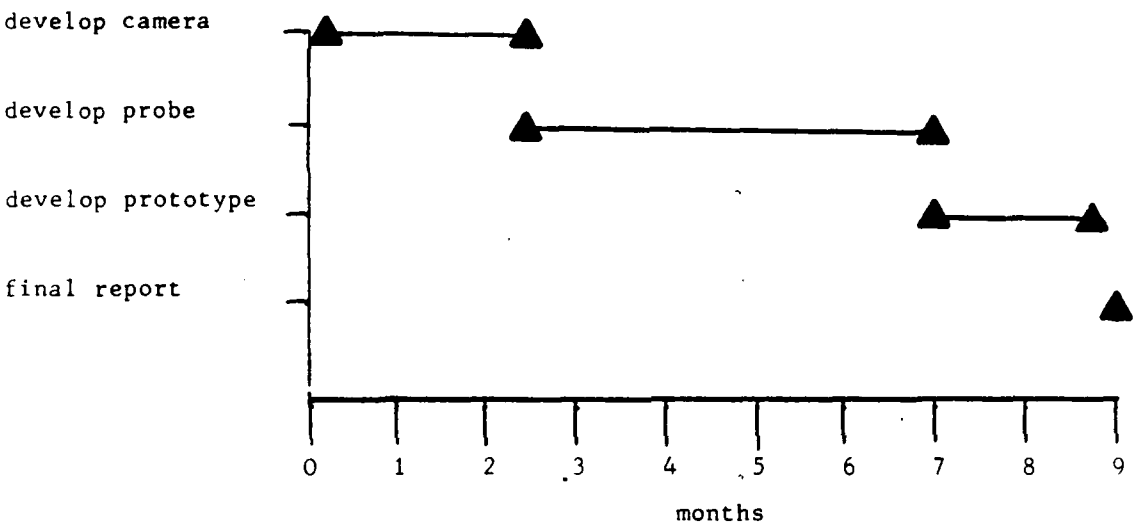
The camera would guide the probe and view the probed areas for evidence of physical discrepancies.

The camera and probe would be mobile as opposed to moving the substrate. This is required by the electrical needs of high speed or electrically sensitive circuits.

This project would address the mechanical requirements and the software integration aspects to support the mechanics rather than the specific fault isolation software needed.

FIGURE 35.

AUTOMATIC CAMERA AND TEST PROBE SYSTEM



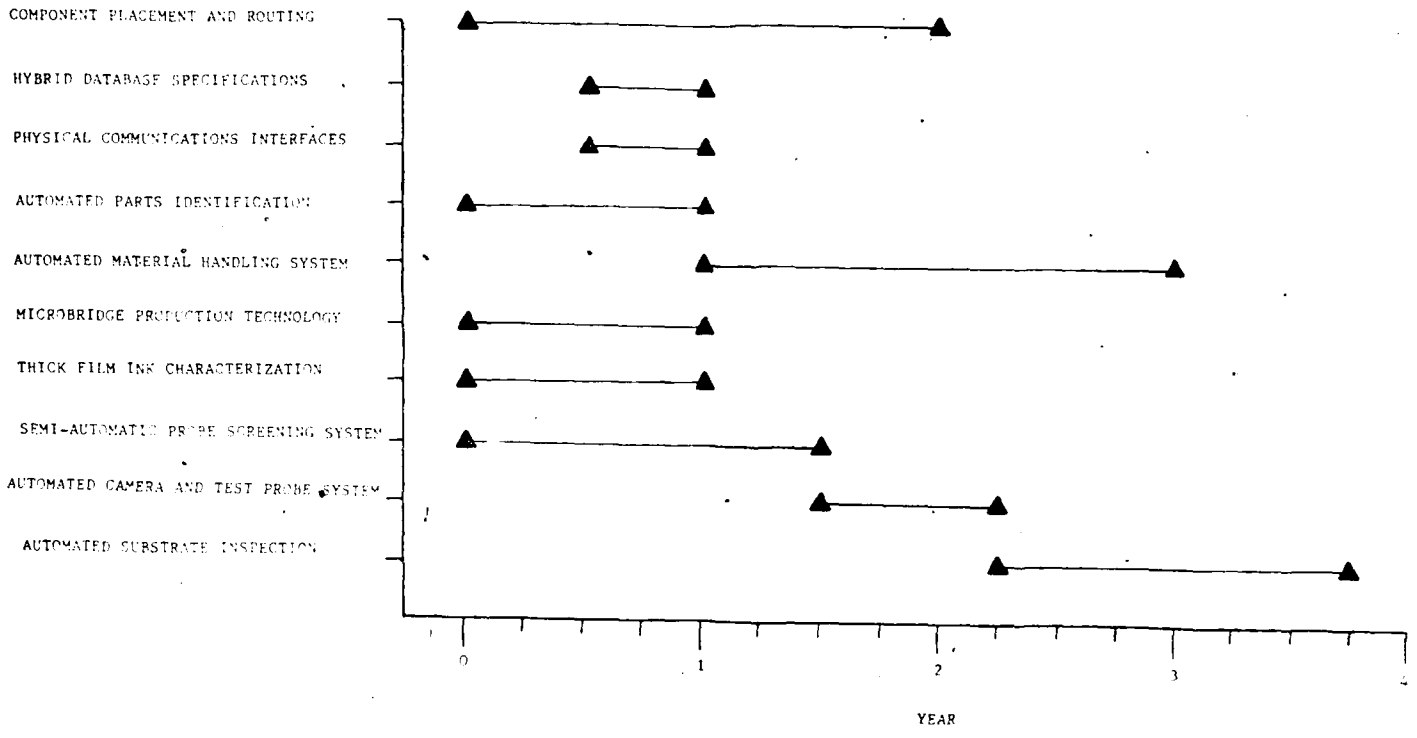
Estimated Budget*:

labor.....	$100,800
travel.....	2,200
materials...	2,000
total cost..	$105,000

*prototype equipment costs are not included

FIGURE 36.

COMPILED SCHEDULES



APPENDIX A
HICADAM ARCHITECTURE

A HICADAM System architecture is proposed. This architecture reflects those generic functions, inputs, outputs, mechanisms, and controls utilized in the design and manufacture of hybrid circuits. The interfaces of a CAD/CAM system and an MIS system are reflected on the node tree diagram.

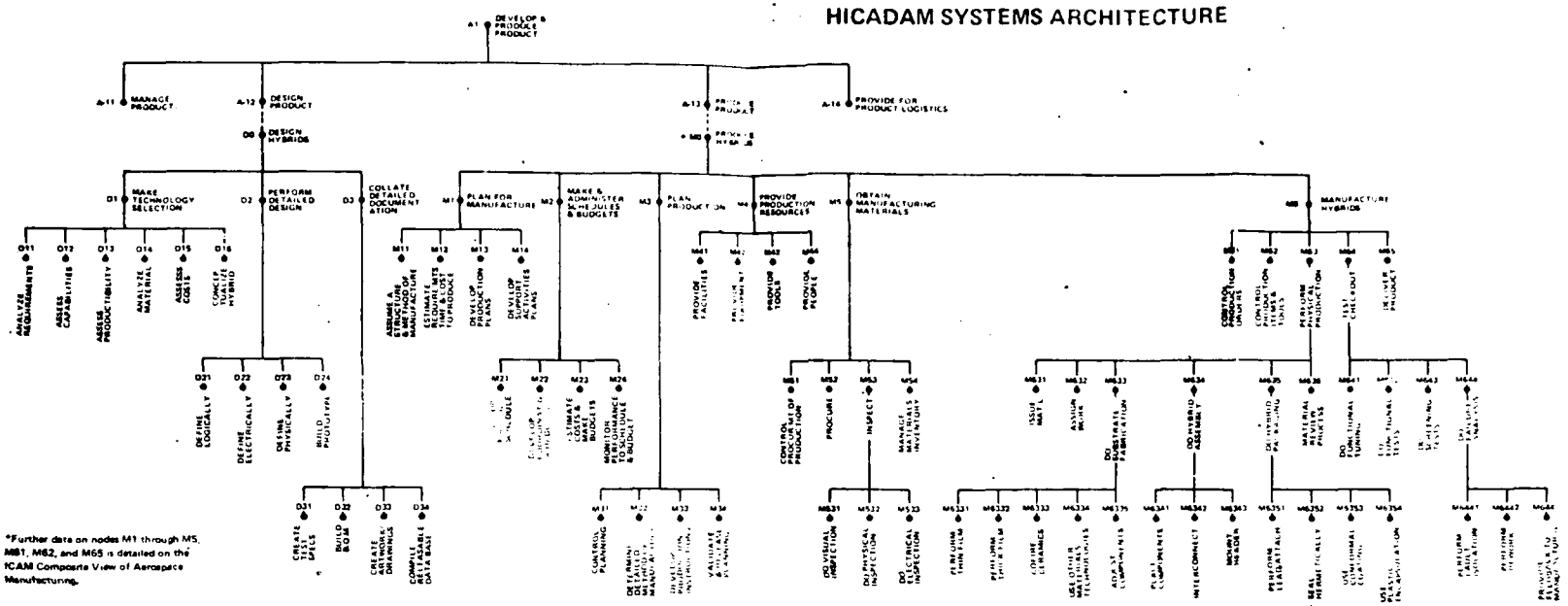
Hybrid design and manufacturing processes and interfaces are highlighted. The processes as depicted were presented to and critiqued by other operating divisions of Hughes Aircraft and by the Hybrid Commodity Group in support of the ECAM MAN TECH. (ECAM is Electronics Computer Aided Manufacturing and is being conducted by Battelle Labs.) The ICAM $IDEF_0$ modeling methodology was utilized in drafting the architecture.

The design activity has been decomposed into three generic activities. These activities are technology selection, detailed design, and detailed documentation.

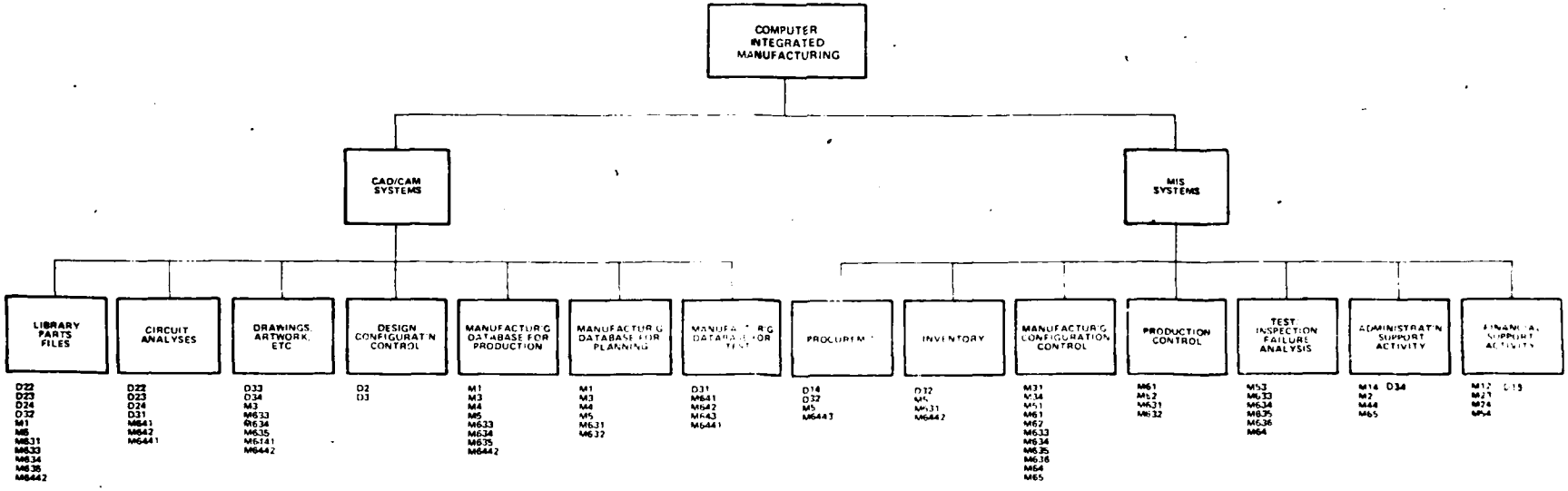
Procurement of the necessary production resources is briefly illustrated. A detailed analysis of these areas is available in the ICAM Composite View of Aerospace Manufacturing.

The manufacturing function has been decomposed into six basic areas. These activities reflect the interfaces of quality, test, and the various production technologies (such as thin film, thick film,..., placement, packaging, etc.). Specific illustrations of process flows are given in the main body of this report.

HICADAM SYSTEMS ARCHITECTURE

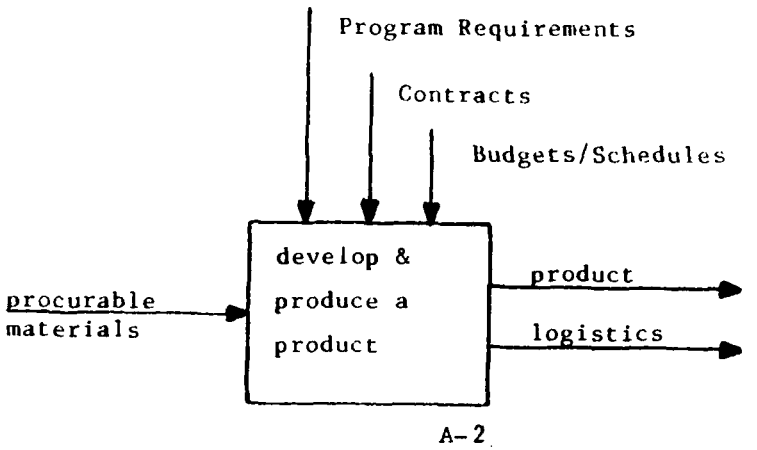


*Further data on nodes M1 through M5, M61, M62, and M65 is detailed on the ICAM Composite View of Aerospace Manufacturing.



(3)

USED AT	AUTHOR: Keller, Dean A.	DATE: 8-24-81			READER	DATE	CONTEXT:
	PROJECT: ICAM Architecture	REV	X	WORKING			
				DRAFT			
	NOTES: 1 2 3 4 5 6 7 8 9 10			RECOMMENDED			
				PUBLICATION			



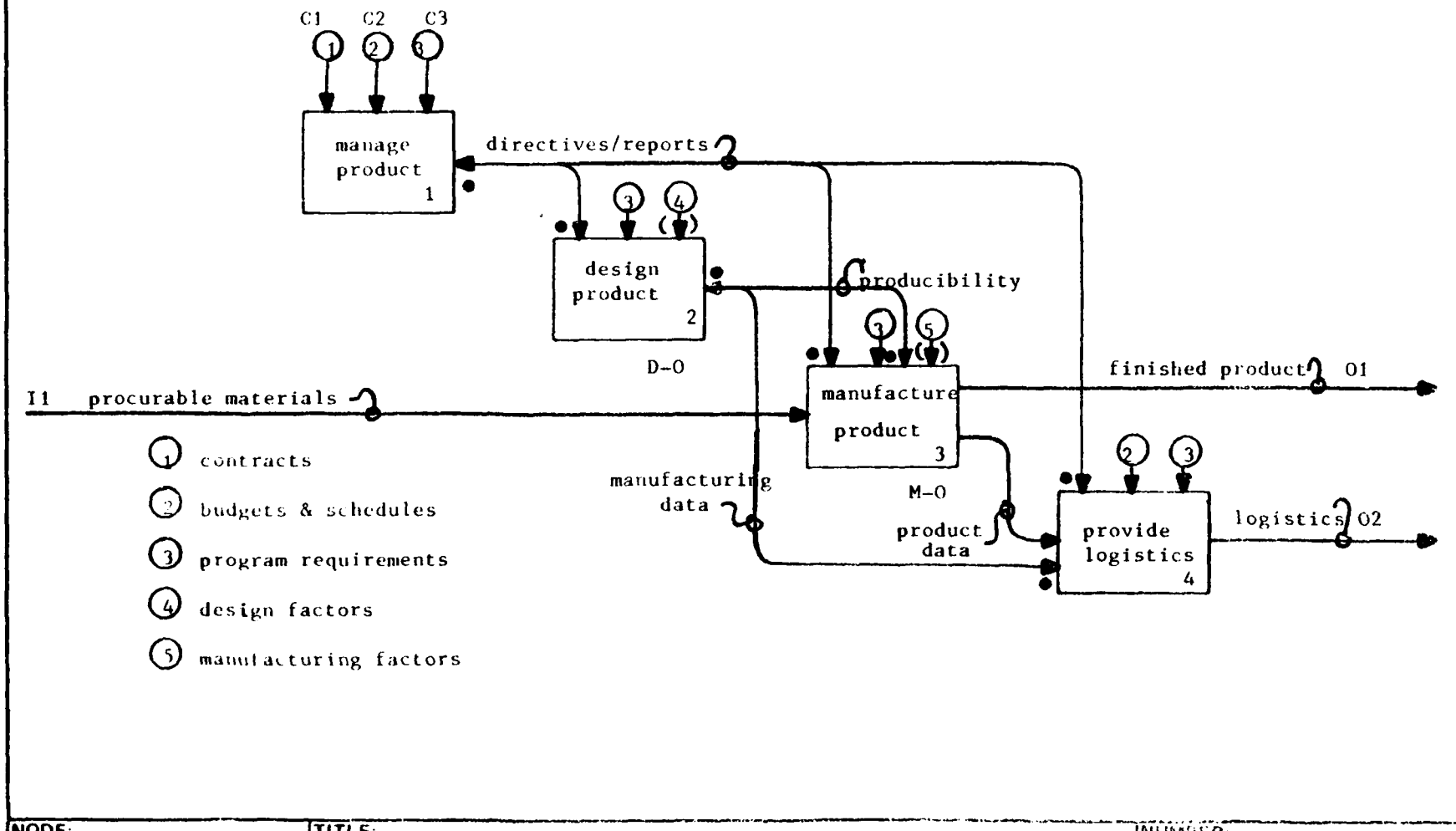
PURPOSE : To reflect a global interface of the decision to manufacture a product and the decision to use hybrid microelectronics in that product.

VIEWPOINT : Production Systems Analyst

CAD/CAM Systems Analyst

NODE:	TITLE:	NUMBER:
A-2	DEVELOP & PRODUCE A PRODUCT	A1

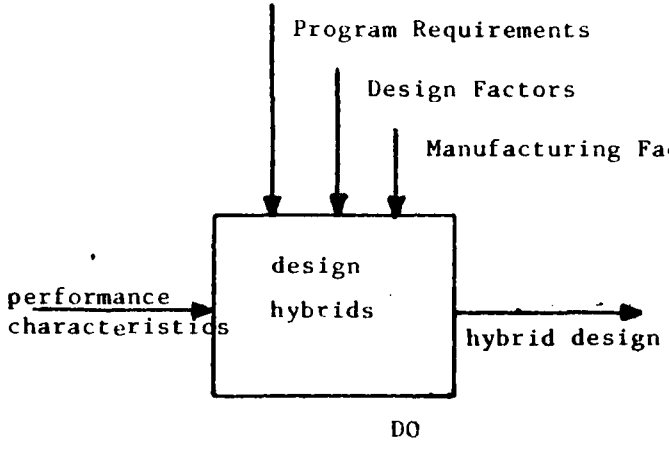
USED AT	AUTHOR	Keller, Dean A.	DATE	8-24-81	X	WORKING	READER	DATE	CONTEXT:
A-2	PROJECT:	HICADAM Architecture	REV			DRAFT			
	NOTES: 1 2 3 4 5 6 7 8 9 10					RECOMMENDED			
						PUBLICATION			



NODE:	TITLE:	NUMBER:
A-1	DEVELOP & PRODUCE A PRODUCT	A2

D16-416 GS 6/79

USED AT	AUTHOR: Keller, Dean A.	DATE: 7-27-81	X	WORKING	READER	DATE	CONTEXT:
	PROJECT: HICADAM Architecture	REV:		DRAFT			
				RECOMMENDED			
	NOTES: 1 2 3 4 5 6 7 8 9 10			PUBLICATION			

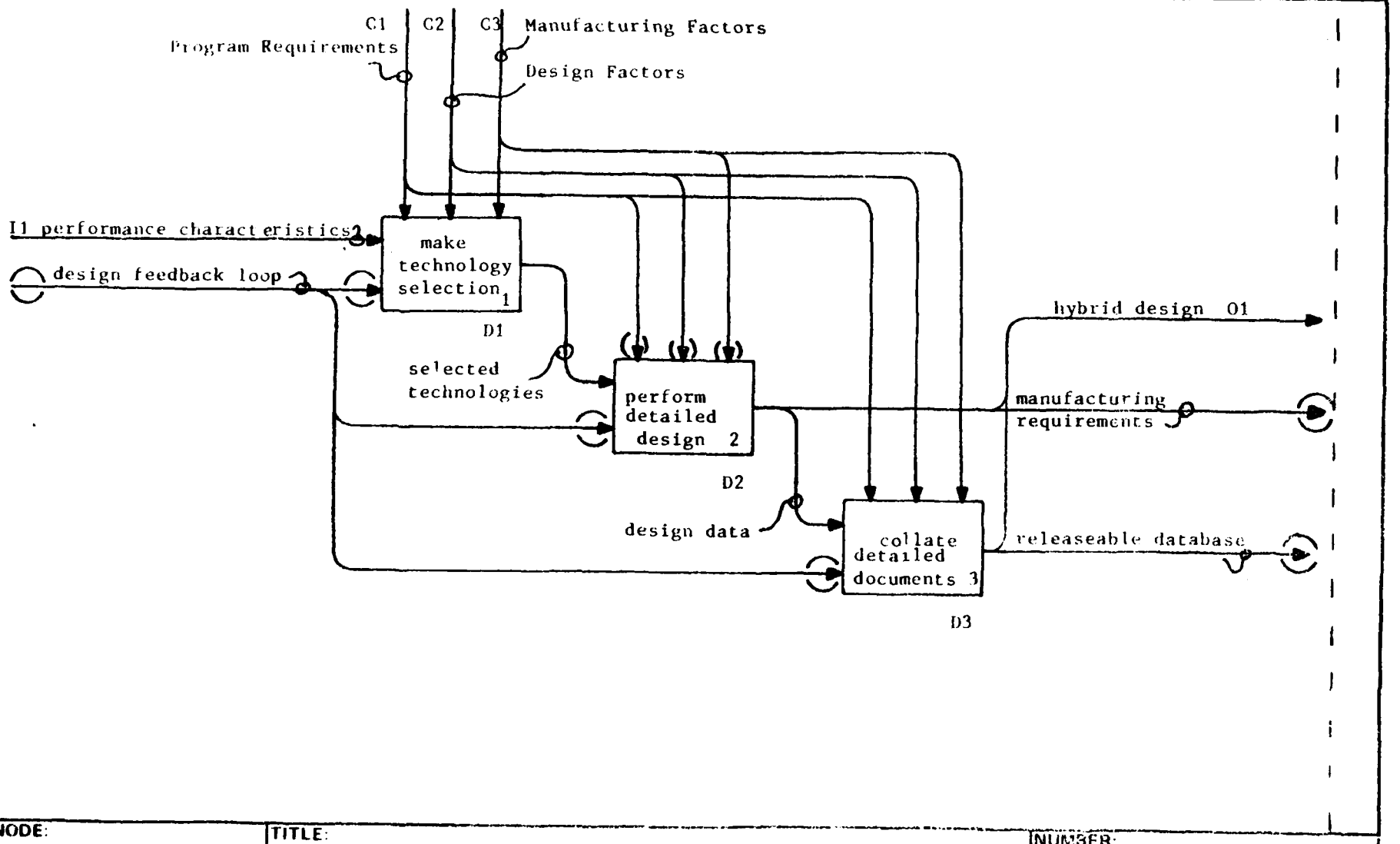


PURPOSE : To detail the functional relationships which occur in the design of hybrid microelectronics.

VIEWPOINT : Production Systems Analyst
CAD/CAM Systems Analyst

NODE:	TITLE:	NUMBER:
D-0	DESIGN HYBRIDS	A3

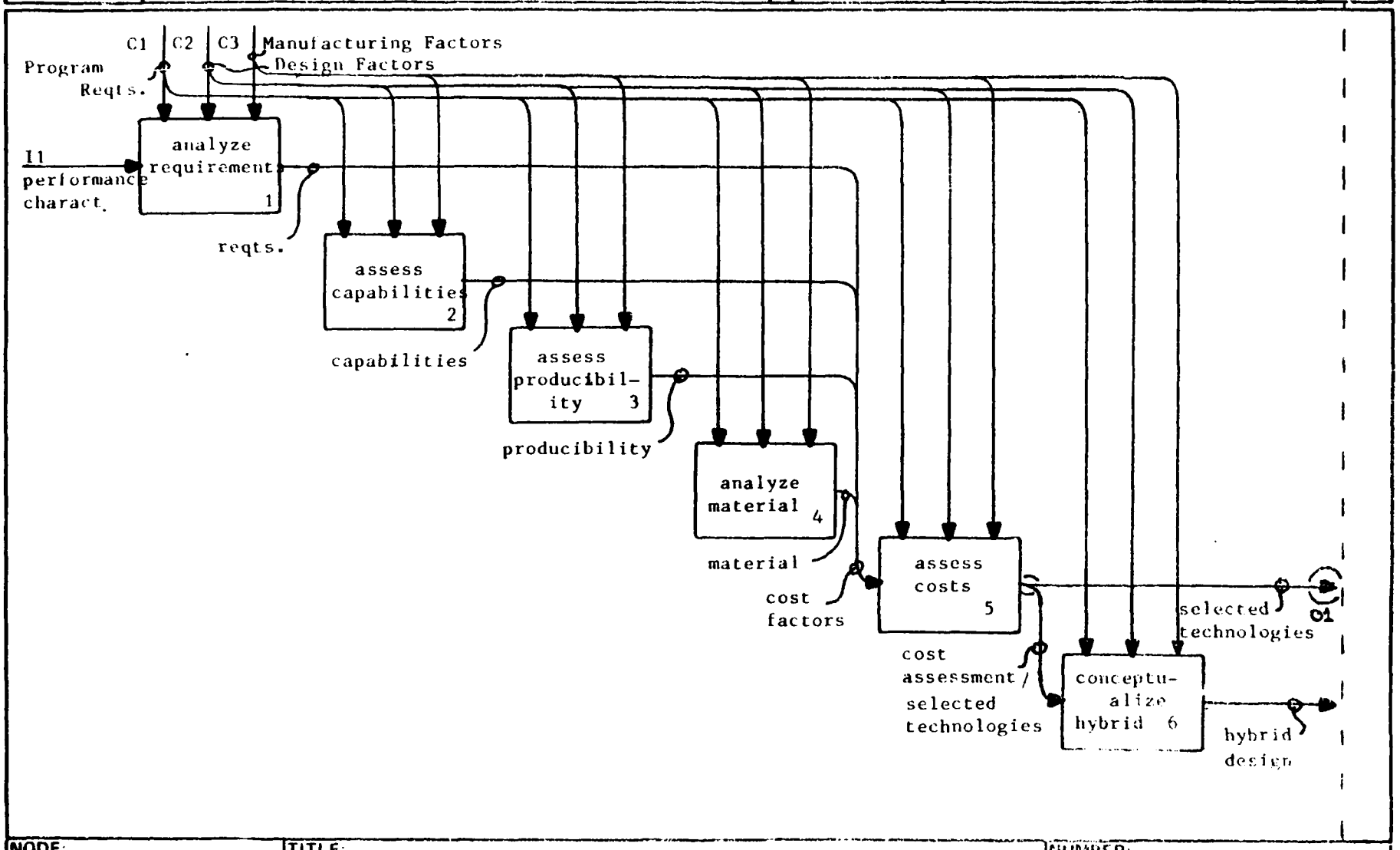
USED AT:	AUTHOR: Keller, Dean A.	DATE: 7-27-81	X	WORKING	READER	DATE	CONTEXT:
D-0	PROJECT: IICADAM Architecture	REV:		DRAFT			
	NOTES: 1 2 3 4 5 6 7 8 9 10			RECOMMENDED			
				PUBLICATION			



NODE:	TITLE:	NUMBER:
D0	DESIGN HYBRIDS	A4

D16-416 GS 6/79

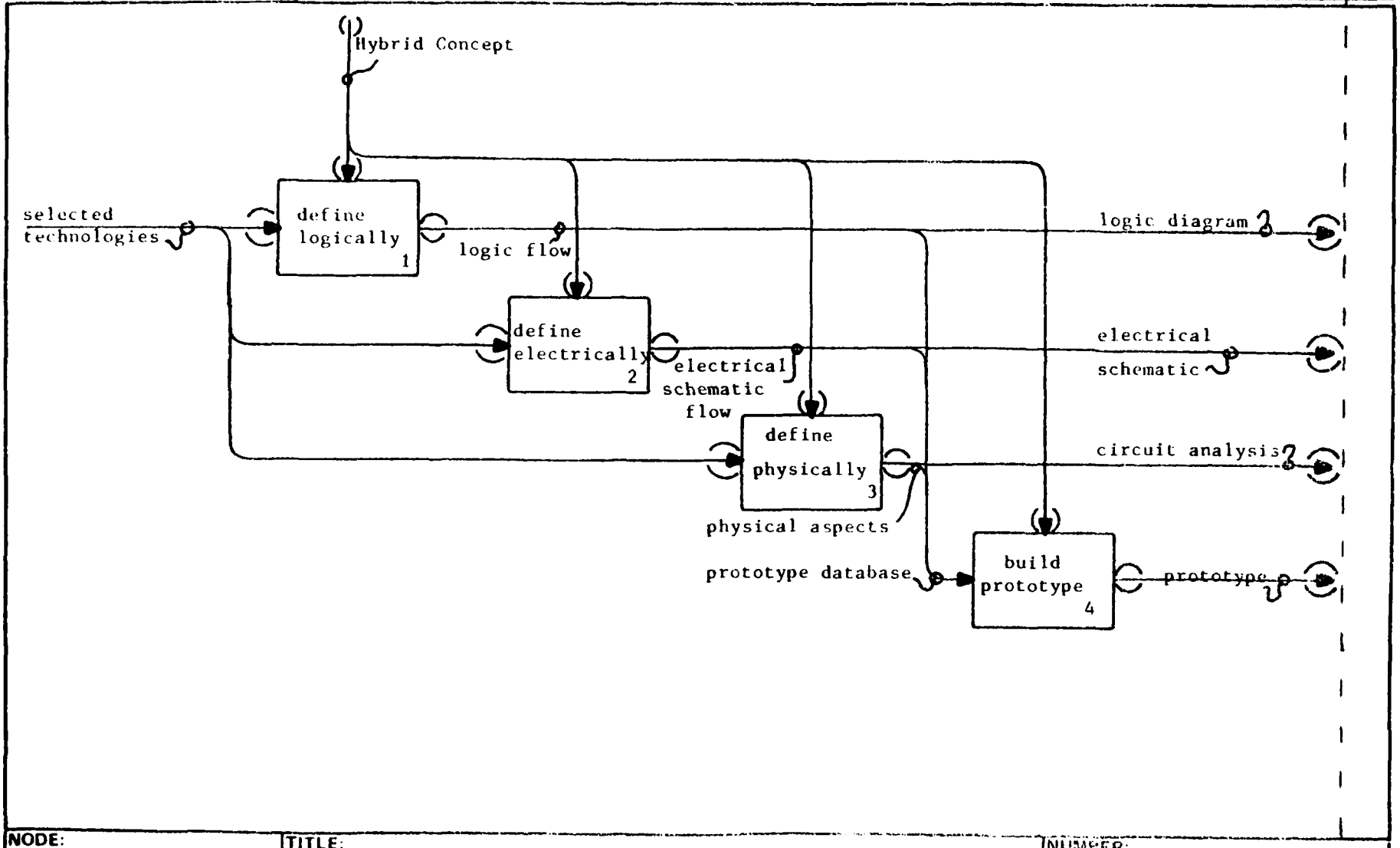
USED AT:	AUTHOR: Keller, Dean A.	DATE: 7-27-81	X	WORKING	READER	DATE	CONTEXT:
D0	PROJECT: IICAM&M Architecture	REV:		DRAFT			1 D0
	NOTES: 1 2 3 4 5 6 7 8 9 10			RECOMMENDED			
				PUBLICATION			



NODE:	TITLE:	NUMBER:
D1	MAKE TECHNOLOGY SELECTION	A5

D16-416 GS 6/79

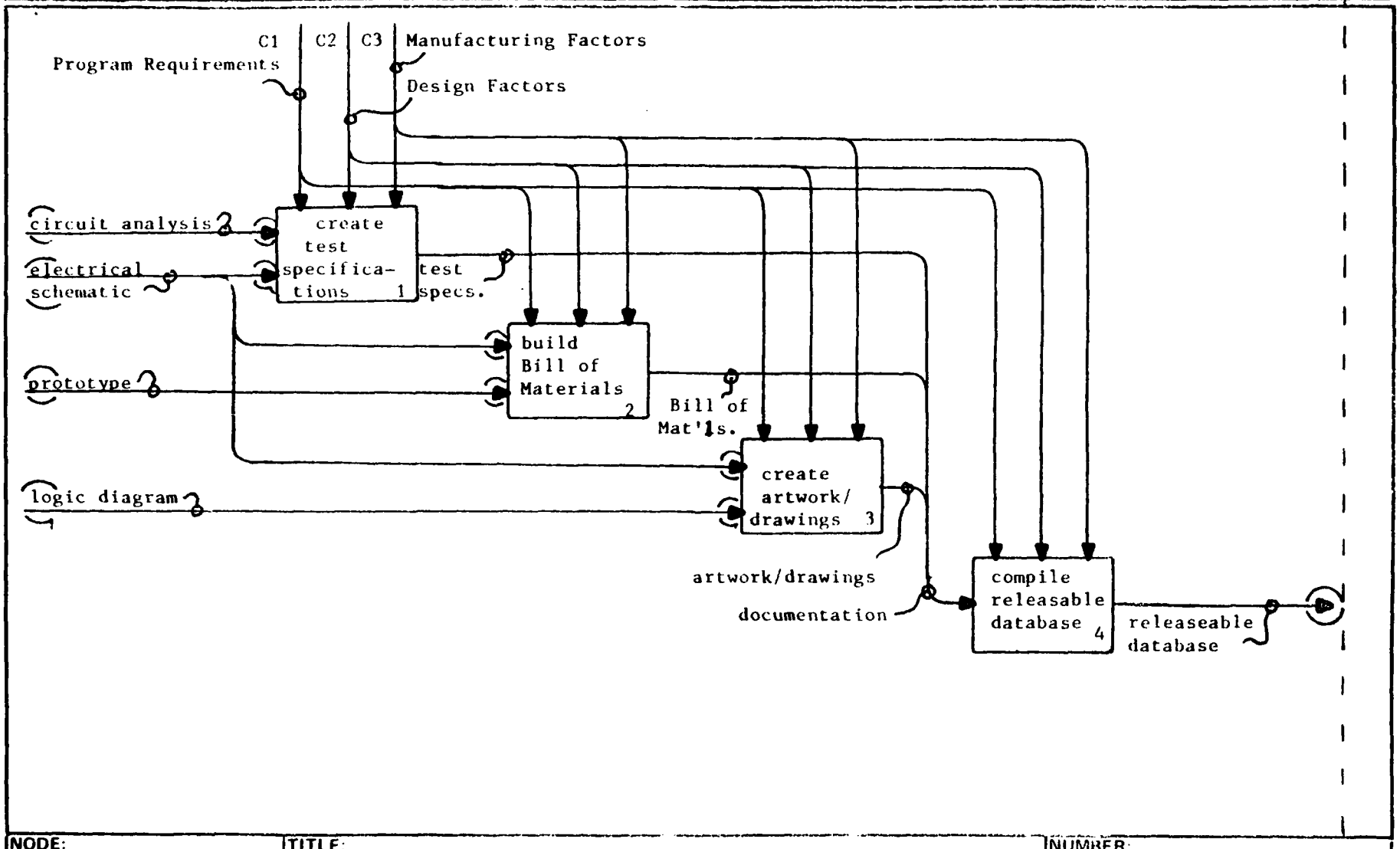
USED AT	AUTHOR: Keller, Dean A.	DATE: 7-27-81	X	WORKING	READER	DATE	CONTEXT:
D0	PROJECT: HICADAM Architecture	REV:		DRAFT			2
	NOTES: 1 2 3 4 5 6 7 8 9 10			RECOMMENDED			D0
				PUBLICATION			



NODE:	TITLE:	NUMBER:
D2	PERFORM DETAILED DESIGN	A6

D16-416 GS 6/79

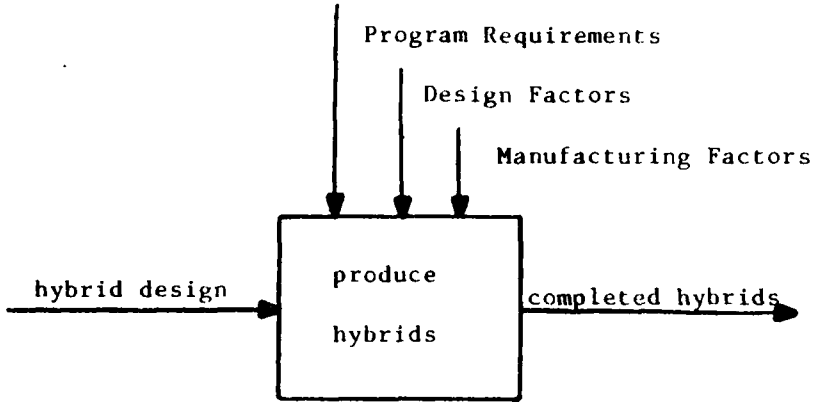
USED AT:	AUTHOR: Keller, Dean A.	DATE: 7-27-81			READER	DATE	CONTEXT:
D0	PROJECT: IICADAM Architecture	REV:	X	WORKING			D0 3
	NOTES: 1 2 3 4 5 6 7 8 9 10			DRAFT			
				RECOMMENDED			
				PUBLICATION			



NODE:	TITLE:	NUMBER:
D3	COLLATE DETAILED DOCUMENTATION	A7

D16-416 GS 6/79

USED AT:	AUTHOR: Keller, Dean A.	DATE: 8-24-81	X WORKING	READER	DATE	CONTEXT:
	PROJECT: ICAM Architecture	REV:	DRAFT			
			RECOMMENDED			
	NOTES: 1 2 3 4 5 6 7 8 9 10		PUBLICATION			



PURPOSE : To detail the functional relationships which occur in the manufacture of hybrid microelectronics.

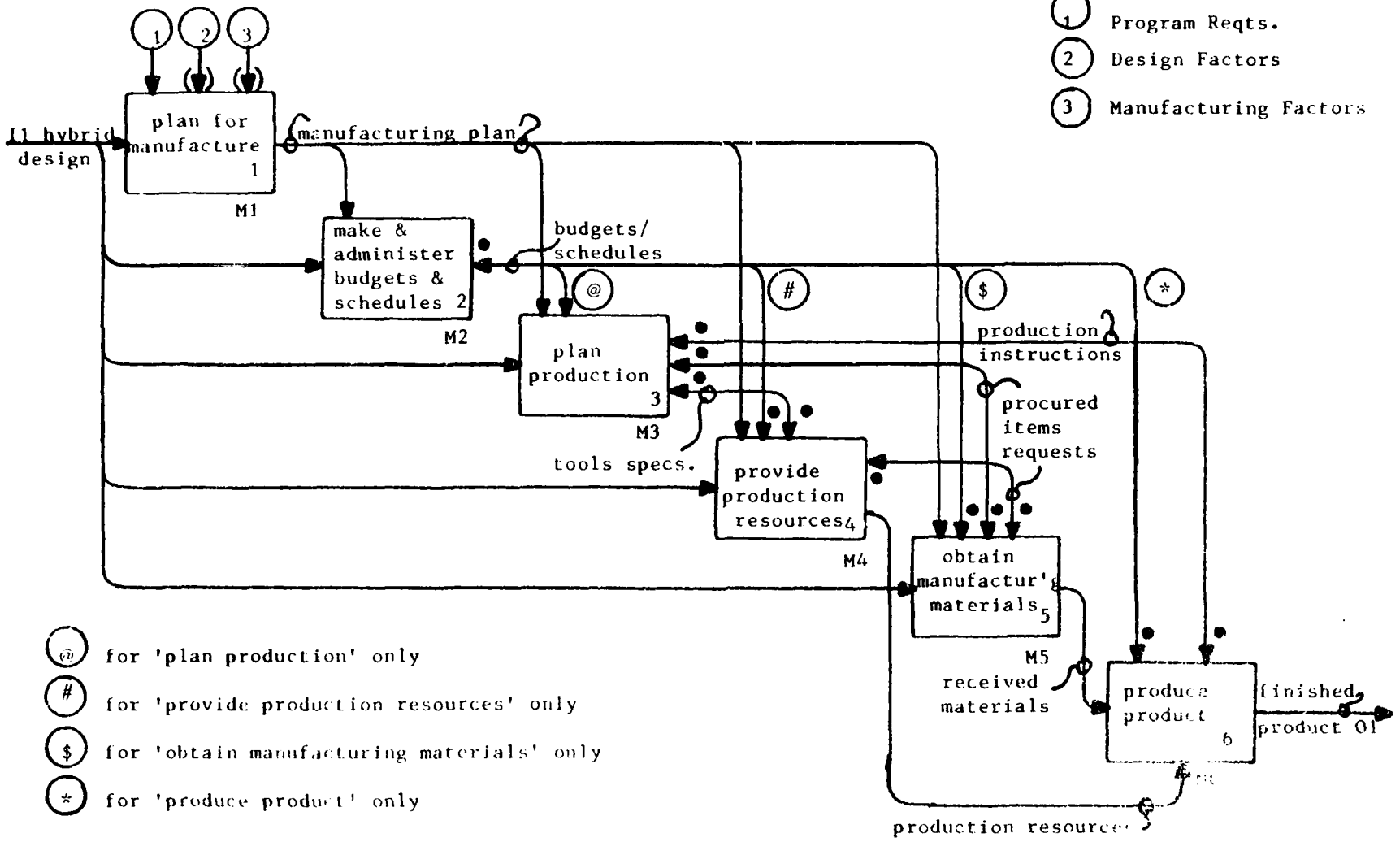
VIEWPOINT : Production Systems Analyst

CAD/CAM Systems Analyst

NODE:	TITLE:	NUMBER:
M-0	PRODUCE HYBRIDS	A8

D16-416 GS 6/79

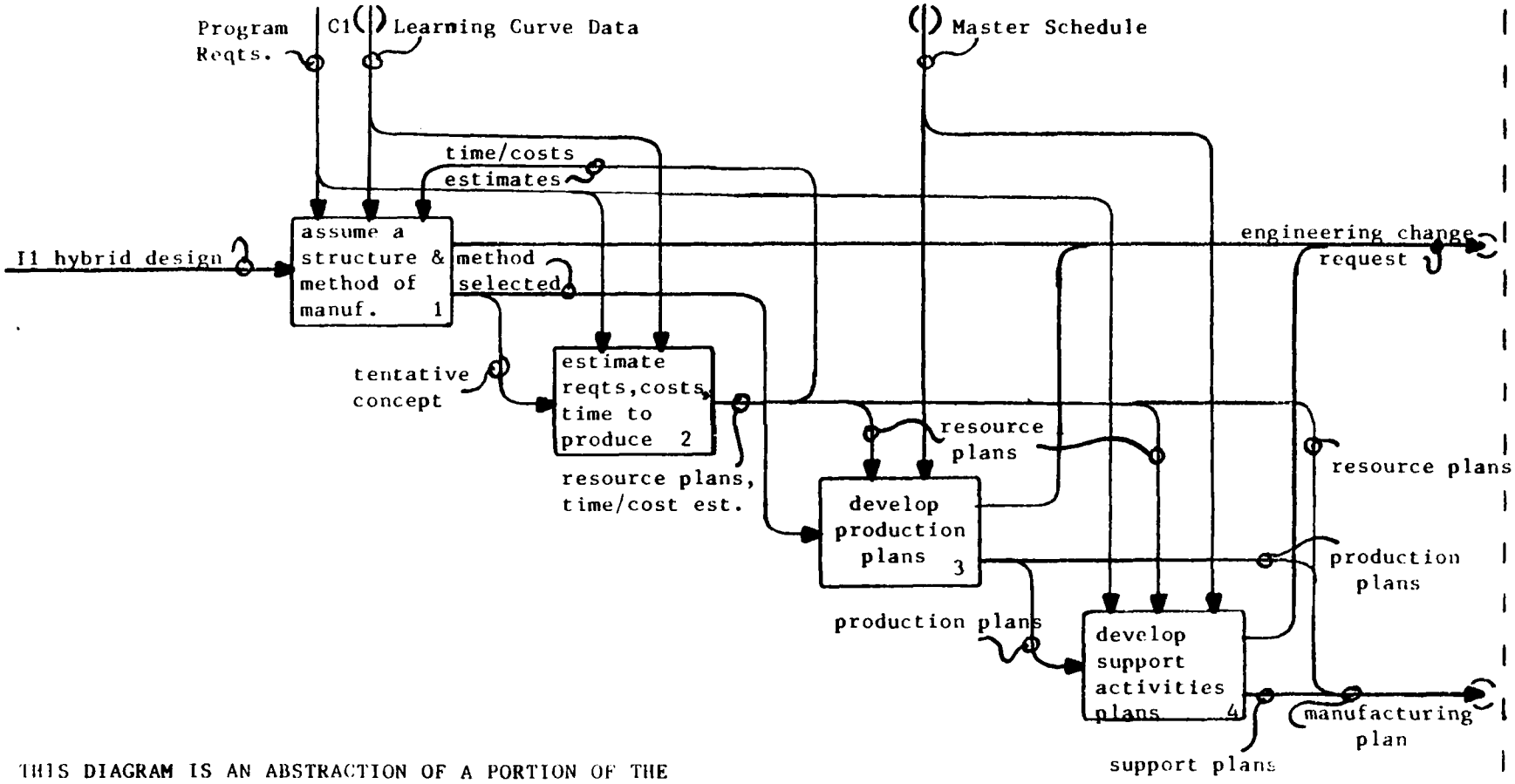
USED AT:	AUTHOR: Keller, Dean A.	DATE: 8-24-81	X WORKING	READER	DATE	CONTEXT:
M-0	PROJECT: HICADAM Architecture	REV:	DRAFT			
	NOTES: 1 2 3 4 5 6 7 8 9 10		RECOMMENDED			
			PUBLICATION			



NODE:	TITLE:	NUMBER:
M0	PRODUCE HYBRIDS	A9

DIG 416 QS 6/79

USED AT:	AUTHOR: Keller, Dean A.	DATE: 8-24-81		READER	DATE	CONTEXT:
MO	PROJECT: HICADAM Architecture	REV:	XX WORKING			1
			DRAFT			MO
	NOTES: 1 2 3 4 5 6 7 8 9 10		RECOMMENDED			
			PUBLICATION			

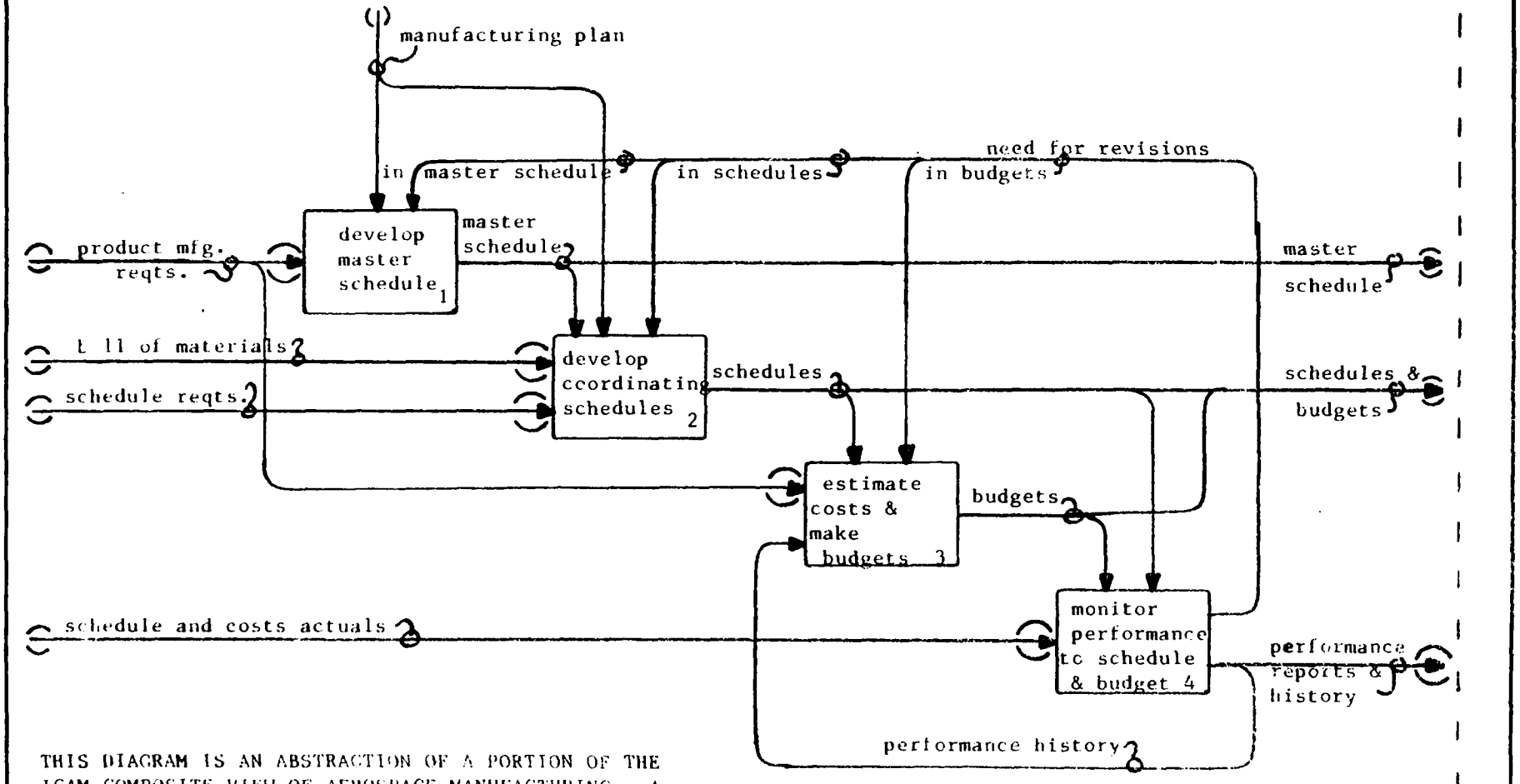


THIS DIAGRAM IS AN ABSTRACTION OF A PORTION OF THE ICAM COMPOSITE VIEW OF AEROSPACE MANUFACTURING. A DETAILED DECOMPOSITION OF THIS AREA IS INCLUDED IN THE ICAM CHART.

NODE:	TITLE:	NUMBER:
M1	PLAN FOR MANUFACTURE	A10

D16-416 GS 6/79

USED AT:	AUTHOR: Keller, Dean A.	DATE: 8-24-81	X	WORKING	READER	DATE	CONTEXT:
MC	PROJECT: HICADAM Architecture	REV:		DRAFT			2
	NOTES: 1 2 3 4 5 6 7 8 9 10			RECOMMENDED			MO
				PUBLICATION			

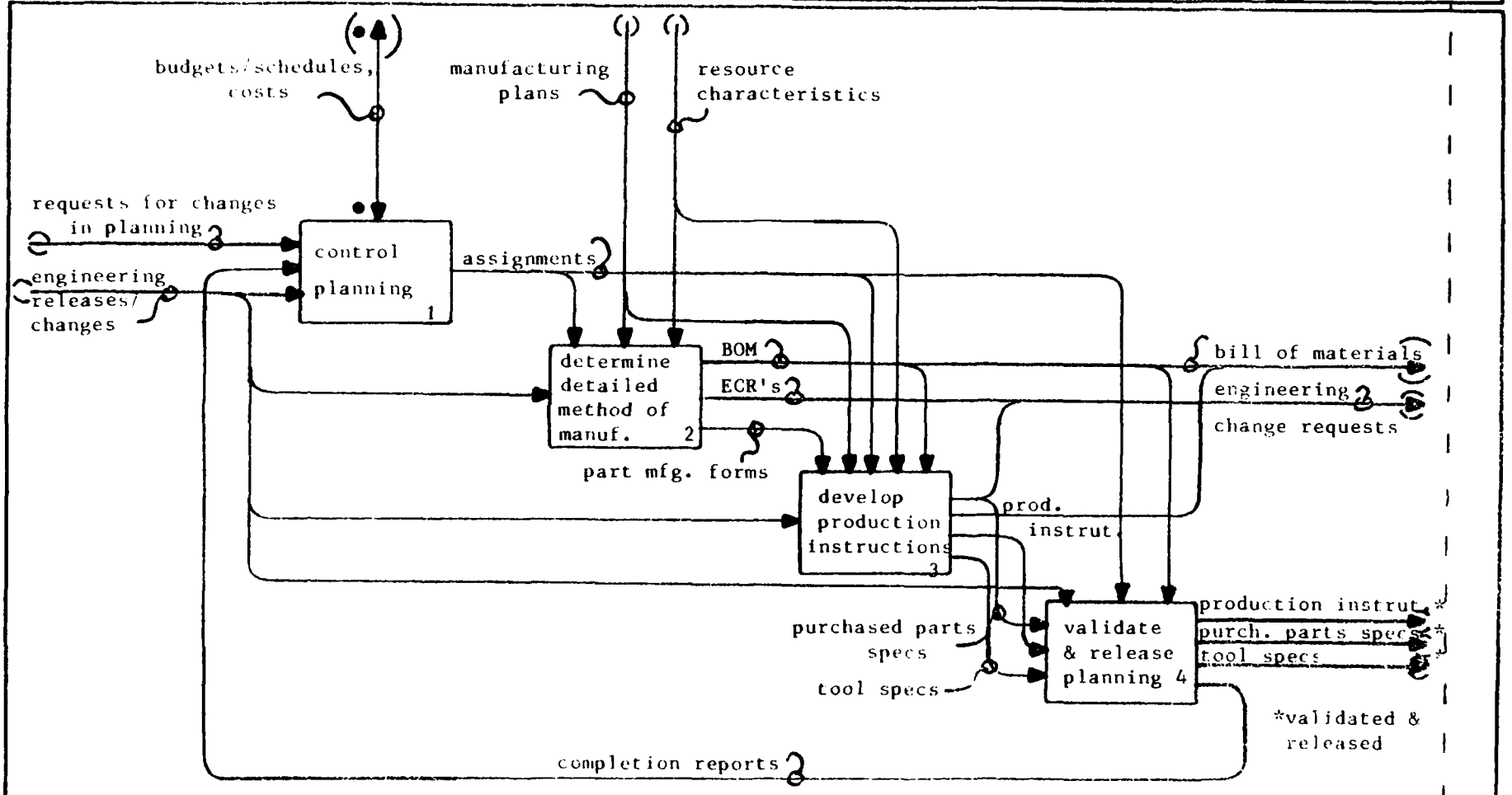


THIS DIAGRAM IS AN ABSTRACTION OF A PORTION OF THE ICAM COMPOSITE VIEW OF AEROSPACE MANUFACTURING. A DETAILED DECOMPOSITION OF THIS AREA IS INCLUDED IN THE ICAM CHART.

NODE:	TITLE:	NUMBER:
M2	MAKE & ADMINISTER SCHEDULES & BUDGETS	A11

D16 416 GS 6/79

USED AT:	AUTHOR: Keller, Dean A.	DATE: 8-25-81	X	WORKING	READER	DATE	CONTEXT:
MO	PROJECT: ICAM Architecture	REV:		DRAFT			3
	NOTES: 1 2 3 4 5 6 7 8 9 10			RECOMMENDED			MO
				PUBLICATION			

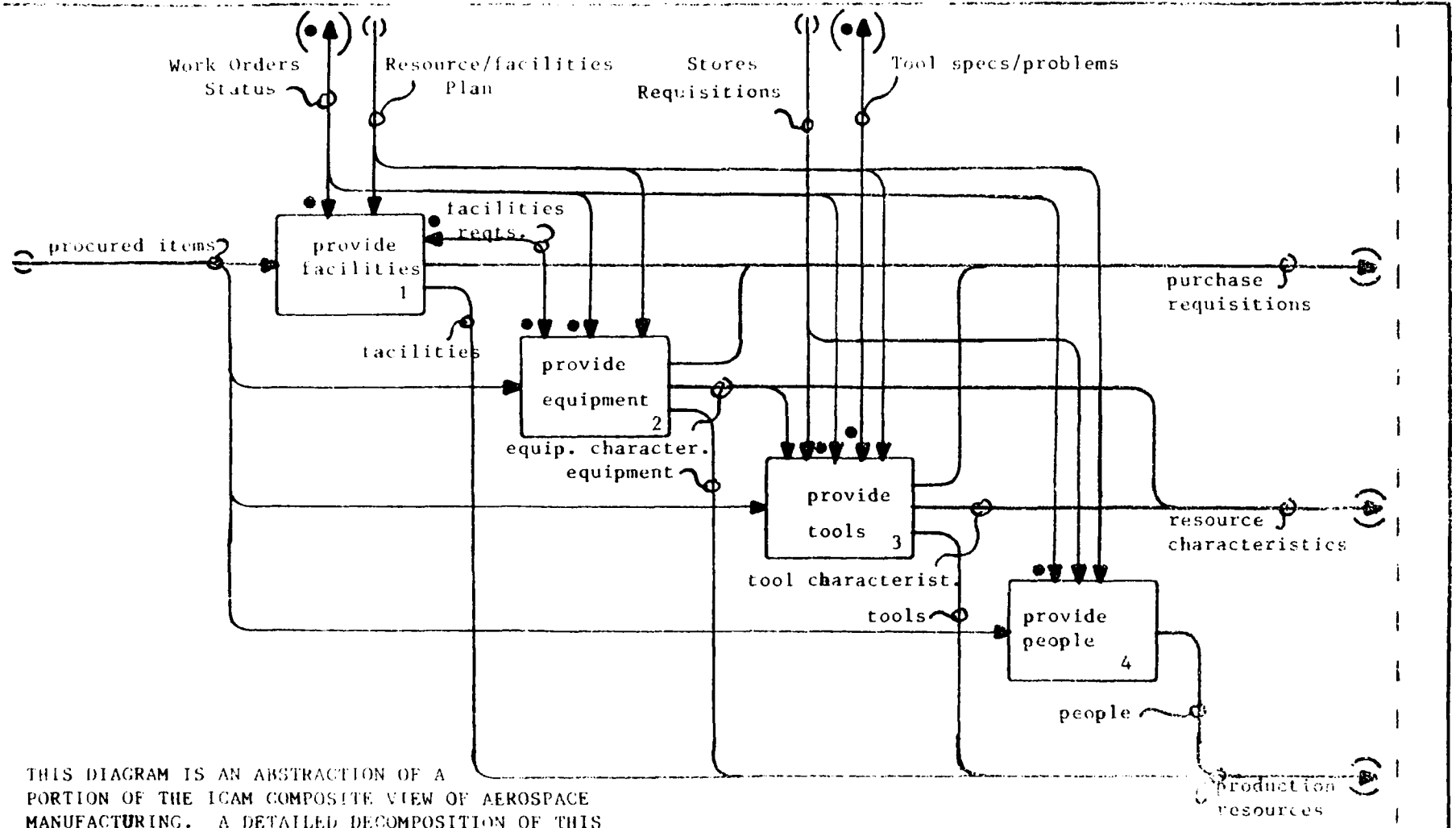


THIS DIAGRAM IS AN ABSTRACTION OF A PORTION OF THE ICAM COMPOSITE VIEW OF AEROSPACE MANUFACTURING. A DETAILED DECOMPOSITION OF THIS AREA IS INCLUDED IN THE ICAM CHART.

NODE:	TITLE:	NUMBER:
M3	PLAN PRODUCTION	A12

D16-416 GS 6/79

USED AT	AUTHOR: Keller, Dean A.	DATE 8-25-81	X WORKING	READER	DATE	CONTEXT:
MO	PROJECT: ICADAM Architecture	REV:	DRAFT			4
	NOTES: 1 2 3 4 5 6 7 8 9 10		RECOMMENDED			MO
			PUBLICATION			

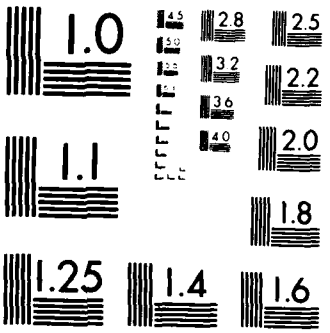


THIS DIAGRAM IS AN ABSTRACTION OF A PORTION OF THE ICAM COMPOSITE VIEW OF AEROSPACE MANUFACTURING. A DETAILED DECOMPOSITION OF THIS AREA IS INCLUDED IN THE ICAM CHART.

NODE:	TITLE:	NUMBER:
M4	PROVIDE PRODUCTION RESOURCES	A13

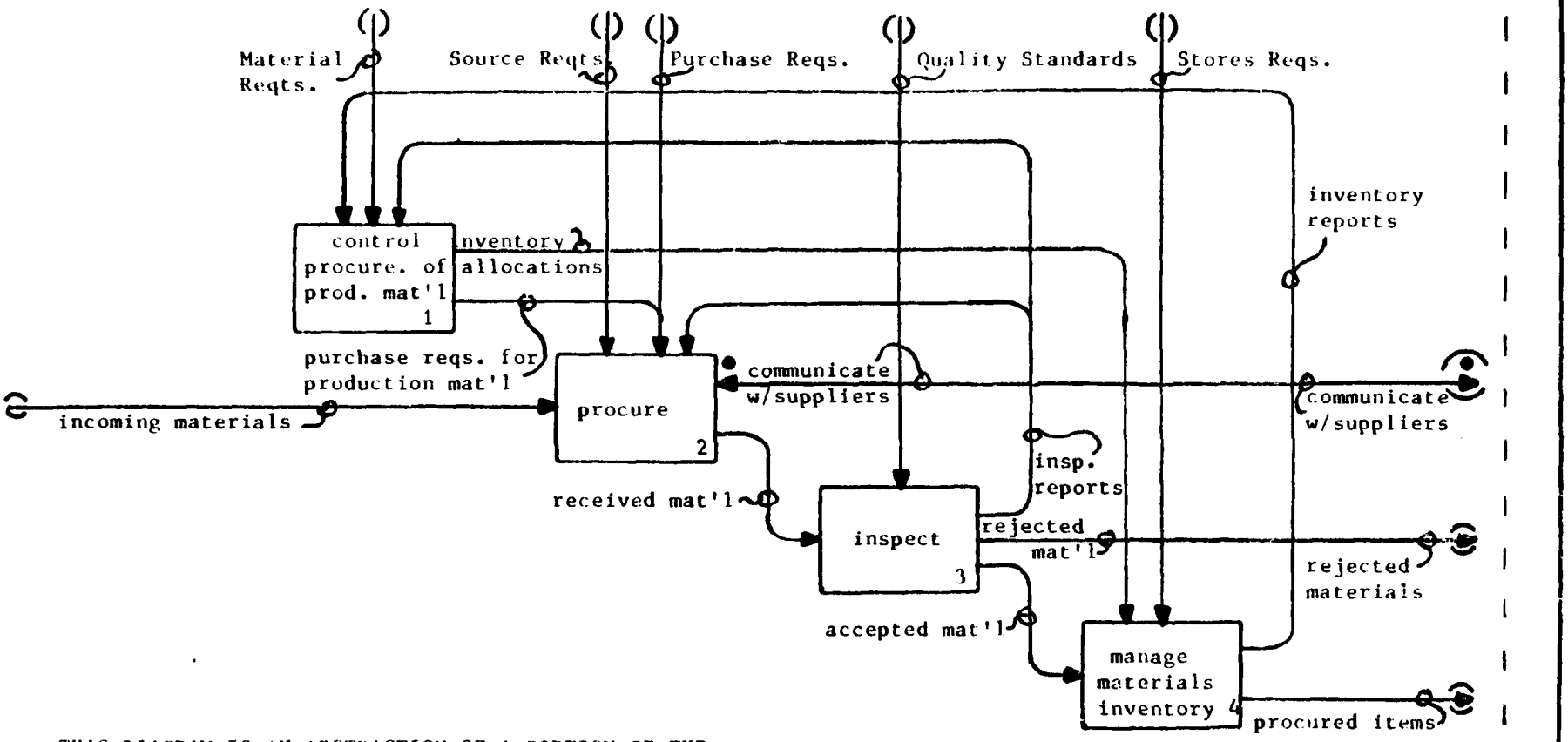
AD-A152 106 HYBRID INTEGRATED COMPUTER AIDED DESIGN AND MANUFACTURING(U) HUGHES AIRCRAFT CO TUCSON AZ TUCSON MFG DIV D A KELLER ET AL. 19 OCT 81 DAAH01-81-D-A002 2/2

UNCLASSIFIED F/G 9/2 NL



MICROCOPY RESOLUTION TEST CHART
NATIONAL BUREAU OF STANDARDS 1963-A

USED AT	AUTHOR: Keller, Dean A.	DATE 8-25-81	X WORKING	READER	DATE	CONTEXT:
MO	PROJECT: ICADAM Architecture	REV	DRAFT			MO 5
	NOTES: 1 2 3 4 5 6 7 8 9 10		RECOMMENDED PUBLICATION			

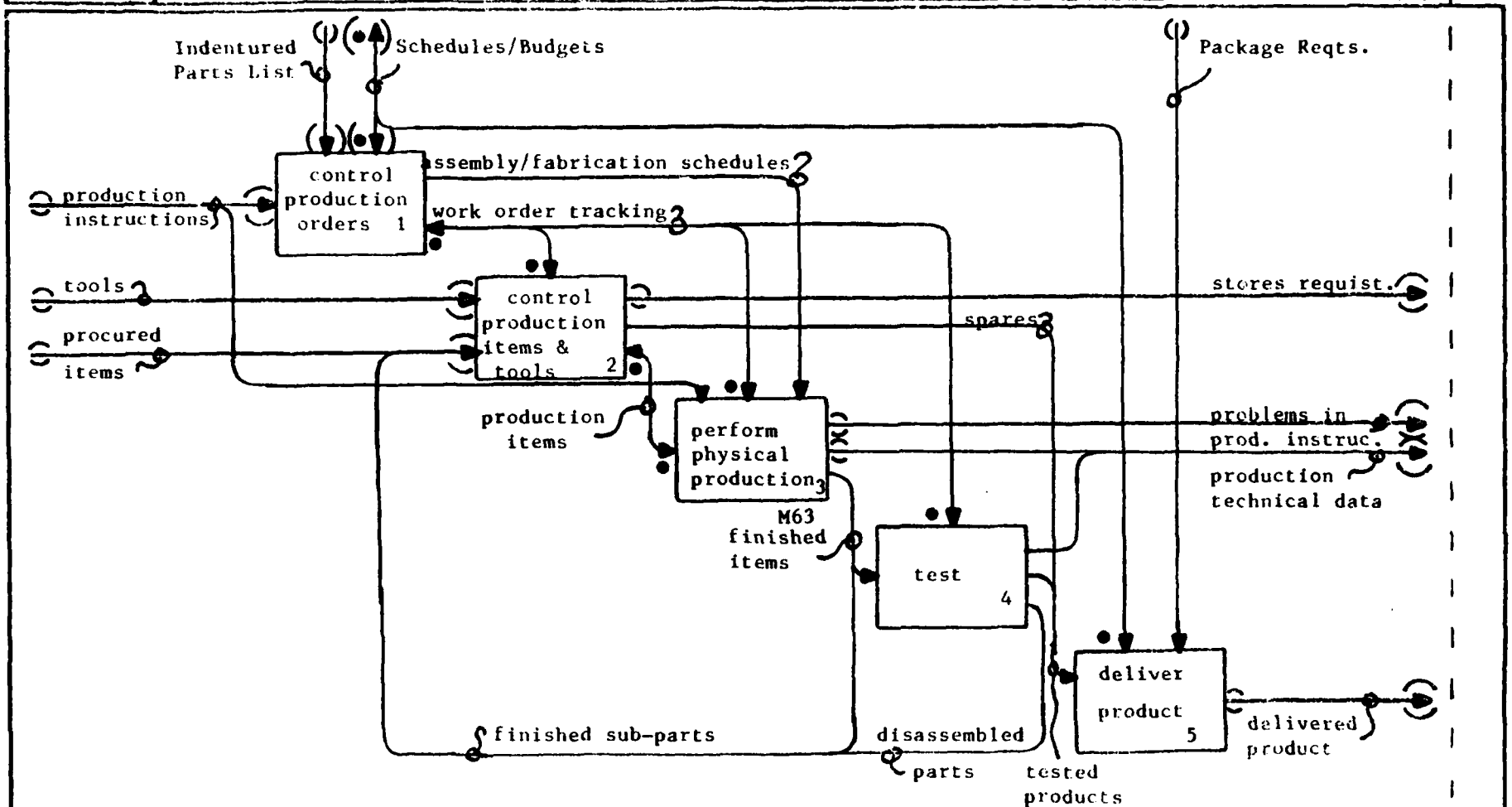


THIS DIAGRAM IS AN ABSTRACTION OF A PORTION OF THE ICAM COMPOSIT VIEW OF AEROSPACE MANUFACTURING. A DETAILED DECOMPOSITION OF THIS AREA IS INCLUDED IN THE ICAM CHART.

NODE:	TITLE:	NUMBER:
M5	OBTAIN MANUFACTURING MATERIALS	A14

D16-416 GS 6/79

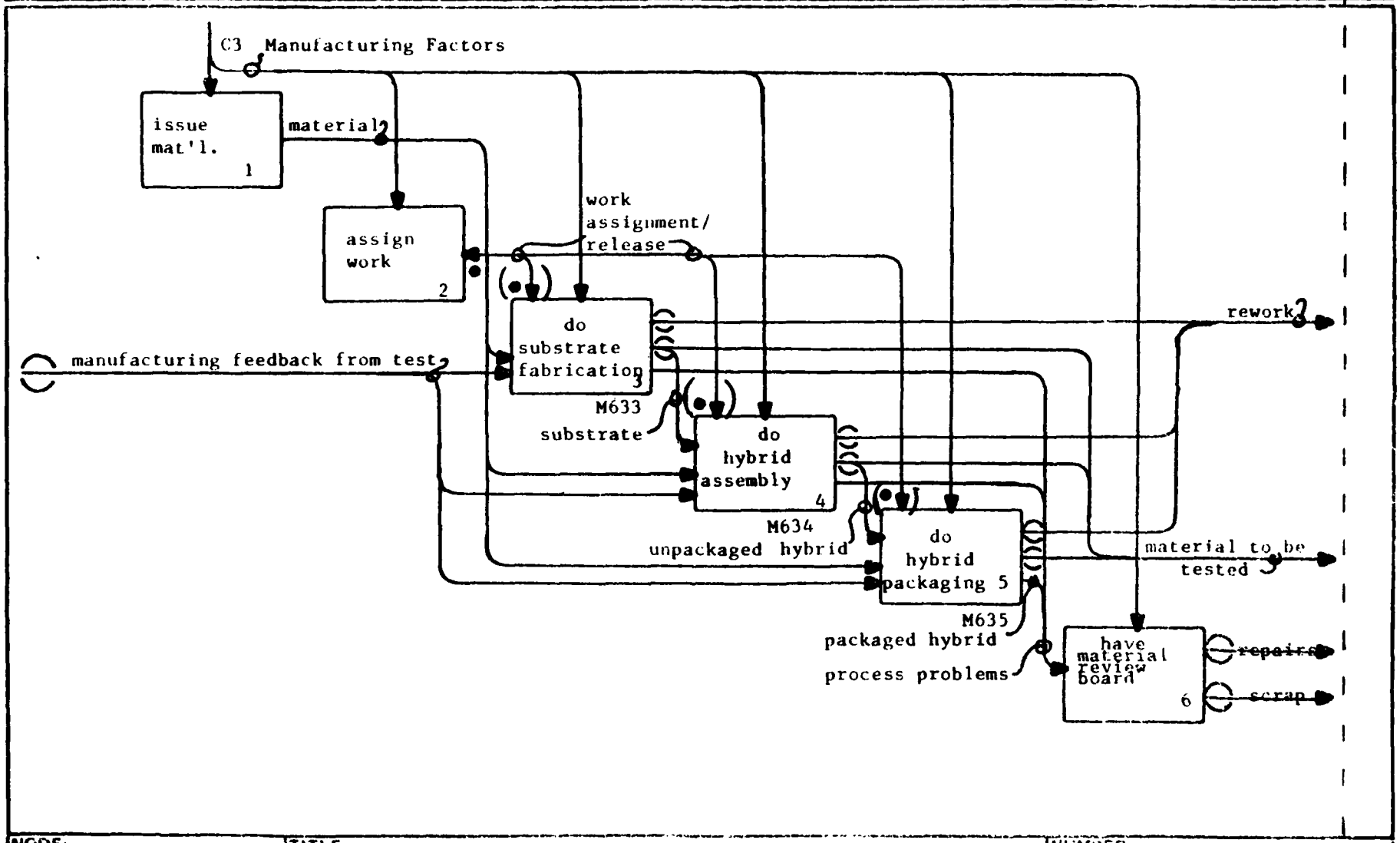
USED AT:	AUTHOR: Keller, Dean A.	DATE 8-25-81	X	WORKING	READER	DATE	CONTEXT:
MO	PROJECT: ICADAM Architecture	REV:		DRAFT			MO 6
	NOTES: 1 2 3 4 5 6 7 8 9 10			RECOMMENDED			
				PUBLICATION			



THIS DIAGRAM IS AN ABSTRACTION OF A PORTION OF THE ICAM COMPOSITE VIEW OF AEROSPACE MANUFACTURING. A DETAILED DECOMPOSITION OF THIS AREA IS INCLUDED IN THE ICAM CHART.

NODE:	TITLE:	NUMBER:
M6	PRODUCE PRODUCT	A15

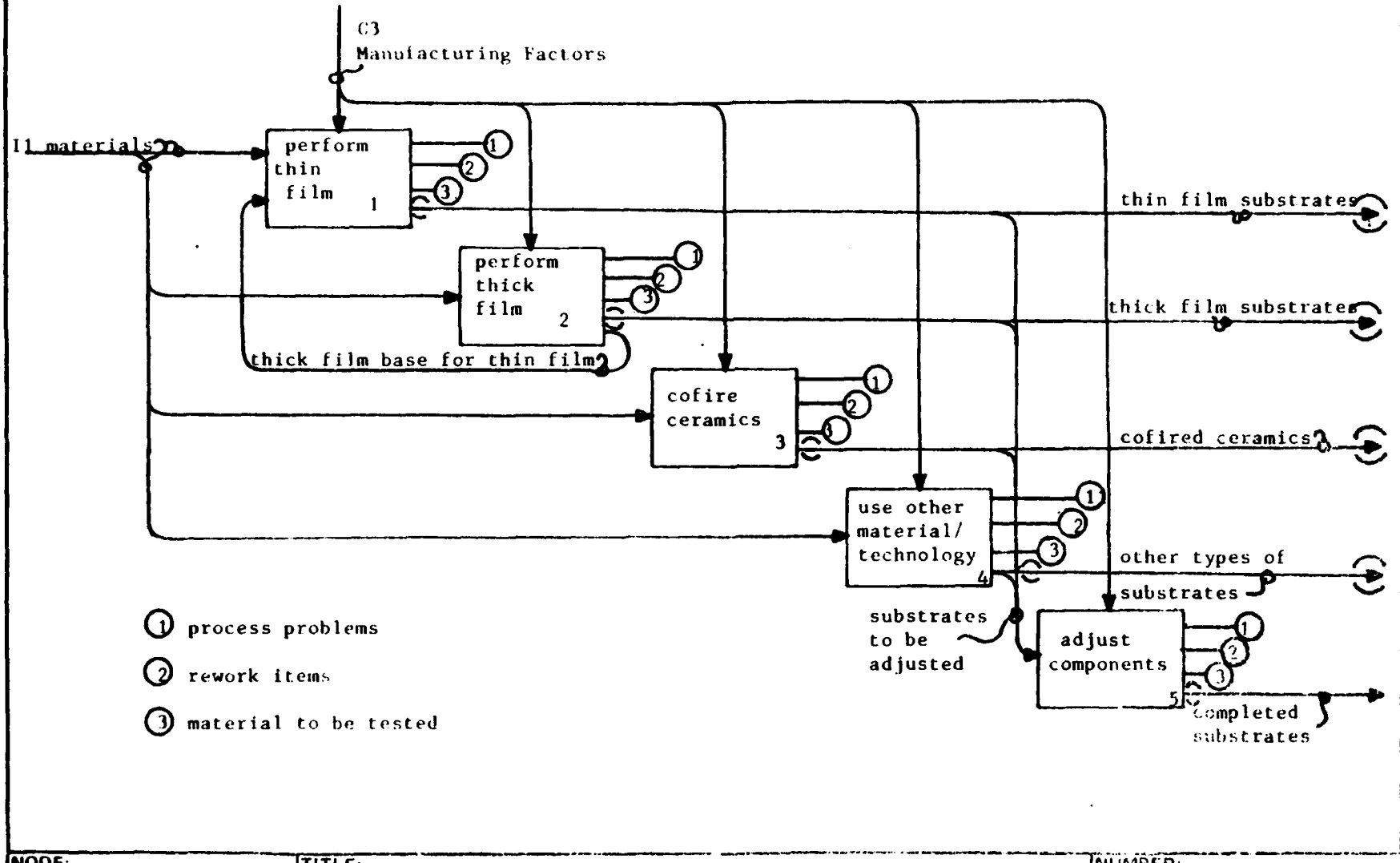
USED AT	AUTHOR: Keller, Dean A.	DATE: 7-27-81	X	WORKING	READER	DATE	CONTEXT:
M6	PROJECT: HICADAM Architecture	REV:		DRAFT			M6
	NOTES: 1 2 3 4 5 6 7 8 9 10			RECOMMENDED			
				PUBLICATION			



NODE:	TITLE:	NUMBER
M63	MANUFACTURE HYBRIDS	A16

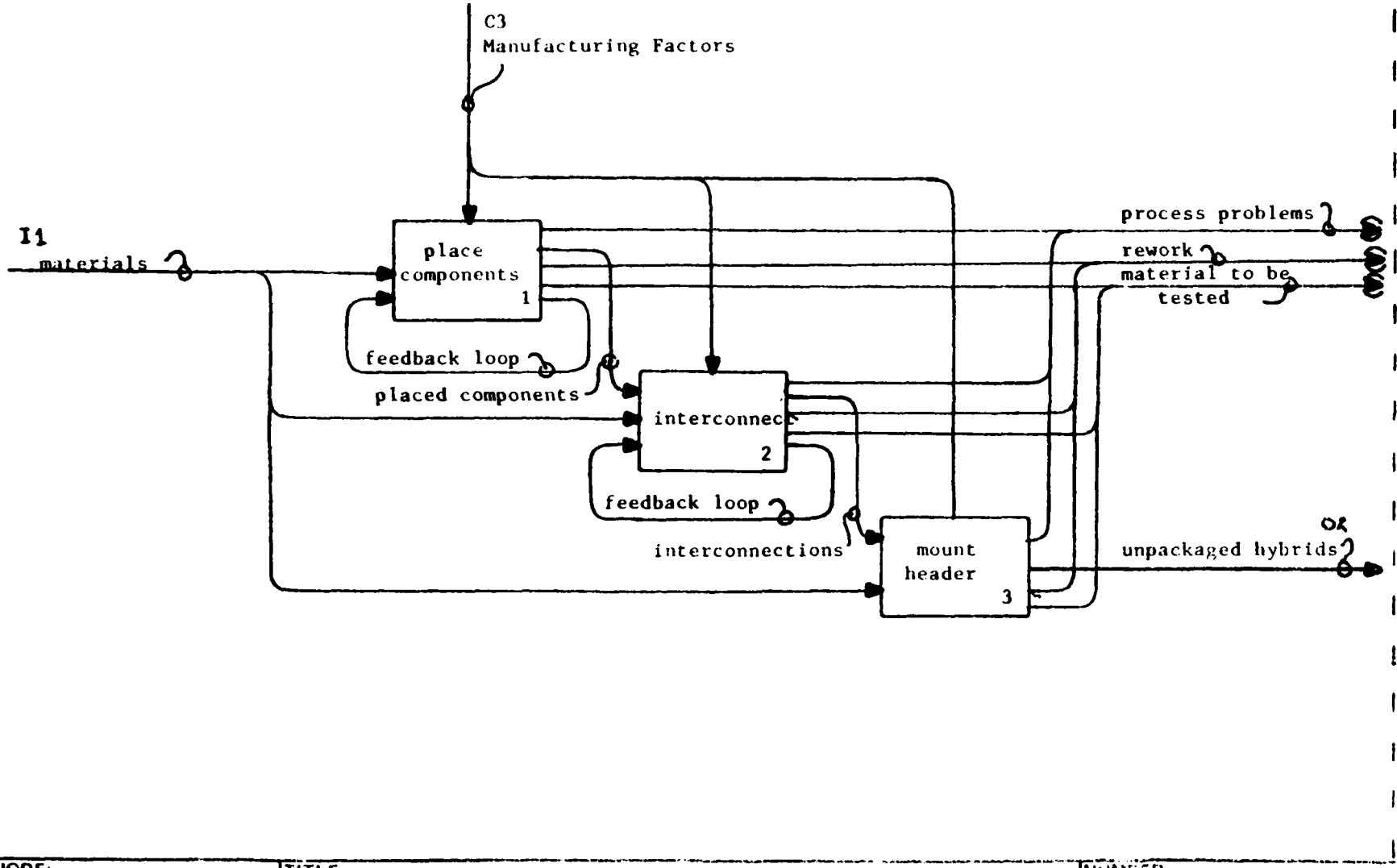
D16-416 GS 6/79

USED AT	AUTHOR: Feller, Dean A.	DATE 8-7-81	XX WORKING	READER	DATE	CONTEXT:
M63	PROJECT: ICAM Architecture	REV:	DRAFT			3
	NOTES: 1 2 3 4 5 6 7 8 9 10		RECOMMENDED			M63
			PUBLICATION			



NODE:	TITLE:	NUMBER:
M633	DO SUBSTRATE FABRICATION	A17

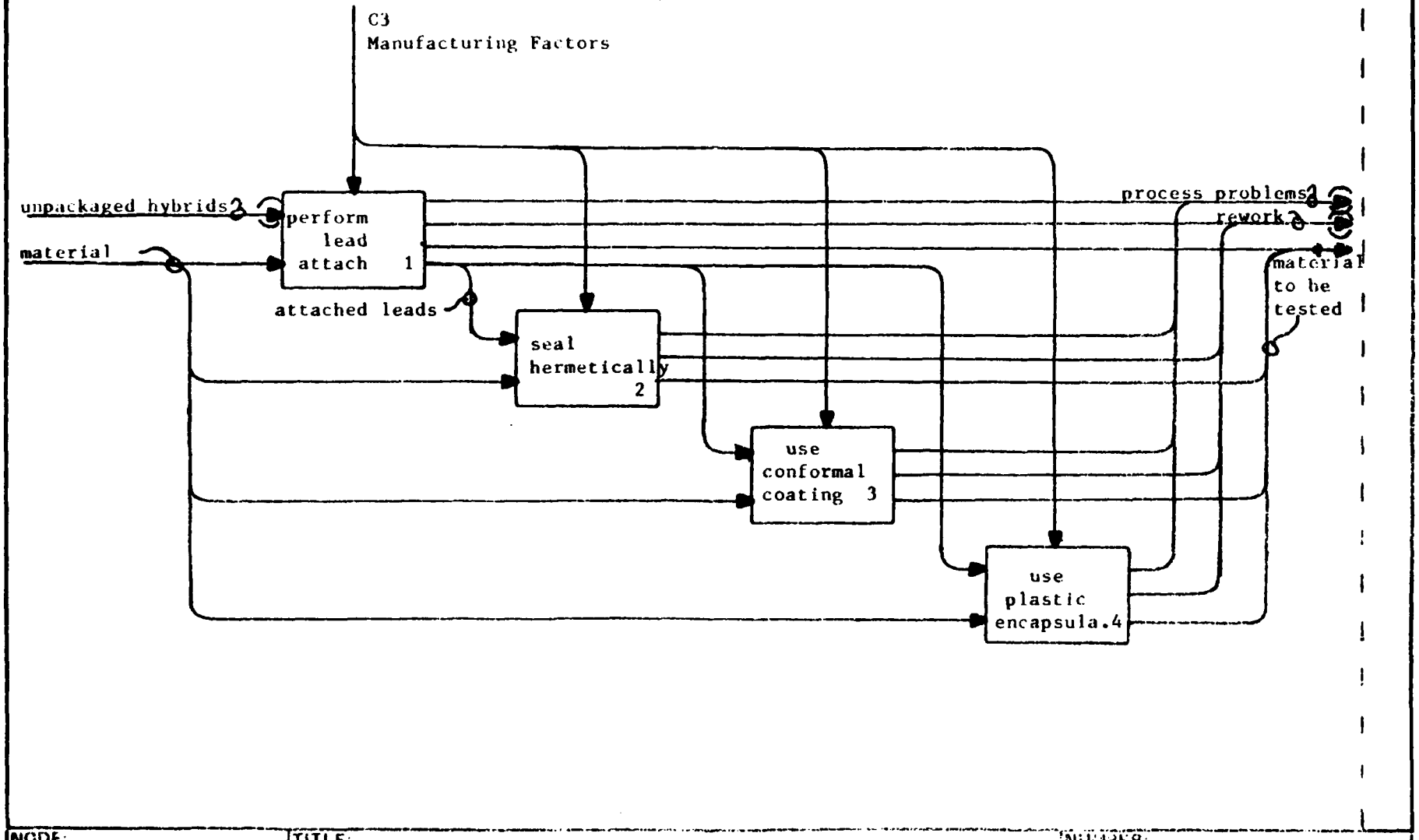
USED AT	AUTHOR	Keller, Dean A.	DATE 7-27-81	X	WORKING	READER	DATE	CONTEXT:
M63	PROJECT	ICAM Architecture	REV		DRAFT			M63 4
	NOTES: 1 2 3 4 5 6 7 8 9 10				RECOMMENDED			
					PUBLICATION			



NODE:	TITLE:	NUMBER:
M634	DO HYBRID ASSEMBLY	A18

D16-416 GS 6/79

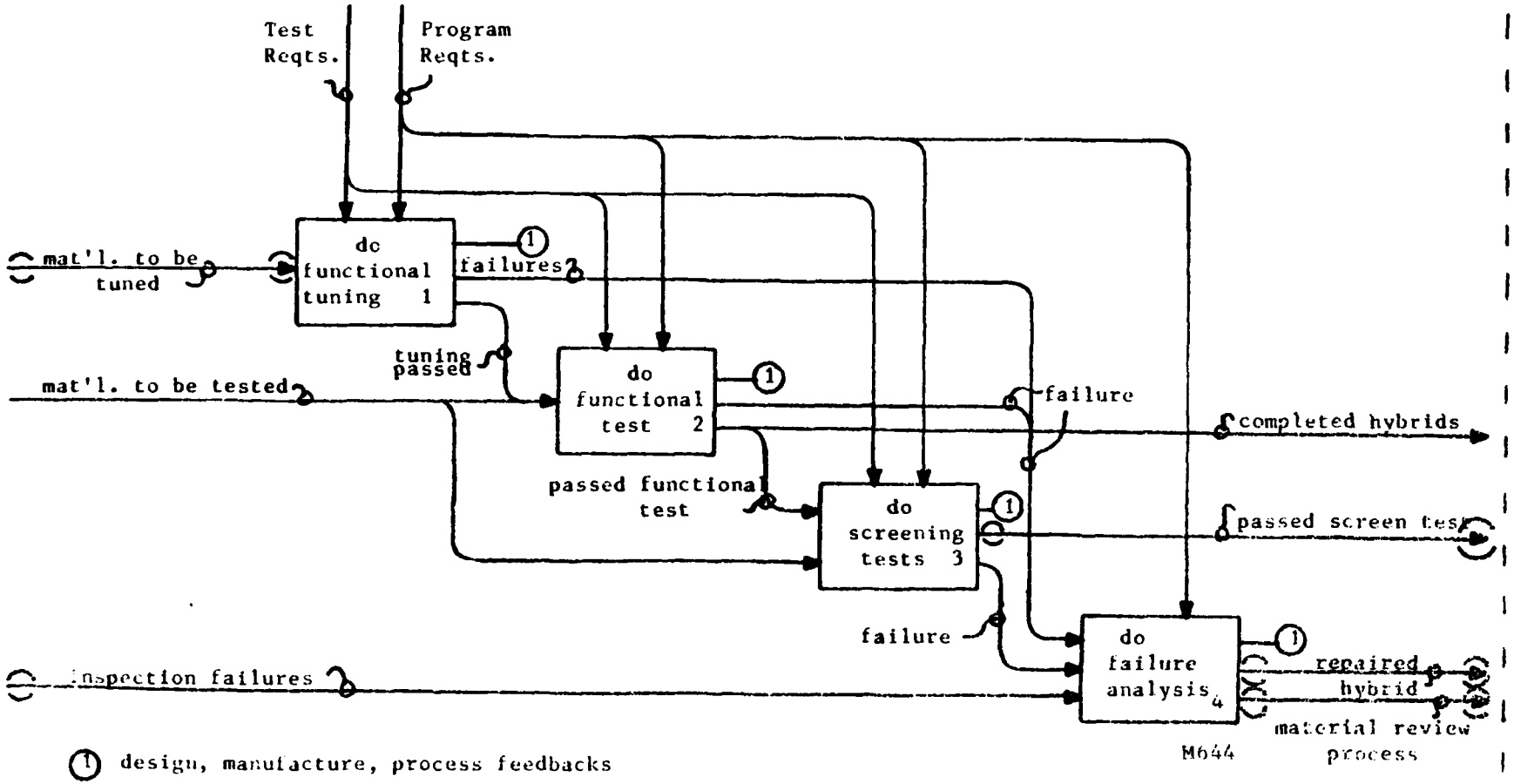
USED AT	AUTHOR: Keller, Dean A.	DATE: 7-27-81	X	WORKING	READER	DATE	CONTEXT:
M63	PROJECT: HICADAM Architecture	REV:		DRAFT			M63 (5)
	NOTES: 1 2 3 4 5 6 7 8 9 10			RECOMMENDED			
				PUBLICATION			



NODE:	TITLE:	NUMBER:
M635	DO HYBRID PACKAGING	A19

D16-41b GS 6/79

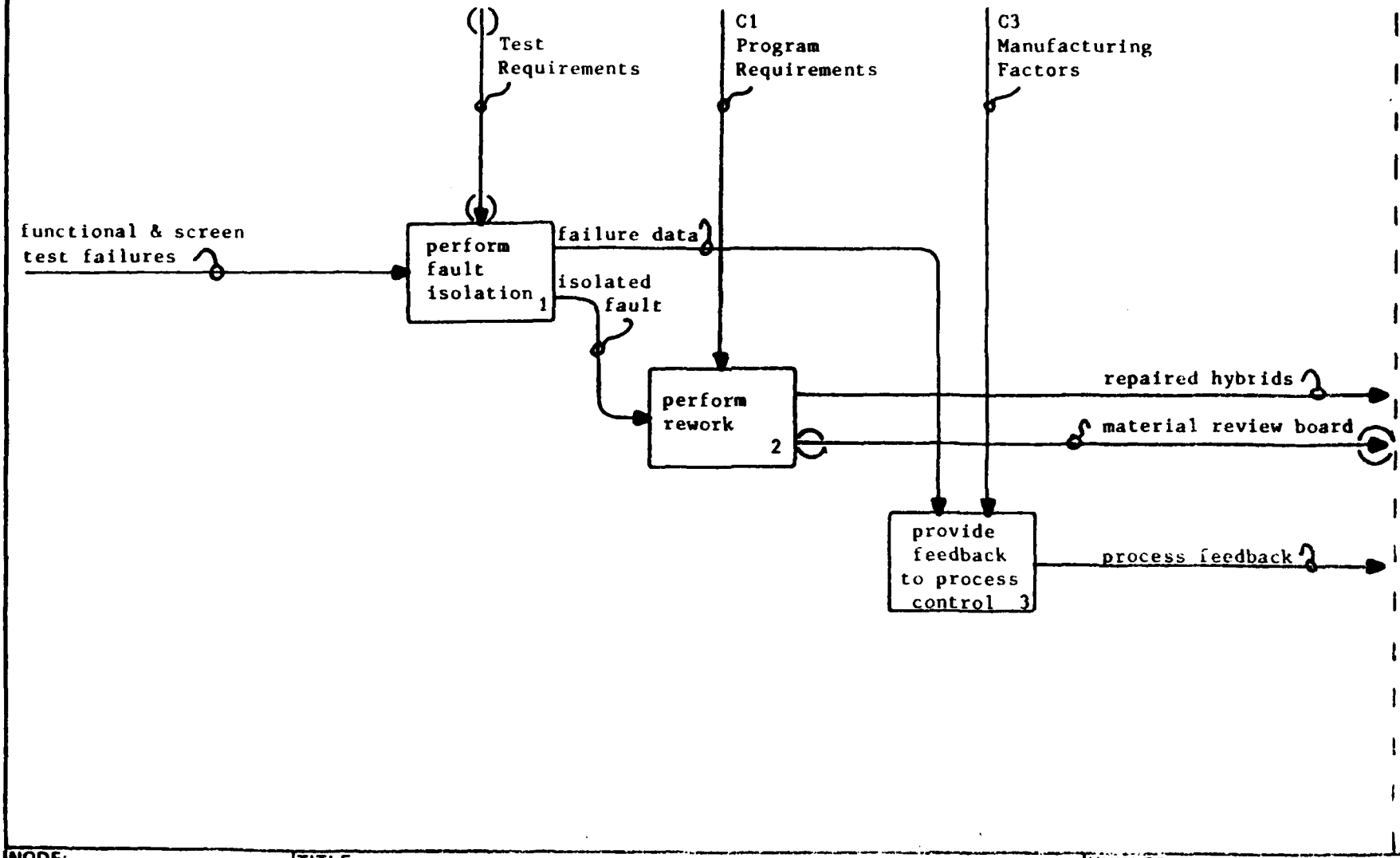
USED AT:	AUTHOR: Keller, Dean A.	DATE: 8-7-81	X	WORKING	READER	DATE	CONTEXT:
M6	PROJECT: HICADAM Architecture	REV:		DRAFT			M6 4
	NOTES: 1 2 3 4 5 6 7 8 9 10			RECOMMENDED			
				PUBLICATION			



NODE:	TITLE:	NUMBER:
M64	TEST HYBRIDS	A20

DI-S415 CS 6/79

USED AT	AUTHOR: Keller, Dean A.	DATE: 7-27-81		READER	DATE	CONTEXT:
M64	PROJECT: HICADAM Architecture	REV:	X WORKING			M64 4
	NOTES: 1 2 3 4 5 6 7 8 9 10		DRAFT			
			RECOMMENDED			
			PUBLICATION			



NODE:	TITLE:	NUMBER:
M644	DO FAILURE ANALYSIS	A21

D16-416 GS 6/79

END

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5-85

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