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3-D LOGIC THREE-DIMENSIONAL CMOS LOCALIZED OVERGROWTH
INTEGRATED CIRCUITS(U) HONEYWELL INC BLOOMINGTON MN
PHYSICAL SCIENCES CENTER S T LIU ET AL. 15 FEB 85

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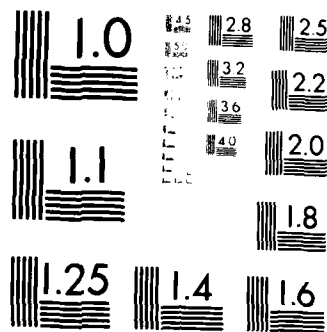
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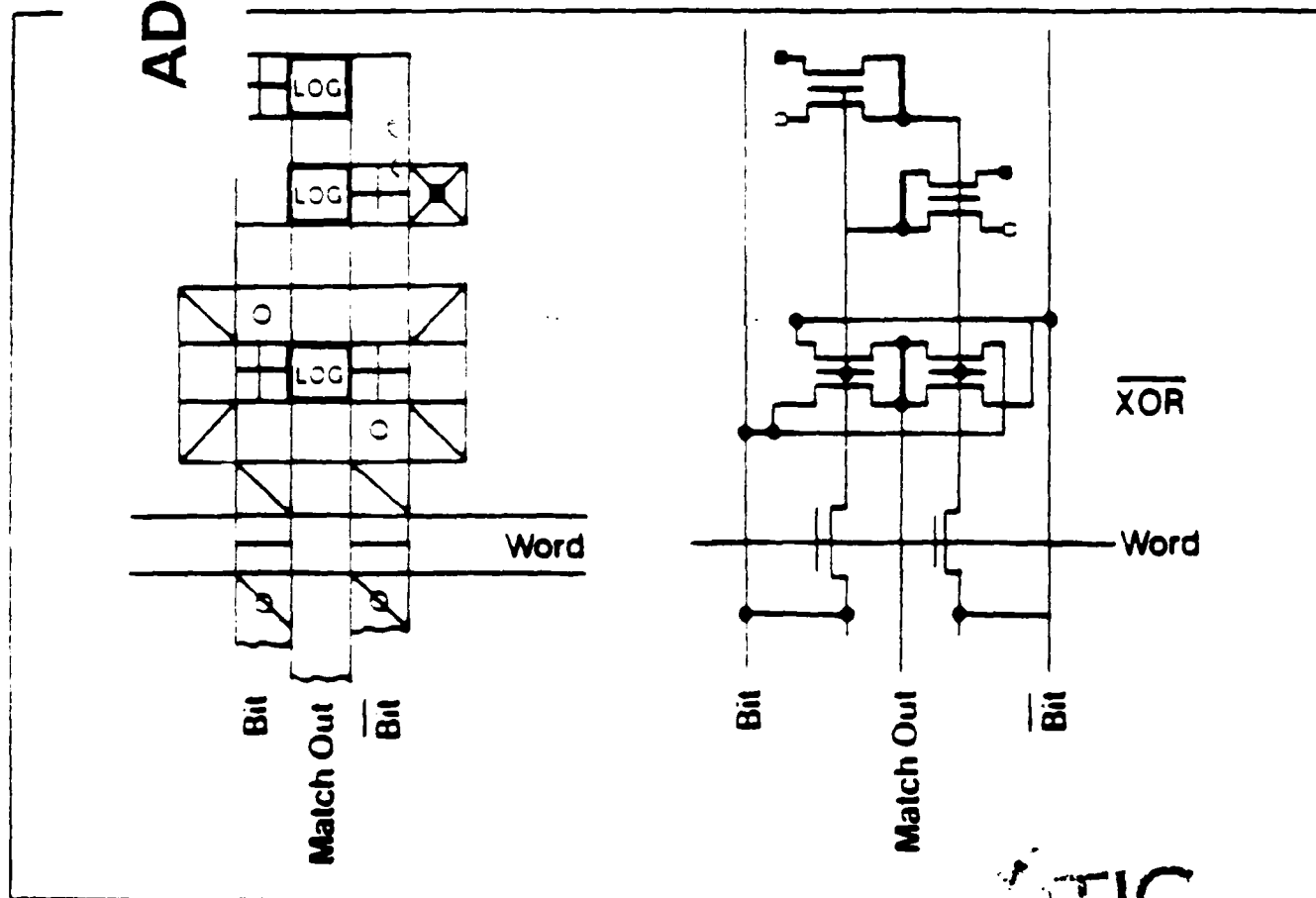
3D LOGIC, Three-Dimensional CMOS Localized Overgrowth Integrated Circuits

Quarterly Progress Report #2

16 November 1984-15 February 1985

N00014-84-C-0475 and
N00014-84-K-0438

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By the Honeywell/Purdue University Team

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THREE-DIMENSIONAL CMOS LOCALIZED
OVERGROWTH INTEGRATED CIRCUITS

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N00014-84-C-0475 and
N00014-84-K-0438

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P. E. Petersen, Manager Paul Petersen Date _____

1. INTRODUCTION

This is the 2nd quarterly report on "Three-Dimensional CMOS Integrated Circuits" program. The program is being done under two separate ONR contracts: Contract N00014-84-C-0475 at Honeywell Physical Sciences Center and Contract N00014-84-K-0438 at Purdue University.

The objective of the program is to develop a stacked ultra-high-density three-dimensional complementary MOS integrated circuit using VLSI compatible Local Over Growth (LOG) silicon technology. Major tasks to be accomplished are:

Task 1.2 Purdue Reactor

Task 1.3 LOG silicon process development

Task 1.4 Material test structure design

Task 2.1 Material test structure design

Task 2.2 Design of test devices

Task 3.0 Design of test vehicles

Task 4.0 Processing

Task 5.0 Testing

Progress to be reported for this quarter includes tasks 1.2, 1.3, 1.4, 2.1, 2.2, and 3.0.

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2. PROGRESS

In this quarter, graduate students R. Zingg and J. Denton, as well as faculty investigators B. Hoefflinger and G. Neudeck have been involved in the program (N00014-84-K-0438). S. Schuda has continued as professional staff in this program at Purdue University. At Honeywell, the program N00014-84-c-0475 has been performed by S.T. Liu, K. Newstrom, M. Hibbs, C. Knudsen, and R. George of the Physical Sciences Center, except the processing task 4.0. We plan to start the processing task at Stanford University involving L. Bousse, J.Meindl of Stanford and S. T. Liu next quarter.

In the quarter, we have submitted an abstract entitled "Single Crystal Films of Silicon Grown by Selective Epitaxy over Silicon Dioxide for 3D CMOS Integrated Circuits", by S. T. Liu, O. N. Tufte, K. Newstrom, B. Hoefflinger, G. Neudeck and R.Zingg to the Sixth University/Government/Industry Microelectronics Symposium for presentation this June.

2A. PURDUE REACTOR

The order for the Gemini II Reactor was placed December 7, 1984. The quoted delivery date is May 15, 1985. Laboratory space in the Potter Engineering Building has been designated for the setup of the reactor. After on-site studies at Gemini, U. S. Semiconductor, and Delco Electronics, all installation specifications have been finalized and work orders for the space preparation have been issued.

2B. DESIGN OF TEST STRUCTURES AND TEST DEVICES

The original test device design of May 1984 has been extensively redesigned and enhanced including structures for TEM evaluation. Test transistors can now be defined and contacted, both on top of the overgrowth and underneath the overgrowth. Masks for the top

transistors have been made at TAU Laboratories in compliance with mask aligner specifications, as provided by Stanford Electronics Laboratories. Figure 1 shows the first mask layer of this design. This mask is intended for LOG process study. The structures on top is for TEM study. Other structures include four point probe, capacitors, van der Pauw, and transistors.

2C. DESIGN OF TEST VEHICLES

On the basis of Stanford CMOS Design Rules, the 3-D CMOS Rules have been finalized February 1, 1985. The CAM cell reported in the last quarterly report has been redesigned accordingly. A test chip is presently in the layout phase, which will consist of four quadrants. Quadrant 1 will have test devices, decoders, sense amplifiers, ring oscillators, and Hamming distance logic. The second quadrant will contain the array of 64 RAM-CAM cells. The third quadrant will contain the complete RAM-CAM with decoders, sense amplifiers, and Hamming distance logic. The fourth quadrant will contain shift registers and frequency dividers.

2D. LOG PROCESS AND CHARACTERIZATION

During this quarter, nine runs of local overgrowth have been made and characterized. Each LOG run contained four or more silicon wafers with patterned oxide windows. The wafers are p-type (100) silicon 3" or 4" in diameter. The oxide window strips are oriented along the [010] direction for the first five runs and along the [110] direction for the next four runs.

Two different sets of patterned oxide windows were prepared using SY-4910 and LOGIC-001 mask sets. The two oxide thickness used were 300 angstroms and 10,000 angstroms. The patterned 300 angstrom and the 10,000 angstrom oxide wafers were prepared at Purdue and Honeywell respectively. The growth of local epitaxial silicon film was done at U. S. Semiconductor Services, Inc. using a modified GEMINI 1 reactor. The conditions for the experiment were $H_2=150$ liters per minute, $SiCl_2$

$H_2=0.6$ liters per minute, and $HCl=0$, 1.8 liters per minute corresponding to the HCl to $SiCl_2H_2$ ratios of zero and three. We grew thicker LOG films (~ 10 microns in these runs to explore details of the growth properties and to provide materials for making test structures according to the design.

We screened the LOG materials by optical microscope before SEM and x-ray analysis. The LOG materials without observable nucleation on SiO_2 in SiH_2Cl_2/H_2 with HCl gas system showed the same x-ray spectra by a computer controlled diffractometer as reported in the last quarter. We noticed some nucleation on SiO_2 even at HCl to $SiCl_2H_2$ ratio of three in the thick LOG runs for this quarter. This was attributed to the wafer surface conditions prior to the growth. Typically, no nucleation would be found on LOG materials at HCl to SiH_2Cl_2 of three in other LOG runs.

Different morphology was noted in the last quarterly report on (100)-[010] samples as compared to (100)-[110] samples. These facets were identified from a detailed study and summarized in Figure 2a and Figure 3a for (100)-[110] and (100)-[010] samples respectively. They show one (100) and four (311) surfaces in the (100)-[110] samples and one (100), four (311) and four (110) surfaces in the (100)-[010] samples. Figure 2a and Figure 3a show the LOG film grown out of the 6×8 micron² and 12×12 micron² oxide windows respectively with $HCl/SiCl_2H_2$ ratio of three.

On the long oxide strips, the (100)-[010] LOG films show more facets at the end as shown in Fig. 3(b) as compared to Fig. 2(b) for the (100)-[110] samples. The major facets are again (100), (311) and (110) for the (100)-[110] samples and (100) and (311) for (100)-[100] samples. The cross-sectional views of the long strips of the two different type of samples are shown in Fig. 2(c) and Fig. 3 (c). Very clearly the slope was steeper in (100)-[010] samples as compared to (100)-[110] samples. In addition, we observed also that the facet may have multiple steps as shown in Fig.4.

From this study, we concluded that the slowest growth planes are clearly (311) on (100)-[110] samples and (110) on (100)-[010] samples.

The implication of these facets is that the area of LOG materials can not be effectively utilized without modification of the growth surfaces (such as thin polysilicon coating) or new device structures. Also for small seeding or device area, (100)-[010] windows are less favorable because more facets are present in LOG films grown from small (100)-[010] windows. We are devising an in-situ etchback scheme to prepare the LOG samples to alleviate this problem for device application as well as detailed material research.

A detailed study of the growth rate of LOG films with $\text{HCl}/\text{SiH}_2\text{Cl}_2$ ratio of three was also made during this quarter. This condition was chosen because it gave us consistent results. The growth rate was 0.35 micron per minute for the (100)-[110] samples as compared to 0.45 micron per minute for the (100)-[010] samples. These rates were obtained from characterization of LOG films grown out of thin oxide (300A). As for the aspect ratio, we observed that it is close to one for the $\text{HCl}/\text{SiCl}_2\text{H}_2$ ratio of three.

Our study of defects in LOG films was delayed because of the delay in the design of the structures for the study by transmission microscope (TEM). We have designed the structures and expect to complete the study in the next quarter.

3. PLANS FOR NEXT QUARTER

The layout of the test vehicle will be finished March 15, 1985. The setup of a parametric and logic tester will begin. Preparation of the reactor site and delivery of the reactor are scheduled for that period.

We plan to start processing the first test structures and test devices at Stanford Integrated Circuits Laboratory next quarter. Defects and some electrical properties will be investigated. We plan to look into the method(s) to provide the planarization specifically required by the 3D CMOS and alternative structure(s) for 3D CMOS by using the local overgrowth technique as developed in this program. We plan also to look into methods of improving the local overgrowth without faceting.

Single Crystalline Films of Silicon Grown by Selective Epitaxy Over Silicon Dioxides for 3D CMOS Integrated Circuits *

by

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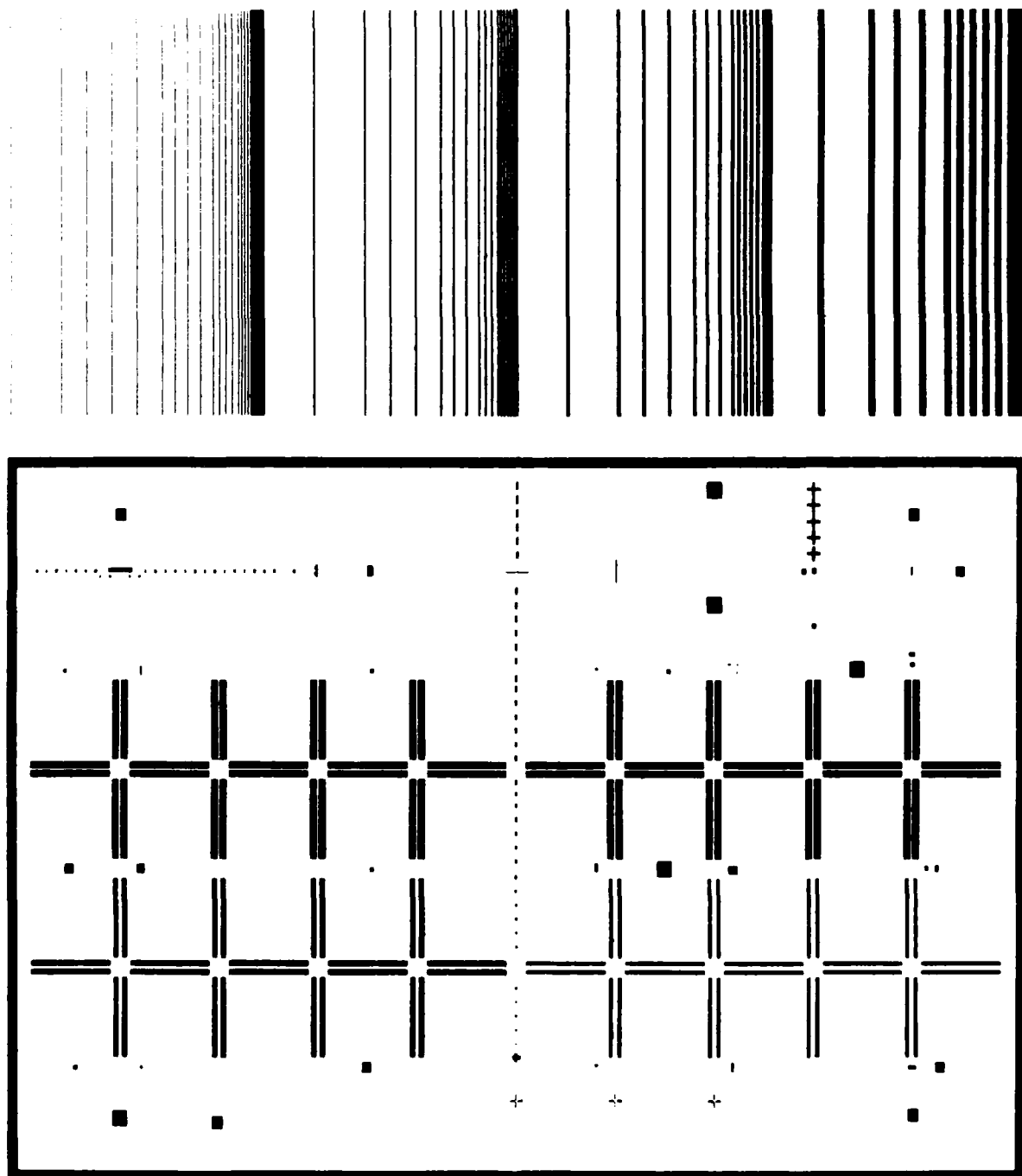
ABSTRACT

The selective epitaxial growth of silicon films for IC fabrication with a special emphasis for three-dimensional CMOS integrated circuits is discussed in this paper.

Localized crystalline thin films of silicon have been grown selectively from window strips, which have been cut in the silicon dioxide. This was done in a RF heated low-pressure epitaxial reactor. The silicon substrates are (100) and the reactant gases are SiH_2Cl_2 , HCl and H_2 . These thin silicon films have well-developed facets, depending on the shapes and orientations of the silicon dioxide window strips.

Specifically, the morphology and the growth rate are studied in detail, as a function of the relative ratio of HCl to SiH_2Cl_2 from 0 to 6 with the silicon dioxide window strips oriented in $[110]$ and $[100]$ directions. At the lower ratios, nucleation on the silicon dioxides results in polycrystalline films. At the higher ratios, etching into bulk silicon, which is defined by the window strips, results in no deposition. The desired results, selective epitaxial growth, are obtained in between. The facets mentioned have been identified to be (100), (101) and (311) by scanning electron and optical micrographs.

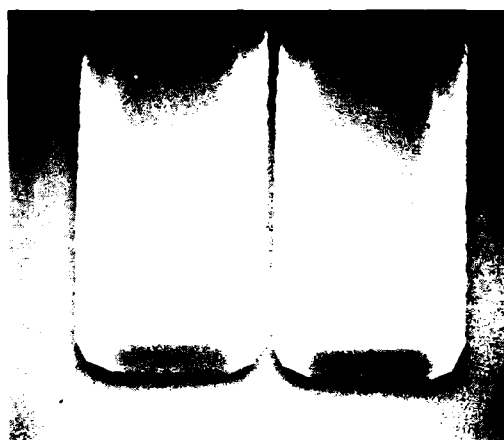
*Supported by Office of Naval Research under contracts N00014-84-C-0475 and N00014-84-K-0438.



**Figure 1 Patterns of Test Structures and Devices
(LOGIC-001)**



(a)



(b)



(c)

Figure 2 (a) Morphology of a LOG film grown out of a $6 \times 8 \text{ micron}^2$ oxide window, displaying one (100) and four (311) major facets; (b) Morphology of a LOG film out of two long strips; (c) cross-sectional profile of a long strip.



(a)



(b)



(c)

Figure 3 (a) Morphology of a LOG film grown out of a 12 x 12 micron² oxide window displaying one (100), four (311) and four (110) facets; (b) Morphology of two long strips; (c) Cross-sectional view of the long strips.

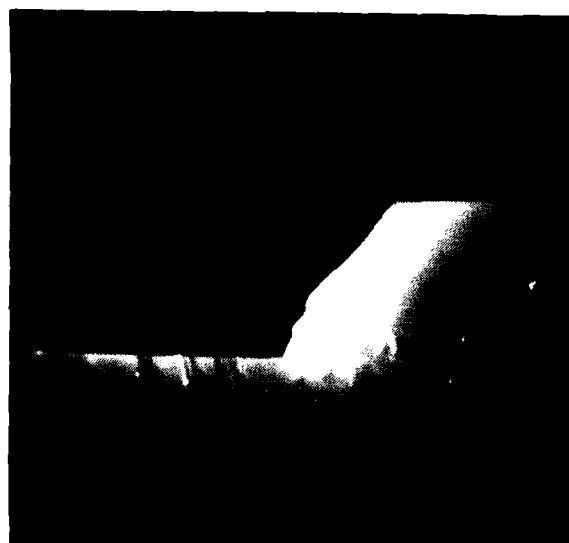


Figure 4 Cross-sectional view of a LOG film in a long strip oriented along $[010]$, showing multiple steps of (110) and (100) surfaces.

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