EFFECT OF DISLOCATIONS ON GALLIUM ARSENIDE FETs

AD-A152 249

R&D Status Report No. 2 for the Period
November 1, 1984 to February 1, 1985

Office of Naval Research/
Defense Advanced Research Projects Agency
Contract No. N00014-84-C-0632

D. L. Barrett, S. McGuigan, G. W. Eldridge,
B. W. Swanson, and R. N. Thomas

February 15, 1985

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Westinghouse R&D Center
1310 Beulah Road
Pittsburgh. Pennsylvania 15235

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18. SUPPLEMENTARY NOTES

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DISLOCATION. INDIUM. DOPING. GALLIUM ARSENIDE. FET. LARGE. DIAMETER. SUBSTRATES. DEVELOPMENT. CRYSTALS. THERMAL. STRESSES.

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

Indium doping at 5×10^{19} cm^{-3} was found to be optimum for the growth of low-dislocation GaAs crystals, and to avoid constitutional supercooling effects. Dislocation etch pit densities of near 200 cm^{-3} were measured in the central region of In-doped crystals, increasing to above 10^4 cm^{-2} in the peripheral regions. Based on the concept that dislocations are generated to relieve excess thermoelastic stress, a preliminary thermal model was used to design a hot zone shield to reduce thermal gradients during growth. An optimum

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Item 20 continued:

combination of indium-doping, reduced thermal gradient growth, and appropriate growth parameters are expected to yield completely dislocation-free GaAs crystals. A FET metrology mask set has been fabricated and preliminary FET device fabrication begun, for evaluation of the effects of dislocations on FET device parameters. Twenty state-of-the-art, low-dislocation, indium-doped GaAs wafers were delivered to the contractor for DARPA-related program evaluation.

R&D STATUS REPORT NO. 2

EFFECT OF DISLOCATIONS ON GALLIUM ARSENIDE FETs

DARPA ORDER NO.: 5217 PROGRAM CODE NO.:

CONTRACTOR: Westinghouse Electric Corporation
R&D Center, Pittsburgh, PA 15235

CONTRACT NO.: N00014-84-C-0632 CONTRACT AMOUNT: $498,018

EFFECTIVE DATE OF CONTRACT: 8/1/84

EXPIRATION DATE OF CONTRACT: 9/30/86

PROGRAM MANAGER: R. N. Thomas
TELEPHONE NUMBER: (412) 256-1871

PRINCIPAL INVESTIGATOR: D. L. Barrett

TELEPHONE NUMBER: (412) 256-1898

SHORT TITLE OF WORK: Dislocations in GaAs FETs

REPORTING PERIOD: 11/1/84 to 2/1/85

The views and conclusions contained in this document are those of the authors and should not be interpreted as necessarily the official policies, either expressed or implied, of the Defense Advanced Research Projects Agency or the U.S. Government.

1. TECHNICAL PROGRESS

During the second quarter of this program, we have directed our efforts toward:

i) optimization of indum doping in 50-mm diameter crystals,
ii) preparation of indium-doped polished wafers,
iii) evaluation of dislocation reduction and electrical characteristics in In-doped wafers,
iv) fabrication of FET metrology mask sets.

Several areas have been studied in our efforts to develop dislocation-free 50-mm diameter In-doped GaAs with the following results:

- An indium concentration of 5×10^{19} cm^{-3} is required to obtain etch pit densities of 200 cm^{-2} or less in the central regions of the 40-mm diameter grown crystals.

- The onset of constitutional supercooling in 50-mm diameter crystals grown from 1 atomic % In-doped melts was observed to occur at approximately g = 0.7 (where g = fraction of melt solidified), with crystal growth rates of 9 mm per hour. Calculations indicate that reducing the growth rate from 9 mm to 3 mm per hour will delay the onset of constitutional supercooling until 90% of the melt has been solidified. This effect will be explored during this next quarter by gradually decreasing the growth rate as the crystal is pulled to avoid growth instabilities.

- Etch pit densities of near 10^4 cm^{-2} are observed in the peripheral region of grown crystals. Increasing the indium

content to $>10^{20}$ cm^{-3} to eliminate these peripheral dislocations results in the onset of constitutional supercooling effects. Consequently, we will explore reduced thermal gradient growth to reduce excess peripheral stresses with the resulting generation of dislocations; however, a trade-off is anticipated since reduced gradients will cause the onset of constitutional supercooling at lower indium concentrations.

- Thermal heat-transfer modeling shows that an increase in boron oxide thickness from 2 cm to 10 cm reduces the temperature gradient in the encapsulant from 120°C/cm to 30°C/cm, and will reduce the excess shear stress by a factor of four. In a growth experiment, a temperature gradient of 60°C/cm was measured in a 6-cm B_2O_3 layer, in qualitative agreement with the calculation. However, attempts to grow crystals from both a 6-cm encapsulated melt and a 4-cm encapsulated melt were not successful because of twin formation. A modification of our crystal growth parameters will be necessary to achieve twin-free crystals from melts with thick encapsulant layers.

- Preliminary modeling of conduction, convection, and radiative heat transfer in the LEC puller shows upper radiation shielding as well as thick B_2O_3 layers to be the most influential factor in reducing thermal gradients in the encapsulant. As a result of these calculations, design criteria for a double-shell radiation shield were established, and this shield is currently being fabricated.

- Annealing indium-doped crystals at 980°C for 18 hours has been found to relieve grown-in stress, with the result that crystal cracking is virtually eliminated and yields of

polished wafers were improved significantly. Improved uniformity was also observed in radial resistivity and mobility profiles as a result of this whole crystal-annealing process.

- Electrical evaluation of In-doped GaAs grown from stoichiometric to slightly As-rich melts show high, thermally stable resistivities and electron mobilities typically 5000 cm^2/Vsec or better, with exceptional radial uniformity (±7% across wafer diameters).

- The FET metrology DSW mask set has been fabricated, and preliminary device fabrication on 50-mm indium-doped and 75-mm undoped wafers is in progress. This mask design consists of seven levels: alignment marks, n^+ implant, n-channel implant, ohmic contact, gate contact, isolation implant, and passivation access.

- One quarter of the mask field is devoted to conventional FETs (1.2 μm gate on 7 μm source-drain spacings) laid out on three spacing centers to evaluate uniformity and correlation with dislocation position. A second quarter is devoted to process verification structures. Both gradients are rotated by 90° to complete the mask field and to permit correlation of FET characteristics with growth striations and residual slip planes.

- Implant qualification and characterization of In-doped wafers is in process using standard contact photolithographic techniques. The relative merits of transient and capped annealing techniques are also under evaluation using low-dislocation indium-doped GaAs substrate wafers to optimize implant technology. The flatness of presently polished wafer

substrates is more than sufficient to meet projection printing autofocus requirements.

Two crystals grown from 1 atomic % indium-doped melts have been characterized and processed into polished wafers for FET characterization and material evaluations. Indium-doped GaAs wafers have been supplied to several DARPA contractors for evaluation, and 20 wafers have been supplied to the scientific officer as part of contract-required delivery. Table 1 lists pertinent crystal and wafer evaluations. The etch pit density profiles are different in the two crystals even though the indium content in both is nearly identical. Crystal BN109 has center etch-pit densities near 200 cm^{-2}, while the center region in crystal BN108 has a density near 10^4 cm^{-2}. This result cannot be accounted for by seed-generated dislocations. Additional studies are required to describe a m chanism for this difference in dislocation density.

TABLE 1

In-DOPED GaAs CRYSTAL AND WAFER EVALUATIONS

Boule	BN108	BN109
Dia. (mm)	53 ± 2	54 ± 2
Ground and Flat	50.8	No
Wafer		
Orientation	<100> 2° off	<100> approx.
Diameter (mm)	50.5 (edge rounded)	49.3 - 0.6 (edge ground)
Thickness (mm)	0.55 ± .02	0.55 ± .02
Polish (NaOCl)	Double-side	Double-side
Wafer Delivery	64-65-66-67-68 69-70-71-72-74	60-66-67-68-69 70-71-72-73-74
Calc. In Content (cm^{-3}) (Keff = 0.1)	6×10^{19}	8×10^{19}
EPD (cm^{-2})	Wafer No. 110	Wafer No. 61
Center	13,000	220
r/2	7,300	1,200
Edge	72,000	28,000
Sheet Resistance (ohm/square) (As grown)	4×10^9	1×10^9
Mobility (cm^2/Vs) (as grown)	3400 seed 5900 tang	7000 seed 5600 tang
Sheet Resistance (ohm/square) Annealed	$> 1 \times 10^8$	$> 1 \times 10^8$

2. KEY PERSONNEL

No change in key personnel associated with the contract has occurred during the reporting period.

3. SPECIAL EVENTS

None.

4. PROBLEM ENCOUNTERED AND/OR ANTICIPATED

No deviation from the original planned effort to achieve the end objectives of the contract is anticipated at present.

5. ACTION REQUIRED BY THE GOVERNMENT

No action is required by the Government at this time.

6. FISCAL STATUS (as of 1/31/85)

1.	Amount currently provided on contract:	$130,018
2.	Expenditures and commitments to date:	$135,370
3.	Funds required to complete work:	$498,018

ENCLOSURE NUMBER 3   CONTRACT NUMBER: N00014-84-C-0632

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