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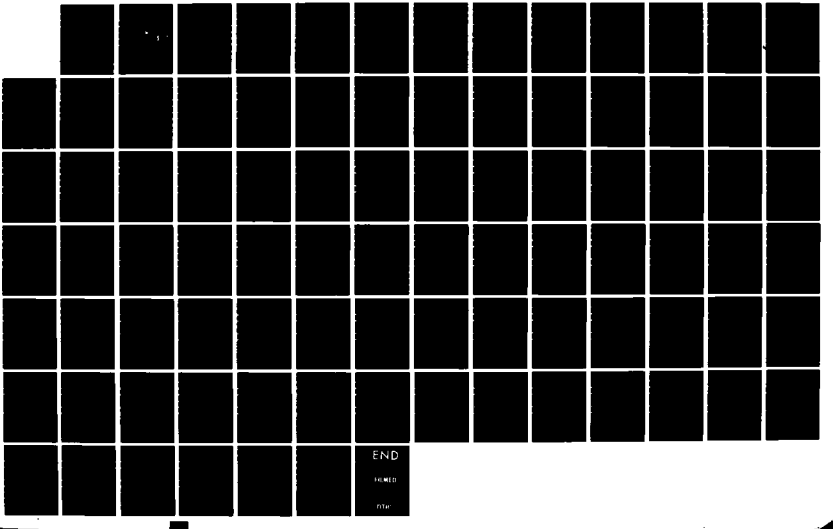

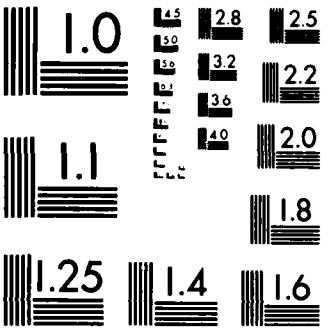

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NAVAL POSTGRADUATE SCHOOL

Monterey, California

THESIS

EXPERIMENTAL PERFORMANCE
OF A
FREQUENCY MEASUREMENT CIRCUIT

by

George H. Eastwood

December 1984

Thesis Advisor: G. A. Myers

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Experimental Performance of a Frequency Measurement Circuit

by

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Submitted in partial fulfillment of the requirements for the degree of

MASTER OF SCIENCE IN ELECTRICAL ENGINEERING

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ABSTRACT

The accuracy with which the frequency of a sinusoid and a pulsed sinusoid can be measured using a phase locked loop is investigated. A frequency divider is inserted into the feedback loop and a very stable local clock is used to determine the effect of these modifications on the frequency measurement accuracy of the phase locked loop. The primary result is that there is no theoretical limit to the accuracy of frequency measurement, independent of gate time, using a phase locked loop with frequency division and very stable clocks. The practical tradeoffs for improved frequency measurement accuracy are a higher required signal to noise ratio and a reduction of the frequency capture range of the phase locked loop.

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I. INTRODUCTION

Paralleling the historically ever increasing requirement to more accurately measure an increment of time is a similar requirement to more accurately measure frequency (of a sinusoidal voltage, typically). The frequency of a sinusoid is often used to represent data or a physical parameter. In some applications, the amount of doppler shift on a received signal is of interest. Moving target indicators (MTI) in radars are an example.

This paper addresses the problem of accurately measuring the frequency of a tone in a small interval of time to determine the theoretical and practical limits of accuracy of measurement. Chapter II begins by providing background on the fundamental limitations of measuring frequency accurately with a frequency counter and developes the concept of using a frequency divider with a phase locked loop as a method to circumvent these limitations. Chapter III is a detailed description of the circuitry used to gather data. The experimental procedures followed and the resulting data are provided by Chapter IV. Chapter V summarizes the data and presents the conclusions evident from the experiment.

II. BACKGROUND

The frequency of a tone can be measured using a frequency counter which converts the number of zero crossings Z occuring during a known gate time, T seconds, into its corresponding frequency F. Since there are two zero crossings per cycle, $F=(Z/2)/T$ HZ. Frequency counters generally have two modes of operation, FREQUENCY and COUNT, and the value of F and the value of (Z/2) is displayed respectively when each is selected.

The accuracy of measurement of the frequency counter is fundamentally limited to $\pm(1/T)$. The ± 1 count in T seconds is caused by the T second window not occuring at the same place relative to a continous waveform each time a measurement is taken. As an example, the square wave of Fig. 1 has five zero crossings in region I and four zero crossings in region II even though both regions have the same duration of T seconds. This fundamental limit of $\pm(1/T)$ accuracy can be further degraded by several factors:

- A stable and precise gate time is required for a consistent and corresponding number of zero crossings; otherwise repeatability of the measurement suffers.
- The frequency counter itself is based upon a clock and any instability in this clock degrades accuracy.
- Noise introduces additional zero crossings which corrupts the accuracy of the measurement of the signal frequency.

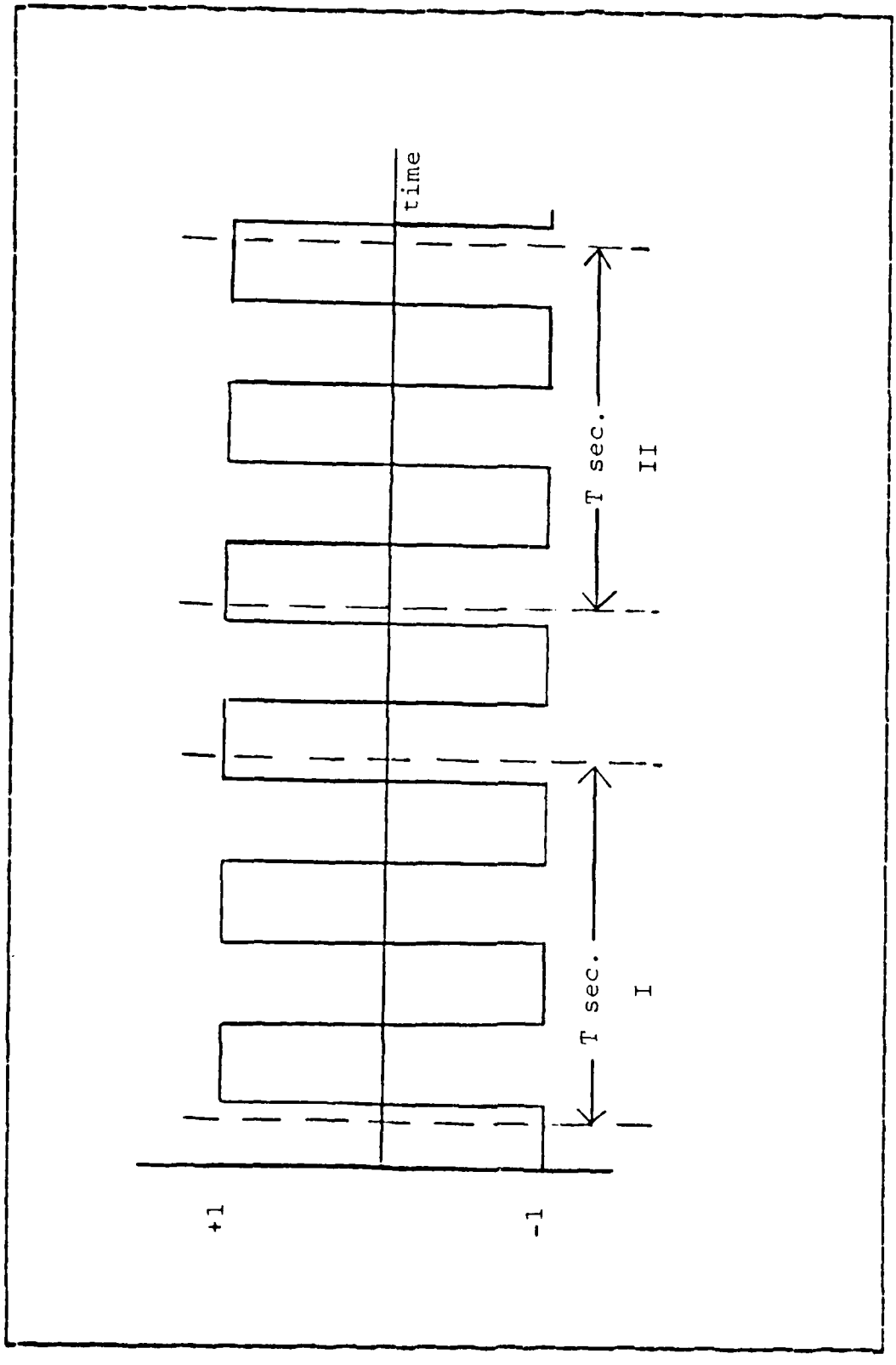

Figure 2.1 Zero Crossings/Window Relationship.

Excepting noise, the degradations to frequency accuracy are a function of the accuracy of the clocks in the circuit. To reduce the effects of noise and introduce frequency divison as a method of improving frequency accuracy, use of a phase locked loop as the keystone of an experimental circuit is considered.

It is well known that a phase locked loop as shown in Fig.2.2(a) will frequency lock to a tone input provided that the rest frequency R of the voltage controlled oscillator (VCO) in the phase locked loop is close to the frequency F of the applied tone; that is, if the frequency of the tone is within the capture range of the phase locked loop. Once in lock, the frequency of the VCO differs from the frequency of the tone by less than one Hertz for high signal to noise ratios. Measuring the frequency of the VCO indirectly measures the frequency of the tone. The accuracy of measurement remains limited to $\pm(1/T)$ HZ using a frequency counter.

A frequency divider is a device which divides the frequency, F, of a square wave at its input and produces a square wave of frequency (F/N) at its output where N is an integer.

As illustrated in Fig.2.2(b), a divide by N frequency divider inserted into the feedback loop of a phase locked loop requires that the rest frequency R of the VCO be multiplied by N for lock on to occur on a square wave of frequency F. Measuring the frequency of the VCO again indirectly measures the frequency F of the square wave; however, since the VCO frequency is now FN, the accuracy of measurement is limited to $\pm(1/NT)$ HZ. This improves the original limitation of measurement accuracy, (1/T), by a factor of N.

This experiment verifies the reasoning above and determines the practical limitations of using a phase locked loop and frequency divider combination as a basis for the accurate measurement of the frequency of a tone of short

is noted that the maximum gate time (10 seconds) is selected on both frequency counters to achieve an accuracy of tenths of a Hertz for the measurements. The data is recorded in Appendix C and a graph of the results is shown in Fig 4.1.

The frequency measurement circuit demonstrates a threshold effect as it measures the 100 kHZ signal to within plus or minus one Hertz for a SNR above four decibels (dB) and quickly loses accuracy below that value of SNR.

D. MEASURING THE FREQUENCY OF A TONE OF SHORT DURATION

No modifications of the circuit of Fig.3.2 are required for this part of the experiment. Frequency counter #1 measures the output of the WAVETEK 136 which is set to approximately 97,700 HZ to match the center frequency of the bandpass filter. Each time the manual switch is closed, frequency counter #2 counts the number of pulses produced by the phase locked loop VCO in 40 milliseconds. It is noted that use of the DATA PRECISION 5740 counter in the counting mode requires that the trigger level of this device be finely adjusted to obtain consistent results.

Frequency counter #2 is accurate to within ±1 count which converts to a ±25 HZ accuracy when measuring a 100 kHZ square wave using a 40 millisecond gate.

The variation in the frequency measured by frequency counter #2 with the input signal frequency constant and as the noise level is incrementally increased is recorded in Appendix D. A plot of the standard deviation of this frequency versus SNR is shown in Fig.4.2 and suggests that the noise has no measurable effect until below a SNR of 6dB. This roughly correlates with the four dB SNR threshold effect observed earlier. However, since the counter's accuracy of ±1 count in 40 milliseconds reflects only an accuracy of ±25 HZ, a more accurate measuring system is required

critical to ensure that the measurement of the frequency output of the phase locked loop commences after the phase locked loop has firmly locked on the signal frequency within the pulse envelope. Lock on time is determined by measuring the settling time of the direct current (DC) output of the lowpass filter of the phase locked loop. To facilitate measurement of this settling time with the oscilloscope, the signal applied to the bandpass filter is modified to be an 80 percent duty cycle, 10 millisecond period pulse modulated 100 kHZ square wave. Lock on time is measured on the oscilloscope as the width of the DC transient response to this waveform. Lock on times for different lowpass filter cutoff frequencies are determined by varying the value of the filter resistor and this data is recorded in Appendix B. The lock on times vary from three to four milliseconds as the filter cutoff frequency varies from 3 HZ to 159 HZ. The effect of noise on the duration of lock on time is observed to be insignificant.

A lowpass filter with cutoff frequency of 80 HZ is selected for the final circuit design. Three milliseconds delay is required. Final design of the counter circuits results in a ten millisecond delay of the 40 millisecond gate, more than adequately accounting for the delay time required.

C. MEASURING THE FREQUENCY OF A TONE

The signal generator of Fig.3.2 is modified to produce a 100 kHZ square wave (no modulation). The frequency of the phase locked loop is measured directly at the output of the WAVETEK 142 voltage contolled oscillator (VCO). The magnitude of the difference between the frequency outputs of the WAVETEK 136 signal generator and of the WAVETEK 142 VCO is measured as the noise level is incrementally increased. It

IV. EXPERIMENTAL PROCEDURE

A. GENERAL

The goal of the experiment is to determine how accurately one can measure the frequency of a tone of short duration that is corrupted by bandlimited white noise using a phase locked loop as a frequency measuring device.

The experiment is conducted in several steps. To provide for proper synchronization in the experimental circuit the settling time (i.e. lock on time) of the phase locked loop is first determined. An unmodulated 100 kHZ square wave is used as the source signal and the frequency of the phase locked loop VCO output is measured as the noise levels are incrementally increased. This provides a benchmark with which to compare the accuracy of the frequency measuring circuit when excited by a pulsed 100 kHZ square wave. A pulsed 100 kHZ square wave is used as the source signal and the frequency output of the phase locked loop is measured as the noise levels are incrementally increased. A frequency divider is inserted into the feedback path of the phase locked loop to determine its effect on the frequency measuring accuracy of the circuit. Lastly, a very stable clock replaces a less stable clock in the circuit to improve the stability of the timing gate and the frequency measuring accuracy of the circuit with the frequency divider.

The details of the procedures and results of each step of the experiment are now examined.

B. PHASE LOCKED LOOP LOCK ON TIME

For the case of a pulse modulated 100 kHZ square wave, determination of the phase locked loop lock on time is

counter #1 is connected to the output of the WAVETEK 136 signal generator to measure the frequency of the 100 kHZ square wave. Frequency counter #2 is connected to the output of the analog switch and is used to count the number of pulses contained within the synchronized 40 millisecond gate time and thereby indirectly determine the frequency of the phase locked loop output.

G. CIRCUIT MODIFICATIONS

During the course of the experiment several minor modifications to the circuit described above are required to obtain necessary data. For example, at one point an unmodulated square wave with no noise is used with frequency counter #2 connected to the cutput of the phase locked loop's VCO to determine how accurately the circuit measures the frequency of that particular waveform. When modifications are required to the circuit, they are explicitly stated in the course of the discussion.

millisecond square wave of frequency 100 KHZ. A manual switch initiates a 90 millisecond one shot as depicted by line E of Fig. 3.3. The 90 millisecond one shot is then logically ANDED with an inversion of the trigger as shown in line F of Fig. 3.3. This inverted trigger is inverted again and used to trigger a 60 millisecond one shot as depicted by lines G and H of Fig. 3.3. The 60 millisecond one shot is then logically ANDED with the 40 millisecond counter to produce a 40 millisecond timing gate as shown in line I of Fig. 3.3. A precise gate of 40 milliseconds is now available at the correct time to achieve the objective of synchronization. An additional circuit not shown in Fig. 3.2 is a four millisecond one shot initiated by the trigger of Fig. 3.2. This one shot provides an "automatic" manual switching capability to facilitate oscilloscope observations. This is accomplished by bypassing the manual switch of figure 3.2 and feeding the output of the four millisecond one shot to the input of the 90 millisecond one shot, thereby providing a closed switch once every 104 milliseconds.

5. Analog Switch

The output of the phase locked loop and the 40 millisecond gate are then applied to the analog switch. The output of the analog switch is the desired 40 millisecond "slice" from the "interior" of the 54 millisecond square wave of frequency 100 kHZ.

F. FREQUENCY MEASUREMENT

Two DATA PRECISION 5740 frequency counters are used to compare the frequency of the signal not corrupted by noise with the frequency measured by the frequency recovery circuit under various levels of noise power. Frequency

follows the instantaneous frequency of a signal at the input of the phase locked loop. It is the frequency of the VCO that is measured and equated to the the frequency of the noisy system input.

B. SYNCHRONIZED GATING CIRCUIT

The purpose of this subsystem is to provide a precise gate time of 40 milliseconds at the proper time.

1. Envelope Detector

The envelope detector recovers the 54 millisecond envelope of the output of the signal generator. This envelope is shown as line B of Fig. 3.3.

2. Trigger

A trigger initiated by the leading edge of the recovered envelope is produced to provide a common reference time for the synchronization of a 40 millisecond counter and a manual switch. This trigger is shown in line C of Fig. 3.3.

3. 40 Millisecond Counter

A four stage digital counter provides a precise timing gate of 40 milliseconds. As shown in line D of figure 3.3, the trigger initiates a 40 millisecond pulse from the counter approximately 10 milliseconds after the trigger time T.

4. Monostable Multivibrators

Several monostable multivibrators (one shots) are required to achieve synchronous operation of the experiment. The objective of this synchronization is to select a 40 millisecond "slice" from the "interior" of the 54

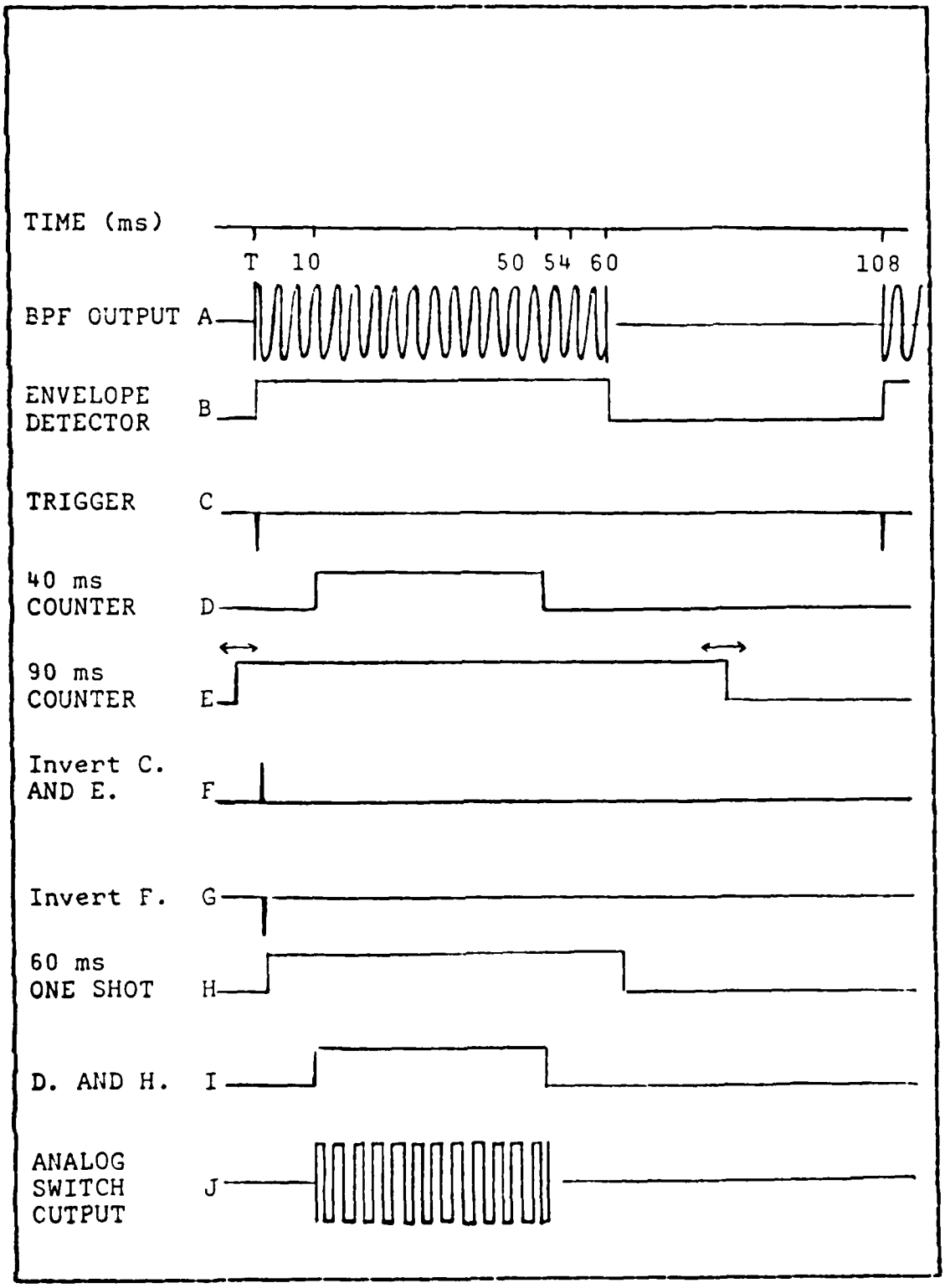

Figure 3.3 Synchronization of Gate Time Timing Diagram.

3. Summer

A simple operational amplifier summer is used to add the signal to the noise prior to bandpass filtering.

C. BANDPASS FILTER

A fourth order Chebyshev biquadratic bandpass filter with a center frequency of approximately 100 kHZ and a 3dB bandwidth of 9 kHZ provides the desired simulation of band-limited signal plus narrowband noise. This filtering of signal plus noise is similar to that of the IF amplifier/filter portion of a superheterodyne radio receiver. The ouput of this filter with no noise at the input is depicted in line A of Fig.3.3.

D. FREQUENCY RECOVERY CIRCUIT

The purpose of this subsystem is to recover the frequency of the sine wave within the pulse envelope.

1. Voltage Limiter/Rectifier

To ensure that the input to the digital multiplier used in the phase locked loop is transistor-transistor logic (TTL) compatible, a voltage limiter/rectifier transforms the 100 kHZ sinusoidal pulse out of the band pass filter to a pulsed 100 kHZ DC biased square wave having amplitudes of 5 volts and 0 volts.

2. Phase Locked Loop

The three blocks in Fig. 3.2 immediately following the voltage limiter/rectifier comprise a phase locked loop. The phase locked loop consists of a digital multiplier, a simple RC lowpass filter, and a voltage controlled oscillator (VCO). The frequency output of the VCO closely

The parts of the five functional subsystems are shown in Fig. 3.2. Key outputs are labeled with capital letters and correspond letter for letter to the waveforms depicted in Fig.3.3. The circuits that make up each part are described in detail in Appendix A. The purpose of each part is presented in this chapter.

B. SIGNAL PLUS NOISE GENERATOR.

The purpose of this subsystem is to add noise to various test signals applied to the experimental circuit.

1. Signal Generator

The desired output of the signal generator is a portion of a square wave. First, a WAVETEK 136 signal generator is used to provide a symmetric square wave of approximately 100 kHZ. It is to be noted that a pure sinusoid tone of the same frequency is not used because the DATA PRECISION 5740 frequency counter more reliably measures the frequency of a square wave. However, since the square wave pulse is to be later passed through a bandpass filter, the output of which is a sine wave pulse, use of the square wave has no detrimental effect on the experiment. A fifty percent duty cycle pulse generator produces 54 millisecond pulses. These and the 100 kHZ symmetric square wave are multiplied using an analog voltage multiplier to generate 54 millisecond pulses of a 100 kHZ square wave.

2. Noise Generator

An ELGENCO noise generator with a selected bandwidth of 500 kHZ is used to provide the various noise levels required.

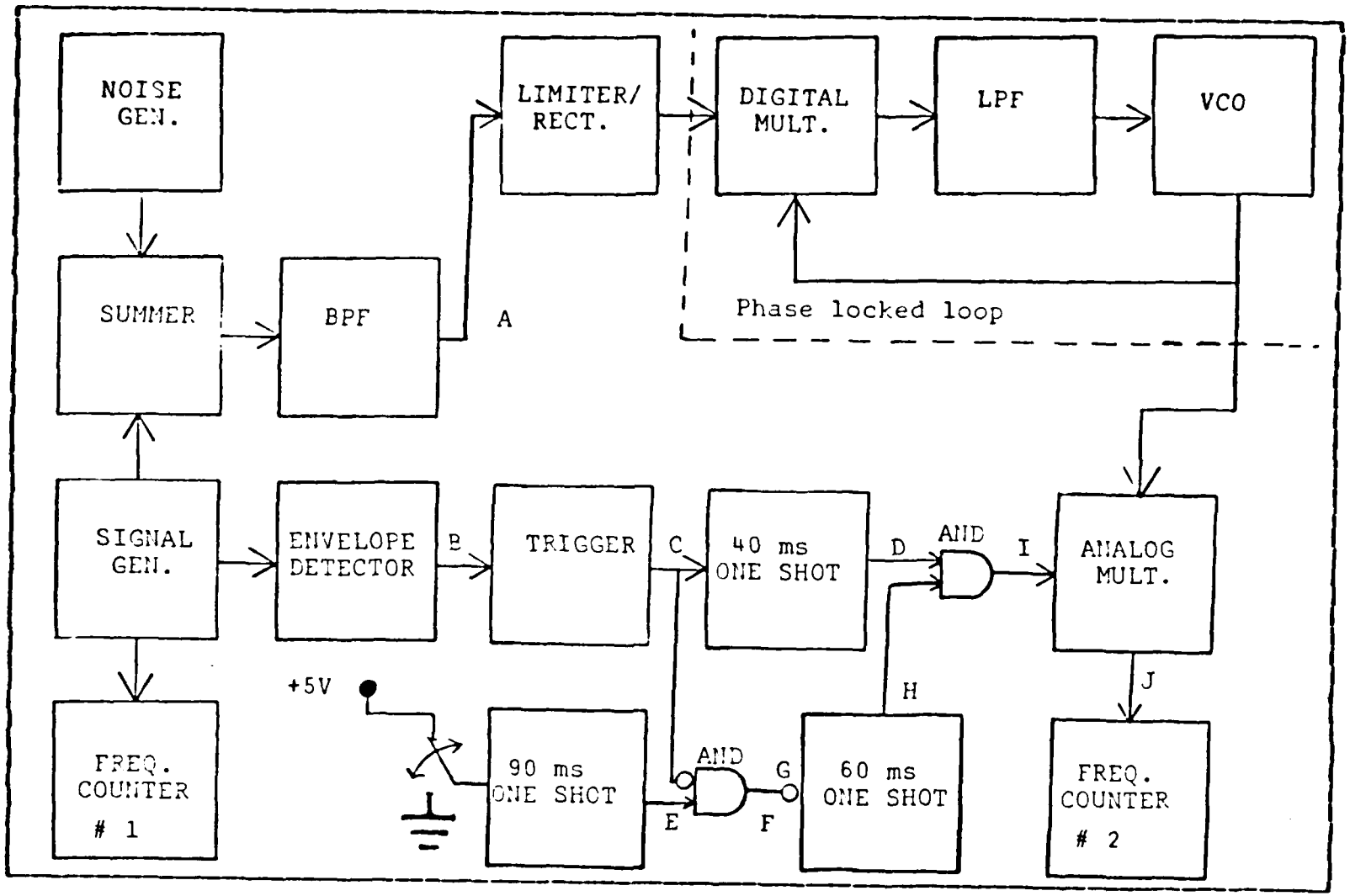

Figure 3.2 Circuit Block Diagram.

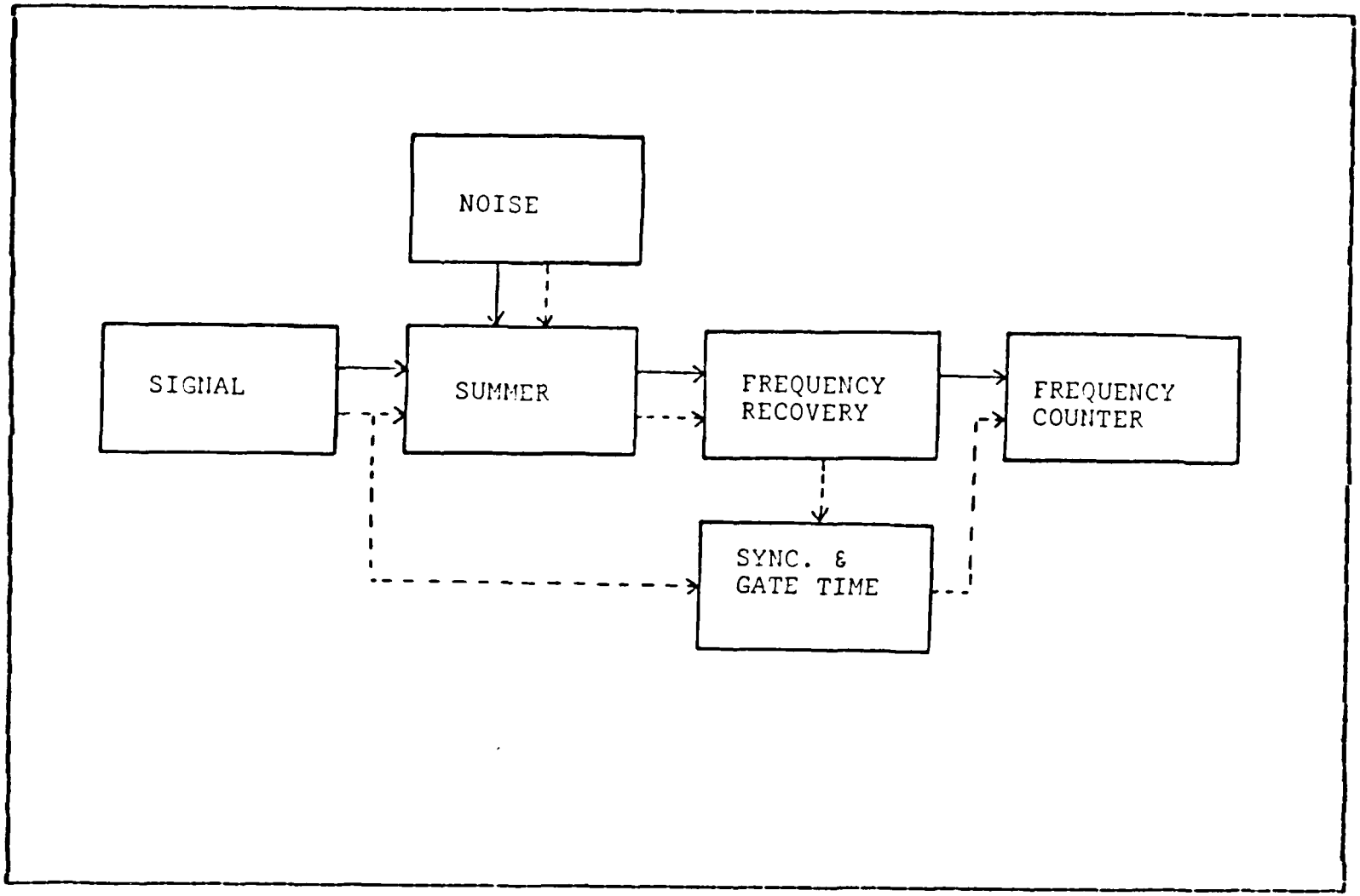

Figure 3.1 Ciruit Concept.

III. EXPERIMENTAL CIRCUIT

A. GENERAL

The general concept of the experimental circuit is shown in Fig.3.1. It consists of a summer to add a signal, either a tone or a pulsed tone, to noise; a frequency recovery circuit to recover the the frequency of the noisy signal; and a counter to measure the frequency of the noisy signal. In the case of the pulsed tone, a synchronization and gate time circuit is also required to enable the frequency counter to measure the number of zero crossings of the tone being pulsed. The two cases are distinguished in Fig.3.1 by using a solid line for the case of a tone and a dashed line for the case of a pulsed tone.

Fig. 3.2 is a block diagram of the system used in this project to realize the concept described above. The overall system basically consists of five functional subsystems:

- -A signal plus noise subsystem to simulate the reception from a channel of a short duration tone corrupted by noise.
- -A bandpass filter to reduce the noise bandwidth and improve the signal to noise ratio. This filter simulates the intermediate frequency (IF) amplifier/filter stage of a superheterodyne receiver.
- -A frequency recovery circuit to determine the frequency of the short duration tone.
- -A synchronized gating circuit to provide a precise gating time needed to accurately measure the frequency of the phase locked loop output.
- -Frequency counters to collect data.

duration. Theoretically, any desired frequency accuracy, $\pm(1/NT)$ HZ, can be achieved by simply increasing the value N of frequency division by the approriate amount. Practically, the conclusions of this experiment show that the tradeoff for increased frequency accuracy is a higher required signal to noise ratio and a reduction of the frequency capture range of the phase locked loop.

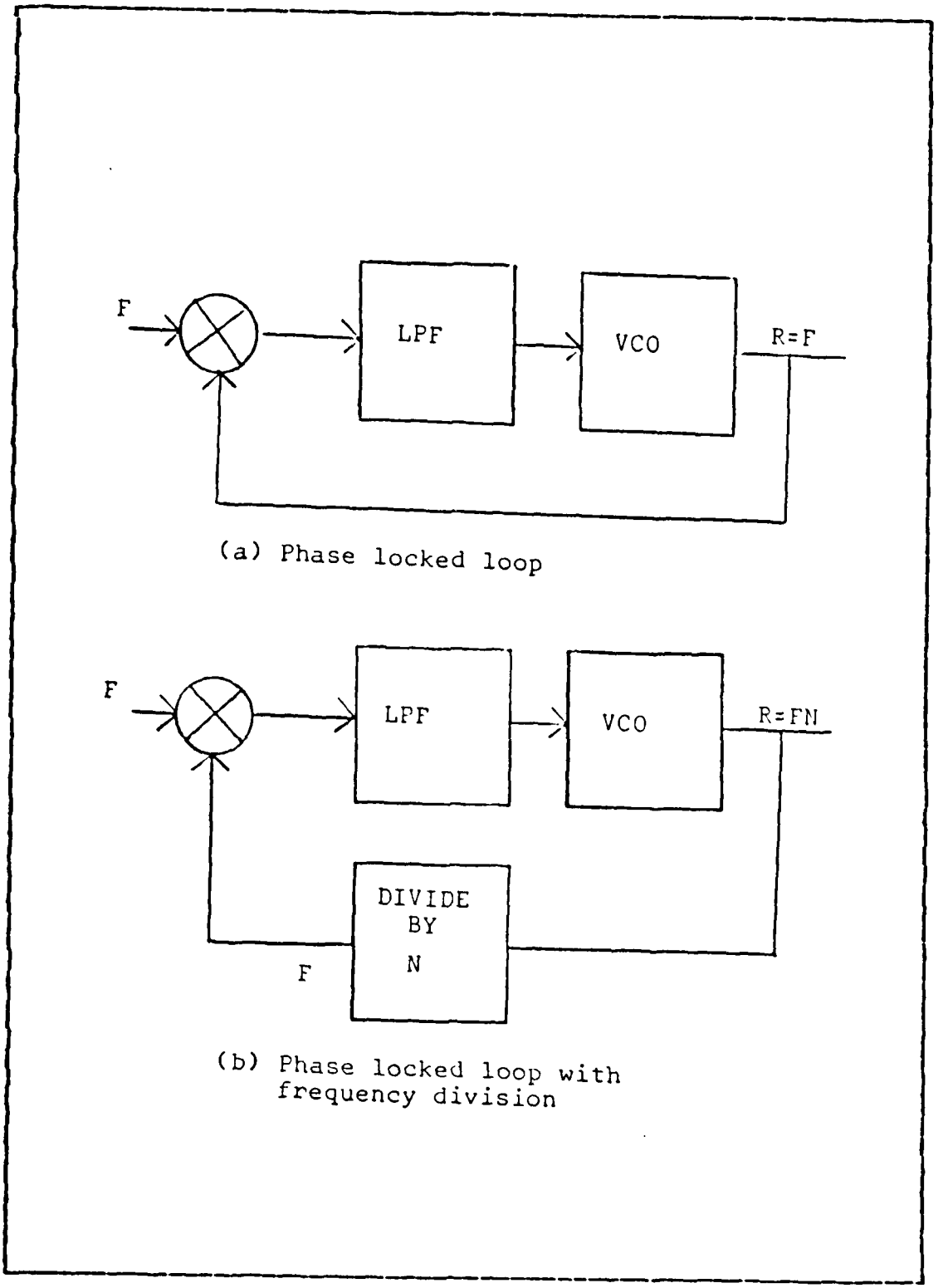

Figure 2.2 Phase Locked Loop Configurations.

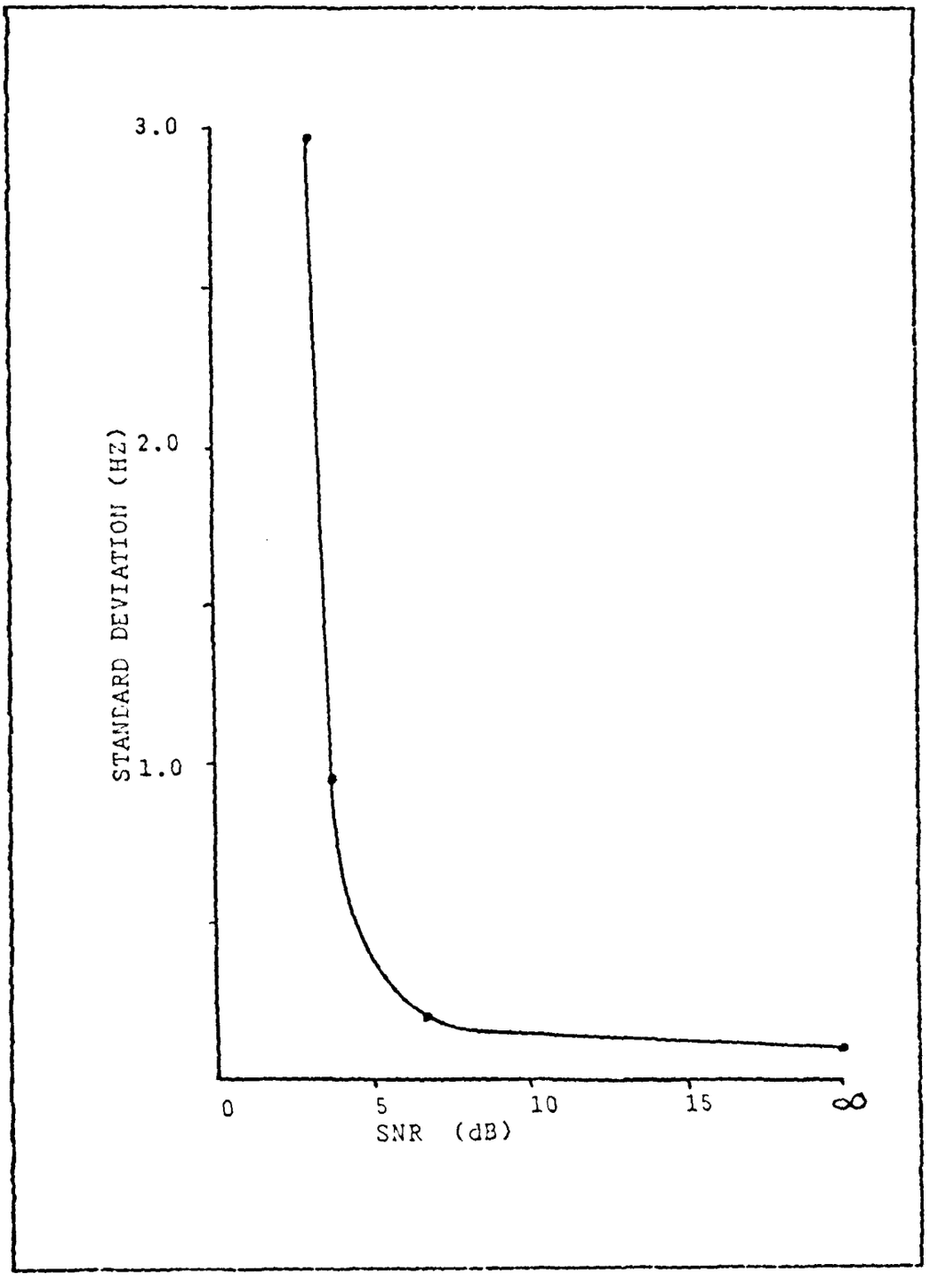

Figure 4.1 Frequency Deviation of a Tone.

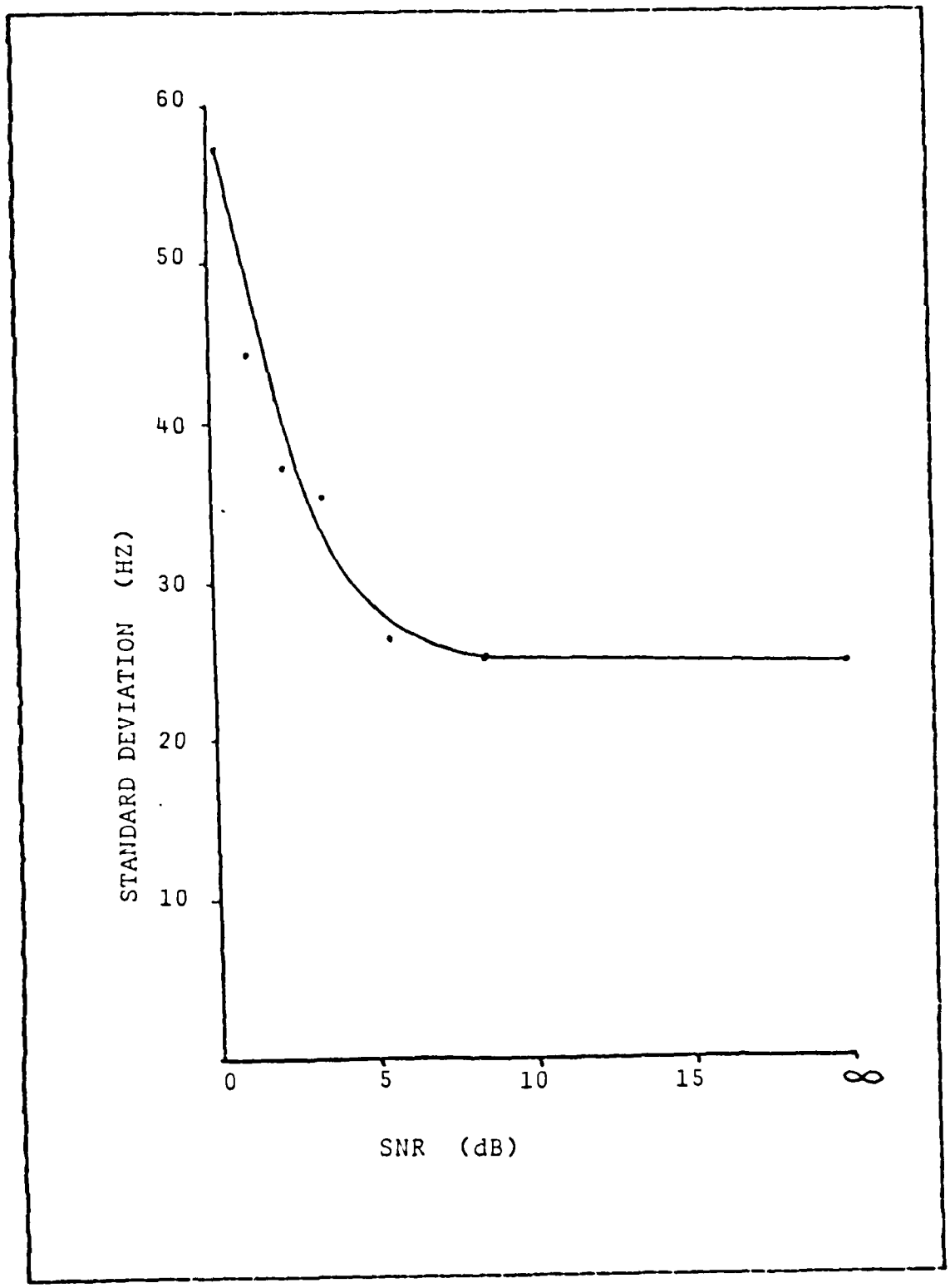

Figure 4.2 Frequency Deviation of a Pulsed Tone.

to investigate the effect of the noise above a SNR of six dB.

E. EFFECT OF A FREQUENCY DIVIDER IN THE PLL FEEDBACK LOOP

A frequency divider is now inserted into the feedback loop of the phase locked loop of Fig.3.2. to increase the frequency of the VCO. The value of the divisor of the frequency divider requires that the rest frequency of the VCO be multiplied by the same value to insure that the signal frequency and the feedback loop frequency are close enough to achieve lock on.

The procedures outlined in paragraph C for the measurement of a pure tone, after being modified slightly by connecting frequency counter #2 to the output of the frequency divider vice the output of the VCO, are repeated for this new configuration. The data for a divide by 40 and a divide by 20 frequency divider inserted into the circuit are recorded in Appendix E and plotted in Fig.4.3. A 7dB SNR is required for a ± 1 HZ measurement accuracy when using a divide by 20 frequency divider. At least 12dB SNR is required for the same performance when using a divide by 40 frequency divider. Use of greater frequency division increases the SNR required to achieve the same accuracy and reduces the frequency capture range of the phase locked loop.

The procedures outlined in paragraph D for measuring the frequency of a tone of short duration are repeated for the circuit with a divide by 20 frequency divider in the circuit and the data is recorded in Appendix F.
In this case the ±1 count accuracy of frequency counter #2 converts to a ±1.25 HZ accuracy when measuring a 100 kHZ square wave using a 40 millisecond gate. The data of Appendix F shows that at even at a very high signal to noise

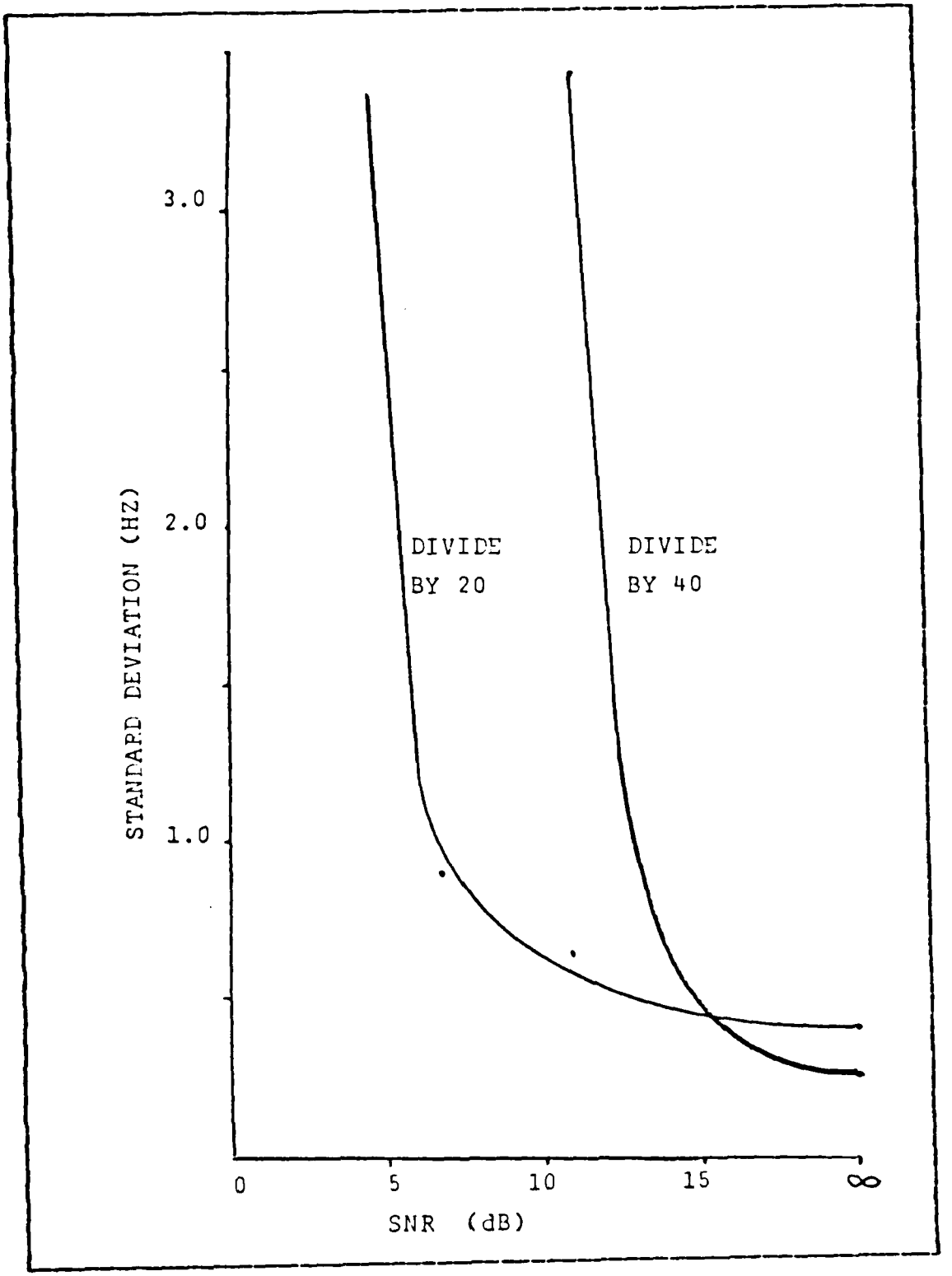

Figure 4.3 Frequency Deviation of a Tone using Division.

ratio, this configuration is not capable of enhancing the performance of the circuit unless the stability of the various clocking systems supporting the circuit is significantly improved.

The relatively unstable WAVETEK 142 providing the 100 kHZ clock to the four stage counter producing the timing gate is replaced with a HP 3320B frequency synthesizer having a stability of ± 10 parts in one million of setting per year. The 100 kHZ sinusicd output of the HP 3320B is made TTL compatible by passing it through a voltage limiter/ rectifier (identical to the one described in Appendix A) followed by a 7404 inverter.

Using the new clock, the measurements of the tone of short duration are repeated with a divide by 20 frequency divider in the circuit and recorded in Appendix G. The improved clock produces a more stable timing gate which results in a standard deviation of 15 HZ for a SNR above 7dB, 10 HZ less than the best standard deviation achievable by the experimental circuit without the frequency divider at any SNR.

V. CONCLUSIONS

Fig.5.1 consolidates the experimental results of measuring the frequency of a steady tone using a phase locked loop with and without a frequency divider inserted into the feedback loop. The effects of frequency division on the experimental circuit's ability to faithfully recover the frequency of a steady tone are:

- Frequency division increases the value of SNR at which the threshold of the phase locked loop occurs and reduces the capture range of the phase locked loop.
- The standard deviation of the circuit with frequency division is always higher than the standard deviation of the circuit without frequency division at the same value of SNR due to the increased sensitivity of the loop when a frequency divider is present.

Fig.5.2 consolidates the experimental results of measuring the frequency of a pulsed tone using a phase locked loop with and without a frequency divider inserted into the feedback loop. The effects of frequency division on the experimental circuit's ability to faithfully recover the frequency of a pulsed tone are:

- The maximum accuracy of frequency measurement possible from a phase locked loop, without a frequency divider, sensing the frequency of a pulsed tone is inversely proportional to the time length of the gated pulse.
- A frequency divider can improve the accuracy of frequency measurement derived from a phase locked loop sensing the frequency of a pulsed tone, provided that the stability of the gate time is not a limiting factor.

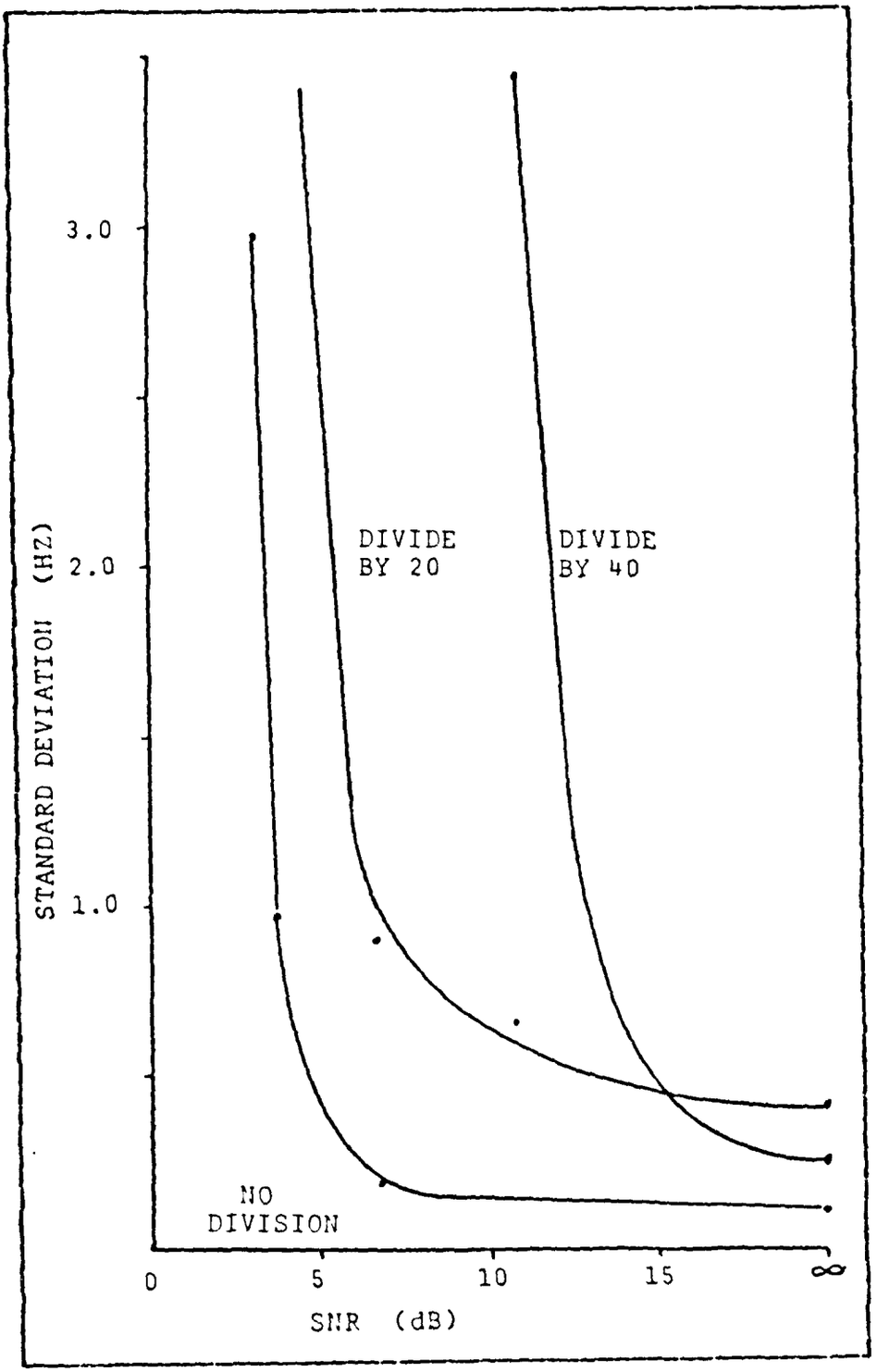

Figure 5.1 Tone Measurements.

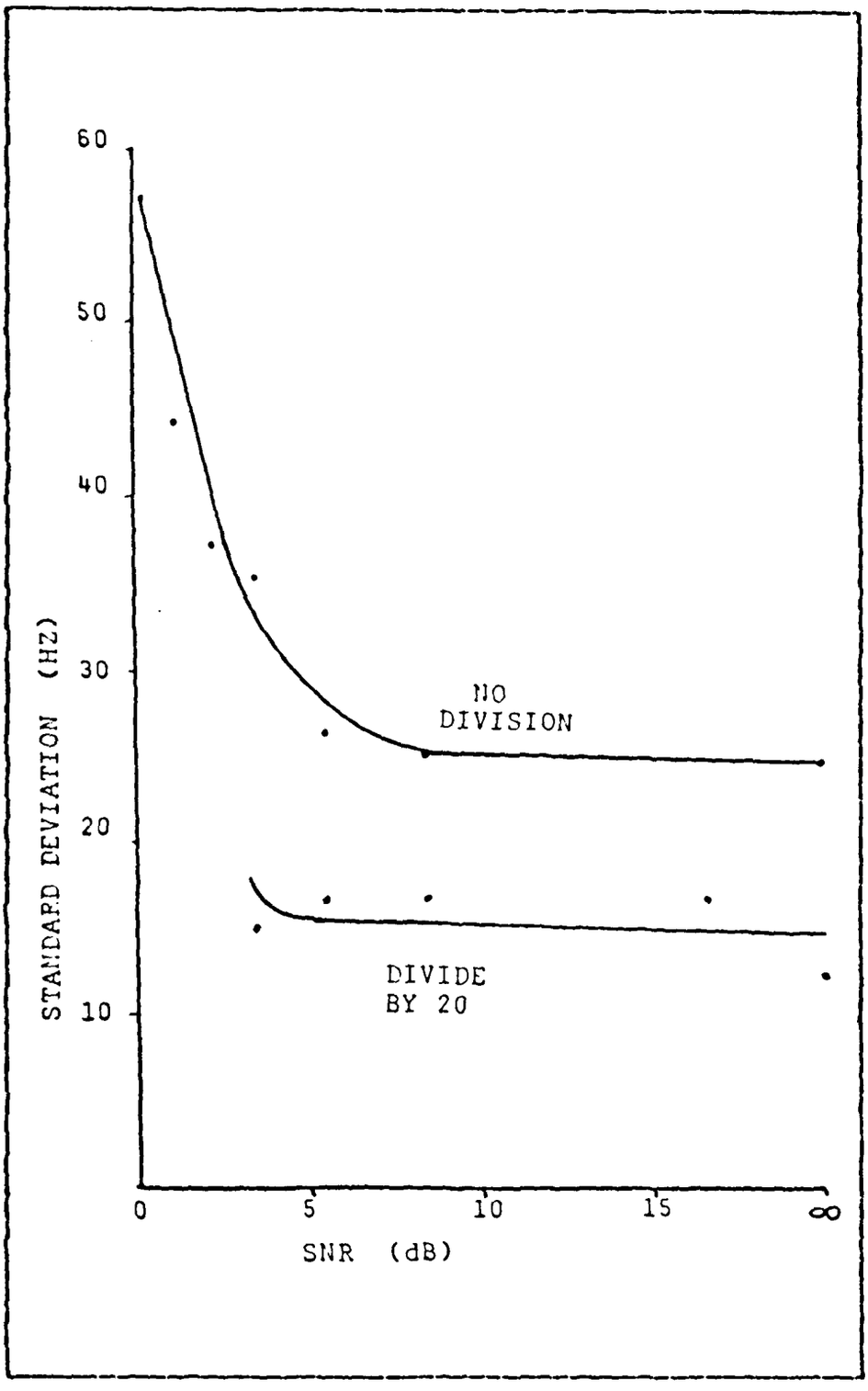

Figure 5.2 Pulsed Tone Measurements.

Finally, it seems reasonable that a phase locked loop with a frequency divider in the feedback loop coupled with a very stable clock to provide a precise and stable gate time can be used to measure the frequency of short duration tone with great accuracy. Assuming that the stability of the clock for the gating circuit is not a limiting factor, the tradeoff for better accuracy using frequency division is a higher required SNR and reduced frequency capture range.

APPENDIX A
CIRCUIT DIAGRAMS

All figures are placed at the end of this appendix. All numerical values for resistors are in units of kilohms and for capacitors in units of micrcfarads. A block diagram of the experimental setup is shown in Fig.3.2 and the circuits comprising each block are now examined in detail.

The signal generator block of Fig.3.2 is to be able to generate three waveforms: a 100 kHZ square wave, a 54 millisecond pulse modulated 100 kHZ square wave, and a 8 millisecond pulse modulated 100 kHZ square wave. Each waveform is depicted (not to scale) in Fig.A.1. The 100 kHZ square wave is obtained directly from a WAVETEK 136 signal generator. The 54 millisecond pulse modulated square wave is produced by mixing the 100 kHZ square wave output of the WAVETEK 136 with 54 millisecond pulses generated by the circuit in Fig.A.2. This circuit is adapted from [Ref.1] and uses a 555 astable multivibrator followed by a 7473 JK level trigger flip flop to produce a 50% duty cycle pulse wave with pulse widths of 54 milliseconds at node A. The 8 millisecond pulse modulated square wave is produced in a similar manner, but an 80% duty cycle pulse wave is obtained from a WAVETEK 142 in this case. Mixing of the two pulse modulated waves is done by the AD534 four quadrant analog multiplier shown in Fig.A.3 where one of the pulse waves is applied to node B and the 100 kHZ square wave is applied to node C to obtain a pulse modulated wave at node D.

The noise generator block represents an ELGENCO Gaussian noise generator with a selected bandwidth of 500 kHZ. To take advantage of the noise power available over a maximum linear range requires that signal levels at the output of

the bandpass filter be selected between 0.2 and 0.5 volts RMS.

Noise is added to the signal using an LM318 operational amplifier summer. To provide an additional measure of buffering before the bandpass filter, an LM310 voltage follower is appended to the summer as shown in Fig.A.4. Signal and noise are applied to node E and F respectively and the buffered sum is produced at node G. For all measurements, the noise generator remains energized and connected to node F. Zero level of noise is selected for a 'no noise' measurement.

The fourth order Chebyshev biquadratic bandpass filter is adapted from [Ref.2]. The filter consists of two stages, each stage constructed as shown in Fig.A.5 using the following resistor values (kilohms):

	STAGE 1	STAGE 2
R1	13	13
R2	18	18
R3	1.5	1.6
R4	1.6	1.6

Signal plus noise is applied to node H of the first stage and the filtered output appears at node I of the second stage. The center frequency, 3dB bandwidth, and gain are measured by observing the output of the filter on a HEWLETT PACKARD 1222A oscilloscope as the frequency of a square wave input is varied. The respective values are 97700 kHZ, 9 kHZ, and 0 dB.

A simple diode resistor rectifier is added to a voltage limiter design found in [Ref.3] to construct the circuit shown in Fig.A.6. The sinusoidal output of the bandpass filter is fed to node J and a train of Transistor-Transistor Logic (TTL) compatible 5 volt amplitude pulses with the same frequency is produced at node K for bandpass filter output

amplitudes ranging from approximately 0.1 volt RMS to over 15 volts RMS.

A phase locked loop consisting of a 7486 digital multiplier (exclusive NOR gate), a simple RC lowpass filter, and a WAVETEK 143 VCO is shown in Fig.A.7. The output of the voltage limiter/rectifier is applied to node L and the output of the VCO is fed back to pin 2 and the product of these two signals is passed through a lowpass filter to produce a DC voltage at node M to drive the VCO. The frequency output of the VCO closely follows the frequency input at node L.

The envelope detector shown in Fig.A.8 detects the envelope of the pulse modulated output of the AD534 mixer. The mixer output is applied to node N and amplified by the adjustable DC offset LM318 operational amplifier (OPAMP); it is then buffered by the LM741 voltage follower and passed to a simple diode and RC lowpass filter which detects the envelope of the signal. The final LM741 OPAMP produces an amplified envelope at node O. The potentiometer in the LM318 OPAMP circuit provides a convenient method for adjusting the peak amplitude of the envelope without having to adjust the magnitudes of the signal inputs to the AD534 mixer. A peak envelope amplitude greater than four volts is required to produce satisfactory trigger pulses.

The envelope is applied to node P of the trigger circuit adapted from [Ref.1] and shown in Fig.A.9. A negative pulse is produced at node Q on the rising edge of the envelope and is used to trigger three monostable multivibrators (one shots): 60 millisecond and 90 millisecond one shots constructed as shown in Fig.A.10 using a dual LM556 timer and a four millisecond one shot using a LM555 timer as shown in Fig.A.11. Circuit designs are adapted from [Ref.1] and [Ref.4]. In Fig.A10 a negative pulse applied to nodes R and S produces 60 and 90 millisecond pulses at nodes T and U

respectively. Similarly, in Fig.A.11 a negative pulse at node V produces a four millisecond pulse at node W.

A block diagram of the four stage 40 millisecond counter is shown in Fig.A.12. The first three stages are 74160 decade counters each of which successively divides the 100 kHZ clock frequency provided by a WAVETEK 142 by 10 to produce a 100 HZ frequency at the 'T' pin of the 74161 binary counter. The four weight(Q4) and eight weight(Q8) outputs of this binary counter are applied to a 7402 NOR gate, producing a 40 millisecond pulse at node X. Fig.A.13 shows the details of the pin connections for each stage of the 40 millisecond counter. The L (load) pin of each stage is connected to the trigger circuit output which resets the counters with each negative pulse. The 'T' enable pin of the first 74160 stage is tied high to 5 volts while the 'T' pins of the remaining stages are connected to the 'C' (carry out) pin of the preceding stage.

The manual switch and the logic circuits required to properly synchronize this switch with the rest of the experimental circuit is shown in Fig.A.14. The negative pulses produced by the trigger circuit are inverted using a 7404 gate and applied to node Y. The 40 millisecond pulse output of the counter is applied to node Z. Throwing the manual switch from +5 volts to ground triggers the 90 millisecond one shot and its output is logically ANDED with the positive trigger pulse at node Y, reproducing this positive trigger pulse at the output of the 7408 gate. This positive trigger pulse is inverted by the 7404 gate and triggers the 60 millisecond one shot, the output of which is logically ANDED with the 40 millisecond pulse at node Z, reproducing the 40 millisecond pulse at node AA. This logical design synchronizes the manual switch with the common basis of synchronization for the rest of the experimental circuit, the trigger circuit.

The 40 millisecond pulse prcduced by closing the manual switch is applied to node AB of the MC14051B analog switch shown in Fig.A.15. The output of the phase locked loop VCO is applied to node AC. The ouput, a 40 millisecond slice of the output of the VCO, appears at node AD after passing through a DC blocking capacitcr. A DATA PRECISION 5740 frequency counter is now used to count the pulses at node AD during the 40 milliseconds time interval.

When required during the course of the experiment, the frequency divider shown in Fig.A.16 is inserted into the phase locked loop feedback line to increase the required rest frequency F of the VCO. The output of the VCO at frequency F is applied to node AE. A train of pulses at frequency F/20 or F/40 is generated at V20 or V40 respectively by the decade-binary ccunter combination. One of these two outputs is then applied to the digital multiplier to complete the phase lock loop again. Note that the original rest frequency of the VCO now must be multiplied by 20 if V20 is selected and by 40 if V40 is selected to ensure lock on by the phase locked loop.

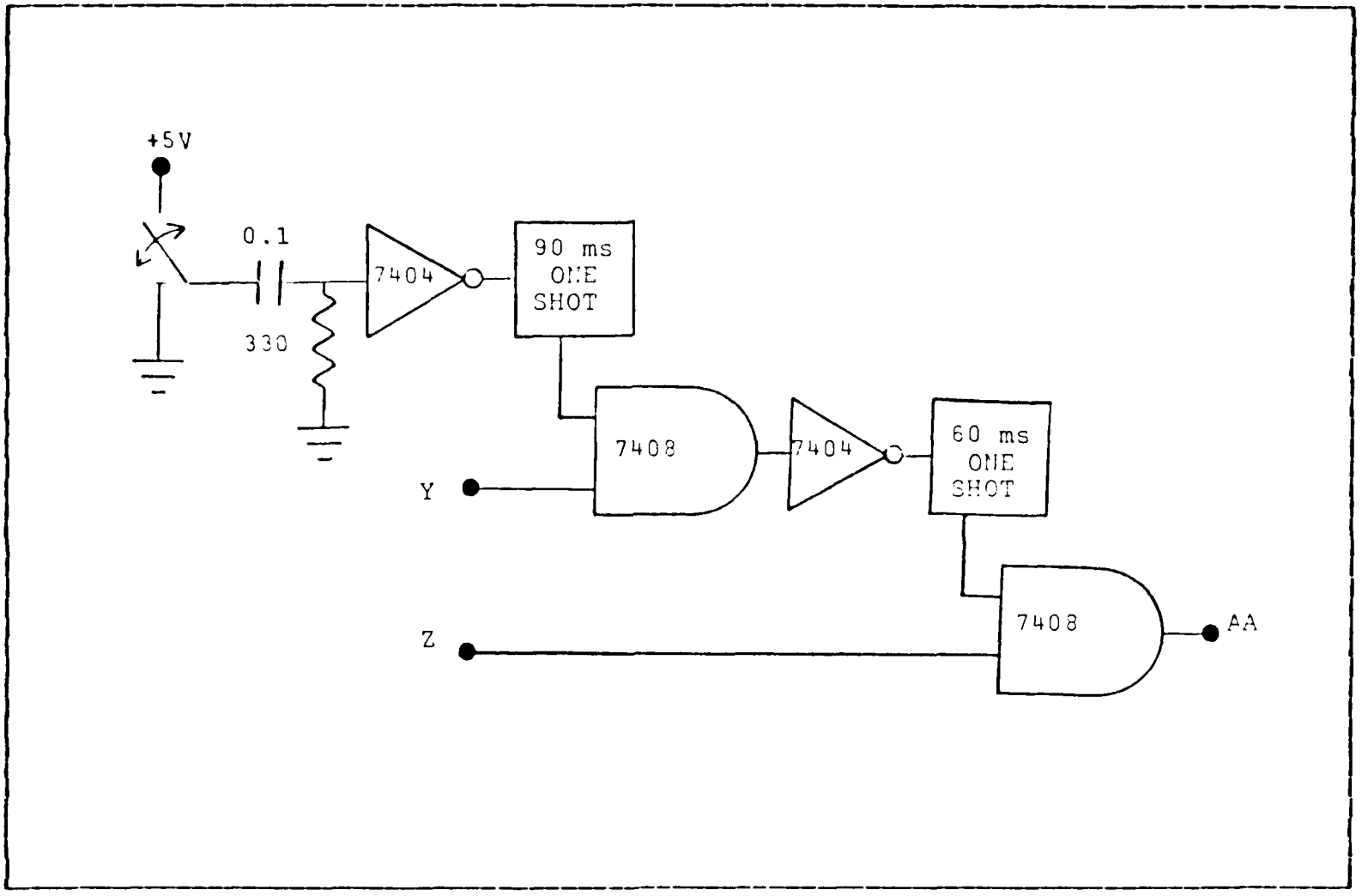

Figure A.14 Manual Switch Interface.

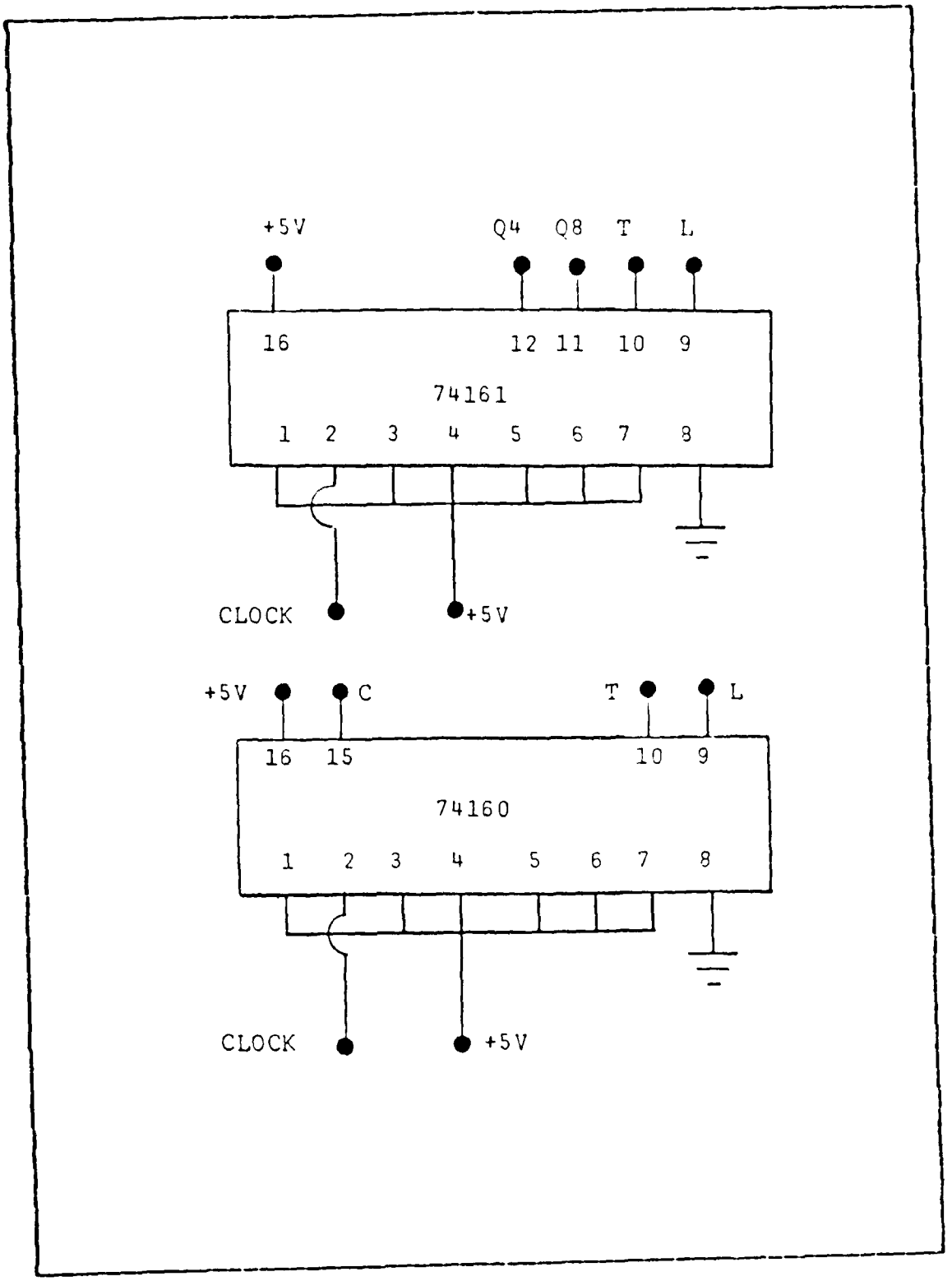

Figure A.13 Binary and Decade Counters.

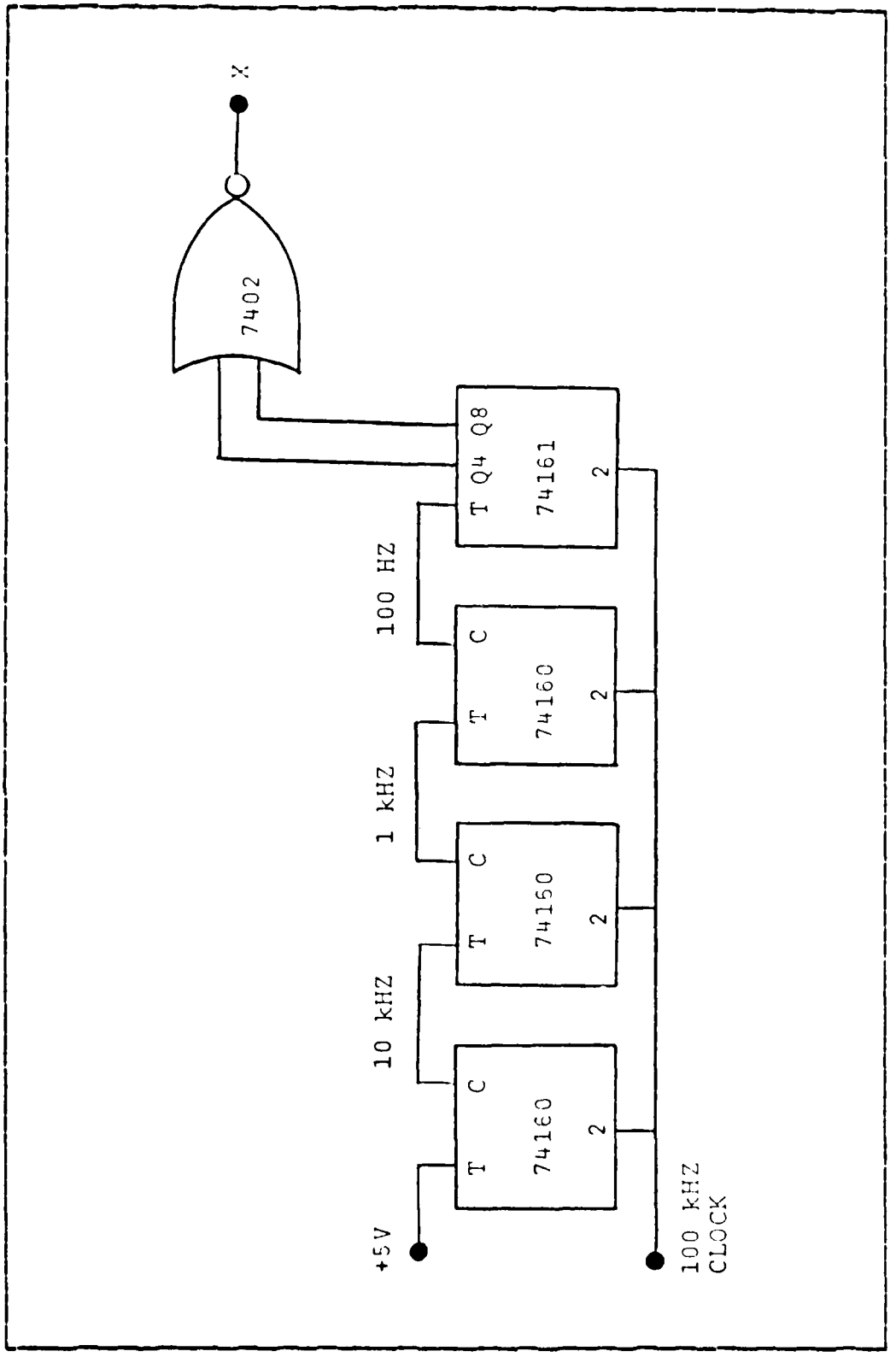

Figure A.12 40 msec Gate.

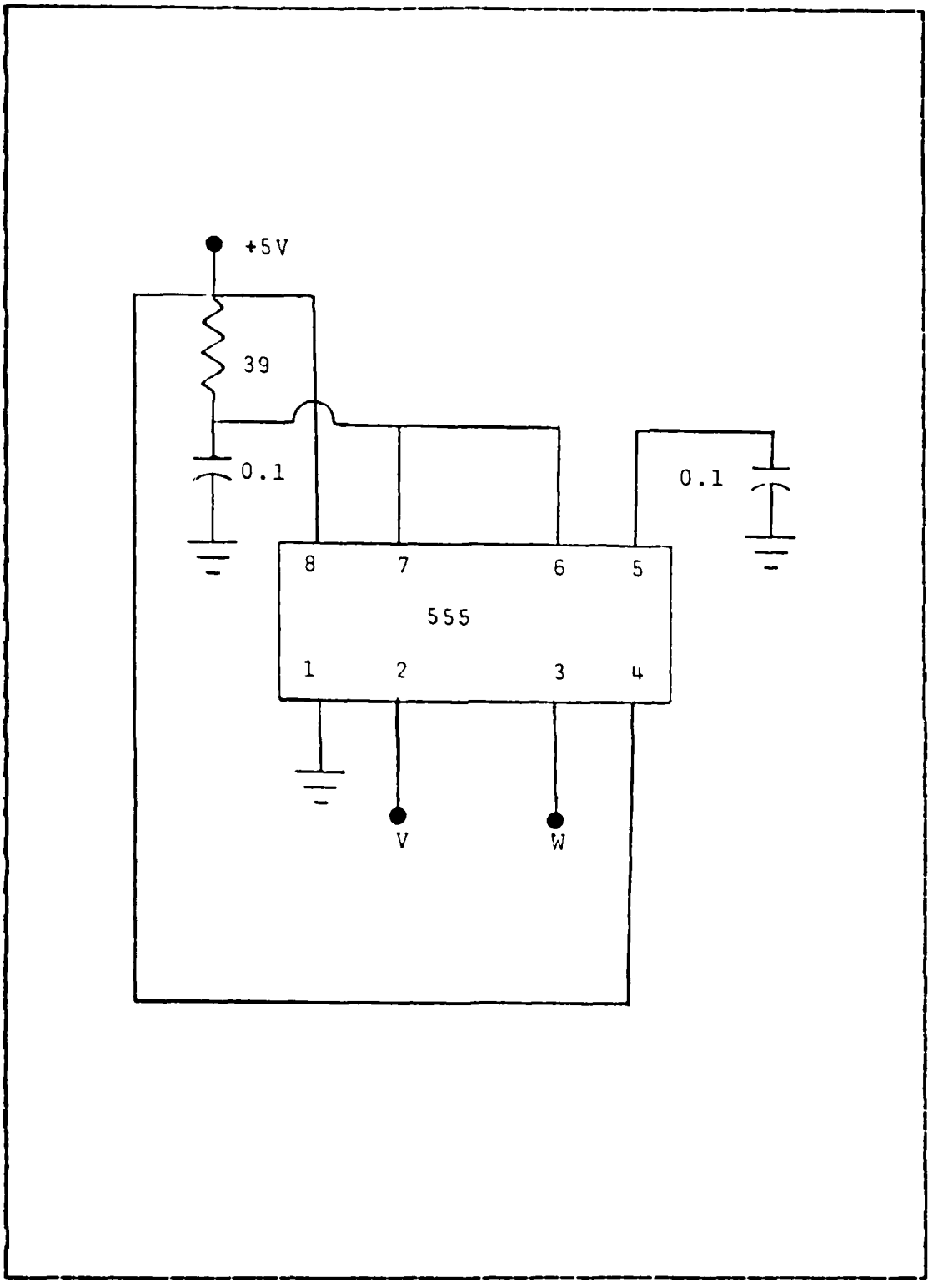

Figure A.11 4 msec One Shot.

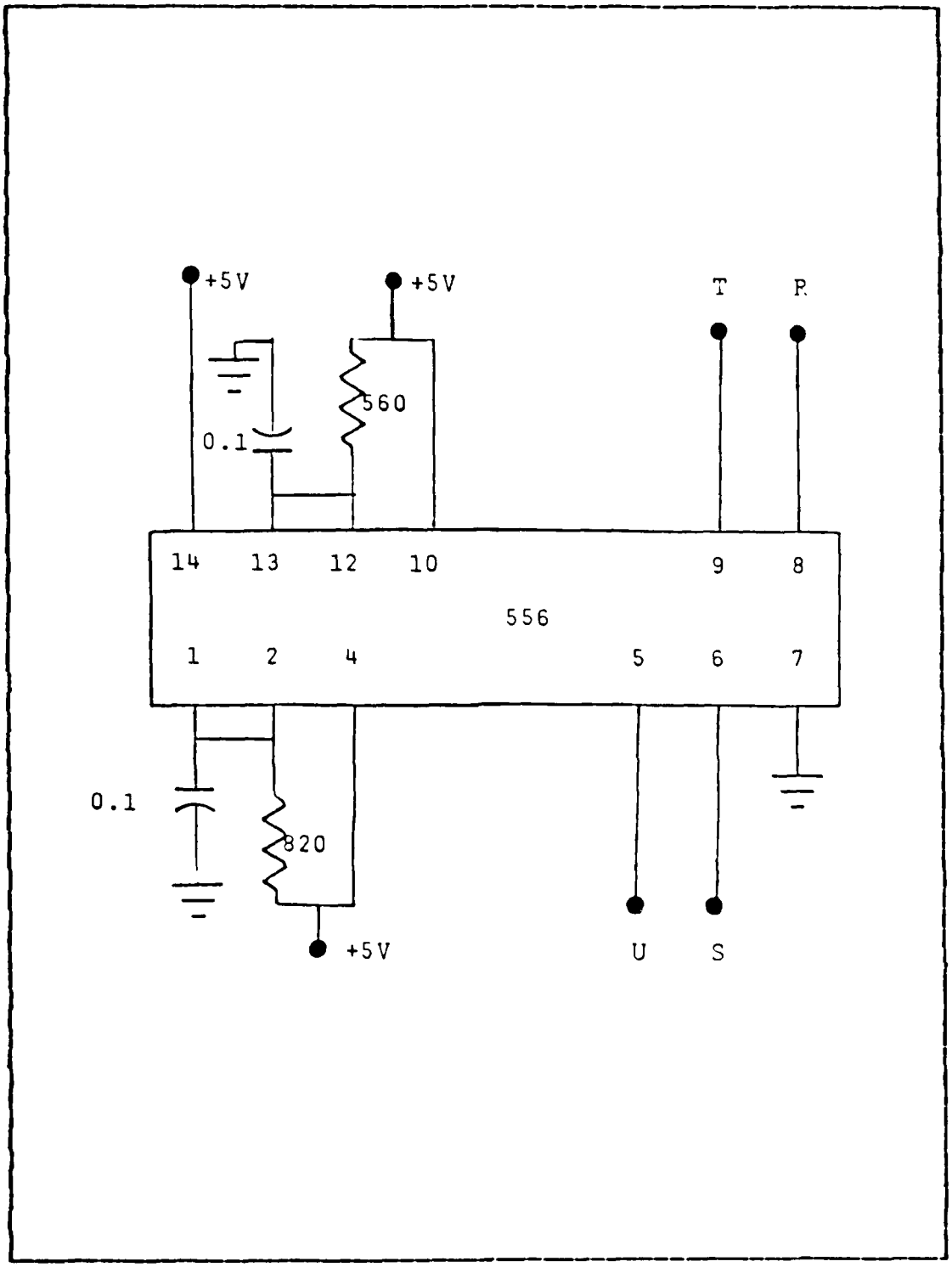

Figure A.10 60 and 90 msec One Shots.

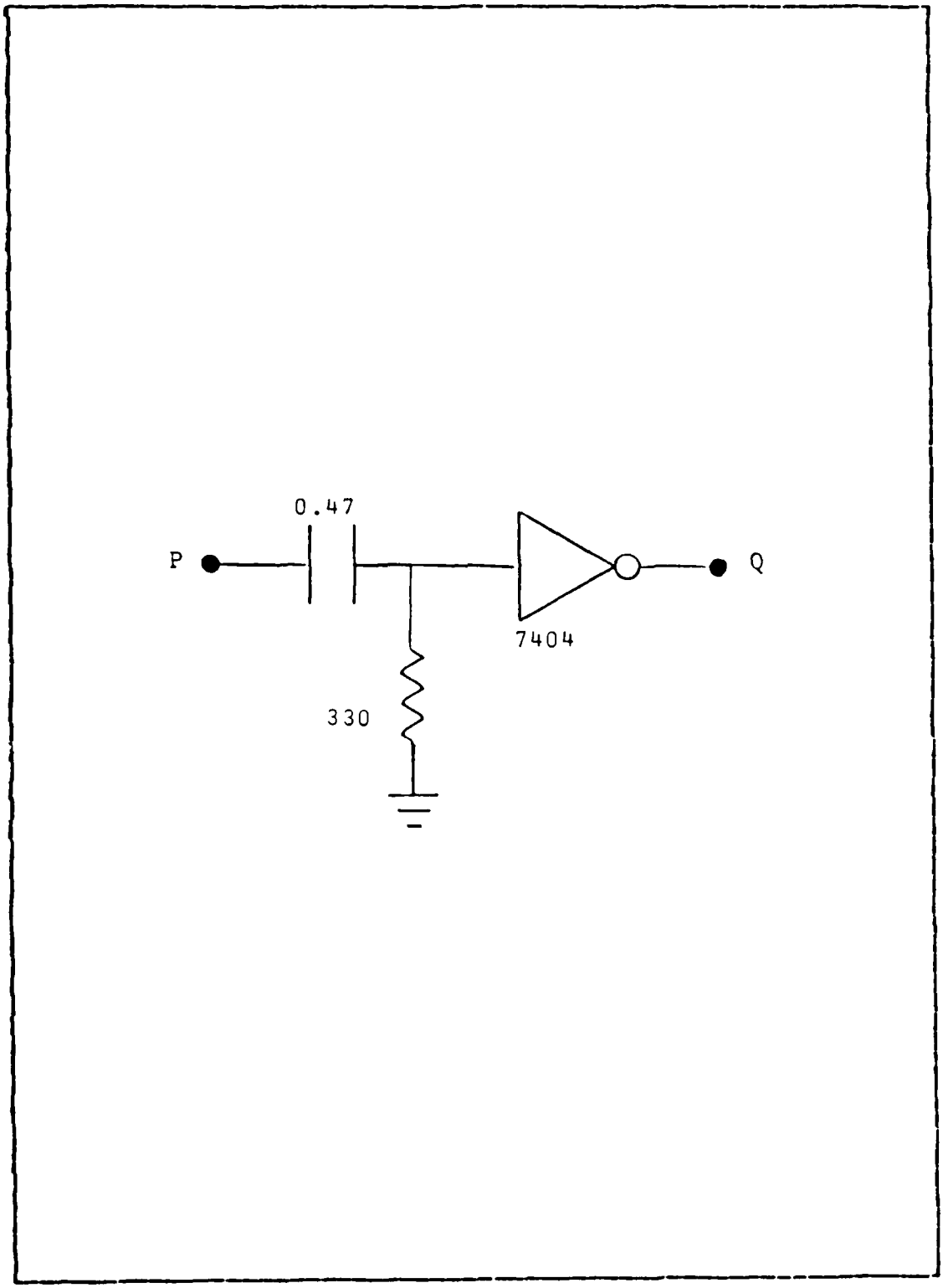

Figure A.9 Trigger Pulse Generator.

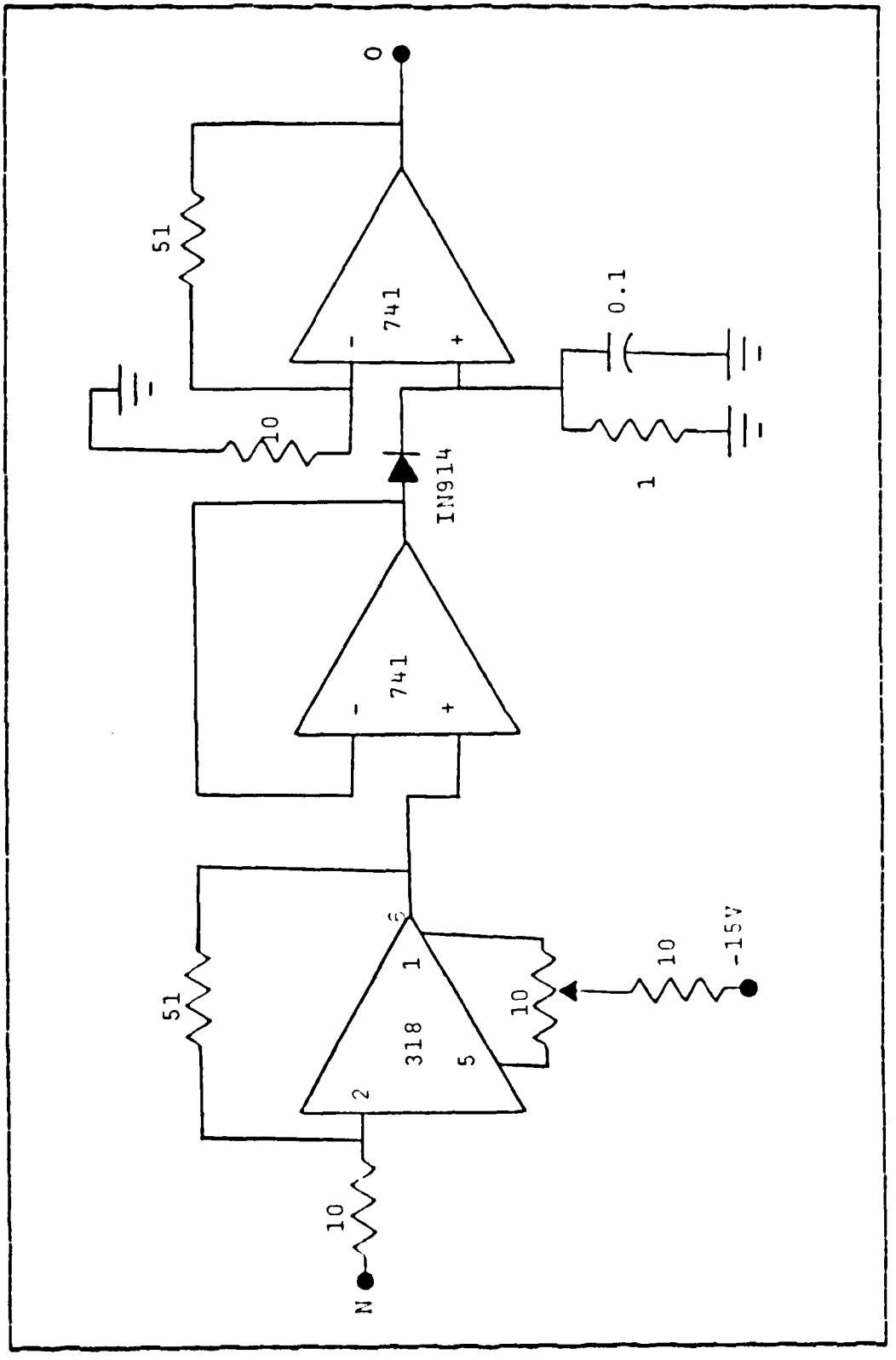

Figure A.8 Envelope Detector.

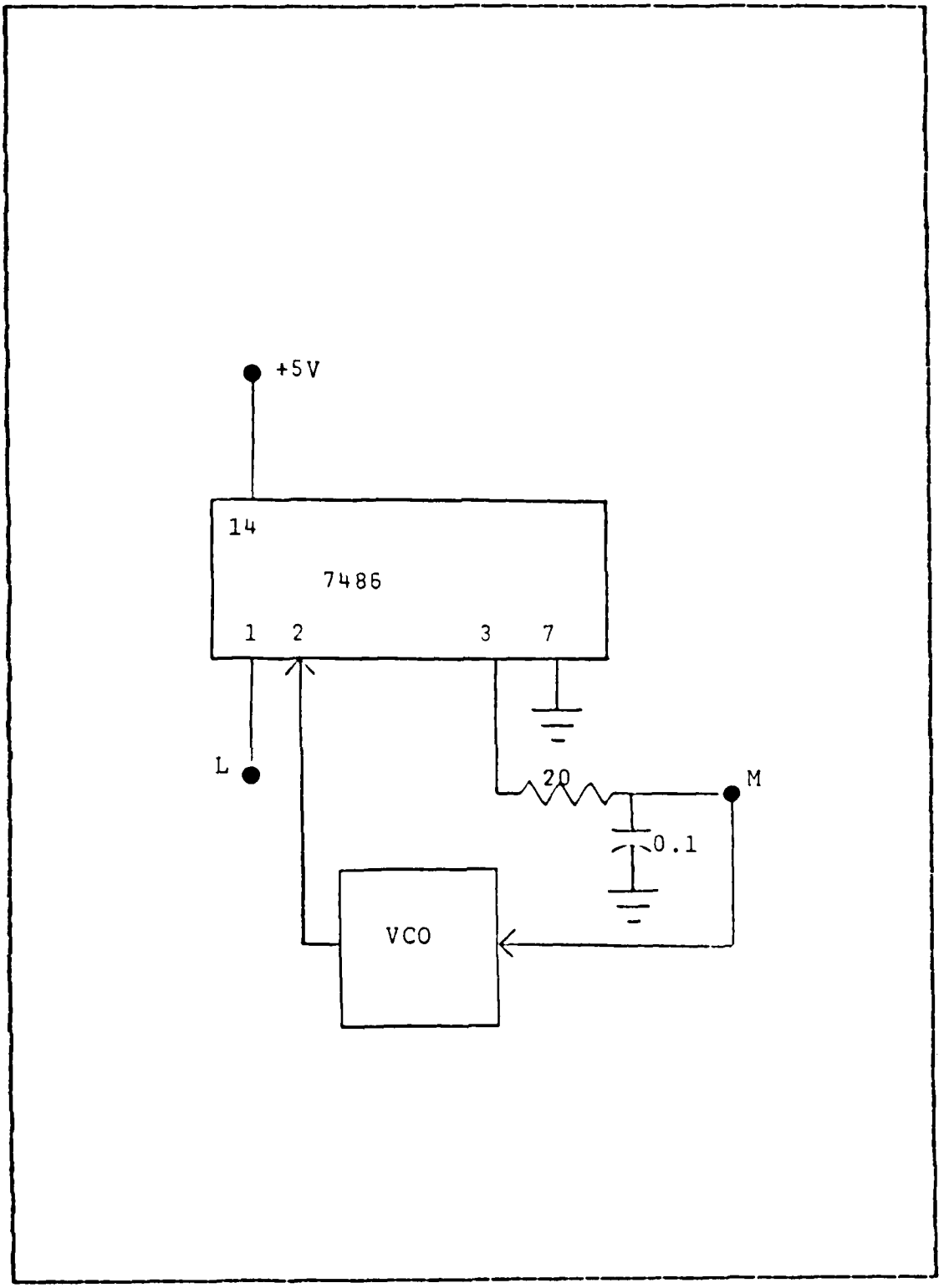

Figure A.7 Phase Locked Loop.

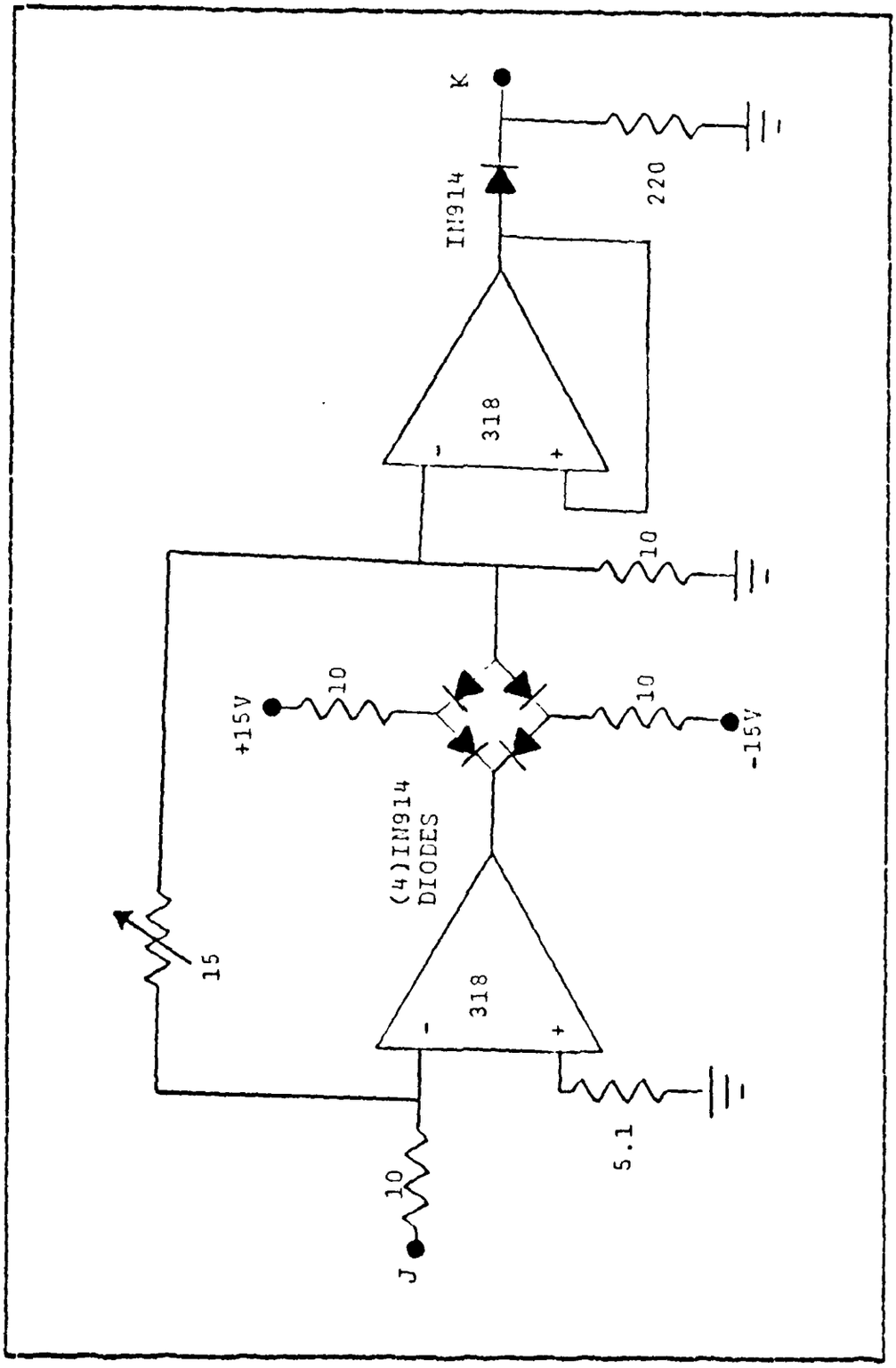

Figure A.6 Voltage Limiter/Rectifier.

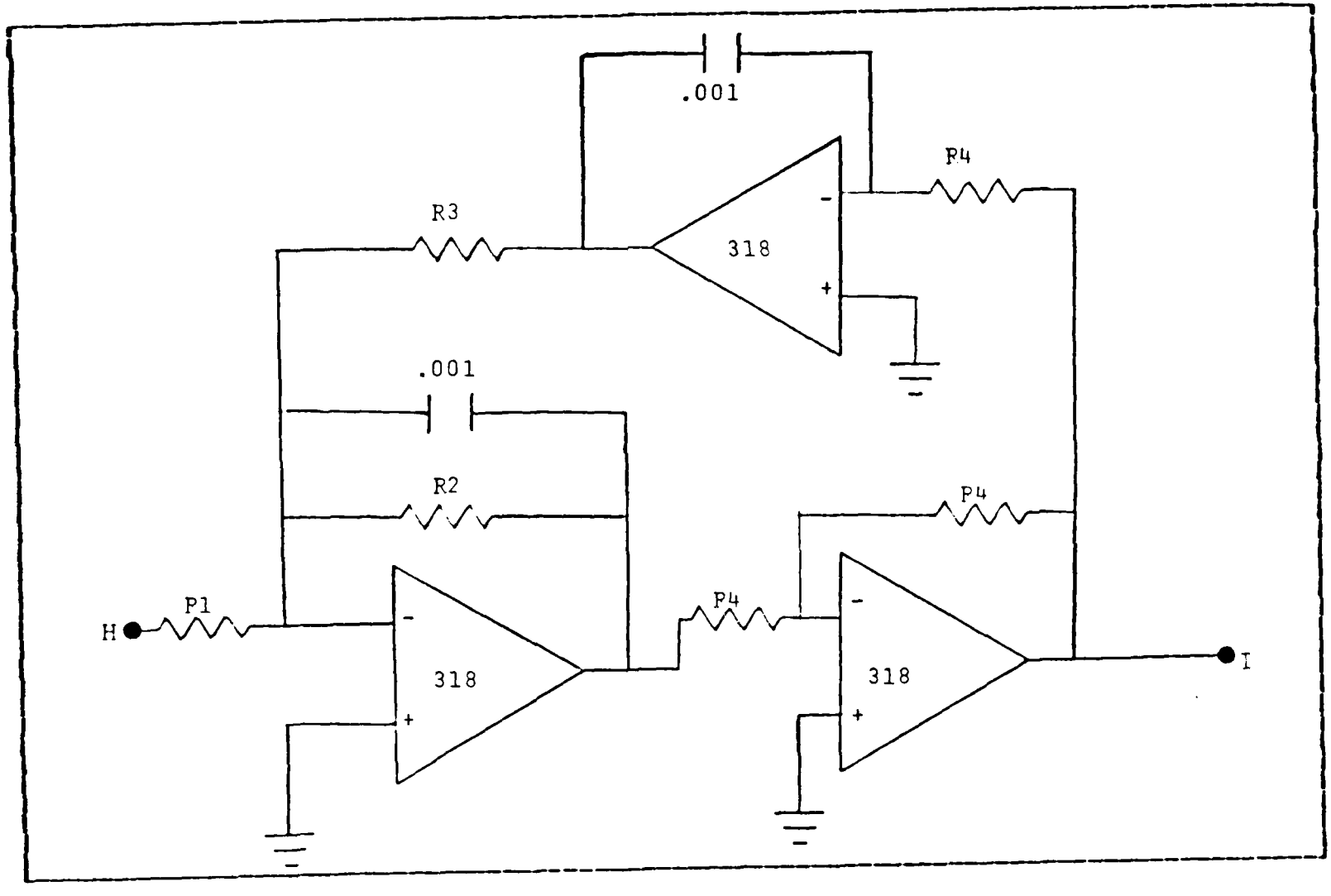

Figure A.5 Bandpass Filter Stage.

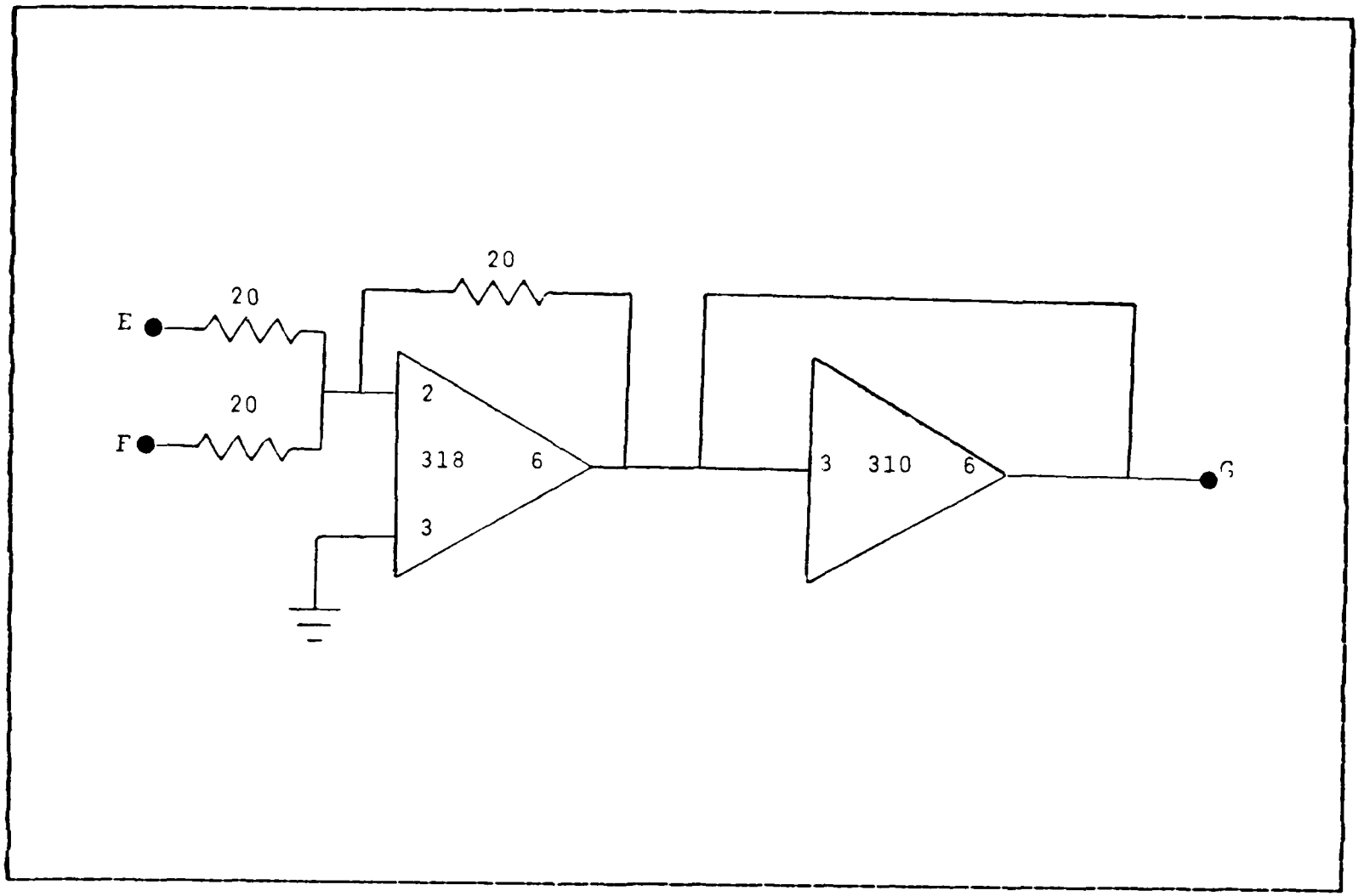

Figure A.4 Summer.

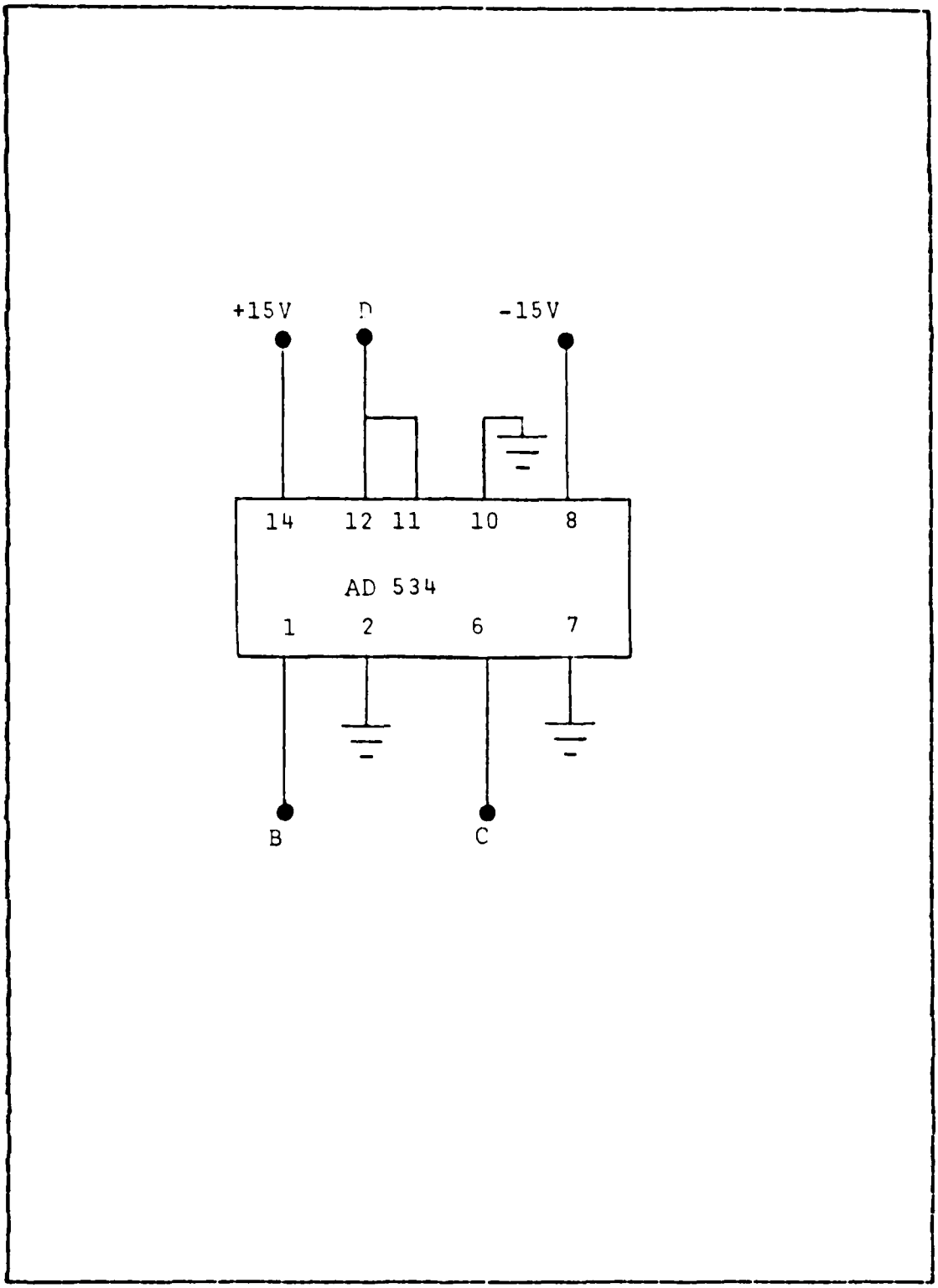

Figure A.3 Analog Multiplier.

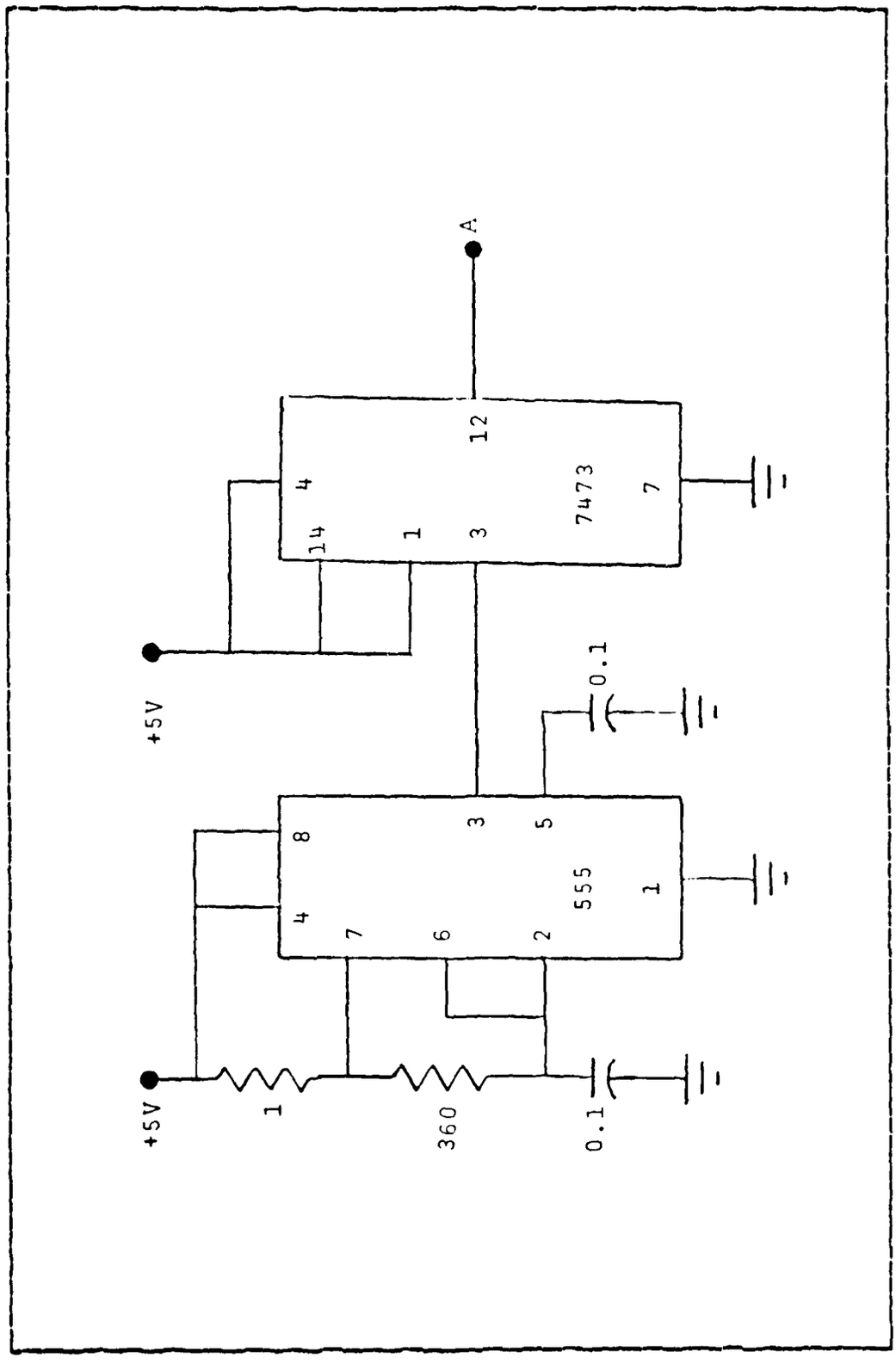

Figure A.2 54 msec Pulse Generator.

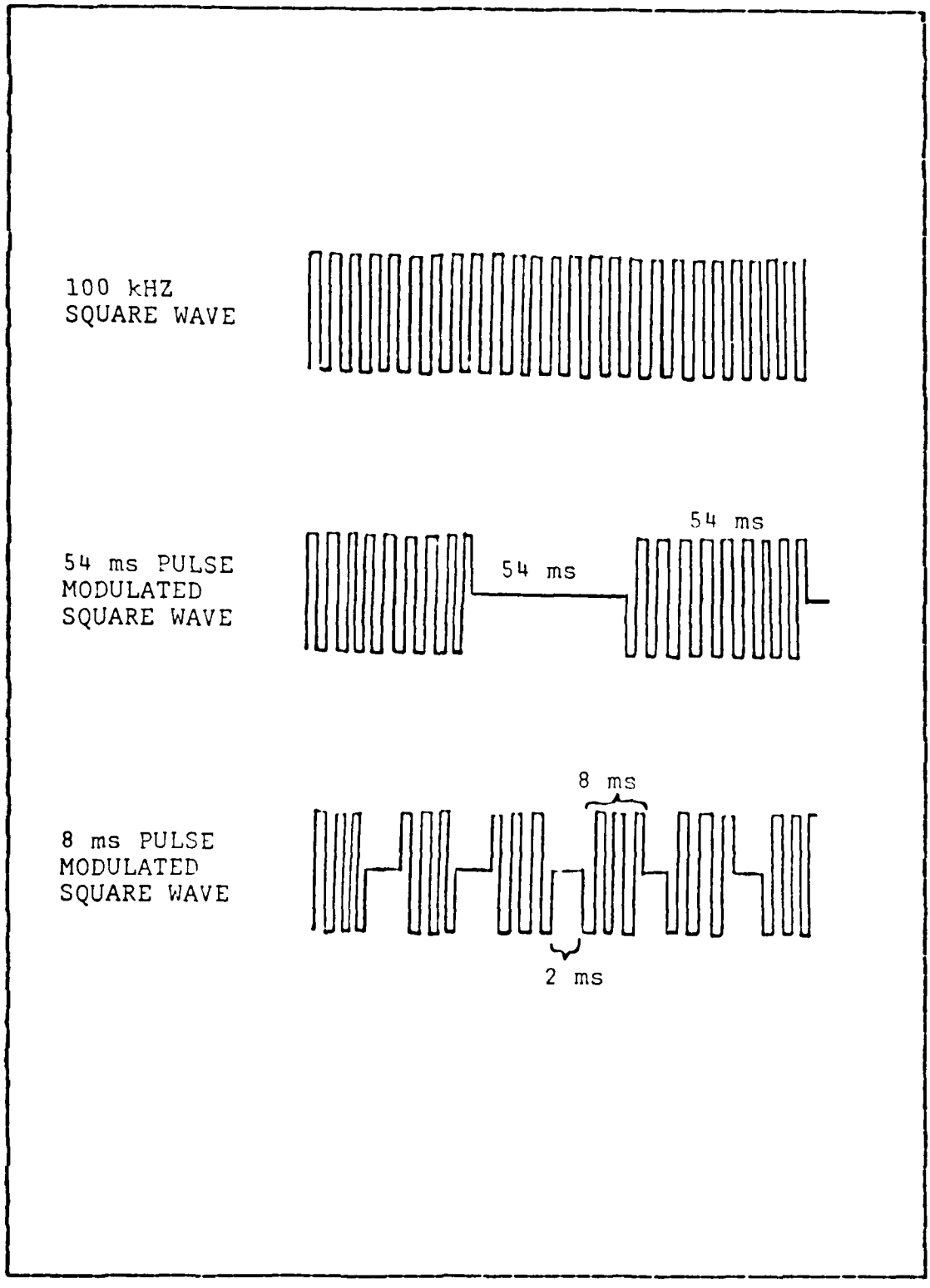

Figure A.1 Test Signals.

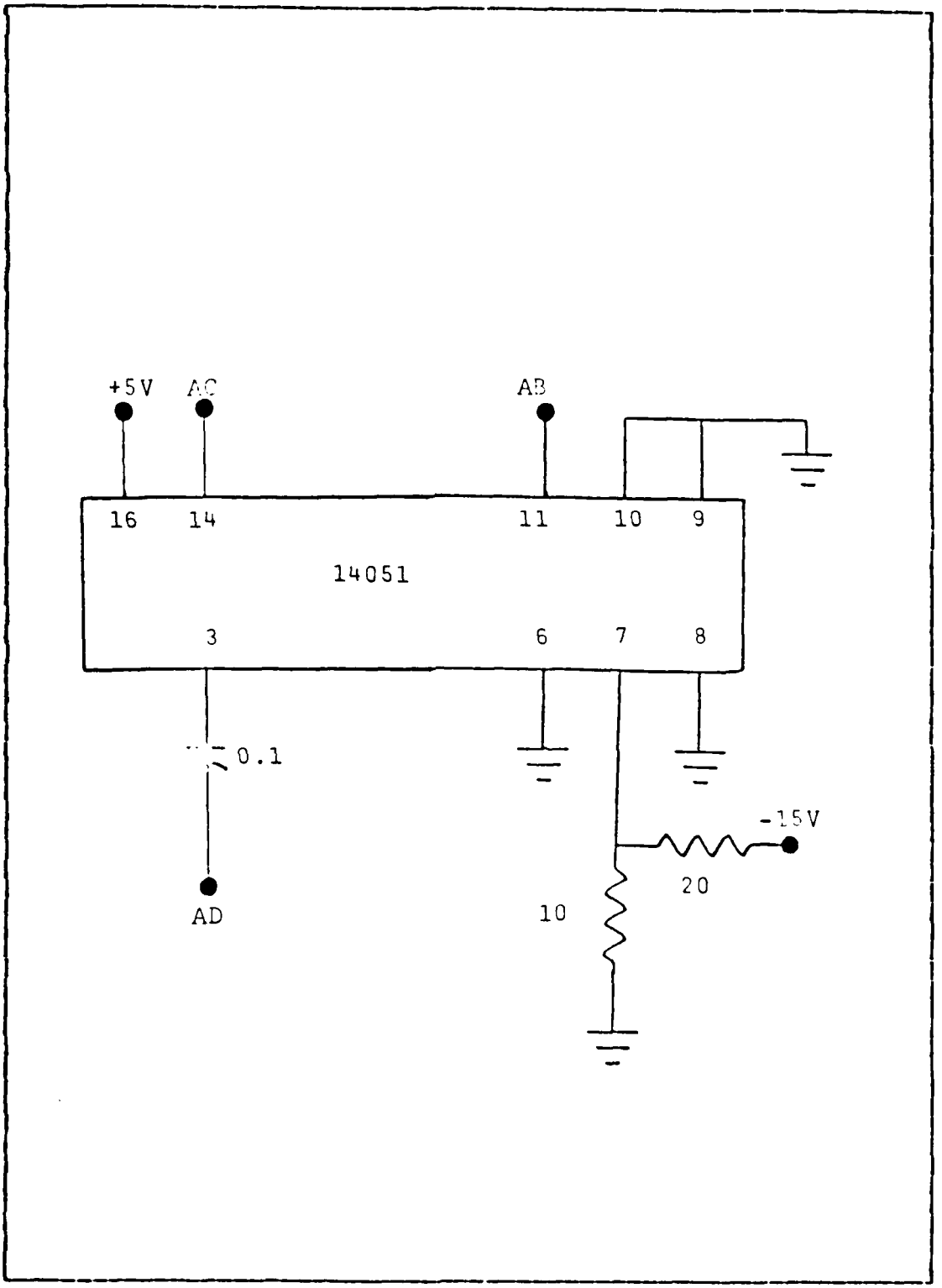

Figure A.15 Analog Switch.

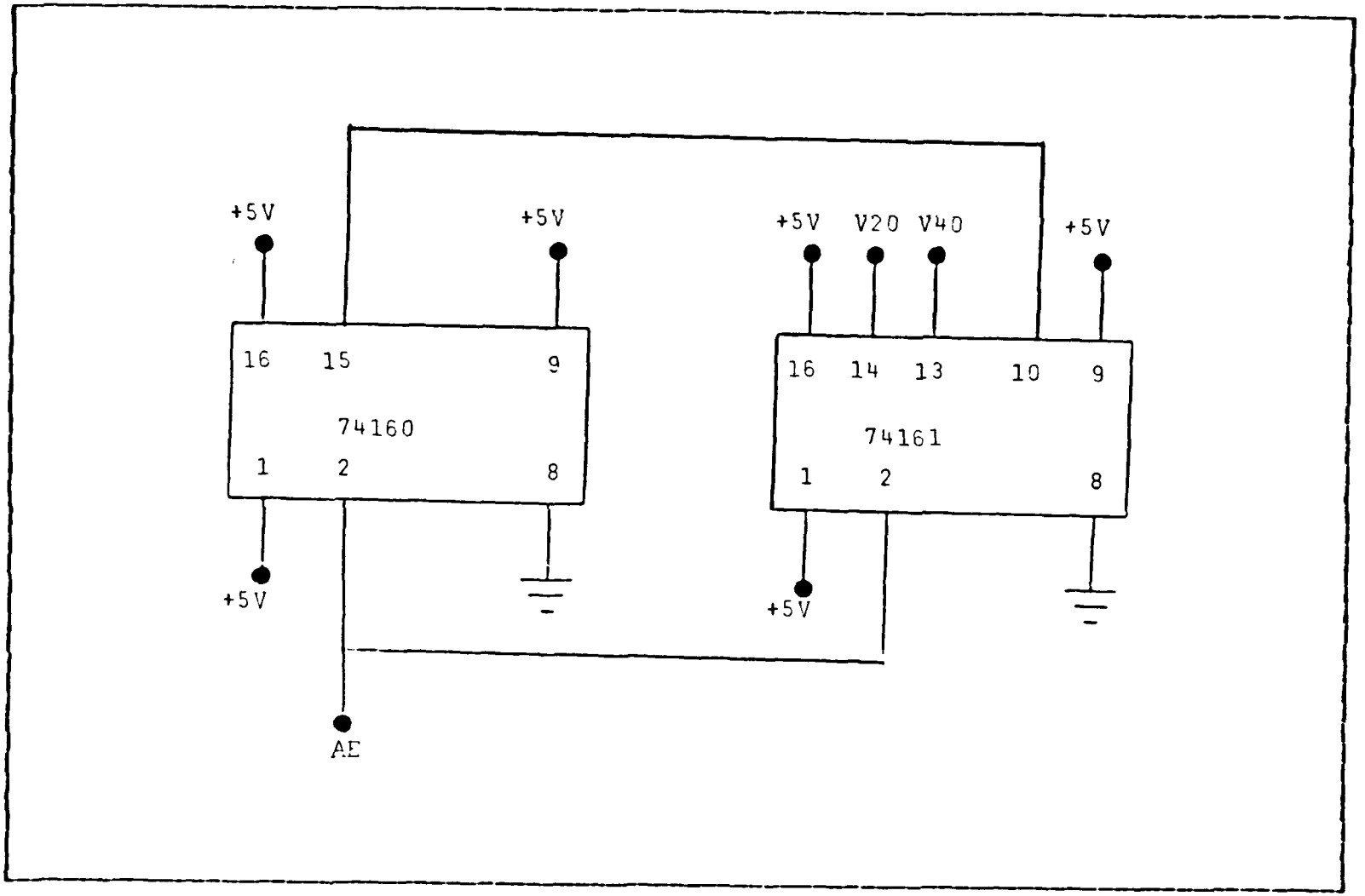

Figure A.16 Frequency Divider.

APPENDIX B

PHASE LOCKED LOOP LOCK ON TIME

R is the value of the resistor in the phase locked loop lowpass filter. The capacitor's value (C) is .001 microfarads and is not varied. Lock on time is measured for various values of R and the 3dB cutoff frequency (F) is calculated for each case using equation F=1/(6.28RC).

R(kilohms)	F(HZ)	Lock On Time(ms)
10	159	3
11	145	3
13	122	3
16	99	3
20	80	3
24	66	3
27	59	3
30	53	3
39	41	3
51	31	4
100	16	4
500	3	4

The above measurements are obtained with no noise added. Noise is added to the circuit and no significant effect on the duration of the lock on time is observed for any SNR greater than 3dB.

APPENDIX C

MEASURING THE FREQUENCY OF A TONE

The following key applies to the data tables in this appendix.

S, N: Root mean square (RMS) value of the signal(S) or noise(N) voltage measured at the output of the bandpass filter with no noise.

V: RMS value of signal plus noise voltage measured at the output of the bandpass filter.

SNR: The signal to noise ratio in decibels (dB) calculated by equations:

$$SNR = 10 \text{ LOG } \{ S^2/N^2 \} \quad \text{where}$$

$$N^2 = V^2 - S^2$$

F(IN): The frequency output of the square wave signal generator (WAVETEK 136) in HZ.

F(VCO): The frequency output of the phase locked loop VCO (WAVETEK 143).

F(DIFF): The magnitude of the difference between F(IN) and F(VCO).

The average, variance, and standard deviation of F(DIFF) is calculated for the twenty values of F(DIFF) using equations:

$$\text{Average F(DIFF)} = \{\text{Sum of F(DIFF) values}\}/20$$

$$\text{Variance F(DIFF)} = \{\text{Sum of [value of F(DIFF)]}^2\}/20 \text{ minus } \{\text{Average F(DIFF)}\}^2$$

$$\text{Std.dev. F(DIFF)} = \text{squareroot}\{\text{Variance F(DIFF)}\}$$

S = .50

V = .50

SNR = infinite

F(IN)	F(VCO)	F(DIFF)
97751.7	97751.8	0.1
49.1	49.1	.0
53.1	52.9	.2
52.1	51.7	.4
52.5	52.7	.2
53.7	53.5	.2
54.0	53.7	.3
49.5	49.2	.3
52.8	53.0	.2
55.0	54.8	.2
54.9	54.8	.1
55.0	54.8	.2
52.6	52.1	.5
54.0	54.0	.0
54.7	54.6	.1
54.9	54.8	.1
55.2	55.0	.2
54.4	54.4	.0
55.1	54.9	.2
54.0	54.0	.0

Average F(DIFF) = .1750

Variance F(DIFF) = .0169

Std.dev. F(DIFF) = .1299

S = .50

V = .55

SNR = 6.8

F(IN)	F(VCO)	F(DIFF)
97756.4	97756.5	0.1
55.3	55.1	.2
56.7	56.6	.1
55.9	55.9	.0
57.3	57.2	.1
56.6	56.5	.1
57.1	57.0	.1
57.2	57.1	.1
55.7	55.6	.1
55.6	55.4	.2
55.0	54.8	.2
55.3	55.2	.1
55.3	55.2	.3
57.7	57.6	.1
57.5	57.3	.2
57.6	57.4	.2
56.1	56.0	.1
57.6	57.5	.1
57.4	57.3	.1
58.2	58.0	.2

Average F(DIFF) = .1350

Variance F(DIFF) = .0428

Std.dev. F(DIFF) = .2069

S = .50

V = .60

SNR = 3.6

F(IN)	F(VCO)	F(DIFF)
97838.7	97841.3	2.6
38.8	40.1	1.3
35.5	37.9	2.4
34.0	35.8	1.8
34.4	36.9	2.5
33.9	35.3	1.4
34.1	34.0	0.1
34.5	35.6	1.1
31.4	33.8	2.4
32.6	35.7	3.1
33.0	35.4	2.4
32.5	34.0	1.5
32.0	34.8	2.8
31.6	35.2	3.6
32.0	35.2	3.2
32.4	32.5	0.1
31.5	33.7	2.2
30.6	33.9	3.3
30.7	32.4	1.7
31.7	34.0	2.3

Average F(DIFF) = 2.09

Variance F(DIFF) = .8929

Std.dev. F(DIFF) = .9449

S = .50

V = .61

SNR = 3.1

F(IN)	F(VCO)	F(DIFF)
97842.1	97853.3	11.2
42.4	51.6	9.2
42.1	51.5	8.7
42.8	55.3	12.5
39.4	48.6	9.2
36.0	47.7	11.9
35.8	41.9	6.1
37.2	48.2	11.0
36.4	41.8	5.4
36.1	43.5	7.4
34.6	44.5	9.9
35.5	41.1	5.6
36.1	40.3	4.2
37.3	44.8	7.5
38.1	48.4	10.3
38.5	45.2	6.7
38.6	45.9	7.3
43.5	54.6	11.1
43.2	59.9	16.7
43.4	56.1	12.7

Average F(DIFF) = 9.23

Variance F(DIFF) = 8.873

Std.dev. F(DIFF) = 2.979

APPENDIX D

MEASURING THE FREQUENCY OF A TONE OF SHORT DURATION

The following key applies to the data tables in this appendix.

S, N: Root mean square (RMS) value of the signal(S) or noise(N) voltage measured at the output of the bandpass filter with no noise.

V: RMS value of signal plus noise voltage measured at the output of the bandpass filter.

SNR: The signal to noise ratio in decibels (dB) calculated by equations:

$$SNR = 10 \text{ LOG } \{ S^2/N^2 \} \quad \text{where}$$

$$N^2 = V^2 - S^2$$

F(IN): The frequency output of the square wave signal generator (WAVETEK 136) in HZ ± 10HZ.

COUNT: The number of pulses produced in 40 milliseconds by the phase locked loop VCO(WAVETEK 143).

F(OUT): The frequency value of COUNT in HZ calulated by

$$F(OUT) = (25)\,COUNT$$

The average, variance, and standard deviation of COUNT is calculated for the twenty values of COUNT using equations:

Average COUNT = (Sum of COUNT values)/20

Variance COUNT = {Sum of (COUNT value)^2}/20 minus (Average COUNT)^2

Std.dev. COUNT = squareroot(Variance COUNT)

S = .30

V = .30

SNR = infinite

F(IN)	COUNT
97639	3905
	3904
	3905
	3905
	3905
	3906
	3904
	3905
	3904
	3903
	3903
	3904
	3903
	3904
	3902
	3904
	3903
	3903
	3904
	3903

	COUNT	F(OUT)
Average	3904.0	97600
Variance	.95	594
Std.dev.	.97	24.4

S = .30

V = .32

SNR = 8.6

F(IN)	COUNT
97668	3906
	3906
	3906
	3909
	3905
	3905
	3905
	3907
	3906
	3906
	3906
	3907
	3905
	3907
	3906
	3905
	3905
	3906
	3905
	3905

	COUNT	F(OUT)
Average	3905.9	97648
Variance	1.00	625
Std.dev.	1.00	25.0

S = .30

V = .34

SNR = 5.5

F(IN)	COUNT
97673	3907
	3909
	3907
	3907
	3908
	3909
	3906
	3908
	3907
	3907
	3907
	3909
	3909
	3908
	3909
	3908
	3907
	3909
	3906
	3906

	COUNT	F(OUT)
Average	3907.6	97690
Variance	1.13	706
Std.dev.	1.06	26.5

S = .30

V = .36

SNR = 3.6

F(IN)	COUNT
97688	3907
	3907
	3909
	3907
	3910
	3907
	3907
	3909
	3909
	3910
	3908
	3908
	3909
	3913
	3910
	3908
	3909
	3908
	3908
	3909

	COUNT	F(OUT)
Average	3908.6	97715
Variance	2.04	1275
Std.dev.	1.43	35.8

S = .30

V = .38

SNR = 2.2

F(IN)	COUNT
97695	3909
	3909
	3908
	3911
	3911
	3914
	3912
	3910
	3911
	3913
	3911
	3909
	3911
	3912
	3909
	3909
	3911
	3910
	3910
	3909

	COUNT	F(OUT)
Average	3910.5	97763
Variance	2.25	1406
Std.dev.	1.50	37.5

Average X = {Sum of X values}/20

Variance X = {Sum of $(X \text{ value})^2$}/20 minus
{Average X}^{2}

Std.dev. X = squareroot (Variance X)

APPENDIX G

MEASURING THE FREQUENCY OF A TONE OF SHORT DURATION WITH FREQUENCY DIVISION AND A VERY STABLE CLOCK

The following key applies to the data tables in this appendix.

S, N: Root mean square (RMS) value of the signal(S) or noise(N) voltage measured at the output of the bandpass filter with no noise.

V: RMS value of signal plus noise voltage measured at the output of the bandpass filter.

SNR: The signal to noise ratio in decibels (dB) calculated by equations:

$$SNR = 10 \text{ LOG } \{ S^2/N^2 \} \quad \text{where}$$

$$N^2 = V^2 - S^2$$

F(IN): The frequency output of the square wave signal generator (WAVETEK 136) in HZ.

COUNT: The number of pulses produced in 40 milliseconds by the phase locked loop VCO(WAVETEK 143).

F(OUT): The frequency value of COUNT in HZ calculated by

$$F(OUT) = (1.25)COUNT$$

The average, variance, and standard deviation of F(IN) and F(OUT) is calculated for the twenty values of each using equations:

DIVIDE BY 20

S = .30

V = .30

SNR = infinite

F(IN)	COUNT	F(OUT)
97710	78228	97785
11	189	736
15	200	750
21	170	713
18	169	711
17	201	751
16	204	755
17	196	745
14	189	736
15	196	745
15	160	700
16	185	731
16	205	756
16	164	705
16	176	658
16	171	714
17	168	710
17	222	778
17	204	755
17	208	760

	F(IN)	F(OUT)
Average	97715.9	97734.7
Variance	5.12	854
Std.dev.	2.26	29.2 cms

Average X = {Sum of X values}/20

Variance X = {Sum of (X value)^2}/20 minus
{Average X}^{2}

Std.dev. X = squareroot(Variance X)

APPENDIX F

MEASURING THE FREQUENCY OF A TONE OF SHORT DURATION WITH FREQUENCY DIVISION

The following key applies to the data tables in this appendix.

S, N: Root mean square (RMS) value of the signal(S) or noise(N) voltage measured at the output of the bandpass filter with no noise.

V: RMS value of signal plus noise voltage measured at the output of the bandpass filter.

SNR: The signal to noise ratio in decibels (dB) calculated by equations:

$$SNR = 10 \text{ LOG } \{ S^2/N^2 \} \quad \text{where}$$

$$N^2 = V^2 - S^2$$

F(IN): The frequency output of the square wave signal generator (WAVETEK 136) in HZ.

COUNT: The number of pulses produced in 40 milliseconds by the phase locked loop VCO(WAVETEK 143).

F(OUT): The frequency value of COUNT in HZ calculated by

$$F(OUT) = (1.25)COUNT$$

The average, variance, and standard deviation of F(IN) and F(OUT) is calculated for the twenty values of each using equations:

DIVIDE BY 20

S = .50

V = .56

SNR = 5.9

F(IN)	F(DIV)	F(DIFF)
97787.8	97784.0	3.8
791.6	786.0	5.6
787.7	783.5	4.2
791.1	788.7	2.4
792.6	787.9	4.7
790.3	785.2	5.1
791.3	786.1	5.2
791.2	786.0	4.2
792.5	789.3	3.2
793.8	788.0	5.8
791.7	786.1	5.6
790.7	785.1	5.6
790.0	791.9	1.9
794.9	792.1	2.8
793.1	785.9	7.2
792.8	789.7	3.1
795.1	791.0	4.1
795.8	792.4	3.4
797.1	793.3	3.8
797.0	793.0	4.0

Average F(DIFF) = 4.23

Variance F(DIFF) = 1.65

Std.dev. F(DIFF) = 1.29

DIVIDE BY 20

S = .50

V = .54

SNR = 6.8

F(IN)	F(DIV)	F(DIFF)
97768.5	97768.5	5.0
769.7	764.7	5.0
767.0	761.8	5.2
765.9	763.9	2.0
768.8	763.2	5.6
772.0	768.5	3.5
773.3	769.0	4.3
772.0	767.8	4.2
773.5	770.2	3.3
773.4	769.2	4.2
770.6	767.1	3.5
775.5	773.1	2.4
776.6	772.6	4.0
778.2	773.8	4.4
775.8	771.7	4.1
772.3	768.5	3.8
771.9	768.1	3.8
775.7	772.5	3.2
775.4	772.5	2.9
776.0	772.9	3.1

Average F(DIFF) = 3.88

Variance F(DIFF) = .816

Std.dev. F(DIFF) = .903

DIVIDE BY 20

S = .50

V = .52

SNR = 10.9

F(IN)	F(DIV)	F(DIFF)
97745.7	97744.8	0.9
745.9	743.9	2.0
741.7	741.7	0.0
744.9	744.9	0.0
740.0	739.4	0.6
747.5	746.9	0.6
745.2	744.2	1.0
745.5	745.7	0.2
750.7	749.5	1.2
744.7	743.1	1.6
740.6	739.6	1.0
740.2	739.9	0.3
743.2	744.0	0.8
755.7	755.4	0.3
751.7	749.0	2.7
744.1	743.7	0.4
751.6	752.6	1.0
755.7	755.6	0.1
757.9	757.2	0.7
756.5	757.5	1.0

Average F(DIFF) = .820

Variance F(DIFF) = .445

Std.dev. F(DIFF) = .667

DIVIDE BY 20

S = .50

V = .50

SNR = infinite

F(IN)	F(DIV)	F(DIFF)
97721.3	97720.9	0.4
720.6	719.4	1.2
707.5	708.4	.9
719.0	719.2	.2
721.3	722.0	.7
726.1	726.0	.1
726.8	726.7	.1
725.1	723.9	1.2
724.3	725.4	1.1
726.7	726.8	.1
727.4	727.5	.1
728.8	728.9	.1
730.4	730.3	.1
729.9	729.8	.1
725.3	724.0	.7
720.0	719.9	.1
727.3	728.4	.9
731.5	731.8	.3
733.5	734.1	.6
733.7	733.6	.1

Average F(DIFF) = .455

Varian e F(DIFF) = .164

Std.dev. F(DIFF) = .406

DIVIDE BY 40

S = .50

V = .52

SNR = 10.9

F(IN)	F(LIV)	F(DIFF)
97809.2	97866.6	57.4
810.3	873.7	63.4
810.9	875.4	64.5
812.9	867.5	54.6
813.3	871.8	58.5
815.0	871.0	56.0
817.2	870.1	52.9
816.2	868.8	52.6
815.5	870.5	55.0
817.3	875.6	58.3
817.3	878.7	61.4
816.4	875.3	58.9
813.9	878.4	64.5
814.7	874.8	60.1
814.8	876.8	61.8
815.0	872.3	57.3
819.6	880.5	60.9
818.9	875.5	56.6
821.6	880.1	58.5
819.5	881.0	61.5

Average F(DIFF) = 58.7

Variance F(DIFF) = 11.9

Std.dev. F(DIFF) = 3.45

DIVIDE BY 40

S = .50

V = .50

SNR = infinite

F(IN)	F(DIV)	F(DIFF)
97778.1	97778.1	0.0
778.9	778.8	.1
778.7	779.2	.5
782.6	782.6	.0
785.9	786.4	.5
787.6	787.2	.4
781.1	787.0	1.1
787.6	787.6	.0
788.8	788.3	.5
787.1	787.2	.1
789.7	789.4	.3
787.1	786.9	.2
790.7	790.7	.0
788.6	788.6	.0
789.9	790.2	.3
795.3	795.6	.3
794.4	794.4	.0
796.8	796.7	.1
796.9	796.7	.2
797.2	797.3	.1

Average F(DIFF) = .235

Variance F(DIFF) = .073

Std.dev. F(DIFF) = .265

APPENDIX E

MEASURING THE FREQUENCY OF A TONE WITH FREQUENCY DIVISION

The following key applies to the data tables in this appendix.

S, N: Root mean square (RMS) value of the signal(S) or noise(N) voltage measured at the output of the bandpass filter with no noise.

V: RMS value of signal plus noise voltage measured at the output of the bandpass filter.

SNR: The signal to noise ratio in decibels (dB) calculated by equations:

$$SNR = 10 \text{ LOG } \{ S^2/N^2 \} \quad \text{where}$$

$$N^2 = V^2 - S^2$$

F(IN): The frequency output of the square wave signal generator (WAVETEK 136) in HZ.

F(DIV): The frequency output of the phase locked loop frequency divider.

F(DIFF): The magnitude of the difference between F(IN) and F(DIV).

The average, variance, and standard deviation of F(DIFF) is calculated for the twenty values of F(DIFF) using equations:

$$\text{Average F(DIFF)} = \{\text{Sum of F(DIFF) values}\}/20$$

$$\text{Variance F(DIFF)} = \{\text{Sum of [value of F(DIFF)]}^2\}/20 \text{ minus } \{\text{Average F(DIFF)}\}^2$$

$$\text{Std.dev. F(DIFF)} = \text{squareroot}\{\text{Variance F(DIFF)}\}$$

S = .30

V = .42

SNR = 0.2

F(IN)	COUNT
97710	3911
	3915
	3912
	3909
	3915
	3911
	3915
	3913
	3911
	3914
	3914
	3916
	3912
	3915
	3910
	3914
	3917
	3917
	3913
	3916

	COUNT	F(OUT)
Average	3913.5	97838
Variance	5.15	3219
Std.dev.	2.27	56.8

S = .30

V = .40

SNR = 1.1

F(IN)	COUNT
97704	3911
	3910
	3910
	3915
	3911
	3910
	3912
	3911
	3910
	3914
	3912
	3913
	3910
	3911
	3910
	3914
	3909
	3913
	3911
	3915

	COUNT	F(OUT)
Average	3911.6	97790
Variance	3.14	1963
Std.dev.	1.77	44.3

DIVIDE BY 20

S = .30

V = .30

SNR = infinite

F(IN)	COUNT	F(OUT)
97713	74262	92828
09	77	46
09	59	24
12	88	60
12	62	28
12	84	55
12	62	28
11	60	25
09	59	24
13	62	28
11	61	26
13	78	48
10	77	46
12	82	53
10	77	46
13	83	54
13	79	49
13	63	29
10	81	51
13	62	28

	F(IN)	F(OUT)
Average	97712	92839
Variance	2.15	155
Std.dev.	1.47	12.5

DIVIDE BY 20

S = .30

V = .32

SNR = 8.6

F(IN)	COUNT	F(OUT)
97714	74262	92828
17	288	60
12	263	29
13	262	28
14	267	34
16	288	60
17	263	29
19	285	56
21	268	35
17	293	66
18	291	64
22	292	65
22	292	65
22	292	65
23	271	39
19	268	35
20	296	70
19	301	76
19	272	40
22	295	69

	F(IN)	F(OUT)
Average	97718	92851
Variance	10.2	278
Std.dev.	3.20	16.7

DIVIDE BY 20

S = .30

V = .34

SNR = 5.5

F(IN)	COUNT	F(OUT)
97717	74289	92861
24	269	36
25	271	39
21	270	38
24	291	64
24	294	68
23	270	38
25	274	43
26	272	40
24	303	79
25	271	39
22	287	59
21	292	65
29	266	58
31	314	93
31	276	45
31	276	45
32	308	65
27	276	45
31	277	46

	F(IN)	F(OUT)
Average	97726	92854
Variance	15.9	276
Std.dev.	3.99	16.6

DIVIDE BY 20

S = .30

V = .36

SNR = 3.6

F(IN)	COUNT	F(OUT)
97726	74300	92875
26	296	70
26	274	43
26	286	58
24	273	41
26	296	70
26	273	41
26	273	41
24	293	66
24	273	41
24	273	41
24	295	69
24	273	41
25	270	38
21	268	35
14	261	26
21	297	71
21	268	35
25	271	39
25	272	40

	F(IN)	F(OUT)
Average	97724	92849
Variance	7.89	223
Std.dev.	2.81	14.9

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