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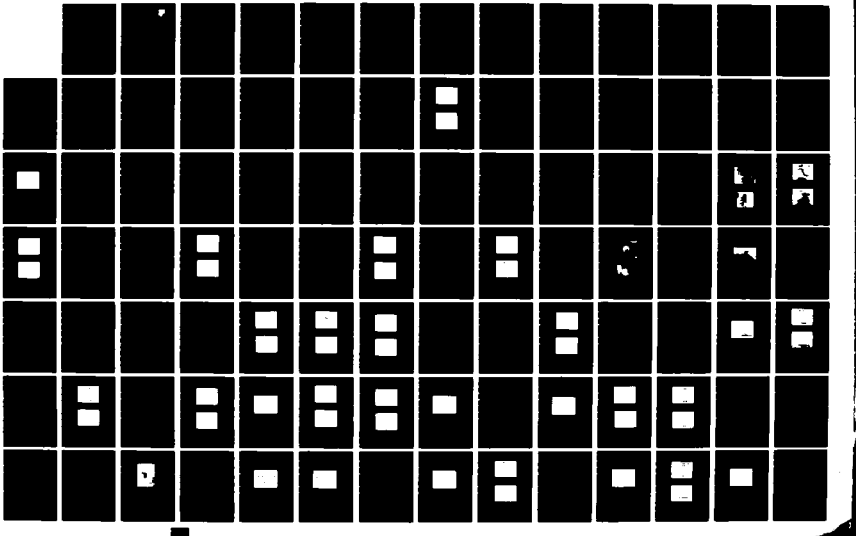

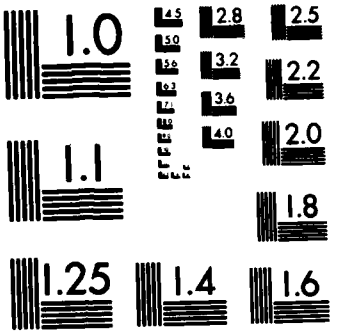

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Final Technical Report
February 1985

FAST TRANSIENT BEHAVIOR OF THYRISTOR SWITCHES

Texas Tech University

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ROME AIR DEVELOPMENT CENTER
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19. ABSTRACT (Continue on reverse if necessary and identify by block number)

The fast transient behavior of thyristor switches above the recommended dI/dt was investigated. Two types of thyristors in compression packages were tested. Both types are fast switching devices, differing principally in their gate-cathode geometries. One type is centered fired, while the other is slightly interdigitated.

Two pulse forming networks were designed. The first was a twelve section, equal inductance, equal capacitance, type E PFN, whose output was a 100 microsecond pulse with a rise time of .5 microsecond. The second PFN was a 125 section equal inductance, equal capacitance, type E network, whose output is a 10 microsecond pulse with a rise time of 10ns.

Twenty devices, ten of each type, were electrically characterized initially. Five of each type switched the 10 microsecond PFN single-shot at step-wise increasing values of dI/dt until the maximum available value was reached. The remaining ten devices were repetitively pulsed at a high dI/dt, and recharacterized at logarithimic time intervals. →(Over)

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Failure analysis consisted of the determination of gross faults by opening the packages and examining the device chip. Additional keywords: Test circuits, printed board technology, Experimental data, Transmission switching devices, Schematic diagrams.

FINAL REPORT EVALUATION

FAST TRANSIENT BEHAVIOR OF THYRISTOR SWITCHES

This Final Technical Report describes the experimental results of a study to characterize the fast transient behavior of thyristors above their recommended dI/dt. The motivation for this effort is that thyristors will occasionally exceed their ratings by factors which cannot be explained on the basis of present models or manufacturing technology.

The purpose of this work was to establish performance characteristics of fast switching thyristors by a careful series of pulsed measurements. Two pulse forming networks (PFN's) were designed and built to perform single-shot stress and repetitive stress on the test devices. A description of the PFN's and characterization circuits (dc parameters, blocking voltage and gate-cathode diode characterization) along with test results and conclusions are discussed.

The results suggest that the specified values of single-shot dI/dt are too conservative, as are repetitive values, at least for short (ten hours) periods of operation. The limited testing time requires that additional work be done in this area before any conclusions can be made.

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I. INTRODUCTION

Although the development of pulsed power technology depends on the availability of high energy density storage devices and suitable pulse forming networks, the principal limitation is probably the switch. No switch at this time meets simultaneously the many specifications of a satisfactory closing device, and opening switches are still primitive. Hard glass tubes, such as thyratrons and spark gaps, are commonly used as closing switches; however, their lifetime and reliability are severely affected by electrode erosion, surface flashover, reaction products, and similar poorly understood effects. On the other hand, semiconductor switches have demonstrated long life and reliability under a variety of conditions which imply similar dependability under the stress of fast, high-power pulses, and the use of semiconductor thyristor closing switches deserves serious consideration.

Thyristors are used at present for many switching applications, and their static characteristics and behavior after turn-on have been extensively studied. However, transient turn-on, probably the most important constraint on fast thyristor switching, has scarcely been addressed. Although thyristor switches have been characterized for low frequency and long pulse operation, there is essentially no information respecting fast

pulse switching by such devices. Models for turn-on of semiconductor thyristor switches have been proposed, but none have been applied to thyristor operation in the very fast, high current, short pulse regime; no significant data respecting such operation are available, and it is not possible to describe theoretical or actual performance limits. User results, generally undocumented, indicate that thyristors will occasionally exceed their ratings by factors which cannot be explained on the basis of present models or manufacturing technology. The purpose of this work was to establish more realistic performance characteristics of semiconductor switching devices by a careful series of pulsed measurements.

II. CHARACTERIZATION PARAMETERS AND TEST CIRCUITS

Although not all the test circuits were used in the characterization procedures which were finally selected, a number of preliminary characterizations were performed. These involved forward and reverse blocking voltage, pulsed gate-cathode diode forward current-voltage behavior, gate trigger voltage and current, anode holding currents, and DC forward voltage drop.

1. Blocking Voltage

Forward and reverse blocking characteristics are probably the most important parameters for establishing degradation. Although maximum leakage current is specified at rated blocking voltage, this current is a 125 °C value; at room temperature, no significant leakage current flows in a good device. It was not practical to establish a percentage change in room temperature leakage current as a criterion for degradation; serious degradation was assumed to have occurred if the room temperature current at 800 V exceeded its 125 °C value, 30 mA for the T7S7 and 35 mA for the T72H. The blocking voltage test circuit, shown in figure 1, provides a continuous or single pulse half-rectified 60 Hz sinusoidal voltage of appropriate polarity to the anode of the test device. The peak voltage amplitude can be varied between almost zero (100 mV) and 1000 V.

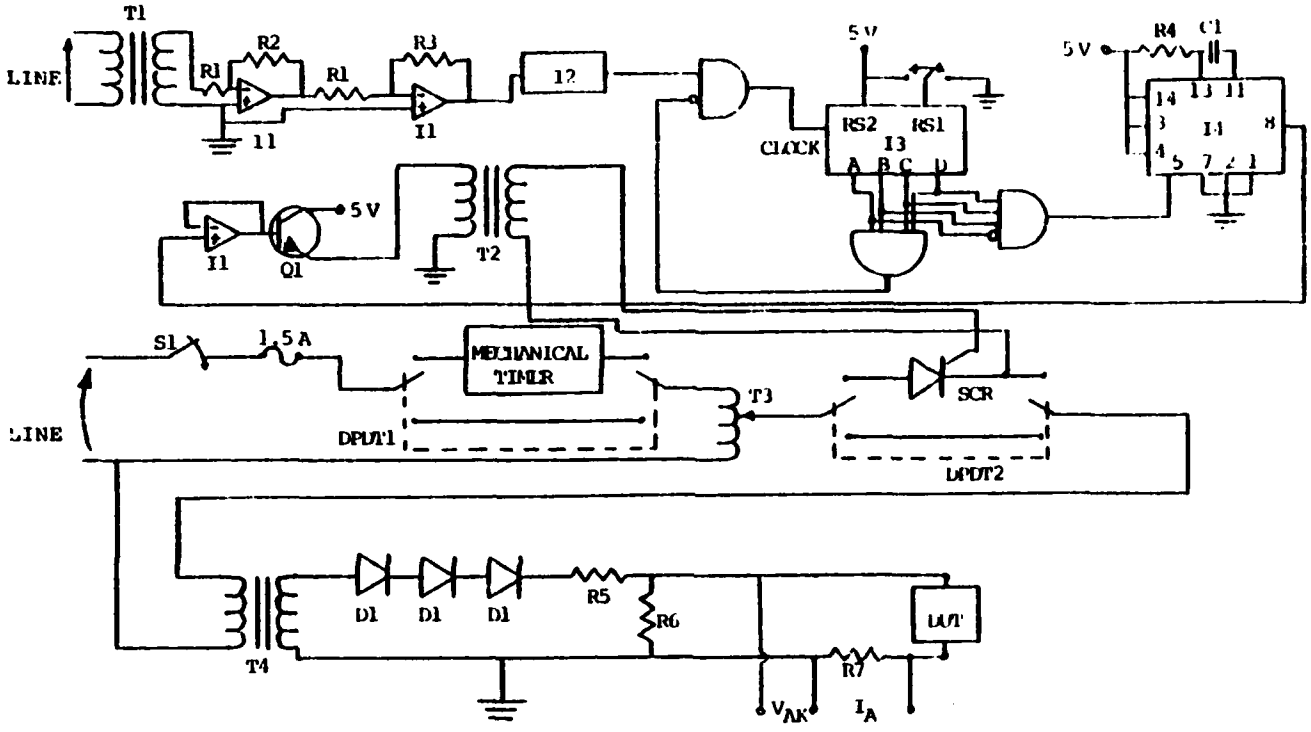
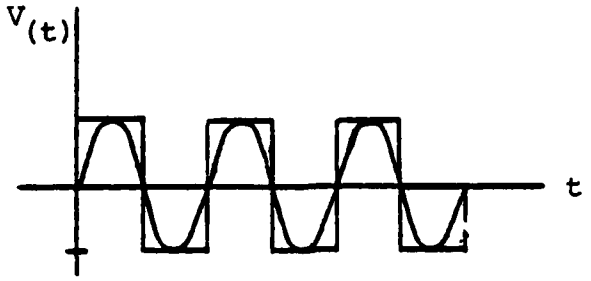


Figure 1. Circuit schematic for the blocking voltage tester. Resistors: R1, 3.3 KΩ; R2, 330 KΩ; R3, 33 KΩ; R4, 12 KΩ; R5, 1 KΩ, 2 W; R6, 235 KΩ; R7, 1 Ω. Capacitors: C1, 0.15 μF. Diodes: SK3081. Transistors: Q1, 2N2222. SCR: SK3627. Integrated circuits: I1, SN72741 operational amplifier; I2, SN7413 Schmitt NAND; I3, SN7493 counter; I4; I5, SN54122 monostable multivibrator.

In the pulse mode, a 5 V signal, transformed down from the line voltage, is fed to a two-stage amplifier. The amplifier has an overall gain of 1000 and saturates rapidly, so that its output is a 10 V square wave with very fast leading and trailing edges. The square wave is fed to a Schmitt NAND gate which clips the negative-going pulse and increases the rise time of the positive-going pulse. Figure 2a shows the output from the secondary of the input transformer relative to the output from the amplifier. In figure 2b, the transformer voltage is shown relative to the Schmitt NAND output. It can be seen that the output of the NAND gate is a positive 5 V, 60 Hz pulse synchronized with the line voltage such that the trailing edge of the pulse is at the positive-going zero-crossing of the line voltage.

The output from the Schmitt trigger is fed to one input of an AND gate. The other input is usually at 5 V (BCD 1) so that the Schmitt pulse feeds directly to the clock of the 4-bit binary counter. One reset of the counter, RS2, is tied directly to 5 V. The other reset, RS1, is connected to a single-pole double-throw switch. In normal counting mode, RS1 is grounded. The clock pulses cause the counter to count from BCD 0 to BCD 15. (A is the least significant bit and D, the most significant bit.) The counter outputs (A, B, C and D) are connected to a 4-input AND gate whose output goes high at BCD 15. This signal is inverted and fed into the AND gate with the Schmitt signal. As the counter changes from BCD 14 to BCD 15, the clock signal goes to 0. In this way, the counter counts from 0 to 15 at 60 Hz and



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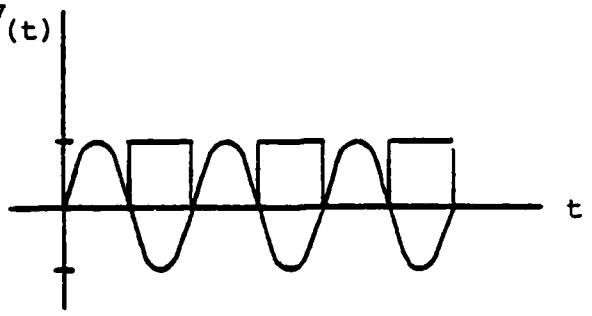


b.

Figure 2. Phase relationships between the voltage at the secondary of the input transformer and a) the amplifier output square wave; b) the Schmitt NAND output.

then stops until the counter outputs are manually reset by switching RS1 to 5 V.

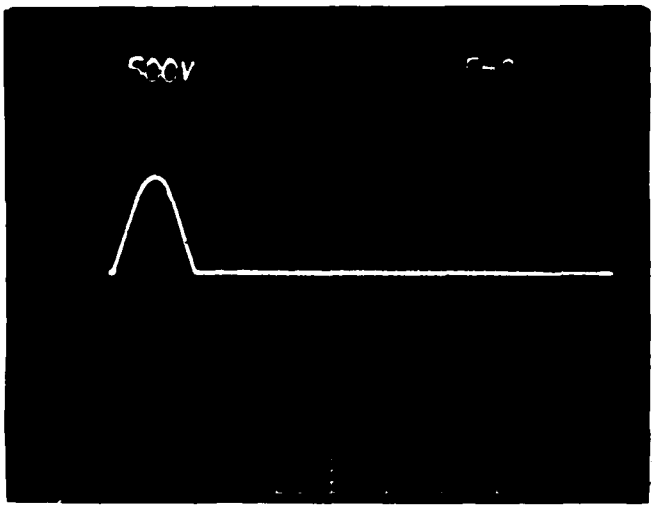
The outputs of the counter are also tied to a second 4-input AND gate (with A inverted), so that a 5 V pulse appears at BCD 14 at the output of the second AND. This pulse is used as a leading edge trigger for a monostable multivibrator which has a 5 V, 500 μS output pulse. The pulse is fed to a transistor, buffered by a unity gain op amp; the transistor drives a transformer which gates an SCR switch.

The line voltage is fed through a DPDT switch, set to continuous mode (connecting the mechanical timer), or to single pulse mode (short), to the primary of a variable transformer. The secondary is connected to another DPDT switch, set to continuous mode (short) or pulse mode (tying in the SCR). In the pulse mode, the SCR is in series with the primary of a power transformer. The gate pulse turns on the SCR just as a positive half-wave rectified current appears at the anode, allowing current flow through the primary of the transformer. The SCR self-commutates on the negative half-cycle so that only one pulse appears at the secondary.

At the secondary, the positive half-wave rectified current flows through three diodes in series to the device under test (DUT). The anode voltage at the test device is measured directly, and the anode leakage current is measured with a sampling resistance. The blocking voltage amplitude is controlled by the variable transformer in the primary circuit.

In the continuous mode, the switch on the primary of the variable transformer is set so that the mechanical timer is in the circuit. The mechanical timer is adjustable for a continuous wave train, 1 to 10 seconds in duration. The switch in the power transformer primary must also be in the continuous mode to allow primary current flow. With the switch in this position, the SCR is completely disconnected from the primary circuit. The diodes in the secondary half-wave rectify the signal so that a train of positive sinusoidal pulses appear at the DUT during the timed interval.

Thyristor blocking voltage is measured with the gate open-circuited. All switches are set in the single-pulse mode with the voltage set to 0 V. The toggle switch connected to RS1 of the counter is switched to 5 V to reset the outputs; the switch is then toggled to ground to permit one pulse to appear across the DUT. The counter is again reset and triggered with the output of the variable transformer increased to some voltage greater than zero. The process is continued until the rated blocking voltage is reached; anode leakage current is measured at this value. The reverse leakage current is measured with the anode and cathode polarities reversed from their forward leakage configuration. Leakage current measurements for a train of continuous pulses are made the same way, except that all switches are placed in continuous mode, placing the mechanical timer in the circuit and short-circuiting the SCR. Typical open circuit single pulse and repetitive pulse voltages are shown in figure 3.



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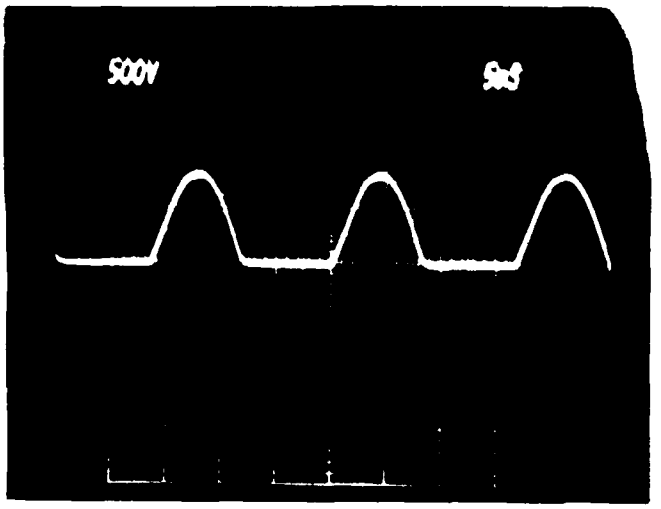


b.

Figure 3. Open circuit output voltages for a) a single pulse; b) repetitive pulses.

2. Gate-Cathode Diode Characteristics

The limiting rate at which a thyristor turns on depends on the amount of power which can safely be dissipated in the region where switching is initiated. A current flows between the gate and the cathode in the p-base when a trigger pulse is applied to the gate; the accompanying lateral voltage drop establishes a greater forward bias at the emitter edge nearest the gate than at the rest of the emitter, and only a small part of the device directly adjacent to the gate turns on. Once forward conduction begins, the gate loses control, and gating current can be supplied to the remaining off portions of the thyristor only by carrier diffusion from the adjacent on-region. A considerable time may elapse before the entire cathode area turns on, and during this time the entire anode current flows only through the small part of the total device area which has been turned on. At high values of dI/dt, high localized power dissipation and heating may damage the device. However, if the gate drive is increased, it is possible to increase the turned on region, and higher dI/dt may be obtained. In this work, the effects of very high values were to be examined, so that correspondingly hard gate drives were desired. The gate drive itself, however, is limited by the maximum power which can be dissipated at the gate-cathode junction. No such values could be obtained from the manufacturer's literature, so that a measurement of the maximum current which could safely flow through the gate was required. Inasmuch as only a pulsed current would flow during the actual

stress, a pulsed measurement was designed, in which a sequence of widely separated pulses, whose widths were the same as the gating pulse to be used during the measurement, and the amplitudes of which increased linearly during the sequence, could be delivered to the gate. The maximum gate current would then be that value just before gate burnout. This measurement could also be used to determine if any changes in the gate-cathode forward characteristics at high gate currents occurred after dI/dt stress. (Changes at lower currents could be safely observed using a curve tracer).

The circuit shown in figure 4 has a family of sixteen current pulses as its output. The first pulse has the lowest amplitude, each succeeding pulse increasing in amplitude. The pulses are 100 μs long; there is 1.5 ms between pulses, so that the pulse period is 1.6 ms. The duration of the pulse train is 25.6 ms. The long interval between pulses permits the gate-cathode diode to recover from any transient effects of one pulse before the next pulse appears. The interval between pulse trains may be increased up to 1.8 s even more to reduce heating. The maximum current pulse amplitude can be varied between 100 μA and 12 A.

The pulses are controlled by two timers. One timer is biased for an output pulse exactly 100 μs wide; the other is biased such that its output, by way of a toggle switch, can reset the counters after one pulse train, then enable another train after some time interval (up to 1.8 s). The potentiometer (R3) on the first timer sets the current pulse width (the clock

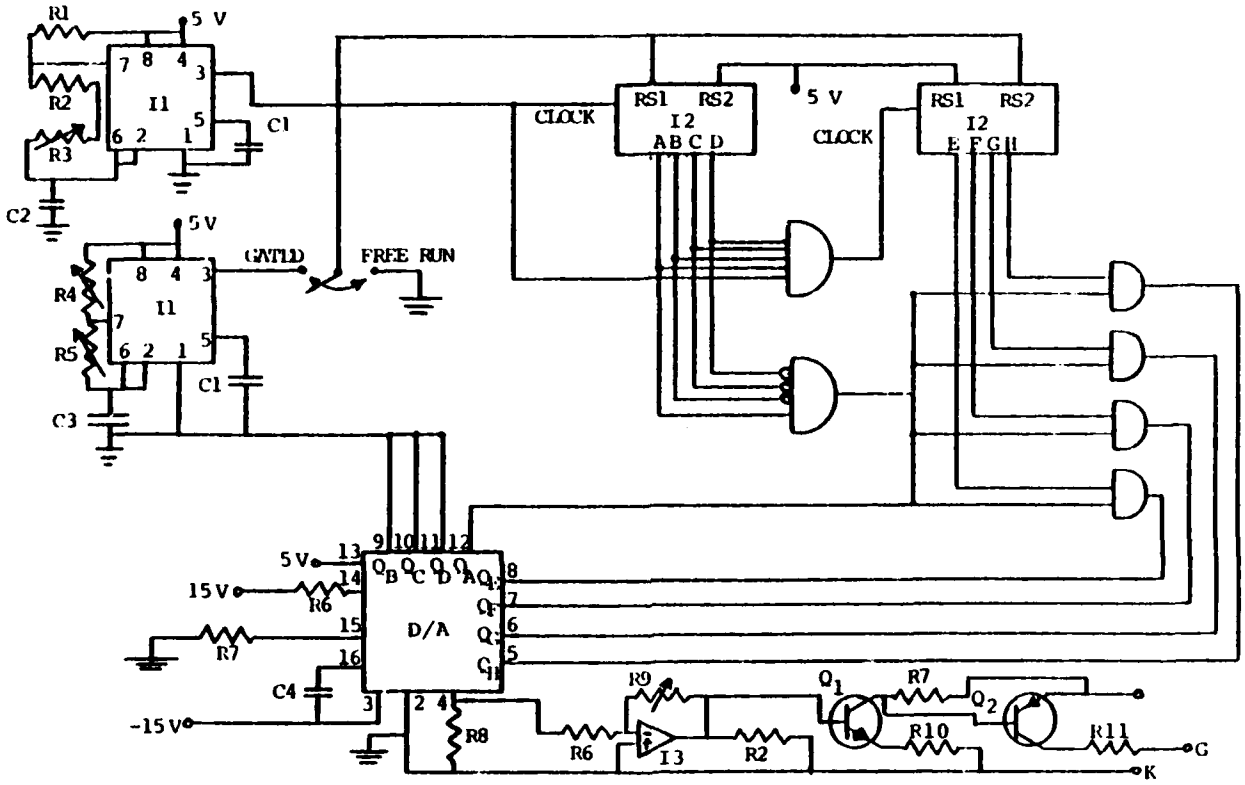


Figure 4. Gate-cathode diode test circuit. Resistors: R1, 5.6 KΩ; R2, 4.7 KΩ; R3, 15 KΩ; R4, 250 KΩ; R5, 5 KΩ; R6, 3.3 KΩ; R7, 1 KΩ; R8, 2.2 KΩ; R9, 10 KΩ; R10, 56 Ω; R11, 1 Ω. Capacitors: C1, 0.01 μF; C2, 5.6 nF; C3, 10 μF; C4, 15 pF. Transistors: Q1, 2N5002; Q2, 2N5003. Integrated circuits: I1, NE555 timer; I2, SN7493 counter; I3, SN72741 operational amplifier; D/A, MC1408L8 digital-to-analog converter.

period) to 100 μs. The potentiometer (R5) on the second timer sets the duty cycle such that exactly one sequence is enabled; following the first sequence, the counters are disabled for a time determined by the potentiometer R4. A timing diagram is shown in figure 5. The switch sets either timed or free running operation (by setting RS1 to 0 and removing the second timer from the circuit).

The output of the first timer is connected to the clock input of the first 4-bit counter. This counter has the four least significant bits, starting with A. The 4 bits are logically ANDed with the clock pulse to provide a clock pulse for the second counter, which generates the four most significant bits, every 1.6 ms. Outputs B, C and D are inverted and tied to a 4-input AND gate. The output of this gate, Q_A, is high at BCD 1, and low for BCD 0 and BCD 2 through 15. This output then has a period of 1.6 ms. Counter outputs E through H are individually ANDed with Q_A. Each AND gate output is tied directly to its appropriate input on the digital-to-analog converter, D/A. Outputs Q_B, Q_C and Q_D are tied to 0 V. Q_A, Q_E, Q_F, Q_G and Q_H are forced to 0 V during the 1.5 ms when B, C or D is at a logic high, and then allowed to take on their corresponding high or low, for 100 μs, from the counter outputs. In this way, the D/A receives a non-zero input for BCD 1, 17, 33, 49, 65, 81, 97, 113, 129, 145, 161, 177, 193, 209, 225 and 241. The remainder of the D/A biasing circuit outputs the proper voltage to the amplifier. The output of the D/A is a stairstep voltage waveform; there are

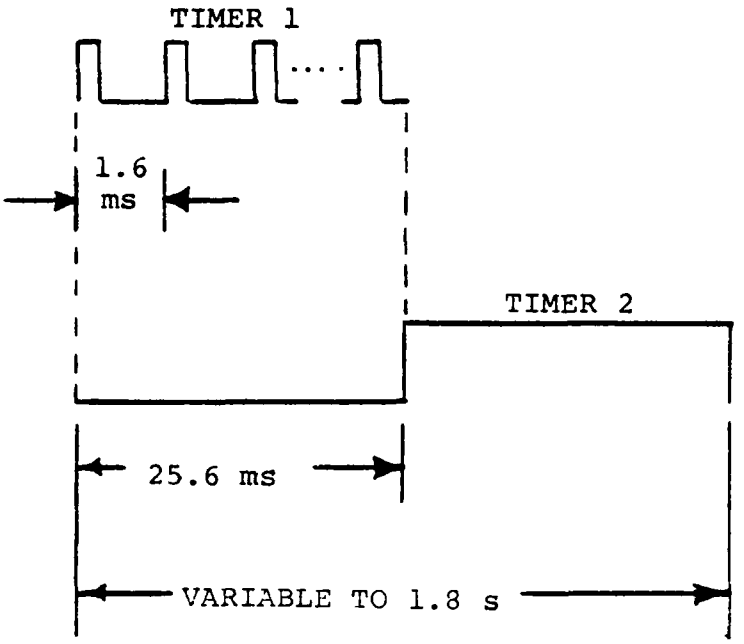


Figure 5. Timing diagram for the timer outputs.

16 steps, each 100 μs long, with 1.5 ms between pulses. The step levels increase in 0.31 V increments to 5 V at the sixteenth pulse. This waveform (figure 6) is fed to the amplifier for voltage gain and isolation from the D/A converter. The amplifier output drives the base of an n-p-n transistor, whose output drives a p-n-p transistor which acts as a current source. Gate current is measured across the sampling resistor, R11. The pulsed gate current vs. gate-cathode voltage characteristic curve is displayed in the x-y mode on an oscilloscope.

3. Gate Trigger Characteristics

The gate trigger current and voltage are measured with the circuit of figure 7. The anode-cathode voltage is set to 12 V, and the gate-cathode voltage is slowly increased until the device switches on. The values of gate current and voltage at this point are the trigger values.

4. Anode Holding Current

The circuit for measuring the anode holding current is shown in figure 8. The gate supply voltage, V_{GK}, is initially set to zero, as is the anode series resistance, R. V_{GK} is slowly increased until the anode-cathode voltage, V_{AK}, drops from 12 V to 1 or 2 V, that is, until the thyristor turns on. The gate is then open-circuited, and remains open-circuited during the measurement. R is then slowly increased until V_{AK} again increases to 12 V, that is, until the device turns off. The anode

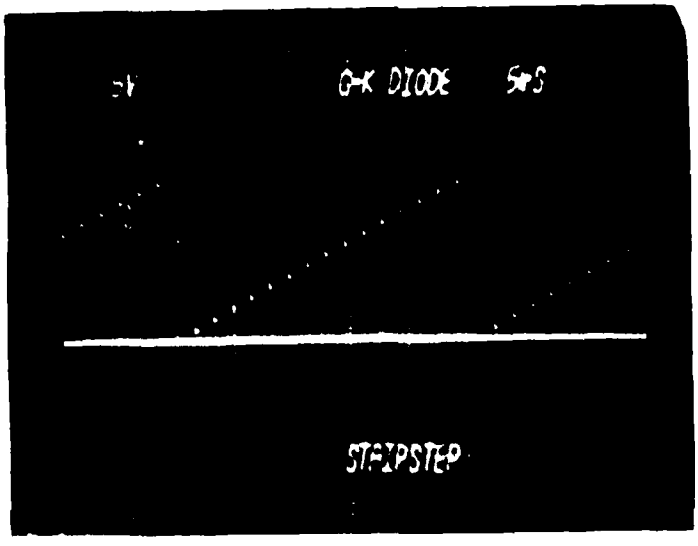


Figure 6. Stairstep output of the digital-to-analog converter.

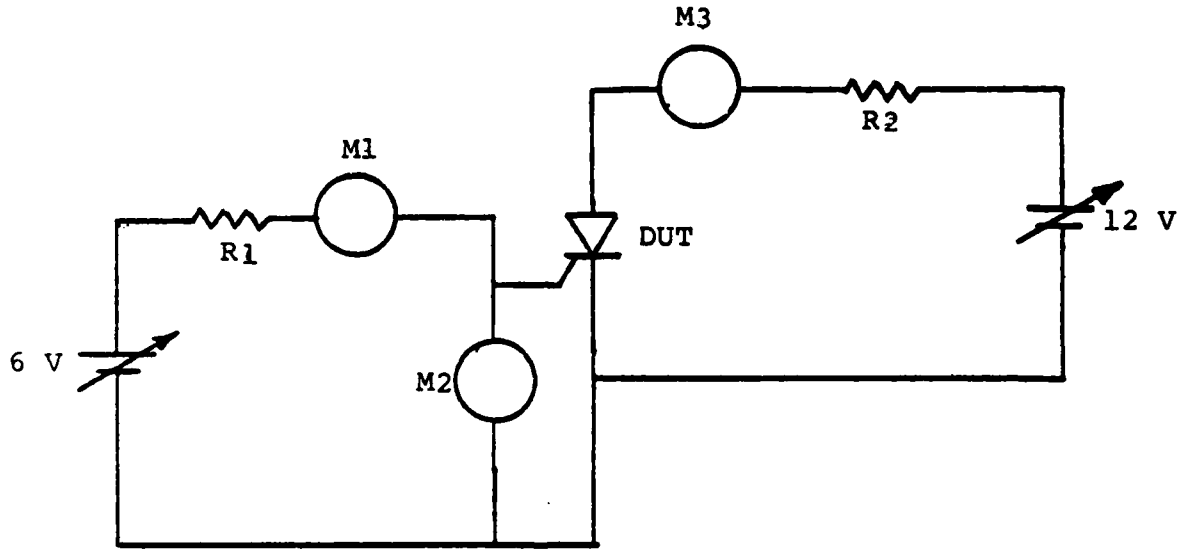


Figure 7. Circuit for the gate trigger measurements. R1 and R2 are 10 Ω, 5 W and 7 Ω, 25 W resistors, respectively; M1 is the gate trigger current ammeter; M2 is the gate trigger voltage voltmeter; and M3 is the anode current ammeter.

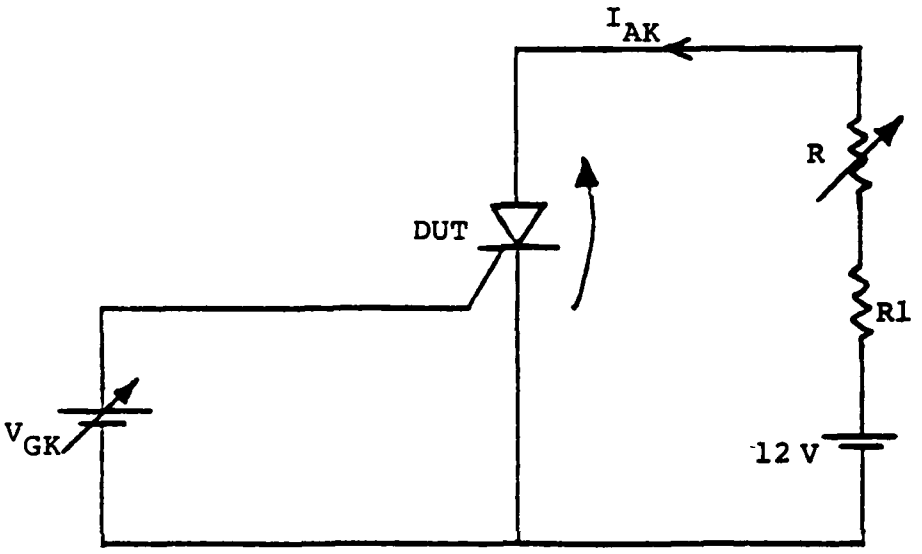


Figure 8. Anode holding current measurement circuit.

current measured just before the transistor turns off is the holding current.

5. Anode Forward Current-Voltage Characteristics

The thyristor is triggered on, after which the gate supply is disconnected. The anode forward current-voltage characteristics are then obtained by varying the anode current and measuring the anode-cathode voltage at a specified current (figure 9). The anode source in these measurements was an HP 6464C high current (500 A) supply.

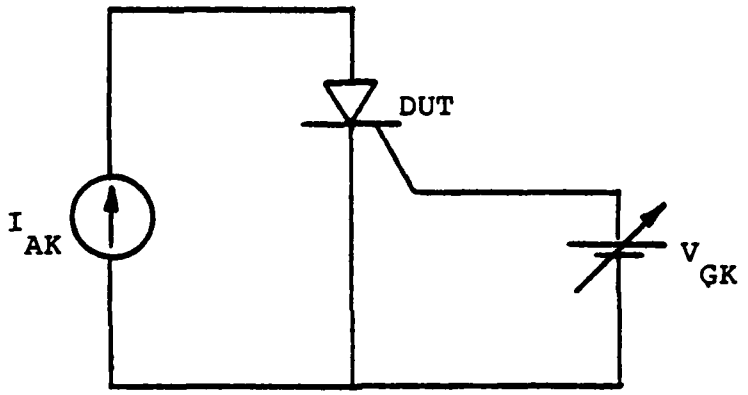


Figure 9. Measurement circuit for the forward voltage drop.

III. TEST CIRCUITS

1. Pulse Forming Networks

Transmission lines cannot be used for generating pulses even of moderate width unless impractically long lines are used; practical circuits are lumped equivalent networks of transmission lines (figure 10). However, high dI/dt pulses are difficult to obtain from pulse forming networks unless the pulses are narrow. In order to obtain the high dI/dt values required as stresses in this work, it was decided to use a pulse around 10 μs wide for the stress pulse. Inasmuch as transient turn-on in the test device was to be examined at this time, a short pulse was considered to be adequate. However, it was desirable to obtain the forward voltage drop at full turn-on, so a longer pulse, around 100 μs wide, was required as well; the rise time of this pulse would be much slower. In both cases, the peak current was chosen to be around 1000 A, approximately twice the rated average current of the test devices. For an 800 V PFN, in which one-half the voltage is dropped across the internal impedance, this required a matched load of 0.4 ohm.

Two pulse forming networks were therefore designed, employing a design program at the Los Alamos National Laboratory. The first was a 12 section, equal inductance, equal capacitance, type E PFN, whose output was a 100 μs pulse with a rise time of around 0.5 μs. Physically, the network was designed to consist of 12

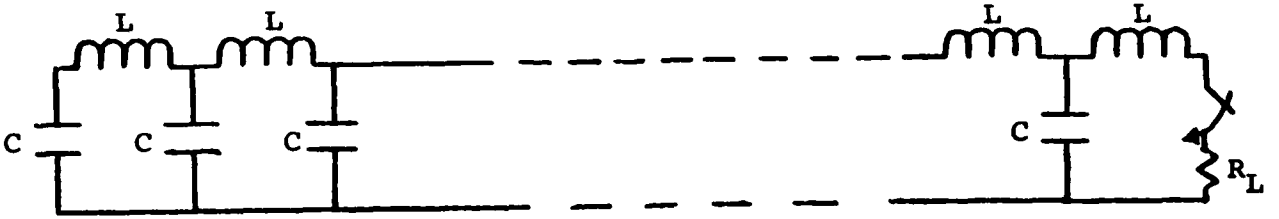


Figure 10. Lumped equivalent of a transmission line (Type E PFN).

sections, each 4 cm long, each consisting of a 1.5 cm radius, 9 turn coil (1.34 μH inductance) and a 10 μF capacitor. Figure 11 shows the simulated output of the PFN obtained with the LANL Net-2 circuit analysis program. The second PFN was a 125 section equal inductance, equal capacitance, type E network; each section was 1.5 cm long, consisting of an 0.75 cm radius, 1 turn coil (10.2 nH) and an 0.1 μF capacitor. This PFN, charged to 800 V, delivers a 1000 A, 10 μs pulse, with a 100 ns risetime, to a matched load. Figure 12 shows the rise time associated with the first 10 sections (0.8 μs pulse width: the width is increased by adding series sections). The rise time can be varied with an appropriate series inductance; figure 13 is a plot of the output pulse with series inductances of 100, 200 and 500 nH. This network is sensitive to stray inductance (although a capacitor series inductance up to around 10 nH does not affect the network seriously) so that the device fixture inductance is important.

For the 100 μs PFN, a continuous inductor, around 19 inches long, was helically wound on a cylindrical Teflon core, using 8 gauge annealed copper wire. (This has a room temperature resistance of 20.6 micro ohms per cm, corresponding to a total resistance of 0.012 Ω (5% of the load) for the 100 μs PFN, and of 0.012 Ω (3% of the load) for the 10 μs PFN.) The L-C sections were obtained by introducing short capacitors to a ground plane at appropriate locations along the inductance. GE 26F6626, 10 μF, 680 VAC capacitors were used in the 100 μs PFN. (These operate safely at 1000 VDC.) The load for this PFN was formed

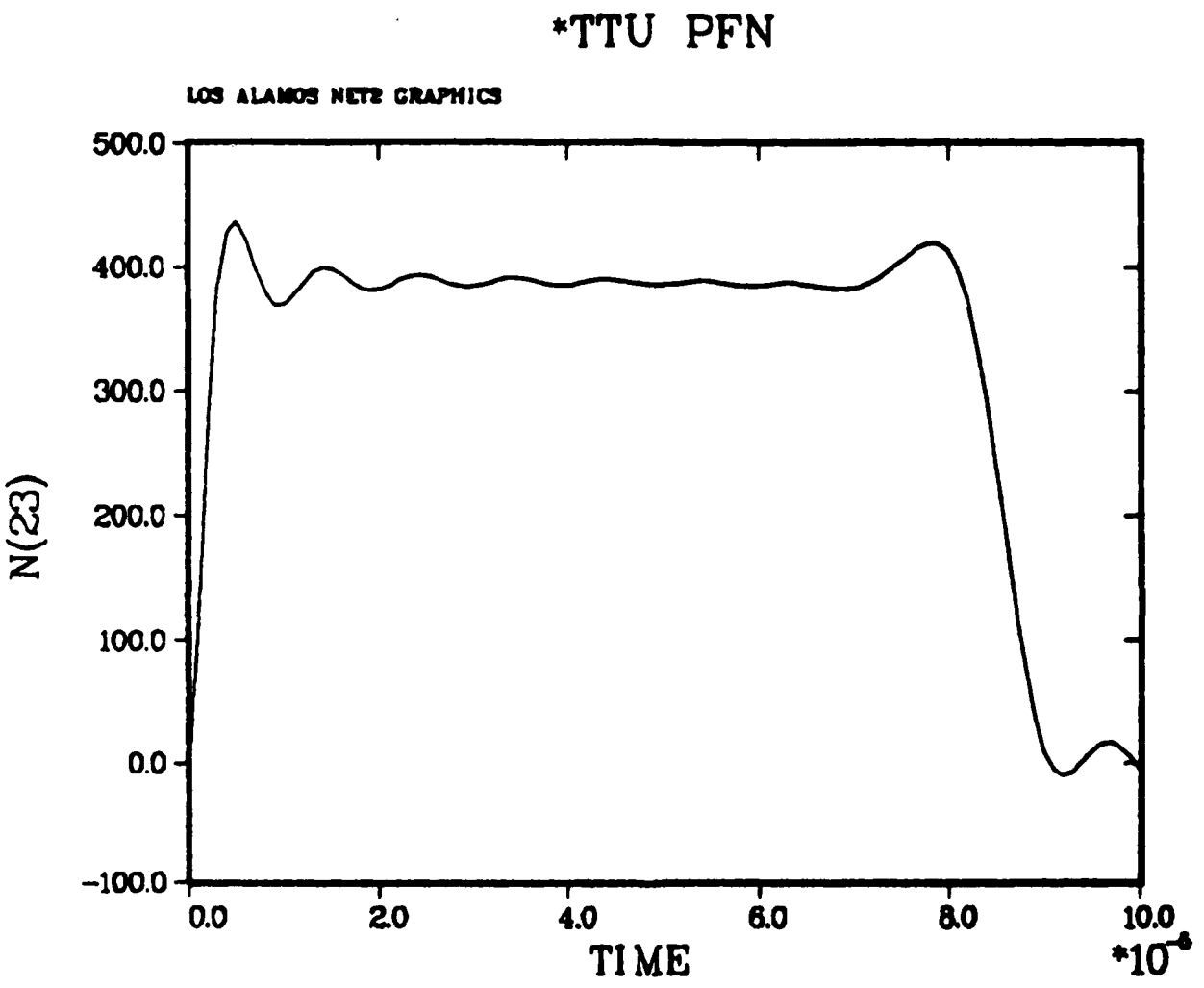


Figure 11. Simulated output of the 100 μs PFN.

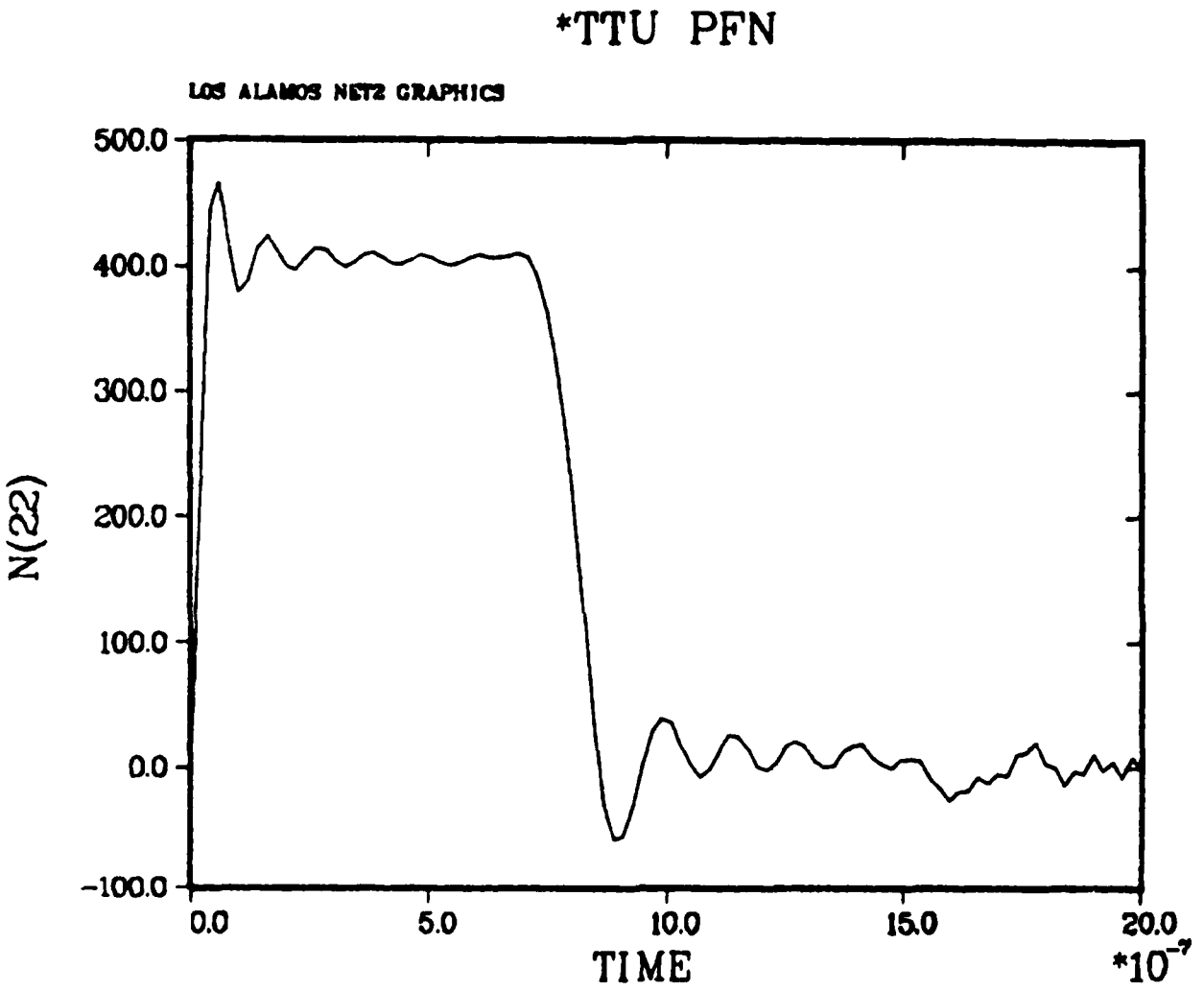


Figure 12. Simulated output of the 10 μs PFN (10 sections).

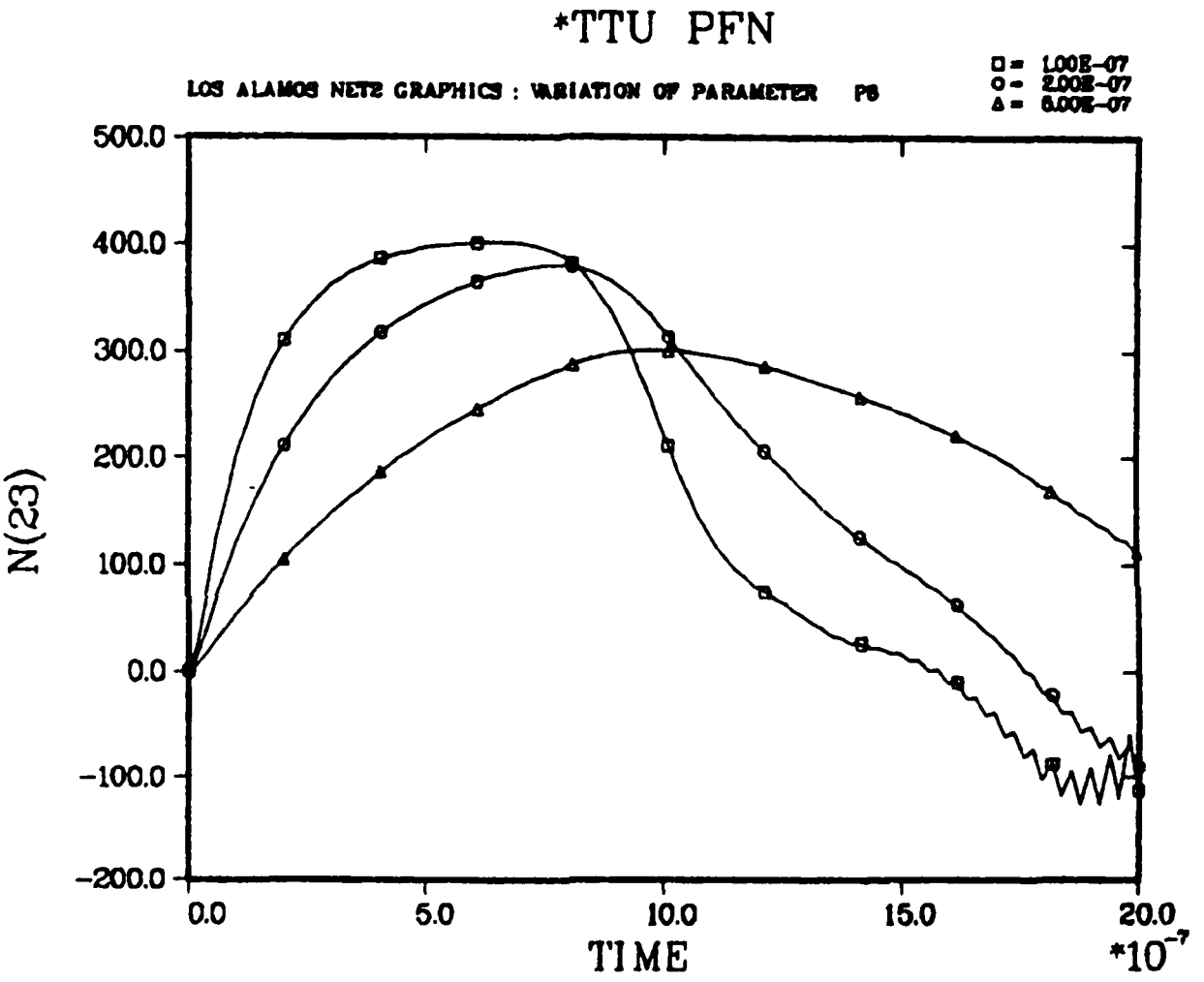
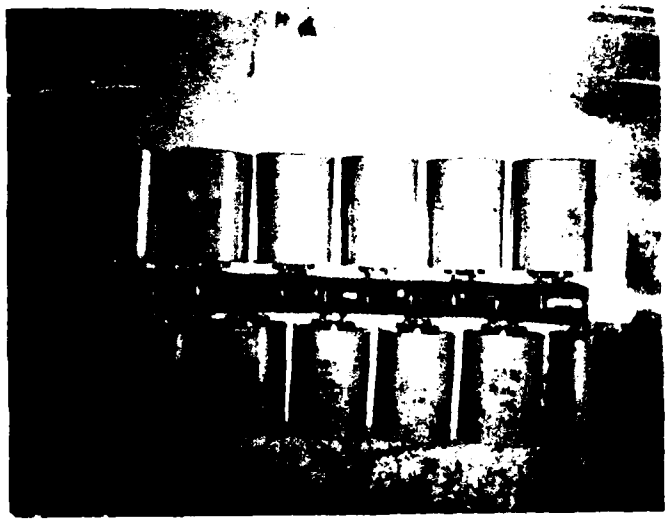


Figure 13. Effect of series inductance on the 10 μs PFN output pulse.

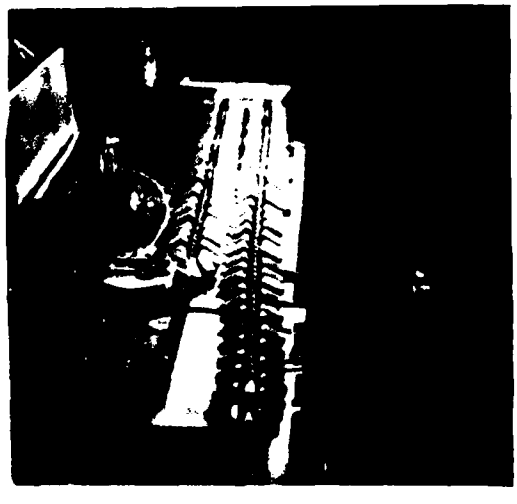
from a parallel array of eight 3.2 ohm, 2 watt carbon composition resistors. The inductor for the 10 μs PFN was similarly wound on a Lucite core; in this case, the total length of the coil, around 74 inches, was not convenient, so the PFN was folded into two sections, each some 37 inches long. This PFN incorporated Sprague 10PS-P10, 0.1 μF, 1000 VDC capacitors. The load here was a T and M Research Products Series A, Model BNC-5-4, 0.4 Ω (0.3972 Ω), low inductance current viewing resistor. Figures 14a and 14b, respectively, are photographs of the 100 μs and 10 μs PFNs.

The PFNs were energized by charging them to 800 V through a 1 MΩ series resistance. Their pulse characteristics were determined by discharging them through their loads and measuring the load voltages. In order to avoid introducing switching artifacts, the PFNs were discharged using a fast discharge switch. This switch consists of two brass electrodes separated by a Mylar layer and a lead sheet. The switch is closed by driving a nail through the top brass electrode and the Mylar layer into the sheet of lead, which rests on the bottom brass electrode, and which prevents bounce. The nail, driven by a hammer, closes the switch in times much shorter than the rise time of the output pulse.

Typical output pulses are illustrated in figure 15 (100 μs PFN) and 16 (10 μs PFN). The measured output of the 100 μs PFN (figure 15a) has very similar characteristics to those predicted by the pulse simulations (figure 11). The predicted width is around 90 μs; the observed width is around 100 μs. The rise time

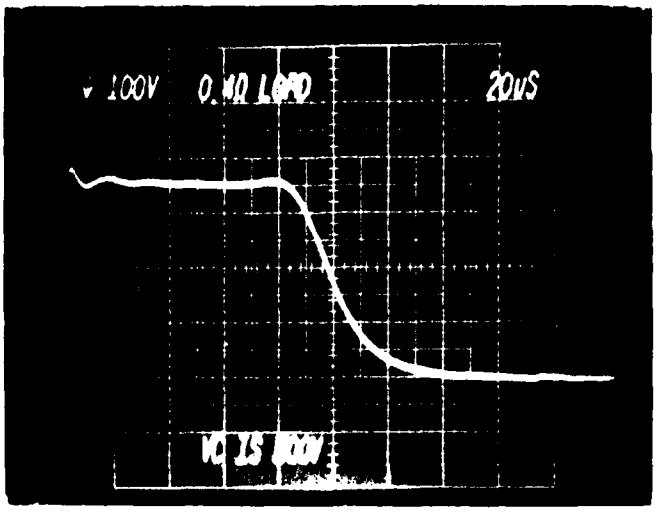


a.



b.

Figure 14. Photographs of the PFNs: a) 100 μs; b) 10 μs.



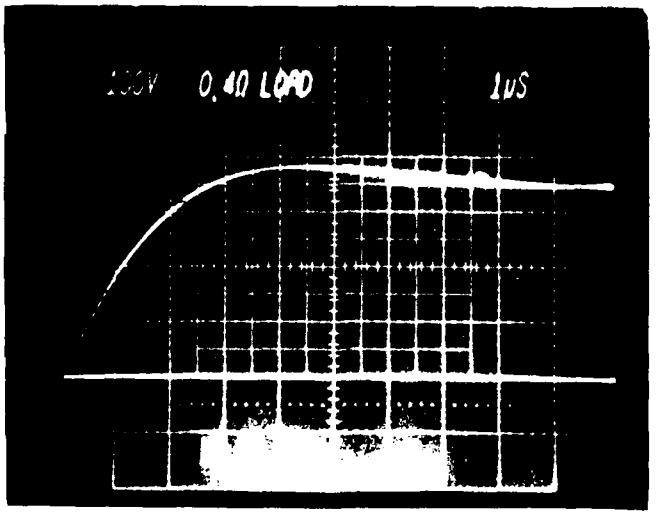
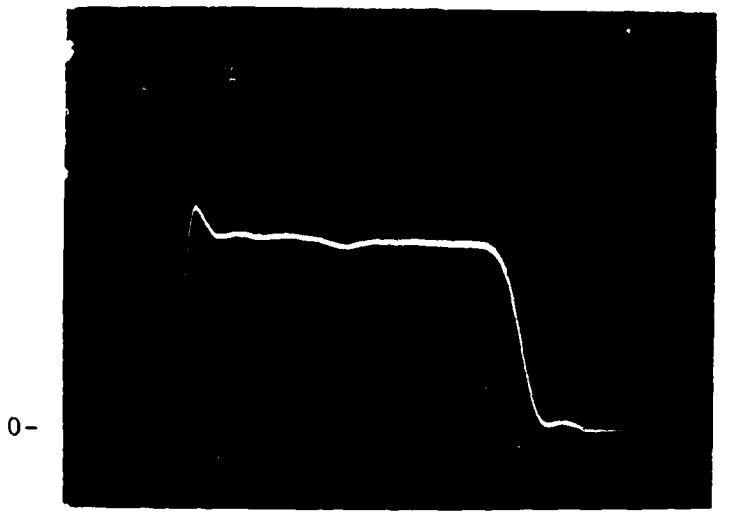
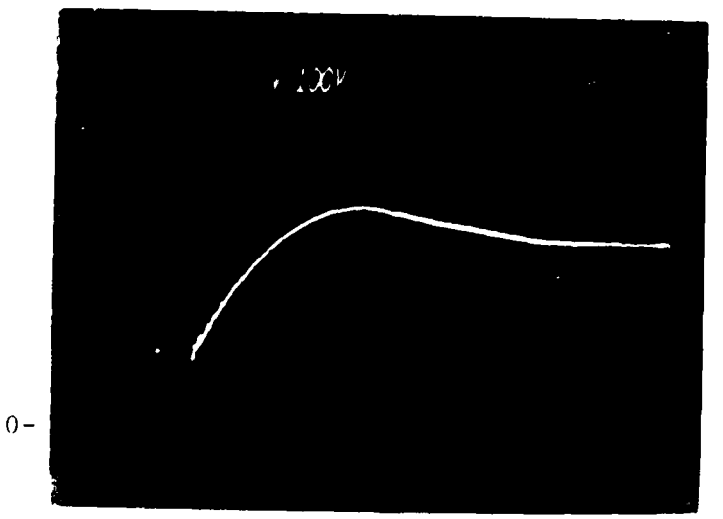


Figure 15. Output pulse of the 100 μs PFN: a) entire pulse; b) pulse leading edge. The horizontal scale for the upper photograph is 20 μs per large division and, for the lower photograph, 1 μs per large division. The vertical scale for both photographs is 250 A per large division.



a.



b.

Figure 16. Output pulse of the 10 μs PFN. a) entire pulse; b) pulse leading edge. The horizontal scale for the upper photograph is 2 μs per large division and for the lower photograph, 200 ns per large division. The vertical scale for both photographs is 250 A per large division.

of the simulated pulse (to 800 A) is around 2.4 μs (330 A/μs); that of the actual pulse (shown on an expanded time scale in figure 15b) is around 2.2 μs (360 A/μs) to 800 A. The observed current at the flat portion of the pulse is 900 A; the predicted current is around 960 A.

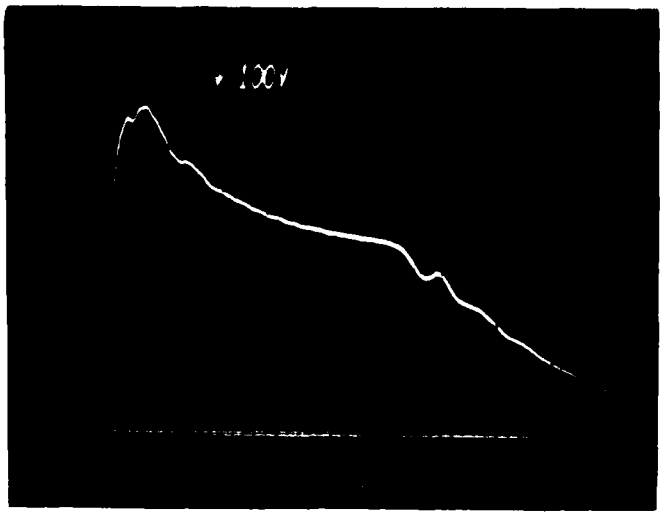
Agreement between the simulated and observed output pulses for the 10 μs PFN is not so good. Predicted values (figure 12) of rise time (to 800 A) and peak current are around 60 ns (13300 A/μs) and 1000 A, respectively (10 sections only: pulse width is scaled); the observed pulse (figure 16) has a peak current of 850 A and a rise time to 800 A of 340 ns (2350 A/μs).

The output pulses were obtained by measuring the voltages across the PFN loads. In both measurements, a Tektronix P6057, 100X, 1.4 GHz probe was used, with a Tektronix 7A19, 600 MHz plug-in amplifier in a 7834, 400 MHz mainframe, so that the measurement was not band-limited by the measuring instruments. The increased rise time and reduced peak current for the 10 μs PFN output pulse is very probably the result of series inductance (see figure 13). Although the load, the current viewing resistor, should be a low inductance configuration, the high dI/dt associated with the 10 μs output pulse could affect the observed rise time even across in low inductance load, so a comparison measurement was made using a Pearson 411 current transformer, with a rise time of 20 ns. The shapes of the pulses obtained with the load voltage measurement and the current transformer were the same, as were the rise times, so that the

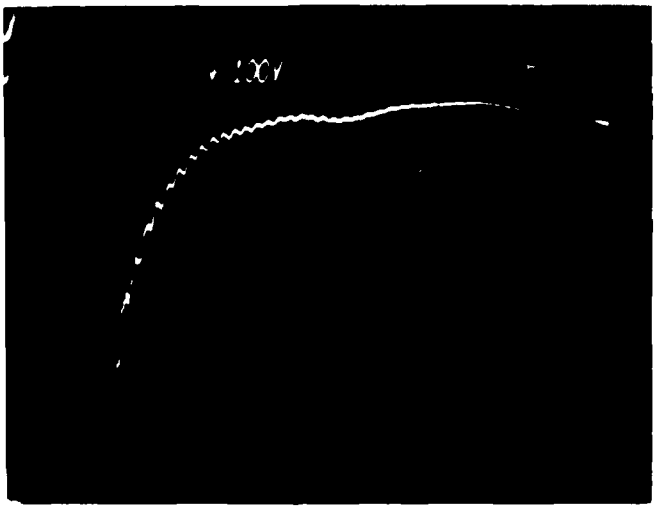
parasitic series inductance is in the PFN itself. In order to reduce the leading edge rise time, 30 turns of the inductor were shorted and an additional 10 μF of shunt capacitance was added at the PFN output. Figures 17a and 17b show the respective output pulse and leading edge; the pulse shape is degraded, but the leading edge dI/dt has been increased to around 8000 A/μs.

2. Gate Drive Circuit

A pulse commonly used when relatively high dI/dt is desired has a fast leading edge, with a current peaking at around three to five times the minimum trigger current, and decaying to a steady value, usually the minimum trigger current; the overall decay time to the steady value is approximately 20% of the pulse width, which is around 100 μs, at the end of which time the thyristor is completely turned on. This pulse shape was chosen for the gate drive in this work, but because very fast pulses were to be switched by the test thyristor, a very high peak current, 10 A or more, was selected, with a final steady value of around 5 A. This shape was to be used for both the 100 μs characterization pulse and the 10 μs stress pulse, except that, in the latter case, the overall gate pulse width was reduced to the stress pulse width, with a proportionally reduced decay time. However, the actual gate drive in this work differed from conventional gate drives in another significant respect. The gate drive circuit is commonly isolated from the switched circuit by a pulse transformer; wave shaping is performed on the primary



a.



b.

Figure 17. Output pulse of the modified 10 μs PFN: a) complete pulse; b) pulse leading edge. The horizontal scale for the upper photograph is 2 μs per large division and, for the lower photograph, 200 ns per large division. Ther vertical scale for both photographs is 250 A per large division.

side of the transformer, with some peaking occasionally done on the secondary side. The gate is then driven by a voltage pulse, and the gate current pulse may have a distorted shape. In order to assure that the gate current pulse had the desired shape, the gate was driven from a pulsed current source (figure 18).

In order to obtain a constant current, the source output resistance must be high relative to the load resistance; in this case, the gate-cathode diode. In that case, in order to obtain a high peak current, the source voltage must also be high; a high voltage switch is then required to discharge the pulse shaping circuit. An IRF610 power MOSFET was selected as the switch because of its high breakdown voltage, relatively low input capacitance, and fast switching rise time. A fast switching diode, the 1N5804, is placed antiparallel across the gate-cathode diode to clamp any reverse voltage when the thyristor switches on. The gate of the FET was driven by both Systron Donner 101D and HP 214A pulse generators; both deliver a 15 V pulse with rise times of around 25 ns. Because the cathode of the test device was tied to the system common during stress, the entire gate trigger circuit was floated with respect to system common.

A typical 100 μs gate trigger pulse is shown in figure 19a. The load is the gate-cathode diode of a test thyristor with an anode-cathode short. Gate current is measured with a Pearson Model 2878 current transformer, which has a rise time of 5 ns. The gate current pulse is 100 μs wide, with a peak current of 13 A and a steady value of 5.5 A; the decay time is around 20 μs

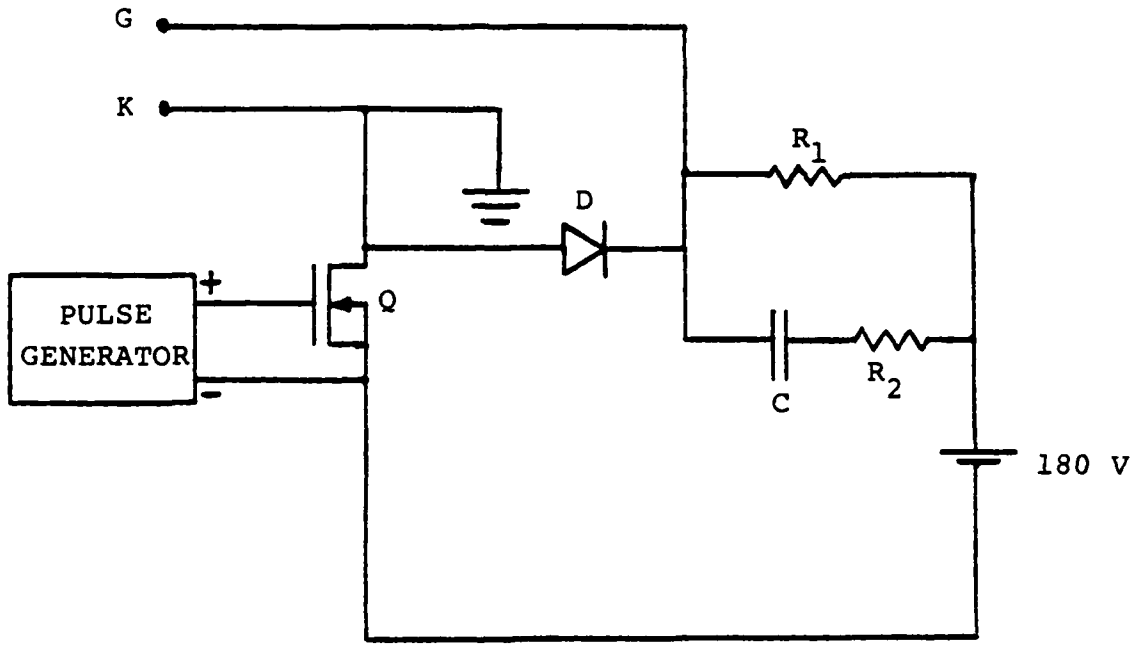
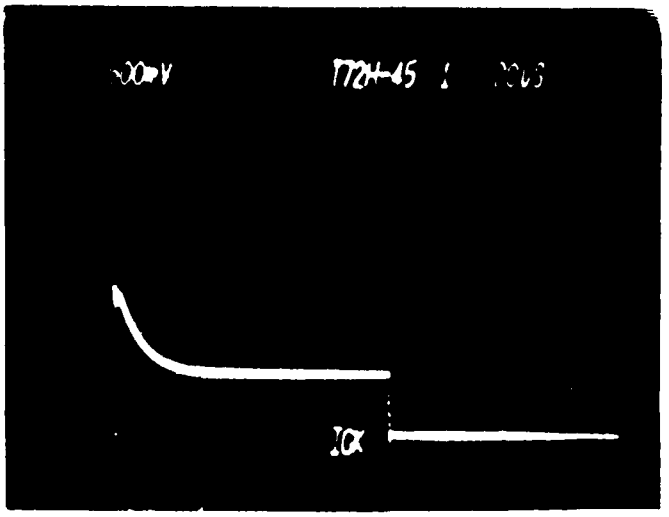
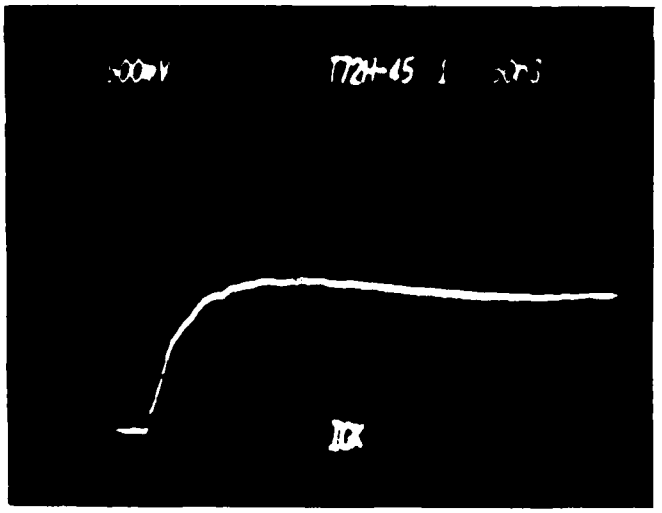


Figure 18. Gate trigger circuit. Q: IRF610; D: 1N5804; R_1: 33 Ω; R_2: 15 Ω; C: 0.47 μF (100 μF pulse), 0.056 μF (10 μs pulse).



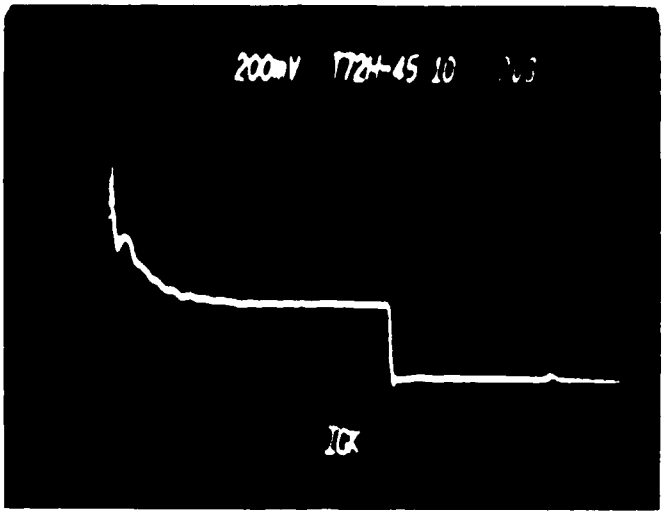
a.



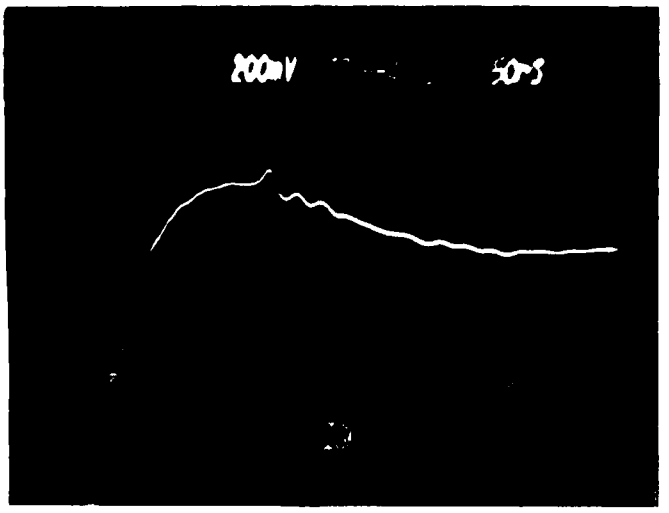
b.

Figure 19. Typical 100 μs gate trigger pulse: a) entire pulse; b) pulse leading edge. The horizontal scale for the upper photograph is 20 μs per large division and, for the lower photograph, 50 ns per large division. The vertical scale for both photographs is 5 A per large division.

to 30 μs. The leading edge of the pulse is shown in figure 19b; the current rises to 10 A in around 40 ns and to 13 A in 70 ns. The 10 μs trigger pulse and pulse leading edge are shown in figures 20a and 20b, respectively. The pulse width here is 10 μs, the peak current is around 14 A, the steady current value is 5 A, and the decay time, 2 μs to 3 μs. The current rise time is 40 ns to 10 A and 70 ns to 13 A. Current is measured with the Pearson Model 2078 current transformer; the slight ringing which is observed may be the result of switching by the test thyristor, which here switches 800 V.



a.



b.

Figure 20. Typical 10 μs gate trigger pulse: a) entire pulse; b) pulse leading edge. The horizontal scale for the upper photograph is 2 μs per large division and, for the lower photograph, 50 ns per large division. The vertical scale for both photographs is 4 A per large division.

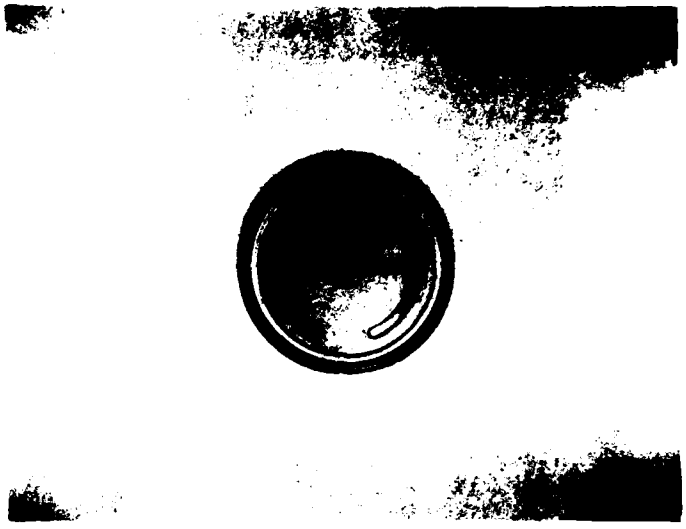
IV. MEASUREMENT PROCEDURES

1. Test Devices

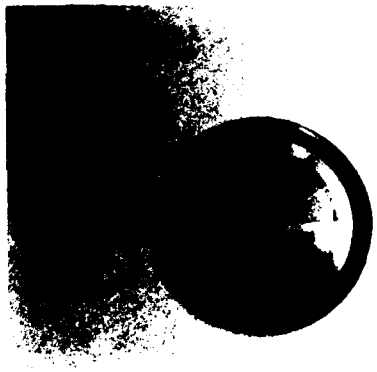
Two types of thyristors in compression packages, the T72H-45 and T7S7-60, were tested. Both are fast switching devices, differing principally in their gate-cathode geometries. The T72H084534DN has a rated repetitive peak blocking voltage of 800 V and an average forward current of 450 A; the T7S7086034DN is rated at 800 V and 600 A average forward current. (The specifications for the two devices are contained in the Appendices.) Both are 33 mm diameter devices with amplifying gates; however, the T7S7 is center-fired, whereas the T72H is slightly interdigitated (figure 21).

2. Measurement Protocol

Twenty devices, ten of each type, were electrically characterized initially. Five of each type switched the 10 μs PFN single-shot at step-wise increasing values of dI/dt until the maximum available value was reached. The remaining ten devices were repetitively pulsed at a high value of dI/dt, and recharacterized at logarithmic time intervals. Failure analysis consisted of the determination of gross fault modes by opening the packages and examining the device chips.



a.



b.

Figure 21. Gate structures for the test thyristors: a) interdigitated, with amplifying gate; b) center-fired, with amplifying gate.

3. Device Fixture

Commercial fixtures for compression packages have too high an inductance for these measurements, so a low inductance coaxial fixture was designed. The fixture was machined from aluminum, with the interior surfaces micromachined to obtain flat and parallel, good electrical and thermal contact. The two parts of the structure enclose the device, and are clamped together under 2000 pounds of force; figure 22 shows the two segments of the fixture. The bottom, or cathode section, is tied to system common. The top, or anode section, is connected to the PFN by way of four braided copper straps. An extra cathode lead and the gate lead are connected to the gate drive circuit through vertical slits in the fixture. Dow-Corning 340 heat sink compound was lightly applied to the anode and cathode surfaces of the device package before it was clamped.

4. Instrumentation

Waveforms were displayed on a Tektronix Model 7834 400 MHz storage oscilloscope, using a 7A19 600 MHz plug-in amplifier for very fast pulse, low impedance measurements, a 7A16A 225 MHz amplifier for fast pulse, high impedance measurements, and a 7A22 1 MHz differential amplifier for low frequency differential measurements. Chopped measurements were performed at the 1 MHz 7834 mainframe chopping rate. A 7B80 time base was used in all the measurements. Low current gate-cathode diode characteriza-

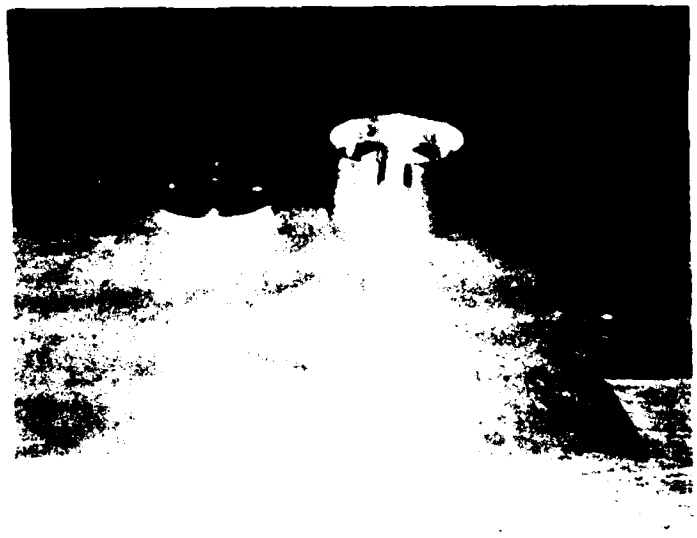


Figure 22. Low inductance device mounting fixture. The top section (anode) of the fixture is at the left, and the bottom section (cathode), at the right of the photograph.

tions were performed on a 7633 mainframe, using a 7CT1N plug-in curve tracer.

Fast low voltage pulse measurements were made with the Tektronix P6057 1.4 GHz, 100X, low impedance probe; this probe was used principally to measure the voltage across the load in the single-shot stresses. High voltage (anode and blocking voltage) measurements were made with the P6009 100 MHz, 100X, high impedance probe. Anode current in the repetitive stresses was measured with the Pearson 110 current transformer, which has a 20 ns rise time; this is a larger version of the Pearson 411 current transformer.

V. RESULTS AND DISCUSSION

1. Initial Characterization

a. Anode forward current-voltage characteristics.

Figure 23 is a graph of the anode forward current-voltage behavior for a T7S7 thyristor after turn-on. The curve is similar to that shown in the manufacturer's handbook (although the dip at low currents in this measurement is puzzling). The measurement was more troublesome to perform than anticipated, and the results were not as useful as those obtained from a pulsed measurement, so this characterization was not continued.

b. Device DC parameters.

The gate trigger current, I_{GT}, trigger voltage, V_{GT}, and anode holding current, I_H, (all with 12 V at the anode) for the twenty devices are contained in Table 1. The average values for the T7S7 thyristors are 51 mA for I_{GT}, 1.28 V for V_{GT}, and 41 mA for I_H, and for the T72H devices, 52 mA for I_{GT}, 0.89 V for V_{GT}, and 46 mA for I_H. The values for I_{GT} and V_{GT} are considerably lower than the specified values, which are 150 mA for I_{GT} and 3 V for V_{GT} for both types. No values are specified by the manufacturer for I_H. These measurements are not difficult to perform, but they are time consuming, and the values were not considered to be as sensitive to degradation as the other parameters, so they were not continued.

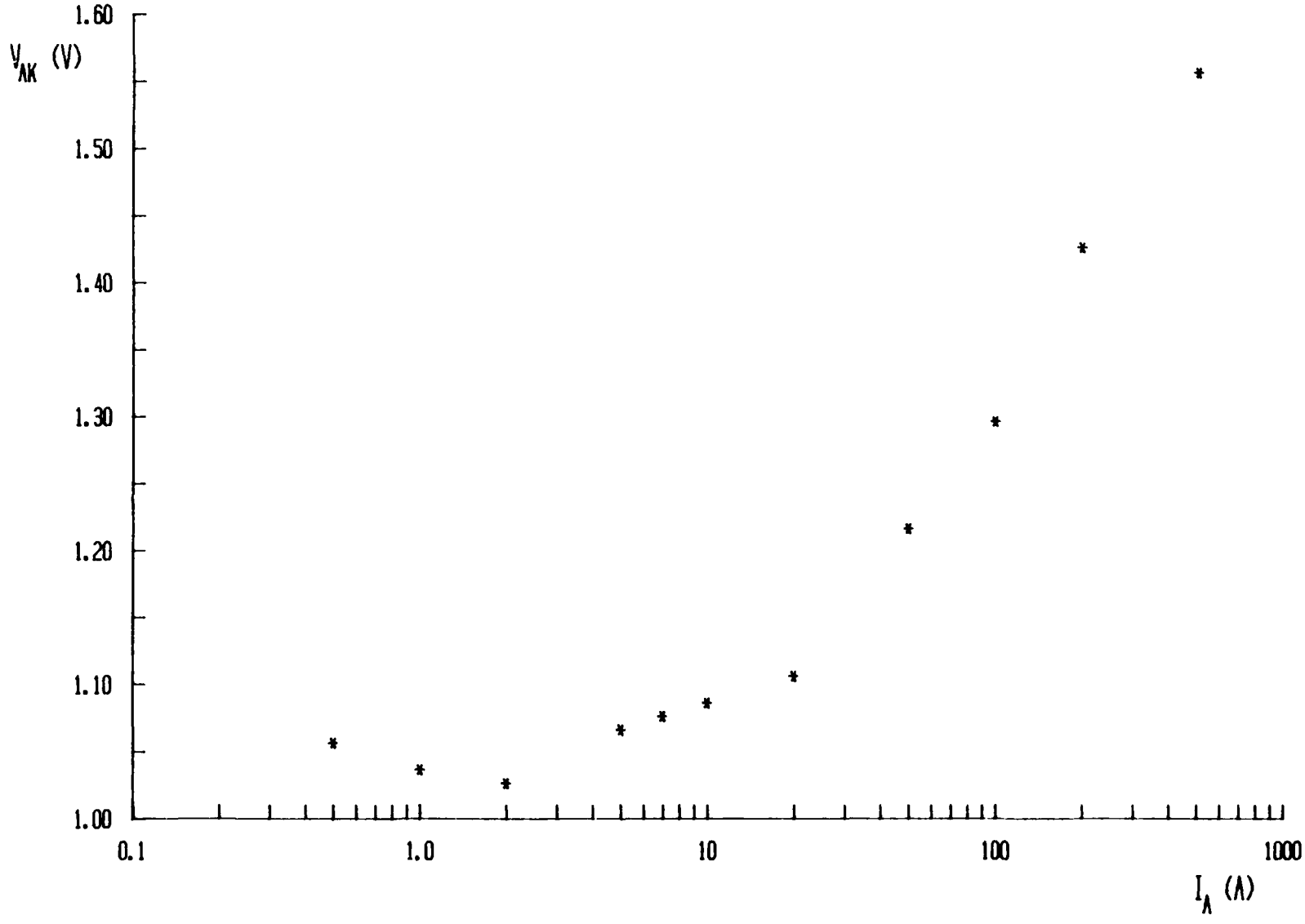


Figure 23. Anode forward current-voltage characteristic curve.

Table 1.

Device DC Parameters

T7S7

Device Number	I_{GT} (mA)	V_{GT} (V)	I_H (mA)
2	71	1.25	73
3	50	1.30	37
4	67	1.34	33
6	49	1.41	37
10	38	1.23	45
11	41	1.25	33
13	38	1.23	43
16	44	1.19	38
18	43	1.25	41
20	67	1.36	31

T72H

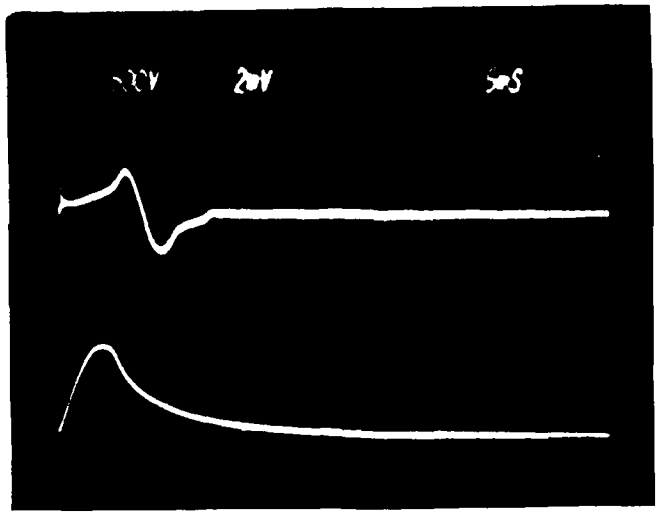
Device Number	I_{GT} (mA)	V_{GT} (V)	I_H (mA)
1	46	0.94	43
2	45	0.89	49
6	44	0.76	47
8	42	0.77	40
10	71	0.83	66
12	40	0.91	28
18	66	0.91	63
21	60	0.99	43
23	53	0.97	45
26	54	0.94	38

c. Blocking voltage.

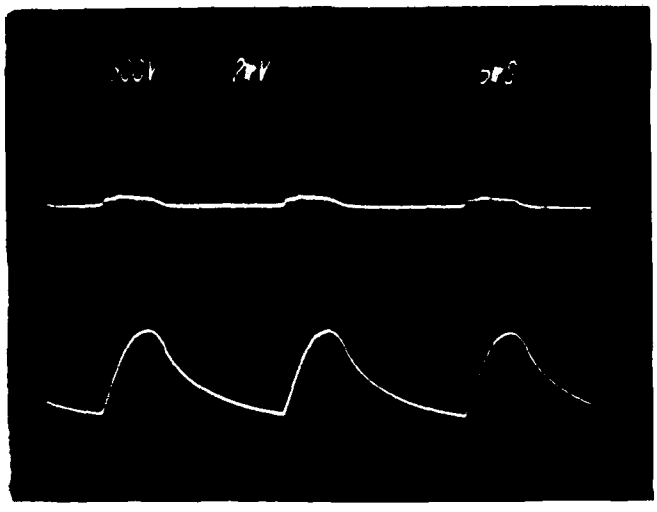
Figure 24 illustrates representative waveforms for forward single pulse (figure 24a) and repetitive (figure 24b) blocking. The current waveforms contain capacitive artifacts which are associated with the open circuit behavior of the blocking voltage test system, and which have no measurement significance. These appear in the reverse blocking waveforms also (not shown), which are very similar. The long tails on the voltage waveforms are the result of capacitive loading of the test circuit by the turned off thyristor. No significant room temperature leakage current ($\leq$ 500 μA) during forward or reverse blocking was observed in seventeen of the twenty devices tested; the other three, T72H-6, T72H-12 and T72H-23, exhibited asymmetric high leakage; that is, T72H-6 and T72H-12 blocked in the reverse direction, but not in the forward, and T72H-23 blocked in the forward, but not in the reverse, direction. Figure 25 shows the single-pulse forward and reverse blocking waveforms for T72H-12 and T72H-23, respectively. Repetitive blocking waveforms are similar, and similar results are obtained for forward blocking in the T72H-6.

d. Gate-cathode diode characterization.

Typical low current ($\leq$ 160 mA) gate-cathode diode characteristic curves are shown for the T72H and T7S7 devices, respectively, in figures 26a and 26b. These curves can be piecewise linearized into several regions (two in figure 26a and three in

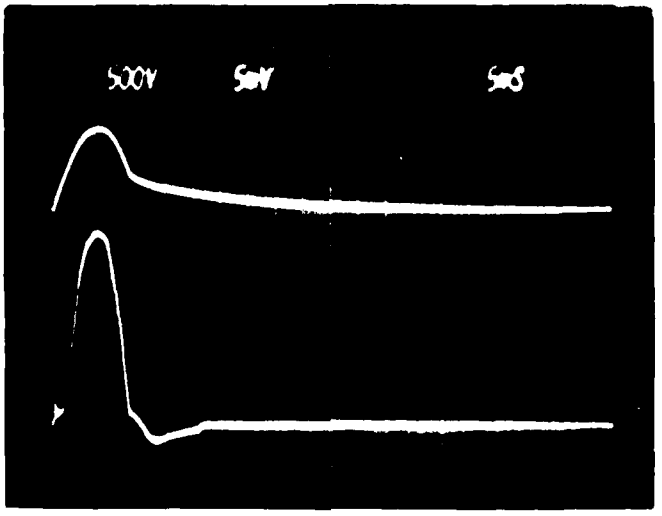


a.

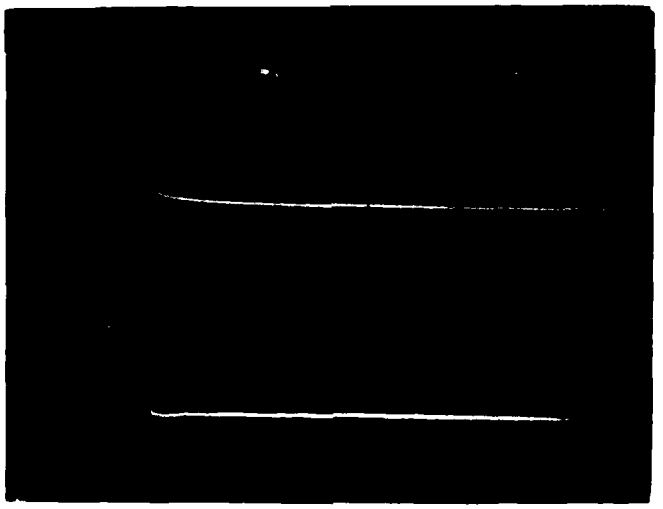


b.

Figure 24. Forward blocking voltage waveforms: a) single-pulse; b) repetitive. The upper curves in both photographs are current waveforms (2 mA per large division) and, the lower curves, voltage waveforms (500 V per large division). The horizontal scales for both are 5 ms per large division.

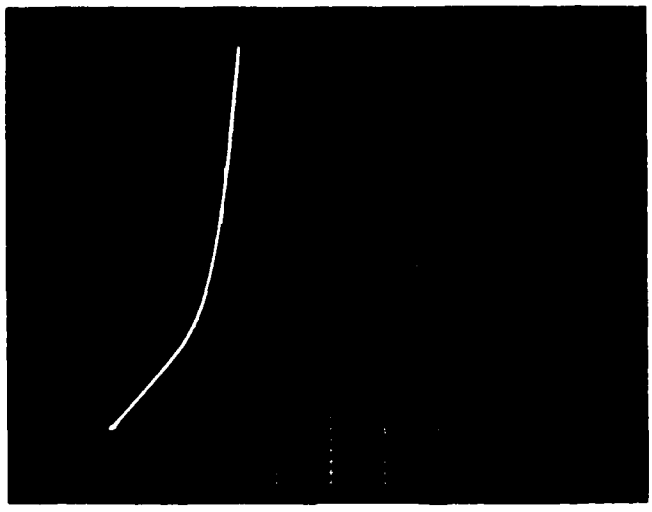


a.

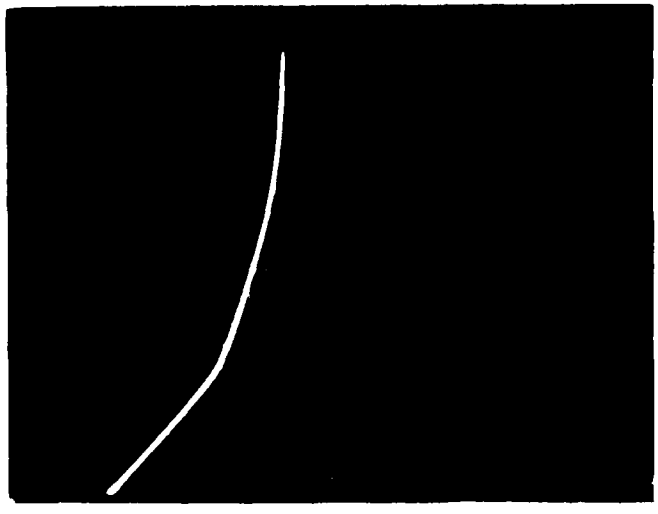


b.

Figure 25. Single-pulse blocking voltage waveforms: a) forward blocking in T72H-12; b) reverse blocking in T72H-23. The lower curves in both photographs are current waveforms (5 mA per large division) and the upper curves, voltage waveforms (500 V per large division). The horizontal scales for both are 5 ms per large division.



a.



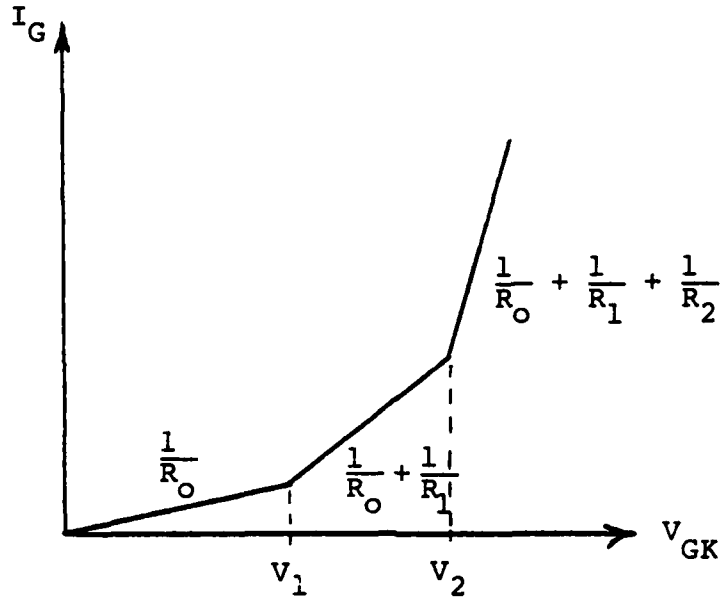
b.

Figure 26. Typical low current gate-cathode diode characteristic curves: a) T72H; b) T7S7. The vertical scales in both photographs are 20 mA per large division; the horizontal scales are 0.5 V per large division.

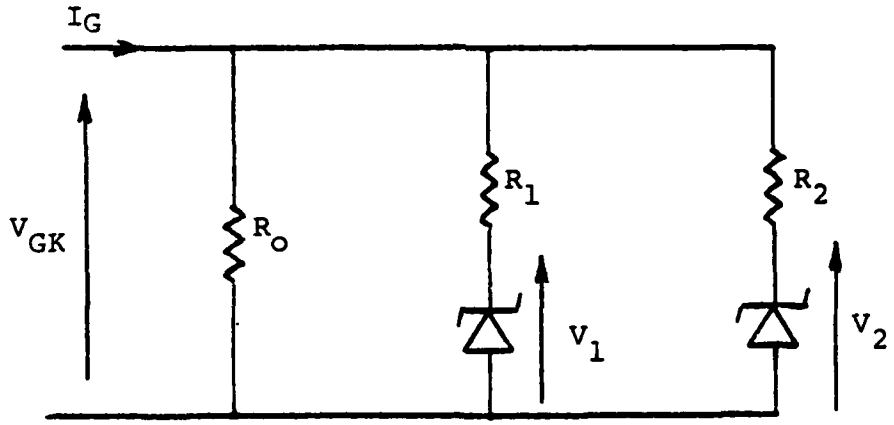
figure 26b), permitting characterization of the gate-cathode diode in terms of the resistance and voltage parameters identified in the model of figure 27. (Three breakpoints are shown in this model, but it can easily be modified to include only two.) The ideal Zener diode voltages correspond to the breakpoints in the linearization, and the resistances, to the slopes of the straight lines. Pulsed high current measurements were performed to 800 mA and to 12 A; these are illustrated in figure 28. The equivalent circuit parameters for the T72H and T7S7 devices are listed in Tables 2 and 3, respectively; in general, two breakpoints were obtained, except for the low current curves for the T72H devices, which contained only one. Only the 12 A pulsed measurements were performed in later recharacterizations.

e. Pulsed characterization.

Eighteen devices were pulse characterized by switching the 100 μs PFN. (T72H-6 and T72H-12, which did not block in the forward direction, were not used.) Representative current and voltage switching waveforms are shown in figure 29; the current waveform was obtained by measuring the voltage across the load, and the voltage waveform was obtained at the anode, relative to the cathode, which was tied to common. The current rise and voltage fall times are shown on expanded time scales in figure 30. The current rises to 750 A in 1.4 μs (540 A/μs) and to its peak value of 1000 A in 4 μs. The voltage falls in several stages: there is a relatively fast drop from 800 V to 600 V in

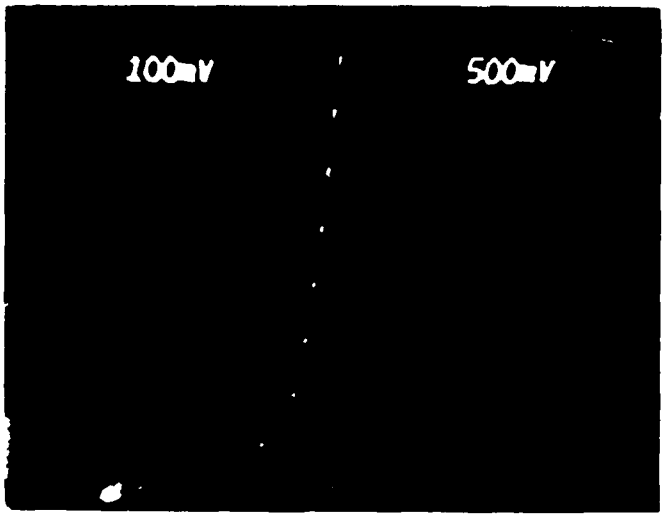


a.

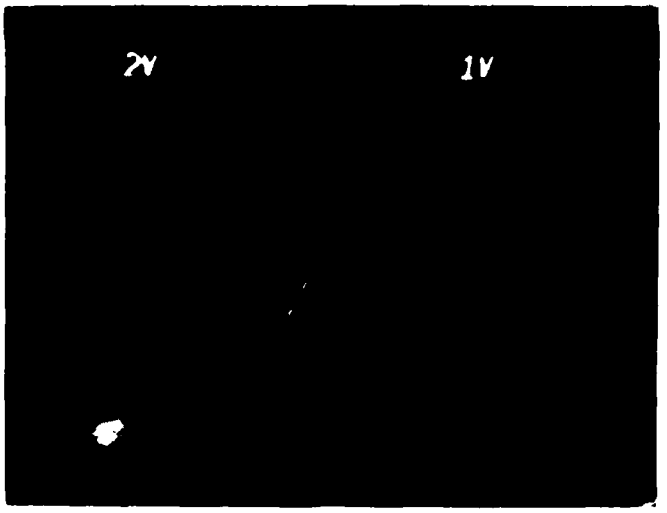


b.

Figure 27. Model for the piecewise linearization of the gate-cathode diode characteristic curve: a) three breakpoint linearization; b) equivalent circuit.



a.



b.

Figure 28. Pulsed high current gate-cathode diode characteristics: a) to 800 mA; b) to 12 A. The vertical and horizontal scales in the upper photograph are 100 mA per large division and 0.5 V per large division, respectively; in the lower photograph, 2 A per large division and 1 V per large division, respectively.

Table 2.

Piecewise Linearized Equivalent Circuit Parameters for the Gate-Cathode Diode Characteristic Curves for the T72H Thyristor

Low Current
($\leq$ 160 mA)

Device Number	1	2	6	8	10	12	18	21	23	26
R_o (Ω)	20.0	19.0	15.0	17.0	11.0	25.0	12.0	19.0	20.0	22.0
R_1^o (Ω)	3.0	3.0	1.5	2.2	1.6	2.8	3.4	3.2	3.0	2.7
V_1^1 (V)	0.88	0.86	0.81	0.80	0.79	0.89	0.85	0.90	0.88	0.91

Pulsed High Current
($\leq$ 12 A)

Device Number	1	2	6	8	10	12	18	21	23	26
R_o (Ω)	3.3	2.8	2.5	2.2	1.7	3.3	2.5	2.5	2.5	3.3
R_1^o (Ω)	0.69	0.89	0.57	1.1	0.65	1.1	1.4	1.2	1.1	1.1
R_2^1 (Ω)	1.2	0.31	0.71	0.28	0.98	0.80	0.74	0.73	0.66	1.3
V_2^2 (V)	2.4	2.0	1.6	1.6	1.2	2.2	1.8	2.0	2.1	2.1
V_2^1 (V)	3.9	3.9	2.8	3.1	3.0	3.8	4.4	4.1	4.1	4.4

Table 3.

Piecewise Linearized Equivalent Circuit Parameters for the Gate-Cathode Diode Characteristic Curves for the T7S7 Thyristor

Low Current
($\leq$ 160 mA)

Device Number	2	3	4	6	10	11	13	16	18	20
R_o (Ω)	15.5	2.9	23.0	25.0	19.2	32.5	22.0	22.5	19.2	23.8
R_1 (Ω)	9.1	16.7	16.9	16.7	5.7	17.0	8.7	9.0	7.7	13.1
R_2 (Ω)		2.5	2.8	2.6		2.0	2.0	3.0	3.5	4.8
V_1 (V)	1.0	0.80	0.85	1.1	1.0	0.90	1.1	1.1	1.0	0.90
V_2 (V)		1.4	1.5	1.7		1.5	1.6	1.5	1.5	1.5

Only two breakpoints were obtained for Devices 2 and 10.

Pulsed High Current
($\leq$ 12 A)

Device Number	2	3	4	6	10	11	13	16	18	20
R_o (Ω)	2.8	2.8	3.1	3.9	2.8	3.1	3.1	2.6	2.8	3.0
R_1 (Ω)	0.49	0.53	0.69	0.82	0.35	0.52	0.55	0.53	0.42	0.61
R_2 (Ω)	0 85	0.95	0.90	1.1	0.70	0.77	0.67	0.44	0.72	0.75
V_1 (V)	2.2	2.2	2.2	2.4	2.0	2.0	2.0	2.0	2.0	2.2
V_2 (V)	3.8	4.2	4.2	4.8	2.9	3.3	3.6	3.3	3.4	4.0

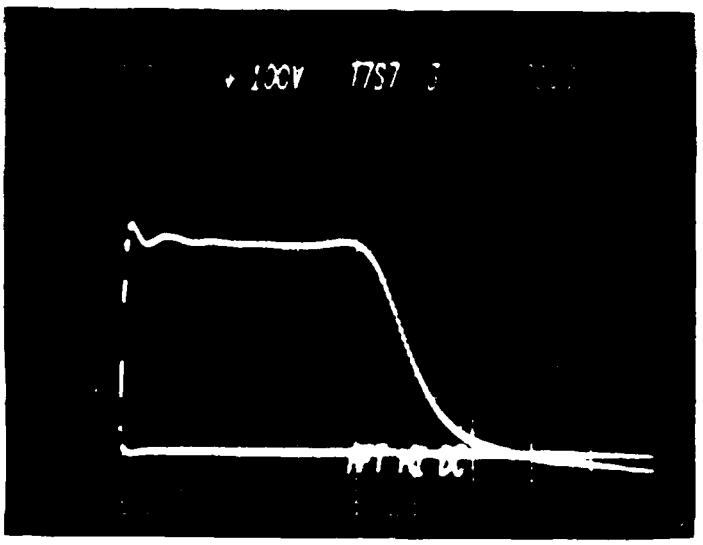
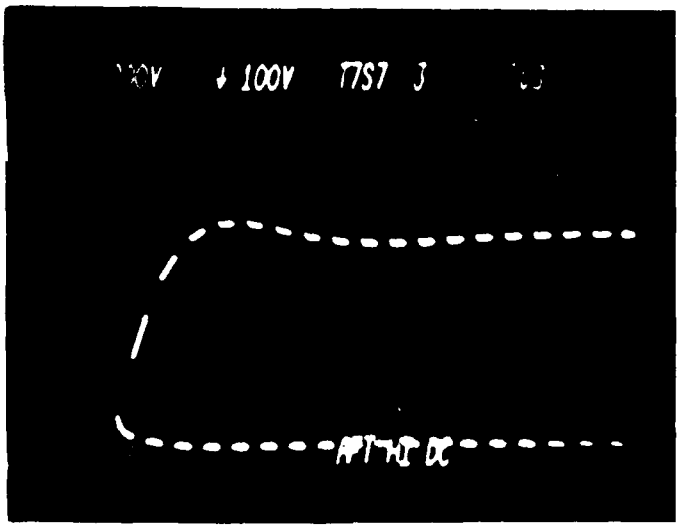
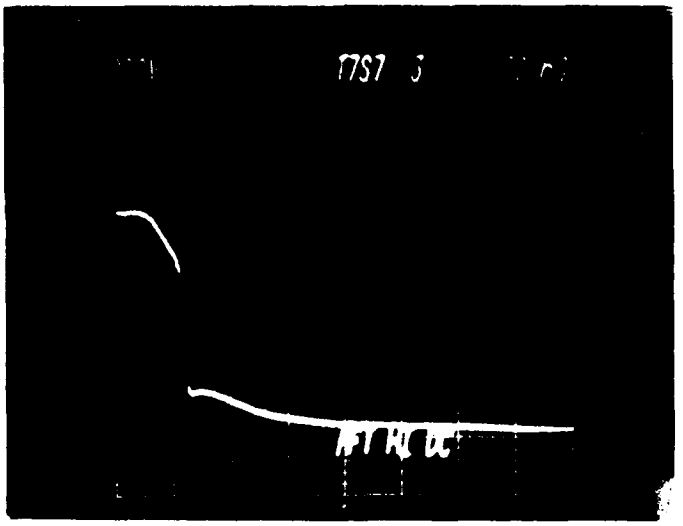


Figure 29. Typical switching waveforms for the 100 μs PFN. The upper curve is the current pulse (250 A per large division); the flat line at zero is the voltage waveform, which falls very rapidly from 800 V. The horizontal scale is 20 μs per large division.



a.



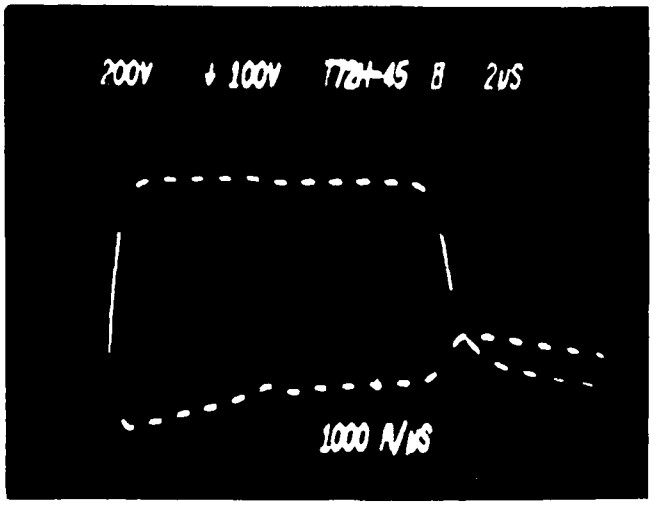
b.

Figure 30. Current rise (a) and voltage fall (b) times on expanded time scales for the switching waveforms for the 100 μs PFN. The upper photograph shows the current rise (upper curve, 250 A per large division) and the voltage fall from 800 V (lower curve). (The dashed appearance of the curves is the result of chopping.) The horizontal time scale is 2 μs per large division. The lower photograph contains the voltage fall waveform; the vertical scale is 200 V per large division and the horizontal scale, 200 ns per large division.

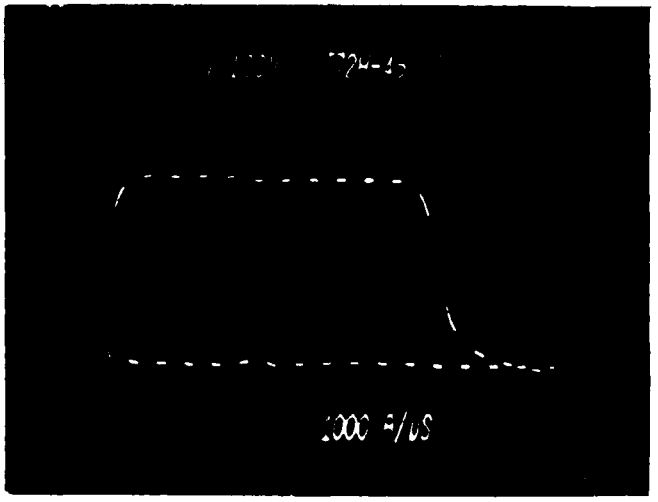
around 100 ns, followed by a very rapid drop to around 160 V in 50 ns, an increase of some 20 V over another 50 ns, and then a slow decay lasting around 1 μs, to the on value of several volts. The forward drop is at its final value after 2 μs. The initial voltage drops are probably associated with the collapse of the electric field, and the rise and slower decay, with the spread of the plasma. After pulse characterization, the gate-cathode diode and blocking characteristics of the devices were compared with the initial measurements to see if any deterioration resulting from pulsed operation had occurred; no changes were observed. It was found during the fast pulse stress that reproducibility of the results was a better criterion for degradation than a slow pulse recharacterization, so that this latter measurement was ultimately discontinued.

2. Single-Shot Stress

Devices T7S7-3, 4, 11, 13 and 20, and T72H-1, 2, 8, 10 and 18 were selected for single-shot stress at high dI/dt. The first stress level was 1000 A/μs (measured to 800 A); four turns were added to the 10 μs PFN inductor to slow the rise time. Figure 31a illustrates the chopped anode current, obtained by measuring the voltage across the load, and anode voltage waveforms for a T72H device. (All single-shot current waveforms were obtained by measuring the load voltage.) The voltage is seen to go negative, to around -200 V; this is an artifact of the measurement, probably the result of ground currents, and was



a.



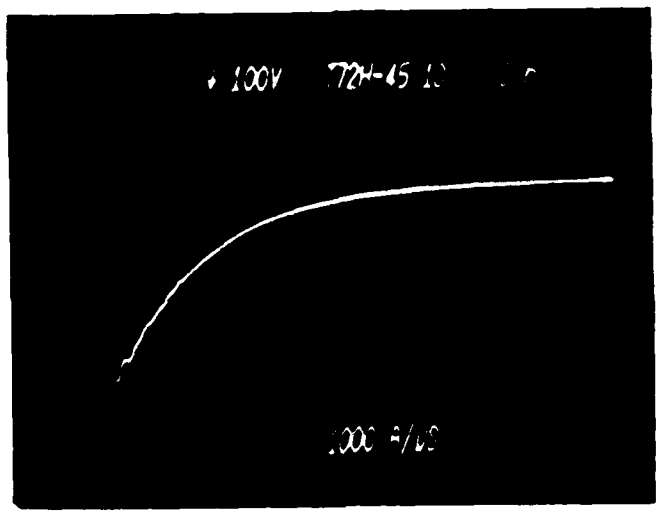
b.

Figure 31. Anode current and voltage waveforms for the T72H at 1000 µs: a) without balun; b) with balun. The upper traces in both photographs are the current waveforms (250 A per large division); the lower traces are the voltage waveforms, falling from 800 V. The horizontal scale in both photographs is 2 µs per large division.

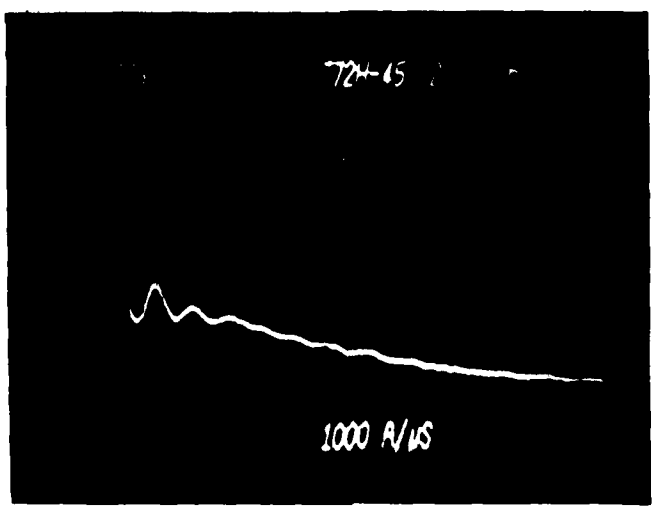
eliminated by wrapping the voltage probe lead around a balun coil (figure 31b) six times. The waveforms in figure 31b are typical for all the T72H thyristors stressed; peak current was around 900 A. The leading edges of the waveforms are shown on expanded time scales in figure 32. dI/dt for the T72H devices was 1000 A/μs (figure 32a), except for device T72H-8, for which dI/dt was 1060 A/μs. Voltage fall (figure 32b) is very rapid, dropping from 800 V to 300 V in 50 ns, and decaying to the static forward drop (zero on this scale) in another 400 ns.

Representative current and voltage waveforms for the T7S7 devices at 1000 A/μs are shown in figure 33. The voltage fall is slower here than for the T72H (compare with figure 31b), as can be seen in figure 34b; in 50 ns, the anode voltage drops to 400 V, and has decayed only to 80 V after an additional 400 ns. dI/dt in these measurements (obtained from the leading edge of the current waveform in figure 34a) was only 800 A/μs, except for T7S7-13, for which dI/dt was 850 A/μs.

The dI/dt of the 10 μs PFN was increased to 2000 A/μs by adding a shunt capacitance of 0.3 μF at its output. Overall current and voltage pulse shapes were similar to those in figures 31 (T72H) and 33 (T7S7). The leading edges of the current waveforms on expanded time scales are shown in figure 35a (T72H) and 35b (T7S7). The corresponding values of dI/dt are 2285 A/μs (T72H) and 2000 A/μs (T7S7). The voltage fall for both types was similar, and is illustrated in figure 36. It is to be noted that the voltage fall time for the T72H has increased, the



a.



b.

Figure 32. Leading edges of current (a) and voltage (b) waveforms on expanded time scales for the T72H at 1000 A/µs. The vertical and horizontal scales for the upper photograph are 250 A and 200 ns per large division, respectively; for the lower photograph, 200 V and 50 ns per large division, respectively.

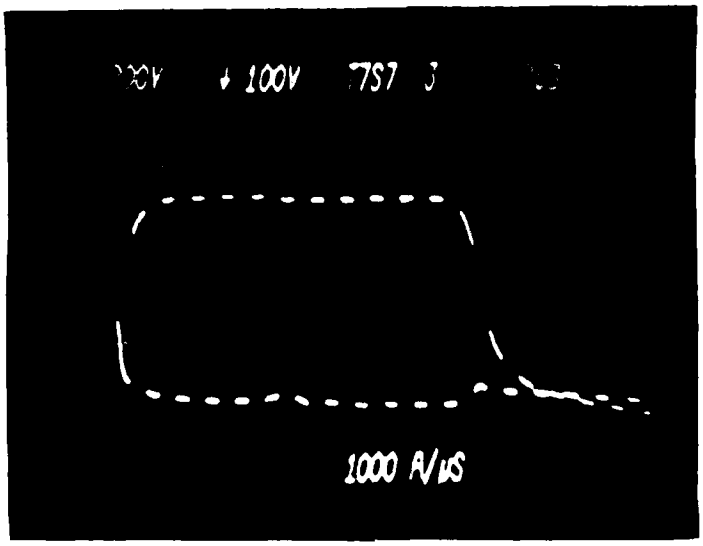
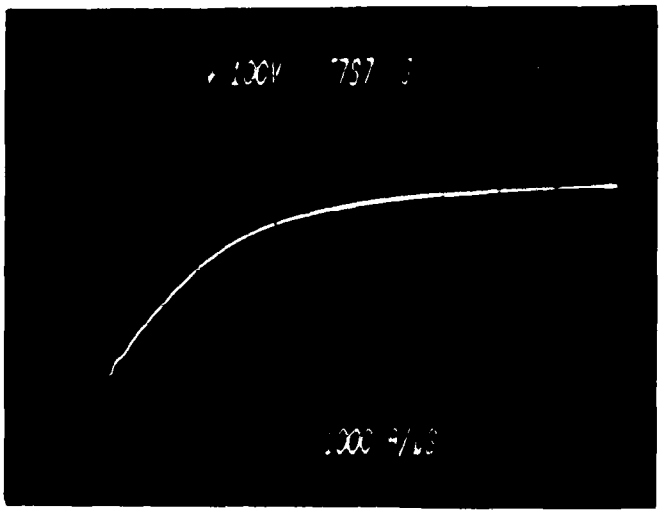
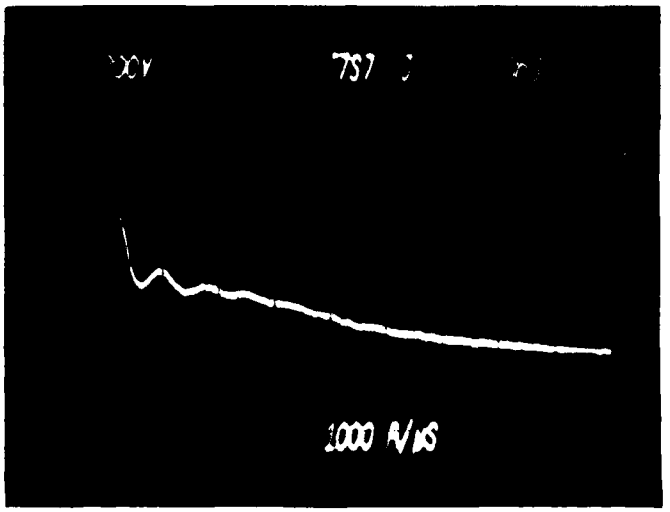


Figure 33. Representative current (upper curve) and voltage (lower curve) waveforms for the T7S7 at 1000 A/µs (nominal). The vertical current scale is 250 A per large division. The horizontal scale for both is 2 µs per large division.

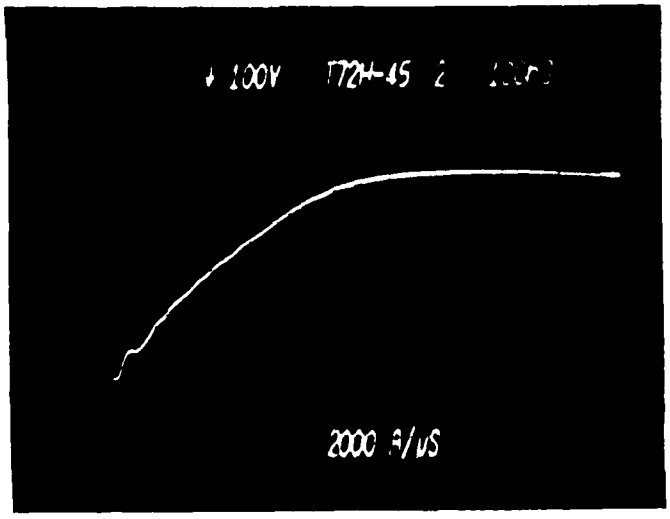


a.

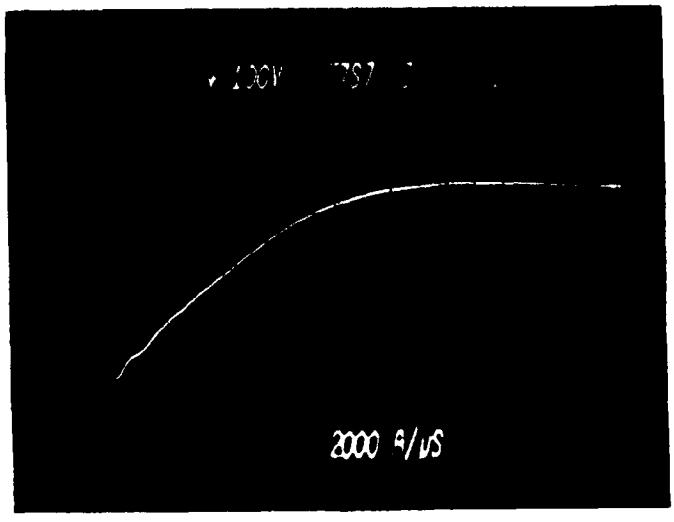


b.

Figure 34. Leading edges of the current (a) and voltage (b) waveforms on expanded time scales for the T7S7 at 1000 A/µs (nominal). The vertical and horizontal scales for the upper photograph are 250 A and 200 ns per large division, respectively; for the lower photograph, 200 V and 50 ns per large division, respectively.



a.



b.

Figure 35. Leading edges of the current waveform on expanded time scales for the T72H (a) and the T7S7 (b) at 2000 A/µs (nominal). The vertical and horizontal scales in both photographs are 250 A and 100 ns per large division, respectively.

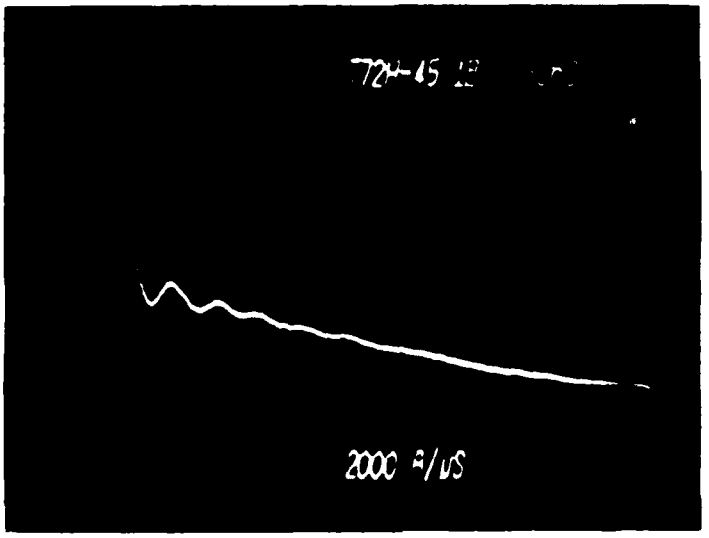


Figure 36. Typical voltage fall on an expanded time scale for the T72H and the T7S7 at 2000 A/µs (nominal). The vertical scale is 200 V per large division, and the horizontal scale, 50 ns per large division.

voltage after 50 ns being around 400 V and, after another 400 ns, around 30 V. The fall time for the T7S7 has decreased somewhat, the voltage decay being faster.

Thirty turns of the 10 μs PFN inductor were shorted to obtain a dI/dt of 5000 A/μs. There was some distortion in the anode current pulse, as shown in figure 37, which is typical of the anode current in all ten devices. This is probably the result of impedance mismatch. The leading edges of the current waveforms for the two devices are shown on expanded time scales in figure 38. The values of dI/dt (to 800 A) are 3640 A/μs for four of the five T7S7 devices, the fifth, T7S7-17, having a dI/dt of 3480 A/μs. There was considerable variation in the values of measured dI/dt for the T72H devices: 4200 A/μs (T72H-1), 4700 A/μs (T72H-2), 5300 A/μs (T72H-8), 5000 A/μs (T72H-10), and 4000 A/μs (T72H-18). Voltage falls on expanded time scales are shown in figure 39. The shapes of the voltage fall curves have changed from those in figures 32b, 34b and 36, and now appear similar to that of figure 30b, the voltage fall obtained with the 100 μs pulse at a low dI/dt (around 350 A/μs). The total decay times to the static forward values are more-or-less comparable, but the time delay, around 100 ns to 200 ns, occurs only at the lowest and highest dI/dt. It could be argued that the change in the voltage fall waveform is the result of damage occurring at the high dI/dt values used here. Blocking voltage, remeasured after stress, was not affected; however, several of the devices (T7S7-3, T72H-8, T72H-18) used in the single stress measurements

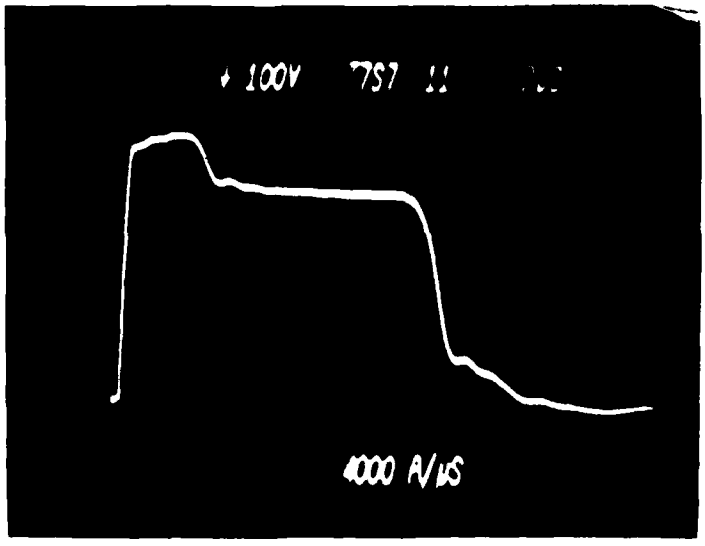
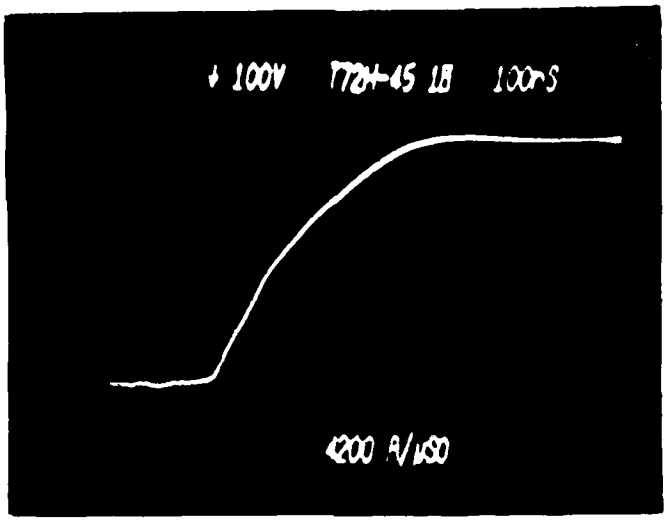
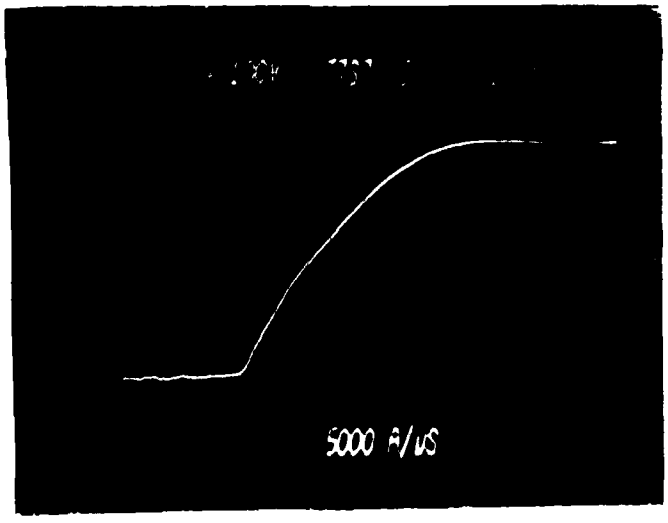


Figure 37. Typical anode current pulse for the T72H and the T7S7 at 5000 A/μs (nominal).

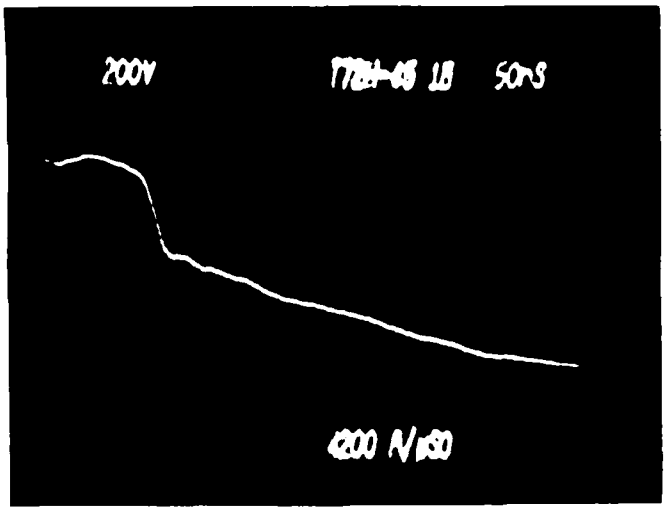


a.

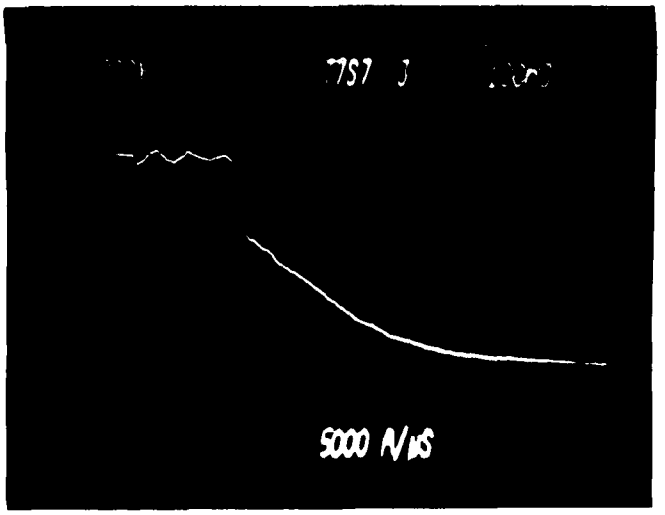


b.

Figure 38. Leading edges of the current waveforms on expanded time scales for the T72H (a) and the T7S7 (b) at 5000 A/us (nominal). The vertical and horizontal scales for both photographs are 250 A and 100 ns per large division, respectively.



a.



b.

Figure 39. Typical voltage falls on expanded time scales for the T72H (a) and the T7S7 (b) at 5000 A/µs (nominal). The vertical and horizontal scales for the upper photograph are 200 V and 50 ns per large division, respectively; and, for the lower photograph, 200 V and 100 ns per large division, respectively.

were used again in the repetitive stress experiments at around 2000 A/μs and the voltage fall results (figures 45b, 47b, and 48) were similar to those observed at 5000 A/μs single-shot, so that the earlier results at 2000 A/μs were not reproduced.

It is also to be noted that, at comparable PFN drives, higher values of dI/dt are obtained for the T72H than for the T7S7. It is possible that the difference is the result of package inductance (the T72H has a somewhat larger diameter package), but is more likely the result of the interdigitation, and increased gate-cathode periphery, in the T72H. (It is also possible that, at these hard gate drives, the main gate is directly triggered.)

The PFN leading edge dI/dt was increased by adding a 10 μF shunt capacitance at its output, but the increased dI/dt of the anode current pulse (device T72H-18) did not change from its previous value, suggesting that the device dI/dt is either self-limited, or limited by parasitic series inductance in the package, fixture, and anode leads. The braided straps were replaced by an 0.4 Ω parallel-plate transmission line, but no change in the anode current dI/dt was observed. Inasmuch as no higher values of anode current dI/dt than 5000 A/μs could be obtained in the single-shot measurements, they were discontinued and repetitive stress was begun.

3. Repetitive Stress

Power requirements for repetitive stress increased signifi-

cantly over those for single-shot discharges. For example, at 500 Hz, the PFN load must dissipate at least 2 KW, and the resistance limiting the steady current (figure 18, R1: 33 Ω) in the gate trigger circuit must dissipate around 2.5 W. R1 was therefore replaced by a parallel array of three 100 Ω, 2 W resistors, and the PFN load was reconfigured. An array of four Stackpole 4 Ω (nominal) carborundum disc resistors was assembled; these discs are 1 inch thick by 4.5 inches in diameter, and have low parasitic series inductance. The array consisted of a paralleled pair of two discs in series, separated from each other and from parallel aluminum end plates, which were bolted together, and which served as mechanical supports and as heat sinks. The entire assembly was force air cooled.

The PFN could no longer be trickle charged because the capacitors could not be charged sufficiently fast between repetitive discharges. Because of the restrictive simultaneous high voltages and high output currents required in a DC charging power supply, it was decided to charge the PFN resonantly. The resonant charging circuit is shown in figure 40. The line voltage is isolated and stepped-up to a peak voltage of 424 V; this voltage is fed to a bridge rectifier whose output is filtered by three paralleled 240 μF, 525 V electrolytic capacitors. The PFN is command charged through the inductor by a control thyristor. Originally, a diode was used instead of the SCR, but recharging of the PFN began before the test thyristor had fully turned off, so that it latched on and was destroyed.

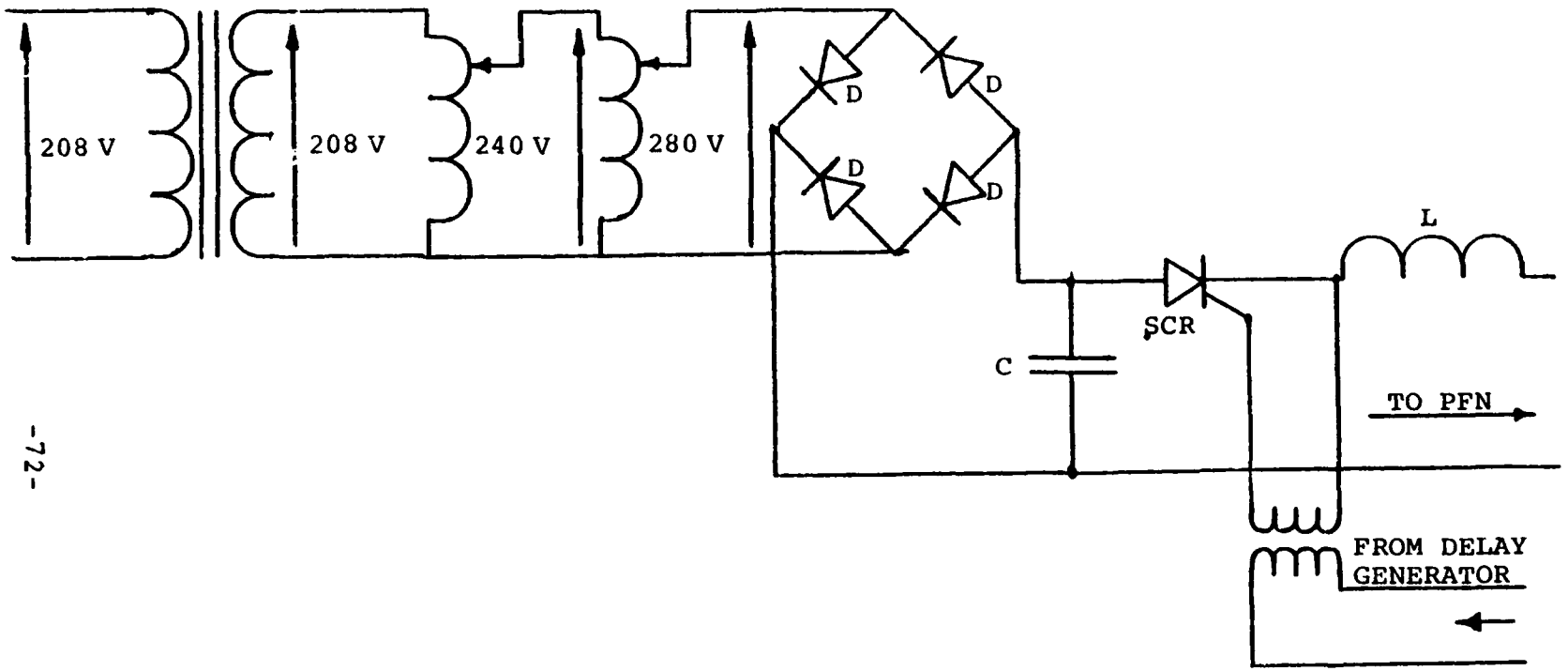


Figure 40. Resonant charging circuit for repetitive discharge of the 10 μs PFN. D: SK3500; SCR: SK6632; C: 720 μF; L: 19.8 mH.

The diode was replaced by the thyristor to introduce a charging delay. The command trigger pulse is derived from the test thyristor trigger pulse, and delayed by 250 μs, so that the charging cycle begins some 240 μs after the PFN has discharged. The delayed pulse is isolated from the charging circuit by a pulse transformer.

Several measurements were made (on T7S7-2 and T72H-21) before the diode was replaced. Load mismatch (an increase in the load resistance caused by heating) increased the width of the anode current pulse; the increased pulse length, and undelayed charging, resulted in destructive latching in the two devices. Neither device blocked in either the forward or reverse direction after latching. The gate-cathode diode showed no deterioration in the failed devices; this measurement is clearly not as sensitive to degradation as anticipated. (It is also worthwhile to note that the gate-cathode diode (T7S7-2) could be pulsed repetitively for one hour at 500 Hz, with the anode open, with no change in characteristics.) At this time, the diode was replaced by the command switch.

Devices T7S7-3, T7S7-6, T7S7-16 and T7S7-18, and T72H-1, 2, 8, 10 and 18, were all stressed at 500 Hz. Devices T7S7-18, T72H-1 and T72H-2 were destroyed because of shorts in the load mount before any data were obtained; T7S7-16 and T72H-8 were also eventually destroyed because of load mount shorts. The load was finally rearranged into a transmission line configuration (figure 41). To assure that enough devices were stressed to

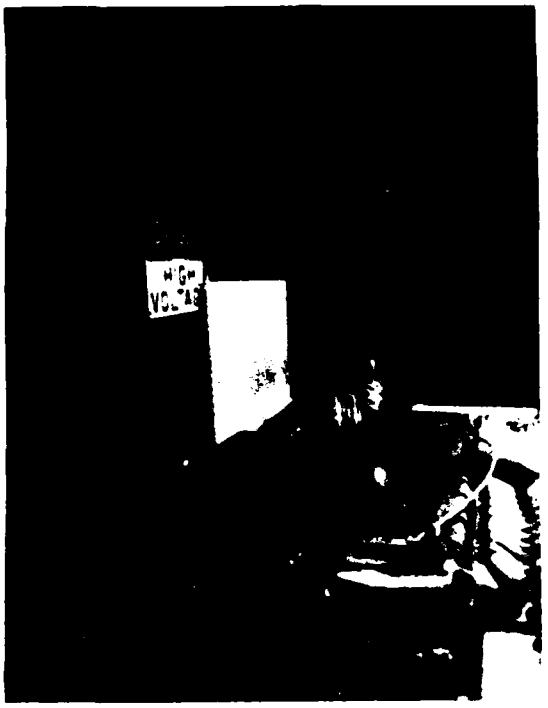


Figure 41. Photograph of the load and mounting structure.

provide a sufficient sample size, thyristors which had been used in the single-shot stresses were reused in the repetitive stress measurements to replace new devices which had been lost through non-stress related events. The pulse shape of the gate trigger for the test thyristors changed somewhat from its shape in the single-shot measurements, but its peak current, leading edge rise time, and steady value remained essentially the same.

Device T7S7-6 was stressed at 500 Hz at a dI/dt (to 800 A) of around 2500 A/μs. (dI/dt changed somewhat during the measurement because of load heating.) The anode voltage charging waveform is shown in figure 42; the anode voltage increases as cosine t to its peak value (around 700 V in the 500 Hz measurements because of charging power supply limitations), switches rapidly to zero, and begins to increase again. A single anode current pulse is shown in figure 43. The pulse distortion is caused by load mismatch and load inductance; this pulse was obtained by measuring the voltage across the load. The device was stressed a total of ten hours, with interruptions after one hour, two hours, and five hours of stress for blocking voltage and gate-cathode diode recharacterizations; final recharacterization was performed at ten hours, after end of stress. (This recharacterization protocol was used in all the 500 Hz repetitive stress measurements.) No changes in either characteristic were observed.

Device T7S7-16 was stressed for five hours at a dI/dt of around 1800 A/μs. The PFN was switched from 700 V; the peak anode current was around 1000 A. No changes in blocking voltage

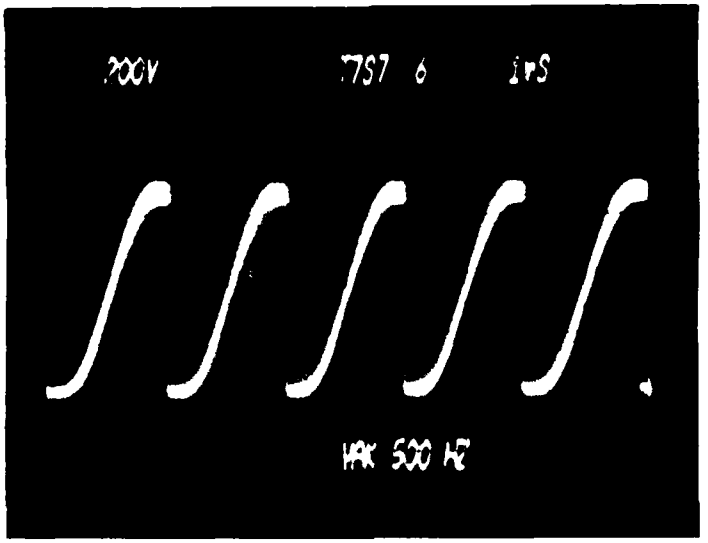


Figure 42. Anode voltage charging waveform (T7S7-6). The vertical scale is 200 V per large division and, the horizontal scale, 1 ms per large division.

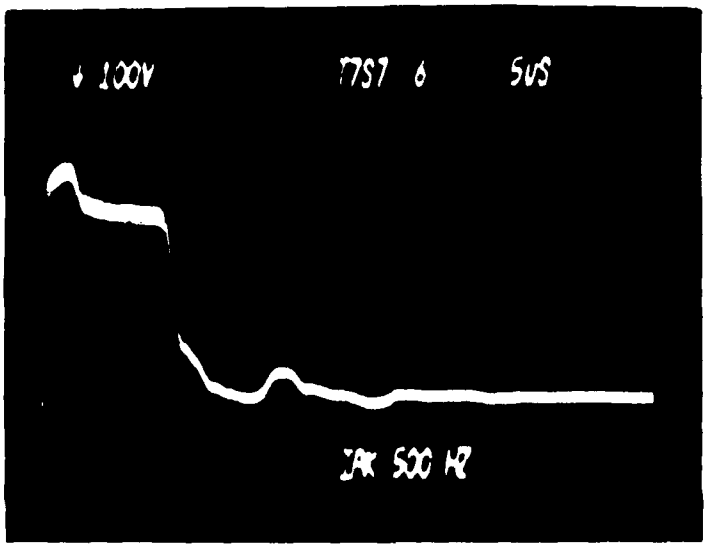


Figure 43. Single anode current pulse at 2500 A/μs and 500 Hz (T7S7-6). The vertical scale is 250 A per large division and, the horizontal scale, 5 μs per large division.

or gate-cathode diode behavior were observed in any of the recharacterizations.

Device T7S7-3 was stressed for ten hours at a dI/dt (to 800 A) of 2000 A/μs. No changes in characteristics were seen at any time. Figure 44 shows a single anode current pulse, and figures 45a and 45b, the leading edges, on an expanded time scale, of the current and voltage fall pulses. (The anode currents in this and all the following measurements were obtained with the Pearson 411 current transformer.) The voltage fall here is similar to that of the 5000 A/μs T7S7 single-shot stress (figure 39), and may be the result of damage during that stress.

One device, T7S7-10, failed (would not block) after 45 minutes of stress at 2600 A/μs, but this was probably the result of a load resistance change and subsequent device latch-on. A second device, T72H-10, failed during reverse blocking recharacterization after two hours of stress at 2000 A/μs. No leakage current was observed until the reverse anode voltage was at 50 V, when the thyristor failed catastrophically, no longer blocking in either direction. The device did not fail during dI/dt stress; otherwise it would not have blocked at all, or would have been leaky, but it may have been sufficiently damaged during that stress so that the additional stress during blocking voltage characterization would cause it to fail completely.

The remaining two T72H devices, T72H-8 and T72H-18, were stressed at 2000 A/μs and 2600 A/μs, respectively, for ten hours in increments of one, one, three and five hours. No changes in

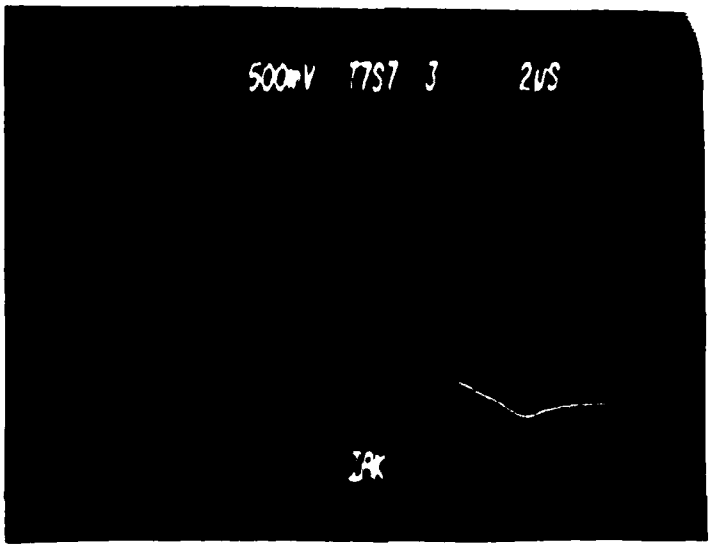
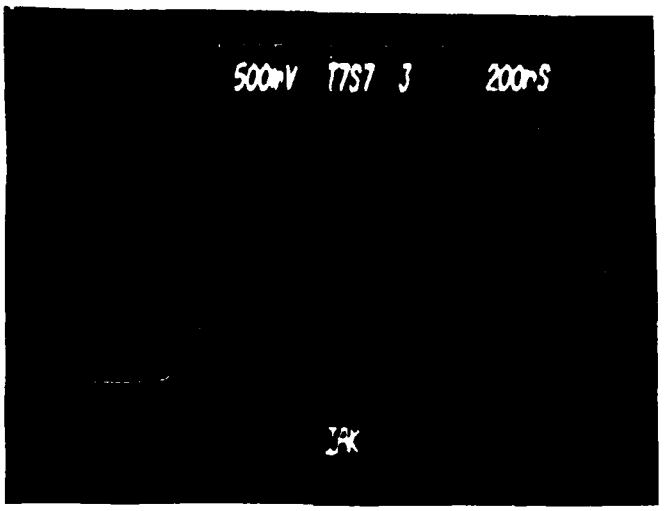
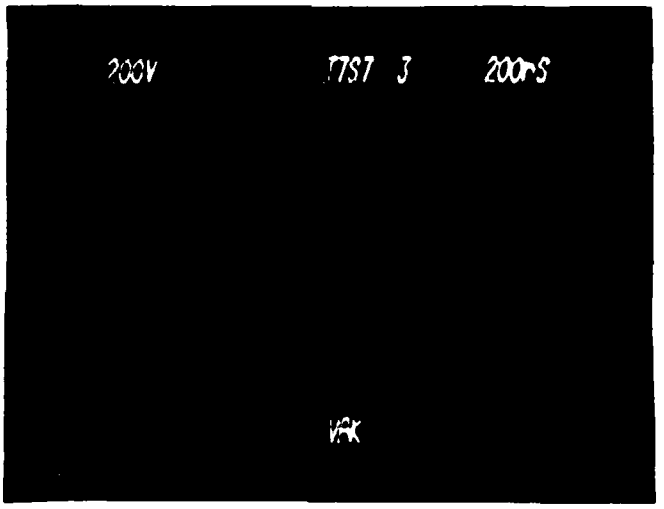


Figure 44. Single anode current pulse at 2000 A/μs and 500 Hz (T7S7-3). The vertical scale is 316 A per large division and, the horizontal scale, 2 μs per large division.



a.



b.

Figure 45. Leading edges of the (a) current and (b) voltage single pulse waveforms on expanded time scales for T7S7-3 at 2000 A/μs and 500 Hz. The vertical and horizontal scales for the upper photograph are 316 A and 200 ns per large division, respectively; for the lower photograph, 200 V and 200 ns per large division, respectively.

blocking voltage or gate-diode characteristics were observed. The single pulse anode current waveform and the current rise and voltage fall, on expanded time scales, for T72H-8, are illustrated in figures 46 and 47, respectively. The PFN is switched from 700 V and the peak anode current is 875 A. The voltage fall characteristics under these conditions are similar to those of the 5000 A/μs voltage fall (figure 39).

After ten hours of stress at 500 Hz, T72H-18 was stressed for an additional 24 hours at 1 KHz. The PFN could be charged only to 500 V, and dI/dt was reduced to 1600 A/μs, because the charging power supply was limited at this frequency. The single pulse voltage fall is shown in figure 48; its behavior is similar to that of the voltage fall in the 5000 A/μs single-pulse stress. The dip at the end of the trace is probably the result of load mismatch and device fixture inductance. The blocking voltage and gate-cathode diode characteristics were remeasured after twenty-four hours of stress and found unchanged from their original values. Stress had been reapplied for another forty-five minutes when the load mount shorted and the device was destroyed, failing to block in either direction (but the gate-cathode diode characteristics were unaffected).

4. Failure Analysis

The failure analysis performed here did not indicate any obvious failure mode for the failed (non-blocking) T72H or T7S7

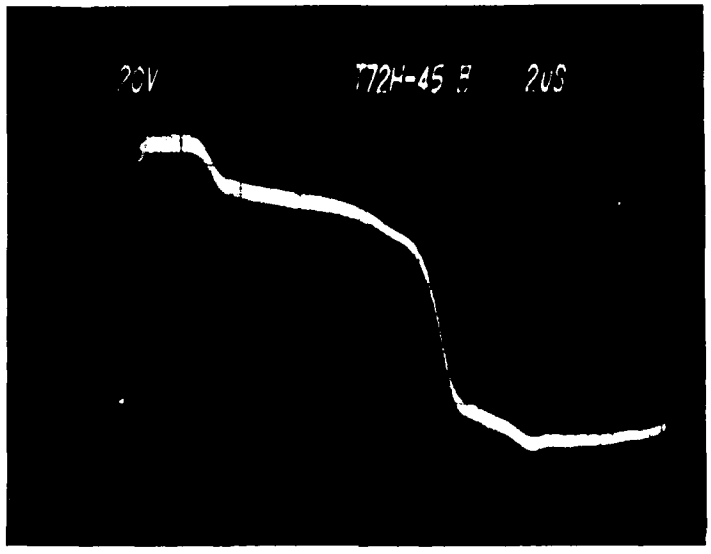
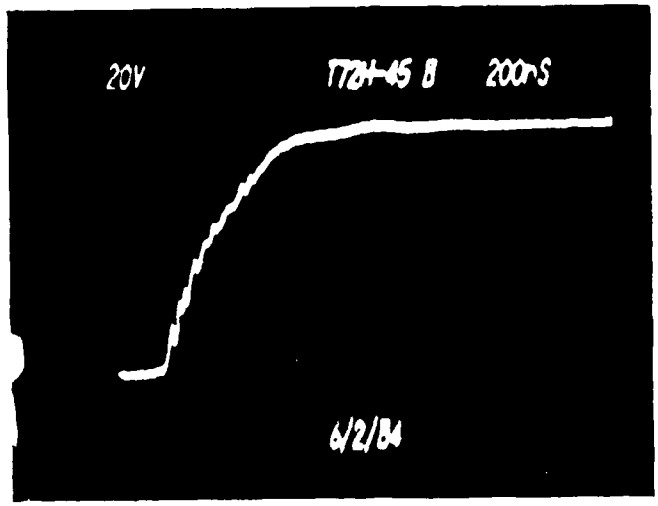
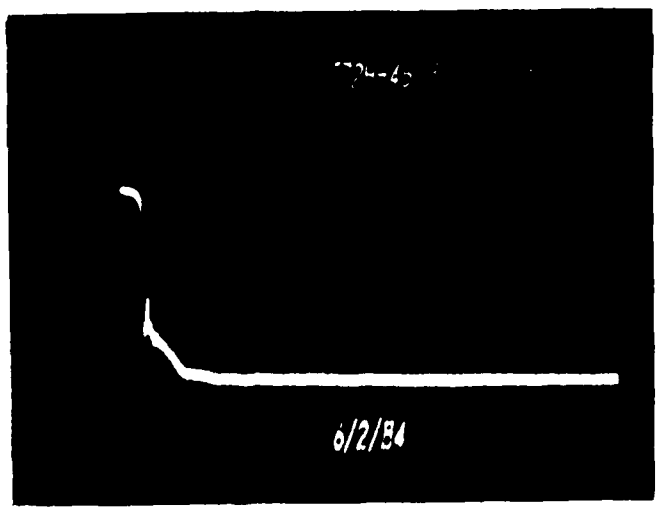


Figure 46. Single anode current pulse at 2000 A/μs and 500 Hz (T72H-8). The vertical and horizontal scales are 200 A and 2 μs per large division, respectively.



a.



b.

Figure 47. Leading edges of the (a) current and (b) voltage single pulse waveforms on expanded time scales for T72H-8 at 2000 A/μs and 500 Hz. The vertical and horizontal scales for the upper photograph are 200 A and 200 ns per large division, respectively; for the lower photograph, 200 V and 500 ns per large division, respectively.

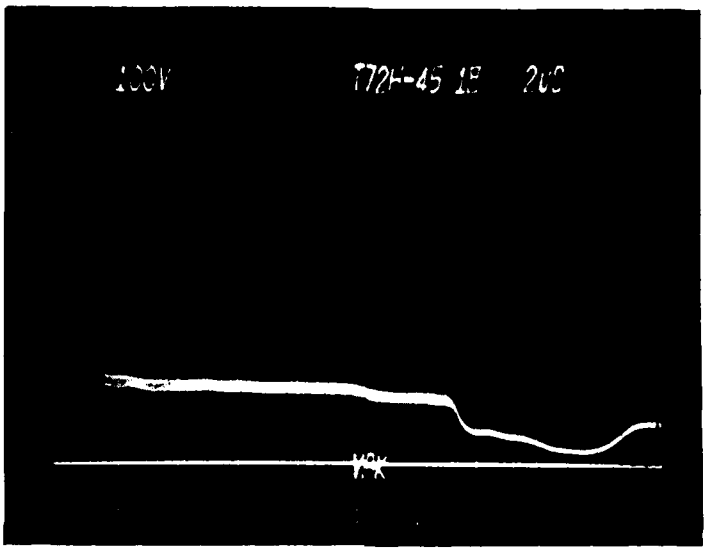


Figure 48. Single pulse voltage fall on an expanded time scale for T72H-18 at 1600 A/μs and 1 Khz. The vertical scale is 100 V per large division, and the horizontal scale, 2 μs per large division.

devices when the packages were opened. No physical damage was seen.

AD-A154 109 FAST TRANSIENT BEHAVIOR OF THYRISTOR SWITCHES(U) TEXAS 2/2
TECH UNIV LUBBOCK DEPT OF ELECTRICAL ENGINEERING
W M PROTNOY FEB 85 RADC-TR-85-20 F30602-82-C-0029

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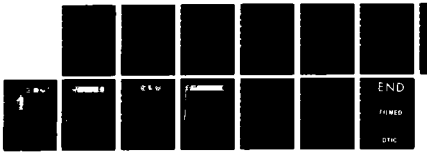
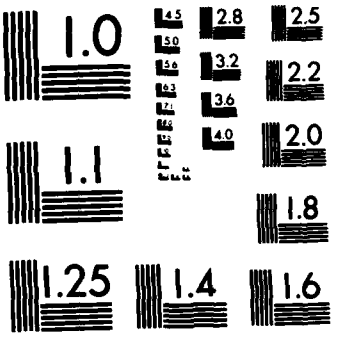




VI. CONCLUSIONS

It is clear from these results that specified values of single-shot dI/dt are much too conservative, as are repetitive values, at least with respect to tens of hours of operation. If blocking voltage is considered to be the most sensitive criterion for damage, no damage occurred to any device except one (T72H-10), and the results there were ambiguous. There may be a more subtle damage mode, in voltage fall characteristics, but there has been no previous suggestion that such changes are significant. In any case, operation without significant failure at 1000 A and 2000 A/μs even for only ten hours is not an insignificant result, inasmuch as it represents 1.8×10^7 switching events at 500 Hz. The conclusions that single-shot dI/dt is too conservatively specified is supported by the analysis, albeit crude, in Appendix 1. Also, dI/dt can be significantly increased by increasing the interdigitation. The T72H thyristor has a gate-cathode periphery of around 9 cm; the peak repetitive current switched in this work per inch of periphery is roughly 100 A per cm. Simply increasing the periphery, without any other changes in the device, will increase the possible peak current, and, in the same rise time, the possible repetitive dI/dt.

The results of this work have suggested additional measurements, preparations for which have already been begun. A new low inductance fast pulse PFN has been designed and is being built,

and a more compact, higher power, low inductance load is under construction. These will be used to study gate drive effects, particularly the result of varying peak current and pulse width.

APPENDIX 1

Calculation of Maximum Single Pulse dI/dt

Calculation of Maximum Single Pulse dI/dt

It is possible to obtain a rough estimate of the maximum single-pulse dI/dt by assuming that power is dissipated only during the turn-on transient, and that heating is adiabatic. (Analysis of repetitive operation involves thermal conduction and is more complex.) The instantaneous power dissipated in the thyrister during turn-on is

$$p(t) = V(t)I(t),$$

where V(t) is the instantaneous anode-cathode voltage, and I(t) is the instantaneous anode current. The total energy delivered to the thyristor at the end of the current rise is

$$U(t_o) = \int_0^{t_o} V(t)I(t)dt,$$

where t_o is the rise time of the current pulse. This energy is dissipated in the total conducting volume which exists at time t_o, that is, $u_p \ell w t_o$, where u_p is the plasma spreading velocity, ℓ is the gate-cathode periphery, and w is the n-base width. The total mass contained in this volume is

$$m(t_o) = \rho u_p \ell w t_o,$$

where ρ is the density of silicon (assumed independent of temperature). If heating is adiabatic,

$$u(t_o) = m(t_o)c_p(T_m - T_a) = \rho u_p \ell w c_p t_o (T_m - T_a),$$

where c_p is the specific heat capacity at constant volume for silicon (assumed independent of temperature), T_a is the ambient temperature, and T_m is the maximum temperature which can be sustained without damaging the thyristor; in this case, $U(t_o)$ is the maximum energy which may be delivered during the current rise time.

If it is assumed that the single-shot current rise and voltage fall waveforms of figures 38a and 39a are representative of those at all high dI/dt for, say, the T72H, then a general approximation may be obtained for the current and voltage behavior. The very approximate expressions are

$$I(t) = I_m(t/t_o)^{1/2} \qquad 0 \leq t_o$$

$$V(t) = V_m \qquad 0 \leq t \leq t_o/4$$

$$V(t) = V_m/2 - \frac{V_m/2 - V_m/8}{3/4\ t_o}(t_o - t/4)$$

$$= V_m/2\ (1.25 - t/t_o) \qquad t_o/4 \leq t \leq t_o$$

where I_m is the peak value of the anode current and V_m is the anode blocking voltage.

The total energy delivered to the conducting volume is

$$U(t_o) = V_m I_m/2 \int_0^{to} (t/t_o)^{1/2}(1.25 - t/t_o)dt$$

$$= V_m I_m t_o/2 \int_0^1 x^{1/2}(1.25 - x)dx$$

$$= 0.217\ V_m I_m t_o.$$

Then

$$.217\ V_m t_o = u_p \ell w c_p t_o (T_m - T_a),$$

or the maximum allowable peak current is

$$I_m = 4.62\ \frac{u_p \ell w c_p}{V_m}\ (T_m - T_a).$$

Note that, in this approximation, the maximum current (that is, the maximum dissipated power), depends only on the parameters of the material, and not on the current rise time. As the current rise time increases, the total conducting volume increases in the same proportion, so that the ratio of the dissipated energy to the total conducting volume remains constant, independent of rise time. In other words, at high dI/dt, less total energy is delivered. This is a general result which does not depend on the approximations for the time dependence of the anode current and voltage, which affect only the numerical constant.

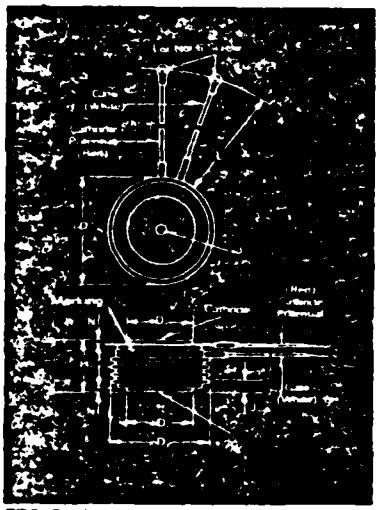
This conclusion is, of course, based on very crude reasoning, and it is to be expected that there is some high value of dI/dt (and current) at which burn-out will, in fact, occur. It is, however, suggestive, and supports the argument (based on experimental results) that dI/dt values are conservatively specified, at least for the voltage fall times observed here.

APPENDIX 2

Specifications for the T72H-45

Fast Switching SCR T72H_45

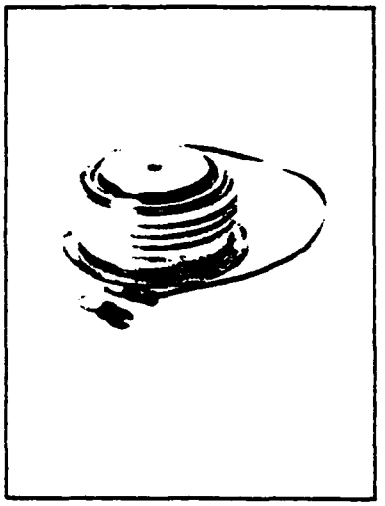
450A Avg (700 RMS) Up to 1400 Volts 25-50 µs



T72 Outline

Symbol	Inches		Millimeters	
	Min.	Max.	Min.	Max.
øD	2.250	2.290	57.15	58.17
øD,	1.333	1.343	33.86	34.11
øD,	2.030	2.090	51.56	53.09
H	1.020	1.060	25.91	26.92
øJ	.135	.145	3.43	3.68
J,	.075	.090	1.91	2.29
L	7.75	8.50	196.85	215.90
N	.040		1.02	

Creep Distance—1.00 in. min. (25.40 mm).
Strike Distance—.69 in. min. (17.53 mm).
(In accordance with NEMA standards.)
Finish—Nickel Plate
Approx. Weight—8 oz. (227 g).
1. Dimension "H" is a clamped dimension.



Features:
- Interdigitated, dI/dt namic Gate structure
- Hard Commutation Turn-Off
- Forward Blocking Capabilities to 1200 Volts
- Low Switching Losses at High Frequency
- Soft Commutation (Feedback Diode) Testing Available
- High dI/dt with softgate control

Applications:
- Induction Heating
- Transportation
- Inverters
- Crowbars
- Cycloconverters

Ordering Information

Type	Voltage		Current		Turn-off		Gate current		Leads	
Code	V_{DRM} and V_{RRM} (V)	Code	$I_{T(av)}$ (A)	Code	tq µsec	Code	I_{GT} (ma)	Code	Case	Code
T72H	100	01	450	45	25	5	150	4	T72	DN
	200	02			30	5				
	300	03			40	4				
	400	04			50	3				
	500	05								
	600	06								
	700	07								
	800	08								
	900	09								
	1000	10								
	1100	11								
	1200	12								
	1400	14								

Example

Obtain optimum device performance for your application by selecting proper Order Code.

Type T72H rated at 450 A average with V_{DRM} = 1000V I_{GT} = 150 ma, tq = 40 µsec max. and leads—order as

Type			Voltage		Current		Turn Off	Gate Current	Leads	
T	7	2	H	1	0	4	5	4	4	D	N

450A Avg (700 RMS) Up to 1400 Volts 25-50 µs

Fast Switching SCR T72H_45

Voltage ①

Blocking State Maximums (T_J = 125°C)	Symbol												
Repetitive peak forward blocking voltage, V	V_{DRM}	100	200	300	400	500	600	700	800	900	1000	1100	1200	1400
Repetitive peak reverse voltage, V	V_{RRM}	100	200	300	400	500	600	700	800	900	1000	1100	1200	1400
Non-repetitive transient peak reverse voltage, t ≤ 5.0 msec, V	V_{RSM}	200	300	400	500	600	700	800	900	1000	1100	1200	1300	1500
Forward leakage current, mA peak	I_{DRM}	← 35 →												
Reverse leakage current, mA peak	I_{RRM}	← 35 →												

Current

Conducting State Maximums (T_J = 125°C)	Symbol	T72H_45
RMS forward current, A	$I_{T(rms)}$	700
Ave. forward current, A	$I_{T(av)}$	450
One-half cycle surge current②, A	I_{TSM}	7500
3 cycle surge current③, A	I_{TSM}	5300
10 cycle surge current③, A	I_{TSM}	4650
I^2t for fusing (for times ≥ 8.3 ms) A^2 sec.	I^2t	234,000
Forward voltage drop at I_{TM} = 1500A and T_J = 25°C, V	V_{TM}	2.30
Min. repetitive di/dt ⓒⓒ① A/µsec	di/dt	600

Switching

(T_J = 25°C)	Symbol	
Max. turn-off time, I_T = 1000A, T_J = 125°C, t_p = 100 µsec, dir R/dt = 50 A/µsec., reapplied dv/dt = 200V/µsec. linear to 0.8 V_{DRM}, µsec ①②	tq	25 to 50
Typ. delay time, I_{TM} = 1000A T_D = .8 V_{DRM} ⓒ, µsec	td	5
Min. critical dv/dt exponential to .8 V_{DRM}, T_J = 125°C, V/µsec ⑦①	dv/dt	300
Min. di/dt, non-repetitive, A/µsec ⓒ⑥④	di/dt	1200

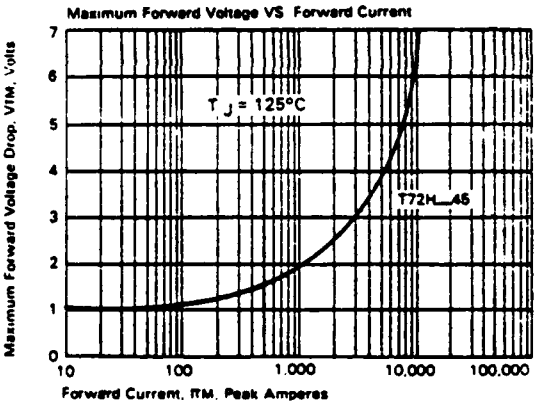
Gate

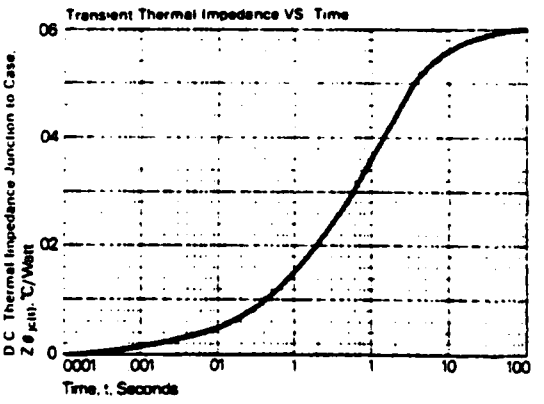
Maximum Parameters (T_J = 25°C)	Symbol	
Gate current to trigger at V_D = 12V, mA	I_{GT}	150
Gate voltage to trigger at V_D = 12V, V	V_{GT}	3
Non-triggering gate voltage, T_J = 125°C, and rated V_{DRM}, V	V_{GDM}	25
Peak forward gate current, A	I_{GTM}	4
Peak reverse gate voltage, V	V_{GRM}	5
Peak gate power, Watts	P_{GM}	16
Average gate power, Watts	$P_{G(av)}$	3

Thermal and Mechanical

	Symbol	
Min., Max. oper. junction temp., °C	T_J	−40 to +125
Min., Max. storage temp., °C	T_{stg}	−40 to +150
Max. mounting force, lb. ... ①		2000 to 2400
Thermal resistance ⑤, double-side cooling, junction to case, °C/Watt	$R_{\theta JC}$	.06
Case to sink, lubricated, °C/Watt	$R_{\theta CS}$	.02

ⓒ Consult recommended mounting procedures.
② Applies for zero or negative gate bias
① Per JEDEC RS-397, 5.2.2.1.
ⓒ With recommended gate drive.
④ Higher dv/dt ratings available, consult factory
⑤ Per JEDEC standard RS-397, 5.2.2.6
⑥ For operation with antiparallel diode, consult factory

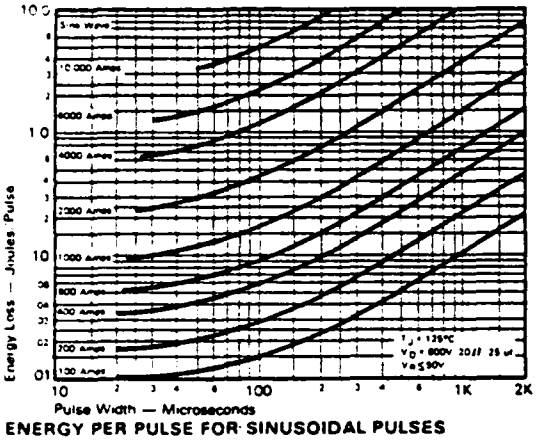




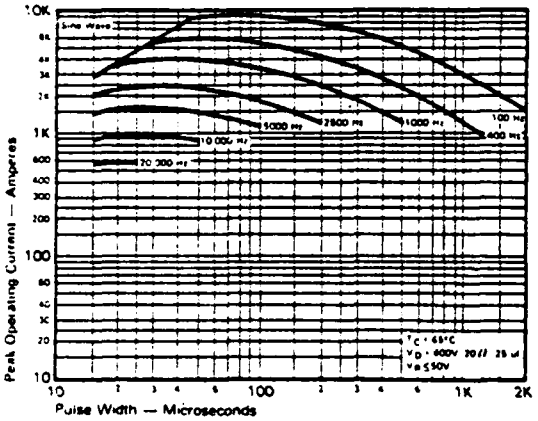
Fast Switching SCR
172HL45

450A Avg (700 RMS)
Up to 1400 Volts
25-50 μsec

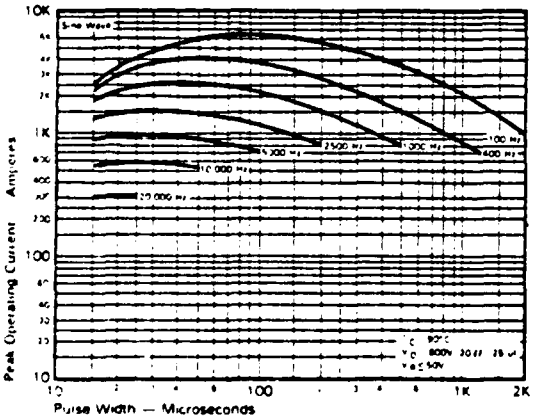
Sinusoidal Current Data



ENERGY PER PULSE FOR SINUSOIDAL PULSES

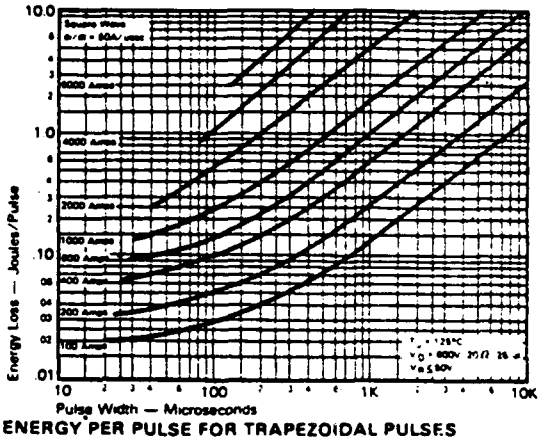


MAXIMUM ALLOWABLE PEAK ON-STATE CURRENT
vs. PULSE WIDTH (T_C = 65°C)

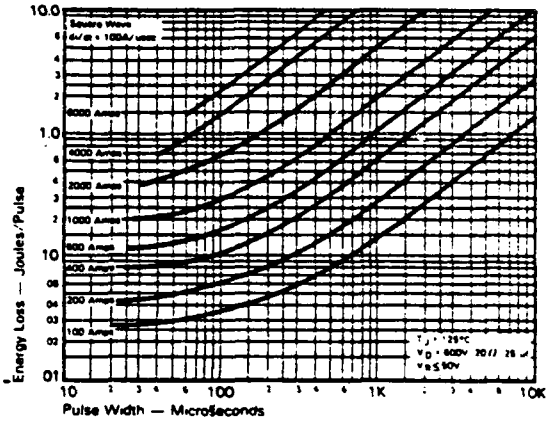


MAXIMUM ALLOWABLE PEAK ON-STATE CURRENT
vs PULSE WIDTH (T_C = 90°C)

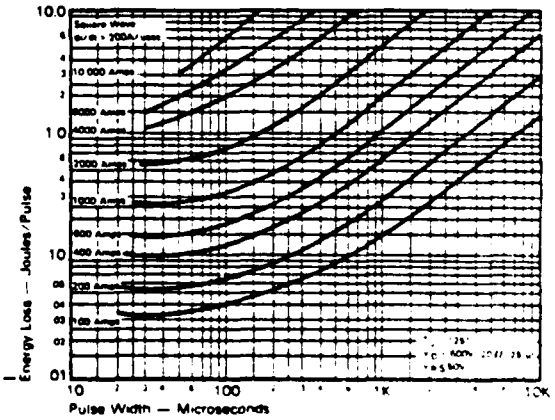
Trapezoidal Wave Current Data



ENERGY PER PULSE FOR TRAPEZOIDAL PULSES
(di/dt = 50A/usec)



ENERGY PER PULSE FOR TRAPEZOIDAL PULSES
(di/dt = 100A/usec)



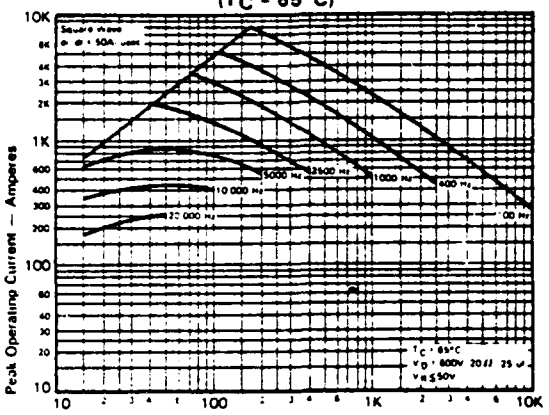
ENERGY PER PULSE FOR TRAPEZOIDAL PULSES
(di/dt = 200A/usec)

FAST SWITCHING THYRISTORS

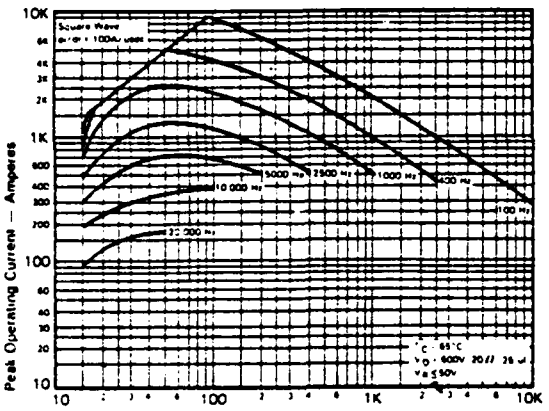
450A Avg (700 RMS) Up to 1400 Volts 25-50 µs Fast Switching SCR T72H..45

FAST SWITCHING THYRISTORS

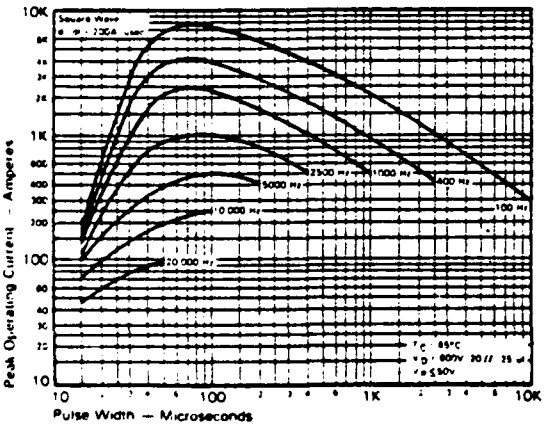
Trapezoidal Wave Current Data
(T_C = 65°C)



MAXIMUM ALLOWABLE PEAK ON-STATE CURRENT
vs. PULSE WIDTH (di/dt = 50A/usec)

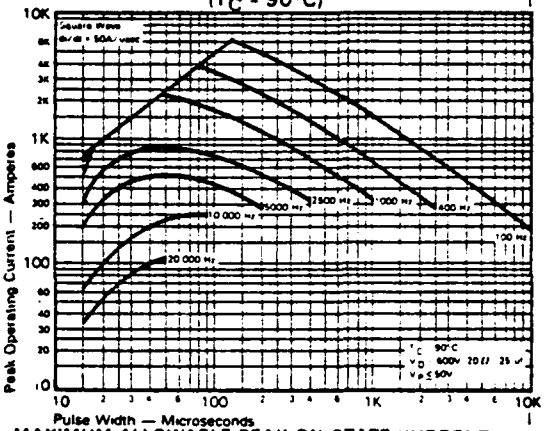


MAXIMUM ALLOWABLE PEAK ON-STATE CURRENT
vs. PULSE WIDTH (di/dt = 100A/usec)

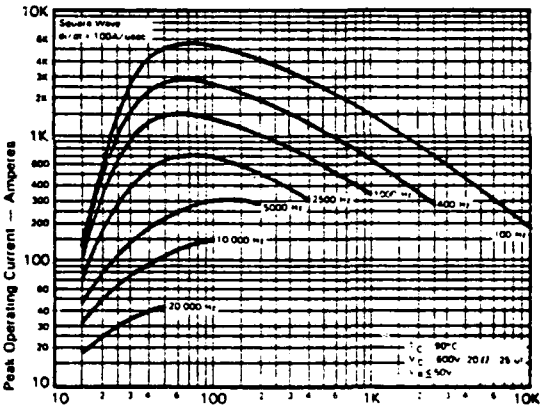


MAXIMUM ALLOWABLE PEAK ON-STATE CURRENT
vs. PULSE WIDTH (di/dt = 200A/usec)

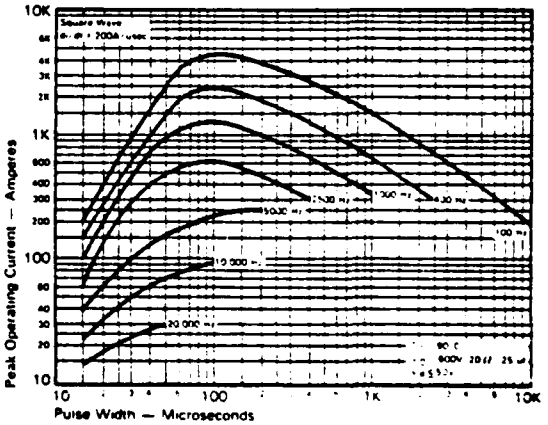
Trapezoidal Wave Current Data
(T_C = 90°C)



MAXIMUM ALLOWABLE PEAK ON-STATE CURRENT
vs. PULSE WIDTH (di/dt = 50A/usec)



MAXIMUM ALLOWABLE PEAK ON-STATE CURRENT
vs. PULSE WIDTH (di/dt = 100A/usec)



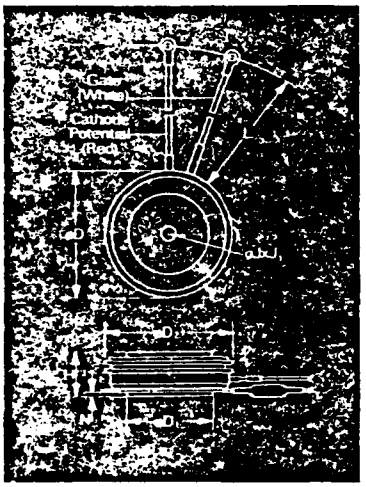
MAXIMUM ALLOWABLE PEAK ON-STATE CURRENT
vs. PULSE WIDTH (di/dt = 200A/usec)

APPENDIX 3

Specifications for the T7S7-60

Fast Switching SCR T7S7_60

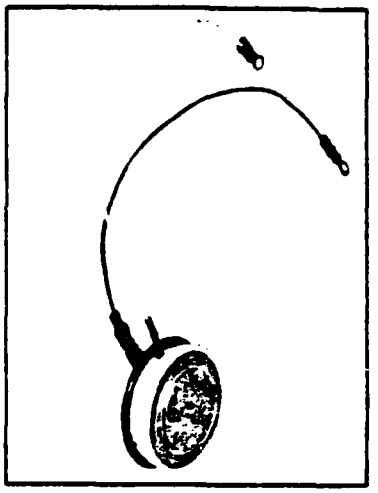
600A Avg. (943 RMS) Up to 1400 Volts 15-60 μs



T7S Outline

Symbol	Inches		Millimeters	
	Min	Max	Min	Max
øD	1.850	1.900	45.72	48.26
øD1	1.140	1.180	28.96	29.97
øD2	1.760	1.850	44.70	46.99
H	.545	.605	13.84	15.37
øJ	.135	.145	3.43	3.68
J1	.072	.082	1.83	2.08
L	7.75	8.50	196.85	215.90
N	.025		64	

Creep Distance—.41 in. min. (10.41 mm).
Strike Distance—.35 in. min. (8.89 mm).
Finish-Nickel Plate
Approx. Weight—4 oz. (113 g.)
1. Dimension "H" is a clamped dimension



Features:
- Center fired di/namic gate
- High di/dt with soft gate control
- High frequency operation
- Sinusoidal waveform operation to 20KHz
- Rectangular waveform operation to 20KHz
- Low dynamic forward voltage drop
- Low switching losses at high frequency
- Lifetime Guarantee

Applications:
- Inverters
  - UPS
  - Induction heating
  - AC motor drives
- Cycloconverters
- Choppers
- Crowbars

Ordering Information

Type	Voltage		Current		Turn-off		Gate Current		Leads	
Code	V_{DRM} and V_{RRM} (V)	Code	$I_{T(av)}$ (A)	Code	t_q μsec	Code	I_{GT} (ma)	Code	Case	Code
T7S7	100	01	600	60	15	7	150	4	T7S	DN
	200	02			20	6				
	300	03			25	5				
	400	04			30	5				
	500	05			40	4				
	600	06			50	3				
	700	07			60	2				
	800	08								
	900	09								
	1000	10								
	1100	11								
	1200	12								
	1400	*14								

Example

Obtain optimum device performance for your application by selecting proper Order Code.

Type		Voltage		Current		Turn Off	Gate Current	Leads	
T	7	S	7	1	0	6	0	5	4	D	N

Type T7S7 rated at 600 A average with V_{DRM} = 1000V, I_{GT} = 150 ma, t_q = 30 μsec max. and standard control leads—order as:

*for maximum rating perimeters, consult factory

600A Avg (943 RMS) Up to 1400 Volts 15-60 μs

Fast Switching SCR T7S7__60

Voltage

Blocking State Maximums ① (T_J = 125°C)

	Symbol											
Repetitive peak forward blocking voltage . V . .	V_{DRM}	100	200	300	400	500	600	700	800	900	1000	1100	1200
Repetitive peak reverse voltage . V	V_{RRM}	100	200	300	400	500	600	700	800	900	1000	1100	1200
Non-repetitive transient peak reverse voltage, t ≤ 5.0 msec, V	V_{RSM}	200	300	400	500	600	700	800	900	1000	1100	1200	1300
Forward leakage current, mA peak	I_{DRM}	30											
Reverse leakage current, mA peak	I_{RRM}	30											

Current

Conducting State Maximums (T_J = 125°C)

	Symbol	T7S7__60
RMS forward current, A	$I_{T(rms)}$	943
Ave. forward current, A	$I_{T(av)}$	600
One-half cycle surge current ③, A . .	I_{TSM}	9000
I^2t for fusing (for times ≥ 8.3 ms) A^2 sec.	I^2t	338,000
Forward voltage drop at I_{TM} = 625 A and T_J = 25°C, V	V_{TM}	1.46
Min. repetitive di_T/dt A/μsec . . . ①②④	di/dt	400

Switching

(T_J = 25°C)

	Symbol	
Max. turn-off time, I_T = 400A T_J = 125°C, di_R/dt = 25 A/μsec, reapplied dv/dt = 20V/μsec linear to 0.8 V_{DRM}, μsec ①⑤ . . .	t_q	15 to 60
Typ. turn-on time, I_T = 1000A V_D = 300V ⑤, μsec	t_{on}	3.0
Min. critical dv/dt, exponential to V_{DRM}, T_J = 125°C, V/μsec ②⑤	dv/dt	300
Min. di_T/dt non-repetitive, A/μsec ①②⑥	di/dt	800

Gate

Maximum Parameters (T_J = 25°C)

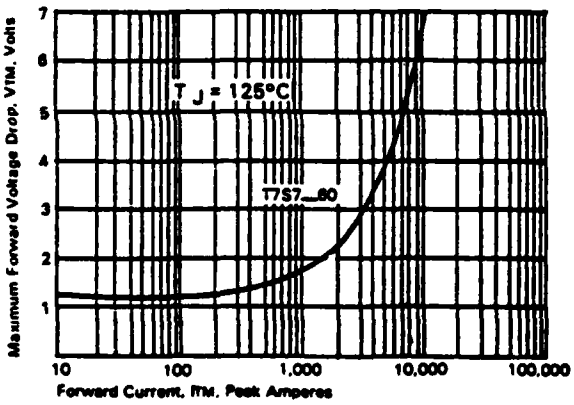
	Symbol	
Gate current to trigger at V_D = 12V, mA	I_{GT}	150
Gate voltage to trigger at V_D = 12V, V . . .	V_{GT}	3
Non-triggering gate voltage, T_J = 125°C, and rated V_{DRM}, V	V_{GDM}	0.15
Peak forward gate current, A	I_{GTM}	4
Peak reverse gate voltage, V	V_{GRM}	5
Peak gate power, Watts	P_{GM}	16
Average gate power, Watts	$P_{G(av)}$	3

Thermal and Mechanical

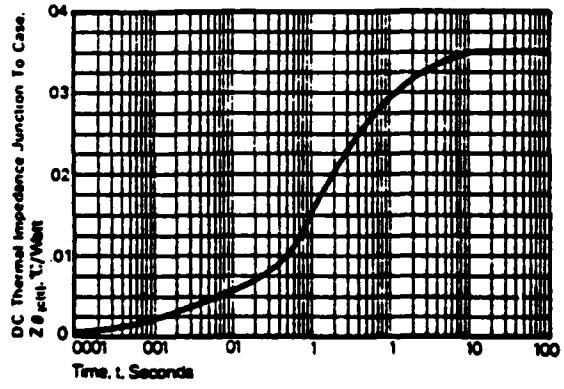
	Symbol	
Min., Max. oper. junction temp., °C	T_J	−40 to +125
Min., Max. storage temp., °C	Tstg	−40 to +150
Max. mounting force lb. ①		2000 to 2400
Max. Thermal resistance ⑦ Double side cooled Junction to case, °C/Watt . . .	$R_{\theta JC}$	.035
Case to sink, lubricated, °C/Watt	$R_{\theta CS}$	.02

① Consult recommended mounting procedures.
② Applies for zero or negative gate bias.
③ Per JEDEC RS-397, 5.2.2.1.
④ With recommended gate drive.
⑤ Higher dv/dt ratings available, consult factory.
⑥ Per JEDEC standard RS-397, 5.2.2.6.
⑦ For operation with antiparallel diode, consult factory.

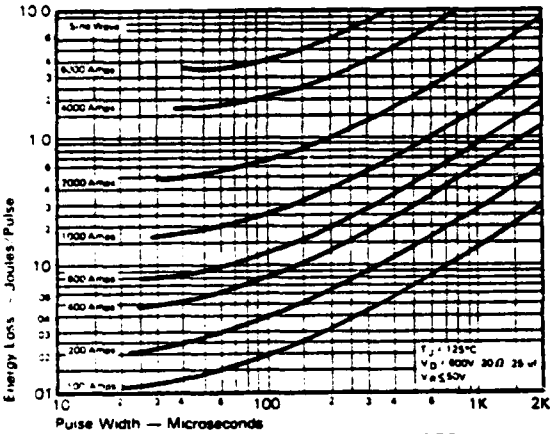
Maximum Forward Voltage Drop VS Forward Current



Transient Thermal Impedance VS Time

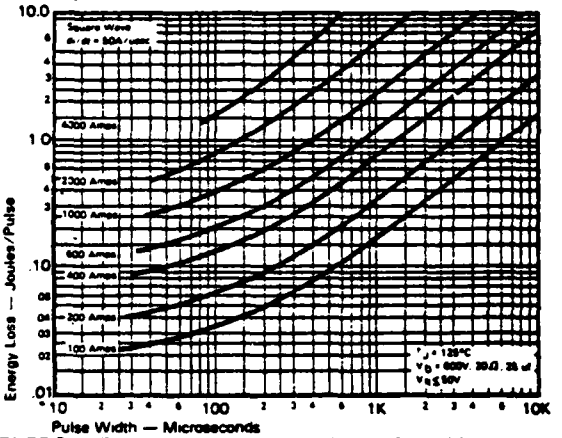


Sinusoidal Current Data

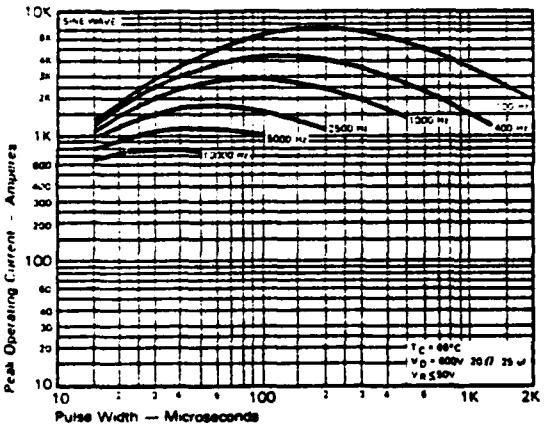


ENERGY PER PULSE FOR SINUSOIDAL PULSES

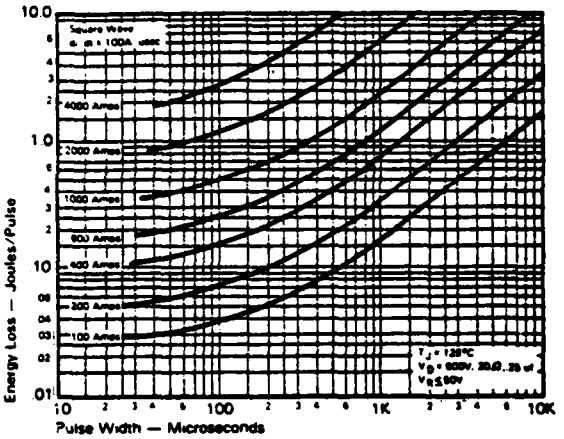
Trapezoidal Wave Current Data



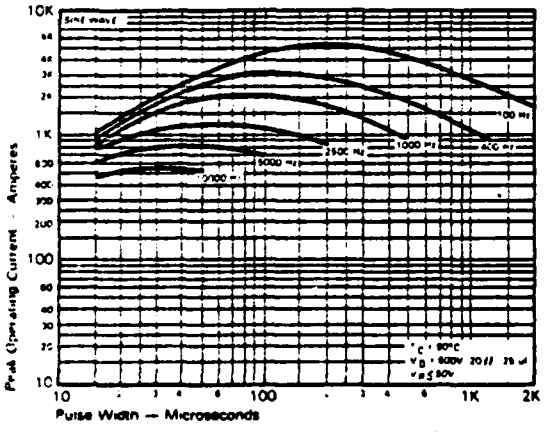
ENERGY PER PULSE FOR TRAPEZOIDAL PULSES
(di/dt = 50A/usec)



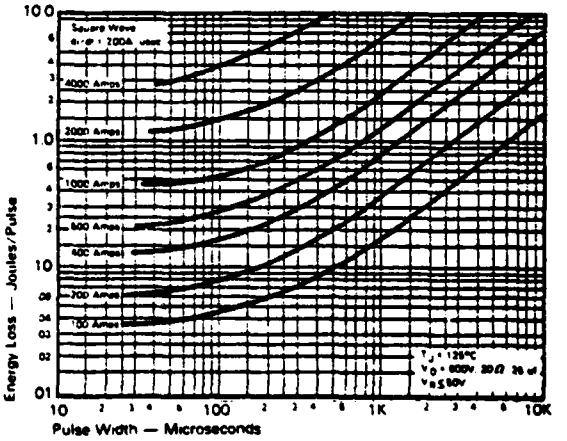
MAXIMUM ALLOWABLE PEAK ON-STATE CURRENT
vs. PULSE WIDTH (T_C = 65°C)



ENERGY PER PULSE FOR TRAPEZOIDAL PULSES
(di/dt = 100A/usec)



MAXIMUM ALLOWABLE PEAK ON-STATE CURRENT
vs. PULSE WIDTH (T_C = 90°C)

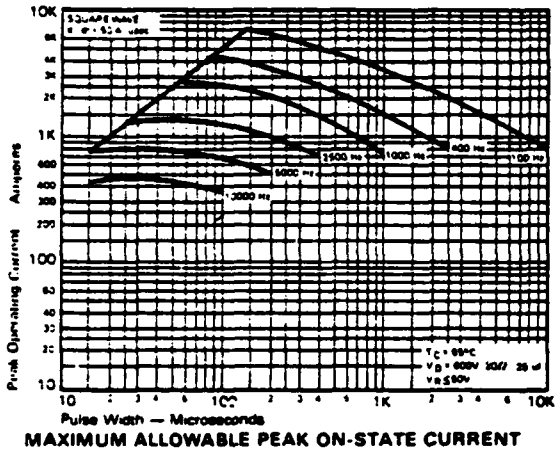


ENERGY PER PULSE FOR TRAPEZOIDAL PULSES
(di/dt = 200A/usec)

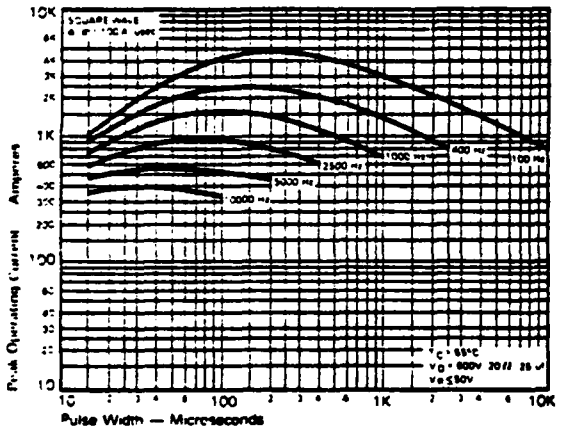
600A Avg (943 RMS) Up to 1400 Volts 15-60 μs

Fast Switching SCR T7S7__60

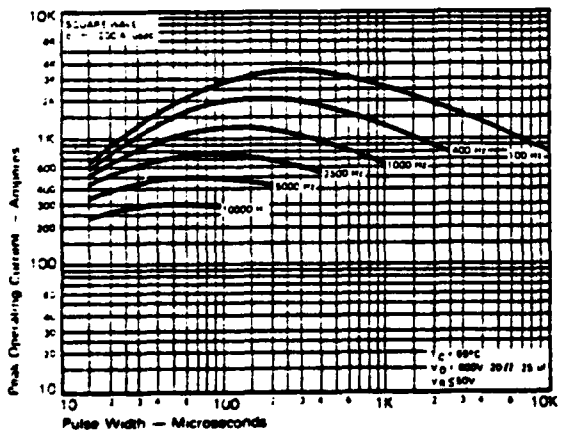
Trapezoidal Wave Current Data
(T_C = 65°C)



MAXIMUM ALLOWABLE PEAK ON-STATE CURRENT vs. PULSE WIDTH (di/dt = 50A/usec)

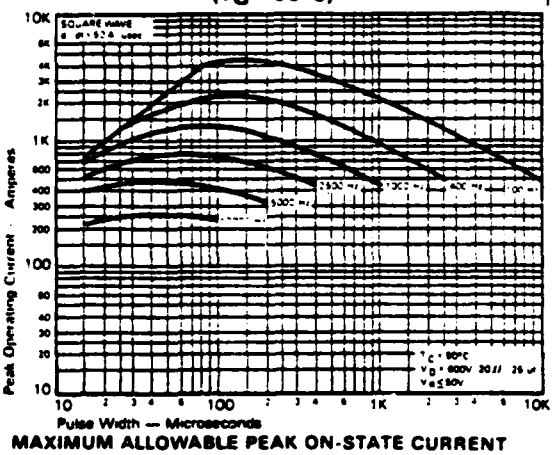


MAXIMUM ALLOWABLE PEAK ON-STATE CURRENT vs. PULSE WIDTH (di/dt = 100A/usec)

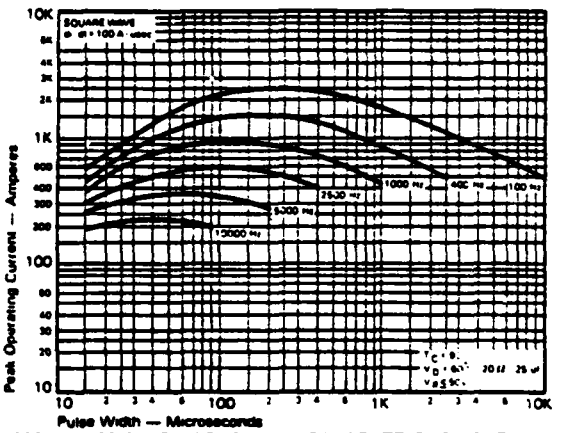


MAXIMUM ALLOWABLE PEAK ON-STATE CURRENT vs. PULSE WIDTH (di/dt = 200A/usec)

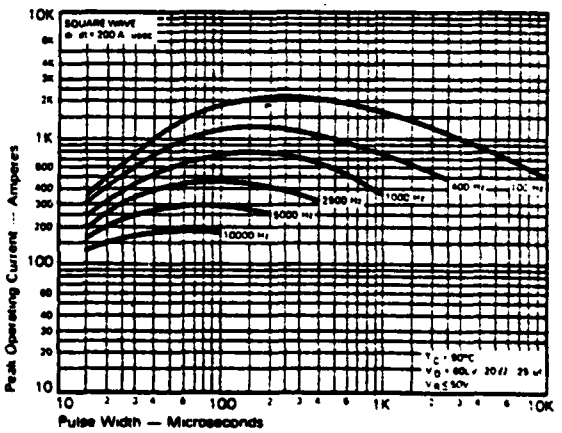
Trapezoidal Wave Current Data
(T_C = 90°C)



MAXIMUM ALLOWABLE PEAK ON-STATE CURRENT vs. PULSE WIDTH (di/dt = 50A/usec)



MAXIMUM ALLOWABLE PEAK ON-STATE CURRENT vs. PULSE WIDTH (di/dt = 100A/usec)



MAXIMUM ALLOWABLE PEAK ON-STATE CURRENT vs. PULSE WIDTH (di/dt = 200A/usec)

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of
Rome Air Development Center

RADC plans and executes research, development, test and selected acquisition programs in support of Command, Control Communications and Intelligence (C^3I) activities. Technical and engineering support within areas of technical competence is provided to ESD Program Offices (POs) and other ESD elements. The principal technical mission areas are communications, electromagnetic guidance and control, surveillance of ground and aerospace objects, intelligence data collection and handling, information system technology, ionospheric propagation, solid state sciences, microwave physics and electronic reliability, maintainability and compatibility.

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