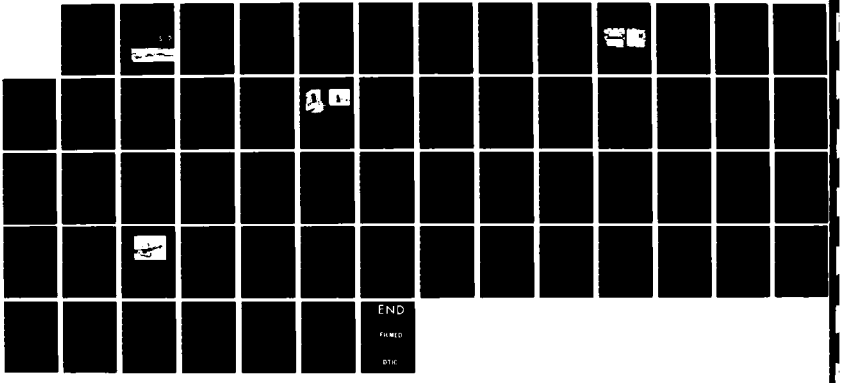
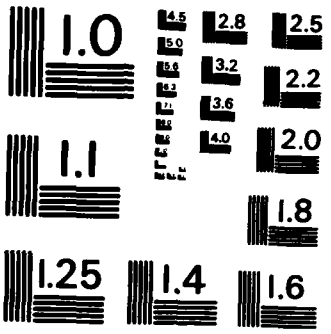
AD-A160 896 MANUFACTURING METHODS AND TECHNOLOGY FOR DIGITAL FAULT ISOLATION OF HYBRI.. (U) HUGHES AIRCRAFT CO FULLERTON CA GROUND SYSTEMS GROUP 01 MAR 82 HAC-FR-82-12-193 1/1

UNCLASSIFIED DAAH01-81-D-A002 F/G 9/3 NL





~MASTER

HUGHES
HUGHES AIRCRAFT COMPANY
GROUND SYSTEMS GROUP

Final Report

Manufacturing Methods And Technology For Digital Fault Isolation Of Hybrid Microelectronic Assemblies

Project No. R1023

1 MARCH 1982
CONTRACT NO. DAAH-01-81-D-A002

FINAL REPORT

Manufacturing Methods and Technology for Digital Fault Isolation of Hybrid Microelectronic Assemblies

Project No. R1023

Prepared for

U.S. Army Missile Command

Redstone Arsenal, Alabama 35809

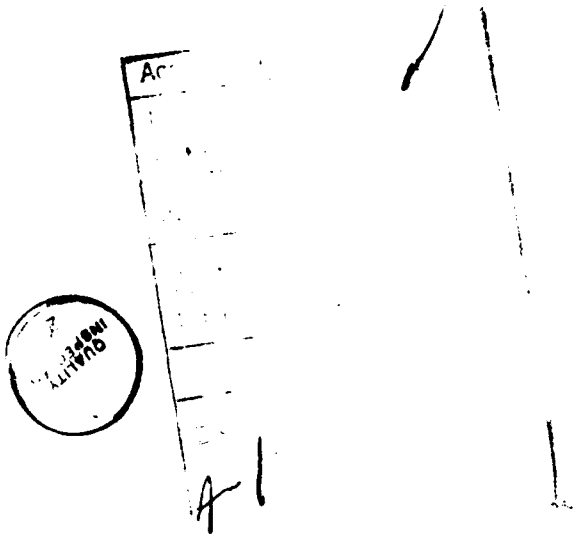
Project Officer: G. D. Little
DRSMI-RST
(205)-876-3604

Contract No. DAAH 01-81-D-A002
Task 0007
CDRL 002

Prepared by

Hughes Aircraft Company
Ground Systems Group
Fullerton, California 92634

Report Date: 1 March 1982
FR 82-12-193



FOREWORD

This final report presents the results, supporting data, and recommendations relating to an automatic test probe system (Autoprobe or AP) performed by Task 0007, under contract DAAH 01-81-D-A002. The program was identified as Project R1023 by the U.S. Army Missile Command at Redstone Arsenal, Alabama.

The manufacturing technology effort described by this report covers automatic test and fault isolation of digital hybrid microelectronic devices (D/HMAs) used in current and future production missile systems. A need for the single automatic probe, or Autoprobe, system was established by high production rate test and fault isolation of D/HMAs having complex LSI, microprocessor devices, and large number of I/O interconnections. Hardware and software resulting from project R1023 was further to be applied to the ATE system previously installed at Redstone Arsenal under project R783242.

An overview and objectives of project R1023 (or HFI Program) are presented in Section 1 of this report. Section 2 describes the work accomplished and includes the successful results of the Industry Demonstration for test and fault isolation of a D/HMA. Section 3 contains recommendations to achieve a full production type Autoprobe system and suggested future effort or study towards necessary AP improvements.

UNCLASSIFIED

SECURITY CLASSIFICATION OF THIS PAGE (When Data Entered)

REPORT DOCUMENTATION PAGE	READ INSTRUCTIONS BEFORE COMPLETING FORM
1. REPORT NUMBER	2. GOVT ACCESSION NO. HD-A160 846	3. RECIPIENT'S CATALOG NUMBER
4. TITLE (and Subtitle) Manufacturing Methods and Technology for Digital Fault Isolation of Hybrid Microelectronic Assemblies.	5. TYPE OF REPORT & PERIOD COVERED Final - June 1981, Feb. 1982
	6. PERFORMING ORG. REPORT NUMBER FR 82-12-193
7. AUTHOR(s)	8. CONTRACT OR GRANT NUMBER(s) DAAH-01-81-D-A002
9. PERFORMING ORGANIZATION NAME AND ADDRESS Hughes Aircraft Company Ground Systems Group Fullerton, California 92634	10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS Task 007 Project No. R1023
11. CONTROLLING OFFICE NAME AND ADDRESS U.S. Army Missile Command Redstone Arsenal, Alabama 35809	12. REPORT DATE 1 March 1982
	13. NUMBER OF PAGES 60 See 18
14. MONITORING AGENCY NAME & ADDRESS(if different from Controlling Office) AFPRO	15. SECURITY CLASS. (of this report) Unclassified
	15a. DECLASSIFICATION/DOWNGRADING SCHEDULE
16. DISTRIBUTION STATEMENT (of this Report) "Distribution Unlimited-Approved for Public Release"	
17. DISTRIBUTION STATEMENT (of the abstract entered in Block 20, if different from Report)	
18. SUPPLEMENTARY NOTES Final Report 60 pages	
19. KEY WORDS (Continue on reverse side if necessary and identify by block number)	
20. ABSTRACT (Continue on reverse side if necessary and identify by block number) (See next page)	

DD FORM 1 JAN 73 1473 EDITION OF 1 NOV 65 IS OBSOLETE

UNCLASSIFIED

SECURITY CLASSIFICATION OF THIS PAGE (When Data Entered)

ABSTRACT

The MM&T Fault Isolation of Hybrid Microelectronic Assemblies contract (HFI program) was awarded by MICOM of Redstone Arsenal, Alabama and performed by Hughes Ground Systems of Fullerton, California. This final report presents the results of project R1023 with supporting data and recommendations.

The HFI program objective was to establish the test and fault isolation requirements for complex digital, hybrid microelectronic assemblies (D/HMAs) of present, and future, production missile electronics. High production rate test and fault isolation of D/HMAs, would use a single probe (Autoprobe or AP) automated for X, Y, Z position, and operating under bus control of an external host computer or ATE system. Project R1023 hardware (HW) and software (SW) were also to be compatible with the ATE system HW and SW previously delivered to MICOM under project R783242.

Specific tasks, defined for the program objectives, were formally approved for a working task plan.

A survey of Hughes-Tucson, production D/HMAs established functional test requirements regarding complexity and physical parameters. Based on a maximum of 140 I/O pins per device, the survey confirmed the need for a single AP to test and fault isolate prior to device seal off.

A second survey selected the Hughes HMC-2460, automatic wire bonder, for the AP application, from among four other positioner candidates. Selection was based on performance of HW/SW, cost, and program schedule.

Hardware adaptation of the HMC-2460 required remounting the Z stage and CCTV camera to the X, Y stage and providing a tungsten probe tip. In addition self contained 6809 microprocessor software and firmware were supplemented for host computer positioning control. An existing design for the IEEE-488 circuit card provided bus communication.

Five elements of AP Interface software were developed for expedient AP control. The HMC-2460 and Hewlett Packard DTS-70 ATE combined SW required 2250 and 3325 program lines distributed among respective terminals.

Test software was purposely minimized by selection of a simple 22 pin D/HMA arranged to have 5 logic levels from input to output. Operating through the DTS-70 TESTAID and FASTRACE software, the test program required 170 lines and provided 0.94 fault detection capability. A test adapter, designed and built for the test, furnished interconnections, and switch selected, non-destructive SA1 or SA0 faults at nodes for a test condition.

Performance achieved by the AP ranged from 8.5 to 9.5 seconds per probe step, limited primarily by the ATE software overhead time.

The Industry Demonstration was conducted at Hughes-Irvine for a total of 44 guests. Following a technical presentation, the Autoprobe system and DTS-70 ATE were introduced and a functional GO/NOGO test was performed on the D/HMA. Test probing and fault isolation was demonstrated with D/HMA faults selected by guests.

To achieve a future production Autoprobe system, further effort and recommendations were made and include: CCTV camera with fiberoptics and probe tip ultrasonics; automatic D/HMA pattern recognition and X, Y alignment; high speed test data intercept SW; dynamic and parametric functional testing; and automatic D/HMA handler for high rate production testing.

CONTENTS

SECTION 1
HFI PROGRAM OVERVIEW

1. PROGRAM OBJECTIVES, TASKS, AND AUTOPROBE SYSTEM

In performing the Digital Fault Isolation of Hybrid Microelectronic Assemblies, or HFI program, Hughes Ground Systems has accomplished all major objectives of the MICOM MM&T effort to automate the functional test and fault isolation of D/HMAs.

Objectives - The HFI (for "Hybrid Fault Isolation") program bears directly on state-of-the-art automatic test systems for high volume production test and fault isolation of D/HMAs. The latter, as used in advanced missile electronic systems, typically contain complex LSI and microprocessor type circuit elements. Because of D/HMA economic factors, the test system fault isolation capability must extend to the minimum size component level or device (die) within a D/HMA.

Major objectives set by MICOM for the HFI program are as itemized.

- Establish the test and fault isolation requirements for production D/HMAs.
- Apply a single testing probe (Autoprobe or AP) automated for X, Y, Z position, and operating under control of an external host computer or Automatic Test Equipment (ATE) system.
- Provide AP system hardware, software compatible with a DTS-70 ATE system.
- Perform an Autoprobe system Industry Demonstration for test and fault isolation of a D/HMA candidate.

Through the six-month program effort, the resultant AP system hardware and software have fully satisfied these objectives.

Program Tasks - The HFI program was organized into major tasks, with scheduled milestones, and submitted to MICOM for approval through the CDRL 006, Task Plan. Task operations most essential to the program are presently summarized below and discussed in detail later in the report.

Administration - Management - Applied broadly experienced senior members to provide technical, administrative control of engineering personnel to meet scheduled item delivery.

AP Select - Analysis - Surveyed production D/HMA test requirements. Surveyed and selected a commercial X, Y, Z positioner for the AP adaptation.

AP Adaptation - Performed all probe, CCTV, mechanical and electronic modifications to the X, Y, Z positioner selected for the AP application.

ATE Interface - Candidate - Established the IEEE-488 positioner to host ATE data link requirements and selected a D/HMA test candidate.

AP Interface Software - Developed five elements of AP operational software distributed between the AP and host ATE.

Test Software - Developed the D/HMA test candidate functional test and fault isolation software for the host DTS-70 digital test system operating with the AP. A test adapter circuit was also designed and built for the D/HMA test candidate.

ATE/AP/SW Integration and Checkout - Completely integrated and proved out the entire ATE, AP, hardware and software for the D/HMA test demonstration.

Industry Demonstration - The AP system successfully performed a D/HMA test and fault isolation to guests representing Government, industry and Hughes agencies.

CDRL Items - Quarterly program reviews at MICOM, reports, and AP system photo slides were carried out according to contractual requirements and task plan of CDRL 006.

Autoprobe System - The resultant system configuration, shown in the photographs began with the AP Select-Analysis task and was progressively developed in both hardware and software during the program. AP system hardware was selected with consideration for the single test probe X, Y, Z positioning requirements, cost, and program schedule. The AP system test capability and accurate, reliable performance were demonstrated during actual test and fault isolation of the D/HMA test candidate.

Figure A. Hughes Modified HMC-2460 Autoprobe

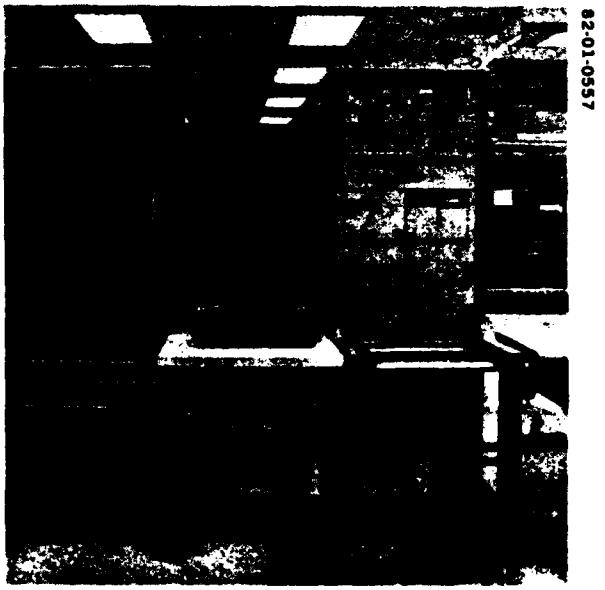


Figure B. Host ATE System, Hewlett-Packard DTS-70

Autoprobe System Equipment as Modified for the HFI Program

2. SUMMARY OF PROGRAM RESULTS

Performance results of the AP system test and fault isolation, with a D/HMA test candidate, fully support the MICOM objective for hardware and software compatible with the DTS-70, or other host ATE system, as exhibited during the HFI program Industry Demonstration.

As configured for the HFI program, the AP system hardware (HW) and software (SW) provide operating features that satisfy two main objectives of a single D/HMA test probe automated for X, Y, Z position, and of HW and SW compatible with the DTS-70, or host ATE. This operating test capability establishes a base from which to produce a production type AP system. To achieve full production D/HMA test capability, the present AP system requires skilled design and manufacturing effort and additional test features to provide:

- Automatic D/HMA pre conditioning and multiple test fixture socket load, unload.
- D/HMA automatic recognition and X, Y alignment.
- Dynamic functional GO/NOGO test.
- Controlled environment functional test, for parametric temperature -55°C to +100°C.
- High rate D/HMA test throughput, 5000 units per month or greater.

While maintaining HFI program objectives, the AP system developed HW and SW through quantitative information gained from surveys, conferences, and observing positioner equipment operation in similar applications.

The production D/HMA test requirements, covering 76 types, were surveyed and formulated from Hughes-Tucson device physical parameters, and electronic complexity. The upper limits of D/HMA parameters confirmed the need for the single autoprobe, and set the required operating range for X, Y, Z position (3in. x 3in. x 0.5in.) and microcircuit probe tip diameter (0.003in.). Actual position range achieved was 4.5in. x 2.5in. x 0.45in.).

Characteristics of five X, Y, Z positioner candidates were surveyed and quantitatively evaluated for performance and cost, and for schedule risk. Results of the positioner survey selected the Hughes HMC-2460 automatic wire bonder for the AP application. As an autonomous device, salient features of the HMC-2460 include 6809 microprocessor, software, firmware; ±0.1 mil X, Y position accuracy, with 20-pound bearing payload; 450-mil Z stage travel, with ultrasonic touchdown sensing; and software alignment of the work item, or D/HMA for X, Y, and θ coordinates. These performance features surpassed the AP system requirements.

AP adaptation of the HMC-2460 required remounting the Z stage and CCTV camera to the X, Y stage, providing a test probe with ceramic capillary and tungsten tip suitable for ultrasonic touchdown control, producing a fixed platform D/HMA socket mount for the D/HMA test candidate, and adapting the IEEE-488 bus electronics card into the HMC-2460 for the host computer or ATE control data link.

Five elements (modules) of AP interface software were produced for distributed AP control among the HMC-2460 and host (Hewlett Packard) DTS-70 ATE termini. The SW elements, discussed later in the report, appear in the table opposite which shows terminus, residency and number of programming lines.

Since a functionally reliable AP system was the primary HFI objective, the test software was purposely minimized by selection of a simple 22-pin D/HMA flatpack, having five TTL logic levels input to output, and consisting of inverters and NAND gates.

A test adapter was designed and built for the D/HMA test that could also furnish externally (switch) selected nondestructive SA1 or SA0 node faults for a test condition.

Operating through the DTS-70 TESTAID and FASTRACE software, the test program using 170 lines achieves 0.94 fault detection capability. The D/HMA GO/NOGO (functional) test is carried out in five seconds. Fault isolation probe time is within 0.6 to 2.5 minutes with a major part contributed by ATE system overhead.

Following integration and checkout, the AP system was used during the Industry Demonstration (CDRL 004 supplement) to test and fault isolate the D/HMA test candidate, using a host DTS-70 ATE. A total of 44 guests attended the ID at Hughes - Irvine in two separate conferences. Guests represented agencies in MICOM, (DRSMI-RST) industry, and Hughes divisions concerned with the AP system and D/HMA testing. The ID was well received and encouraged future effort for production AP system implementation.

AP INTERFACE SOFTWARE, MAJOR SW ELEMENTS AND DISTRIBUTIONS

SW Element	Principal Language	Program Lines and Terminus	
		DTS-70	HMC-2460
Probe Control Driver	Fortran IV	1100	
AP Utility	Fortran IV	1000	
Hybrid Alignment (X, Y, θ)	Ftn IV-6809 Assembly	150	300
IEEE-488 Driver	6809 Assembly		425
Command Processor/Executive	6809 Assembly		2500

SECTION 2
WORK ACCOMPLISHED

Section 2 - Work Accomplished
Subsection A - Digital Hybrid Microelectric Assembly (D/HMA) Survey

1. PRODUCTION D/HMA TEST REQUIREMENTS

The functional test requirements of Hughes - Tucson production D/HMAs surveyed can be met through an AP system having extended capability for dynamic and parametric temperature test, and high throughput with automatic UUT loading, recognition, and alignment.

A survey of production D/HMA test requirements for Hughes - Tucson missile systems, confirmed the need for a single type autoprobe (AP) test system and established most of the X, Y, Z positioner requirements.

Physical parameters of production D/HMA test requirements representing maximum or limit boundaries are shown in the table. For the 76 D/HMA types included, the package dimensions set the AP positioner X, Y, Z travel range requirements at 3 by 3 by 0.5 inches. The 0.5-inch AP height travel from the reference surface, for example, easily accommodates the 0.25 inch D/HMA substrate case or carrier height.

Most D/HMAs require from 80 to 90 input/output (I/O) test connections, with an upper limit of 140 I/Os. This feature bears on two facets of D/HMA test. First for a given D/HMA type, the test socket or fixture can be emplaced during the initial setup for a large quantity run or batch. Second is that 140 I/O test connections present technical risks of the ATE to UUT cable relating to:

- Cable length and test pattern bit rate transmission at MHz rates for dynamic tests.
- Cable long-term reliability under continued motion for high test throughput.

These considerations determined the AP positioner requirement to have a stationary UUT or D/HMA test fixture, with single test probe automated for X, Y, Z position.

The D/HMA minimum trace width of 0.005 inches (5 mils) with minimum spacing of 5 mils, set a requirement for the 0.003-inch maximum probe tip diameter for correct (unambiguous) circuit node probing.

Microprocessor, LSI devices, high circuit complexity, and dynamic as well as parametric test requirements are D/HMA or UUT features that determine overall ATE and autoprobe test versatility and method of production implementation.

Commercial ATE systems are available to perform functional dynamic tests of complex, microprocessor type D/HMAs. The production AP system design must further provide a D/HMA feed mechanism, multiple type test sockets or adapters, and a localized UUT vessel for functional tests at temperature.

The engineering model AP system, for the HFI Program, demonstrated most of the production D/HMA functional test requirements using an IEEE-488 bus data link under control of a DTS-70 ATE system. The mechanical feed, test adapter, dynamic and temperature test requirements were not included in the scope of the HFI program.

Through extended D/HMA test adapters and software, however, the DTS-70 offers the capability to provide dynamic functional or parametric voltage (UUT power) tests.

A microprocessor type D/HMA dynamic test and fault isolation, for example, can be accomplished with latch and ROM circuitry in the test adapter, and appropriate application software operating through the TESTAID-III SW. Main features of this Hewlett Packard progressive static and dynamic technique include

- Static digital test excluding (deactivated) microprocessor.
- Models UUT and test adapter as a ROM. Independent latches or registers from interconnecting ports to DTS-70 driver comparators.
- Exercises microprocessor functions or instructions at speed while ATE operates at lower test speed.
- Applies test sequence and test sequence file to fault isolate a failed component.

This test method, however, must be proven by further experimental testing to determine its suitability for high volume production test rates.

PRODUCTION HYBRID TEST REQUIREMENTS

Item	Unit	Requirements
Digital Types		76
Package Dimensions	in	2.7 x 1.4 x 0.25
I/O Pins		140
Dice/Hybrid		50
Wire Bonds/Hybrid		400
Circuit Trace	μ in	250
Trace Width/Space	mils	5/5
Multiple LSI/Hybrid		Microprocessor
Circuit Complexity		High
Substrate Type		Thin Film - Thickfilm, (ML)
Functional Tests		Static, Dynamic, Parametric V, T $-55° \leq T \leq 100°C$
Throughput (Initial)	hybrids/month	5000

1. POSITIONER CANDIDATES AND SELECTION OF THE HMC-2460

The AP positioner survey of five candidates selected the Hughes HMC-2460 automatic wire bonder to provide high performance positioning with hardware and software modifications suitable to the Autoprobe (AP) application.

Positioner Candidates - The Autoprobe X, Y, Z positioner requirements were derived and formulated from the previously established production D/HMA test requirements. Selection of a suitable AP positioner was accomplished through a thorough survey of five candidates shown in Table I.

The survey tabulated important positioner hardware and software characteristics including:

- X, Y, Z mechanical position, range, increment, accuracy, and load capacity.
- Angular alignment of work item or UUT, and viewing equipment.
- UUT surface contact (touchdown) method and control.
- Software and firmware features for random access positioning and host control.
- IEEE-488 data link for host control.
- Economic factors; cost to implement for AP application.

In addition to tabulated performance characteristics, the positioner candidates were discussed with other users (in and outside Hughes) for actual performance. HFI program personnel further observed actual operating demonstrations at Hughes for the Rucker-Kolls 1032 and the Hughes HMC-2460. Actual operation of the Electroglas 1034X was observed at Frontier Incorporated (Costa Mesa, Ca) in a computer-controlled test of production wafers containing 1200 dice.

As shown in Table I, the HMC-2460 and 1034X survived prescreening and passed to final evaluation. The Probe 2,1032(R-K), and PR 100 were eliminated based on major characteristics in the results column that did not directly meet the AP positioner requirements.

Selection of HMC-2460 - Selection of the Hughes HMC-2460 (automatic microcircuit wire bonder) was determined by its excellent performance features and least schedule risk to the HFI program. The major X, Y, and Z stage positioner characteristics are summarized in Table II which presents the HFI required parameter values, and comparative performance supplied by the two final candidates - HMC-2460 and 1034X.

Among the HMC-2460 performance features that surpass HFI requirements with ample margin, are its positioning accuracy, bearing load capacity, and Z stage travel range with servo control of surface contact.

The random access feature of X, Y position is required because the D/HMA test and fault isolation backtrace probing is host computer directed and is not a repeatable routine that can be "learned." The HMC-2460 software, firmware, therefore, required adaptation as shown.

Host control of the AP system, using the HMC-2460, required adaptation of an existing design for the IEEE-488 bus electronics, which also included a test switch function (logical 0) for the DTS-70 ATE. Appropriate IEEE-488 driver software was required to complement the data link hardware.

Selection of the HMC-2460 increased the amount of AP interface SW with a compensating reduction in mechanical design effort. Major features resulting in its selection include:

- X, Y stage accuracy of ± 0.1 mil.
- Ultrasonic Z stage touchdown sensing to protect D/HMA conductor trace.

- D/HMA alignment software and firmware to translate UUT relative X, Y coordinates to positioner absolute X, Y coordinates.
- Bearing load capacity of 20 pounds; permits mounting Z stage and CCTV camera to the X, Y stage for AP X, Y, Z positioning.

TABLE I. HFI AUTOPROBE POSITIONER CANDIDATES

Device Model	Supplier	Function	Results
1034X	Electroglas	Positioner X, Y, Z,	Final Evaluation
HMC 2460	Hughes CB	Wirebonder	Final Evaluation
Probe 2	Pacific Western	Positioner	Limited Z, 40 MIL Minimal Customer Contact
1032	Rucker-Knolls	Positioner	Difficult SW Application
PR100	Teledyne TAC	Positioner	Limited Z, 15 MIL Needs Host Comp Link Dev No Host Readback X, Y 12 Wk ARO

TABLE II. HFI AP POSITIONER CHARACTERISTICS

Parameter	Unit	HFI Required	Electroglas 1034X	Hughes HMC-2460
X, Y Stage				
Travel	In x In	3 x 3	5 x 5	4.3 x 4.3
Accuracy	±MIL	0.5	0.5	0.1
Θ Alignment	±ϕ°	5	360 Manual*	By Software
Alignment		Manual	Manual + SW	Manual + SW
Random Access		Yes	Yes	Adapt SW
Bearing Load	LB	5 - 10	7	20
Z Stage				
Travel	MIL	250	250	450
Over Travel	MIL	10	9	NA
Increment	MIL	1	0.5	0.8
Contact		Optional	Edge Sens.**	Ultrasonic
Host Computer (Interface)	IEEE-488 RS-232C	Either	Available Opt D	Adapt HW + SW
Availability ARO	WK	10/12/81	6 - 8	6 - 8

* Alternately By Host Computer SW
** Not Directly Applicable to Hybrid Because of Obstructing Die and Wire Bonds

1. HMC-2460 EQUIPMENT ADAPTATION

Adaptation of the HMC-2460 wire bonder for the Autoprobe application was achieved by judicious remounting of the CCTV camera and Z stage, and with mininal design effort for the test hybrid socket mount and test probe tip.

As a self contained automatic wire bonder, the HMC-2460 operating system of hardware and software does not interact with external peripherals or host system. Adaptation of the HMC-2460, however, for the host controlled AP application was accomplished by four modification tasks as outlined.

- Remounting the Z stage and CCTV camera to the X, Y stage.
- Producing a fixed platform D/HMA socket mount for the test candidate.
- Providing a test probe with ceramic capillary and tungsten tip.
- Incorporating the IEEE-488 bus electronics card for host computer control of the AP.

The photo of Figure A shows the HMC-2460 AP hardware adaptation at a time shortly before completion. The entire servo controlled Z stage was mounted to the X, Y stage using its original mounting plate to straddle two vertical brackets. The Z stage appears at the dark assembly between the lower part of the vertical brackets.

Similarly the CCTV camera was mounted to the X, Y stage by its original base plate to retain the camera optical focus adjustment mechanism. In an attempt to display the probe tip when contacting the test D/HMA surface, the camera optical axis was inclined in one plane approximately 12.5 degrees from the vertical or zenith.

A close up of the D/HMA in its test socket is shown in the photo of Figure B. The test socket used two parallell 11 pin IC sockets (Azimuth Electronics, 5226-050-11) having lead wire locking clamps. A fiberglass laminate, bonded between the sockets, firmly supports the bottom part of the D/HMA test candidate. Each 11 pin socket was securely wired to one half of a combined 22 wire flat ribbon cable which was routed to the test adapter and terminated at the DTS-70 ATE test fixture. This cable supplied the D/HMA test candidate with power and digital data.

The socket assembly was further fastened to an aluminum pedestal and bolted, at a fixed location, to the massive, stationary X, Y stage mounting plate. Probe tip coverage of the entire D/HMA test candidate, in Figure B, was assured by locating the D/HMA lower right corner at X, Y coordinates of 0.09, 0.09 inches relative the probe tip origin X, Y coordinates at 0.00, 0.00.

Wirebonding assemblies, electronics, and viewing microscope assembly, not required for the AP, were removed. A Z stage motor protective shield and a DTS-70 test probe cable were added as required. To complete the adaptation, the plastic deck cover cutouts were extended to clear the test socket and allow the X, Y stage structure travel clearance.

As remounted, the CCTV camera was physically rotated 90 degrees which also rotated the TV display for X, Y orientation. This, however, was not a problem during operation.

To avoid a physical travel interference of the CCTV camera with the display panel, the Y axis limit switch was repositioned to restrict Y travel to 2.5 inches (measured) while maintaining full X travel of 4.5 inches (measured). The net X, Y range was ample for normal probing operations.

81-11-890

Figure A. The Hughes HMC-2460 Automatic Wire Bonder Adapted for Autoprobe Testing

81-11-892

Figure B. Closeup View of the D/HMA Test Socket and Ceramic Capillary Mounted to the Ultrasonic Bar

2. DESIGN OF THE PROBE

The main test probe design parameters are probe diameter and safe contact pressure, which were established as three mils and 30 grams respectively.

A 3 mil diameter tungsten wire was selected for the probe tip. This selection satisfied requirements of the D/HMA trace width of 5 mils, spacing of 5 mils and positioner objective accurracy of ±0.5 mils. To avoid circuit trace damage (tested and discussed later) a probe tip force of 30 grams or less provides safe contact pressure.

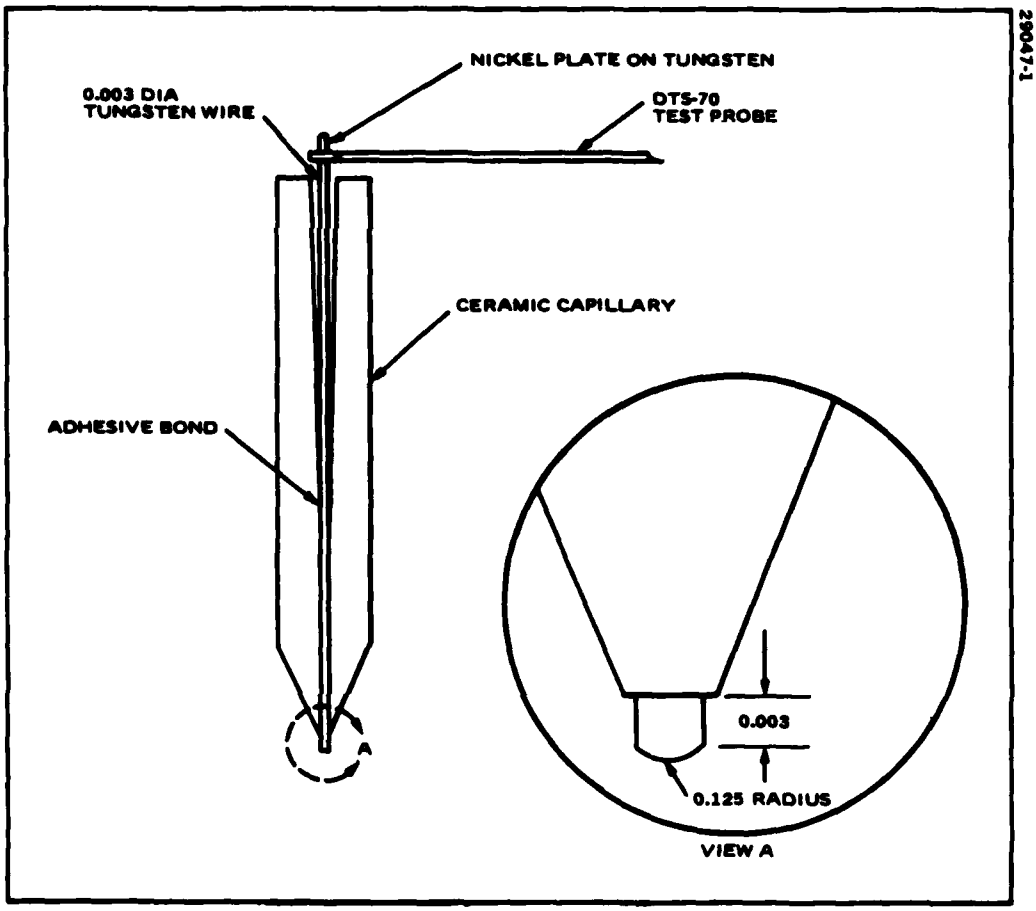
To utilize the HMC-2460 ultrasonic, servo controlled touchdown sensing, the 3-mil probe wire was mounted in a ceramic capillary as shown in the Figure. The capillary mounting, to the cylindrical ultrasonic bar of the Z stage, is shown near the center of the Figure B photo in the preceding topic, before installation of the test wire. Three probe tips were procured for the demonstration.

With moderate input impedance probes, as the DTS-70 ATE test probe, (approximately 100K ohms) the D/HMA test probe contact resistance is orders of magnitude less, and therefore not a problem. In cases where probe contact resistance is significant, (as in low resistance measurement) probe resistance errors can be corrected by system test software.

Although convergence of the TV camera optical axis with the hybrid surface, and test probe tip were closely controlled, the probe tip appeared out of focus, at the TV display, relative to the magnified, sharp hybrid circuit image. The probe image, however, is not essential to the AP operation. In practice the camera electronic crosshair X, Y displacement (in mils from the probe tip contact point) was measured and displayed at the HMC-2460 keyboard terminal. The measured X, Y displacement is corrected for in the HMC-2460 software to achieve accurate probe positioning to the hybrid circuit test node.

The TV camera with electronic crosshair is vital to initial alignment of the test hybrid for X, Y coordinates and θ (angular rotation) using the hybrid alignment software developed.

Overall the modified HMC-2460 successfully passed the X, Y positioning accuracy test and proved to be a reliable performer in test probing operations.



Construction Details of D/HMA Test Probe. The ceramic capillary supports the tungsten test probe wire, as well as propagating the ultrasonic energy.

3. IEEE-488 BUS AND HOST INTERFACE CONTROL

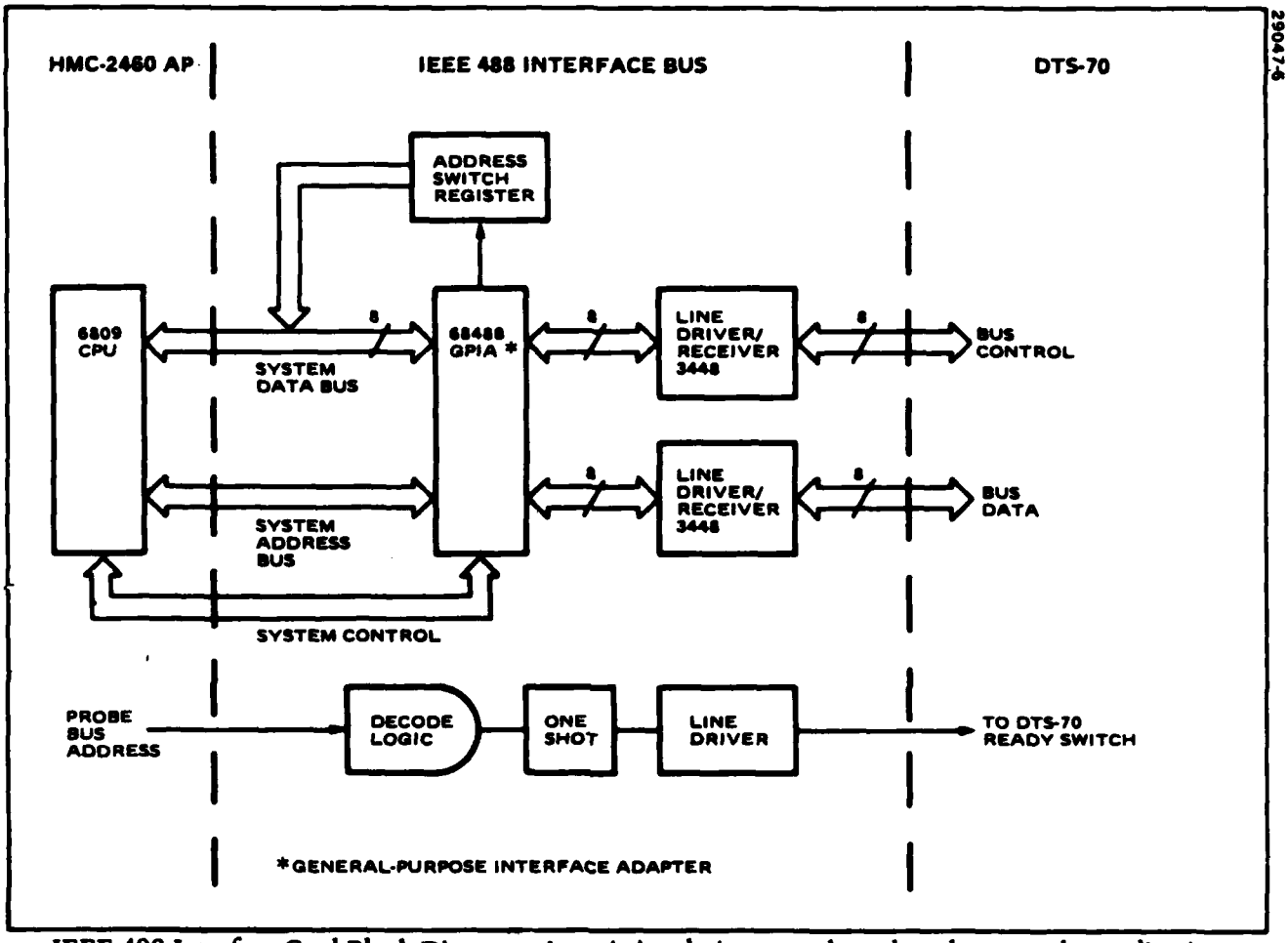
A specialized circuit card provides for communication between the HMC-2460 Autoprobe and the HP DTS-70 ATE over the IEEE-488 instrumentation bus.

Communication between the HMC-2460 Autoprobe and the HP DTS-70 ATE is via the IEEE-488 instrumentation bus. This bus was originally developed to provide a standard format for the exchange of data and control signals between the instruments of a system. The bus is bidirectional and provides sixteen parallel lines, eight for data and eight for bus management and data transfer control. The task of controlling the bus communications between the HMC-2460 and the DTS-70 is accomplished with a single interface card. The block diagram of this interface card is shown in the figure.

Three special-purpose integrated circuits are utilized on the interface card to provide this bus controlling capability. The three integrated circuits are the Motorola MC68488 General Purpose Interface Adapter (GPIA), and two Motorola MC3488 bus drivers. The MC68488 GPIA circuit was designed specifically to interface the MC6800 family of microprocessors to the IEEE-488 bus. This circuit provides all the signals required to control communications between the MC6809 microprocessor and the DTS-70. The MC3448 circuit is a bidirectional bus driver and receiver used to provide the high current driving capability necessary when using long cables. The address switch register shown in the figure is used by the GPIA to identify which instrument the 6809 will be communicating with over the bus, in this case the DTS-70.

A second function provided by the interface card is the generation and transfer of the DTS-70 READY switch signal. The interface circuitry monitors the microprocessor's address bus and whenever the ready signal's address is detected a pulse is generated by the one shot. This ready switch pulse is then buffered with a line driver and presented to the DTS-70.

The IEEE-488 circuit card presented was adapted from an existing design and successfully operated in the Autoprobe system for the D/HMA test and fault isolation.



IEEE-488 Interface Card Block Diagram. An existing design was adapted to the autprobe application.

1. HMC-2460 AUTOPROBE

The HMC-2460 Autoprobe is a host computer controlled multiple microprocessor X, Y and Z positioning system. Its advanced electronics and software design provide high mechanical resolution, simplified interfacing, and minimal operator intervention.

The HMC-2460 Autoprobe block diagram is shown in the figure. The following describes the elements of the HMC-2460 and their relationships.

Main Electronics and Power - The main electronics and power cabinet houses the system power supplies, servo power supplies, main CPU, system RAM and ROM memory, X, Y and Z stage drive interfaces, and other interfaces to the various HMC-2460 subsystems and host computer. The system power supplies supply all the required voltages for the various system components with the exception of the CCTV camera, TV monitor, and the X, Y and Z stage servo motor. The X, Y and Z stage servo power supplies provide the required operating voltages to the individual stage servo motors. There is one power supply for each stage and each has built-in protection designed to prevent damage to itself or its respective stage components.

The main CPU is a Motorola 6809 microprocessor. Supporting the main CPU are 28 Kbytes of RAM memory and 28 Kbytes of ROM memory. With the exception of certain system diagnostic programs, all Autoprobe resident software is located in ROM. The RAM memory is utilized for run-time scratch and variable storage. The X, Y and Z stage interfaces are also microprocessor controlled but operate under control of the main CPU. Each interface is comprised of a Motorola M6809 microprocessor, RAM and ROM memory, and associated support circuitry. These interfaces communicate with the main CPU via a bi-directional Parallel Interface Adapter (PIA). This design allows stage movement in all 3 axes simultaneously, optimizing the probe movement process.

For CCTV system, there is a crosshair and sync-generation interface card. This card allows physical alignment of the actual probe touchdown point with the crosshair targeted point at the viewing monitor. DIP switches on this card provide various operating modes for the crosshairs.

The IEEE-488 interface implements the host computer data and control link. Also contained on this interface card is the probe ready signal generation and driver circuitry. Additional interfaces include those for the keyboard, display, and ultra-sonics generator.

Visual Targeting System - The visual targeting system is comprised of the CCTV camera, a 9-inch B&W TV monitor, and the crosshair/sync generation circuitry in the main electronics cabinet. It is utilized for manual location or adjustment of fault node test points. Illumination is provided by a light source through fiber light pipes with terminating lenses mounted to the camera magnifying lens system. The CCTV magnifying optics consists of a single lens, and telescoping tube system. Focusing is accomplished manually at the camera pedestal. The CCTV camera is offset approximately 12.5° from vertical for line-of-sight clearance past the probe capillary and support arm. Physical target offset (the distance between the crosshair targeted touchdown point and the probe physical touchdown point) is compensated for automatically in the AP software. This compensation can be verified or reset by the operator when necessary to maintain camera crosshair to probe alignment. The probe touchdown point is displayed in the crosshairs on the TV monitor.

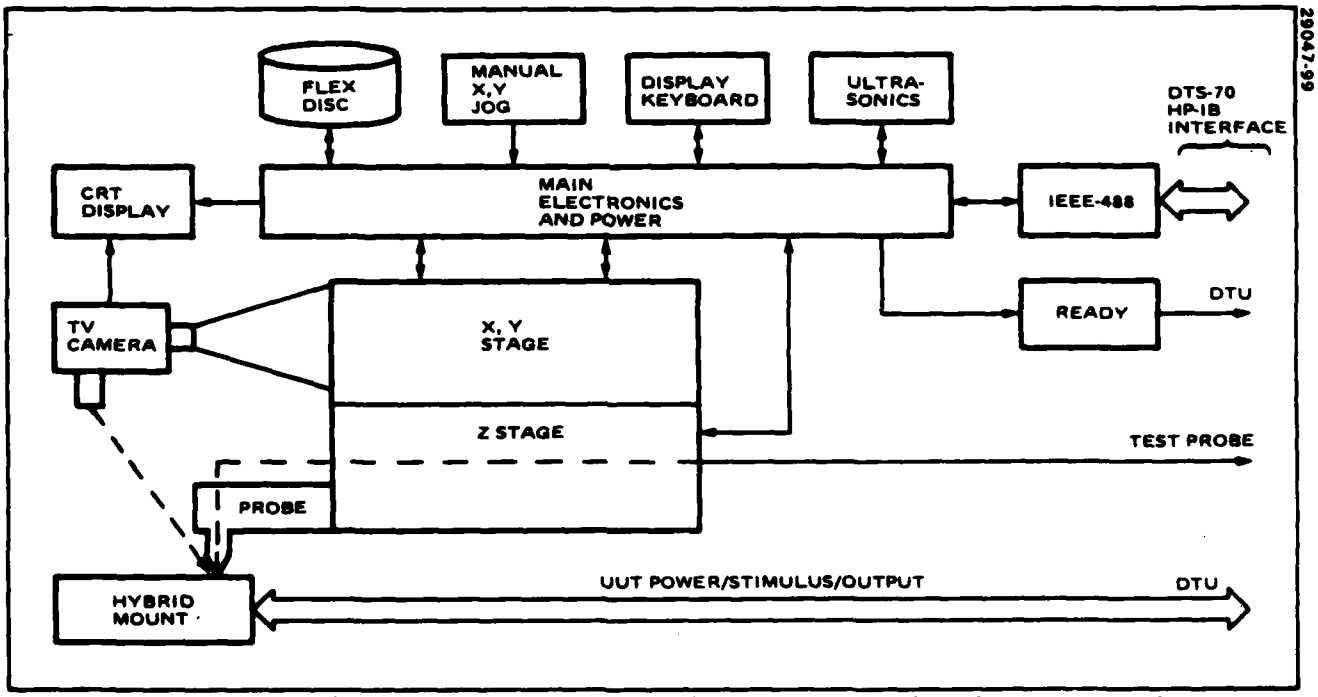
Flexible Disc - The flexible disc drive is a standard 5-1/4" model. It is used for diagnostic program loading for use by field maintenance engineers.

Jog Knobs - The two jog knobs are located at the front of the AP operator's control panel. These are used to manually adjust the X, Y position of the probe.

These knobs are enabled or disabled automatically by the AP software to prevent unauthorized or accidental changes to the probe position during testing.

Display/Keyboard - The system display/keyboard is the human interface to the AP. The display is a 32-character dot matrix type that is used to inform the operator of error conditions, prompt him through a sequence of steps, or display messages from the host computer. To eliminate the possibility of lost messages, the system will not clear a displayed message until the operator acknowledges it via the keyboard. The keyboard contains 19 function keys and 10 numeric keys. The function keys are backlighted to indicate an enabled condition or operational mode. A flashing key indicates an expected response from the operator. As with the jog knobs, the keyboard is enabled and disabled by the AP software to eliminate erroneous operator input at specific times.

Ultrasonics System - The ultrasonics system is comprised of an ultrasonic generator, transducer, probe assembly, touchdown sensor circuit (servo), and the ultrasonic interface in the main electronics cabinet. The ultrasonic system is used to determine probe surface contact and is a practical alternative to either an edge sensor or fixed over travel method. The ultrasonic interface controls the output power level of the ultrasonic generator, and returns status to the main CPU when touchdown is detected by the touchdown sensor circuit. The transducer is matched to an 0.437-inch ceramic capillary in which a tungsten probe tip is epoxied in place.



HMC-2460 Autoprobe Block Diagram. The system and servo power supplies, the main CPU, the system RAM and ROM memories, and the X, Y and Z interfaces to the various HMC-2460 subsystems and host computer are all housed in the main electronics and power cabinet.

IEEE-488 Interface - The IEEE-488 link was implemeted for HOST/AP data transfer and control. Data transfer is bidirectional and may originate at either the HOST computer system or the AP. The AP does not originate any bus control signals, but responds to those generated by the Host computer or system controller. The AP may be regarded as a slave of the Host computer. It performs no action or sends no data until commanded to do so by the Host. The capabilities of the AP, as defined by the IEEE-488 standard of 1978, are: SH1, AH1, T8, L4, SR0, RL0, PP0, DC1, DT0, C0 and E1.

Ready Line Interface - The READY line interface is a simple one-shot line driver circuit that simulates a switch closure for the normal guided probe to the DTS DTU probe interface. It generates a negative going pulse of approximately 150 milliseconds. This circuit is activated by the AP software when probe touchdown is detected or when the Probe Trigger key is depressed and the AP is in the proper mode.

X, Y Stage - The X, Y stage runs on a set of cross-roller slides with a maximum stop-to-stop travel limit of 4.3 inches in each direction. Both X and Y axis motors are low intertia, high torque, DC voltage type and are rigidly mounted to the X, Y slide. One increment of the X or Y motor encoder results in 0.0001 inches of table travel. Linear accuracy is within 0.0001 inches per foot of travel with repeatability of $\pm$0.00005 inches. The speed and direction of the X or Y motor are controlled by the respective driver circuit under the direction of the central processor.

Z Stage - The Z stage is a rack and pinion drive system controlling the vertical travel of the probe mechanism. The probe mechanism is held in position by a pair of cross roller slides with a maximum stop-to-stop travel of 0.450 inches. The Z axis motor is a low-inertia, high torque, DC voltage type and is rigidly mounted to the X, Y stage. One increment of the Z axis motor encoder results in 0.0008 inches of probe travel. The Z stage includes the probe mechanism and ultrasonic transducer. The speed and direction of the Z axis motor is controlled by the Z stage driver under direction of the central processor.

2. HOST DTS-70 CONTROLLER AND EXECUTIVE SOFTWARE

The System Controller, combined with its executive software, enables the DTS-70 to operate three different production test stations simultaneously, with as many as six different programmers developing new test software at the same time.

The hardware and software breakdown of the test System Controller is shown in the table opposite. The hardware block diagram is shown in the facing figure.

The System Controller (SC) uses the HP 1000 computer system (HP 2176C) as its central core of operations. It has been supplied with 256 KBytes of high performance memory and four 16 channel I/O interfaces. With this SC, the DTS-70 can support high-level languages such as FORTRAN, COBOL, BASIC, and ATLAS. It has the capability of controlling three Test Stations, reducing the need for test software to one set of software for every three Test Stations. The SC is conducive to system expansion by allowing additional peripherals to be easily integrated with the system. The SC hardware consists of four major elements.

Hewlett Packard Interface Bus (HP-IB) - The HP-IB is Hewlett Packard's implementation of IEEE Standard 488-1975, Digital Interface for Programmable Instrumentation. The HP-IB is capable of linking up to 15 devices at one time.

Disc Drive - The HP 7906 is a 20-MByte master disc drive with a disc controller for interface with the HP 1000. It has an upper (removable) and lower (fixed) disc, each having a ten MByte capacity. Each disc is subdivided further into:

- 4 Logic Units (LU)
- 293 Tracks (TRK)/LU
- 12.2 KBytes/TRK

Line Printer - The HP 2613A is a 136-column, 300 LPM printer. It has a 64 ASCII character set with the option of other character sets.

Keyboard/CRT Terminal - The HP 2621A is a keyboard, display terminal with 3840 bytes of RAM memory. The keyboard is full ASCII code with eight user definable function keys. The CRT screen is 24 lines by 80 columns with video and inverse video display modes.

For the HFI program, four elements of HP systems executive software were provided.

RTE IVB - The Real Time Executive (RTE), version IVB is the operating system software. It programs in FORTRAN and Hewlett Packard Assembler with expansion capability for other languages. The RTE manages operations of the computer, main memory, disc memory storage, and all I/O devices.

TESTAID - This software supplies simulator-based test program generation for digital circuits. It can be used to both manually and automatically generate test patterns for fault isolation, while simultaneously keeping track of the percent fault detection. TESTAID is made up of the following subprograms:

- SGLST - Topology generation.
- SMSET - Fault directory generation.
- SIMUL - Simulator and test pattern generation.
- PATDK - Post processor program, creates the Preliminary Test File for FASTRACE.

FASTRACE - This software provides the test program executive for UUTs. It performs pass, fail testing and the computer-guided probing if a failure is found. FASTRACE is made up of the following subprograms:

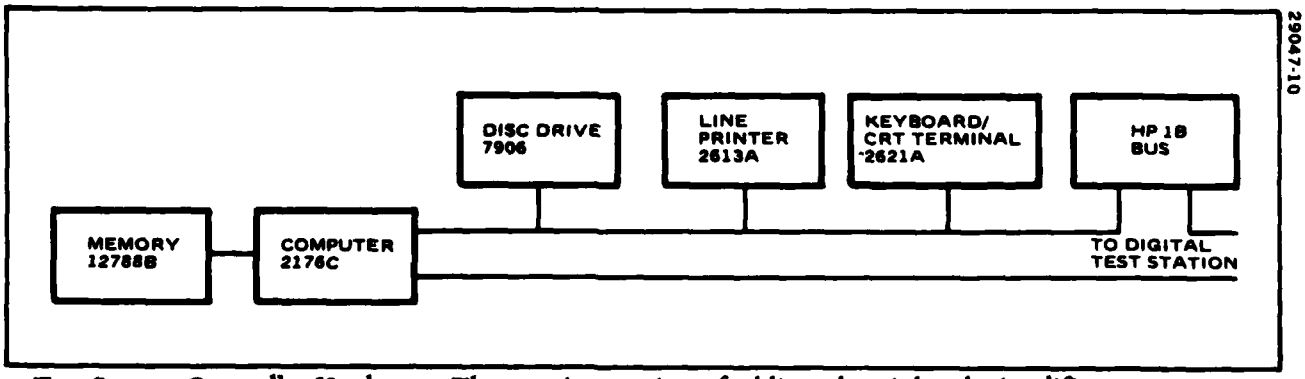
- SETUP - adds hardware setup data to the Test file.
- CHECK - performs hardware confirmation of values specified in SETUP.
- PONOF - applies and removes power from the UUT.

- GONO - performs the pass, fail test on the UUT.
- PROB - performs fault isolation to the node on a failed UUT.

Diagnostic Self Test - Software for two system tests is provided to verify test station operation. These are the System Functional Test (SFT) and the System Performance Test (SPT). The SFT is a comprehensive test which verifies that the various stimulus, response, measurement, and switching functions of the Digital Test Unit (DTU) are working correctly. It serves as a good test for checking system integrity before actual production testing begins. The SPT serves as an excellent overall system calibration test and is used for maintaining functions to the required specifications.

HFI TEST SYSTEM CONTROLLER

Hardware	Software
Computer - 2176C -four 16 I/O Channels Memory - 12788B -256 KByte Peripherals -Disc Drive - 7906, 20 MByte -Line Printer - 2613A, 300 LPM -Keyboard/CRT Terminal; 2621A Interface -HP-IB	RTE IVB-Operating System, 92068A TESTAID-Simulator, 91075B FASTRACE - Fault Isolation Diagnostic Self Test, Tape CT



Test System Controller Hardware. The easy integration of additonal peripherals simplifies test system controller expansion.

3. DESCRIPTION OF THE HOST DTS-70 DIGITAL TEST STATION

The HP 9571A Digital Test Station can handle the testing of digital circuits having multiple power requirements and mixed family logic. It is well suited to meet the challenges of the 1980s in digital circuit testing requirements.

The HP 9571A Digital Test Station block diagram is shown in the figure opposite. The following describes features of the test station's major hardware.

Digital Test Unit (DTU) - The DTU is an integral part of the digital test station. It is computer controlled through user programs to generate stimulus signals to the unit under test (UUT), to check the expected responses, and to interrupt the controller in case of a test failure. The DTU is capable of testing TTL, CMOS or mixed logic digital circuits. For mixed logic testing, the DTU contains eight programmable driver/comparator (PDC) cards with a capacity expandable to 24 cards. Since each card operates with 15 DTU I/O pins, the eight cards provide a total of 120 I/O pins for the HFI system configuration.

To accommodate mixed logic or frequent changes in board logic types tested, the PDC card can operate under program control. Logic high or low voltage circuits (two each) may be programmed over a range of -16V to +16V with ±80mV accuracy. The programmed voltage is common to all 15 I/O pins in any one set. Each driver can supply a maximum of 20mA up to 14V. The PDC card can operate with any one of four voltage reference sets supplied by the DTU.

Programmable Rate Generator (PRG) - The PRG is an option that provides a digital waveform signal on a coaxial connector at the system interface. It is used whenever high-speed refresh clocks are required for dynamic devices. PRG output is controlled by a user test program. Its waveform can be a continuous pulse train or a specific number of pulses. Pulse width and delay are programmable from 100 nsec to a maximum of 100 sec at a resolution of 0.1%, thus allowing a maximum repetition rate of 5 MHz.

Repair Ticket Printer - The HP 5150A Thermal Printer provides a hard copy of the test failure report. The printer outputs the test result at six lines per inch on a 2-1/4 inch wide strip of paper. The report can be conveniently torn off and attached to the failed UUT for repair station action. The printer is controlled via the HP-IB.

System Power Supplies (SPS) - The SPSs furnish all the operating power required by the DTU. There are four SPSs used by the DTU: +5V, ±20V, and +12V. The +5V power supply provides VCC power to all the logic circuits used in the DTU. The ±20V supplies are used in the voltage reference probe, and the driver comparator circuits. The +12V supply is for controlling the thermal cutoff assembly, which protects the DTU from excessive room ambient heat.

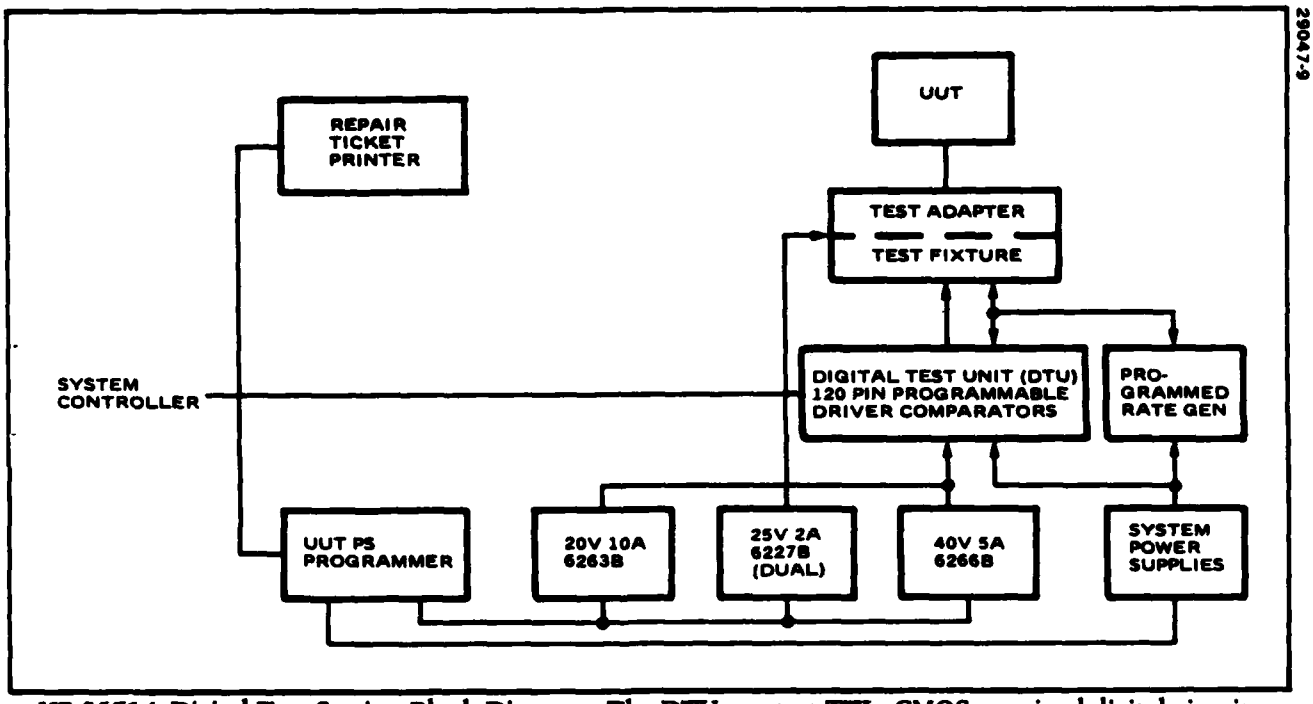
Power Supply Programmer (PSP) - Through software the PSP fully controls the UUT power supplies. It is activated by the proper data command on the HP-IB. The PSP controls the voltage and current settings of the power being supplied to the UUT.

UUT Power Supplies - The DC power to the UUT is provided by four programmable power supplies in the HP 9571A. These supplies are directly controlled by the PSP. Further, they feature high-performance constant-current, constant-voltage operation with built in over voltage protection. The HP power supplies included with the system are:

- 6227B 0-25V, 0-2A Dual Power Supply (two outputs) for low current applications.
- 6263B 0-20V, 0-10A for high current applications.
- 6266B Dual - 0-40V, 0-5A used for D/PCBs containing +28VDC logic families.

Test Fixture/Test Adapter - The test fixture (PN 09570-60018) provides the mechanical holding apparatus for securing the board-under-test and serves as the electrical port through which all test signals pass between UUT and DTU.

Used with the test fixture, the test adapter is specially designed to mate with the test fixture, and each test adapter accepts passive or active circuitry to suit the test requirements of the individual UUT. Together the test fixture and the test adapter form the interface between the UUT and the DTU.



HP 9571A Digital Test Station Block Diagram. The DTU can test TTL, CMOS or mixed digital circuits.

4. DISTRIBUTED SOFTWARE ELEMENTS

A distributed software approach was utilized for the HFI Autoprobe system, which achieved a well balanced system, easily adaptable to other host computer test systems or other testing environments

To achieve a desirable level of universality, without losing sight of the goals of the HFI program, the D/HMA test requirements and the DTS-70 system capabilities were carefully analyzed. This analysis showed that four major software modules, distributed between the DTS-70 and the HMC-2460, would be required to accomplish the host positioning and control task (see figure). The four modules would accomplish:

- Host communications, between HMC-2460 and DTS-70.
- Host interface, DTS-70 FASTRACE to HMC-2460.
- Utilities, for DTS-70 hybrid data base maintenance.
- Command processing, to execute host or operator directed operations on the HMC-2460.

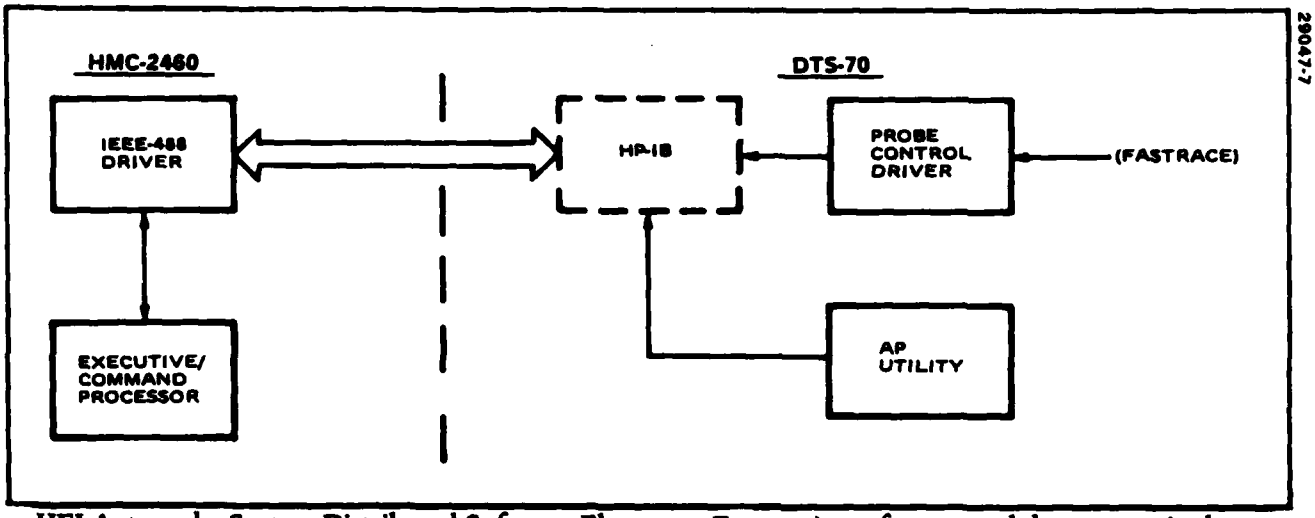
IEEE-488 Driver - The IEEE-488 driver module handles all HMC-2460 data communications to or from the DTS-70. It also is responsible for executing standard IEEE-488 defined bus commands originating from the host computer or system controller. Received data messages are queued for processing by the HMC-2460 command processor. Data messages destined for the host computer are placed in the IEEE-488 output queue for transmission. They are sent when the HMC-2460 is made a "talker" by the host computer or system controller.

Executive/Command Processor - The HMC-2460 Autoprobe operates under the control of the system Executive/Command Processor. The Executive is a round-robin, prioritized, task scheduler. Its primary function is to monitor external events and dispatch them for processing. The defined events are the HMC-2460 AP keyboard input, the host data message input, and the IEEE-488 bus failure. Upon occurrence of any of these events, the appropriate task is activated by the Executive.

The Command Processor is responsible for carrying out all keyboard requests from the operator and execution of commands received from the host computer. As such, it performs the major burden of the work in the AP. The Command Processor, although physically separate from the Executive may be thought of as an extension to the Executive. This is primarily for two reasons : it is significantly larger in size than the Executive, and most of the time is spent in this position of the software.

Probe Control/Driver - The Probe Control Driver is the software interface between the DTS-70 FASTRACE test program and the AP. It is responsible for validating a FASTRACE probe request and translating it into an appropriate sequence of commands to be sent to the AP. The Probe Control Driver also monitors the AP and DTS-70 for error conditions and reports them to the operator via the DTS-70 system console.

AP Utility - The AP utility program is an independent software element designed to perform all the functions required to maintain a hybrid fault node data file on the HP-1000 disc. The hybrid fault node data file contains fault node point identification names and their relative X, Y coordinates on the hybrid. The AP Utility may also be utilized to validate a fault node data file in conjunction with the HMC-2460 AP or to perform remote diagnostic AP testing using the standard AP command set.



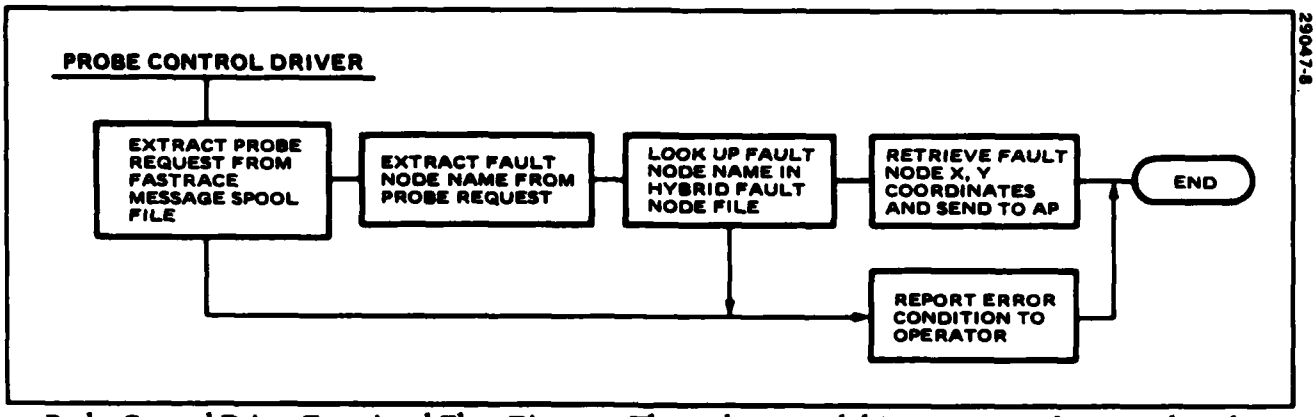
HFI Autoprobe System Distributed Software Elements. Four major software modules are required to accomplish the host positioning control tasks of host communications and interface, utilities for hybrid data base maintenance and command processing.

1. PROBE CONTROL DRIVER (PCD)

The Probe Control Driver software element is the interface between the HMC-2460 Autoprobe and the DTS-70 system with its FASTRACE software.

In order to automate the process of fault node isolation, it was necessary to be able to detect and intercept fault node probe requests issued by FASTRACE to the DTS-70 operator via the DTS-70 console. This was accomplished by utilizing standard RTE-IV operating system functions to determine that FASTRACE was in suspension, waiting for operator response to a fault node probe request. Simultaneously, the fault node probe request information, as issued by FASTRACE, was routed to a special disc spool file for capture by the Probe Control Driver. Once these two events occurred, the Probe Control Driver was activated to complete the probe request cycle.

A functional flowchart of the Probe Control Driver is shown in the figure. The first task the PCD performs is to retrieve and analyze the probe request message from the FASTRACE disc spool file. If the data are not of the appropriate format, an error is reported to the operator. If the probe request message appears correct, the PCD then extracts from the data the name of the fault node point which FASTRACE wants probed. The PCD then performs a linear search of the hybrid fault node file for a name match. If the specified probe point name cannot be found in the file, the error is reported to the operator. If the node name is located in the file, its X, Y coordinate data are retrieved from the file and sent to the AP. The Probe Control Driver then terminates itself.



Probe Control Driver Functional Flow Diagram. The probe control driver is activated to complete the probe request cycle once the fault node request information has been routed to a special disc spool.

2. IMPLEMENTATION TECHNIQUE FOR HYBRID ALIGNMENT

Hybrid alignment is a manual, operator interactive task required to insure Autoprobe touchdown at the appropriate point on the hybrid under test. The task is controlled and initiated by two distributed software elements, one at the DTS-70 and the other at the AP.

Technique - To achieve the goal of being able to probe any point on any hybrid with repeatable accuracy, an alignment technique was required that was:

- Independent of hybrid type and size,
- Independent of hybrid socket location on the AP,
- Able to compensate for hybrid physical size variances, and
- Able to compensate for variations in hybrid X, Y, and θ position when placed in the test socket.

Referring to Figure A, the following is a description of the alignment technique. The outer box represents the travel limits of the probe located on the X, Y stage. The inner box represents the physical area of any hybrid in its adapter socket and may be located anywhere within the X, Y stage travel limits. A and B are two reference points located anywhere on the hybrid. The further the distance between them, the greater the accuracy of point location. Points A and B, and all other node test points, are located (measured) from the hybrid origin at H (0, 0). The origin may be defined anywhere on the hybrid. After the hybrid points are measured and known, coordinate transformation calculations are used to translate the hybrid point coordinates into a derived D, E coordinate system. Thus each hybrid point now has a unique D, E location relative to the alignment points A and B.

To illustrate the process, when A and B are measured, point M is determined which represents the midpoint of the line AB. From there, an arbitrary point Z may be found by expressing its location in terms of a specific value of D and E. The value of D represents a displacement along line AB from M (defining Z'), while E is the displacement along line ZZ' which is orthogonal or perpendicular to line AB. Therefore, once points A and B are physically located within the positioner absolute coordinate system, or X, Y stage travel limits, the AP may find the point Z by specifying its D(z), E(z) coordinates. Having determined the positioner absolute X, Y location of reference points A, B, the transformation calculation process is reversed. This in effect takes all other hybrid point relative D(x), E(x) coordinates and translates them to absolute positioner X, Y coordinates.

Host Alignment Element - The host computer hybrid alignment task is activated only once by the Probe Control Driver, upon the first FASTRACE probe request for every hybrid tested. If the hybrid passes the GO/NOGO test, the alignment task is not activated since no probing is required. A block diagram of the host alignment task is shown in Figure B. Host alignment retrieves the Hybrid A and B coordinates from the fault node point data file and sends them to the AP. The A, B locations were previously "learned" during the fault node file generation, utilizing the AP Utility program. The A, B coordinates are used to sequentially display the two alignment points on the CCTV targeting system, thus avoiding a lengthy operator search to locate them. When the host sends the A and B coordinates to the AP, it then issues a "LOAD" command.

This initiates operator interaction to precisely locate the A, B reference points using the CCTV camera crosshair, jog knobs, and AP keyboard. The operator action indicates acquisition of the reference points in the targeting crosshair.

AP Alignment Element - The AP alignment task receives the A and B reference coordinates from the host computer. When both points are known, the AB

midpoint reference position is calculated for use by the coordinate transformation calculations. The physical alignment task is performed by another element in the Command Processor when the AP receives the "LOAD" command. This merely allows the operator to make any adjustments required, if any, to the real A and B reference point locations.

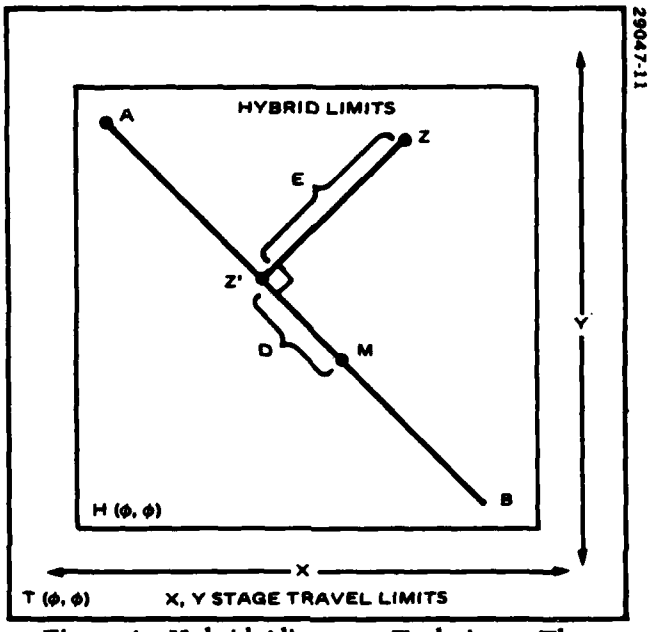


Figure A. Hybrid Alignment Technique. The alignment technique existed in the HMC-2460 software, as part of the wire bonding system prior to its conversion to an autoprobe system.

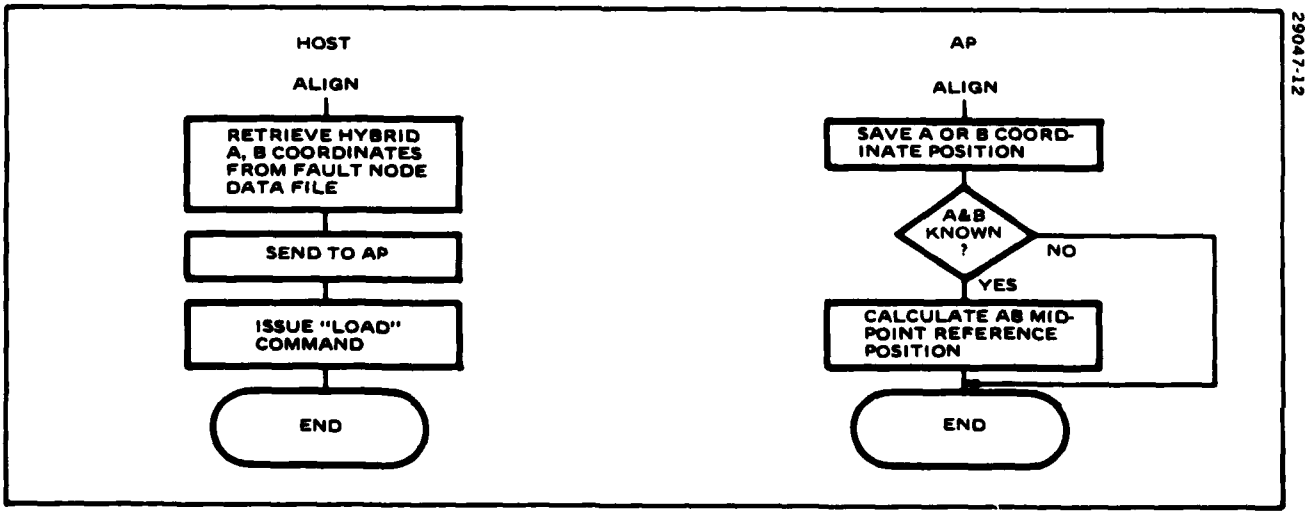


Figure B. Distributed Hybrid Alignment Tasks. The alignment is performed interactively by the operator and the system.

3. EXECUTIVE AND COMMAND PROCESSOR IN THE AUTOPROBE

The AP Executive is responsible for controlling all Autoprobe operations as directed either by the host computer or system operator. The AP Command Processor carries out host computer commands and operator keyboard requests.

Executive - Figure A shows a block diagram of the AP Executive. The executive monitors the AP keyboard, host computer message input queue, and IEEE-488 status. Keyboard input is given highest priority so that the operator may intervene in an emergency or override host computer control.

IEEE-488 bus failure is second in priority. This prevents system hang-up in case of failure during message transmission. If an IEEE-488 error occurs, the system is completely re-initialized. This is due to the high probability of a host system failure as the cause of this error. Recovery must then be made from the DTS-70 which will automatically initiate a new test sequence on the AP.

Host command input is lowest in priority, and when a complete messge has been received by the IEEE-488 driver, the executive activates the command processor task.

Command Processor - Figure B shows a block diagram of the Command Processor. The table below details a list of host commands the AP recognizes. The AP keyboard was designed to closely mimic the functions available through host computer control. Upon receipt of a command or request, the command processor performs a series of validations to ensure error free operation. Any detected errors are appropriately noted and reported. The command or request may then be corrected or AP conditions altered and retried, if desired. If the command or request is successfully validated, the AP performs the associated function. If during execution of the function an error is detected, it is noted and reported. Once the function is complete, the command processor returns control to the AP Executive.

AP-HOST COMMAND LIST

COMMAND	FUNCTION
• MS (up to 32 characters)	- Display a message on the AP display.
• MO	- Set AP operating mode to automatic.
• M1	- Set AP operating mode to manual.
• M2	- Set AP operating mode to test.
• UP	- Raise probe.
• DN	- Lower probe.
• XxxxxxYyyyyy	- Go to table position (X, Y).
• DdddddEeeeee	- Go to hybrid position (D, E).
• HO	- Home the probe.
• AXxxxxxAYyyyyy	- Define reference point A position.
• BXxxxxxBYyyyyy	- Define reference point B position.
• LD	- Load hybrid (physical alignment).
• UL	- Unload hybrid.
• SP	- Send current probe (X, Y) position.
• SD	- Send current probe (D, E) position.
• SE	- Send current error code.
• ??	- Send AP status byte.

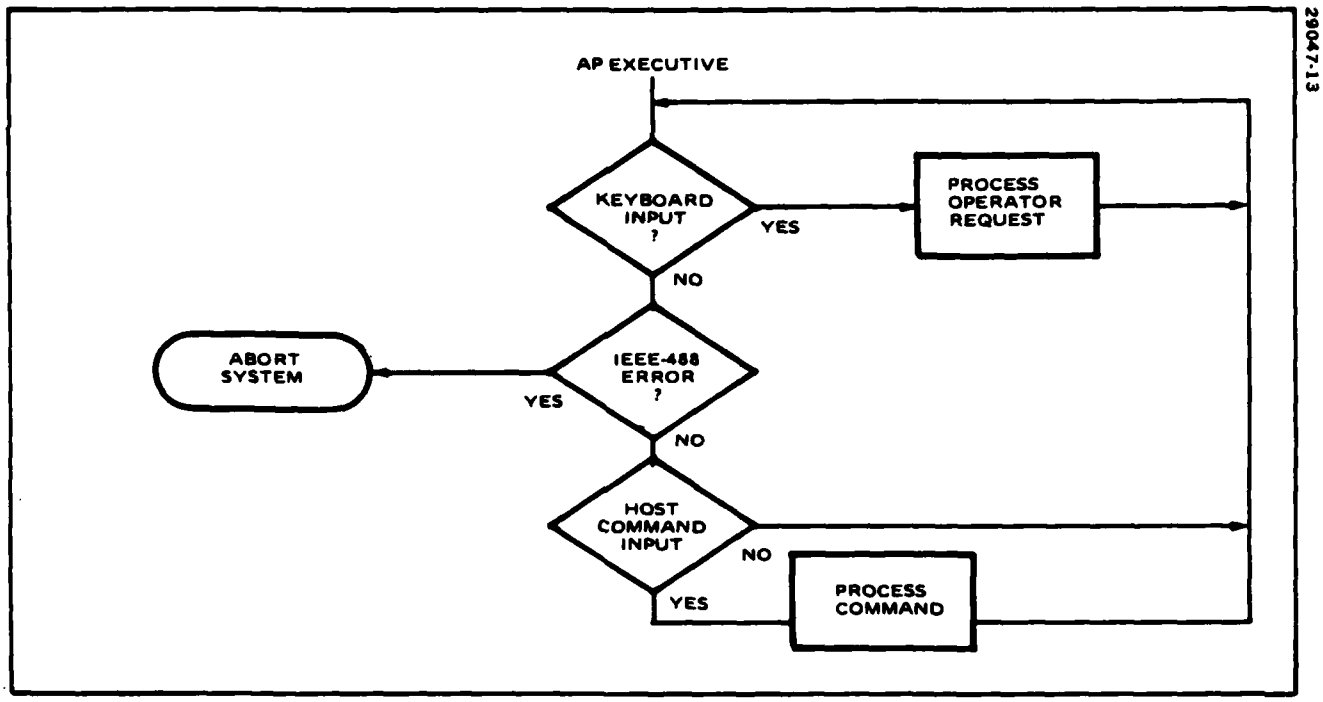


Figure A. AP Executive Block Diagram. The AP executive monitors the status of the IEEE-488 and the host computer message input queue. The highest priority is given to monitoring AP keyboard input so as the operator may intervene in an emergency or override host computer control.

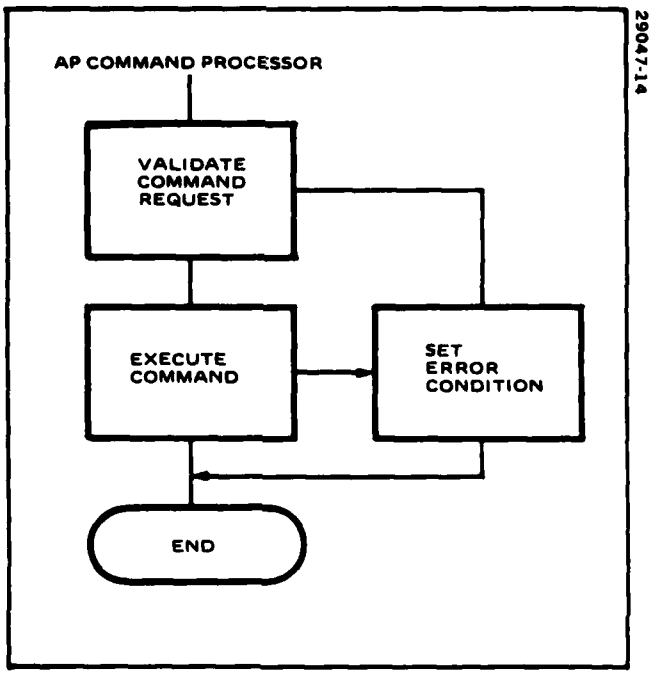


Figure B. Command Processor Block Diagram. Upon receipt of a command or request, the command processor performs a series of validations to ensure error free operation.

4. FUNCTIONS OF THE AUTOPROBE UTILITY

The Autoprobe Utility is designed to effectively maintain any hybrid fault node file and perform remote system diagnostic testing of the HMC-2460 AP, utilizing the standard command set.

The Autoprobe (AP) Utility software can be categorized into five major functions:

- fault node data file creation
- hybrid reference point initialization
- fault node data file review
- hybrid fault node data file edit, and
- AP diagnostic testing.

File Creation - When a new hybrid fault node file is created, certain basic data must be entered or initialized. The operator or test programmer must first specify the number of hybrid node test points to be contained in the file so that adequate disc space may be reserved. Next, the hybrid position of the A, B reference points must be entered. These coordinates are utilized to calculate the A, B line midpoint, M and corresponding D, E relative coordinates. Next, the hybrid node point name and respective hybrid X, Y coordinates are entered. As each X, Y node position is entered, its corresponding D, E value is calculated and placed in the file.

Reference Point Initialization - After the hybrid fault node file is created, the absolute location of the A, B reference points are "learned" from the AP through operator interaction and placed in the file. This is accomplished by placing the hybrid in the test adapter socket mounted on the AP and physically locating each reference point, manually, using the CCTV targeting system. As each point (A or B) is located, its respective X, Y position is read by the AP Utility using the SP command and placed in the node file. For any given hybrid type or part number, the "initial" A, B coordinates are subsequently used to perform the "final" or actual test hybrid alignment task. Because of individual hybrid variances in the test socket, as well as hybrid substrate location variances in its carrier (case), the "initial" A, B coordinates will not, nor can they be, exact on a unit to unit basis. However, they are accurate enough to automatically bring the A or B reference point into view on the TV monitor for "final" targeting by the operator.

File Review - This facility allows viewing of the contents of a specified hybrid fault node data file in an easy to read format at the DTS-70 system console. An optional hardcopy printout may be selected if desired.

File Edit - If an error, or omission occurs during initial creation of a hybrid fault node data file, it may be edited at any time. Capabilities exist to add new fault node points, delete existing fault node points or change existing fault node names or hybrid X, Y coordinates. If new node points are added or their X, Y coordinates are changed, their new D, E coordinates are automatically calculated.

Diagnostics - The AP system can be tested remotely using the AP utility. This feature allows the operator, via a CRT menu, to select any of the available host commands and send them to the AP to verify correct operation of the system. Additionally, the AP utility can be directed to "walk through" a specified hybrid fault node data file. This feature is useful in verifying the contents of the file by verifying each hybrid test node location with the AP CCTV targeting system. As each node location is sent to the AP, the operator may adjust the touchdown point using the X, Y jog knobs on the AP front panel. When the operator has finished, the AP returns the new node location coordinates to the AP Utility. This position is then displayed along with the node file specified position. If differences exist, the file may then be edited for correction.

Section 2 - Work Accomplished
Subsection E - Autoprobe Interface Software Elements

5. DESCRIPTION OF THE IEEE-488 DRIVER

The IEEE-488 driver is responsible for sending and receiving all data execution of IEEE-488 bus commands, and handling of host status requests. The driver consists of a data handling section and a bus command section.

Data Handling Section - The data handling portion of the IEEE-488 driver is sub-divided into 2 areas: data input and data output. Although data transfers occur a byte at a time to and from the bus, the driver is organized as a data message handler. Messages can consist of any number of characters and are complete only if properly terminated. It is the data sender's responsibility to properly terminate the message and the data receiver's responsibility to verify such. On data input, received characters are placed in an input buffer queue. When the message terminator is detected, a message count is incremented, signifying to the AP executive that a host command has been received. The one exception to this is if the host message happens to be a status request (??). In this instance, the IEEE-488 driver queues up a status message for immediate transmission to the host. This allows the host system to monitor AP operations while it is busy performing other tasks.

Bus Command Section - The bus command section of the IEEE-488 driver handles the pre-defined bus commands that are issued by the system controller (HP-1000). These messages are: Remote/Local, Serial Poll, and Device Clear. The Remote/Local commands have no purpose for the Autoprobe System and basically are ignored. The Serial Poll feature was never implemented, but basically performs the same function as the host status request (??). The Device Clear command will cause the AP to re-initialize itself. Any other unrecognized command will cause the driver to set an appropriate error code that will be analyzed by the AP executive for appropriate action.

1. D/HMA TEST CANDIDATE

The 3178069 D/HMA is a digital hybrid circuit chosen to minimize test software generation. This allowed the maximum project effort to be devoted toward developing the AP interface software and the accurate, repeatable microcircuit test probing.

The test candidate is a component found in the Intensity-Compensation and Gating Circuit Card Assembly (CCA), 3177045. This CCA is required in the naval display systems found in Project SID (Standard Information Display). The display systems of Project SID are part of our defense radar systems.

The 3178069 D/HMA is a leading-trailing edge delay hybrid microcircuit. The hardware characteristics are shown in the table below. The D/HMA test candidate is a thin film hybrid with a 22-pin flatpack header. It has a +5Vdc, 100-mA power requirement and contains these logic devices (or elements):

- 74S00 - Quadruple 2-input Nand Gates
- 74S04 - Hex Inverters
- 2N2369A - NPN High Speed Switching Transistor

To achieve 5 logic levels input to output, the D/HMA test candidate with 20 active I/O pins was reconfigured through the test adapter to 8 active I/O pins.

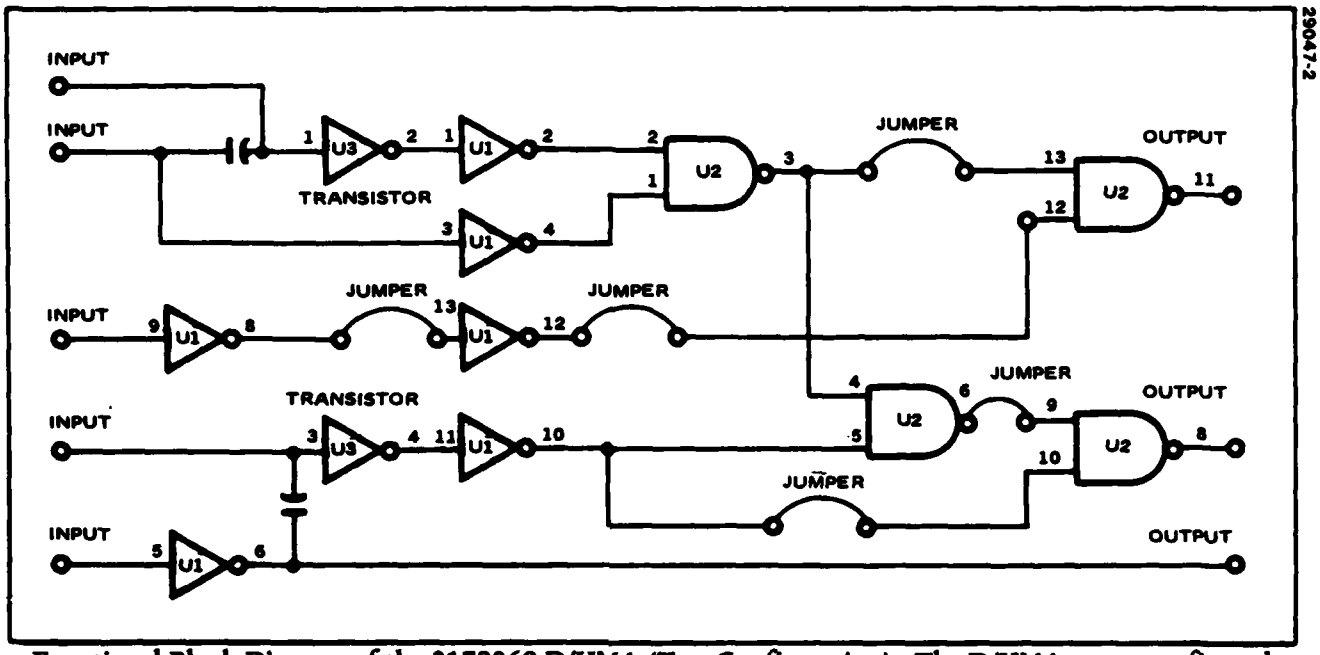
The reconfigured test candidate is functionally depicted in the figure opposite. It shows that some of the logic outputs have been connected to logic inputs through adapter jumpers. In this circuit configuration, the DTS-70 must backtrace (or probe) through additional logic levels (a maximum of 5) to locate a fault at node U1.3 (U1 pin 3). The maximum logic level probing sequence for U1.3 would follow the node path

U2.8
↓
U2.6
↓
U2.3
↓
U1.4
↓
U1.3

before isolating a fault at that node. By reconfiguring the test candidate, there is an increase in the number of probes during fault isolation. The added probes provide a more effective exercise for the AP hardware and software.

3178069 D/HMA HARDWARE CHARACTERISTICS

ITEM	QUANTITY
Hybrid Technology - Thinfilm	NA
Header Type - 22 pin flatpack	1
Power Supply, +5VDC; 100 MA	1
IC Logic - 74S00	1
IC Logic - 74S04	1
Transistor - 2N2369A	2
I/O Pins (actual)	20
I/O Pins (Test configuration)	8



Functional Block Diagram of the 3178069 D/HMA (Test Configuration). The D/HMA was reconfigured to provide a more effective test exercise for AP hardware and software.

2. D/HMA TEST ADAPTER/FIXTURE

The Test Adapter and Test Fixture add electrical features to the test candidate to fully exercise the capabilities of the AP.

The Test Adapter and Test Fixture are shown in Figure A. The Test Fixture is the electro-mechanical interface to the DTS-70. It provides pin-to-pin interconnections between the DTS-70 and the Test Adapter. The Test Adapter adds additional logic (or circuitry) required to protect the test candidate, to interconnect the logic stages of the D/HMA test candidate (3178069), and to provide nondestructive SA1, SA0 node faults through switch selectors.

The simplified electrical functions of the Test Adapter/Test Fixture are shown in Figure B.

Input Circuit - The input circuit, at the very top of Figure B, provides the electrical connection between the DTS-70 driver and the D/HMA input pin. It also has a switch circuit used to introduce a selectable SA1 or SA0 circuit fault at the D/HMA. When the switch is in the up position, the D/HMA input is held high by a pullup resistor (SA1 fault). When the switch is in the down position, the input pin is tied to ground (SA0 fault). When the switch is in the center position, the DTS-70 driver is connected directly to the D/HMA input pin. The SA1, SA0 switches were used during the Industry Demonstration for creating circuit faults which the AP proceeded to locate. In addition, the Test Adapter circuit provides testpoints (TPs) for signal monitoring.

Output Circuit - The output circuit, second from the top in Figure B, provides the electrical interface between the D/HMA output pin and the DTS-70 comparator. This circuit contains a 74S241 line driver and receiver to eliminate any transmission line problems which could result from the 10 feet of ribbon cable connecting the Test Adapter to the Test Fixture.

Transistor Switch Circuit - The transistor switch circuit consists of a two-position switch tied into the base of the test hybrid transistor. The switch is used to produce a SA1 fault at the transistor circuit. When the switch is in the down position, the transistor base is pulled to ground, and the transistor collector is forced to a high state (SA1). When the switch is in the up position, the transistor circuit operates normally. This circuit also contains monitoring TPs.

Jumper Circuit - The jumper circuit is the adapter jumper described in the preceding topic. It connects a D/HMA output pin with an input pin. Its purpose is to increase the test circuit complexity and provide a better test demonstration for the AP. TPs are also found on the circuit.

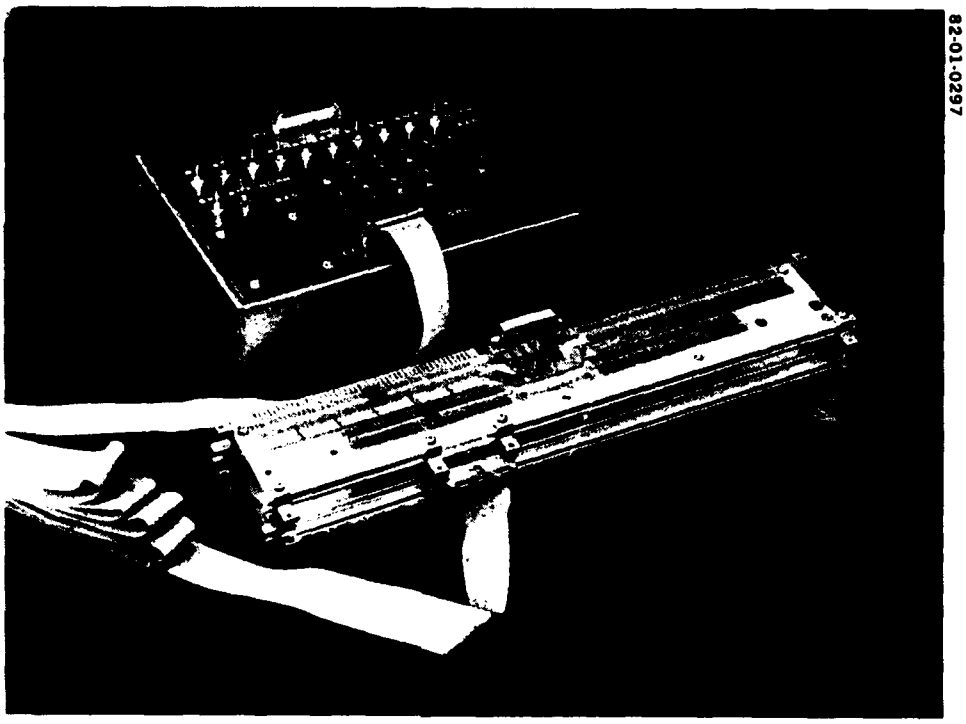


Figure A. 3178069 Test Adapter/Test Fixture. The Test Adapter/ *Test Fixture is the electro-mechanical interface to the DTS-70.*

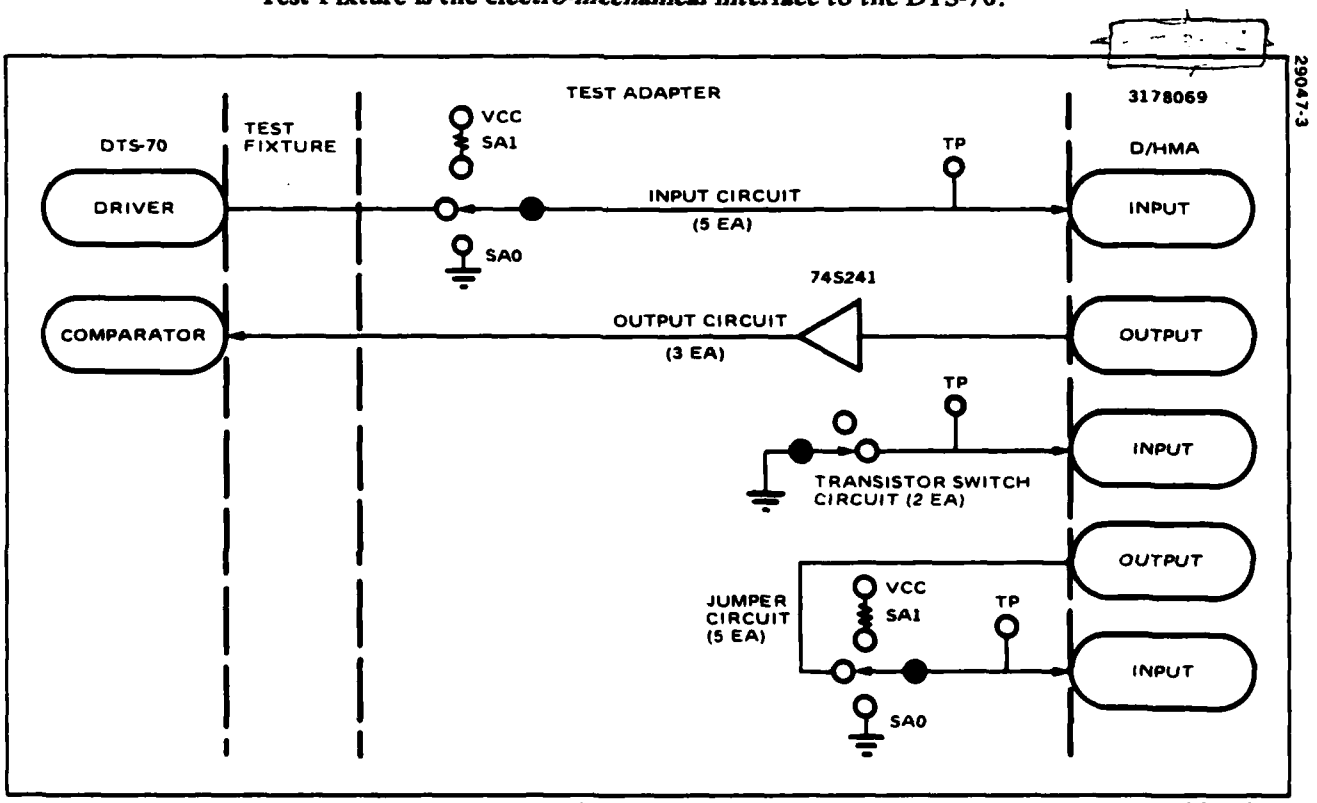


Figure B. Test Adapter/Test Fixture Functional Block Diagram. The Test Adapter/Test Fixture adds additional logic to the test candidate.

1. D/HMA HOST TESTAID/FASTRACE

The development of the simple D/HMA test software was easily accomplished through the use of the host DTS-70 digital test software package, TESTAID/FASTRACE.

The Hewlett-Packard DTS-70 Digital Test Software is comprised of two software packages, TESTAID III and FASTRACE III. TESTAID, which is made up of four main programs, can be used to both manually and automatically generate test patterns for fault isolation while simultaneously keeping track of the percent of fault detection. TESTAID generates simulator-based test programs for digital electronic assemblies. FASTRACE executes the test programs created by TESTAID on the UUT. It performs pass, fail testing and computer-guided probing if a failure is found. The figure shows the Test System Software Structure.

TESTAID is made up of the following four main programs.

SGLST - This program is concerned with topology generation. It initializes the statefile (disc working area) and stores into it the user created source file that represents the UUT topology. In addition, SGLST checks this source file for the correct syntax and completeness. If logic models are specified in the source file, the program will append the appropriate logic model to the statefile. These logic models are either user created, if complex or special, or they exist in the TESTAID Device Library.

SMSET - This program generates the Fault Directory which contains the fault data used by program SIMUL to produce fault machines. Fault machines are software models of the UUT circuit faults.

SIMUL - Program SIMUL is the simulator and the test pattern generator. It uses the UUT topology model created by the previous programs to simulate the logical behavior of the actual UUT circuit in response to input test patterns. The test patterns are chosen such that they will reveal at the UUT outputs the faults defined by the Fault Directory. Test pattern generation can be accomplished manually by the user or by the SIMUL automatic pattern generation, PGEN. When a fault is detected, the fault and the fault response are stored in the statefile. Detected faults are automatically removed from the Fault Directory and the percentage of the faults currently detected is maintained.

PATDK - This is the TESTAID post processor program. It uses selected information from the statefile and creates the Preliminary Test File for FASTRACE.

FASTRACE is composed of five main programs as discussed below.

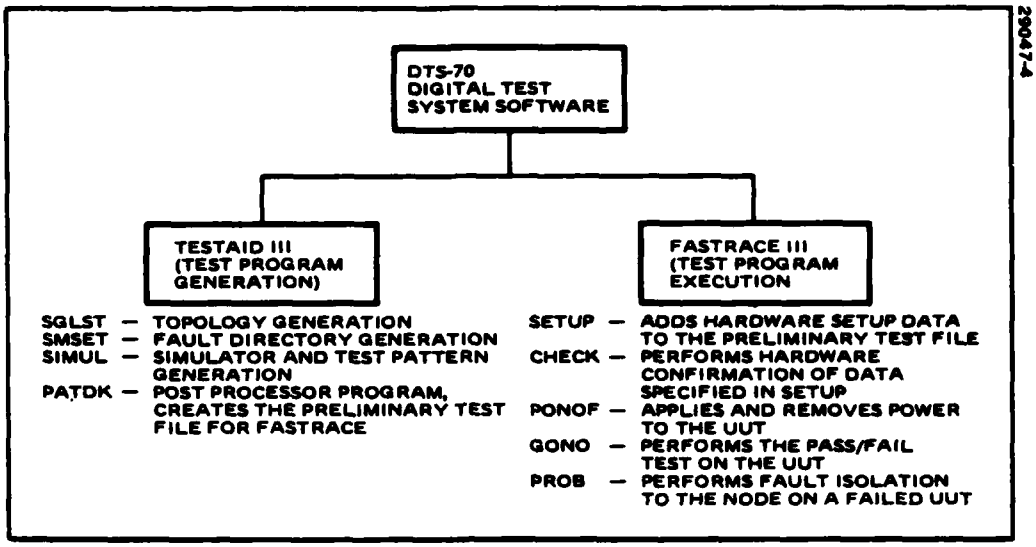
SETUP - This program adds hardware setup data to the Preliminary Test File. Such data consists of the test station's digital test unit card configuration, the UUT test adapter number, the power supply parameters, and the reference voltages for the programmable driver, comparator cards. Once processed by SETUP, the Preliminary Test File becomes the Fastrace Statefile.

CHECK - This program performs the hardware confirmation of values specified in SETUP.

PONOF - This program applies and removes the power to the UUT.

GONO - This program performs the pass, fail test on the UUT. It uses test stimulus and response patterns created by TESTAID to apply GO/NOGO tests to the UUT.

PROBE - This program performs fault isolation to the node level on a failed UUT. When the user calls the BACKTRACE command, PROBE directs the test probing sequence, node by node, until the fault is identified, displayed, and printed out.



DTS-70 Digital Test System Software Structure. TESTAID supplies simulator-based test program generation for digital circuits. FASTRACE provides the test program executive for UUTs.

2. D/HMA TEST METHOD

The 3178069 test software, based entirely on TESTAID/FASTRACE, executes the complete UUT test with a 94-percent test comprehensiveness.

The test method required to generate the digital test program for the D/HMA was the direct application of the TESTAID/FASTRACE software. All the logic devices found in the test candidate were readily available in the TESTAID Device Library and, therefore, no device modeling was necessary. Since no device models had to be created, the D/HMA test program required a minimum of effort to complete.

The transistors found in the test candidate were modeled by considering them to be inverters. As can be seen from the figure, a TTL high at the base input of the transistor would produce a TTL low at the collector output. This behavior is identical to the behavior of a standard inverter and, thus, the transistor circuits were modeled as such. The transistors were modeled as inverters found in the 74S04 IC package (hex inverters).

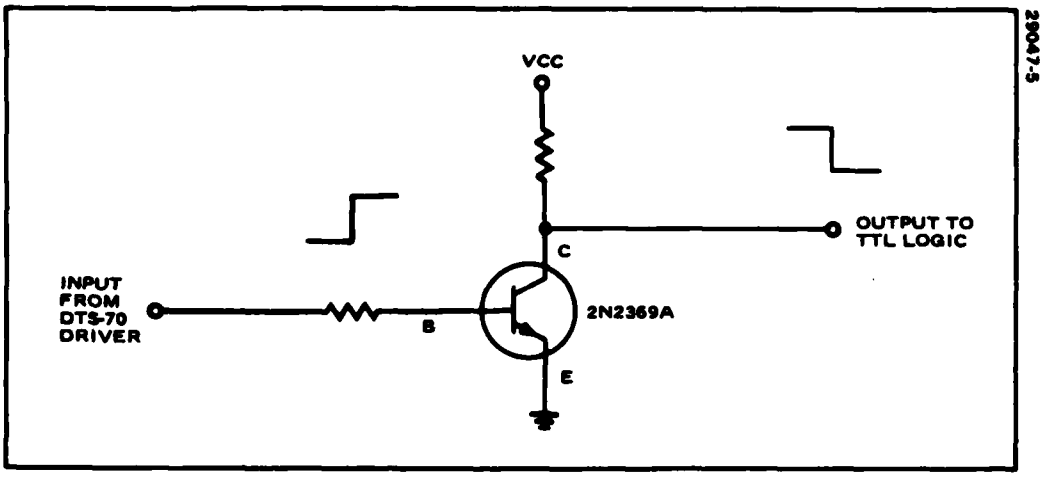
The test pattern generation was completed using the DTS-70 supplied automatic pattern generator, PGEN. PGEN generated 11 test patterns for a 94-percent fault detection. There was 1 fault out of 18 which was undetectable from any test circuit output pin. The 94-percent fault detection was acceptable, since the primary goal of the HFI project was to demonstrate the AP, rather than the DTS-70's fault isolation capabilities. The table shows the Test Software Parameter Breakdown for the 3178069 test circuit. SGLST required 42 program statements (lines) to create the topological model of the test candidate. In the case of SMSET, it calculated that the total number of possible faults which needed detecting by the simulator was 18. A total of 11 input test patterns was generated in program SIMUL to test the 3178069 D/HMA to the 94-percent fault detection level. Program PATDK required five statements to create the Preliminary Test File. SETUP required 20 lines to completely define the hardware setup for the DTU.

To illustrate the testing of the D/HMA, here is a typical hybrid test scenario:

(1) The test operator activates the appropriate hybrid test program at the host system console.
(2) The operator is then instructed to load the hybrid UUT into the AP hybrid socket.
(3) The DTS-70 then executes a GO/NO-GO test (program GONO) on the UUT with the AP in standby.
(4) If the UUT passes the GO/NO-GO test, the operator can test another UUT of the same type or exit the hybrid test program.
(5) If the UUT fails the GO/NO-GO test, the Host Alignment procedure discussed in Topic 2.E.2 will be performed.
(6) The DTS-70 then performs fault isolation testing (program PROB) to the node directing the AP to the probe locations.
(7) After AP completes fault isolation, the operator can test another UUT of the same type or exit the hybrid test program.

TEST SOFTWARE PARAMETER BREAKDOWN

Program Name	Parameter	Number
SGLST	STATEMENTS	42
SMSET	FAULTS	18
SIMUL	PATTERNS	11
PATDK	STATEMENTS	5
SETUP	STATEMENTS	20



Transistor Circuit. The transistor was modeled as an inverter.

1. POSITIONING ACCURACY AND PROBE CONTACT RESULTS

An X, Y Positioning Accuracy Test and a Probe Contact Test were performed to prove that the Z-stage and CCTV camera could be mounted on the X-Y table and that the HMC-2460's ultrasonic sensor could be used for touchdown detection.

During the AP implementation, two major questions arose which greatly concerned the mechanical engineers:

- How much load will the X-Y table handle before positioning accuracy would be affected, and
- What damage is done to the hybrid circuit pads during the ultrasonic probe touchdown?

To address these two questions, the X-Y Table Positioning Accuracy Test and the Probe Touchdown Test were performed.

The X-Y Table Positioning Accuracy Test was required because, for the AP application, the Z-stage and the CCTV camera would have to be mounted onto the X-Y stage. The purpose for the Z-stage and camera relocation is explained in Topic 2.C.2. The Z-stage and camera weights were 7 and 7.5 pounds, respectively. To test the positioning accuracy of the X-Y table, a weight approximately 14 pounds was mounted onto the X-Y table and then the 4-position test was executed. The 4-position test is an HMC-2460 self-diagnostic test. In this test, the HMC 2460 learns with the CCTV monitor electronic crosshair four X-Y reference coordinates, and these coordinates are tracked continuously for a user specified number of cycles. The whole process is operator viewed on the CCTV monitor. By observing the electronic crosshairs relationship to the X-Y reference coordinates, the positioning accuracy of the X-Y table can be determined. The 4-position test was executed with the added weight on the X-Y table for 50 cycles. There was no observable change in the positional accuracy of the X-Y table with the added 14 pounds.

The Probe Contact Test was performed on an actual hybrid circuit pad. A total of 200 probe touchdowns was executed on a single point on the pad and the pad was then observed on the CCTV monitor for noticeable damage. There was some apparent damage to the pad after the 200 touchdowns but it was minimal, and did not affect circuit operations. When a single touchdown was performed on a new pad, no damage to the pad surface could be detected.

The table shows the results of the X, Y Positioning Accuracy Test and the Probe Contact Test.

X, Y POSITIONING ACCURACY TEST AND THE PROBE CONTACT TEST RESULTS

Test	Number of Operations	Results
X, Y Positioning Accuracy	50	No change in accuracy
PROBE Contact	200	Minimal damage
PROBE Contact	1	No damage

2. D/HMA TEST TIME FOR HW/SW AND PROBING

The simple D/HMA test candidate minimized test HW/SW development time while providing measured autoprobe fault isolation time data for preselected test adapter SA0, SA1 circuit faults.

The 3178069 D/HMA Test Hardware/Software Development Summary is shown in Table I. This summary gives the labor hours involved in accomplishing the following tasks.

Topology Design and Edit - This task represents the time required to create the source code file containing the topological model of the test candidate.

Test Program Generation - This task represents the time required to prepare for the execution and the running of TESTAID programs SGLST, SMSET, SIMUL, and PATDK.

Hardware Design and Fabrication - This task represents the time required to design and fabricate the Test Adapter/Fixture, the DTS-70 probe to capillary probe interface, and the test candidate large-scale breadboard using discrete solid state devices.

Hardware Verification - This task represents the time required to prepare for execution and the running of the FASTRACE programs SETUP, CHECK, PONOF, GONO, and PROB. The total time required to develop the test hardware and software was 83 hours.

Table II is the Autoprobe Fault Isolation Time Data taken during test verification. It represents the length of time it took the AP System to isolate selected test adapter faults (SA0 and SA1) within the 3178069 D/HMA circuit nodes.

A summary of the HFI Autoprobe 3178069 Test and Fault Isolation performance data is as follows:

GO/NO-GO Test - This is the time it takes to execute a go/no-go test on the test candidate. This test had an execution time of 5 seconds.

Digital Fault Isolation - This represents the range of the measured values in Table II, the times required for the AP to isolate SA0 and SA1 faults. The time range was $0.68 < t < 2.25$ minutes.

Probe Time - This represents the range of the measured time between successive probes by the AP during fault isolation. The time range was $8.5 < t < 9.8$ seconds.

TABLE I. D/HMA TEST HARDWARE/SOFTWARE DEVELOPMENT TIME SUMMARY

Item	Total Labor Hours
Topology Design and Edit	16
Test Program Generation	3
Hardware Design and Fabrication	40
Hardware Verification	24
Total	83

TABLE II. MEASURED AUTOPROBE FAULT ISOLATION TIME DATA FOR THE D/HMA TEST CANDIDATE (3178069)

Fault Type - SA0 Node Name	Probe Time Minutes	Fault Type - SA1 Node Name	Probe Time Minutes
U1.9	1.5	U1.9	1.5
U4.2	2.25	U4.2	2.25
U1.3	1.5	U1.3	1.5
U5.2	1.67	U5.2	1.65
U1.5	0.68	U1.5	0.68
U2.12	1.08	U2.12	1.05
U2.13	1.01	U2.13	1.13
U2.9	1.47	U2.9	1.47
U2.10	0.92	U2.10	0.95
U1.13	1.45	U1.13	1.45
U3.3	1.48		
U3.1	2.07		

3. AUTOPROBE INTERFACE OVERHEAD SOFTWARE

There is significant loss in system efficiency due to the nature of the host ATE FASTRACE probe request data intercept technique.

Although the Autoprobe timings show a significant increase in throughput over standard manual probing methods, a significant portion of the fault isolation (probing) time is lost in HP-1000 operating system overhead. This loss can be attributed to two areas, one in the FASTRACE intercept technique itself (causing the Probe Control Driver to be activated) and the other in the fault node name lookup technique utilized by the Probe Control Driver. Of the two, the data intercept phase is the most detrimental.

Table I shows the average time required to determine that FASTRACE was suspended because it had just issued a probe request. The difference between the OLD and the NEW method was that the NEW method involved combining all DTS-70 software elements into single program load module rather than letting each element stand alone as an individual program module. As can be seen, this provided very little improvement. The average time then, is approximately 2.5 seconds for the Probe Control Driver to be activated once FASTRACE issues a probe request.

Once the Probe Control Driver is activated, it then validates the probe request and looks up the fault node name in the hybrid fault node data file. Table II shows average search times for this file. These times include file open and close functions. U1.1 is the third record in the file, U2.5 is the nineteenth record in the file and U.22 is file record thirty-eight. The data of Table II are plotted in the figure to reveal the hybrid fault node search time contribution to overhead. At record number 0, the line vertical intercept shows about 1.1 seconds time contributed to overhead for the hybrid fault node data file Open/Close process.

Extrapolating this data and applying it to the additional functions the Probe Control Driver must perform with the spool file utilized to intercept the actual FASTRACE probe request, there is estimated to be 1.5 to 2.5 seconds additional overhead for FASTRACE message spool file manipulation.

An estimate of the total DTS-70 ATE system overhead can now be made by summing respective overhead time contributed by operations with: hybrid fault node data file; FASTRACE message intercept (probe data) spool file; and FASTRACE suspend detection (about 1.5 seconds).

The three factors combined above contribute from 5.1 to 6.1 seconds time that is attributed to the DTS-70 ATE system overhead. It should be noted this overhead occurs for every point probed! These times should therefore be subtracted from the probe test time results for a more realistic evaluation of the capabilities of the HFI Autoprobe System.

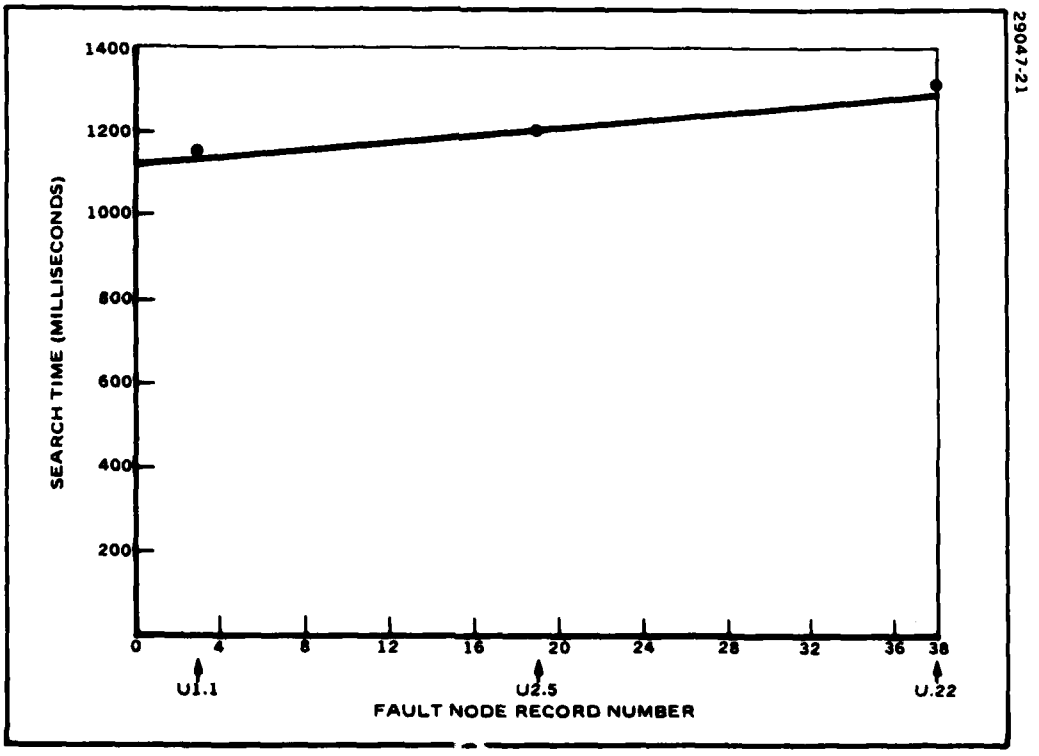
This FASTRACE probe request intercept technique was the only one HP would recommend or support for the DTS-70 system. No other alternatives were made available.

TABLE I. FASTRACE SUSPEND AND DETECT TIMES, IN MILLISECONDS

	OLD	NEW
	2520	2470
	2500	2490
	2480	2490
	2580	2490
	2500	2480
	2500	2490
	2520	2490
	2500	2490
	2500	2490
	2510	2490
	2500	2490
	2520	2490
	2530	2490
	2540	2510
	2490	2510
	2520	2510
	2480	2510
avg	2511	2493

TABLE II. HYBRID FAULT NODE FILE SEARCH TIMES, IN MILLISECONDS

FILE	SEARCH	TIME
	U1.1	U2.5	U.22
	1160	1200	1300
	1148	1200	1300
	1152	1200	1300
	1148	1200	1300
	1160	1200	1300
	1148	1200	1300
	1152	1200	1300
	1150	1200	1300
	1150	1200	1300
	1150	1200	1300
avg	1151	1200	1300



Hybrid Fault Node File Search Time versus Record Number. This time contributes to probe step total overhead time, and specifically applies to the DTS-70 ATE system.

4. INDUSTRY DEMONSTRATION

Guest visitors to the Hughes Industry Demonstration participated in an expository conference, of the Autoprobe system HW, SW and D/HMA test candidate, that proved the HFI program objectives by systematic examples.

The Industry Demonstration (ID) conference for the Autoprobe (AP) system HW, SW and D/HMA test candidate exemplified the HFI program objectives:

- Production D/HMA test requirements
- Single test probe under host or ATE control
- AP system HW, SW compatible with the DTS-70 ATE
- Actual test and fault isolation of a D/HMA.

As a supplement to CDRL 004, the ID plan was submitted to the MICOM project office in December 1981, complete with an abstract, guest invitations, and information.

Hughes-Irvine provided the ID conference facilities where the AP system and DTS-70 ATE were integrated. Cooperation by the U.S. Navy, in their concurrent SVS production project, authorized their DTS-70 Acceptance Test Station for use in the HFI program.

Two separate ID conferences, held in January and February 1982, were attended by a total of 44 guests directly concerned with D/HMA testing and the AP system applications. The visitors were members of the Government, industry, and Hughes entities (see table). In the January conference, 17 members of Hughes management, engineering, and supervision attended, representing the microelectronic divisions at Fullerton and Newport Beach. There were 27 visitors at the February conference representing all participants and other Hughes divisions, except Newport Beach. The objectives and technical details of the AP system and DTS-70 HW, SW were discussed in a 3 hour period, and one additional hour was devoted to the D/HMA test demonstration.

The ID conference generated an active interest in further product development and future applications of the AP system. This interest was expressed by several visitors, both in and outside of Hughes, to fulfill the needs of production hybrid testing, both digital and analog types.

Several important questions asked by visitors and answered during the technical discussions (as well as this report) pertained to the following items:

- Single AP versus fixed multiprobe with moveable UUT and multiconductor cable.
- SW method of X, Y, θ D/HMA relative coordinate alignment to positioner absolute X, Y coordinates.
- D/HMA surface or topographical variance and test probe touchdown control.
- Tungsten probe tip design and contact resistance.
- General application and transportability of the AP Interface SW.
- Per unit test probing time contributed by the host ATE SW overhead, and AP system probing time.
- DTS-70 FASTRACE SW fault node data intercept method (spooling) and improved techniques.

Following a functional GO/NOGO D/HMA test demonstration, visitors were asked to introduce SA0, SA1 type faults readily selected by switches at the test adapter. Selected faults were accurately and reliably isolated by the AP system with speed limited primarily by SW rather than mechanical reaction time.

In general visitors expressed approval of the Hughes ID conference for the AP system and D/HMA test, in meeting the HFI program objectives.

GUEST PARTICIPANTS IN THE HUGHES INDUSTRY DEMONSTRATION OF THE AUTOPROBE SYSTEM

Name	Location
Aerojet Electrosystems	- Azusa, CA
BDM Corporation	- Albuquerque, NM
General Dynamics	- Pomona, CA
Hartman Associates	- Woodland Hills, CA
Hewlett Packard	- Fullerton, CA
Hughes Aircraft Company	- Canoga Park, CA
	- Carlsbad, CA
	- El Segundo, CA
	- Fullerton, CA
	- Inglewood, CA
	- Irvine, CA
	- Newport Beach, CA
	- Tucson, AZ
Naval Avionics Center	- Indianapolis, IN
Teledyne Microelectronics	- Los Angeles, CA
TRW Systems	- Redondo Beach, CA
US Army Missile Command	- Redstone Arsenal, AL

SECTION 3
REMARKS AND RECOMMENDATIONS

Section 3 - Remarks and Recommendations

1. RECOMMENDATIONS CONCERNING THE CCTV CAMERA, PROBE, AND AP INTERFACE SOFTWARE

Development of a production Autoprobe would benefit from use of a fiberoptic scope and lens system, and of an optimized ultrasonic touchdown sensing system. Test rate improvement should be sought through changes in host ATE probe fault data intercept software, and in the D/HMA automatic recognition and X, Y alignment technique.

CCTV Camera - One reason for implementing a fiberoptic image scope and lens system with the CCTV camera assembly is to reduce the load on the X, Y table. The present weight of the camera assembly is 7.5 pounds, and by removing this weight from the X, Y table, the mechanical life of the table would be prolonged. With fiberoptics, the CCTV camera assembly would be completely supported by the AP mainframe, and only a lightweight fiberoptic lens and cable assembly would be mounted to the X, Y table.

The second reason in support of fiberoptics is that the constant stop and go motion of the X, Y table will eventually cause the video interface cable between the camera and the video generator to wear out. The constant vibrations to the camera due to the rapid X, Y table motion could also affect the longterm life of the camera.

Probe - The ultrasonic touchdown sensing system consists of the ultrasonic transducer, the ultrasonic generator, and the ceramic capillary probe. The ultrasonic transducer converts electrical energy into an ultrasonic mechanical vibration. The ultrasonic generator provides the varying electrical power levels that drive the transducer, and it also has sensing circuitry which detects the probe touchdown. The ceramic capillary probe propagates the ultrasonic energy to the UUT surface and also provides the electrical interface between the UUT and the host backtrace probe. For a production application, the optimum energy level supplied to the transducer must be determined so that there is minimal damage to the UUT surface while still providing consistent operation of the touchdown sensing. An alternative approach to the ceramic probe design is to use a tungsten-carbide capillary in the probe design. This could prove to be a viable approach for the production system probe design.

AP Interface Software - The most important candidates for improvement, to increase the effective hybrid test rate for the HFI Autoprobe System, are the host ATE probe fault data intercept software and the D/HMA automatic recognition and X, Y alignment technique utilized.

As detailed in Topic 2.H.3, the technique of intercepting a FASTRACE probe request via a spool file contributes significantly to the overhead of the Autoprobe system. Ideally, the optimum method would be to have FASTRACE issue probe requests directly to the AP. There is no reason not to expect to be able to do this provided that the host ATE supplier would actively support this effort.

Although it is not as significant as the intercept overhead, time is lost in the Probe Control Driver for fault node name lookup in the hybrid fault node data file. This file could be modified to be memory resident in either the HP-1000 or the AP. If stored in the AP, the file could initially be loaded into memory from the flexible disc or downloaded from the host computer. The AP RAM memory could hold approximately 2000 test points.

AUTOPROBE AND INTERFACE SOFTWARE IMPROVEMENTS

Item	Proposed Improvement	Resultant Advantage
CCTV Camera	Targeting - Fiberoptic Image Scope. Fixed camera mounting to AP mainframe.	- Remove 7.5 pound mass of camera assembly from X, Y stage. - Increase X, Y stage drive mechanism and camera life.
Probe Touchdown Sensor	Optimize test probe tip and ultrasonic sensing design.	- Minimize incidental damage to hybrid UUT.
AP Interface SW		
• FASTRACE Probe Data Intercept	- Provide AP control through direct exit or reentry of FASTRACE or other host ATE probe backtrace SW.	- Increase test throughput by reducing time per probe step contributed by host ATE SW overhead.
• Fault Node File	- Host or AP memory resident hybrid UUT fault node X, Y coordinate data storage.	- Reduce SW overhead for node coordinate look up time.

2. AUTOPROBE APPLICATION TO PRODUCTION D/HMA TEST

A Production version Autoprobe system delivering high test throughput can be achieved through addition of proven hardware and software, which will provide D/HMA handling, recognition and alignment, and controlled temperature testing.

As outlined in Topic 1-2, the engineering model Autoprobe system can achieve full production test capability by skilled design and addition of hardware and software to provide:

- Automatic D/HMA handling and multiple socket test fixture equipment.
- Localized D/HMA and test probe chamber, and temperature control equipment for parametric functional tests -55°C to +100°C.
- Automatic D/HMA recognition and X, Y alignment SW.

The Hughes, Tucson production D/HMA test throughput has an initial objective of completing 5000 units per month or greater.

Equipment and software above for the production AP system can be realized by present technology with low technical risk. Part of the AP proposed improvements are summarized in the accompanying table. By a cursory estimate, a 12 to 18 month period can provide appropriate design, fabrication, and test evaluation of one prototype equipment and software, to assure reliable operation at the required throughput rates.

The Hughes-Tucson production group has already designed a D/HMA handler that has been tested and is presently operational. Further design and test evaluation of the D/HMA test sockets and fixtures, test probe, localized temperature chamber, and temperature control equipment are due to follow within the master production plan.

The third item of automatic D/HMA alignment has been developed and is currently available in one form through the Hughes-Carlsbad wirebonder group. The Carlsbad technique utilizes the CCTV camera and video processor (to scan, digitize, and correlate) plus the flexible disc storage and software to provide automatic D/HMA alignment. This entire process requires about 0.15 seconds.

An alternative technique, proposed by Hughes-Tucson, is to use a Three Reference point Edge Sensing method, under computer control, to provide automatic D/HMA alignment. This technique relies on software to measure circuit trace continuity to an edge pin (D/HMA) and by iterative process determines the trace position to carry out D/HMA alignment. The ultimate alignment method used whether video/SW or SW-only depends on realizable long term economic benefits.

Automatic hybrid recognition can be accomplished by the addition of hybrid markings or bar code, developing related software and providing ATE memory storage.

Hybrid test experience at Hughes-Tucson indicates that 47% of units pass the first time through. Hughes-Canoga Park test results indicate 75% of failures are temperature related and 25% are dynamic (at speed) test related. This experiece is indicative of present yields as well as dominant failure class.

Autoprobe temperature tests of a D/HMA affect environmental equipment design, but are otherwise straightforward. Autoprobe dynamic D/HMA tests, however, affect the ATE system or test adapter operating capability.

Dynamic testing of microprocessor type D/HMAs at speed can be direclty accomplished by such ATE systems as: Instrumentation Engineering-IE 390, 10 megahertz at I/O pin; Hewlett Packard-3060A, 2 megahertz at I/O pin; and Tektronix-S 3260, 20 megahertz at I/O pin. A future increase in D/HMA operating speed, however, can cause an apparent "obsolete" condition even with the ATE systems identified. In that situation the ATE system would either be replaced with a

higher speed and costlier system, or the D/HMA test adapter could furnish the increased testing speed, operating with the original ATE system. One form of this test adapter dynamic assist to the ATE system was described at the end of Topic 2.A.1.

By incorporating proven hardware and software features discussed in the preceding, a functional prototype Autoprobe system can be achieved having full production D/HMA test capability.

AUTOPROBE IMPROVEMENTS FOR HIGH RATE PRODUCTION TEST OF HYBRIDS

Item	Proposed Improvement	Resultant Advantage
Hybrid Handler	Provide automatic hybrid handler and multiple socket test fixture equipment.	Vital for high rate hybrid test throughput. Hughes-Tucson has built an operational handler.
Parametric Hybrid Testing	Provide localized hybrid and probe chamber and equipment for -55°C to +100°C testing.	Assure hybrid function in environment for missile electronics.
	Procure or provide ATE system or hybrid test adapters for dynamic functional testing.	Assure hybrid function at operating data rate of missile electronics.
Automatic Hybrid Alignment and Recognition	Use CCTV camera and SW to provide automatic hybrid alignment of X, Y coordinates.	Video-SW technique, developed for Hughes, HMC-2460 wirebonder, is available for direct AP use to increase test throughput and reduce operator error. Hybrid auto alignment requires about 0.15 seconds.
	Provide hybrid markings or bar code, SW and ATE memory for auto recognition.	Increase hybrid test throughput and reduce operator error.

END

FILMED

12-85

DTIC