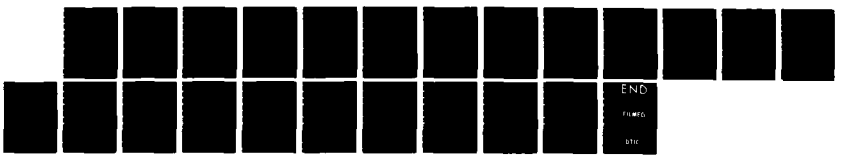
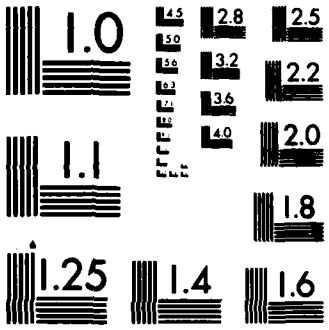
AD-A161 244 COMPUTER-AIDED FABRICATION SYSTEM IMPLEMENTATION(U) 1/1
MASSACHUSETTS INST OF TECH CAMBRIDGE DEPT OF ELECTRICAL
ENGINEERING AND COMPUTER SCIENCE P PENFIELD ET AL
UNCLASSIFIED 30 SEP 85 N00014-85-K-0213 F/G 9/2 NL





DEPARTMENT OF ELECTRICAL ENGINEERING AND COMPUTER SCIENCE

MASSACHUSETTS INSTITUTE OF TECHNOLOGY

CAMBRIDGE, MASSACHUSETTS 02139

COMPUTER-AIDED FABRICATION SYSTEM IMPLEMENTATION

Semiannual Technical Report
for the period
April 1, 1985 to September 30, 1985

Massachusetts Institute of Technology
Cambridge, MA 02139

Principal Investigators:
Paul Penfield, Jr. (617) 253-2506
Stanley B. Gershwin (617) 253-2149
Dimitri A. Antoniadis (617) 253-4693
Donald E. Troxel (617) 253-2570

This research was sponsored by Defense Advanced Research Projects Agency (DoD), through the Office of Naval Research under Contract N00014-85-K-0213.

TABLE OF CONTENTS

Selected Publications (starting after page 5)

Stanley B. Gershwin, "Dynamic Production Scheduling in Computer-Aided Fabrication;" MIT VLSI Memo No. 85-243, April 1985.

Duane S. Boning and Dimitri A. Antoniadis, "MASTIF - A Workstation Approach to Fabrication Process Design," to appear in Proc. IEEE International Conference on Computer-Aided Design, Santa Clara, CA, November 18-21, 1985.

RESEARCH OVERVIEW

During this period, much of our effort was involved in specifying, ordering, and installing equipment. A DEC VAX-785 was ordered and delivered. At the same time data lines were installed in every room of the building housing the new MIT VLSI Research Laboratory. These all lead to a central location where seven concentrators using PDP 11/73 computers on the MIT Chaosnet are located. After much investigation, concentrator software was selected (SWITCH). Two of the concentrators are working at this time; the others are awaiting some hardware. The 785, to be known as MIT-CAF, is scheduled for installation during October 1985.

Because equipment is being moved into the clean room starting in mid September, a rudimentary CAF system was required at that time. During the summer the capabilities of the initial system were discussed with many classes of users, and features ordered according to urgency. The goal of having a working system by September 1 was met, although the system does not have anywhere near its ultimate capability, and does not use a particularly sophisticated data base. The most important principle guiding the development of the system was that it be an open system, capable of graceful extension and modification. The system relies heavily on UNIX utilities and consists principally of UNIX shell scripts. It is really more of an environment than a program, and was given the name CAFE, standing for Computer Aided Fabrication Environment.

SCHEDULING

During this period, we have begun to gather information on the scheduling issues in semiconductor fabrication facilities. We plan to develop a model of such systems which will allow the development of scheduling algorithms that incorporate feedback of state information. Such models will include phenomena such as machine failures, demand variations, set-up times, parts mix, maintenance, finite machine capacities, and other features. These very features are the ones that frequently make system scheduling difficult.

It is anticipated that the management system will be organized hierarchically. Short-term management and control--real-time control--must be consistent with long-term management decisions. Lower levels in the hierarchy are more spatially (as well as temporally) limited than higher levels. That is, they deal with fewer machines. Higher levels have more power than lower, in the sense that they set objectives for the lower levels, which must indicate their capabilities to the higher levels.

MODULAR PROCESS

We have developed a preliminary architecture for a CAD program to implement modular process synthesis. The program, called MASTIF, implements a workstation approach to IC fabrication process design. It is a menu- and window-oriented program which provides a methodology and uniform software structure for the connection of process- and device-design tools.

MASTIF is written in C and Fortran, which permits easy connection to existing and prospective process and device simulators and related tools. MASTIF currently supports incremental development and version management of a process specification under development. It also provides mechanisms for the simulation and analysis of physical cross sections, and includes interactive graphics interfaces to SUPREM-III and MINIMOS.

CAF SYSTEM STRUCTURE

We have implemented a preliminary version of a CAF system for use in our fabrication facility. The architecture and capabilities of this system, named CAFE, Computer-Aided Fabrication Environment, were defined during summer 1985, and the system was ready for brave users (who don't mind a few bugs) on September 1, 1985.

The desired ultimate set of capabilities was described over a year ago by a multi-university group.[1] During the summer a selection was made of features to be implemented first. The features with the highest perceived immediate value were not those of ultimate scientific and engineering interest, so much as those that enabled the new facility to start off immediately without paper. This was deemed important in setting people's attitudes toward contamination right from the beginning. The specific features selected for the initial implementation were:

User List
Machine list
User Qualification Table
Message-of-the-day
Personal Laboratory Notebook
Machine Operating Instructions
Activity Log

The hardware features deemed most urgent (aside from a central computer to run the system) were terminals in key technicians' and engineers' offices, a terminal in the gowning room, and terminals in the clean room.

The approach taken in this first implementation is to do as much as possible by using UNIX shell scripts, and other standard UNIX features. The user list was implemented by expanding the UNIX password file. Each machine is a directory in the data area, and therefore the machine list is merely a directory listing. The message-of-the-day is the standard UNIX facility. The laboratory notebooks were implemented by a relatively simple shell script which merely appends terminal input to a file. The data structures are all file-based. No attempt was made to use a relational data base at this early stage.

At this time CAFE is being taught to the first group of users. It appears adequate to support the paperless feature of the lab, but is still very crude.

---

[1] P. Penfield, Jr., S. B. Gershwin, D. A. Hodges, C. M. Osburn, J. Reynolds, J. Schott, A. J. Steckl, and D. E. Troxel, "Requirements for Computer-Aided Fabrication," MIT VLSI Memo No. 84-200, January 17, 1984.

PUBLICATIONS LIST

Stanley B. Gershwin, "Dynamic Production Scheduling in Computer-Aided Fabrication," MIT VLSI Memo No. 85-243, April 1985.

Duane S. Boning and Dimitri A. Antoniadis, "MASTIF - A Workstation Approach to Fabrication Process Design," to appear in Proc. IEEE International Conference on Computer-Aided Design, Santa Clara, CA, November 18-21, 1985.

DEPARTMENT OF ELECTRICAL ENGINEERING AND COMPUTER SCIENCE

MASSACHUSETTS INSTITUTE OF TECHNOLOGY

CAMBRIDGE, MASSACHUSETTS 02139

VLSI Memo No. 85-243 April 1985

Dynamic Production Scheduling in Computer-Aided Fabrication*

Stanley B. Gershwin**

ABSTRACT

The Massachusetts Institute of Technology is beginning a project in computer-aided fabrication (CAF) of very large scale integrated (VLSI) circuits, with support from the Defense Advanced Research Projects Agency. This project deals with a wide range of issues related to the computer-supported fabrication of chips, including process design and process control.

One important set of issues is in the management of the facility. In order to get optimal utilization of the very expensive capital equipment in a semiconductor production system, careful monitoring of the state of the system is required. Management decisions must be made based on the current state of the system and on anticipated future changes in the state. By "system state" we mean the repair condition of the machines, the levels of inventories, and other important dynamic variables that affect the ability of the system to produce material.

In this paper we discuss some of the system management issues that we plan to study during the course of this project.

---

*This work was supported in part by the Defense Advanced Research Projects Agency of the Department of Defense under the Office of Naval Research contract no. N00014-85K-0213 and in part by the International Business Machines Corporation.

**Laboratory for Information and Decision Systems, Room 35-433, MIT, Cambridge, MA 02139, (617) 253-2149.

DYNAMIC PRODUCTION SCHEDULING IN COMPUTER-AIDED FABRICATION

by

Stanley B. Gershwin
Laboratory for Information and Decision Systems
Massachusetts Institute of Technology
Cambridge, MA 02139

INTRODUCTION

The Massachusetts Institute of Technology is beginning a project in Computer-Aided Fabrication (CAF) of Very Large Scale Integrated (VLSI) circuits, with support from DARPA. This project deals with a wide range of issues related to the computer-supported fabrication of chips, including process design and process control.

One important set of issues is in the management of the facility. In order to get optimal utilization of the very expensive capital equipment in a semiconductor production system, careful monitoring of the state of the system is required. Management decisions must be made based on the current state of the system and on anticipated future changes in the state. By "system state" we mean the repair condition of the machines, the levels of inventories, and other important dynamic variables that affect the ability of the system to produce material.

In this paper we discuss some of the system management issues that we plan to study during the course of this project.

ISSUES

An extensive set of requirements for a computer-aided fabrication system for VLSI was enumerated by Penfield, et al. (1984). Among them were the following capabilities for the management of a plant:

Plant Description: There should be a data base that completely describes all the equipment used in analysis and fabrication.

Environmental Monitoring: This is necessary for safety and to insure process quality. Both reasons may require management actions if exceptional conditions are encountered.

Utilities Monitoring: The quality of gases, deionized water, power sources, and so forth must be monitored.

Consumables Inventory: Quantity, quality, and, in some cases, age of raw materials must be monitored. Management and scheduling decisions may be influenced by these factors.

Equipment History and Usage: Use periods, idle periods, and maintenance events should be recorded. The history of a piece of equipment can provide important information about its capacity and availability for a given operation.

Equipment Status: The current status of each component of the fabrication system should be recorded and made available for management and scheduling decisions. Such information includes the repair state of each machine and the length of each queue.

Maintenance Scheduling: The CAF system should schedule maintenance events as well as production.

Management of Materials Handling Equipment: When the movement of material is automated, the CAF system should issue movement commands to the transportation system. In manual systems, the CAF system can request human operators to move material.

Personnel Management: Human resources are no less crucial to the operation of a fabrication system than equipment. The CAF system should maintain a data base on personnel, including skills available, presence or absence, and other information relevant to the capability of the system to produce the required products.

The following requirements are for product management capabilities:

Lot Tracking: The system should keep track of the location and status of each lot in the system.

Scheduling of Lots: The system should provide movement recommendations for manually operated lines and movement commands for automated systems. It should take into account the current states of all machines and transport devices, production surpluses and backlogs, priorities, and maintenance requirements. It should also consider future events by using a statistical model of disruptive events such as failures, engineering changes, etc. It must provide its recommendations or commands quickly, so that the system is not required to wait for these calculations.

Tooling Management: The system should keep track of the locations and states of masks.

Cost Accounting: The system should keep track of costs due to the consumption of raw materials and the utilization of machines and personnel.

This is only the subset of the numerous capabilities listed in Penfield, et al. (1984) that are closely related to system scheduling.

APPROACH

Manufacturing systems are difficult to manage because of their complexity and randomness. Software developers have re-

sponded to the complexity by creating large data base and MRP systems. However, randomness is not treated. Some academic research has been directed toward some kinds of randomness--such as variations in processing time using queuing network theory--but these kinds of randomness are of minimal importance. The major thrust of our scheduling research will be on more important stochastic effects such as machine failures, demand perturbations, engineering changes, etc. These effects can cause major disruptions, and managers must respond by taking action.

Hierarchical Management and Control

It is widely appreciated that the management of a manufacturing system should be organized hierarchically. Short term management and control--real time control--should be consistent with long term management decisions.

Capacity plays a central role in manufacturing system management and control. The definition of capacity depends on time scale, i.e., hierarchical level; instantaneous (low level) capacity takes the current set of available resources into account, while long term (high level) capacity considers average availability of resources.

Lower levels in the hierarchy are more spatially (as well as temporally) limited than higher levels. That is, they deal with fewer machines. Higher levels have more power than lower, in that they set objectives for them. Lower levels must indicate their capacities to the higher levels. Higher levels are based on an aggregation of lower level models.

The fundamental issue in dynamic scheduling--at any level of the hierarchy--is to determine the current capacity of the system, and to make a management decision within that capacity. The decision must be based on anticipated future changes in the system.

A more complete statement of dynamic scheduling appears in Gershwin, et al. (1984). A detailed description of the present version of the algorithm appears in Kimemia and Gershwin (1983), Gershwin, Akella, and Choong (1985), and Akella, Choong, and Gershwin (1984).

NEW RESEARCH

Among the goals of the current research program at MIT are the extension of this scheduling work to semiconductor fabrication. Research activities will include:

1. Plant visits to improve our understanding of semiconductor fabrication, to learn about features that will have to be included in our methods, and to gather data.

2. Extensions of our models to include those features. We anticipate that the new features will include large set-up times, low

yields, demand variations, and engineering changes. We also feel that these extensions will fit well within the existing framework.

3. Mathematical analysis and optimization.

4. Testing by simulation. Detailed simulations of semiconductor fabrication facilities will be written and managed by the scheduling algorithms developed under this program. The behavior of the system will influence modifications of the models or the algorithms.

5. Implementation. The algorithms developed here will be considered for implementation at one or more working production facilities, including the MIT Microsystems Technology Laboratories.

CONCLUSION

A philosophy for the on-line management, scheduling, and control of a manufacturing system has been developed and is being extended to semiconductor fabrication.

REFERENCES

R. Akella, Y. Choong, and S. B. Gershwin (1984), "Performance of Hierarchical Production Scheduling Policy," *IEEE Transactions on Components, Hybrids, and Manufacturing Technology*, Vol. CHMT-7, No. 3, September, 1984.

S. B. Gershwin, R. Akella, and Y. F. Choong (1985), "Short Term Production Scheduling of an Automated Manufacturing Facility," submitted to *IBM Journal of Research and Development*, 1985.

S. B. Gershwin, R. R. Hildebrant, R. Suri, and S. K. Mitter (1984), "A Control Theorist's Perspective on Recent Trends in Manufacturing Systems," *Proceedings of the 23rd IEEE Conference on Decision and Control*, December, 1984.

J. Kimemia and S. B. Gershwin (1983), "An Algorithm for the Computer Control of a Flexible Manufacturing System," *IEE Transactions*, Volume 15, No. 4, December, 1983.

P. Penfield, S. B. Gershwin, D. A. Hodges, C. M. Osburn, J. Reynolds, J. Schott, A. J. Steckl, D. E Troxel (1984), "Requirements for Computer-Aided Fabrication," Microsystems Program Office VLSI Memo No. 84-200, Massachusetts Institute of Technology, January 17, 1984.

ACKNOWLEDGMENTS

This work was supported in part by the Advanced Research Projects Agency of the Department of Defense and in part by the International Business Machines Corporation.

DEPARTMENT OF ELECTRICAL ENGINEERING AND COMPUTER SCIENCE

MASSACHUSETTS INSTITUTE OF TECHNOLOGY

CAMBRIDGE, MASSACHUSETTS

VLSI Memo No. 85-259 September 1985

MASTIF - A Workstation Approach to Fabrication Process Design*

Duane S. Boning and Dimitri A. Antoniadis**

ABSTRACT

The design of a fabrication process increasingly necessitates the availability and use of a variety of tools, including process and device simulation, analysis, and synthesis aids. The MASTIF workstation (MIT Analysis and Simulation Tools for IC Fabrication) is a menu and window oriented program written in C and Fortran which provides a methodology and uniform software structure for the connection of process and device design tools. MASTIF currently includes a facility for incremental development and version management of a process description, management mechanisms for definition of physical cross sections deriving from the overall process description, and an interactive graphics interface and data interchange for process and device simulators (SUPREM-III and MINIMOS). With MASTIF, the user can effectively develop and evaluate a fabrication process via a single integrated workstation.

---

*To be presented at the International Conference on Computer-Aided Design, Santa Clara, California, November 18-21, 1985. This work was supported in part by DARPA contract no. N00014-85K-0213 and by a National Science Foundation Graduate Fellowship.

**Department of Electrical Engineering and Computer Science, MIT, Cambridge, MA 02139, Boning: Room 39-315 (617) 253-6963; Antoniadis: Room 39-227, (617) 253-4693.

PRELIMINARY DRAFT
This paper is to be presented at ICCAD-85.

MASTIF - A Workstation Approach to Fabrication Process Design

Duane S. Boning and Dimitri A. Antoniadis
Massachusetts Institute of Technology
Room 10-372H Cambridge, MA 02139
617-253-6963 dsb%mit-waif mit-mc.arpa

Abstract

The design of a fabrication process increasingly necessitates the availability and use of a variety of tools, including process and device simulation, analysis, and synthesis aids. The MASTIF workstation (MIT Analysis and Simulation Tools for IC Fabrication) is a menu and window oriented program written in C and Fortran which provides a methodology and uniform software structure for the connection of process and device design tools. MASTIF currently includes a facility for incremental development and version management of a process description, management mechanisms for definition of physical cross sections deriving from the overall process description, and an interactive graphics interface and data interchange for process and device simulators (SUPREM-III and MINIMOS). With MASTIF, the user can effectively develop and evaluate a fabrication process via a single integrated workstation.

Motivation

Spurred by the increasing complexity of VLSI design, many CAD tools have been developed to provide help in successive phases of design, from system specification through circuit realization to mask layout. Many of these design tasks can be accomplished on integrated workstations, where tools for capture and synthesis are accompanied by verification and simulation programs.

The design of the fabrication process, on the other hand, is a task which suffers from a lack of similar computer assistance. Process simulators such as SUPREM [1] and SUPRA [2] have been developed to model the fabrication process; simulators such as MINIMOS [3] also exist for the evaluation of semiconductor devices. Few integrated systems exist which provide both simulation and synthesis tools in the domain of device and process design [4]. Such an integrated workstation is needed to meet a number of particular process design needs.

Requirements for a Process Design System

As with each of the other IC design phases, a process design system is needed to provide aid in roughly two categories: simulation and synthesis. This section will examine these two aspects in turn. The role, utilization, and requirements of CAD tools in process simulation are discussed below:

1. ROLE OF PROCESS SIMULATION: A process simulator transforms a starting representation of the wafer structure (or initial wafer state) into a final representation under the influence of a specified wafer treatment. By performing successive simulation steps to model the actual sequence of fabrication operations, one, two, or (eventually) even three dimensional models of a a device or wafer structure can be constructed. Thus, SUPREM-III provides material and impurity concentration information for one-dimensional cross-sections, while SAMPLE [5] calculates two-dimensional geometric effects resulting from lithographic, deposition, and etching process steps.

2. USE OF PROCESS SIMULATORS: The structure produced by process simulators is useful only so far as means are also available for the analysis and evaluation of the structure with respect to formal or informal goals. Some analysis capabilities, such as sheet resistance or junction depth calculations, are usually built into process simulators.

3. PROCESS SIMULATION REQUIREMENTS

a. Common Interface: An interface between the process engineer and the multitude of simulators is important for two reasons. First, the variety of simulation protocols or languages makes use tedious; a translation from a single description of the process to the particulars of each simulator is needed. Secondly, a unique description of the process is important in order to guarantee that the various simulators create consistent structural information.

b. Computation: Process simulation is driven by complex and often incompletely understood physics. As such, process simulation is a computationally intensive and time consuming task. Mechanisms for reducing the amount of simulation during process development are needed.

c. Device Simulation: Often very sophisticated analysis of the wafer structure is needed. A model of a whole device structure constructed from process simulation results is usually evaluated using device simulators. For example, the threshold voltage for an MOS device or a response to specified bias conditions may be the measure of "success" for a particular process. Adequate process analysis thus requires a good interface between device and process simulators.

The requirements for process "capture" or synthesis can be summarized as follows:

1. PROCESS REPRESENTATION: The goal of process synthesis is to produce a fabrication process which meets a set of goals. Clearly, some representation of the process is required. This process specification must be powerful enough to construct structure representations using a variety of process simulators, but must be independent of any particular simulator.

2. STRUCTURE REPRESENTATION: A uniform representation of device or wafer structures would be useful as a common interchange between different process simulators, analysis tools, device simulators, and graphic display packages. In the absence of such an interchange format, explicit interfaces must be developed where needed.

3. DESIGN MANAGEMENT: Just as in circuit design, a great need for documentation and version management exists in the design of a process. Version control is particularly complicated in process design. The engineer must not only compare the effects of different process parameter choices, but it must also examine the effects of a choice in several different regions or cross-sections of the physical structure. That is, the system must manage structures that change with process modifications, spatial position, and simulation time.

4. AUTOMATIC SYNTHESIS: The creation of a fabrication process is currently a highly intuitive and complex task. The physical structure depends on process parameters in a very nonlinear manner, and the tradeoffs to be managed are ill-defined. These characteristics make it difficult both for engineers to develop processes and for researchers to develop expert systems.

The MASTIF Process Design Workstation

The MASTIF workstation is a first attempt at meeting the requirements for process design outlined above. The current capabilities of MASTIF will be summarized; tools that have been developed or incorporated into the workstation will be described. This will be followed by a discussion of the implementation of MASTIF, with emphasis on mechanisms for extending the system to include additional tools.

1. MASTIF CAPABILITIES: an integrated workstation approach to process design has been adopted. The user interacts with a single graphics screen via a tablet and keyboard; a variety of menus and windows can be displayed simultaneously. The basic user modules in MASTIF are summarized in Figure 1.

A Process Description Window gives the engineer the ability to interactively create and edit a fabrication Process Description. This description is independent of any particular process simulator, and includes constructs for version management.

A Cross Section Summary Window allows the engineer to specify a number of one or two dimensional regions or cross sections for both process and device simulation. Masking or layout information is incorporated here. This window is also responsible for maintaining consistency between the Process Description Window and the various Process Simulation Windows.

A number of different Process Simulation Windows can be used simultaneously. Given the global Process Description and masking information for a specified cross section, a SUPREM One-Dimensional window can be created and updated automatically. From the menu in this window, the user can direct background simulation of particular steps, as well as interactively produce plots or calculations of steps in the process. Currently, only SUPREM-III simulations are available; eventually both one and two-dimensional simulators will be incorporated.

A Device Simulation Window can also be generated, given the cross section and process simulation information. The user may direct and evaluate MINIMOS simulations from the menu of this window. The results of simulations may

also be examined graphically through a MIDAS window. This subsystem consists of a general purpose MINIMOS plotting module and an interactive Focused Ion Beam simulation subsystem.

2. MASTIF IMPLEMENTATION: Mastif is implemented in C and Fortran, and currently runs on a multi-user VAX 11/750 under VMS. An AED 767 color graphics display terminal with tablet and mouse and a keyboard completes the hardware. The MFB graphics package [6] has been used to achieve some degree of device independence. Several modules have been written to support the user windows described above.

A simple syntax generation and parsing subsystem provides the capability for programmers to write new "syntaxes" using a parameter specification grammar (similar to the grammar used in SUPREM-III). Examples of syntaxes which are expressed by MASTIF using this grammar include the Process Description, the SUPREM-III input language, the Cross Section summary, and the MINIMOS input language. Once a syntax is specified, text files may be read by MASTIF, expressed and manipulated either graphically or textually by window handlers, and rewritten as text files for storage purposes.

A menu handling subsystem provides for the generation and use of simple menus. These menus are associated with each window, and may be either permanent or "pop-up" in format. Special purpose menus (such as a color selection menu) can also be generated.

A Main Menu and Command Area are included. Information and prompts may be issued, and textual inputs accepted from the window. A Browsing Window allows the user to examine system files.

A Background Job Handling system manages the executions of SUPREM and MINIMOS jobs. In order to maintain modularity and extensibility of the system, MASTIF has adopted a methodology for inclusion of simulation tools whereby all simulators are maintained in a stand-alone form. MASTIF will generate the input files, manage execution, and access results of simulators in a manner that does not require modification of the simulation programs themselves.

Evaluation of MASTIF

MASTIF has so far been useful in a number of ways. At the very least, the SUPREM Cross Section Windows provide a powerful, interactive user interface to the SUPREM-III simulator. Secondly, the ability to create a Process Description and maintain simulation consistency in multiple regions of the wafer in the face of an evolving process is quite useful. Moreover, the availability of a Process

Description is advantageous in that it may interface quite well with process recipe generation programs.

In an effort to maintain the interactive and extensible nature of MASTIF, we have found that MASTIF becomes file intensive. Intermediate SUPREM simulation results are now stored as the binary data files normally produced by SUPREM. All interfaces, both with regard to input file generation and to wafer structure exchange, have been written explicitly. A profile or wafer interchange format for the storage and exchange of wafer and device structure information is currently under consideration.

A workstation approach, stress upon a uniform, interactive interface between tools, MASTIF, and the engineer, and the availability of a base of MASTIF subsystems make it possible to add tools to MASTIF as they are developed. As additional process and device simulation and analysis tools are integrated into the system, it is expected that MASTIF will become a powerful system for the design of semiconductor devices and fabrication processes.

Acknowledgements

This material is based upon work supported by DARPA contract N00014-85K-0213. The work of D. Boning was supported in part by a National Science Foundation Graduate Fellowship. The contributions of J. Jacobs, T. Tung, and R. Lowther are gratefullly acknowledged.

References

[1] C.P. Ho, J.D. Plummer, S.E. Hansen, and R.W. Dutton, "VLSI Process Modeling -SUPREM III", IEEE Trans. Electron Devices, Vol. ED-30, No. 11, pp. 1438-1452, Nov. 1983.

[2] D. Chin, M. Kump, R.W. Dutton, "SUPRA -Stanford University PRocess Analysis program", Reference Manual, July 1981.

[3] S. Selberherr, A. Schutz, H. W. Potzl, "MINIMOS -A Two-Dimensional MOS Transistor Analyzer," IEEE Trans. on Electron Devices, Vol. ED-27, No. 8, p. 1540, August 1980.

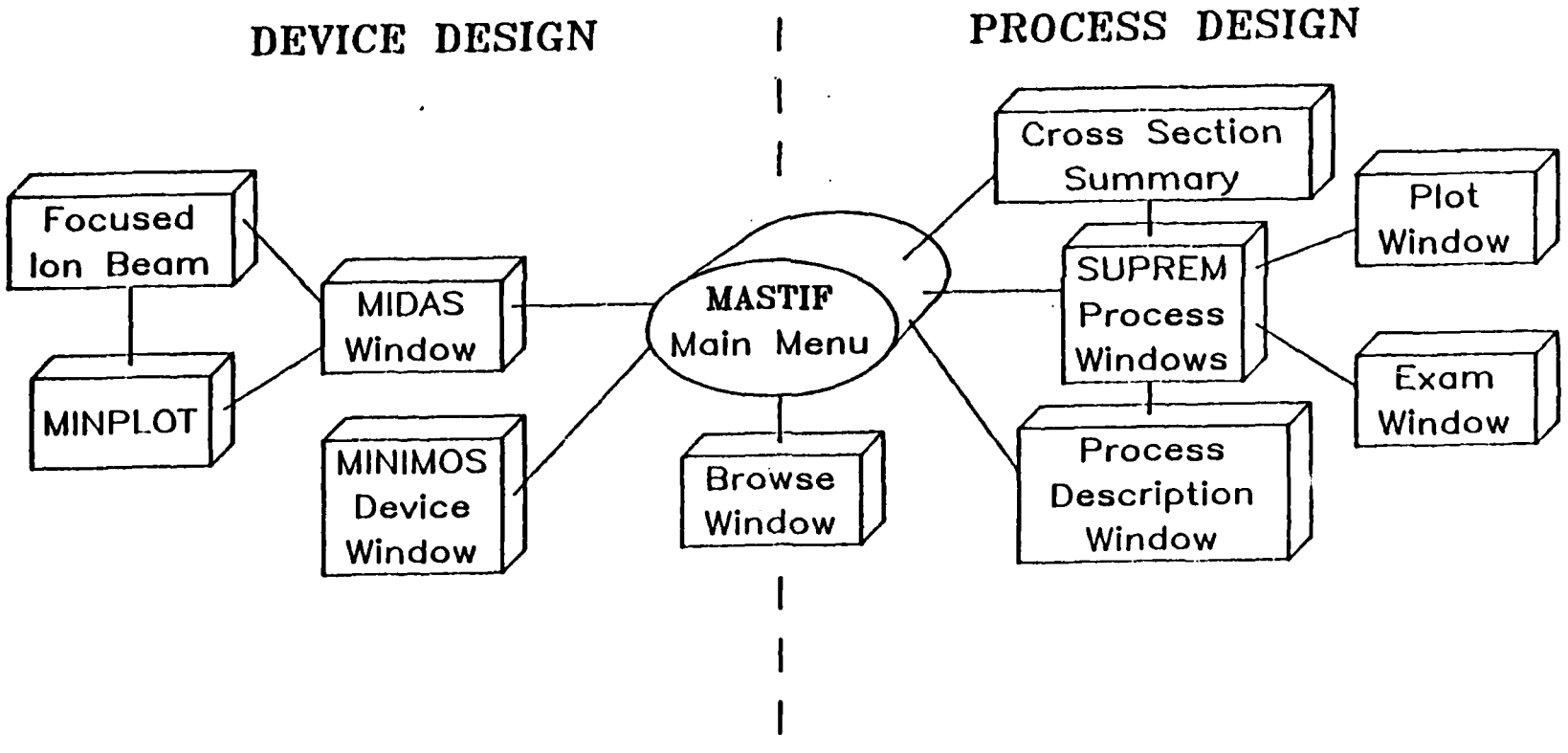
[4] K.M. Cham, S.-Y. Oh, and J.L. Moll, "Computer Aided Design in VLSI Device Development", IEEE J. Solid State Circuits, Vol. SC-20, No. 2, pp. 495-500, April 1985.

[5] A.R. Neureuther, C.H. Ting, and C.Y. Liu, "Application of Line-Edge Profile Simulation to Thin-Film Deposition

Processes," IEEE Trans. Electron Devices, vol. Ed-27, No. 8, pp. 1449-1459, August 1980.

[6] G. L. Billingsley, "Program Reference for KIC," Electronics Research Laboratory, U.C. Berkeley Memorandum No. UCB/ERL M83/62, October 1983.

List of Figures


DEVICE DESIGN
PROCESS DESIGN
Focused Ion Beam
MINPLOT
MIDAS Window
MINIMOS Device Window
MASTIF Main Menu
Browse Window
Cross Section Summary
SUPREM Process Windows
Process Description Window
Plot Window
Exam Window

END

FILMED

12-85

DTIC