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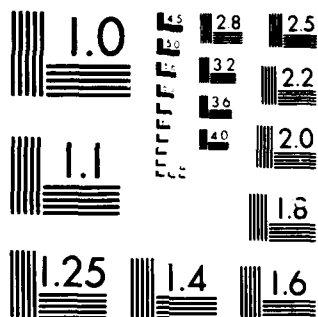
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EXPERIMENTS FOR COMMUNICATIONS STUDENTS

THESIS

Jerome B. Thompson
First Lieutenant, USAF

AFIT/GE/ENG/85D-48

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AND EXPERIMENTS FOR COMMUNICATIONS STUDENTS

THESIS

Presented to the Faculty of the School of Engineering
of the Air Force Institute of Technology

Air University

In Partial Fulfillment of the
Requirements for the Degree of
Master of Science in Electrical Engineering

Jerome B. Thompson, B.S.E.E.
First Lieutenant, USAF

December 1985

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Preface

The purpose of this study was to develop a series of laboratory experiments which could be conducted by graduate electrical engineering students in the AFIT communications curriculum and could be used by course instructors as demonstrations in the classroom.

The experiments were designed to include detailed analysis of analog and digital communication systems with topics ranging from amplitude modulation to frequency shift keying.

I would like to thank Capt G. Prescott, my thesis advisor, for his exceptional guidance during the development of this thesis effort. Thanks also go to Capt D. King for his many suggestions on the scope and details of the experiments and to Capt W. Thomson who tested several of the experimental procedures. Special acknowledgement is in order for DEGEM Systems Ltd. who provided the experimental communication circuit boards and sample experiments used as a starting point for this thesis. Finally, I extend my gratitude to Ms. Betty Johnson who gave me the endless encouragement needed to complete such a task.

Jerome B. Thompson

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Abstract

This study was a development of a series of experiments for an electronics communications laboratory. These experiments were designed to reinforce theoretical courses offered in the Air Force Institute of Technology Electrical Engineering Core Communications Sequence in the form of demonstrations or laboratory exercises.

The experiments were developed under the criteria of investigating a significant number of analog and digital communication system concepts with a minimum amount of experimentation time. Extensive use of a spectrum analyzer was included in many of the experiments.

The topics covered in the experiments include: amplitude modulation; frequency modulation; balanced modulator; single sideband modulation; phase-lock loop and frequency synthesizer; pulse amplitude modulation; pulse code modulation; delta modulation; amplitude shift keying; phase shift keying; and frequency shift keying.

The results of this study indicated that many more system concepts could be included in laboratory exercises, such as spread spectrum communications, time and frequency division multiplexing, and computer oriented testing and analysis.

THE DEVELOPMENT OF THE AFIT COMMUNICATIONS LABORATORY
AND EXPERIMENTS FOR COMMUNICATIONS STUDENTS

I. Introduction

It is desirable that theoretical engineering courses, such as courses in analog and digital communications theory, be supplemented with laboratory exercises and demonstrations. Such "hands-on" exercises reinforce the theoretical principles and provide an appreciation of practical problems and methods.

The goal of this thesis was to develop a series of laboratory experiments which could be conducted by graduate electrical engineering students in the AFIT communications curriculum and could be used by course instructors as demonstrations in the classroom.

The Problem

The specific task of this thesis project was to develop student electronics communications experiments for the AFIT Department of Electrical and Computer Engineering. These experiments will serve to provide reinforcement of theoretical studies in related courses.

Certain criteria for the experiments was initially prescribed by the department. This criteria included the following:

1. To develop experiments that would reinforce specific course material presented in the AFIT Communications Core Curriculum to include analog and digital modulation methods.

2. To cover a maximum amount of communications concepts in a minimum amount of student experimentation time.

3. To develop experimental procedures in sufficient detail to describe complete circuit and equipment arrangements including specific instructions for collecting data.

4. To provide extensive use of the spectrum analyzer to observe the frequency domain representation of communications signals and circuit characteristics.

General Approach

The approach used in developing the communications experiments was as follows:

1. The circuit boards and sample experiments provided by DEGEM Systems Ltd. were tested in the laboratory. The laboratory manuals containing the DEGEM experiments and theoretical background are listed in the References section of this thesis.

2. The sample experiments, and in some cases the circuit boards, were modified to meet the criteria of this thesis. The modifications are described in chapter III.

3. The completed experiment procedures and equipment were tested in the laboratory to ensure proper performance.

Thesis Organization

Chapter II describes the AFIT Communications Curriculum while chapter III presents an overview of the experiments developed. Chapter IV concludes the thesis and lists recommendations for further development. The actual experiments that were developed for the AFIT Communications Laboratory are contained in the Appendices.

II. AFIT Communications Curriculum

This chapter provides an overview of the AFIT Communications Curriculum. The curriculum is an 18 month graduate level program consisting of six-11 week quarters. Each student is required to complete a thesis study of a topic of interest to the Air Force and/or Department of Defense Agencies.

The curriculum consists of a core sequence and four applications sequences. A student entering the communications sequence is required to complete the core sequence and at least one of the applications sequences. The applications sequences are:

Communications and Radar Engineering Sequence

Command/Control/Communications Sequence

Optical Communications Sequence

Electronic Warfare Sequence

Since this thesis study only dealt with systems and concepts presented in the Core Communications Sequence, only this sequence will be described here. For information regarding the application sequences, refer to the AFIT Electrical Engineering Graduate Programs description (1).

Core Communications Sequence

This sequence is required for all graduate communications students and "builds an understanding of the

statistical analysis of communications systems." (1:38) The sequence includes a study of the various theories of modulation, linear systems, and probability. The required courses are:

EENG 431 - "Introduction to Communication Systems"--emphasizes the deterministic analysis of analog and digital communication systems. Topics include: review of classical time and frequency domain signal and system representation techniques; analysis of analog amplitude, frequency, and phase modulation signals and systems; sampling theory, analog pulse modulation, pulse code modulation, and digital carrier modulation; time and quadrature multiplexing of communications signals; and introduction to the performance analysis of systems in the presence of noise. (2:4)

MATH 586 - "Probability Theory for Communication and Control"--introduces probability theory as a basis for applications in the analysis and design of modern communication and control systems. Topics include the concepts of: sample spaces; random variables and vectors; probability densities and distributions; discrete and continuous distributions; expectations and moments; statistical independence; and transformations of random variables and vectors. (2:30)

EENG 665 - "Principles of Stochastic Communications"--presents the theory of random signals and random processes related to communications systems. Topics include concepts of: random signals and moments; correlation functions;

stationarity and ergodicity; power spectral density; joint processes; linear mean square estimation for random variables and processes; and series representations of random processes. (2:17)

EENG 667 - "Coding and Information Theory"--introduces the theory of information as applied to communication and error correcting codes. Selected topics are: the theorems and applications of information theory; entropy and mutual information; characterization of sources and channels; performance of noiseless source coding; channel capacity; source-channel coding; and block coding, interleaving, and concatenation. (2:18)

EENG 670 - "Digital Communications Theory"--presents the significant considerations necessary for design, analysis, and performance of digital communications techniques and systems. Topics include: mathematical representation of digital signals; performance analysis of various signalling schemes; channel bandwidth constraints; and analysis of the use of different methods of channel coding.

EENG 671 - "Analog Communications Theory"--develops the theory of analog communication techniques in the presence of noise. Topics include: statistical models of noise and modulated carriers; system noise calculations; antennas; nonlinear processing of random signals; performance of analog modulation techniques and phase locked loops in noise; matched filters; quantization error; and analysis of

baseband binary communication systems in noise. (2:18)

The experiments developed in this thesis effort mainly reinforce the material covered in the courses "Introduction to Communication Systems" and "Digital Communication Theory". These two courses present a significant number of communication systems concepts that are easily demonstrated in a laboratory setting.

III. Overview of the Laboratory Experiments

This chapter describes the experiments that were developed in this thesis. The experiments are listed with a brief description of each. Also included is a description of some of the problems encountered while developing the experiments.

The Experiments

The experiments developed are based on the communications experimental units and sample experiments supplied by DEGEM Systems Ltd., Atidim, P.O. Box 13005, Tel-Aviv, Isreal. The DEGEM experiments were tested in the laboratory and modified to meet the criteria of this thesis. The actual experiment procedures, ready for use by students, are contained in the Appendices of this thesis. Each is complete within itself, fully describing what needs to be done in the laboratory and should require no more than three hours to complete. Each experiment was fully tested by the author and several experiments tested by a communications student. Sample data sheets with experimental results are included with each experiment in the appendices.

It was not feasible to use the experiments as written by DEGEM Systems Ltd. for a laboratory course at AFIT. These experiments made no use of the spectrum analyzer and included many tedious, data gathering procedures. (e.g.

determining the frequency response of a system by measuring and plotting output signal amplitudes versus input frequencies.) To keep the number of concepts explored versus the experimentation time at a maximum, some of the DEGEM Systems procedures were excluded. Most of these procedures did not show a significant communications concept for the amount of experimentation time required.

Most of the experiments were written in the following format:

OBJECTIVE - States the scope of the particular experiment.

PREREQUISITES - States any prior work that must be done before completing the experiment.

REQUIRED EQUIPMENT - Lists the equipment needed to complete the experiment.

REFERENCES - Lists references used in the experiment.

THEORETICAL BACKGROUND - References the theoretical material provided in the DEGEM Systems manuals located in the laboratory. Additional background is also provided in some cases where specific equations and concepts are referred to in the experiment procedure.

DEGEM CIRCUIT BOARD DESCRIPTION - References the information in the DEGEM Systems manuals describing the circuit test boards used in the experiment.

EXPERIMENT PROCEDURE - Details the steps to be taken by the student to complete the experiment. Specific circuit and test equipment connections are described.

The laboratory experiments developed in this thesis are listed in table I. Table II contains a list of set-up procedures for use by instructors or technicians to adjust certain circuit board components before conducting a laboratory course.

TABLE I

List of Experiments

<u>LAB</u>	<u>TITLE</u>	<u>OBJECTIVE/TOPICS</u>	<u>RELATED COURSE</u>
1	Equipment Familiarization	Familiarize the student with the equipment used in the laboratory. Primary emphasis is on use of a spectrum analyzer.	EENG 431
2	Amplitude Modulation	Conventional AM modulator; envelope detector; synchronous AM detector; superhetrodyne AM receiver; and the effect of automatic gain control.	EENG 431
3	Frequency Modulation	FM modulator; ratio detector; product detector; superhetrodyne FM receiver; and the effect of automatic frequency control.	EENG 431
4	Balanced Modulator	Characteristics of balanced modulator used as a mixer, AM detector, phase detector, and double sideband-suppressed carrier AM modulator.	EENG 431
5	Single Sideband Modulation	Single sideband modulation and detection; and single sideband compatible AM.	EENG 431

TABLE I (Continued)

List of Experiments

<u>LAB</u>	<u>TITLE</u>	<u>OBJECTIVE/TOPICS</u>	<u>RELATED COURSE</u>
6	Phase-Lock Loop and Frequency Synthesizer	Characteristics of voltage controlled oscillator and phase detector; phase-lock loop operation; and frequency synthesizer use of the phase-lock loop.	EENG 431
7	Pulse Amplitude Modulation	Simple and flat-torped sampling; Nyquist sampling; time-division multiplexed pulse amplitude modulation; and cross-talk between multiplexed channels.	EENG 431
8	Pulse Code Modulation	Pulse code modulation and demodulation; linear and companded quantization; and analog-digital and digital-analog conversion.	EENG 431
9	Delta Modulation	Delta modulation and demodulation; integrating, adaptive, and current source modulation; and effects of slope-overloading.	EENG 431
10	Amplitude Shift Keying	Performance characteristics (bit error rate versus input signal-to-noise ratio) of binary and bitternary amplitude shift keying.	EENG 670

TABLE I (Continued)

List of Experiments

<u>LAB</u>	<u>TITLE</u>	<u>OBJECTIVE/TOPICS</u>	<u>RELATED COURSE</u>
11	Phase Shift Keying	Performance characteristics (bit error rate versus input signal-to-noise ratio) of binary and differential phase shift keying; and carrier recovery in noise.	EENG 670
12	Frequency Shift Keying	Performance characteristics (bit error rate versus input signal-to-noise ratio) of binary and bitternary frequency shift keying.	EENG 670

TABLE II
List of Set-up Procedures

<u>LAB</u>	<u>TITLE</u>	<u>OBJECTIVE/TOPICS</u>
2-S	Amplitude Modulation Set-up	Procedure for instructor or technician to properly tune circuit components prior to having students perform Lab 2.
3-S	Frequency Modulation Set-up	Procedure for instructor or technician to properly tune circuit components prior to having students perform Lab 3.
4-S	Balanced Modulator Set-up	Procedure for instructor or technician to properly tune circuit components prior to having students perform Lab 4.

Problems Encountered In Developing The Experiments

The main problem encountered when developing these experiments was getting the circuit boards to operate properly. Much time was spent diagnosing problems and adapting the circuit boards and input signals to achieve desired results. Slight changes to circuit components were made in two cases and are described in a section below.

An unresolved problem in a circuit board prevented including an experiment on synchronization for a time division multiplexing (TDM) system. This problem is detailed later.

Circuit Board Modifications.

The first modification was made to the DEGEM Unit COM-1/3 board used in Lab 2 (Amplitude Modulation). The intermediate frequency (IF) amplifiers could not be tuned to the center frequency of the mixer stage causing much distortion in the output signal. Therefore the capacitors that set the tunable ranges of the amplifiers' resonant frequencies were changed from 330 pf to 390 pf. These capacitors are located inside the board and are in parallel with the IF tuning transformers. Figure 1 shows the circuit diagram of the IF amplifier stages with the specific capacitors noted.

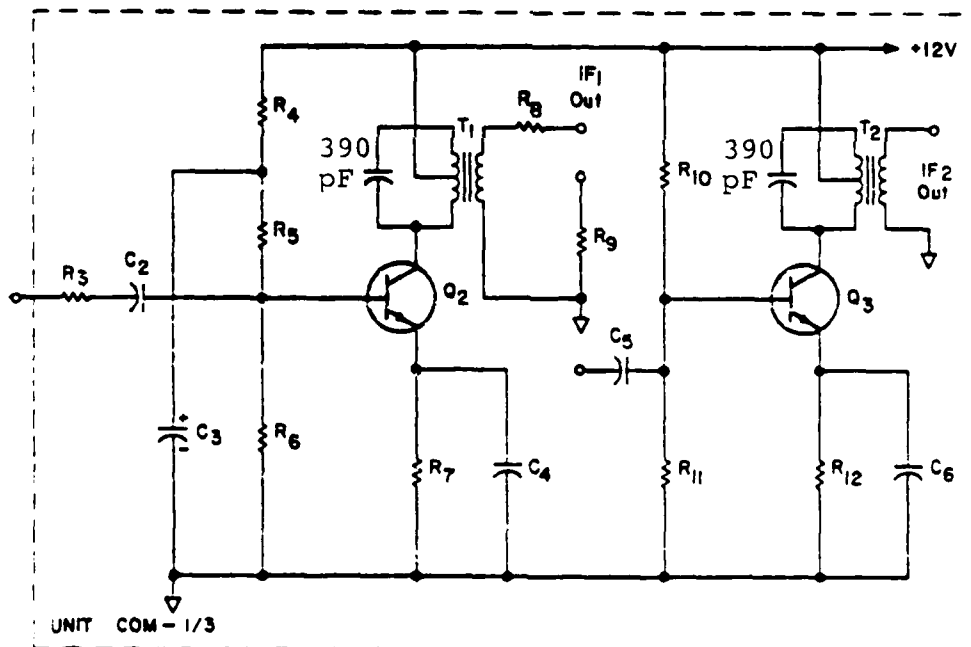


Figure 1. DEGEM Unit COM-1/3 IF Amplifiers. (3:36)

The second modification made was the addition of a capacitor to a control signal used on the DEGEM Unit

COM-6B/2 board. This board is used in Lab 8 (Pulse Code Modulation). A 680 pf capacitor was added inside the board between the PCL control signal and ground to reduce the amount of noise on this signal. Without the capacitor, the PCL signal was clocking data out of the modulator's parallel to serial converter one bit too soon, causing improper demodulation of the PCM codewords. Figure 2 shows the circuit board with the capacitor attached to the PCL signal.

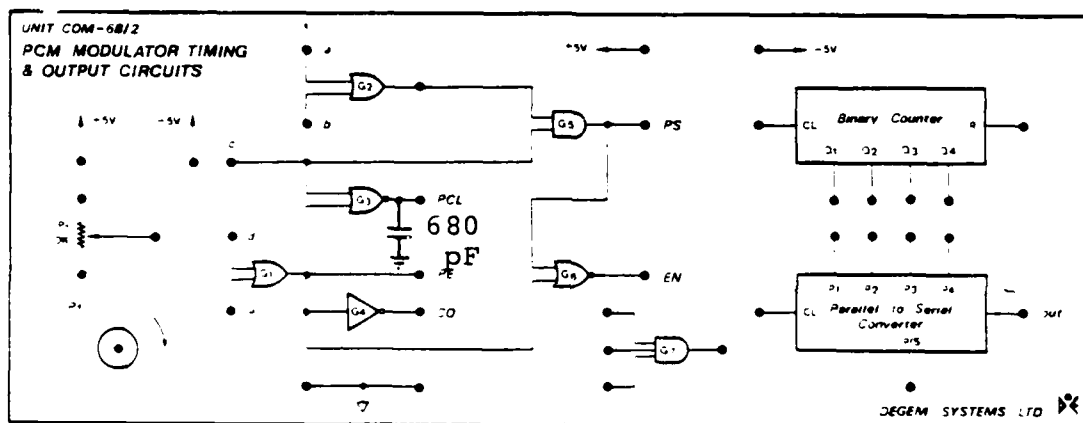


Figure 2. DEGEM Unit COM-6B/2 Board. (4:106)

Problem With TDM Synchronization Circuit.

There are problems with the time division multiplexing synchronization circuit that were not resolved, thus leaving this topic unexplored in the developed experiments. While TDM is briefly covered in Lab 7 (Pulse Code Modulation), the full scheme of time division multiplexing and demultiplexing did not work.

The problem lies in the DEGEM Unit COM-6A/3 board shown in figure 3. The synchronization circuit is designed to detect and lock onto a pseudo-random binary code that is placed, by the TDM modulator, in the first time slot of the TDM signal. The Synch. Indicator light on the right side of the board shown in figure 3 turns on when synchronization is achieved. After connecting the proper circuit according to the DEGEM Course COM-6 Experiments manual (4:134-140), the circuit would lock either onto the first or second time slot of the TDM signal. This caused improper demultiplexing of the TDM signal. Locking onto the second time slot may have been due to a high level of crosstalk between the TDM time slots. If this crosstalk were reduced, the circuit may operate properly and could be included in the experiments.

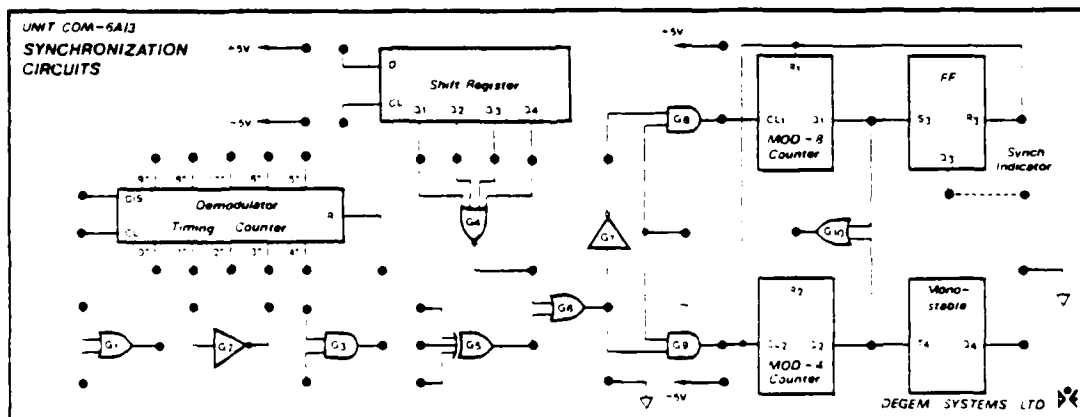


Figure 3. DEGEM Unit COM-6A/3 Board. (4:102)

IV. Conclusion

The twelve communications laboratory experiments developed and tested can be used as a foundation for one or more laboratory courses and numerous classroom demonstrations.

The experiments were designed with the concept of presenting as many communications concepts as possible with a minimum amount of experimentation time. They should prove to be worthwhile to students in reinforcing their theoretical knowledge of communications systems.

In developing these experiments, several ideas came to mind on how these experiments may be enhanced and used in the AFIT Communications Curriculum as explained below.

Recommendations

1. The time division multiplexing synchronization circuit can be further analyzed to find and correct the fault in the circuit, as was discussed in chapter III. The circuit may then be used to implement a full time division multiplexed system where several channels could carry different types of signals, such as a pulse amplitude modulated signal, a pulse code modulated signal, an encoded binary signal, and a delta modulated signal. All of these signals can be generated using the DEGEM Systems circuit boards and details on how to multiplex and demultiplex the signals are

contained in the DEGEM Course COM-6 Experiments manual (4).

2. DEGEM Systems Ltd. provided circuit boards and sample experiments for frequency division multiplexing (FDM) that could be included in the laboratory experiments. This system was not included in the developed experiments for this thesis. It was felt that an FDM experiment would have been more meaningful if it were accompanied by a TDM system for comparison. As discussed previously, the TDM system was omitted from the list of experiments. Therefore the FDM experiment was also omitted to allow more time to develop the digital modulation experiments.

3. A frequency hopping system could be made by using the frequency synthesizer studied in Lab 6 (Phase-lock Loop and Frequency Synthesizer) to change the center frequency of a modulator circuit. Binary codewords could be supplied from a psuedo-random binary code generator and applied to the synthesizer frequency multiplier circuit. If this is accomplished, another experiment, or several experiments, could be provided to study the concepts of spread spectrum communications.

4. It is recommended that AFIT acquire a 1 MHz bandwidth, true RMS voltmeter for use in the digital modulation experiments. These experiments include Lab 10 (Amplitude Shift Keying), Lab 11 (Phase Shift Keying), and Lab 12 (Frequency Shift Keying). These experiments required the RMS amplitude measurement of signals with a carrier

frequency of 512 kHz. The only true RMS voltmeter available in the laboratory at the time of this thesis study had a 500 kHz bandwidth. Although data was acquired while testing these experiments using this voltmeter, the results would be more accurate if a wider bandwidth true RMS voltmeter were used.

5. There are almost limitless applications for a computer to control the testing and data gathering of the circuits explored in the experiments. Use of a computer for circuit analysis can add another dimension to the testing of the communication systems.

6. Use of the experiments in laboratory courses:

a. These experiments can be combined into a single laboratory course where several of the experiments may be required and others made optional to the student. Such a course would be appropriate during the 5th quarter of the student's curriculum when all of the necessary theoretical background has been previously covered. Consideration must be made though to the burden on the student's time as this quarter is traditionally the thesis research quarter.

b. Alternatively, the experiments could be broken up into analog (Labs 1 through 6) and digital (Labs 1 and 7 through 12) laboratory courses. These separate courses could be integrated with theoretical courses such as EENG 431 and EENG 670.

c. The experiments are also ideal for use in the professional continuing education courses offered at AFIT in the communications area.

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1. Air Force Institute of Technology. Electrical Engineering Graduate Programs 1985-1986. 2nd Edition, May 1985.
2. Air Force Institute of Technology Electrical and Computer Engineering Department. Course Descriptions. March 1985.
3. DEGEM Systems Ltd. AM Communication Circuits Course COM-1 Experiment and Technical Manual. DEGEM Systems Ltd., 1976.
4. DEGEM Systems Ltd. Time Division Multiplexing: Sampling & Multiplexing, Pulse Code Modulation, & Delta Modulation Course COM-6. Degem Systems Ltd., 1976.

APPENDIX A

Laboratory Experiment Number 1

Equipment Familiarization

This laboratory experiment familiarizes the student with the equipment used in the laboratory. Special emphasis is placed on the use of a spectrum analyzer. This experiment is dependent upon using equipment provided by specific manufacturers. Should the equipment in the laboratory change, this is the only experiment that would need to be modified.

OBJECTIVE: To familiarize the student with the test equipment that will be used in the laboratory.

PREREQUISITES: None.

REQUIRED EQUIPMENT

The following equipment is required to perform this experiment.

1. Tektronix 7104 Oscilloscope with the following plug-in modules:

LEFT VERT	7A26 or 7A29
RIGHT VERT/A HORIZ	7L5
B HORIZ	7B10 or 7B15

(If these units are not installed as specified, refer to Appendix A.)
2. Hewlett-Packard 5248M Electronic Counter
3. Wavetek Model 148 AM/FM/PM Generator (2 required)
4. Circuit Proto-board
5. 220 Ω resistor
6. 0.01 μ F capacitor
7. Test Leads

REFERENCES

1. Tektronix, Inc. 7104 Oscilloscope with Options-Operators Instruction Manual. Tektronix, Inc., 1978.
2. Tektronix, Inc. 7L5 Spectrum Analyzer Operators Instruction Manual. Tektronix, Inc., 1978.
3. Tektronix, Inc. L3 Plug-in Module Instruction Manual. Tektronix, Inc., 1978.
4. Wavetek. Model 148 20 MHZ AM/FM/PM Generator. Wavetek, 1978.

INTRODUCTION

The test equipment used in the laboratory will be described and then used to observe various waveforms. This should provide sufficient understanding of the equipment controls

and functions necessary to complete the experiments in the laboratory.

TEKTRONIX 7104 OSCILLOSCOPE

Figures 1 and 2 show the front panel controls and indicators on the 7104 and figure 3 shows the rear panel controls and connectors. Some of the 7104 controls and functions are described below. For more details refer to the 7104 Oscilloscope Operators Instruction Manual (1) located in the laboratory.

NOTE

Most pushbuttons on the 7104 and its plug-in modules become illuminated when the button is active.

Vertical and Horizontal Modes

The plug-in units that control the display trace are selected through the vertical and horizontal mode pushbuttons.

The vertical mode is controlled by the LEFT, ALT, ADD, CHOP, and RIGHT pushbuttons above the plug-in compartments. The horizontal mode is controlled by the A, ALT, CHOP, and B pushbuttons. With these buttons, any desired combination of the plug-in units can be used without re-installing the units.

For example, with the plug-in units installed as specified in the Required Equipment section above, pressing LEFT Vertical Mode and B Horizontal Mode causes a display of the time-domain trace of the input signal. Pressing RIGHT Vertical Mode and A Horizontal Mode causes a display of the frequency-domain trace.

Trigger Sources

The A HORIZ and B HORIZ time base units can be triggered from either the LEFT or RIGHT vertical units. Usually the A and B TRIGGER SOURCE switches are kept in the VERT MODE position. This allows for automatic switching of the trigger source as the Vertical Mode is changed. If desired, the trigger source can be set to the LEFT or RIGHT vertical unit by pressing the LEFT VERT or RIGHT VERT buttons.

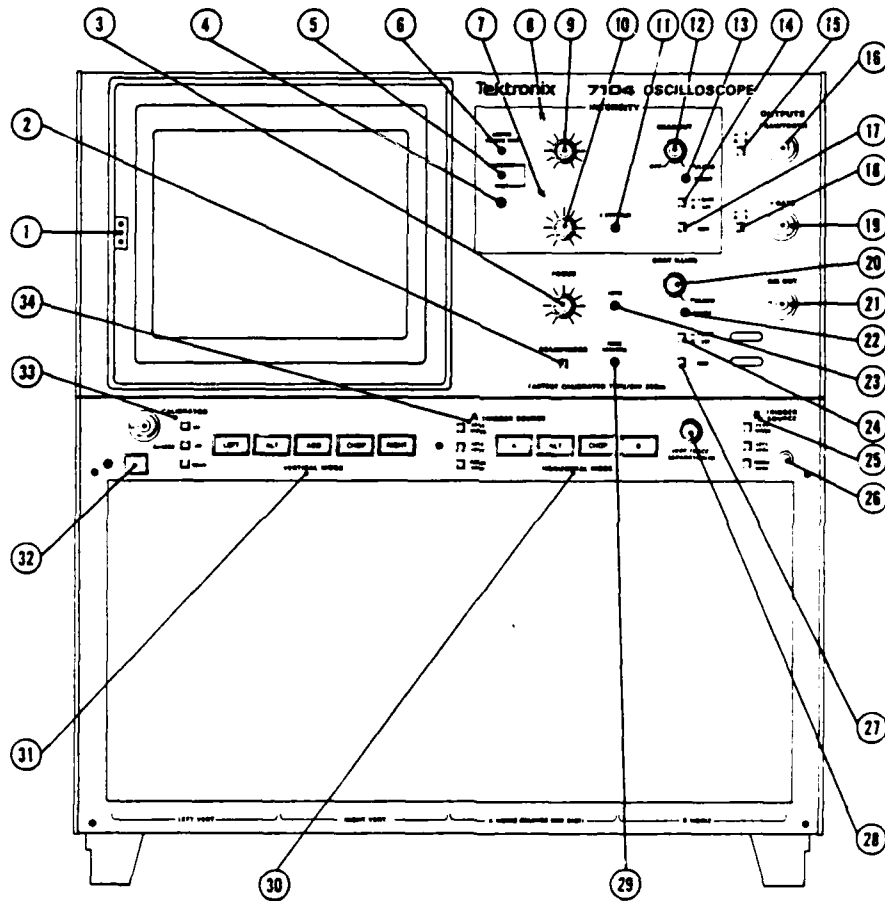


Figure 1. Front-panel Controls, Connections, and Indicators. (1:2-4)

- ① Camera Power Connector (not labeled)—Three-pin connector provides power for camera operation and receives single sweep-reset signal.
- ② BEAMFINDER—Switch when pressed compresses and defocuses display within graticule area.
- ③ FOCUS—Control optimizes crt trace definition.
- ④ RESET—Switch when pressed initiates another cycle of viewing time.
- ⑤ SHUTDOWN—Indicator to signal that crt display is off.
- ⑥ LIMITED VIEWING TIME—Indicator to signal that crt display shutdown will occur.
- ⑦ B INTENSITY—Indicator illuminates when selected by the HORIZONTAL MODE switch.
- ⑧ A INTENSITY—Indicator illuminates when selected by the HORIZONTAL MODE switch.
- ⑨ A INTENSITY—Control to determine brightness of trace produced by the plug-in unit installed in the A HORIZ compartment.
- ⑩ B INTENSITY—Control to determine brightness of trace produced by the plug-in unit installed in the B HORIZ compartment.
- ⑪ B CONTRAST—Control varies brightness of intensified portion of display.
- ⑫ READOUT INTENSITY—Control to determine brightness of readout display. Disables Readout System in counterclockwise detent position. Activates PULSE in clockwise detent position.
- ⑬ READOUT PRESET—Adjustment (PULSED operation only) sets PULSED readout intensity.
- ⑭ READOUT +GATE OR EXT—Switch to select either +GATE or EXT actuation of the PULSED readout mode.
- ⑮ A OR B +SAWTOOTH—Switch to select A or B time-base unit as source for +SAWTOOTH OUTPUT signal.
- ⑯ +SAWTOOTH—Connector to output signal derived from the A or B time-base unit.
- ⑰ READOUT MAN—Switch when pressed actuates one frame of readout display.
- ⑱ A OR B +GATE—Switch to select either A or B time-base unit as source of +GATE output.
- ⑲ +GATE—Connector to output positive-going gate signal from the time-base unit in the A or B horizontal compartment.
- ⑳ GRAT ILLUM—Control varies level of graticule illumination or activates PULSED GRAT ILLUM functions.
- ㉑ SIG OUT—Connector to output signal derived from vertical signal as selected by B TRIGGER SOURCE switch.
- ㉒ GRAT ILLUM PRESET—Screwdriver adjustment to vary level of graticule illumination in GRAT ILLUM PULSED mode.
- ㉓ ASTIG—Screwdriver adjustment used in conjunction with FOCUS control to obtain a well defined display.
- ㉔ GRAT ILLUM +GATE OR EXT—Switch to select between +GATE or EXT actuation of graticule illumination.
- ㉕ B TRIGGER SOURCE—Switches select internal trigger source for B HORIZ plug-in unit.
- ㉖ Ground (not labeled)—Binding post to establish common ground between associated equipment.
- ㉗ GRAT ILLUM MAN—Switch when pressed actuates one graticule illumination.
- ㉘ VERT TRACE SEPARATION (B)—Control vertically positions the B HORIZ trace with respect to the A HORIZ trace (dual-sweep only).
- ㉙ TRACE ROTATION—Screwdriver adjustment to align trace(s) with graticule lines.
- ㉚ HORIZONTAL MODE—Switches select input source for horizontal deflection.
- ㉛ VERTICAL MODE—Switches select source of input for vertical deflection.
- ㉜ POWER (Switch and Indicator)—Switch controls power to instrument; indicator illuminates when power is on.
- ㉝ CALIBRATOR—Switches select 4 V, 0.4 V, and 40 mV calibrated square-wave voltages at 1 kHz repetition rate at connector output.
- ㉞ A TRIGGER SOURCE—Switches select internal trigger source for A HORIZ plug-in unit.

Figure 2. Front-panel Controls, Connections, and Indicators Description. (1:2-5)

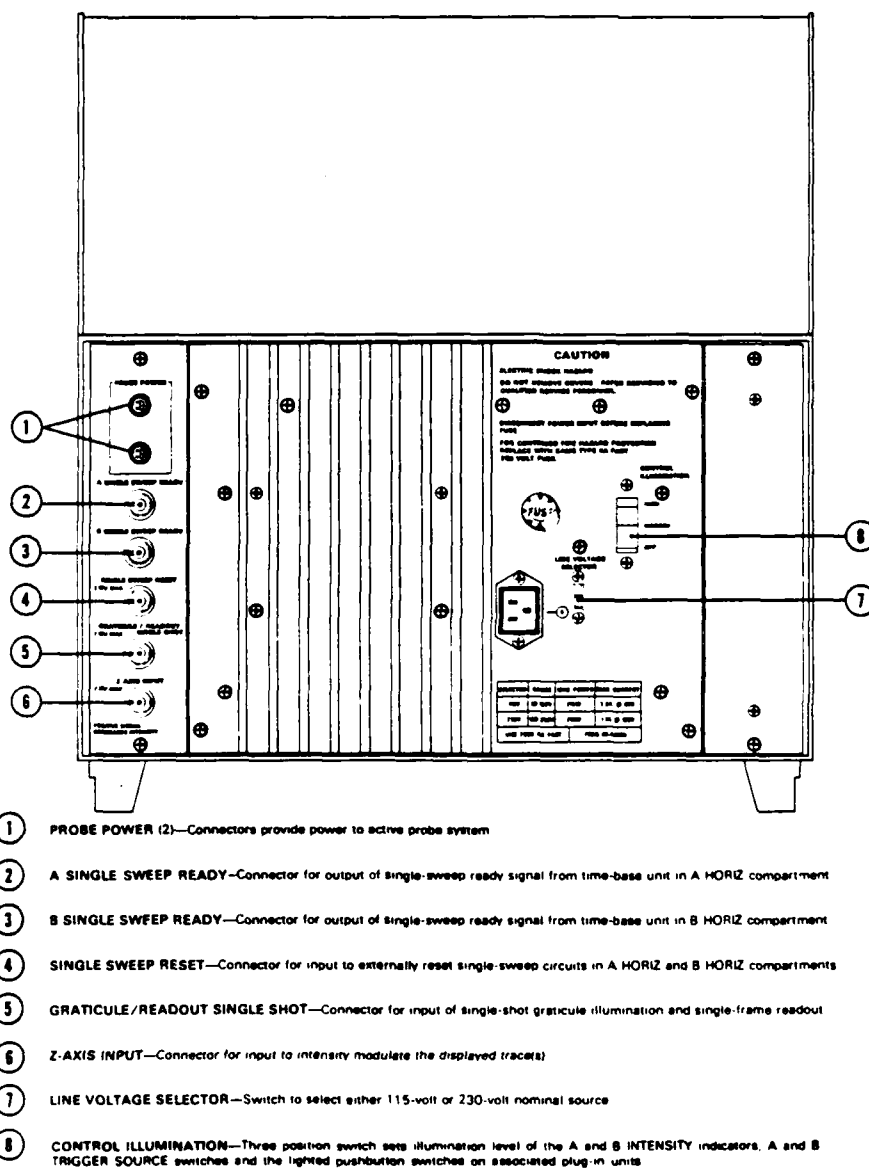


Figure 3. Rear-panel Controls and Connections with Description. (1:2-6)

Limited Viewing Time, Shutdown, and Reset

The 7104 has the feature of automatically reducing the display intensity when damage to the crt may result from sustained display. If the intensity is set high enough to cause damage to the crt, the display will automatically shutdown after a few minutes.

The LIMITED VIEWING TIME indicator shows how long the trace will remain on the display. The indicator has three modes of operation:

OFF	Trace remains on indefinitely.
ON	Trace will shut down in a few minutes.
FLASHING	Trace will shut down in about 1 minute.

Just before display shutdown, the red SHUTDOWN indicator will flash. Pressing the RESET button will keep the trace on the display and start the timing sequence again.

After display shutdown, the red SHUTDOWN indicator will be on continuously. Pressing the RESET button will turn the display back on and start the timing sequence again.

Readout Display

The readout display shows alphanumeric information about the settings of controls on the plug-in units. Figure 4 describes the location of the information on the display.

TEKTRONIX 7L5 SPECTRUM ANALYZER WITH L3 INPUT MODULE

The 7L5 Spectrum Analyzer can display the frequency spectrum of an input signal in the range of 0 Hz to 5 MHz. Figures 5 and 6 show the front panel controls of the 7L5 unit with some description about their functions. Appendix B contains the full description of each control.

L3 Input Module

The L3 input module matches the impedance of the test lead to prevent wave reflections that cause inaccurate amplitude measurements and degradation of performance. The impedances available are 1 M Ω , 600 Ω and 50 Ω . These are selected by the TERMN 2 switch on the L3 module. For the laboratory experiments, the 1 M Ω setting will be used.

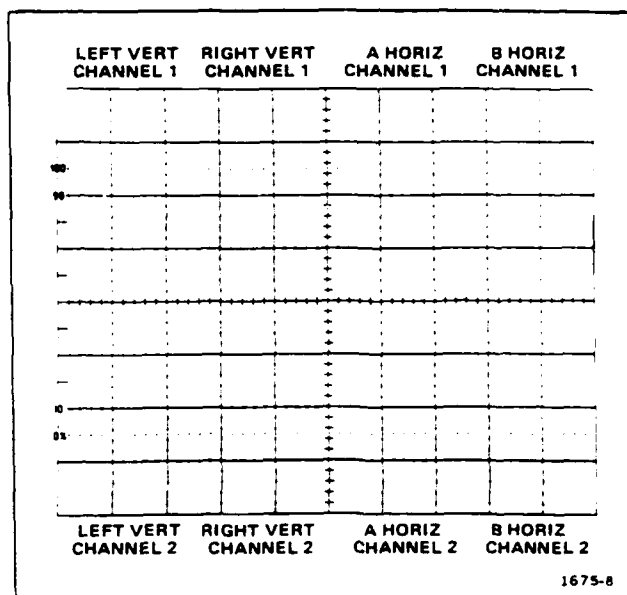


Figure 4. Locations of readout display information. (1:2-10)

CAUTION

Failure to keep input signals to the L3 module below maximum levels may result in damage to internal components.

The maximum input levels are stated according to the TERMN 2 setting on the L3 module.

1 Mohm/28 pF: 15 Vpp for ac or pulse signals with risetimes of 2 V/μsec or faster.
100 V (dc plus peak) with risetimes slower than 2 V/μsec.

600 ohm: 12 V (dc or rms).

50 ohm: 3.5 V (dc or rms).

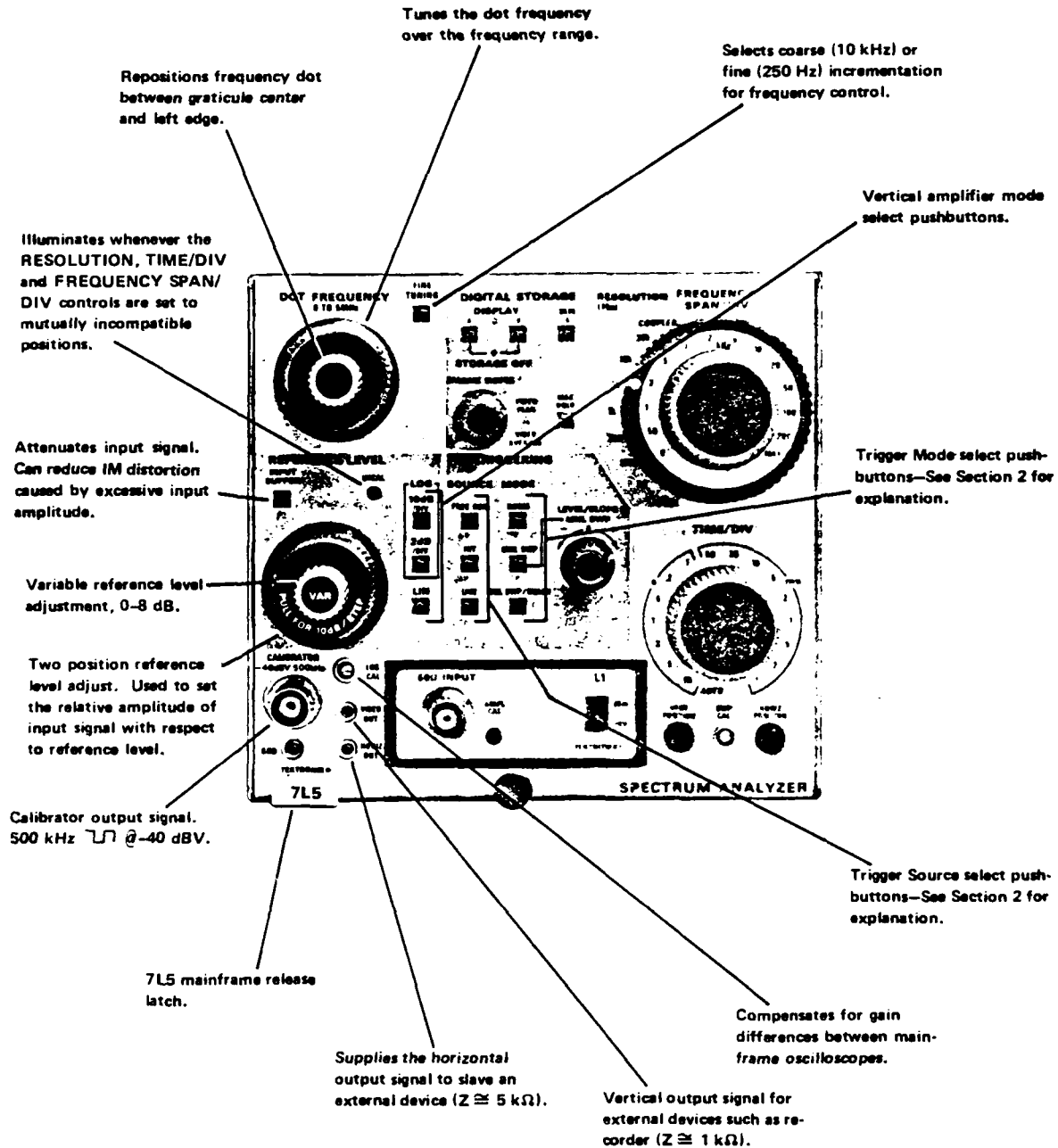


Figure 5. 7L5 Front Panel Controls and Connections with Description. (2:3-4)

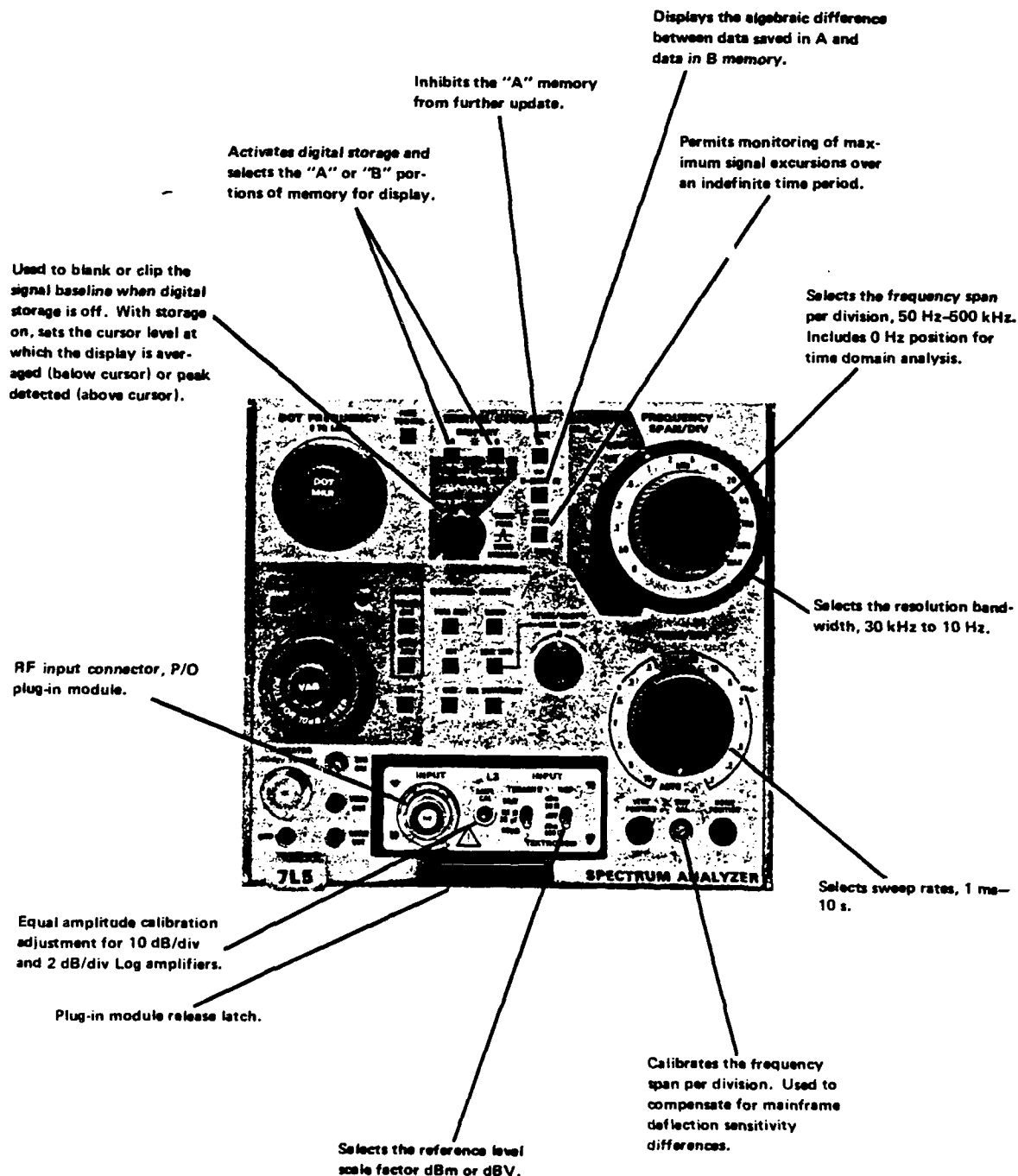


Figure 6. 7L5 Front Panel Controls and Connectors with Description. (2:3-5)

The INPUT REF control on the L3 module selects the scale factor for the reference level of the 7L5. There are three settings and the dBV (voltage expressed in decibels) setting will be used in the experiments.

Display Readout

The present position of controls on the 7L5 are indicated on the display. As the controls are changed, the readout on the display changes. Figure 7 shows the display.

The dot frequency and the reference level readouts are located near the top graticule (scale) line of the display. The dot frequency is suffixed by KHZ (500.00 KHZ in the figure) and the reference level is suffixed by dBV or dBm depending on the INPUT REF switch setting on the L3 module (-40 dBV in the figure).

The readouts located near the bottom graticule line show the vertical amplifier mode (10 dB/DIV, 2 dB/DIV, LIN), RESOLUTION, and FREQUENCY SPAN/DIV control settings. Figure 7 shows these settings at 2 dB/DIV, 3 kHz, and 2 kHz respectively.

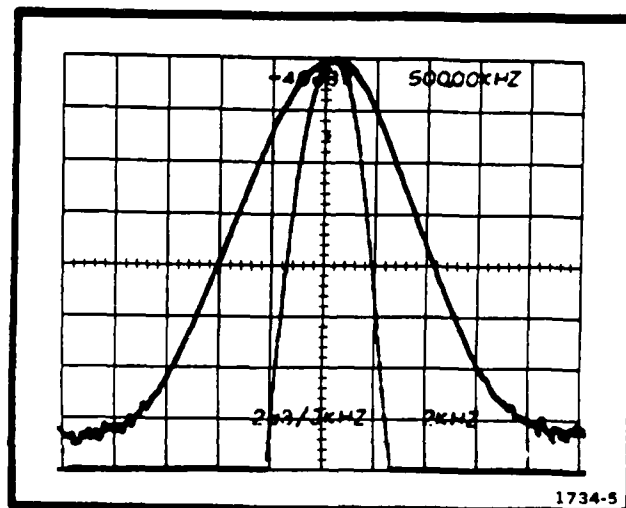


Figure 7. Display Readout. (2:3-8)

Dot Frequency

With the FINE TUNING pushbutton off, turning the DOT FREQUENCY knob changes the frequency setting in 10 kHz steps. With the FINE TUNING pushbutton on, turning the same knob changes the frequency in 0.25 kHz steps. The dot on the display shows the present horizontal frequency position of the dot frequency. This dot is stationary unless changed by the HORIZ control or the DOT FREQUENCY VAR control. When the dot frequency is changed, the spectrum moves relative to the dot on the display.

Reference Level and Amplitude Measurements

The reference level and vertical amplifier modes are used to measure spectral component amplitudes and get a good "picture" of the spectrum on the display.

There are three pushbuttons that determine the vertical amplifier mode (vertical scale). They are 10 dB/DIV, 2 dB/DIV and LIN (linear). The selection of the vertical amplifier modes determines how the REFERENCE LEVEL knob operates and how amplitude measurements are made.

The top graticule line is known as the reference level and the REFERENCE LEVEL knob changes the amplitude value of this top line.

When the vertical amplifier is in one of the dBV/DIV settings, the knob changes the reference level in two different increments. With the knob pulled out, the reference level can be changed in 10 dB steps. When the knob is pushed in, the reference level is changed in 1 dB steps. The amplitudes of spectral components are measured down from the top graticule line value (reference level) taking into account the vertical amplifier mode. The trace baseline must be set even with the bottom graticule line and the VAR control on the REFERENCE LEVEL knob must be fully ccw to make accurate measurements.

When the vertical amplifier mode is in the LIN (linear) mode, amplitude measurements are made with reference to the trace baseline. The voltage level indicated by the reference level readout on the display is the vertical voltage per division.

It is important to use the BASELINE CLIPPER (Peak/Average) control dial when measuring amplitudes. The BASELINE CLIPPER control moves a horizontal line (cursor) up and down the display. When digital storage is used (i.e. DISPLAY A and/or DISPLAY B on), the area above the cursor is peak detected and the area below is averaged. Therefore to measure the peak of a spectral component, the cursor should be placed no less than 1/4 division below the peak. To average noise, the cursor should be placed no less than 1/4 division above the noise level.

The INPUT BUFFER is also important when making amplitude measurements. If the impedance is not perfectly matched by the L3 plug-in module, the INPUT BUFFER can improve the plug-in swr and allow more accurate measurements.

Resolution, Frequency Span/Div, and Time/Div

The resolution of the spectrum analyzer refers to the analyzer's ability to display adjacent signal responses discretely. As the resolution bandwidth is decreased by the RESOLUTION control, the spectral components will be narrowed and adjacent components will become more apparent. The sensitivity and signal-to-noise ratio will also improve.

The FREQUENCY SPAN/DIV control adjusts the horizontal scale of the display. Increasing this control will allow more spectral components of a signal to be displayed.

The TIME/DIV control sets the sampling time of the analyzer. Higher resolution will require slower sampling time thus a greater TIME/DIV setting.

With high resolution (low resolution bandwidth), the span time must be reduced accordingly to keep the analyzer in calibration. If the UNCAL light is illuminated while adjusting the RESOLUTION, FREQUENCY SPAN/DIV, and TIME/DIV controls, the settings are not compatible. Usually the TIME/DIV must be decreased until the UNCAL light goes out.

For most applications, the RESOLUTION and TIME/DIV should be set at COUPLED and AUTO respectively. This provides automatic setting for best sweep rate and resolution bandwidth along with maximum accuracy when measuring amplitudes.

Digital Storage

The 7L5 can digitally store two separate signal spectrums and allow comparisons to be made.

This is done by turning DISPLAY A on and adjusting the 7L5 controls to observe a signal spectrum. This signal spectrum is stored and inhibited from updating by pressing the SAVE A push-button.

A second signal spectrum can be viewed by turning off the DISPLAY A pushbutton and activating the DISPLAY B pushbutton. Controls can be changed to observe the second signal but when comparisons are made, the first signal's "picture" is not adjusted according to the new control settings. It simply overlays the second signal on the display. Therefore the controls should not be adjusted, if possible, when comparisons are to be made.

To compare the "B" signal to the stored "A" signal, both DISPLAY A and DISPLAY B must be on without deactivating the SAVE A pushbutton. Both signals will appear on the display as long as the SAVE A control is on.

Another feature of the digital storage is the MAX HOLD pushbutton. When this pushbutton is activated, the digital storage and display will only be updated if the amplitude of the signal is increased. No change will occur if the amplitude decreases. This feature is useful, for example, when tracing the frequency response of an amplifier or circuit. With the spectrum analyzer attached to the output of the circuit, turning MAX HOLD on and varying the circuit input frequency, the frequency response of the circuit is traced on the display.

Triggering

The FREE RUN and NORM pushbuttons are used for normal display of a signal spectrum. The LINE pushbutton is used for triggering off the line voltage. The INT pushbutton allows triggering from the left or right vertical sources.

The SGL SWP/READY (Single Sweep/Ready) pushbutton allows for single sweep triggering. The MNL SWEEP (manually controlled sweep) allows manual sweeping using the MNL SWP knob. A dot on the cursor line moves across the display indicating the present position of updated information.

HEWLETT-PACKARD 5248M ELECTRONIC COUNTER

This electronic counter is used as a frequency counter in the laboratory. To be used as such, the FUNCTION dial is set in the FREQUENCY mode. The TIME BASE dial is used to control the gate time when sampling the input signal. This dial also controls the position of the decimal point on the display. For most signal inputs, the SELECTIVITY switch should remain in the 0.1 setting.

WAVETEK MODEL 148 AM/FM/PM GENERATOR

This generator will be the chief source of signals in the laboratory. It can produce continuous waves along with AM, FM, and PM modulated signals. The message signal for the various types of modulation can be generated internally or externally. The following material was extracted from the Wavetek Model 148 20 MHz AM/FM/PM Generator Instruction Manual. (4:3-1 to 3-6)

Front Panel Controls and Connectors

The front panel controls are shown in figure 8.

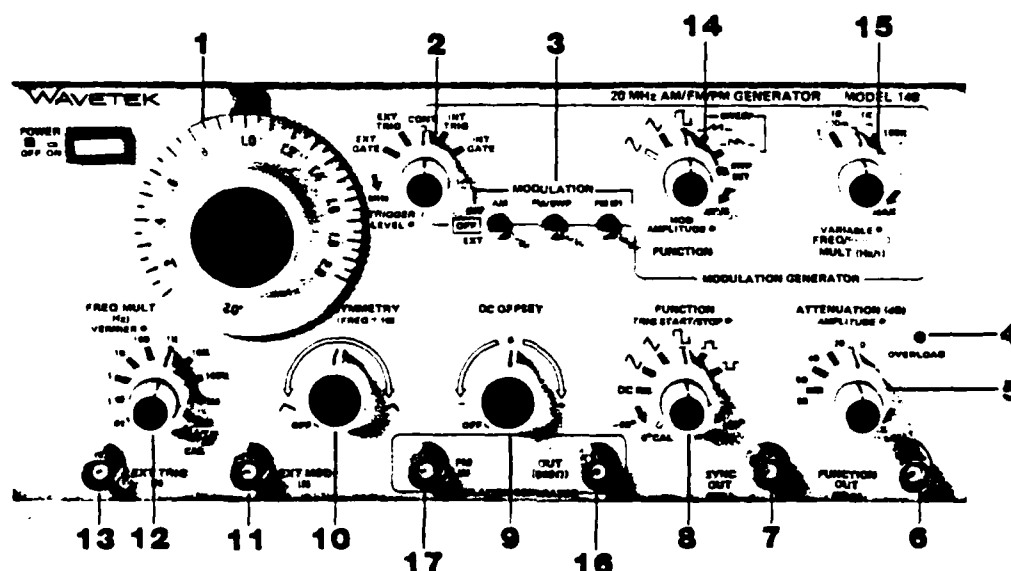


Figure 8. Wavetek Model 148 Generator Controls and Connectors. (4:3-1)

Main Generator:

- 1 Frequency Dial - This dial setting multiplied by the FREQ MULT (12) sets the main generator frequency of the signal at FUNCTION OUT (6). This frequency may be varied slightly by the FREQ VERNIER (12) and, in some cases, by the modulation generator.
- 2 Mode Switch - The outer switch selects the operating mode of the generator. It will be set in the CONT (continuous) mode for normal operation in the laboratory. The other settings are described in the Wavetek Model 148 Instruction Manual located in the laboratory. The Trigger Level control should be set in the 12 o'clock position for CONT operation.
- 3 MODULATION Switches - These three switches (AM, FM/SWP, and PM) set the type of modulation of the main generator. They also select the source of modulation signals. The signal attached to the EXT MOD IN (11) connector is used as the modulating signal for the EXT (external) switch setting. When the AM switch is in the INT (internal) mode, the generator amplitude (carrier) is reduced to 50% of the normal amplitude to prevent over-modulation. When the AM switch is in the external mode, the generator amplitude is zero to allow for suppressed carrier (DSB-SC) operation.
- 4 OVERLOAD Indicator - This LED lights if ± 7.5 peak voltage into 50 ohms is exceeded.
- 5 ATTENUATION Switch - This switch attenuates the signal at FUNCTION OUT (6) and the inner AMPLITUDE control adjusts the signal attenuation between the two values selected by the ATTENUATION switch.
- 6 FUNCTION OUT (50 ohm) Connector - The main generator waveform is obtained from this connector.
- 7 SYNC OUT (TTL) Connector - A TTL pulse at the main generator frequency is available at this connector.
- 8 FUNCTION Switch - This switch selects the primary waveform output of the main generator at the FUNCTION OUT (6) connector. The TRIG START/STOP control is not used in the laboratory but is described in the Wavetek Model 148 Instruction Manual.

- 9 DC OFFSET Control - This controls the dc offset of the main generator signal and is usually kept in the OFF position.
- 10 SYMMETRY Control - This controls the symmetry of the main generator waveform. It is kept in the OFF position for experiments in the laboratory.
- 11 EXT MOD IN Connector - The signal applied to this connector becomes the modulation source when a MODULATION switch (3) is in the EXT position.
- 12 FREQUENCY MULT Switch - The outer switch selects the frequency multiplier for the frequency dial (1). The VERNIER control allows fine adjustment of the main generator frequency.
- 13 EXT TRIG IN Connector - This connector is not used in the experiments but is described in the Wavetek Model 148 Instruction Manual.

Modulation Generator:

- 14 FUNCTION Switch - This switch selects the waveform output of the modulation generator. The modulating signal is available at the OUT (600 ohm) connector (16) at a fixed amplitude of 10 Vpp. A SWP SET detent holds this OUT (600 ohm) connector at a dc level corresponding to the MOD AMPLITUDE (14) level and is used to set the upper sweep frequency for FM internal modulation. The MOD AMPLITUDE control attenuates the modulation generator signal that is internally fed to the main generator when modulating.
- 15 FREQ/PERIOD MULT Switch - The outer switch sets the internal modulation source frequency range and is denoted in frequency and period. The VARIABLE control fine tunes this modulation frequency within the selected frequency range.
- 16 OUT (600 ohm) Connector - This connector is the modulation generator output at a fixed amplitude of 10 Vpp, except when the FUNCTION switch (14) is set in the SWP SET position.
- 17 FM IN Connector - This connector is the input for frequency modulation of the modulation generator. Sensitivity is 20% of the frequency range per volt input.

Operation

The generator can perform seven basic types of operation. They are Continuous, Triggered, Gated, AM, FM, PM and DC. Only the Continuous, AM, FM and PM types will be discussed below. The Wavetek Model 148 Instruction Manual contains a full discussion of the other modes.

Continuous Operation:

In continuous operation, a continuous, unmodulated waveform is generated and available at the FUNCTION OUT connector. The MODULATION switches must be set to their OFF positions and the mode set to CONT. The main generator signal, set by its frequency dials, function selectors, and attenuation controls, is the continuous wave that appears at FUNCTION OUT. Settings of the modulation generator have no effect on the output in the continuous, unmodulated mode.

AM Operation:

For AM Operation, the instantaneous amplitude of the signal varies with the modulation amplitude. The AM MODULATION Switch must be selected for INT or EXT and the other MODULATION Switches set to OFF. The mode must also be CONT.

Internal Modulation - Internal modulation is generated by the modulation generator. A conventional AM signal is produced and obtained from FUNCTION OUT. The carrier (main generator signal) amplitude is reduced by half to prevent clipping of the AM signal. The modulating frequency should always be set less than the carrier frequency. The MOD AMPLITUDE dial controls the modulation signal amplitude and thus the modulation index of the AM signal.

External Modulation - When in the External AM Modulation mode, the Wavetek generator can create conventional AM (with carrier component) or Double-Sideband Suppressed Carrier (without carrier component). With the DC Offset OFF, DSB-SC will be generated. The DC Offset may be adjusted to give power to the carrier for conventional AM operation. The modulating signal must be supplied to the EXT MOD IN connector. For best performance, the external modulating signal should have an amplitude close to, but not to exceed, 5 Vp. The main generator ATTENUATION and AMPLITUDE should then be used to adjust the signal to the desired amplitude.

FM Operation:

In this mode, the instantaneous frequency of the output signal varies with the instantaneous amplitude of the modulation signal.

NOTE

The output frequency modulation will not be linear when the instantaneous modulated frequency exceeds the following ranges:

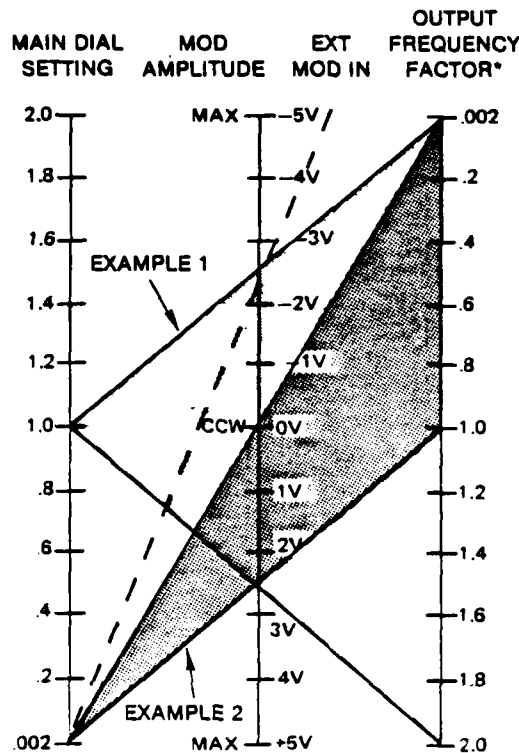
Upper Limit: $2.0 \times \text{Main Generator FREQ MULT}$
Lower Limit: $0.001 \times \text{Upper Limit}$

For FM operation, the FM MODULATION switch must be set in the INT or EXT positions and the other MODULATION switches set to OFF. The mode must also be set to CONT. For external modulation, the modulation source signal must be supplied to EXT MOD IN. The main generator frequency setting will be the center frequency from which the modulated signal will vary.

Care must be taken to prevent the modulating signal from driving the output frequency beyond its limits. When in the INT mode, the modulating frequency is set by the FREQ/PERIOD MULT switch and VARIABLE control. This frequency must be within the ranges specified above.

Figure 9 shows an example of keeping within the main generator frequency limits. The main generator is limited in frequency range by approximately the dial range for any given multiplier setting. Example 1 in the figure shows the MAIN DIAL SETTING at 1.0. This is the desired setting for a balanced modulating signal such as a sine wave. Note that to stay within the OUTPUT FREQUENCY FACTOR range, the MOD AMPLITUDE or EXT MOD IN cannot exceed certain values. If these amplitudes are exceeded, the output signal frequency will not be linear.

The SWP SET mode allows for precise setting of the upper frequency limit. To set the upper frequency limit, the mode must be SWP SET and the main generator frequency dial set for the center frequency (usually $1.0 \times \text{FREQ MULT}$ for



*Multiply by FREQ MULT for actual output.

Figure 9. Frequency Modulation Nomograph. (4:3-5)

balanced waveforms). The FUNCTION OUT can be monitored with a frequency counter and the modulation amplitude, either external or internal, is then adjusted to set the upper frequency limit. The modulating signal then should not exceed this maximum amplitude.

The Sweep Operation is used to linearly sweep the main generator frequency. The sweep modulation functions are  and  for sweep up or sweep down respectively. These signals have double the frequency of the FREQ/PERIOD control. Example 2 in figure 9 shows a sweep up operation using the  modulation function. The main generator frequency dial is set fully cw and the VERNIER is set fully ccw for minimum center frequency. The MOD AMPLITUDE control is set at midrange. Notice the positive sweeping is from

0.002 to 1.0 on the OUTPUT FREQUENCY FACTOR scale. The dashed line shows what would happen if a balanced modulating signal, such as a sine wave, were used. Any negative amplitudes would drive the output frequency below its lower limit.

PM Operation:

In this mode, the instantaneous phase of the output signal varies with the instantaneous change in amplitude of the modulating signal. The frequency of the generator is changed until the correct phase angle is obtained.

Nominally, the phase of the main generator is shifted by 10 degrees for each volt of the instantaneous modulation signal amplitude. The main generator dial should not be set above midpoint (1.0) to prevent roll-off due to the internal differentiator circuit. Also, there is no PM operation for main generator frequency multiplier settings of 100 or less. The full input range is 5 Vp thus allowing a maximum phase shift of 50 degrees in either direction from zero degrees.

NOTE

The output phase will not be linear when the instantaneous transition frequencies required to effect the phase change exceeds the following ranges:

Upper Limit: $2.0 \times \text{Main Generator FREQ MULT}$
Lower Limit: $0.001 \times \text{Upper Limit}$

PROCEDURE

The following describes the procedure to familiarize use of the test equipment. Freely adjust the various front panel controls to observe their effect. Damage to equipment will not result from any front panel controls as long as maximum input levels, as described previously, are not exceeded.

Turn all of the equipment on. The 7LS unit in the 7104 Oscilloscope requires a 10 minute warm-up period before accurate measurements can be made.

Use of the 7104 Oscilloscope and 7L5 Spectrum Analyzer

Objective: To familiarize use of the 7104 Oscilloscope and 7L5 Spectrum Analyzer.

Set-up:

1. Connect a test lead from the FUNCTION OUT connector on the Wavetek Model 148 Generator to one of the vertical amplifier channels of the 7104 Oscilloscope. Also connect the frequency counter to this signal.

CAUTION

To prevent damage to the 7L5 Spectrum Analyzer, do not connect anything to its input at this time.

2. Set the 7104 front panel controls to display the time-domain trace of the signal attached to the vertical amplifier:

7104 Controls:

Vertical Mode	LEFT
Horizontal Mode	B

3. Adjust the Wavetek main generator signal using the oscilloscope and frequency counter:

Wavetek Controls:

FUNCTION	Sine Wave
MODULATION Switches	OFF
ATTENUATION and AMPLITUDE	Obtain 1 Vpp on scope
Frequency Dial, FREQ MULT and VERNIER	Obtain 10 kHz on frequency counter

4. Connect the signal to the L3 INPUT connector on the 7L5 Spectrum Analyzer.
5. Adjust the 7104 controls to observe the spectrum of the input signal:

7104 Controls:

Vertical Mode	RIGHT
Horizontal Mode	A

6. Adjust the spectrum analyzer controls:

L3 Input Module Controls:

INPUT TRMN Z	1 M Ω /28 pF
INPUT REF	dBV

7L5 Controls:

DOT MARKER	max ccw (detent position)
DOT FREQUENCY	0 kHz
DISPLAY A	on
DISPLAY B	on
SAVE A	off
B-(SAVE A)	off
MAX HOLD	off
BASELINE CLIPPER	max cw
RESOLUTION	COUPLED
FREQUENCY SPAN/DIV	5 kHz
INPUT BUFFER	off
REFERENCE LEVEL	-10 dBV
VAR	max ccw (detent position)
10 dB/DIV	on
SOURCE	FREE RUN
MODE	NORM
TIME/DIV	AUTO
VERT POSITION	So Baseline is on bottom graticule
HORIZ POSITION	So Dot Marker is on center vertical graticule

Description of Display Traces:

1. The trace on the display is the spectrum of the input signal.
2. There are frequency components at 0, 10 and 20 kHz.
 - a. The 0 kHz component is inherent from the spectrum analyzer mixer stage. Therefore the dc component of any input signal cannot be accurately measured.
 - b. The 10 kHz component is the main component from the input signal.
 - c. The 20 kHz component is a secondary component caused by the sampling window of the spectrum analyzer. the component is not actually present in the input signal.

Resolution Adjustment:

1. Reduce the RESOLUTION control on the 7L5 unit from its COUPLED setting down to a point just above the position where the analyzer UNCAL light next to the REFERENCE LEVEL knob comes on.
2. Notice the spectral components begin to approach impulse functions and the sweep rate is reduced. The TIME SPAN/DIV is automatically increased as long as the control is in the AUTO position.
3. Vary the TIME SPAN/DIV, FREQ SPAN/DIV and RESOLUTION controls to change the display of the spectrum. When the UNCAL light comes on, one or more of these controls must be adjusted slightly to keep the trace in calibration.

Dot Frequency:

1. Return the 7L5 controls to their initial positions as described in the Set-up step 6 above.
2. Adjust the DOT FREQUENCY to 10 kHz and notice the movement of the spectrum displayed. The 10 kHz component will be centered on the dot in the middle of the display.
3. Change the input frequency on the Wavetek generator to about 12.5 kHz. Using the FINE TUNING button and the DOT FREQUENCY knob, adjust the DOT FREQUENCY to 12.5 kHz. The 12.5 kHz component is now centered on the display.

Reference Level and Amplitude Measurement:

1. Set the reference level to -15 dBV by using the REFERENCE LEVEL knob in the pushed-in (1 dB increments) and pulled-out (10 dB increments) modes. Notice the peak of the spectral component exceeds the top graticule line.
2. Adjust the cursor (Baseline Clipper) to midway between the peak and baseline.
3. Set the vertical amplifier mode from 10 dB/DIV to 2 dB/DIV. Adjust the reference level so the 12.5 kHz peak is on or just below the top graticule line.

4. Measure the amplitude of the peak with reference to the top graticule line (the reference level). If the peak is directly on the top line, then its amplitude is the reference level value. If the peak is below the top line, then the amplitude is the reference level value minus the distance down to the peak (remembering 2 dB/DIV).
5. Change the L3 unit TERMN Z switch to change the matching impedance. Notice how the peak amplitude changes.
6. Reset the TERMN Z switch to 1 M Ω /28 pF.

Digital Storage and Waveform Comparisons:

1. Make sure DISPLAY A and DISPLAY B are on.
2. Set the DOT FREQUENCY to 12.5 kHz, FREQ SPAN/DIV to 1 kHz and REFERENCE LEVEL to -6 dBV.
3. Change the input signal frequency to about 15 kHz.
4. Turn on SAVE A. This 15 kHz spectral component is now the stored "A" signal.
5. Turn off DISPLAY A.
6. Change the input signal frequency to about 10 kHz. This spectral component is the "B" signal.
7. Turn on DISPLAY A and notice the 15 kHz component appear. This component is saved in memory as long as the SAVE A button is on, thus allowing comparisons to other signals.
8. Change the FREQ SPAN/DIV to 2 kHz and notice only the "B" signal is affected on the display. Return the switch back to 1 kHz.
9. Turn on MAX HOLD and increase the input signal amplitude slightly. The "B" signal amplitude will increase but the "A" signal will be unchanged.
10. Decrease the input signal amplitude and notice the "B" signal amplitude does not drop. The amplitude is held at a maximum level until the MAX HOLD is turned off.

11. Turn off MAX HOLD and the 10 kHz component will drop to the proper input level. Also turn off SAVE A and the "A" signal will disappear.

Measuring the Frequency Response of a Filter:

1. Connect the low pass filter on a proto-board as shown in figure 10.
2. Set the Wavetek FUNCTION OUT signal to 1 Vpp sine wave using the oscilloscope. The frequency should be roughly 1 kHz.
3. Connect this FUNCTION OUT signal to the input 220 Ω resistor as shown in figure 10.

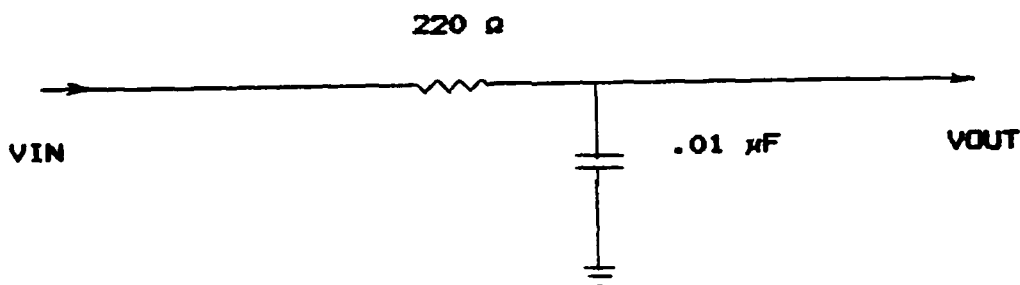


Figure 10. RC Lowpass Filter.

4. Connect the output of the filter in figure 10 to the spectrum analyzer and adjust the analyzer to the following settings:

DOT MARKER	max ccw (detent position)
DOT FREQUENCY	30 kHz
DISPLAY A	on
DISPLAY B	on
SAVE A	off
B-(SAVE A)	off
MAX HOLD	off
BASELINE CLIPPER	to center the cursor line
RESOLUTION	COUPLED
FREQUENCY SPAN/DIV	10 kHz
INPUT BUFFER	off
REFERENCE LEVEL	-8 dbV

VAR	max ccw (detent position)
2 dB/DIV	on
SOURCE	FREE RUN
MODE	NORM
TIME/DIV	AUTO
VERT POSITION	So Baseline is on bottom graticule
HORIZ POSITION	So Dot Marker is on center vertical graticule

5. Turn on MAX HOLD and vary the input signal frequency slowly between 0 and 80 kHz so the component peak starts to "trace" the filter frequency response across the display. Press SAVE A to store this waveform and then turn off MAX HOLD.
6. Adjust the input frequency to the 3 dBV point (half power point) by watching the spectral peak move across the display as the frequency is changed. Measure the input frequency with a frequency counter. This 3 dB point should be about 72.3 kHz (454.5 kradians/sec).
7. Turn off SAVE A to clear the display.

Use of the Wavetek Model 148 AM/FM/PM Generator

Objective: To familiarize use of the Wavetek Signal Generator.

AM Internal Modulation:

1. With all generator MODULATION switches OFF, adjust the main generator to a 1 Vpp, 500 kHz sine wave using the oscilloscope and frequency counter.
2. Set the AM MODULATION switch to INT and modulation generator mode to a sine wave.
3. Adjust the FREQ/PERIOD MULT to the setting between 1 kHz and 100 kHz. Connect only the frequency counter to the Wavetek OUT (600 ohm) connector and use the VARIABLE control to set the modulation frequency to 10 kHz.
4. Observe the AM waveform from FUNCTION OUT on the oscilloscope and adjust the percent modulation to about 30% by varying the MOD AMPLITUDE vernier.

5. Connect the FUNCTION OUT to the 7L5 INPUT. Adjust the DOT FREQUENCY to 500 kHz, use 10 dB/DIV vertical amplifier mode and set the REFERENCE LEVEL so the carrier component peak is near the reference level. Adjust the FREQ SPAN/DIV to a setting where the two modulation spectral components are in view.
6. Vary the following AM signal parameters noticing how the spectrum changes:
 - Carrier Frequency - use main generator frequency dial.
 - Carrier Amplitude - use main generator AMPLITUDE dial.
 - Modulation Frequency - use FREQ/PERIOD MULT VARIABLE dial.
 - Modulation Amplitude - use MOD AMPLITUDE dial.

AM External Modulation:

1. Turn off the MODULATION switches and reset the carrier frequency to 500 kHz using the frequency counter. Then set the AM MODULATION switch to EXT.
2. Use a second Wavetek Model 148 AM/FM/PM Generator and create a 1 Vpp, 10 kHz, sine wave at FUNCTION OUT with no modulation.
3. Connect FUNCTION OUT of this second generator (modulation source) to EXT MOD IN of the first generator (modulating generator).
4. Make sure the DC OFFSETs on both generators are OFF and connect the FUNCTION OUT signal of the modulating generator to the spectrum analyzer and oscilloscope.
5. Examine the time domain trace on the oscilloscope showing a suppressed carrier (DSB-SC) waveform. Vary the modulation source amplitude and notice a change in the waveform.
6. Set up the spectrum analyzer at 500 kHz and observe the signal's spectrum. The carrier component at 500 kHz is reduced and is overpowered by the modulation sidebands.

FM Internal Modulation:

1. With all MODULATION switches OFF, generate a 1 MHz, 1 Vpp sine wave at FUNCTION OUT measured with the oscilloscope and frequency counter.
2. Connect the frequency counter to the OUT (600 Ω) connector.
3. Set the FM/SWP MODULATION switch to INT and the modulation FUNCTION to SWP SET. Turn the MOD AMPLITUDE fully ccw.
4. The frequency counter should read about 1 MHz. Increase the MOD AMPLITUDE until the frequency counter reads 2 MHz. The MOD AMPLITUDE dial should be in the 12 o'clock position.
5. Set the modulation FUNCTION to a square wave and adjust the modulation FREQ/MULT and VARIABLE until the frequency counter attached to OUT (600 ohm) reads 10 kHz.
6. Connect the spectrum analyzer to the FUNCTION OUT signal. Set up the spectrum analyzer controls for a REFERENCE LEVEL of -8 dBV, DOT FREQUENCY of 1000 kHz and FREQ SPAN/DIV of 200 kHz.
7. Observe the frequency spectrum on the display. Since the modulation signal is a square wave, most of the power is located at 0 Hz and 2 MHz. This corresponds to frequency modulating the positive and negative amplitudes of the square wave.
8. Decrease the MOD AMPLITUDE and notice both peaks moving toward 1 MHz. Decrease MOD AMPLITUDE until the peaks are at 600 kHz and 1400 kHz.
9. Switch the modulation FUNCTION to a sine wave. Notice that the spectrum of the FM signal flattens out with smaller peaks at 600 kHz and 1400 kHz.
10. Try a triangular modulation and observe the spectrum.

FM External Modulation:

1. Generate a 10 kHz, 1 Vpp, no dc offset square wave at the FUNCTION OUT of a different Wavetek Generator. Use the frequency counter and oscilloscope. This signal

will be used to externally modulate the first Wavetek Generator.

2. Connect the modulation source FUNCTION OUT to the EXT MOD IN of the first generator (modulating generator).
3. Set the modulating generator FM/SWP to EXT.
4. Observe the spectrum of the FUNCTION OUT signal of the modulating generator. There are spectral peaks at about 800 kHz and 1200 kHz.
5. Apply a DC OFFSET to the modulation source generator but not to the modulating generator. The entire frequency spectrum of the FM signal should move across the display.
6. Turn off the DC OFFSET and observe the FM signal on the oscilloscope. Set the oscilloscope time base to 500 ns.
7. Notice two dominant sine waves on the display. One is at about 800 kHz and the other at about 1200 kHz. These sine waves correspond to the peaks observed on the spectrum analyzer and result from frequency modulating the positive and negative voltage levels of the square wave.
8. Switch the modulation source to a sine wave. Decrease the source amplitude until the familiar FM time-domain signal is obtained.

APPENDIX A

INSTALLATION AND REMOVAL OF 7104 PLUG-IN UNITS

The following is a description of the installation and removal of plug-in modules for the Tektronix 7104 Oscilloscope.

CAUTION

Damage will result to the Oscilloscope and plug-in unit if the power is not turned off prior to installation or removal of a plug-in unit.

INSTALLATION

1. Make certain the 7104 power is off.
2. Check and remove any foreign objects from the desired plug-in compartment.
3. Align the slots on the top and bottom of the plug-in unit with the guide rails of the desired plug-in compartment. Slide the plug-in unit gently down the rails and press firmly and evenly on the unit's front face until the front face is flush with the 7104 housing face. The unit will lock into place.

REMOVAL

1. Make certain the 7104 power is off.
2. Pull the release latch marked with the plug-in unit number. This will unlock the unit from the 7104 compartment.
3. Slide the plug-in unit out carefully.

SPECIAL NOTE

If any compartments are unused in the 7104, an EMC shielded blank plug-in panel should be installed in each empty compartment. This will minimize electromagnetic interference.

APPENDIX B

DESCRIPTION OF 7L5 SPECTRUM ANALYZER CONTROLS,
INDICATORS, AND CONNECTORS

Operating Instructions—7L5 Operators

FRONT PANEL CONTROLS AND
CONNECTORS

Pushing any front panel pushbutton switch activates a bistable electronic circuit to change its output state. When in the active state, the plastic pushbutton is illuminated. Pressing the pushbutton a second time changes the output of the circuit to the inactive state and extinguishes the illuminated button.

Front panel controls also include two special photo-optic switch assemblies, the FREQUENCY SPAN/DIV-RESOLUTION switch and the TIME/DIV switch. Designed especially for the 7L5, each assembly is a mechanical/photo-electric, digital switch, that provides a TTL compatible five-bit binary output. The reliability of these switches has been demonstrated and with normal use they should last the life of the instrument. Dismantling or field repair of these switches is discouraged since their proper operation requires precision alignment of their internal components. If either switch assembly is damaged or suspected of malfunction, it should be replaced as an assembly.

The following describes the function of the front panel selectors for the 7L5. A layout of the front panel is shown in Fig. 3-2.

DOT FREQUENCY Changes the dot (marker) frequency in coarse (10 kHz) or fine (250 Hz) steps over the input frequency range of 0 Hz to 5 MHz. The frequency of the dot marker is displayed on the crt readout in the upper right set of characters. Dot frequency will not extend beyond the 7L5 frequency range, even if the control is rotated. When power is applied, dot frequency starts at 0.000.

FINE TUNING Selects coarse or fine incrementation for the DOT FREQUENCY control. When the FINE TUNING switch is activated (illuminated), each rotational click of the DOT FREQUENCY control changes the dot frequency in increments of 250 Hz. When the FINE TUNING switch is inactive (extinguished), each rotational click of the DOT FREQUENCY control changes the dot frequency in increments of 10 kHz.

DOT MKR

Used to horizontally position the frequency dot. The displayed frequency readout characters enumerate the actual frequency of the dot. When the DOT MKR control is in its detent position (fully ccw), the frequency dot and the selected frequency are on the vertical center line of the graticule. The 7L5 can be operated in a start sweep mode when the frequency dot is positioned to the left vertical graticule line. The DOT MKR control is disabled when the FREQUENCY SPAN/DIV switch is at MAX.

**REFERENCE
LEVEL**

Sets the full screen signal amplitude level (dBm, dBV) required at the INPUT to the plug-in module. This level is relevant to the input impedance of the plug-in module. Reference level is associated to the top graticule line of the display area and signal level is relative to this reference. The reference level range depends on the plug-in module, however, in the 2 dB/Div mode it covers 149 dB, in the 10 dB/Div mode the range is 90 dB and in the Lin mode 20 nV/div to 200 mV/div. The control has two speeds or stepping increments; pulled out, each increment is 10 dB, pushed in each increment is 1 dB or in some cases (dependent on the plug-in module) 2 dB.

VAR

The VAR (variable) control provides 8 dB or more gain adjustment between each calibrated reference level step. A < symbol is displayed on the crt, preceding the reference level readout, whenever the reference level is not calibrated (VAR is not in its detent position).

INPUT BUFFER

The active (illuminated) state of this pushbutton switch inserts 8 dB of signal attenuation at the input of the first mixer and adds 8 dB of vertical gain (after the variable resolution filters). When used, it reduces intermodulation distortion caused by excessive input signal amplitude. Because of its increased gain, the noise figure is increased 8 dB when this switch is activated.

Operating Instructions—7L5 Operators

LOG 10 dB/DIV	The illuminated condition of this pushbutton selects a logarithmic display of 10 dB/div with a dynamic range of 80 dB.
LOG 2 dB/DIV	The illuminated condition of this pushbutton selects a logarithmic display of 2 dB/div with a dynamic range of 16 dB.
LIN	The illuminated condition of this pushbutton selects a linear display. Signal amplitude is a linear function of input level.
FREQUENCY SPAN/DIV	Selects frequency spans from 50 Hz/div to 500 kHz/div (MAX position). A 0 Hz position provides time domain display with a bandpass dependent on the setting of the RESOLUTION selector. In the 0 Hz position the frequency dot is not displayed and when in the MAX position the frequency dot position is controlled by the DOT FREQUENCY control.
RESOLUTION	Selects resolution bandwidths of 10 Hz to 30 kHz in a 1-3 sequence. A COUPLED position electronically selects the best compatible resolution bandwidth setting for the FREQUENCY SPAN/DIV selection.
TIME/DIV	Selects the analyzer's sweep rate. Sweep rates are 10 s/div to 0.1 ms/div in a 5-2-1 sequence. An AUTO position electronically programs sweep rate so the display remains calibrated for the selected frequency span and resolution bandwidth settings.
UNCAL	When the display is uncalibrated because the FREQUENCY SPAN/DIV, RESOLUTION, and TIME/DIV switch settings are incompatible, this indicator lights and a > symbol is displayed on the crt as a prefix to the reference level readout characters.
TRIGGERING	Two trigger sources (Line and Internal) plus a Free Run mode can be selected. In the Free Run mode (FREE RUN button activated) the sweep free runs and will not sync with any trigger signal. When the LINE pushbutton is activated (illuminated) the sweep is triggered

by the line voltage to the mainframe. The INT pushbutton selects ac coupled signal components from the mainframe Trigger Source (left or right vertical).

Three trigger modes are provided: NORM (normal), SGL SWP/READY (single sweep/ready) and MNL SWEEP (manually controlled sweep). When the NORM button is activated, the sweep is triggered from the source selected; or, if the trigger is not present, the sweep automatically runs in about 10-second intervals to provide a baseline display. When the SGL SWP/READY button is activated, the sweep runs with the next trigger or in about 10 seconds if trigger is not present. In time domain operation (FREQ SPAN/DIV at 0 Hz) pushing the button activates the sweep ready state. The button lights to indicate the trigger circuit is armed and ready. The sweep will run with the arrival of a trigger. The button remains illuminated until the sweep has completed its run. This provides a ready indication of the sweep state when photographing a display.

LEVEL/SLOPE—
MNL SWP

A dual function control. As a level slope/control, it adjusts the level of the trigger threshold on either a positive or negative slope. As a manual sweep control, it positions the crt beam anywhere along the X-axis. Maximum ccw corresponds to a beam location at the left graticule edge.

DIGITAL
STORAGE

SAVE A: The SAVE A button inhibits one half of the storage locations from further updating. (Note that this inhibition takes place, whether A is displayed or not.) This "captures" a waveform for comparison, for instance, with a subsequent waveform which can be displayed via DISPLAY B.

DISPLAY A/B: When DISPLAY A or DISPLAY B is selected, the corresponding pushbutton switch is illuminated and the contents in A or B sections of memory are displayed. With SAVE A off, all memory locations are displayed and updated continuously. With SAVE A on, DISPLAY A and DISPLAY B are also selected. The contents of both memories are interlaced and displayed.

Operating Instructions—7L5 Operators

PEAK AVERAGE/BASELINE CLIPPER: A dual function control. When digital storage is off, this control operates as a conventional baseline clipper, i.e., as the control is rotated ccw, more of the vertical display is progressively blanked or clipped over the last 1/3 turn of the control. When digital storage is on, the PEAK AVERAGE control sets the level at which the vertical display is either peak detected or digitally averaged. Video signals above the level set by the PEAK AVERAGE control (and denoted by a horizontal cursor) are peak detected and stored. Video signals below the level set by the PEAK AVERAGE control are digitally averaged and stored.

B-(SAVE A): If B-(SAVE A) is activated, the algebraic difference between A and B sections of memory is displayed (SAVE A is activated if it was not previously). This display is available at the same time as DISPLAY A and DISPLAY B, if desired. The display reference level of B-(SAVE A) can be positioned vertically by a binary switch inside the instrument. Refer to service instructions and qualified service personnel.

MAX HOLD: Activating this button causes the digital memory to be updated only if the new input is of a higher magnitude than the former one (B memory only, if SAVE A is activated). This feature allows monitoring of signals that may change with time to provide a graphic record of amplitude/frequency excursions.

SWP CAL

Adjusted during the operational check to calibrate the sweep. This adjustment compensates for differences in deflection sensitivity between mainframe oscilloscopes. The SWP CAL control should be adjusted or checked for proper setting each time the 7L5 is installed in an oscilloscope.

LOG CAL

Adjusted during the operational check to calibrate the 2 dB/div and the 10 dB/div displays. This adjustment is used to compensate for differences in vertical gain between mainframe oscilloscopes. The LOG CAL control should be adjusted or checked for proper setting each time the 7L5 is installed in an oscilloscope.

AMPL CAL (L1 Plug-In Module)

The AMPL CAL control is adjusted during the initial calibration to calibrate the full screen reference level. This control is used to compensate for gain differences in the RF and IF portions of the instrument. The AMPL CAL control should be adjusted or checked for proper setting each time a plug-in module is installed in the 7L5.

HORIZ POS

Positions the display or baseline on the crt X-axis.

VERT POS

Positions the display or baseline on the crt Y-axis.

dBm/dBV

Located on the plug-in module front panel, the dBm/dBV control selects the reference level scale factor; decibels with respect to one milliwatt or decibels with respect to one volt.

Calibrating the 7L5 to the Oscilloscope Mainframe

1. Install or verify the presence of a plug-in module (see Optional Accessories, Section 1).
2. Select oscilloscope Vertical Mode, Horizontal Mode and Trigger Source (Right or Left) corresponding with plug-in compartments occupied by the spectrum analyzer. Turn on the mainframe power and allow a 10 minute warm-up period.
3. Set the front panel controls as follows:

DOT MKR	max ccw (detent position)
FREQUENCY	
SPAN/DIV	MAX (500 kHz)
RESOLUTION	COUPLED
VAR	max ccw (detent position)
BASELINE	
CLIPPER	max cw
LOG 10 dB/DIV	on
REFERENCE LEVEL	-40 dBV
INPUT BUFFER	off
FREE RUN	on
NORM	on
SAVE A	off
MAX HOLD	off
dBm/dBV	dBV (plug-in module switch)
TIME/DIV	AUTO

APPENDIX B

Laboratory Experiment Number 2

Amplitude Modulation

The topics of this experiment include:

1. Conventional AM modulator
2. Envelope detector
3. Synchronous AM detector
4. Superhetrodyne AM receiver
5. The effect of automatic gain control

OBJECTIVE: To familiarize the student with Amplitude Modulation and the circuitry associated with AM signal generation and reception.

PREREQUISITES: Completion of Lab 1, "Equipment Familiarization".

REQUIRED EQUIPMENT

The following equipment is required to perform this experiment. It is assumed the student is familiar with the controls and functions of each item listed below.

1. Oscilloscope (dual trace)
2. Spectrum Analyzer (0 to 2 MHz minimum)
3. Signal Generator (CW and AM capability)
4. Frequency Counter (0 to 2 MHz minimum)
5. Digital Voltmeter (DVM) (-20 to +20 Vdc minimum)
6. 8 Ω Speaker with Cable
7. Test Leads
8. DEGEM PS-MB-1/A Power Supply Board
9. DEGEM Boards Unit COM-1/1
Unit COM-1/2
Unit COM-1/3

REFERENCES

1. DEGEM Systems Ltd. AM and FM Communication Circuits Courses COM-1 and COM-2 Theoretical Background Manual. DEGEM Systems Ltd., 1976.
2. DEGEM Systems Ltd. AM Communication Circuits System COM-1 Experiment and Technical Manual. DEGEM Systems Ltd., 1976.

THEORETICAL BACKGROUND

SOURCE: Reference (1).

1. Section 1.2 - Amplitude Modulation
2. Section 1.3 - Frequency & Power Spectrum of an AM Wave
3. Section 2.3 - Non-linear Device Modulators
4. Section 2.6 - AM Demodulation (Detection)
5. Section 4.3 - The Superheterodyne Receiver

- 6. Section 4.4 - Characteristic Parameters of Receivers
- 7. Chapter 5 - AM Superheterodyne Receiver Circuits

Additional Background

AM Modulation Index: To calculate the modulation index (m) for sinusoidal modulation, use the following equation and refer to figure 1.

$$m = (V_1 - V_2) / (V_1 + V_2) \quad (1)$$

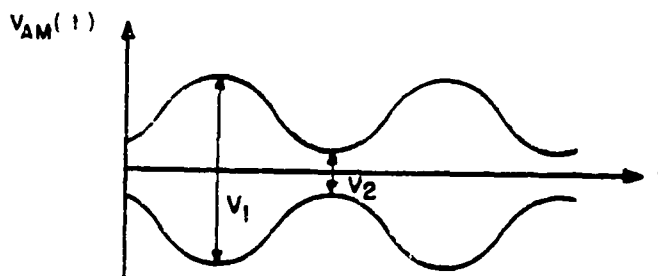


Figure 1. Definitions of AM Waveform Amplitudes. (2:26)

AM Signal RMS Amplitudes: Use the following equations to determine the RMS amplitudes of an AM waveform as described in figure 1 above.

$$V_c = 0.25 (V_1 + V_2) / 1.414 \quad V_{rms} \quad (\text{carrier}) \quad (2)$$

$$V_m = 0.125 (V_1 - V_2) / 1.414 \quad V_{rms} \quad (\text{one sideband}) \quad (3)$$

$$dBV = 20 \log_{10} V_{rms} \quad (\text{for comparing to values measured from the spectrum analyzer}) \quad (4)$$

Image Frequency Calculation: The calculation of the Image Frequency (f_{image}) is:

$$f_{image} = f_{RF} + 2 \times f_{IF} \quad (5)$$

where f_{RF} = RF frequency of desired signal

f_{IF} = receiver IF frequency

DEGEM Circuit Board Description

SOURCE: Reference (2).

Technical Description of Plug-In Units

- Unit COM-1/1
- Unit COM-1/2
- Unit COM-1/3

EXPERIMENT PROCEDURE

General Instructions

SPECIAL NOTE

Do not attempt to adjust any of the variable transformers on the DEGEM boards. These transformers are easily damaged and are preset for optimal performance.

WARNING

Turn the DEGEM Power Supply Board off before removing or inserting any plug-in boards. Damage to circuit components may result if the boards are changed while the power is on.

1. DO NOT turn the DEGEM PS-MB-1/A Power Supply Board on. Install the Unit COM-1/1, 1/2, and 1/3 boards into the power supply board by pressing each unit into a power socket and tightening the hold-down screws on each end of the unit.
2. Turn the power supply board on. All plug-in units are internally powered and therefore need no external power connections.
3. Turn all of the remaining equipment on.

AM Modulator

Objectives: To determine the AM modulator bandwidth and observe variations of the AM waveform parameters in the time and frequency domains.

1. Connect the oscillator output to the Carrier In on Unit COM-1/1 board as shown in figure 2 (AM Modulator).

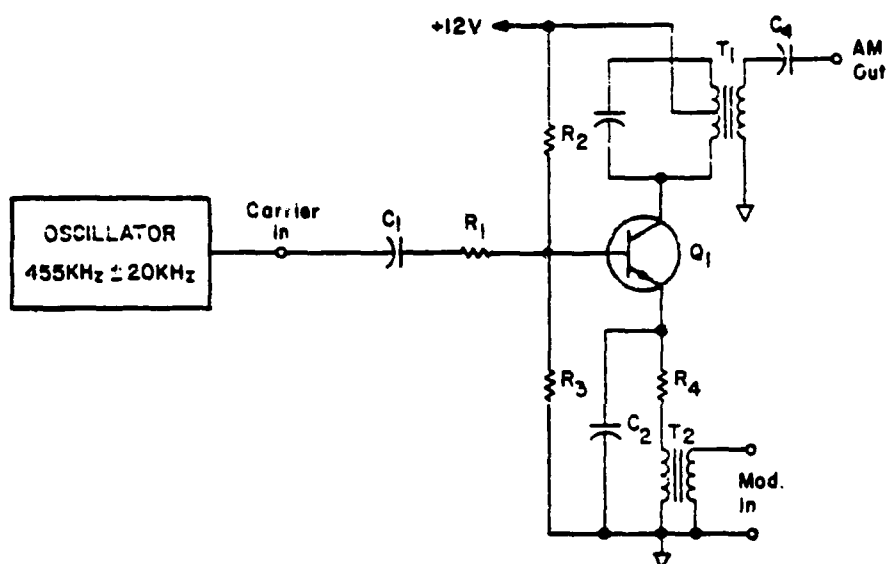


Figure 2. AM Modulator. (2:26)

2. Tuning the oscillator for the center frequency of the modulator:
 - a. Connect an oscilloscope and frequency counter to Carrier In.
 - b. Use the oscilloscope and potentiometer P₃ to set the Carrier In amplitude to 1 V_{pp}.
 - c. Use the frequency counter and potentiometers P₁ and P₂ to set the Carrier In frequency to 455 kHz.
 - d. Generate a 10 kHz, 0.5 V_{pp} sine wave from the signal generator using a frequency counter and oscilloscope to make measurements. Connect this signal to Mod. In.

- e. Connect the frequency counter to Carrier In and the spectrum analyzer to AM Out.
 - f. Observe AM Out on the spectrum analyzer at 455 kHz and adjust the analyzer so both modulation sidebands are visible.
 - g. Adjust the Carrier In frequency slightly (using P_1 and P_2) until the modulation sidebands have equal power as displayed on the spectrum analyzer.
 - h. The oscillator (AM carrier) is now adjusted for the center frequency of the modulator. Record the Carrier In frequency, as indicated on the frequency counter, on the data sheet.
3. Measuring the AM waveform parameters:
- a. Observe the AM Out signal on the oscilloscope and determine the modulation index using equation (1) in the theoretical background section. Record the modulation index on the data sheet.
 - b. Measure the amplitude of the carrier spectral component on the spectrum analyzer in dBV. Calculate the rms voltage of the carrier component from the time-domain signal amplitudes using equation (2) in the theoretical background section. Convert this value to dBV using equation (4) and compare to the measure value. Record both values.
 - c. Repeat step b above for one of the modulation sidebands using equation (3) to calculate the rms voltage.
4. Measuring the AM Modulator bandwidth:
- a. Using the frequency counter adjust the Mod. In signal connected to the signal generator to a 1 kHz sine wave.
 - b. Observe the AM Out signal on the spectrum analyzer at the carrier frequency so that both modulation sidebands are visible.
 - c. Note the vertical position of the sideband peaks and increase the Mod. In signal frequency until the sideband peaks have dropped by 3 dB (0.5 of the original power).

- d. The modulation peaks are now at the 3 dB points of the modulator's frequency response. Measure the bandwidth between these points and record it on the data sheet.
5. Changing the modulation index:
- a. Adjust the Mod. In signal back to a 1 kHz sine wave using the frequency counter to make measurements.
 - b. Observe AM Out on the oscilloscope and spectrum analyzer.
 - c. Vary the Mod. In amplitude and notice the change in the sideband power and the modulation index.
 - d. Continue increasing the Mod. In amplitude until a modulation index of 1.0 (100%) is obtained as viewed on the oscilloscope.
 - e. Measure the amplitude of the carrier and the upper or lower sideband on the spectrum analyzer. Record these values on the data sheet. The power of a single sideband should be 0.25 (-6 dB) of the carrier power.

Envelope Detector

Objective: To observe detection of a standard and over-modulated AM waveform by an envelope detector. Also to determine the bandwidth of the envelope detector.

1. Adjust the signal generator output (Mod. In signal on Unit COM-1/1) to a 1 kHz, 0.5 Vpp sine wave measuring with the frequency counter and oscilloscope.
2. Connect AM Out to the envelope detector on Unit COM-1/3 as shown in figure 3.
3. Determining the envelope detector bandwidth:
 - a. Connect the spectrum analyzer to the output of the envelope detector (i.e. to the negative lead of the dc blocking capacitor C₂ on Unit COM-1/3).
 - b. Observe the output of the envelope detector on the spectrum analyzer at 1 kHz.

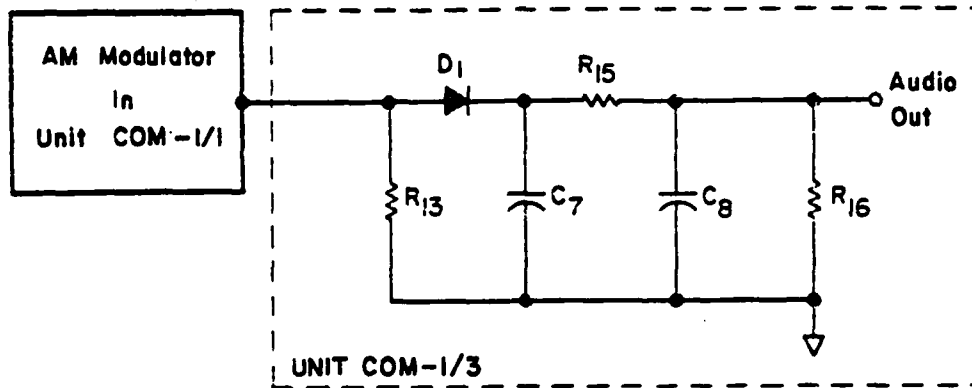


Figure 3. Diode Envelope Detector. (2:28)

- c. Trace out the frequency response of the envelope detector on the spectrum analyzer by varying the modulation frequency. Determine and record the 3 dB point and bandwidth.
4. Detecting an overmodulated AM waveform:
 - a. Reset the Mod. In frequency to 1 kHz using the frequency counter.
 - b. Observe the envelope detector output on one channel of the oscilloscope and the AM Out signal on the other channel.
 - c. Increase the Mod. In amplitude until the AM signal is overmodulated. Notice the distorted waveform that is reconstructed from the envelope detector.

Synchronous AM Detector

Objective: To observe the output of a synchronous AM detector.

1. Reset the Mod. In amplitude to 1 Vpp measured with an oscilloscope.

2. Connect the synchronous AM detector on Unit COM-1/1 to the AM Out signal as shown in figure 4. Also connect the Carrier In signal to the base input capacitor C₃.
3. Examine the waveform at Audio Out on the oscilloscope and notice it is the same as the modulating signal.

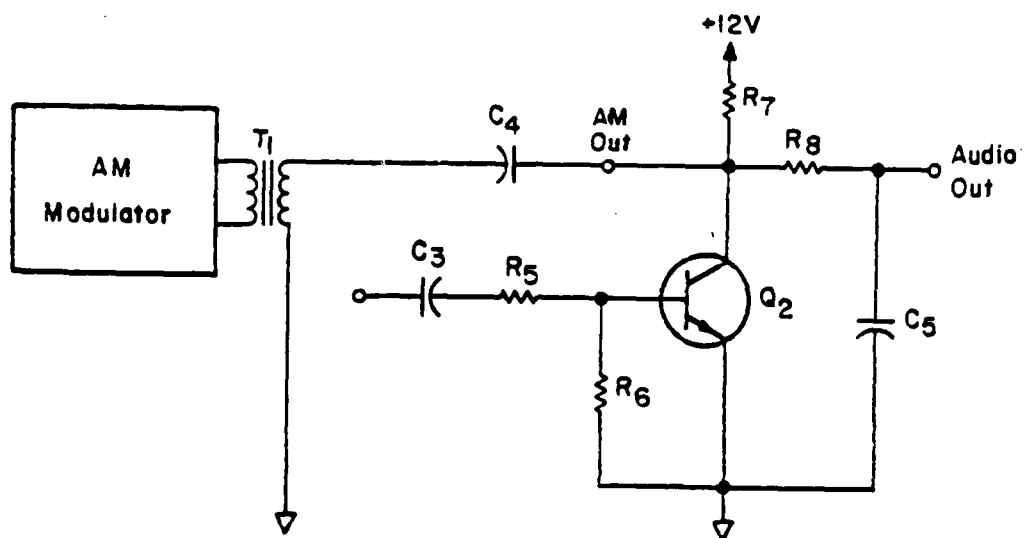


Figure 4. Synchronous AM Detector. (2:29)

Receiver Local Oscillator

Objective: To measure the characteristics of the local oscillator.

1. The receiver local oscillator (L.O.) is shown in figure 5.
2. Connect a frequency counter and oscilloscope to L.O. OUT and set potentiometer P₁ fully cw.
3. Determine and record the frequency range of the oscillator by turning the frequency dial (Coec) to its maximum and minimum frequencies.

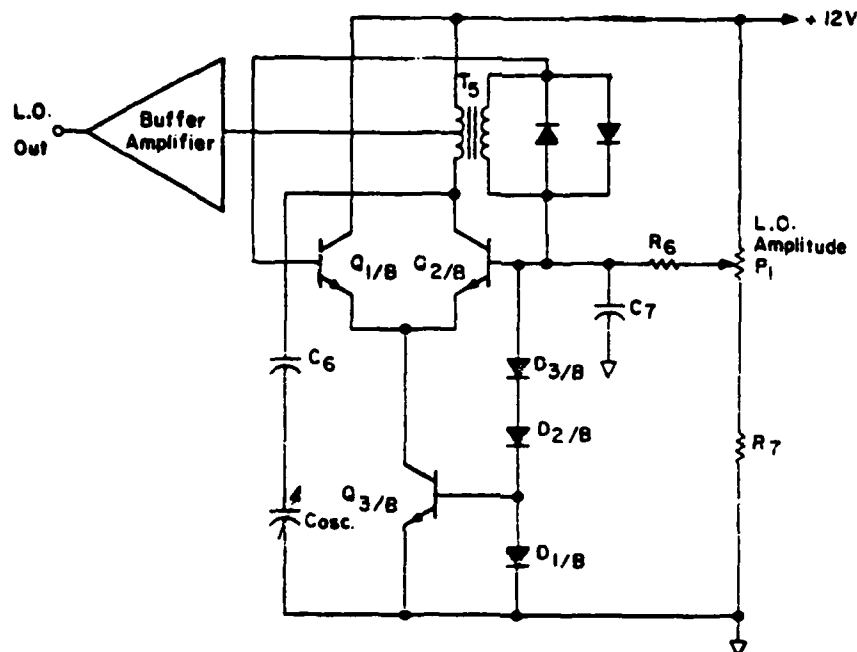


Figure 5. Local Oscillator Circuit. (2:32)

4. Measure and record the maximum amplitude of the local oscillator as adjusted by P_1 . Note that the local oscillator can be stopped by reducing the L.O. amplitude.

Determining the Intermediate Frequency from the Mixer Circuit

Objective: To determine the center frequency of the mixer circuit which is the intermediate frequency (IF) of the superhetrodyne AM receiver.

1. Set-up:

- a. The mixer circuit is located on Unit COM-1/2 and is shown in figure 6.
- b. Generate a 455 kHz, 1 Vpp sine wave from the signal generator measured with the frequency counter and oscilloscope. Connect this signal to the 1:1000 attenuator on Unit COM-1/2.

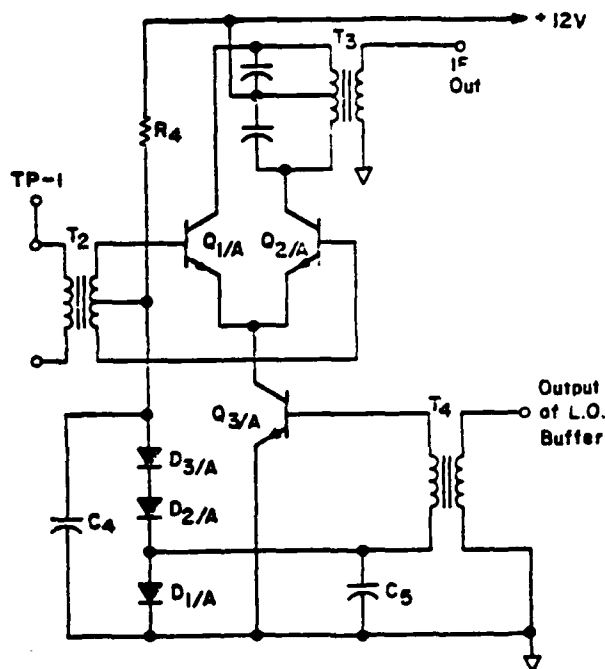


Figure 6. Mixer Circuit. (2:34)

- c. Turn both the potentiometer P_1 and frequency dial on Unit COM-1/2 fully ccw.
 - d. Observe the IF OUT signal on the oscilloscope. If the signal is distorted, reduce the signal generator amplitude slightly.
 - e. Connect the spectrum analyzer to the IF OUT signal and examine the spectral pulse at 455 kHz.
2. Trace the frequency response of the mixer circuit on the spectrum analyzer by varying the input signal frequency. Determine the center frequency of this response curve. This frequency is the IF frequency. All other receiver stages are tuned to this frequency.

Determining the RF Amplifier Frequency Response

Objective: To determine the RF Amplifier frequency response.

1. Set-up:

- a. The RF Amplifier is shown in figure 7.

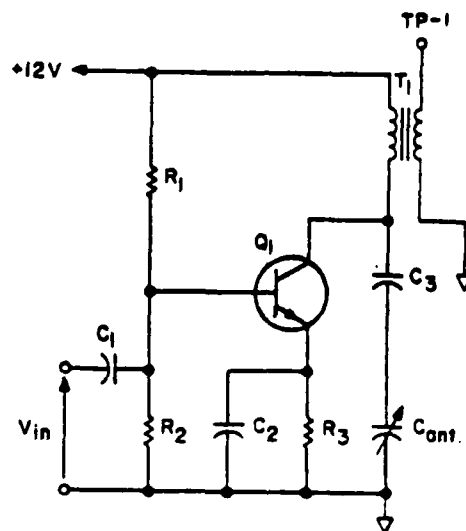


Figure 7. RF Amplifier Circuit. (2:33)

- b. Generate a 1 MHz, 1 Vpp sine wave from the signal generator measured with the frequency counter and oscilloscope. Connect this signal to the 1:1000 attenuator on Unit COM-1/2.
- c. Turn P1 fully cw and connect a frequency counter to L.O. OUT. Set the L.O. frequency to 1 MHz plus the IF frequency measured in the last section by adjusting the frequency dial on Unit COM-1/2.
- d. Turn P1 fully ccw to stop the L.O.
- e. Connect the frequency counter and spectrum analyzer to TP-1.

2. Observe the spectral component at 1 MHz on the analyzer. Trace the RF Amplifier frequency response on the analyzer by varying the signal generator frequency.
3. Determine and record the center frequency and 3 dB bandwidth. The center frequency should be at about 1 MHz.
4. Change the L.O. frequency dial slightly and retrace the RF Amplifier frequency response. Notice that the center frequency has moved.

Determining the IF Amplifiers Frequency Responses

Objective: To determine the frequency responses of the two IF amplifiers.

1. The two IF Amplifiers are shown in figure 8.

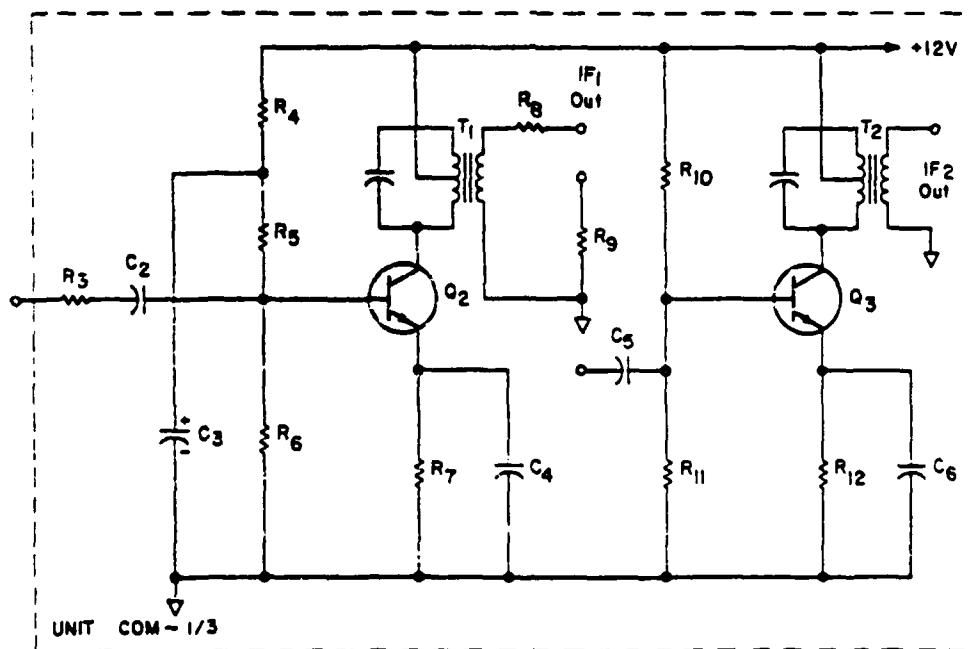


Figure 8. IF Amplifiers. (2:36)

2. First IF Amplifier:

- a. Connect a 1 Vpp sine wave at the IF frequency (measured with an oscilloscope and frequency counter) from the signal generator to R₃ on Unit COM-1/3.
- b. Connect the frequency counter, oscilloscope, and spectrum analyzer to IF₁ OUT. Connect IF₁ OUT to R₄.
- c. Examine the time-domain trace of the first amplifier signal. Reduce the signal generator amplitude if there is any distortion.
- d. Observe the IF₁ OUT signal on the spectrum analyzer at the IF frequency. Vary the input frequency and trace out the frequency response of the first IF amplifier. Determine and record the center frequency and 3 dB bandwidth.

3. Second IF Amplifier:

- a. Disconnect the input signal from R₃ and connect it to C₆ (the input of the second IF stage). Reset the input frequency to the IF frequency using the frequency counter.
- b. Connect the frequency counter and oscilloscope to IF₂ OUT.
- c. Reduce the input signal amplitude until the IF₂ OUT signal is 500 mVpp as measured on the oscilloscope.
- d. Connect the IF₂ OUT to the spectrum analyzer and examine the spectral component at the IF frequency. Trace the frequency response of this IF stage by varying the input frequency. Determine and record the center frequency and 3 dB bandwidth.

Effect of AGC

Objective: To determine the gain varying characteristics of the automatic gain control.

1. Set-up:
 - a. Connect the signal generator, set at the IF frequency, to the input of the first IF Amplifier (R_3). Also attach IF₁ OUT to C_5 .
 - b. Connect the potentiometer P_1 on Unit COM-1/3 to AGC In as shown in figure 9 below.
2. Connect IF₂ OUT and the input signal to a dual trace oscilloscope. Also connect a DVM to AGC IN.
3. Compute and record amplifier gains for AGC voltages of 0.5, 0.6, 0.7, and 0.75 Vdc using inputs of 20 and 40 mVpp.

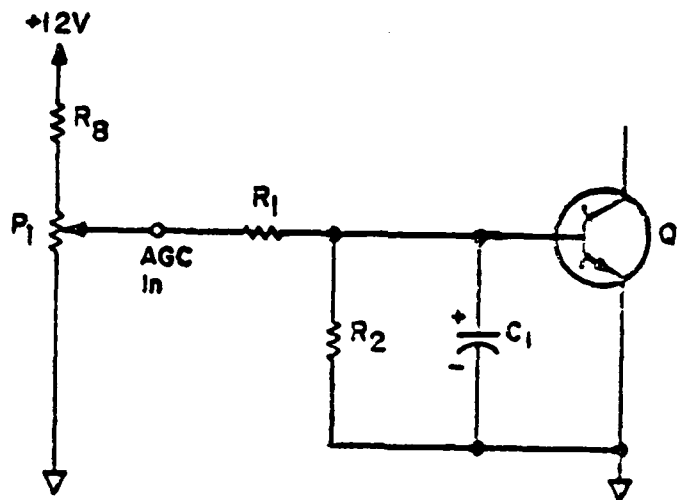


Figure 9. AGC Circuit. (2:37)

Complete AM Superheterodyne Receiver

Objective: To observe the performance and operation of the AM superheterodyne receiver. Also to observe the reception of a standard AM signal and an AM signal at the image frequency of the receiver.

1. Set-up:
 - a. Assemble the complete receiver as shown in figure 10.

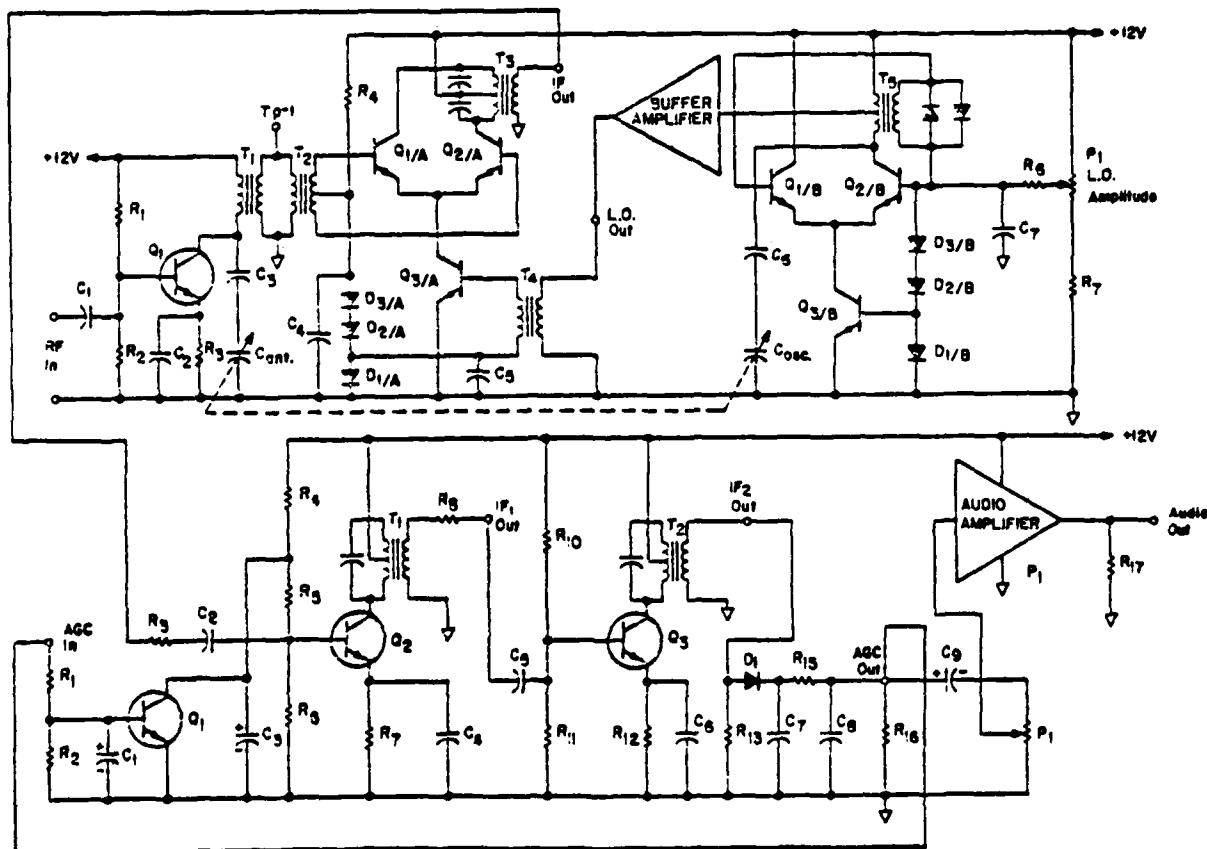


Figure 10. Complete AM Superheterodyne Receiver. (2:41)

- b. Generate an AM waveform from the signal generator with the following parameters using the frequency counter and oscilloscope to make measurements.

Carrier - 700 kHz, 1 Vpp sine wave
 Modulation - 30 % at 1 kHz sine wave

- c. Connect the AM waveform to the 1:1000 attenuator input of the RF Amplifier. Connect a speaker and oscilloscope to the output of the receiver (Audio Out). Connect a frequency counter to L.O. OUT on Unit COM-1/2.

2. Reception of the AM signal:

- a. Calculate and record the proper L.O. frequency to receive the 700 kHz RF signal knowing the IF frequency measured previously.
- b. Turn P₁ on Unit COM-1/2 fully cw.
- c. Adjust the L.O. to this frequency and observe the receiver output on the oscilloscope. Vary the L.O. slightly and notice how the signal fades and returns. Return the L.O. frequency to the best received frequency.

3. Reception of the Image Frequency:

- a. Calculate and record the Image Frequency based on the 700 kHz carrier and IF frequency using equation (5).
- b. Do not change the L.O. frequency.
- c. Set the carrier frequency of the AM waveform to the calculated Image Frequency. Apply this signal to the receiver and notice reception of the signal without changing the L.O. frequency.
- d. Increase the L.O. frequency to the Image Frequency plus the IF frequency to receive the Image signal directly. The signal should be much stronger because the receiver is now tuned to the input RF signal. Measure and record the L.O. frequency for maximum output amplitude.

STUDENT NAMES _____ DATE PERFORMED _____

Note: Indicate unit of measurement with each data entry.

MODULATOR:

Center Frequency	_____	
Modulation Index	_____	
Carrier Amplitude (dBV)	_____	_____
	(from analyzer)	(from scope)
Sideband Amplitude (dBV)	_____	_____
	(from analyzer)	(from scope)
Bandwidth	_____	
100 % Carrier Ampl. (dBV)	_____	
100 % Sideband Ampl. (dBV)	_____	

ENVELOPE DETECTOR

3 dB point	_____
Bandwidth	_____

LOCAL OSCILLATOR

Frequency Range	_____	_____
	(lower)	(upper)

Maximum Amplitude	_____

MIXER

Intermediate Frequency	_____

RF AMPLIFIER

Center Frequency	_____
Bandwidth	_____

IF AMPLIFIERS

First Center Frequency _____

First Bandwidth _____

Second Center Frequency _____

Second Bandwidth _____

AUTOMATIC GAIN CONTROL

Gains for Input Voltages (mVpp)

AGC (Vdc)	20	40
0.5	_____	_____
0.6	_____	_____
0.7	_____	_____
0.75	_____	_____

COMPLETE AM SUPERHETERODYNE RECEIVER

L.O. Frequency _____ (for 700 kHz RF)

Image Frequency (RF) _____ (for 700 kHz RF)

L.O. Frequency _____ (at Image Recept.)

STUDENT NAMES SAMPLE DATE PERFORMED

Note: Indicate unit of measurement with each data entry.

MODULATOR:

Center Frequency	<u>456.89 kHz</u>	
Modulation Index	<u>0.16</u>	
Carrier Amplitude (dBV)	<u>-5 dBV</u> (from analyzer)	<u>-5.19 dBV</u> (from scope)
Sideband Amplitude (dBV)	<u>-26.6 dBV</u> (from analyzer)	<u>-27.09 dBV</u> (from scope)
Bandwidth	<u>28.0 kHz</u>	
100 % Carrier Ampl. (dBV)	<u>-6.4 dBV</u>	
100 % Sideband Ampl. (dBV)	<u>-12.5 dBV</u>	

ENVELOPE DETECTOR

3 dB point	<u>11.60 kHz</u>
Bandwidth	<u>11.60 kHz</u>

LOCAL OSCILLATOR

Frequency Range	<u>1051.1 kHz</u> (lower)	<u>2141.5 kHz</u> (upper)
Maximum Amplitude	<u>4 Vpp</u>	

MIXER

Intermediate Frequency	<u>458.76 kHz</u>

RF AMPLIFIER

Center Frequency	<u>1.0 MHz</u>
Bandwidth	<u>40.0 kHz</u>

IF AMPLIFIERS

First Center Frequency	<u>459.50 kHz</u>
First Bandwidth	<u>29.0 kHz</u>
Second Center Frequency	<u>460.25 kHz</u>
Second Bandwidth	<u>27.5 kHz</u>

AUTOMATIC GAIN CONTROL

Gains for Input Voltages (mVpp)

AGC (Vdc)	20	40
0.5	<u>56</u>	<u>55</u>
0.6	<u>57</u>	<u>55</u>
0.7	<u>48</u>	<u>49</u>
0.75	<u>38</u>	<u>37</u>

COMPLETE AM SUPERHETERODYNE RECEIVER

L.O. Frequency	<u>1158 kHz</u>	(for 700 kHz RF)
Image Frequency (RF)	<u>1616 kHz</u>	(for 700 kHz RF)
L.O. Frequency	<u>2075 kHz</u>	(at Image Recept.)

APPENDIX C

Laboratory Experiment Number 2-5

Amplitude Modulation Set-Up

This experiment provides a procedure for use by instructors or technicians to tune several circuit components on the boards used by students performing laboratory experiment number 2, Amplitude Modulation.

OBJECTIVE: To enable the instructor or technician to tune the DEGEM Unit COM-1/2 and 1/3 boards for use by students performing Lab 2, "Amplitude Modulation".

PREREQUISITES: Familiarization of all required equipment. Completion of Lab 1, "Equipment Familiarization", is recommended.

REQUIRED EQUIPMENT

The following equipment is required to tune the DEGEM boards used in the Lab 2 experiment.

1. Oscilloscope (dual trace)
2. Spectrum Analyzer (0 to 2 MHz minimum)
3. Signal Generator (sine wave)
4. Frequency Counter (0 to 2 MHz minimum)
5. Test Leads
6. Transformer Tuning Tool
7. DEGEM PS-MB-1/A Power Supply Board
8. DEGEM Boards Unit COM-1/2
Unit COM-1/3
9. Masking Tape

REFERENCES

1. DEGEM Systems Ltd. AM and FM Communication Circuits Courses COM-1 and COM-2 Theoretical Background Manual. DEGEM Systems Ltd., 1976.
2. DEGEM Systems Ltd. AM Communication Circuits System COM-1 Experiment and Technical Manual. DEGEM Systems Ltd., 1976.

PROCEDURE

General Instructions

WARNING

Turn the DEGEM Power Supply Board off before removing or inserting any plug-in boards. Damage to circuit components may result if the boards are changed while the power is on.

1. DO NOT turn the DEGEM PS-MB-1/A Power Supply Board on. Install the Unit COM-1/2 and 1/3 boards into the power supply board by pressing each unit into a power socket and tightening the hold-down screws on each end of the unit.
2. Turn the power supply board on. All plug-in units are internally powered and therefore need no external power connections.
3. Turn all of the remaining equipment on.

Tuning the Receiver Local Oscillator

Objectives: To tune the local oscillator to a minimum frequency of 1050 kHz.

1. Connect a frequency counter to L.O. Out on the Unit COM-1/2 board.
2. Set the tuner frequency dial on the Unit COM-1/2 board to its minimum frequency and turn potentiometer P₁ fully cw.
3. Adjust transformer T_o so the L.O. Out frequency is 1050 kHz using the transformer tuning tool.
4. Place a piece of tape on top of transformer T_o.

Determining the Intermediate Frequency from the Mixer Circuit

Objective: To measure the mixer intermediate frequency for tuning the IF and RF amplifiers.

1. Generate a 455 kHz, 1 Vpp sine wave from the signal generator measured with the frequency counter and oscilloscope. Connect this signal to the 1:1000 attenuator on Unit COM-1/2.
2. Turn both the potentiometer P₁ and frequency dial on Unit COM-1/2 fully ccw.
3. Observe the IF OUT signal on the oscilloscope. If the signal is distorted, reduce the signal generator amplitude slightly.

4. Connect the spectrum analyzer to the IF OUT signal and examine the spectral pulse at 455 kHz.
5. Trace the frequency response of the mixer on the spectrum analyzer by varying the input signal frequency. Determine the center frequency of this response curve. This frequency is the IF frequency and all other receiver stages will be tuned to this frequency.

Tuning the IF Amplifier Stages

Objective: To center the IF amplifiers' frequency response on the mixer intermediate frequency.

1. Connect the signal generator, set at the IF frequency, to resistor R_3 on the Unit COM-1/3 board. Connect IF₁ OUT to R_4 and to the oscilloscope.
2. Observe the IF₁ OUT on the oscilloscope and reduce the input signal amplitude if the signal is distorted.
3. Connect the frequency counter and spectrum analyzer to IF₁ OUT. Examine the spectral component at the IF frequency.
4. Adjust transformer T_1 on Unit COM-1/3 until the IF spectral component is at a maximum.
5. Verify that this is the center frequency of the first IF amplifier stage by varying the input frequency and tracing the amplifier frequency response. If the IF frequency is not the center frequency of this stage, then readjust T_1 slightly and retrace the amplifier frequency response.
6. When the first IF amplifier is tuned to the IF frequency, place a piece of tape on top of transformer T_1 .
7. Tune the second IF amplifier in the same manner. Connect the input signal (set at the IF frequency) to capacitor C_6 on Unit COM-1/3 and IF₂ OUT to resistor R_{14} . Connect the IF₂ OUT signal to the oscilloscope, spectrum analyzer, and frequency counter.
8. Reduce the input signal amplitude until the IF₂ OUT signal is not distorted.

9. Observe the IF spectral component on the spectrum analyzer. Tune transformer T_2 until this component is maximum.
10. Verify that the IF frequency is the center frequency of the second amplifier by tracing out the frequency response curve. Adjust T_2 if necessary.
11. Place a piece of tape over T_2 when the second amplifier is tuned properly.

Tuning the RF Amplifier

Objective: To center the RF Amplifier frequency response on the mixer IF plus the L.O. frequency.

1. Connect a frequency counter to L.O. OUT on Unit COM-1/2 and turn potentiometer P_1 fully cw.
2. Adjust the frequency dial on Unit COM-1/2 until the L.O. OUT frequency is 1 MHz plus the IF frequency.
3. Adjust the signal generator for a 1 Vpp, 1 MHz sine wave measured with the oscilloscope and frequency counter. Connect this signal to the 1:1000 attenuator on Unit COM-1/2.
4. Observe the RF amplifier output at TP-1 on the spectrum analyzer at 1 MHz. Adjust transformer T_1 on Unit COM-1/2 until the spectral component is maximum.
5. Verify that the 1 MHz component is the center frequency of the RF Amplifier by tracing out the amplifier frequency response. Adjust T_1 slightly if necessary to center the frequency response.
6. Place a piece of tape over T_1 when it is properly tuned.

APPENDIX D

Laboratory Experiment Number 3

Frequency Modulation

The topics of this experiment include:

1. FM modulator
2. Ratio detector
3. Product detector
4. Superhetrodyne FM receiver
5. The effect of automatic frequency control

OBJECTIVE: To familiarize the student with Frequency Modulation and the circuitry associated with FM signal generation and reception.

PREREQUISITES: Completion of Lab 1, "Equipment Familiarization".

REQUIRED EQUIPMENT

The following equipment is required to perform this experiment. It is assumed the student is familiar with the controls and functions of each item listed below.

1. Oscilloscope (dual trace with horizontal time delay)
2. Spectrum Analyzer (0 to 2 MHz minimum)
3. 2 Signal Generators (CW capability)
5. Frequency Counter (0 to 2 MHz minimum)
6. DC Power Supply (-5 to +5 Vdc minimum)
7. Digital Voltmeter (DVM) (-20 to +20 Vdc minimum)
8. Test Leads
9. DEGEM PS-MB-1/A Power Supply Board
10. DEGEM Boards Unit COM-2/1
Unit COM-2/2
Unit COM-2/3

REFERENCES

1. DEGEM Systems Ltd. AM and FM Communication Circuits Courses COM-1 and COM-2 Theoretical Background Manual. DEGEM Systems Ltd., 1976.
2. DEGEM Systems Ltd. FM Communication Circuits System COM-1 Experiments and Technical Manual. DEGEM Systems Ltd., 1976.
3. AFCC Systems Evaluation School. Evaluation of FDM and FM Systems. AFCC 30000-1. January, 1983.

THEORETICAL BACKGROUND

SOURCE: Reference (1).

1. Section 1.4 - Phase & Frequency Modulation
2. Section 1.5 - FM Spectrum
3. Chapter 3 - FM Modulators and Detectors

4. Section 4.4 - Characteristic Parameters of Receivers
5. Section 4.5 - FM Radio Receivers
6. Chapter 6 - FM Superheterdyne Receiver Circuits

Additional Background

Modulator Linearity: Figure 1 shows the modulator transfer characteristics of an ideal and practical modulator. The graph is a plot of the peak frequency deviation versus the input modulation amplitude. The slope of the ideal line is the sensitivity, K_{FM} of the modulator.

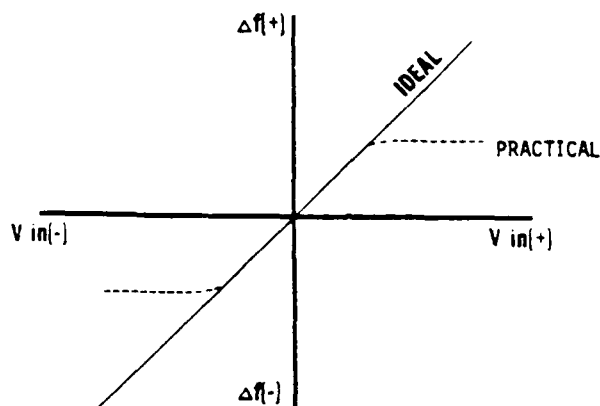


Figure 1. Modulator Transfer Characteristic. (3:9-1)

In the practical modulator case, the transfer characteristic will deviate from the ideal line for larger input amplitudes. Modulation amplitudes of this magnitude will cause intermodulation distortion of the transmitted signal.

Determining the Sensitivity of the Modulator: The sensitivity of the modulator is the constant K_{FM} and represents the frequency deviation from the carrier due to instantaneous modulation amplitude. The equation to calculate K_{FM} is:

$$K_{FM} = \Delta f / A_m \quad (1)$$

where Δf = peak frequency deviation

A_m = modulation amplitude

The peak frequency deviation (Δf) is determined from:

$$\Delta f = \beta f_m \quad (2)$$

where f_m = modulation frequency

β = modulation index

The β value of an FM modulator varies with input modulation amplitude and can be determined when the carrier spectral component drops out. The carrier power follows the first order Bessel Function which has nulls at certain points. These nulls cause the carrier to drop out (i.e. have no power). The β values have been tabulated and are constant for different dropout points. These are shown in Table 1.

Therefore the peak deviation at a particular dropout can be determined from the modulation frequency and associated β value. A plot of peak deviation, Δf , versus modulation peak amplitude, A_m , can be made. The slope of the line on this plot is the sensitivity of the modulator, K_{FM} . If a sufficient number of dropout points were examined and plotted, the linearity of the modulator could also be determined.

DEGEM CIRCUIT BOARD DESCRIPTION

SOURCE: Reference (2).

Technical Description of Plug-In Units

- Unit COM-2/1
- Unit COM-2/2
- Unit COM-2/3

Table 1. Table of β Required for Carrier and Sideband Dropouts. (3:9-2)

Dropout Number (n)	Carrier β_n	First Sideband β_n
1	2.4048	3.8317
2	5.5201	7.0156
3	8.6537	10.1735
4	11.7915	13.3237
5	14.9309	16.4706
6	18.0711	19.6159
7	21.2116	22.7601
8	24.3525	25.9037
9	27.4935	29.0468
10	30.6346	32.1897
11	33.7758	35.3323
12	36.9171	38.4748
13	40.0584	41.6171
14	43.1993	44.7593
15	46.3412	47.9015
16	49.4826	51.0435
17	52.6241	54.1856
18	55.7655	57.3275
19	58.9070	60.4695
20	62.0485	63.6114

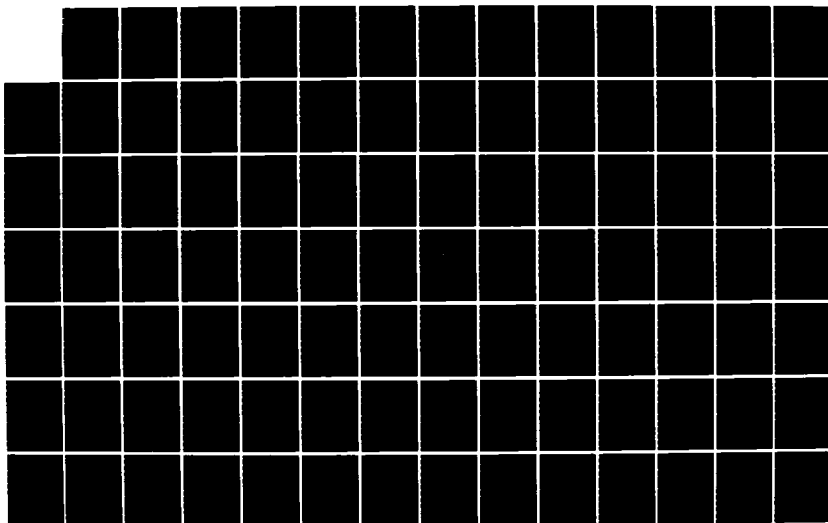
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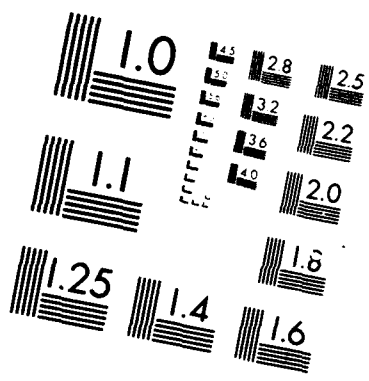
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EXPERIMENT PROCEDURE

General Instructions

SPECIAL NOTE

Do not attempt to adjust any of the variable transformers on the DEGEM boards. These transformers are easily damaged and are preset for optimal performance.

WARNING

Turn the DEGEM Power Supply Board off before removing or inserting any plug-in boards. Damage to circuit components may result if the boards are changed while the power is on.

1. DO NOT turn the DEGEM PS-MB-1/A Power Supply Board on. Install the Unit COM-2/1, 2/2 and 2/3 boards into the power supply board by pressing each unit into a power socket and tightening the hold-down screws on each end of the unit.
2. Turn the power supply board on. All plug-in units are internally powered and therefore need no external power connections.
3. Turn all of the remaining equipment on.

FM Modulator

Objectives: To determine the frequency ranges of the FM oscillator and to determine sensitivity constant K_{FM} of the modulator by using carrier dropouts.

1. Determining the oscillator frequency ranges:
 - a. Connect a frequency counter to Osc. Out on Unit COM-2/1.
 - b. Turn the Oscillator Output Amplitude (potentiometer P_2) to its centered position.
 - c. Set the FM Oscillator to Range A.
 - d. Measure and record the lowest and highest frequencies by adjusting potentiometer P_1 .

- e. Set the oscillator to Range B.
 - f. Measure and record the lowest and highest frequencies by adjusting potentiometer P_1 .
2. Measuring the sensitivity (K_{FM}) of the modulator:
- a. Set the FM oscillator to 1 MHz (measured with a frequency counter attached to Osc. Out) by using Range A and adjusting P_1 .
 - b. Set Osc. Out to 3 Vpp measured with an oscilloscope by adjusting P_2 .
 - c. Generate a 1 kHz sine wave from a signal generator (measured with an oscilloscope and frequency counter).
 - d. Connect the signal generator output to Mod. In and the spectrum analyzer to Osc. Out. Reduce the Mod. In signal to minimum amplitude.
 - e. Connect the spectrum analyzer to Osc. Out. Observe the spectrum of the FM signal at 1 MHz so the FM carrier is clearly visible. Recommended settings on the spectrum analyzer are 1 kHz/DIV and 10 dB/DIV.
 - f. Increase the modulation amplitude (Mod. In signal) very slowly until the carrier component drops out. This drop out point corresponds to the first carrier dropout and β value of 2.4048.
 - g. Measure and record the Mod. In amplitude (V_p - zero-to-peak) at the first carrier dropout point.
 - h. Increase the modulation amplitude until the second carrier dropout point is reached. This point corresponds to a β value of 5.5201. Measure and record the Mod. In amplitude (V_p).
 - i. Increase the modulation amplitude until the third carrier dropout point is reached. This point corresponds to a β value of 8.6537. Measure and record the Mod. In amplitude (V_p).
 - j. Calculate and record the frequency deviation for each dropout point using equation (2) in the theoretical background section. Note that f_m is 1 kHz.

- k. Use equation (1) to calculate K_{FM} for each dropout point and average the three values. Record the averaged value as K_{FM} on the data sheet.
- m. Set the modulation amplitude to a 2 V_{pp} sine wave and observe the full spectrum of the FM signal (i.e. so the bandwidth of the signal is shown).
- n. Notice the spectral peaks at a frequency deviation from the carrier of about K_{FM} times 1 V_p.

Ratio Detector

Objectives: To observe the detection of an FM signal by a ratio detector and to determine the linearity of the ratio detector.

1. Set-up:

- a. Connect the ratio detector circuit on Unit COM-2/1 as shown in figure 2 below (i.e. connect C_4 to R_2).

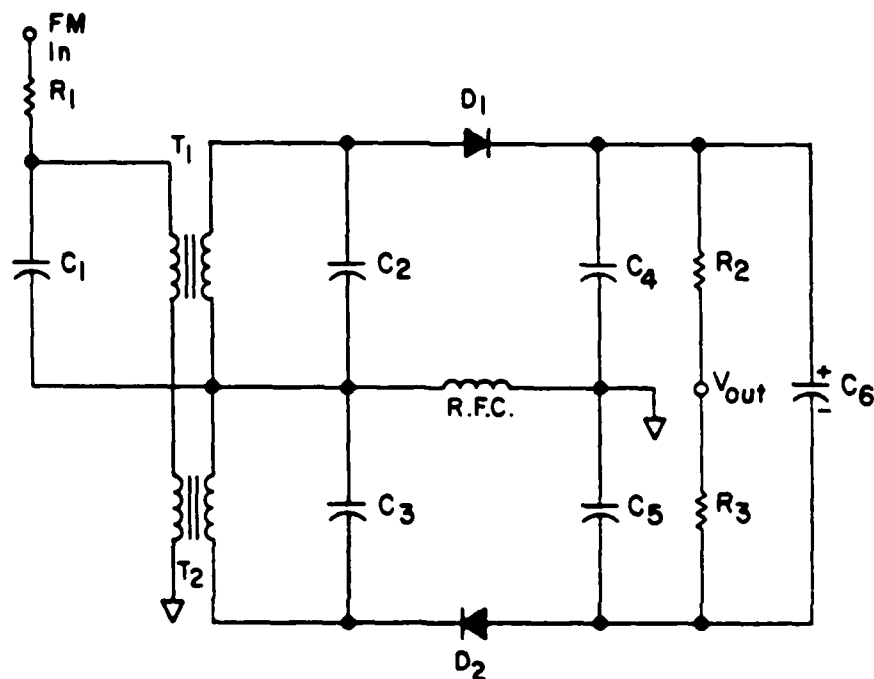


Figure 2. Ratio Detector. (2:26)

- b. Set up the FM Modulator with the following parameters using an oscilloscope and frequency counter to make measurements.

Carrier	455 kHz	Maximum Amplitude
Modulation	1 kHz	3 Vpp (sine wave from signal generator)

- c. Connect the output of the FM Modulator to FM In on the Ratio Detector.

2. Linearity:

- Connect an oscilloscope to the V_{out} of the ratio detector.
- Increase the modulation amplitude until the detected signal is distorted. Measure and record the input modulation amplitude.
- Determine and record the maximum modulation amplitudes for a triangular wave and square wave.

Product Detector

Objective: To observe the detection of an FM signal with a product detector.

- Assemble the product detector on Unit CDM-2/2 as shown in figure 3.
- Connect the FM signal used for the ratio detector to the input of the product detector.
- Connect a dual trace oscilloscope to the Mod. In and AF Out signals. Vary the Mod. In amplitude and verify that the product detector demodulates the signal properly.

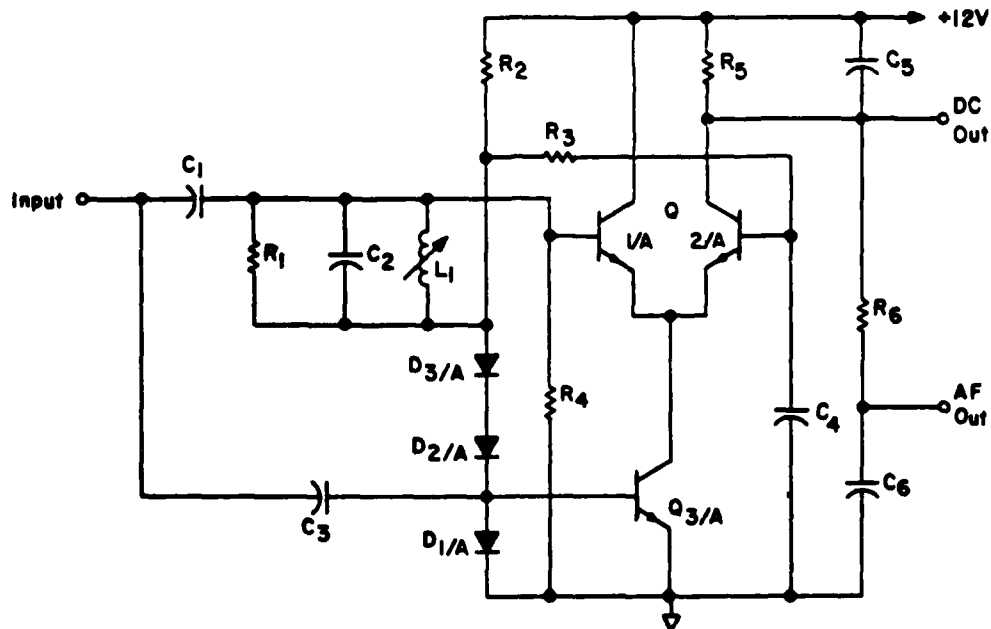


Figure 3. Product Detector. (2:28)

IF Amplifiers

Objectives: To determine the IF of both amplifiers and to observe the effect of the amplifiers on amplitude and bandwidth limiting.

1. Determining the Intermediate Frequency of the IF Amplifiers:
 - a. Connect a 455 kHz, 0.5 Vpp sine wave from a signal generator to the 1:100 attenuator input on Unit COM-2/2. Use the frequency counter and oscilloscope to make the measurements.
 - b. Connect IFs Out to the spectrum analyzer and observe the spectral component at 455 kHz.
 - c. Trace out the frequency response of the IF amplifiers by varying the input frequency. Determine and record the center frequency (IF frequency) of the IF amplifiers.

2. Amplitude Limiting:

- a. Adjust the signal generator frequency to the IF center frequency determined in the last section. The amplitude of the input sine wave should be 0.5 Vpp and connected to the 1:100 attenuator.
- b. Connect the input signal (1:100 attenuator) and the output signal (IFs Out) to a dual trace oscilloscope. Increase the input amplitude until the IFs Out signal starts to become limited. Measure the input amplitude when disconnected from the circuit with the oscilloscope. Calculate the actual amplitude driving the IF stages by dividing the measured amplitude by 100 (due to the 1:100 attenuator). Record this value on the data sheet.
- c. Increase the input amplitude so the output amplitude is fully limited. Measure and record the limited output amplitude using the oscilloscope.
- d. Connect IFs Out to the oscilloscope in place of IFs Out. Vary the input amplitude until the output starts to become limited. Again determine and record the open circuit input amplitude (1:100 value divided by 100).
- e. Increase the input amplitude so the output amplitude is fully limited. Measure and record the limited output amplitude.

3. Bandwidth Limiting:

- a. Connect a 455 kHz, 1 Vpp sine wave to the 1:1000 attenuator (actually a 1 mVpp input to the IF amplifiers) measured with a frequency counter and oscilloscope. Measure the amplitude with the signal disconnected from the 1:1000 attenuator.
- b. Connect IFs Out to the spectrum analyzer and observe the spectrum at 455 kHz.
- c. Vary the input frequency and trace the frequency response on the spectrum analyzer.
- d. Measure the 3 dB points and determine the bandwidth of the IF amplifier at this input amplitude. Record this bandwidth.

- e. Adjust the input to the 1:1000 attenuator to 2 Vpp open circuit. Again trace the frequency response on the spectrum analyzer. Determine and record the 3 dB bandwidth at this amplitude setting.
- f. Do the same for 3 Vpp through 10 Vpp in 1 Vpp increments. Notice the limiting on the amplifier bandwidth.

The Complete FM Superhetrodyne Receiver

Objective: To study the operation of the FM superhetrodyne receiver with and without automatic frequency control (AFC).

1. AFC Control of the Local Oscillator (LO):

- a. Connect T.P. Counter on Unit COM-2/3 to a frequency counter. Adjust P_1 to set the LO frequency at 1455 kHz.
- b. Connect a DVM, set to measure Vdc, to the DC power supply output. Adjust the power supply to 0 Vdc. Connect the power supply with the DVM to DC In of the amplifier A_1 .
- c. Vary the DC voltage between -3 and +5 Vdc, measuring the LO frequency for each voltage input. Plot the LO frequency versus DC voltage on the provided graph paper.

2. Mixer Operations:

- a. Generate a 455 kHz, 0.5 Vpp sine wave using a signal generator. Use the frequency counter and oscilloscope to make the measurements. Connect this signal to RF In on Unit COM-2/3.
- b. Connect the spectrum analyzer and frequency counter to the mixer output (IF Out).
- c. Determine the center frequency of the mixer by tracing the frequency response on the spectrum analyzer. Do this by varying the signal generator frequency. Record this center frequency as the IF frequency of the mixer.

- d. Also measure and record the 3 dB bandwidth of the mixer.
3. Operation Without AFC:
- a. Assemble the circuit as shown in figure 4.

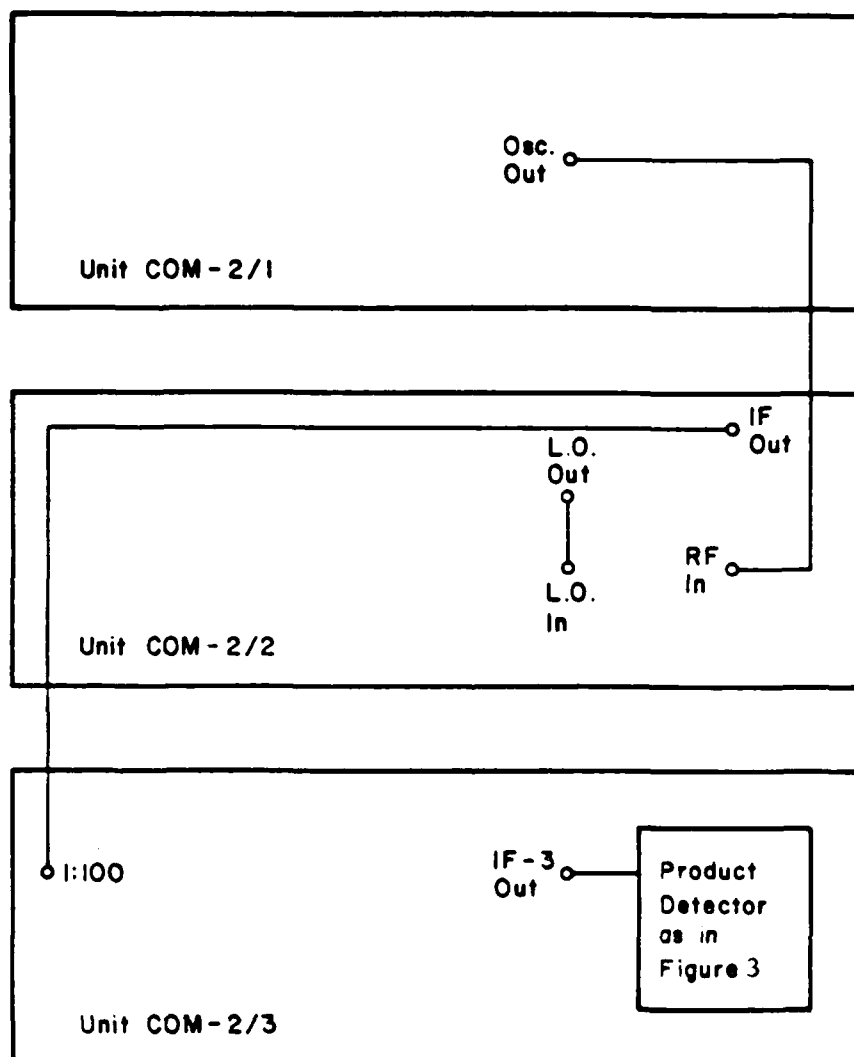


Figure 4. FM Receiver Circuit Without AFC. (2:37)

- b. Adjust the FM Oscillator on Unit COM-2/1 to 1 MHz at 0.5 Vpp using the frequency counter and oscilloscope.
 - c. Connect the frequency counter to T.P. Counter on Unit COM-2/3. Set the LO on Unit COM-2/3 to 1 MHz plus the mixer IF frequency by adjusting P₁ on this board.
 - d. Generate a 1 kHz, 1 Vpp sine wave from the signal generator making measurements with the frequency counter and oscilloscope. Connect this signal to Mod. In on Unit COM-2/1.
 - e. Connect AF Out on Unit COM-2/2 to the oscilloscope. Adjust the LO frequency slightly until a maximum amplitude sine wave is obtained at AF Out.
 - f. Connect the frequency counter to Osc. Out on Unit COM-2/1 and the spectrum analyzer to AF Out on Unit COM-2/2. Observe the AF Out spectrum at the 1 kHz signal component.
 - g. Increase the center frequency of the FM modulator on Unit COM-2/1 until the 1 kHz component has dropped by 3 dB. Disconnect Mod. In momentarily and measure the FM Modulator frequency with a frequency counter. Record this frequency as the upper 3 dB point on the data sheet.
 - h. Connect Mod. In again and decrease the center frequency of the modulator until the 1 kHz component has again dropped by 3 dB. Disconnect Mod. In and again measure the center frequency with a frequency counter. Record this frequency as the lower 3 dB point on the data sheet.
 - i. Calculate and record the difference between these two 3 dB frequencies. This is the frequency range of the receiver when it is tuned to a 1 MHz carrier without AFC.
4. Operation With AFC:
- a. Connect DC Out on Unit COM-2/2 to DC In of amplifier A₁ on Unit COM-2/3. This is the AFC feedback line.

- b. Readjust the carrier of the FM Modulator to 1 MHz without a modulation input. Use a frequency counter to measure the signal. Reconnect the modulation input.
- c. Connect the frequency counter to T.P. counter and set the LO to 1 MHz plus the IF frequency.
- d. Observe Mod. In and AF Out on the dual trace oscilloscope.
- e. Connect the spectrum analyzer to AF Out and observe the 1 kHz spectral component. Connect the frequency counter to RF In.
- f. Adjust the LO frequency slightly to obtain a maximum 1 kHz pulse.
- g. Increase the FM signal carrier frequency until the 1 kHz component has dropped by 3 dB. Disconnect Mod. In and measure the RF In frequency. Record this frequency as the upper 3 dB point on the data sheet. Reconnect Mod. In.
- h. Decrease the carrier frequency until the 1 kHz component has again dropped by 3 dB. Record the RF In frequency after disconnecting Mod. In. This is the lower 3 dB point.
- i. Calculate and record the difference between these two frequencies. This is the frequency range of the receiver set to receive a 1 MHz signal with AFC.
- j. Reset the FM carrier frequency to 1 MHz. Connect the frequency counter to T.P. Counter to measure the LO frequency.
- k. Vary the FM carrier and notice how the frequency of the LO changes with the input carrier. This is due to the AFC attempting to keep the LO frequency locked onto the RF signal. Observe that at a certain point the LO frequency stops changing and the detector output signal becomes very distorted.

STUDENT NAMES _____ DATE PERFORMED _____

Note: Indicate unit of measurement with each data entry.

FM OSCILLATOR

Range A: Low Frequency _____

High Frequency _____

Range B: Low Frequency _____

High Frequency _____

FM MODULATOR

	Modulation Amplitude	Frequency Deviation
First Carrier Dropout	_____	_____
Second Carrier Dropout	_____	_____
Third Carrier Dropout	_____	_____
Sensitivity (K _{FM})	_____	

RATIO DETECTOR

Sine Wave Max. Amplitude _____

Triangular Max. Amplitude _____

Rectangular Max. Amplitude _____

IF AMPLIFIERS

Center Frequency _____

IFs Input Limiting Ampl. _____

Output Limited Ampl. _____

IF₂ Input Limiting Ampl. _____

Output Limited Ampl. _____

Input Ampl.	Bandwidth	Input Ampl.	Bandwidth
1 mVpp	_____	6 mVpp	_____
2 mVpp	_____	7 mVpp	_____
3 mVpp	_____	8 mVpp	_____
4 mVpp	_____	9 mVpp	_____
5 mVpp	_____	10 mVpp	_____

MIXER

Center Frequency (IF) _____

Bandwidth _____

OPERATION WITHOUT AFC

3 dB Points _____

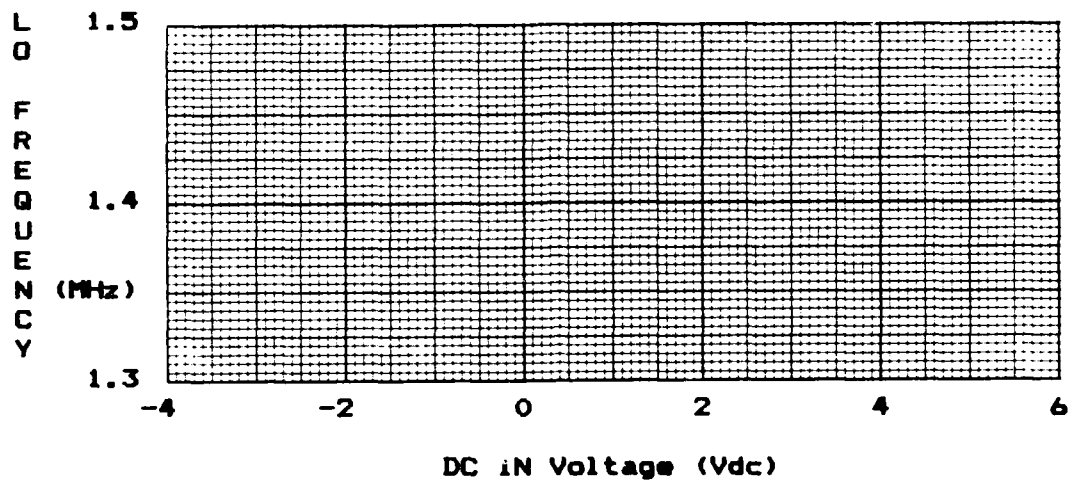
Frequency Range _____

OPERATION WITH AFC

3 dB Points _____

Frequency Range _____

AFC CHARACTERISTIC CURVE



STUDENT NAMES SAMPLE DATE PERFORMED

Note: Indicate unit of measurement with each data entry.

FM OSCILLATOR

Range A: Low Frequency 900.64 kHz
High Frequency 1296.40 kHz
Range B: Low Frequency 422.98 kHz
High Frequency 479.02 kHz

FM MODULATOR

	Modulation Amplitude	Frequency Deviation
First Carrier Dropout	<u>105 mVp</u>	<u>2.405 kHz</u>
Second Carrier Dropout	<u>240 mVp</u>	<u>5.520 kHz</u>
Third Carrier Dropout	<u>384 mVp</u>	<u>8.654 kHz</u>
Sensitivity (K _{FM})	<u>22.81 kHz/Vp</u>	

RATIO DETECTOR

Sine Wave Max. Amplitude 7.8 Vpp
Triangular Max. Amplitude 7.8 Vpp
Rectangular Max. Amplitude 7.8 Vpp

IF AMPLIFIERS

Center Frequency 456.63 kHz
IFs Input Limiting Ampl. 6 mVpp
Output Limited Ampl. 1.4 Vpp

IF₂ Input Limiting Ampl. 60 mVppOutput Limited Ampl. 1.4 Vpp

Input Ampl.	Bandwidth	Input Ampl.	Bandwidth
1 mVpp	<u>36.80</u> kHz	6 mVpp	<u>51.73</u> kHz
2 mVpp	<u>39.31</u> kHz	7 mVpp	<u>53.64</u> kHz
3 mVpp	<u>41.70</u> kHz	8 mVpp	<u>56.31</u> kHz
4 mVpp	<u>45.71</u> kHz	9 mVpp	<u>56.76</u> kHz
5 mVpp	<u>49.00</u> kHz	10 mVpp	<u>57.60</u> kHz

MIXER

Center Frequency (IF) 458.32 kHzBandwidth 8.03 kHz

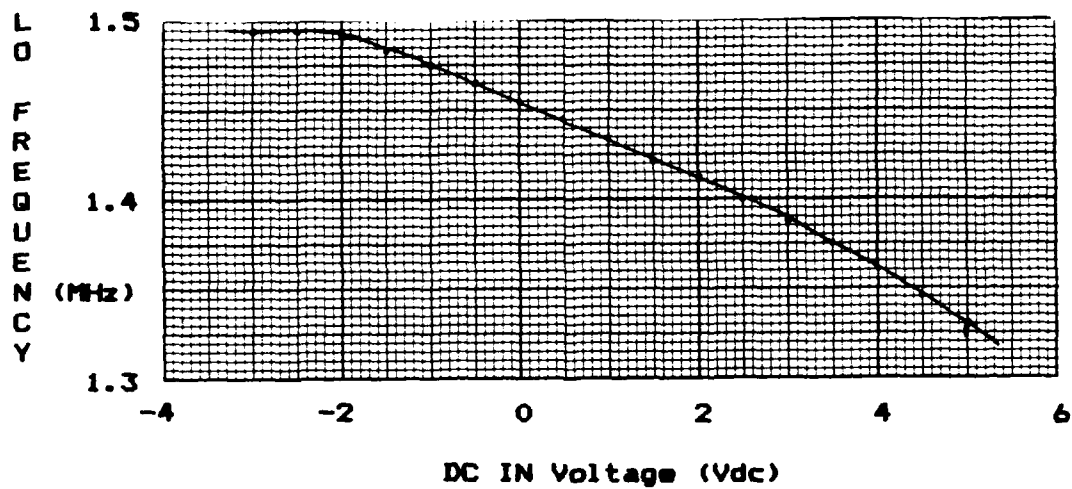
OPERATION WITHOUT AFC

3 dB Points 987.13 kHz 1009.25 kHzFrequency Range 22.12 kHz

OPERATION WITH AFC

3 dB Points 980.44 kHz 1029.87 kHzFrequency Range 49.43 kHz

AFC CHARACTERISTIC CURVE



APPENDIX E

Laboratory Experiment Number 3-S

Frequency Modulation Set-Up

This experiment provides a procedure for use by instructors or technicians to tune several circuit components on the boards used by students performing laboratory experiment number 3, Frequency Modulation.

OBJECTIVE: To enable the instructor or technician to tune the DEGEM Unit COM-2/1 and 2/2 boards for use by students performing Lab 3, "Frequency Modulation".

PREREQUISITES: Familiarization of all required equipment. Completion of Lab 1, "Equipment Familiarization", is recommended.

REQUIRED EQUIPMENT

The following equipment is required to tune the DEGEM boards used in the Lab 3 experiment.

1. Oscilloscope (dual trace)
2. Spectrum Analyzer (0 to 2 MHz minimum)
3. Signal Generator (sine wave)
4. Frequency Counter (0 to 2 MHz minimum)
5. Digital Volt Meter (DVM -2Vdc to 2 Vdc minimum)
6. Test Leads
7. Transformer Tuning Tool
8. DEGEM PS-MB-1/A Power Supply Board
9. DEGEM Boards Unit COM-2/1
Unit COM-2/2
10. Masking Tape

REFERENCES

1. DEGEM Systems Ltd. AM and FM Communication Circuits Courses COM-1 and COM-2 Theoretical Background Manual. DEGEM Systems Ltd., 1976.
2. DEGEM Systems Ltd. FM Communication Circuits System COM-2 Experiment and Technical Manual. DEGEM Systems Ltd., 1976.

PROCEDURE

General Instructions

WARNING

Turn the DEGEM Power Supply Board off before removing or inserting any plug-in boards. Damage to circuit components may result if the boards are changed while the power is on.

1. DO NOT turn the DEGEM PS-MB-1/A Power Supply Board on. Install the Unit COM-2/1 and 2/2 boards into the power supply board by pressing each unit into a power socket and tightening the hold-down screws on each end of the unit.
2. Turn the power supply board on. All plug-in units are internally powered and therefore need no external power connections.
3. Turn all of the remaining equipment on.

Ratio Detector

Objective: To tune the ratio detector for best detection of an FM signal.

1. Set-up:
 - a. Connect a frequency counter to Osc. Out on the Unit COM-2/1 board.
 - b. Set potentiometer P_2 fully cw.
 - c. Use Range B and adjust potentiometer P_1 so the carrier is 455 kHz.
 - d. Generate a 1 kHz, 3 Vpp sine wave from a signal generator using a frequency counter and oscilloscope to make measurements. Connect this signal to Mod. In on the FM Modulator.
 - e. Connect the FM signal at Osc. Out to FM In of the ratio detector as shown in figure 1. Connect C_4 to R_8 as shown.
 - f. Connect Mod. In and V_{out} to a dual trace oscilloscope. Also connect a DVM (set to Vdc) to V_{out} .
2. Tuning the Ratio Detector:
 - a. Turn transformer T_2 almost fully cw but DO NOT JAM the adjusting screw. Turn the transformer T_1 almost fully ccw but do not allow the adjusting screw to come out of the transformer.

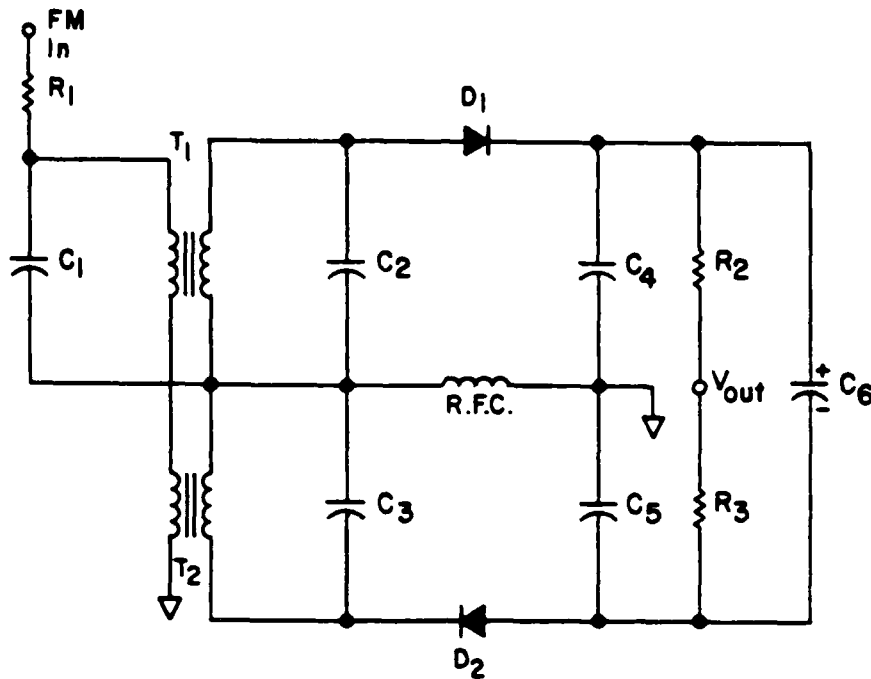


Figure 1. Ratio Detector. (2:26)

- b. Adjust T_2 ccw slightly and then adjust T_1 cw until the DVM reads zero volts.
- c. Make sure the trace of the detected waveform at V_{out} is not distorted. If it is distorted, adjust T_2 slightly and then T_1 to achieve zero volts again. Again check for distortion.
- d. Continue adjusting T_1 and T_2 until a clear, un-distorted waveform is detected and the dc level at V_{out} is zero volts.

Product Detector

Objective: To tune the product detector using an input sine wave signal set at the center frequency of IF amplifier stages.

1. Determining the Intermediate Frequency of the IF Amplifiers:
 - a. Connect a 455 kHz, 0.5 Vpp sine wave from a signal generator to the 1:100 attenuator input on Unit COM-2/2.
 - b. Connect IFs Out to the Spectrum Analyzer and observe the spectral component at 455 kHz.
 - c. Trace out the frequency response of the IF amplifiers by varying the input frequency. Determine the center frequency (IF frequency) of the IF amplifiers.
2. Tuning the Phase Shifting Network of the Product Detector:
 - a. Set the FM oscillator on Unit COM-2/1 to 0.5 Vpp at the IF frequency determined in the last section. Use an oscilloscope and frequency counter to make the measurements.
 - b. Connect a 1 kHz, 1 Vpp sine wave from a signal generator to Mod. In on the FM oscillator.
 - c. Connect the product detector, IF amplifiers, and FM oscillator as shown in figure 2.
 - d. Connect one channel of the dual trace oscilloscope to AF Out on Unit COM-2/2. Connect the other channel to the signal generator (input modulation signal). Observe both traces on the oscilloscope and use the time delay and vertical amplifier verniers to line up the traces.
 - e. Adjust inductor L₁ on the Unit COM-2/2 board so the AF Out signal is an undistorted sine wave.
 - f. Increase the modulation signal from the signal generator until the detector output becomes slightly distorted.
 - g. Adjust L₁ again to get the best sine wave possible. The product detector is now tuned.

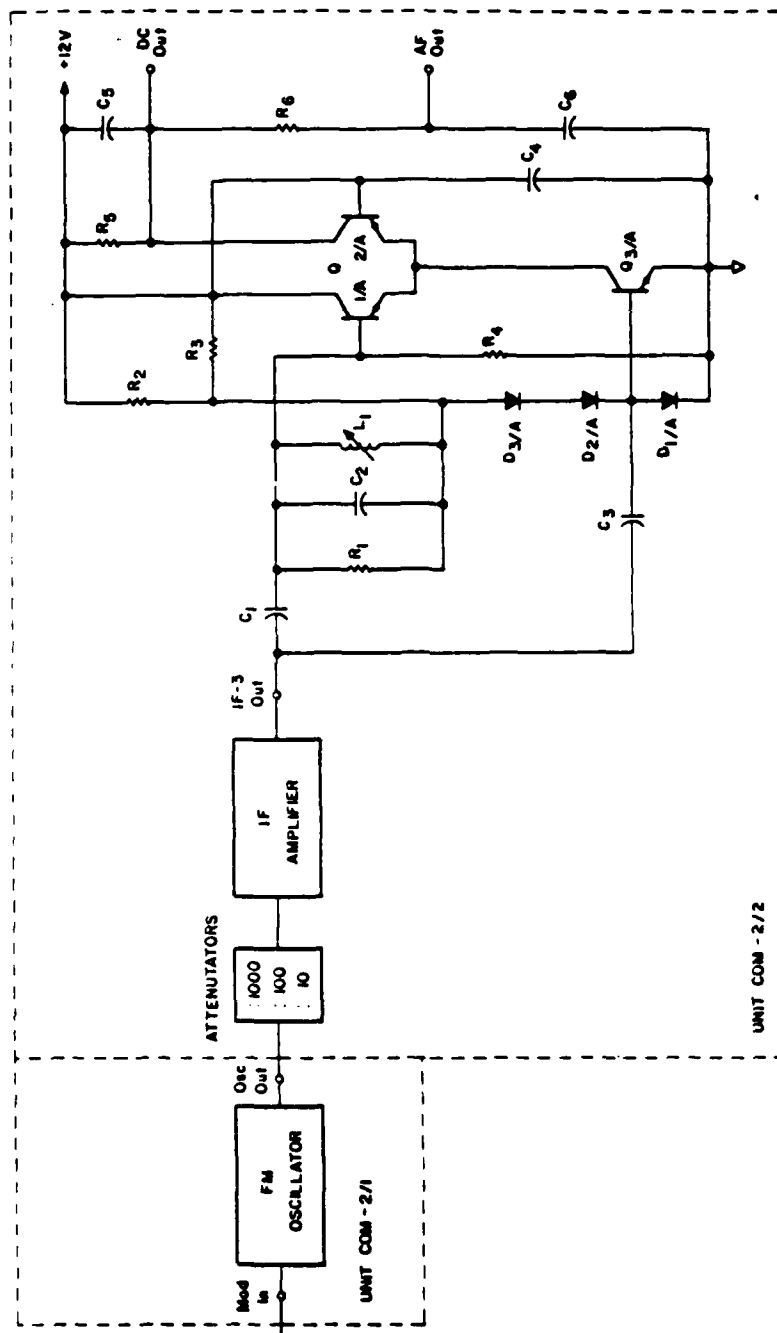


Figure 2. Circuit for Tuning the Product Detector. (2:32)

APPENDIX F

Laboratory Experiment Number 4

Balanced Modulator

This experiment studies the characteristics of balanced modulator used as a mixer, AM detector, phase detector, and double sideband-suppressed carrier AM modulator.

OBJECTIVE: To familiarize the student with the operation of the balanced modulator as a mixer, detector, and modulator.

PREREQUISITES: Completion of Lab 1, "Equipment Familiarization".

REQUIRED EQUIPMENT

The following equipment is required to perform this experiment. It is assumed the student is familiar with the controls and functions of each item listed below.

1. Oscilloscope (dual trace)
2. Spectrum Analyzer (0 to 2 MHz minimum)
3. 2 Signal Generators (CW capability)
4. Frequency Counter (0 to 2 MHz minimum)
5. Decade Resistor Bank (0 Ω to 10 k Ω)
6. Digital Volt Meter (DVM) (-20 to +20 Vdc minimum)
7. Test Leads
8. DEGEM PS-MB-1/A Power Supply Board
9. DEGEM Boards Unit COM-3/1
Unit COM-3/2
Unit COM-3/3

REFERENCES

1. DEGEM Systems Ltd. SSB Communication Circuits System COM-3 Theoretical Background Manual. DEGEM Systems Ltd., 1976.
2. DEGEM Systems Ltd. SSB Communication Circuits System COM-3 Experiment and Technical Manual. DEGEM Systems Ltd., 1976.

THEORETICAL BACKGROUND

SOURCE: Reference (1)

Chapter 1 - The Balanced Modulator

Additional Background

The balanced modulator can be used as a mixer, AM detector, phase detector, and modulator. Figures 1 through 4 show the block diagrams for the balanced modulator circuit in each of these configurations.

Figure 1 shows the block diagram of the the balanced modulator used as a mixer. In this case, the local oscillator and signal generator frequencies are relatively close and the output of the circuit is at an intermediate frequency (IF).

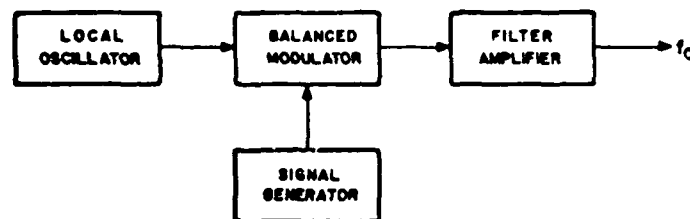


Figure 1. Balanced Modulator used as a Mixer. (2:27)

Figure 2 shows the block diagram for an AM detector. The balanced modulator acts as a synchronous detector. The carrier, or RF signal, is used as a reference for the modulator to detect the envelope of the AM signal.

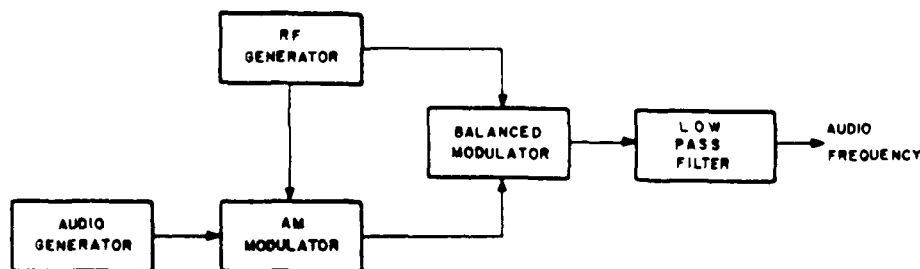


Figure 2. Balanced Modulator used as an AM Detector. (2:33)

Figure 3 shows the diagram for a phase detector. A phase reference signal and the phase shifted signal are applied to the balanced modulator circuit. The dc component that is filtered out represents the phase shift of the incoming signal compared to the phase reference signal.

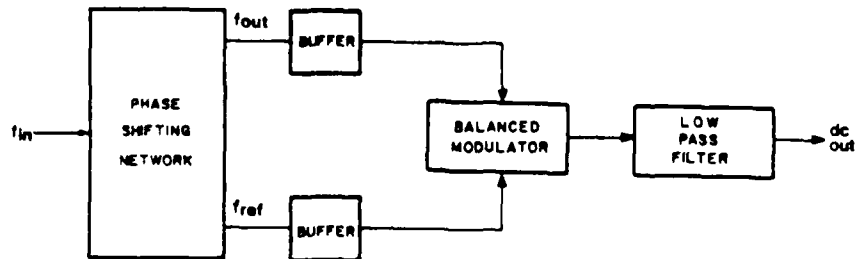


Figure 3. Balanced Modulator used as a Phase Detector. (2:35)

Figure 4 shows the balanced modulator being used as a double sideband-suppressed carrier (DSB-SC) modulator. In this case, the audio signal has a much lower frequency than the local oscillator (RF carrier). The result is a modulated waveform.

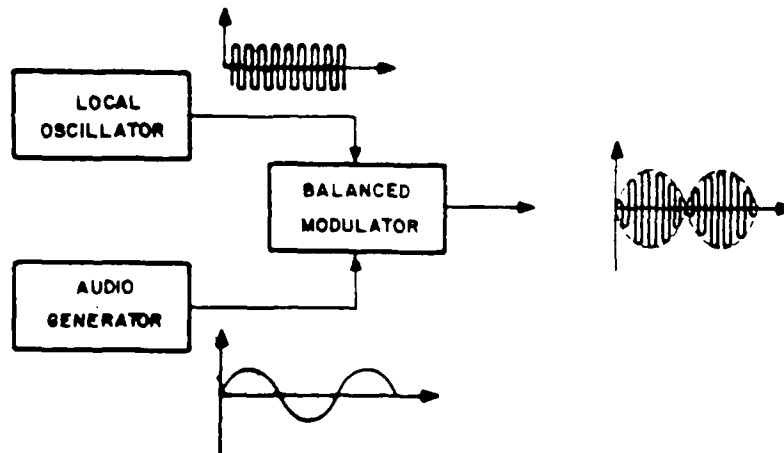


Figure 4. Balanced Modulator used as a DSB-SC Modulator. (2:38)

DEGEM CIRCUIT BOARD DESCRIPTION

SOURCE: Reference (2).

Technical Description of Plug-In Units

- Unit COM-3/1
- Unit COM-3/2
- Unit COM-3/3

EXPERIMENT PROCEDURE**General Instructions****WARNING**

Turn the DEGEM Power Supply Board off before removing or inserting any plug-in boards. Damage to circuit components may result if the boards are changed while the power is on.

1. DO NOT turn the DEGEM PS-MB-1/A Power Supply Board on. Install the Unit COM-3/1, 3/2 and 3/3 boards into the power supply board by pressing each unit into a power socket and tightening the hold-down screws on each end of the unit.
2. Turn the power supply board on. All plug-in units are internally powered and therefore need no external power connections.
3. Turn all of the remaining equipment on.

Amplifier-Filter Circuit

Objective: To determine the bandwidth, center frequency, and gain of the amplifier-filter circuit.

1. Generate a 100 kHz, 200 mVpp sine wave, from the signal generator, using a frequency counter and oscilloscope to make the measurements. Connect this signal to C₆ on Unit COM-3/3. Connect the output of the amplifier (C₇) to an oscilloscope and spectrum analyzer.
2. Observe the output on the analyzer at 100 kHz. Trace the frequency response on the analyzer by varying the input frequency. Determine and record the center frequency and 3 dB bandwidth of this response curve.

3. Set the input frequency to the center frequency of the amplifier. Remove the spectrum analyzer from the circuit and observe the input and output of the amplifier on the oscilloscope. Determine and record the gain of the amplifier.

Balanced Modulator Used as a Mixer

Objective: To observe the operation of the balanced modulator used as a mixer. To also determine the gain of the mixer, conversion loss as a function of load, and the effect of spurious responses.

1. Mixing Operation:

- a. Generate a 450 kHz, 250 mVpp sine wave with a signal generator using a frequency counter and oscilloscope to make measurements. This signal will be called the local oscillator (LO) signal.
- b. Generate a 550 kHz, 200 mVpp sine wave with a second signal generator using a frequency counter and oscilloscope to make measurements. This signal will be called the RF signal.
- c. Construct the circuit as shown in figure 5. Connect the signal generators to their respective inputs (RF IN and LO IN).
- d. Connect a spectrum analyzer to the output of the amplifier-filter (C7) and observe the spectrum at 100 kHz.
- e. Measure and record the following frequencies using a frequency counter.

IF Frequency at C7

LO Frequency at LO IN (may need to disconnect from circuit)

RF Frequency at RF IN (may need to disconnect from circuit)

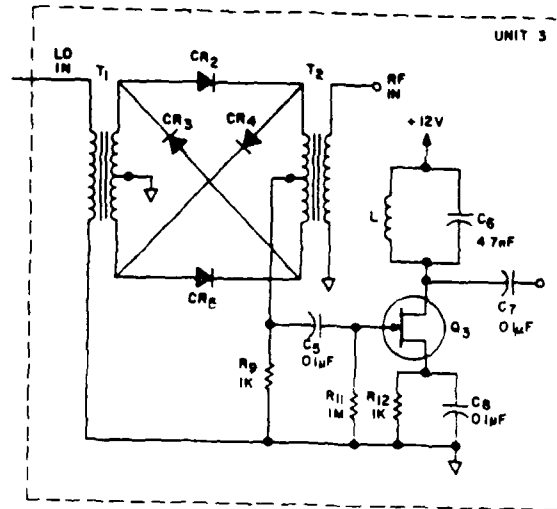


Figure 5. The Mixer Circuit. (2:28)

2. IF OUT to RF IN Gains:

- a. Remove the frequency counter from the circuit to prevent any unnecessary loads.
- b. Connect a dual trace oscilloscope to RF IN and IF OUT (C7). Measure and record the IF to RF gains for RF closed circuit amplitudes of 20 mVpp to 160 mVpp in 20 mVpp increments.

3. Conversion Loss as Function of Load:

- a. Adjust the LO amplitude to 250 mVpp closed circuit. Also adjust the RF amplitude to 120 mVpp closed circuit. Remove the jumper between resistor R6 and ground. Connect the dual trace oscilloscope to R6 and to LO IN (T1 primary).
- b. Determine and record the input impedance by dividing the input voltage by the input current, or:

$$R_{IN} = (V_{LO})(100 \Omega) / V_{R6} \quad \text{ohms}$$

where V_{LO} and V_{RF} are measured peak-to-peak.

- c. Calculate and record the input power by:

$$P_{IN} = (V_{LO}/2)(V_{RF}/2) / (100 \Omega)(1.414) \quad W_{rms}$$

- d. Connect the decade resistor bank in place of resistor R_2 keeping R_1 in the circuit. Connect the oscilloscope to C_2 .

- e. Set the decade resistor bank (R_L) to 50Ω and measure the C_2 amplitude. Determine and record the output power from:

$$P_{OUT} = (V_{C_2}/2)^2 / (Gain)^2(R_L)(1.414) \quad W_{rms}$$

where V_{C_2} is measured peak-to-peak and Gain is the gain of the amplifier for an RF input of 120 mVpp previously measured.

- f. Also calculate and record the conversion loss from:

$$Loss (dB) = 10 \log_{10} (P_{IN}/P_{OUT})$$

- g. Perform the same measurements and calculations for load resistances of 100, 200, 400, 1k, 3k and 10k Ω . Record the values on the data sheet.

4. Spurious Responses of the Balanced Modulator:

- Connect the circuit again as was shown in figure 5. Generate a 450 kHz, 250 mVpp sine wave LO signal with a signal generator and a 550 kHz, 200 mVpp sine wave RF signal with another. Use the frequency counter and oscilloscope to make measurements.
- Connect the spectrum analyzer to the output of the amplifier-filter (C_2) on Unit COM-3/3. Observe the spectrum at 100 kHz.
- Measure the amplitude of the 100 kHz spectral component on the spectrum analyzer in dBV. Record the amplitude on the data sheet for an RF of 550 kHz.
- Calculate and record the RF frequencies for the following equations using $f_{LO} = 450$ kHz and f_{IF} = center frequency of the amplifier-filter.

$f_{LO} - f_{IF}$	$(f_{LO} - f_{IF}) / 2$
$f_{LO} + f_{IF}$	$(f_{LO} + f_{IF}) / 2$
$2f_{LO} - f_{IF}$	$(f_{LO} - f_{IF}) / 3$
$2f_{LO} + f_{IF}$	$(f_{LO} + f_{IF}) / 3$
$3f_{LO} - f_{IF}$	$(2f_{LO} - f_{IF}) / 2$
$3f_{LO} + f_{IF}$	$(2f_{LO} + f_{IF}) / 2$
f_{IF}	

- d. While keeping the LO and RF amplitudes constant at all times, set the RF frequency to each of the frequencies calculated. It may be necessary to disconnect the RF input to measure the frequency. For each frequency, vary the RF frequency slightly to set the spectral component of the amplifier output at 100 kHz. Measure and record the amplitude of the 100 kHz spectral component in dBV for each RF frequency using the spectrum analyzer.

Balanced Modulator as a Detector

Objectives: To observe the operation of the balanced modulator as an AM detector and a phase detector.

1. AM Detector:

- Generate a 500 kHz, 250 mVpp sine wave from a signal generator measured with a frequency counter and oscilloscope. Call this signal the LO signal.
- Using a second signal generator, generate a 1 kHz, 100 mVpp sine wave measured with a frequency counter and oscilloscope. Call this signal the Audio signal.
- Connect the AM detector circuit as shown in figure 6. Make sure proper connections of the balanced modulator are made.
- Turn potentiometer P₃ on Unit COM-3/1 fully cw.
- Connect a dual trace oscilloscope to the amplitude modulator output (AM OUT) and to the four signal on Unit COM-3/1. Also connect the spectrum analyzer to the four signal.

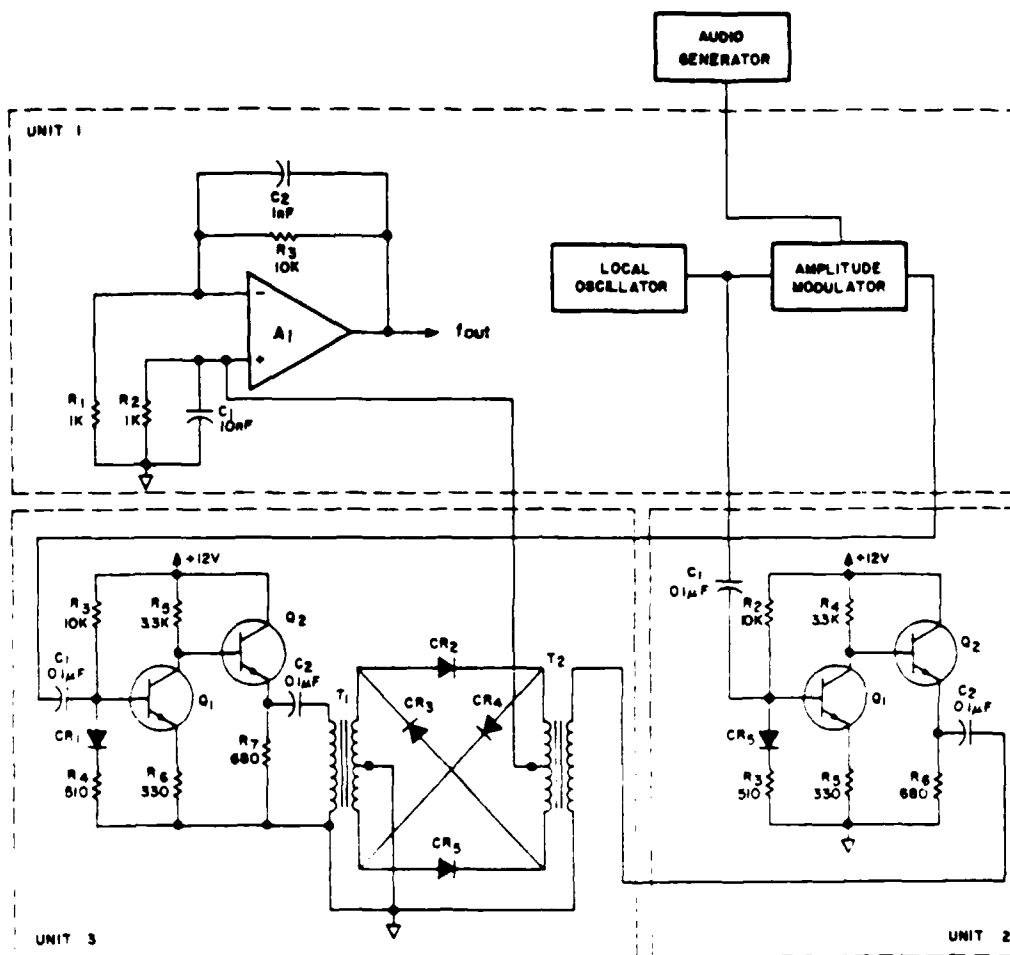


Figure 6. AM Detector Circuit. (2:34)

- f. Observe both traces on the oscilloscope at 1 msec/DIV. Vary the Audio signal amplitude and notice a change in the modulation index and output waveforms.

2. Phase Detector:

- a. Assemble the circuit as shown in figure 7.

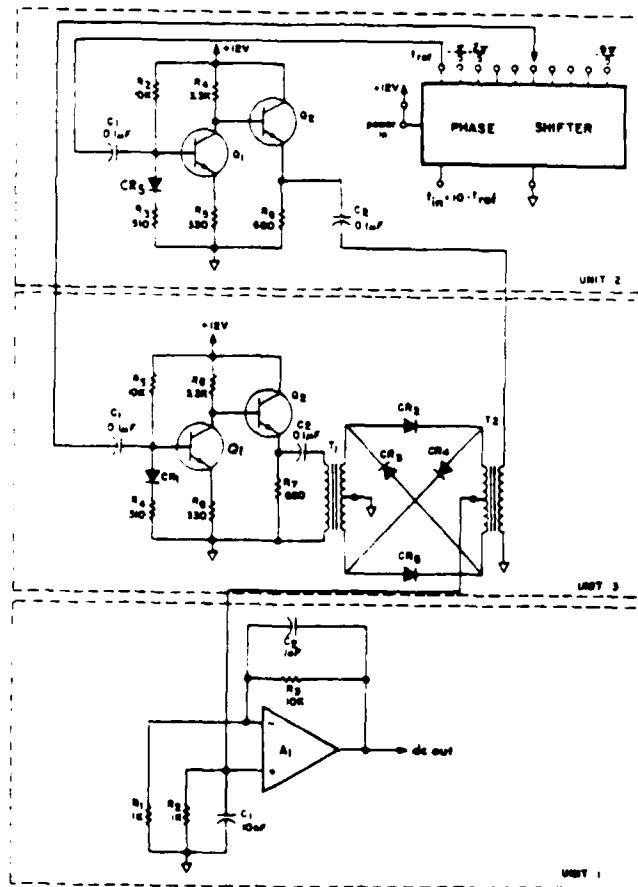


Figure 7. Phase Detector Circuit. (2:35)

- b. Generate a 100 kHz TTL (0 to +5 Vdc) square wave signal from a signal generator. Connect this signal to f_{IN} on the phase shifter located on Unit COM-3/2.
- c. Connect a dual trace oscilloscope to the f_{REF} of the phase shifter. The other channel will be connected to the phase shifter tap that is currently connected

to the detector circuit. Also connect a DVM to output of the op-amp circuit on Unit COM-3/1 (dc out).

- d. Connect the detector circuit (C₁ on Unit COM-3/3) and the second channel of the oscilloscope to the **f_{REF}** signal.
- e. Measure and record the dc level from the detector output amplifier.
- f. Measure and record the output dc level for all the phase shifted taps. In each case observe the shifted waveforms on the oscilloscope as compared to the **f_{REF}** signal.

Balanced Modulator used as a DSB-SC Modulator

Objective: To observe the operation of the balanced modulator as a double sideband-suppressed carrier modulator.

1. Generate a 455 kHz, 500 mVpp sine wave from a signal generator using a frequency counter and oscilloscope to make measurements. Call this signal the LO signal.
2. Using another signal generator, generate a 4 kHz, 500 mVpp sine wave using the frequency counter and oscilloscope to make measurements. Call this signal the Audio signal.
3. Connect the circuit on Unit COM-3/2 as shown in figure 8.
4. Connect the oscilloscope to the resistor R₁ and the audio signal input. Observe the DSB-SC waveform. Vary the LO signal frequency and notice how the output waveform changes. The balanced modulator is tuned to 455 kHz and varying from this frequency causes the balanced modulator to be unbalanced.
5. Connect the spectrum analyzer (set for linear mode) to the modulator output signal and observe the spectrum at the LO frequency. Increase the LO frequency above 455 kHz and notice the carrier component increase in amplitude, forming a standard AM signal.

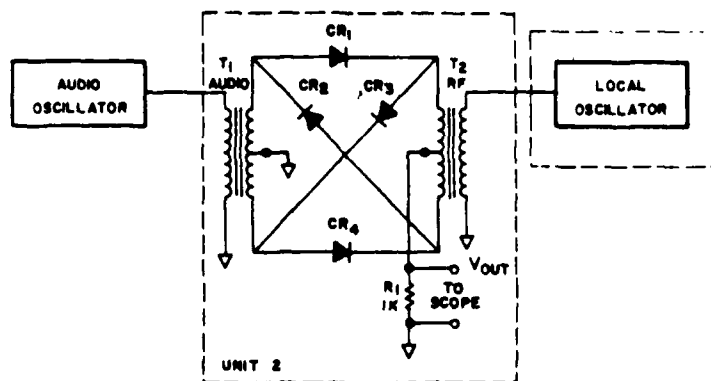


Figure 8. DSB-SC Modulation Circuit. (2:39)

6. Adjust the LO frequency for balanced operation (i.e. set the LO frequency for the best DSB-SC output waveform). Change the Audio signal waveform and observe the modulator output on the oscilloscope and spectrum analyzer.

STUDENT NAMES _____ DATE PERFORMED _____

Notes: Indicate unit of measurement with each data entry.

AMPLIFIER-FILTER CIRCUIT

Center Frequency _____

Bandwidth _____

Gain _____

BALANCED MODULATOR USED AS MIXER

 f_{IF} _____ f_{LO} _____ f_{RF} _____

RF Amplitude	Gain	RF Amplitude	Gain
20 mVpp	_____	100 mVpp	_____
40 mVpp	_____	120 mVpp	_____
60 mVpp	_____	140 mVpp	_____
80 mVpp	_____	160 mVpp	_____

Input Impedance _____

Input Power _____

Load (Ω)	Power Out (nW _{rms})	Loss (dB)	Load (Ω)	Power Out (nW _{rms})	Loss (dB)
50	_____	_____	1 k	_____	_____
100	_____	_____	3 k	_____	_____
200	_____	_____	10 k	_____	_____
400	_____	_____			

	RF (kHz)	Amplitude (dBV)		RF (kHz)	Amplitude (dBV)
	<u>550.0</u>	-----			
$f_{LO}-f_{IF}$	-----	-----	$(f_{LO}-f_{IF})/2$	-----	-----
$f_{LO}+f_{IF}$	-----	-----	$(f_{LO}+f_{IF})/2$	-----	-----
$2f_{LO}-f_{IF}$	-----	-----	$(f_{LO}-f_{IF})/3$	-----	-----
$2f_{LO}+f_{IF}$	-----	-----	$(f_{LO}+f_{IF})/3$	-----	-----
$3f_{LO}-f_{IF}$	-----	-----	$(2f_{LO}-f_{IF})/2$	-----	-----
$3f_{LO}+f_{IF}$	-----	-----	$(2f_{LO}+f_{IF})/2$	-----	-----
f_{IF}	-----	-----			

BALANCED MODULATOR USED AS A DETECTOR

AM Detector Center Frequency

Phase	DC Amplitude (V _{dc})	Phase	DC Amplitude (V _{dc})
0	-----	$-\pi$	-----
$-\pi/5$	-----	$-6\pi/5$	-----
$-2\pi/5$	-----	$-7\pi/5$	-----
$-3\pi/5$	-----	$-8\pi/5$	-----
$-4\pi/5$	-----	$-9\pi/5$	-----

STUDENT NAMES SAMPLE DATE PERFORMED

Note: Indicate unit of measurement with each data entry.

AMPLIFIER-FILTER CIRCUIT

Center Frequency 100.82 kHz

Bandwidth 40.68 kHz

Gain 8.32 (18.4 dB)

BALANCED MODULATOR USED AS MIXER

f_{IF} 99.84 kHz

f_{LO} 449.92 kHz

f_{RF} 549.78 kHz

RF Amplitude	Gain	RF Amplitude	Gain
20 mVpp	8.46 (18.5 dB)	100 mVpp	8.80 (18.9 dB)
40 mVpp	8.73 (18.8 dB)	120 mVpp	8.77 (18.9 dB)
60 mVpp	8.80 (18.9 dB)	140 mVpp	8.40 (18.5 dB)
80 mVpp	8.80 (18.9 dB)	160 mVpp	8.10 (18.2 dB)

Input Impedance 183.8 ohmsInput Power 60.1 microwatts rms

Load (Ω)	Power Out (nW _{rms})	Loss (dB)	Load (Ω)	Power Out (nW _{rms})	Loss (dB)
50	484	20.94	1 k	2270	14.24
100	847	18.51	3 k	1590	15.76
200	1330	16.55	10 k	656	19.62
400	1930	14.93			

	RF (kHz)	Amplitude (dBV)		RF (kHz)	Amplitude (dBV)
	<u>550.0</u>	<u>-32.0</u>			
$f_{LO-f_{IF}}$	<u>349.2</u>	<u>-32.1</u>	$(f_{LO-f_{IF}})/2$	<u>174.6</u>	<u>-73.8</u>
$f_{LO+f_{IF}}$	<u>550.8</u>	<u>-32.0</u>	$(f_{LO+f_{IF}})/2$	<u>275.4</u>	<u>-74.2</u>
$2f_{LO-f_{IF}}$	<u>799.2</u>	<u>-72.0</u>	$(f_{LO-f_{IF}})/3$	<u>116.4</u>	<u>-69.5</u>
$2f_{LO+f_{IF}}$	<u>1001</u>	<u>-72.4</u>	$(f_{LO+f_{IF}})/3$	<u>183.6</u>	<u>-64.5</u>
$3f_{LO-f_{IF}}$	<u>1249</u>	<u>-45.4</u>	$(2f_{LO-f_{IF}})/2$	<u>399.6</u>	<u>-71.4</u>
$3f_{LO+f_{IF}}$	<u>1451</u>	<u>-45.0</u>	$(2f_{LO+f_{IF}})/2$	<u>500.4</u>	<u>-70.8</u>
f_{IF}	<u>100.8</u>	<u>-73.4</u>			

BALANCED MODULATOR USED AS A DETECTOR

AM Detector Center Frequency 55.78 kHz

Phase	DC Amplitude (Vdc)	Phase	DC Amplitude (Vdc)
0	<u>0.866</u>	$-\pi$	<u>-0.203</u>
$-\pi/5$	<u>-0.121</u>	$-6\pi/5$	<u>0.187</u>
$-2\pi/5$	<u>-0.056</u>	$-7\pi/5$	<u>-0.031</u>
$-3\pi/5$	<u>-0.069</u>	$-8\pi/5$	<u>0.010</u>
$-4\pi/5$	<u>0.193</u>	$-9\pi/5$	<u>-0.022</u>

APPENDIX G

Laboratory Experiment Number 4-S

Balanced Modulator Set-Up

This experiment provides a procedure for use by instructors or technicians to tune several circuit components on the boards used by students performing laboratory experiment number 4, Balanced Modulator.

OBJECTIVE: To enable the instructor or technician to tune the DEGEM Unit COM-3/2 and 3/3 boards for use by students performing Lab 4, "Balanced Modulator" and Lab 5, "Single Sideband Modulation".

PREREQUISITES: Familiarization of all required equipment. Completion of Lab 1, "Equipment Familiarization", is recommended.

REQUIRED EQUIPMENT

The following equipment is required to tune the DEGEM boards used in the Lab 4 experiment.

1. Oscilloscope (dual trace)
2. Spectrum Analyzer (0 to 2 MHz minimum)
3. Signal Generator (sine wave)
4. Frequency Counter (0 to 2 MHz minimum)
5. Test Leads
6. Flat Blade Screwdriver
7. DEGEM PS-MB-1/A Power Supply Board
8. DEGEM Boards Unit COM-3/2
Unit COM-3/3

REFERENCES

1. DEGEM Systems Ltd. SSB Communication Circuits Course COM-3 Theoretical Background Manual. DEGEM Systems Ltd., 1976.
2. DEGEM Systems Ltd. SSB Communication Circuits Course COM-3 Experiment and Technical Manual. DEGEM Systems Ltd., 1976.

PROCEDURE

General Instructions

WARNING

Turn the DEGEM Power Supply Board off before removing or inserting any plug-in boards. Damage to circuit components may result if the boards are changed while the power is on.

1. DO NOT turn the DEGEM PS-MB-1/A Power Supply Board on. Install the Unit COM-3/2 and 3/3 boards into the power supply chassis by pressing each unit into a power socket and tightening the hold-down screws on each end of the unit.
2. Turn the power supply board on. All plug-in units are internally powered and therefore need no external power connections.
3. Turn all of the remaining equipment on.

Tuning the Amplifier-Filter Circuit on Unit COM-3/3

Objective: To check and tune, if necessary, the center frequency of the amplifier-filter circuit.

1. Checking the Center Frequency:
 - a. Generate a 100 kHz, 200 mVpp sine wave from a signal generator. Use a frequency counter and oscilloscope to make the measurements. Connect this signal to C₅ on Unit COM-3/3.
 - b. Connect the spectrum analyzer to C₇ on Unit COM-3/3 and observe the spectrum at 100 kHz. Vary the input frequency and trace the amplifier frequency response on the analyzer. Determine the center frequency. If this frequency is between 99.0 kHz and 101.0 kHz, skip step 2 below.
2. Adjusting the center frequency:
 - a. Turn off the power supply board and pull the Unit COM-3/3 board out of the power supply board. Remove the back cover of Unit COM-3/3. Make external +12 Vdc and ground connections between the power supply board and the Unit COM-3/3 board. Turn the power supply board on.
 - b. On the back side of the board, adjust the ferrite core, marked L, until the 100 kHz spectral component is maximum. Trace the frequency response on the analyzer by varying the input frequency. Make certain the center frequency is between 99.0 kHz and 101.0 kHz. If it is not, readjust L.

Tuning the Balanced Modulator on Unit COM-3/3

Objective: To check and tune, if necessary, the transformers making up the balanced modulator on Unit COM-3/3.

1. Checking T_2 of the Balanced Modulator:

- a. Connect a 455 kHz (± 200 Hz), 250 mVpp sine wave to the primary of T_2 on Unit COM-3/3 as shown in figure 1. Make all other connections as shown in the figure. Note that T_1 should be open circuited.

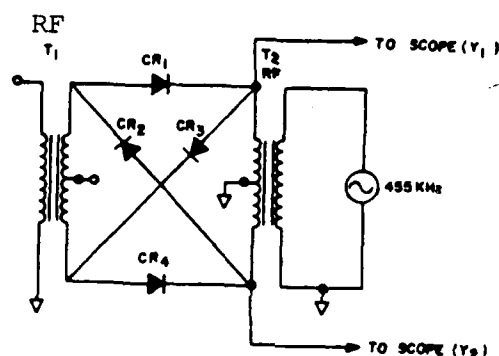


Figure 1. Balanced Modulator Test Circuit. (2:17)

- b. Observe Y_1 and Y_2 on the oscilloscope. If the amplitudes of Y_1 and Y_2 are not equal, then the T_2 must be tuned. If the amplitudes are equal, skip step 2 below.
- #### 2. Tuning T_2 :
- a. Turn off the power supply board and remove the back cover of Unit COM-3/3 if this has not been done so already.
 - b. Using the flat blade screwdriver, adjust the ferrite cores on the back side of the board that correspond to the transformer until the secondary amplitudes are equal.

3. Checking T_1 of the Balanced Modulator:

- a. Remove the input signal from T_2 and connect it to the primary of T_1 . Remove the jumper between the center tap of T_2 and ground. Connect the center tap of T_1 to ground. Connect the oscilloscope to the top and bottom terminals of the secondary of T_1 instead of T_2 .
- b. Observe the T_1 secondary outputs on the oscilloscope. If the amplitudes are not equal, then the T_1 must be tuned. If the amplitudes are equal, skip step 4 below.

4. Tuning T_1 :

- a. Turn off the power supply board and remove the back cover of Unit COM-3/3 if this has not been done so already.
- b. Using the flat blade screwdriver, adjust the ferrite cores on the back side of the board that correspond to the transformer until the secondary amplitudes are equal.

Tuning the Balanced Modulator on Unit COM-3/2

Objectives: To check and tune, if necessary, transformer T_2 of the balanced modulator on Unit COM-3/2. The audio transformer is not tunable.

1. Checking T_2 of the Balanced Modulator:

- a. Connect a 455 kHz (± 200 Hz), 250 mVpp sine wave to the primary of T_2 on Unit COM-3/2 as shown in figure 2. Make all other connections as shown in the figure. Note that T_1 should be open circuited.
- b. Observe Y_1 and Y_2 on the oscilloscope. If the amplitudes of Y_1 and Y_2 are not equal, then the T_2 must be tuned. If the amplitudes are equal, skip step 2 below.

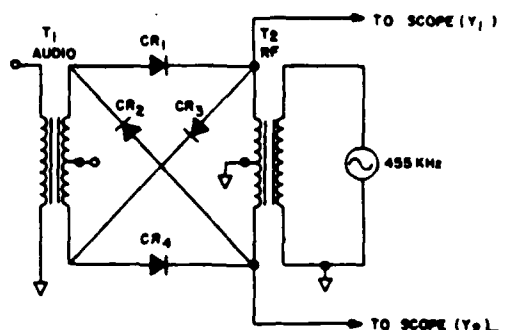


Figure 2. Balanced Modulator Test Circuit. (2:17)

2. Tuning T₂:

- a. Turn off the power supply board and remove the back cover of Unit COM-3/3 if this has not been done so already.
- b. Using the flat blade screwdriver, adjust the ferrite cores on the back side of the board that correspond to the transformer until the secondary amplitudes are equal.

APPENDIX H

Laboratory Experiment Number 5 Single Sideband Modulation

The topics of this experiment include:

1. Single sideband modulation and detection
2. Single sideband compatible AM

OBJECTIVE: To familiarize the student with the principles of single sideband (SSB) modulation and detection.

PREREQUISITES: Completion of Lab 1, "Equipment Familiarization", and Lab 4, "Balanced Modulator".

REQUIRED EQUIPMENT

The following equipment is required to perform this experiment. It is assumed the student is familiar with the controls and functions of each item listed below.

1. Oscilloscope (dual trace)
2. Spectrum Analyzer (0 to 2 MHz minimum)
3. 2 Signal Generators (CW capability)
4. Frequency Counter (0 to 2 MHz minimum)
5. Test Leads
6. DEGEM PS-MB-1/A Power Supply Board
7. DEGEM Boards Unit COM-3/1
Unit COM-3/2
Unit COM-3/3

REFERENCES

1. DEGEM Systems Ltd. SSB Communication Circuits System COM-3 Theoretical Background Manual. DEGEM Systems Ltd., 1976.
2. DEGEM Systems Ltd. SSB Communication Circuits System COM-3 Experiment and Technical Manual. DEGEM Systems Ltd., 1976.

THEORETICAL BACKGROUND

SOURCE: Reference (1).

1. Chapter 2 - Single Sideband Modulation
2. Chapter 3 - SSB Compatible AM

Additional Background

A single side band signal is created by first generating a double side band-suppressed carrier (DSB-SC) signal and then filtering out the unwanted side band. Figure 1 shows the block diagram for generating a DSB-SC waveform and figure 2 shows the block diagram for a SSB modulator.

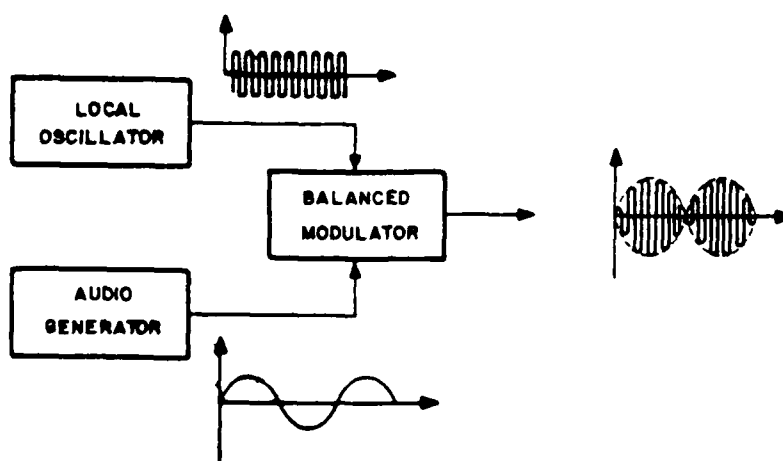


Figure 1. DSB-SC Modulation Block Diagram. (2:38)

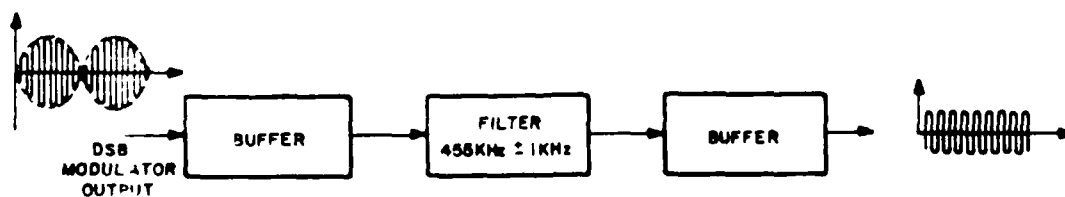


Figure 2. SSB Modulation Block Diagram. (2:39)

Usually, the carrier of the signal is fixed and then selection of the sideband requires the selection of one of two filters to attenuate either the upper side band (USB) or the lower side band (LSB). For the purposes of this experiment, only one filter is used and the carrier frequency is changed so the desired sideband is passed through a single band-pass filter while the other sideband is attenuated.

The governing equations to determine the frequency of the carrier (or local oscillator) that will allow attenuation of the unwanted sideband are:

$$f_{LO} = f_{FC} - f_{AF} \quad (\text{USB modulation condition}) \quad (1)$$

$$f_{LO} = f_{FC} + f_{AF} \quad (\text{LSB modulation condition}) \quad (2)$$

where f_{LO} = carrier (local oscillator) frequency of the DSB-SC modulator

f_{FC} = center frequency of the band-pass filter

f_{AF} = frequency of the audio signal being modulated

The SSB signal is detected by mixing the SSB signal with the carrier signal (LO signal) using a balanced modulator. The signal coming out of the balanced modulator will be the upper or lower sideband modulation signal, whichever is present. Figure 3 shows the block diagram for the SSB detector.

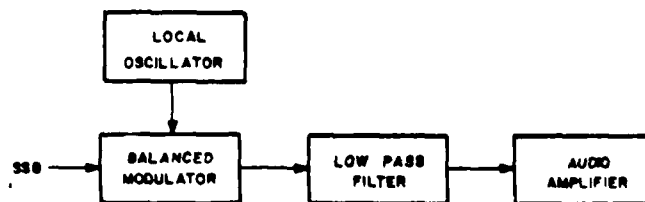


Figure 3. SSB Detector Block Diagram. (2:41)

In SSB Compatible AM, one of the sidebands and the carrier signal are transmitted. The receiver then uses the carrier information to detect the SSB signal (e.g. using an envelope detector).

Figure 4 shows the block diagram of the SSB Compatible AM transmitter and receiver. Notice that the local oscillator is added to the SSB signal before being transmitted. The receiver consists of a simple envelope detector and amplifier.

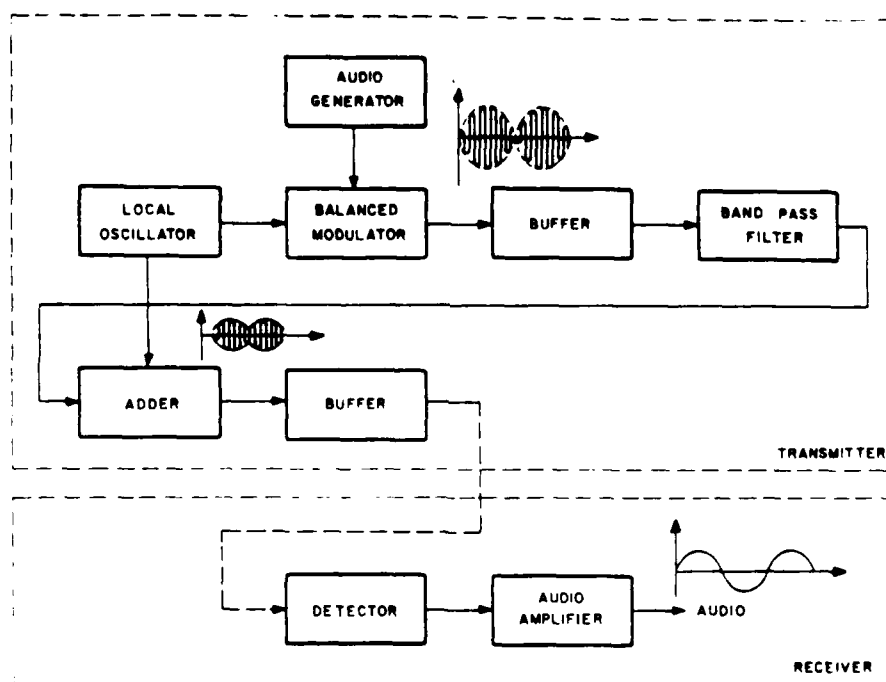


Figure 4. SSB Compatible AM System Block Diagram. (2:46)

EXPERIMENT PROCEDURE

General Instructions

WARNING

Turn the DEGEN Power Supply Board off before removing or inserting any plug-in boards. Damage to circuit components may result if the boards are changed while the power is on.

1. DO NOT turn the DEGEN PS-MB-1/A Power Supply Board on. Install the Unit COM-3/1, 3/2 and 3/3 boards into the power supply board by pressing each unit into a power socket and tightening the hold-down screws on each end of the unit.
2. Turn the power supply board on. All plug-in units are internally powered and therefore need no external power connections.
3. Turn all of the remaining equipment on.

Band-pass Filter

Objective: To determine the frequency response of the band-pass filter used to attenuate one of the sidebands.

1. Connect a 455 kHz, 1 Vpp sine wave to the input of the bandpass filter located on Unit COM-3/2. Use a frequency counter and oscilloscope to make the measurements. Connect the output of the filter to the spectrum analyzer and observe the spectrum at 455 kHz.
2. Trace the frequency response of the bandpass filter on the spectrum analyzer by varying the input frequency. Measure and record the filter's center frequency, 3 dB points and bandwidth.

DSB-SC Modulator

Objective: To generate a DSB-SC waveform.

1. Generate a 455 kHz, 500 mVpp sine wave from a signal generator using a frequency counter and oscilloscope to make measurements. Call this signal the LO signal.
2. Using another signal generator, generate a 4 kHz, 500 mVpp sine wave using the frequency counter and oscilloscope to make measurements. Call this signal the Audio signal.
3. Connect the circuit on Unit COM-3/2 as shown in figure 5.
4. Connect an oscilloscope to resistor R₁ and confirm that the signal is a DSB-SC waveform.

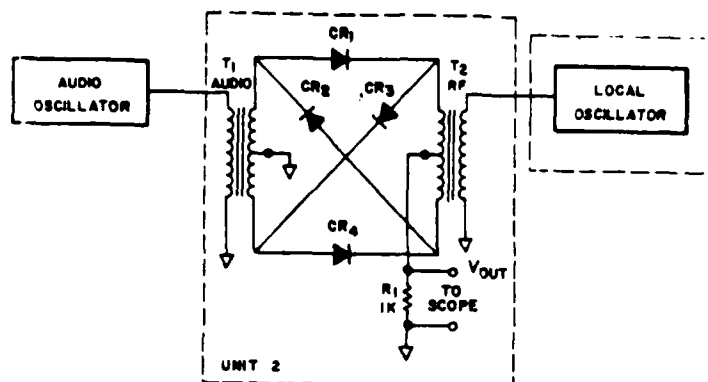


Figure 5. DSB-SC Modulation Circuit. (2:39)

SSB Modulator

Objective: To generate a SSB waveform and observe its spectrum.

1. Connect the circuit as shown in figure 6. Calculate and record the LO frequency needed for USB modulation using the equation (1) in the theoretical background section with:

$$f_{AF} = 4 \text{ kHz}$$

$$f_{FC} = \text{Center Frequency of BPF}$$

2. Set the LO frequency to this calculated value. Connect an oscilloscope and spectrum analyzer to capacitor C₂ on Unit COM-3/3 (output of the transmitter). Observe the spectrum on the spectrum analyzer at 455 kHz in the linear mode. Notice the attenuation of the LSB.
3. Vary the LO frequency and notice how the spectrum of the SSB signal changes.
4. Calculate and record the proper LO frequency for LSB modulation using equation (2) in the theoretical background section. Set the LO to this frequency and observe the spectrum. The USB is now attenuated in this signal.

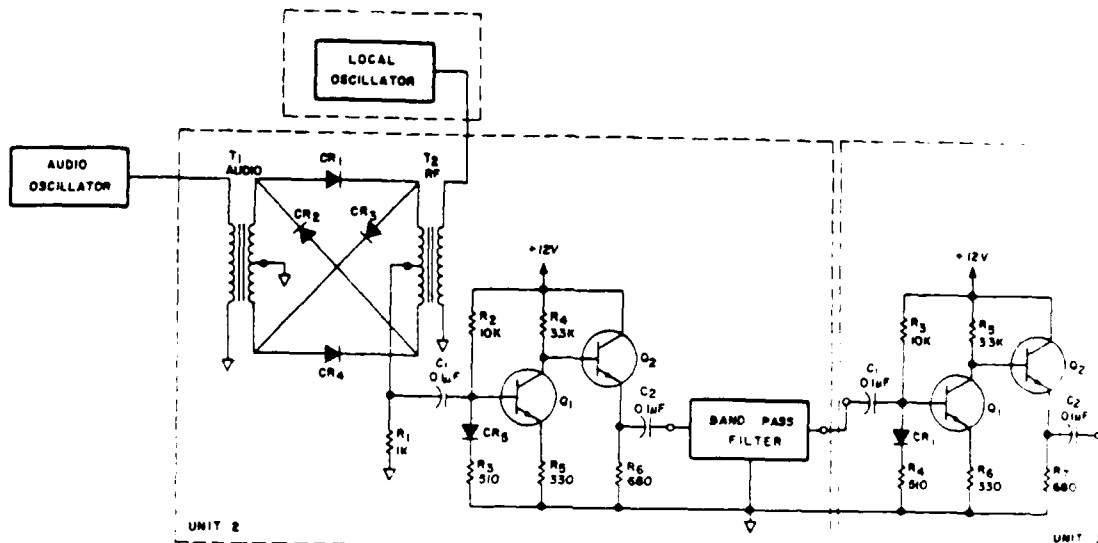


Figure 6. SSB Transmitter Circuit. (2:40)

SSB Detection

Objective: To observe the detection of a SSB signal.

1. Connect the circuit as shown in figure 7 where the Audio signal is a 500 mVpp, 4 kHz sine wave and the LO signal is 500 mVpp set for LSB modulation. Use external signal generators for both signals. Notice that the LO signal is attached to the transmitter and receiver balanced modulators in the circuit.
2. Connect the Audio signal and the detector output signal to a dual trace oscilloscope. Observe both waveforms. Connect the spectrum analyzer to the transmitter output at C₂ on Unit COM-3/3 and observe the SSB spectrum at 455 kHz.

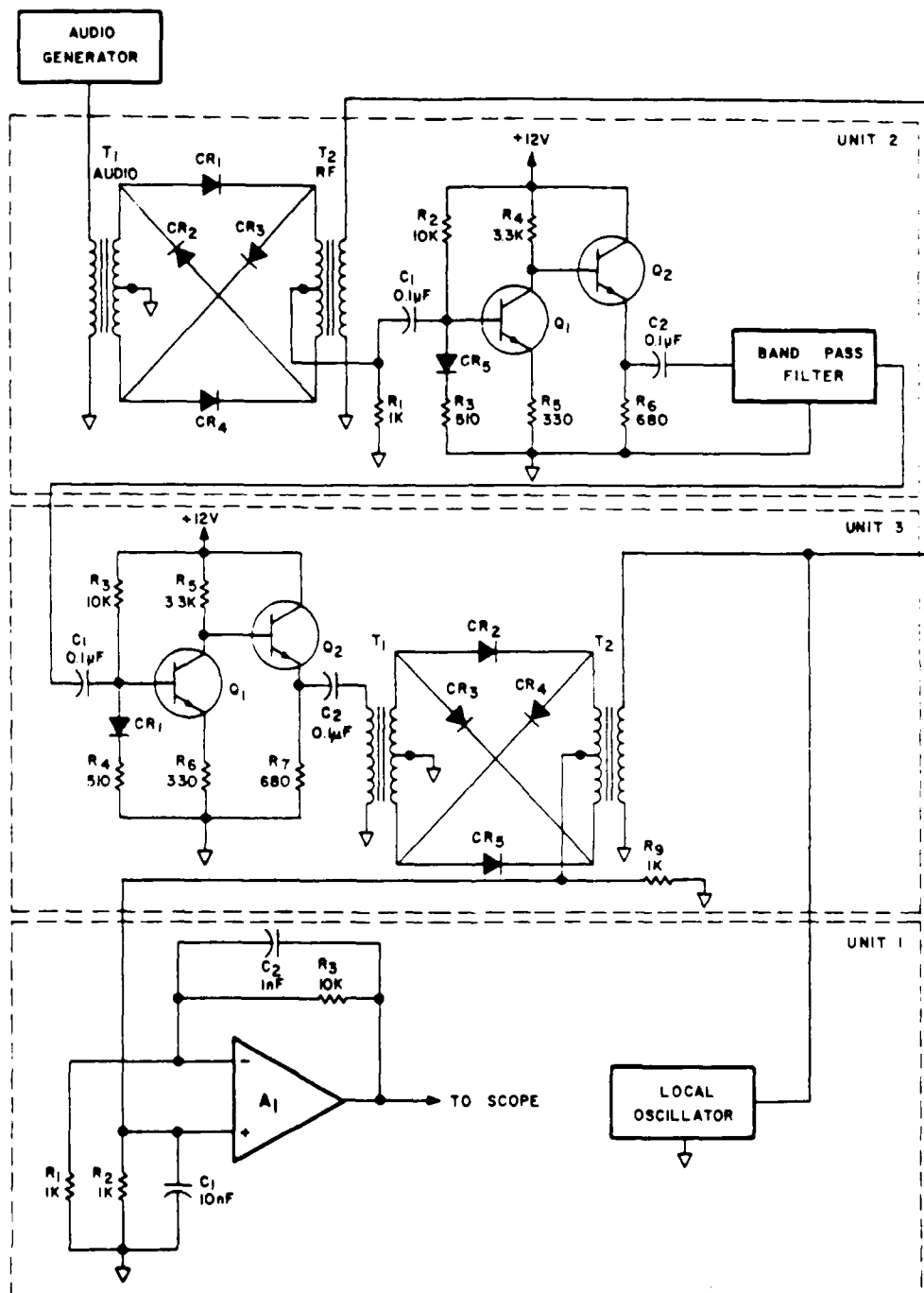


Figure 7. SSB Transmitter and Receiver Circuit. (2:42)

3. Adjust the LO frequency slightly to obtain a maximum LSB component on the spectrum analyzer. Measure the LO frequency with a frequency counter and record the value. This is the best LO frequency for transmitting a 4 kHz sine wave on the LSB.
4. Vary the Audio frequency slightly and observe the SSB spectrum and the time-domain trace of the detector output.
5. Set the Audio signal back to 4 kHz using a frequency counter and set the LO frequency for USB operation. Again observe the detector output on the oscilloscope and the SSB signal on the spectrum analyzer. Determine and record the best LO frequency for USB operation.

SSB Channel Frequency Response

Objective: To determine the frequency response of the SSB Channel.

1. With the Audio signal set at 4 kHz and the LO tuned for USB operation, connect the spectrum analyzer to the detector output at the point before the op-amp circuit on Unit COM-3/1 (R_2 on Unit COM-3/2). Observe the signal spectrum at baseband.
2. Trace the baseband frequency response by varying the Audio signal frequency. Notice that this response is similar to that of the bandpass filter, but shifted down to center on 4 kHz.
3. Determine the center frequency and bandwidth from the frequency response trace.
4. Readjust the Audio signal back to 4 kHz and the LO to LSB operation. Again observe the baseband spectrum of the detector output and trace the response curve. Notice that this frequency response is a mirror image of the response curve obtained from using USB modulation.
5. Determine and record the center frequency and bandwidth of the response curve.

Effect of a Difference in LO Frequency Between the Transmitter and Receiver

Objective: To observe the effect on SSB detection when there is a frequency difference between the LO in the transmitter and the LO in the receiver.

1. Set the LO frequency for LSB operation using a 4 kHz modulation sine wave. Adjust the FM oscillator output on Unit COM-3/1 to 500 mVpp at the same LO frequency. Use a frequency counter and oscilloscope to make measurements.
2. Replace the LO signal attached to the receiver balanced modulator (T₂ on Unit COM-3/3) with the FM oscillator. Keep the external LO signal attached to the transmitter balanced modulator. Both LO signals should have the same frequency.
3. Observe input Audio signal and the output of the receiver (at the output of the op-amp circuit on Unit COM-3/1) on a dual trace oscilloscope.
4. Connect a frequency counter to the receiver output signal and adjust the receiver LO frequency (FM oscillator on Unit COM-3/1) until the receiver output signal is at 4 kHz.
5. Vary the receiver LO frequency and notice that a slight change in this frequency causes a significant change in the detected signal frequency.
6. Adjust the receiver LO frequency until the output signal is at about 0 Hz. Measure and record the receiver LO frequency. Notice that it is approximately the same frequency as the BPF center frequency in the transmitter.

SSB Compatible AM

Objective: To observe the modulation and demodulation of a SSB Compatible AM signal.

1. Connect the circuit shown in figure 8. Set the external Audio generator to a 4 kHz, 500 mVpp sine wave and the external LO generator to a 455 kHz, 500 mVpp sine wave measuring with a frequency counter and oscilloscope.

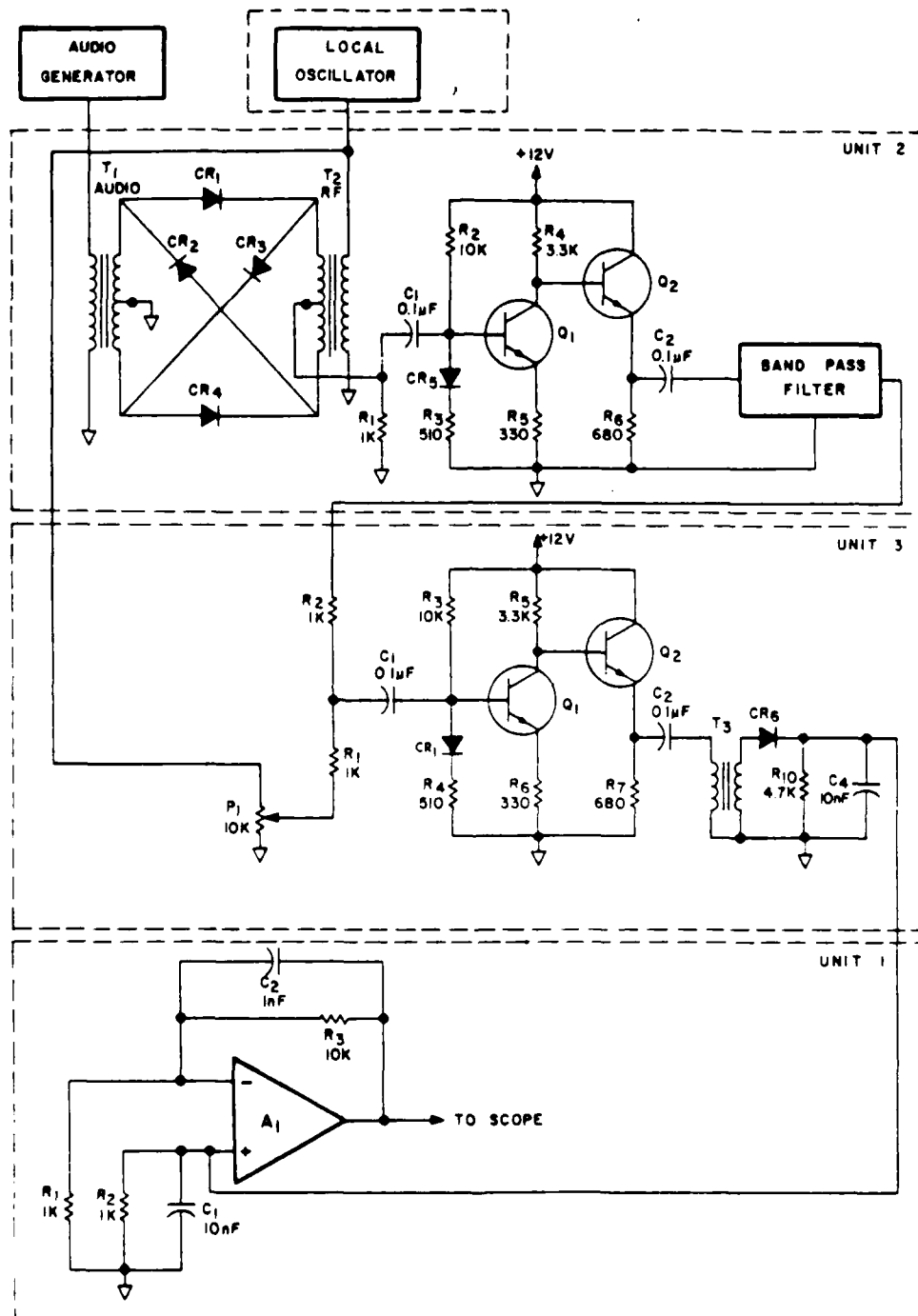


Figure 8. SSB Compatible AM Transmitter-Receiver Circuit. (2:47)

2. Connect an oscilloscope to C₂ on Unit COM-3/2 and verify that a DSB-SC waveform exists.
3. Connect the spectrum analyzer to the output of the BPF and a frequency counter to the LO input signal. Observe the BPF output on the spectrum analyzer at 455 kHz and adjust the LO frequency for USB operation.
4. Connect the spectrum analyzer and oscilloscope to the input of the envelope detector (C₂ on Unit COM-3/3). Observe the spectrum at the LO frequency. Also observe the time-domain trace. Vary potentiometer P₁ on Unit COM-3/3 and notice how the carrier power is added to the USB signal. Also note that the time-domain trace of the this signal resembles a conventional AM waveform, but is slightly distorted since the LSB component is attenuated.
5. Connect the oscilloscope to the audio amplifier output of the receiver (on Unit COM-3/3). Vary potentiometer P₁ until the output sine wave is undistorted.
6. Vary the LO frequency slightly and observe how the detected signal varies in amplitude. Set the LO frequency for a maximum USB frequency component on the spectrum analyzer.
7. Input a square wave as the audio signal and observe the input signal and the detected signal on a dual trace oscilloscope. Notice the detected signal is still a sine wave.

STUDENT NAMES _____ DATE PERFORMED _____

Note: Indicate unit of measurement with each data entry.

BAND-PASS FILTER

Center Frequency _____

3 db Points _____

Bandwidth _____

SSB MODULATOR

USB LO Frequency _____

LSB LO Frequency _____

SSB DETECTION

LSB "Best" LO Frequency _____

USB "Best" LO Frequency _____

SSB CHANNEL FREQUENCY RESPONSE

USB Center Frequency _____

Bandwidth _____

LSB Center Frequency _____

Bandwidth _____

EFFECT OF DIFFERENCE IN LO FREQUENCIES

Receiver LO Frequency _____

STUDENT NAMES SAMPLE DATE PERFORMED

Note: Indicate unit of measurement with each data entry.

BAND-PASS FILTER

Center Frequency	<u>456.14 kHz</u>	
3 db Points	<u>454.83 kHz</u>	<u>456.75 kHz</u>
Bandwidth	<u>1.92 kHz</u>	

SSB MODULATOR

USB LO Frequency	<u>452.14 kHz</u>
LSB LO Frequency	<u>460.14 kHz</u>

SSB DETECTION

LSB "Best" LO Frequency	<u>460.41 kHz</u>
USB "Best" LO Frequency	<u>452.38 kHz</u>

SSB CHANNEL FREQUENCY RESPONSE

USB Center Frequency	<u>4.00 kHz</u>
Bandwidth	<u>3.57 kHz</u>
LSB Center Frequency	<u>4.00 kHz</u>
Bandwidth	<u>3.47 kHz</u>

EFFECT OF DIFFERENCE IN LO FREQUENCIES

Receiver LO Frequency	<u>456.11 kHz</u>

APPENDIX I

Laboratory Experiment Number 6 Phase-Lock Loop and Frequency Synthesizer

The topics of this experiment include:

1. Characteristics of voltage controlled oscillator and phase detector
2. Phase-lock loop operation
3. Frequency synthesizer use of the phase-lock loop

OBJECTIVE: To familiarize the student with the principles and circuits of the Voltage Controlled Oscillator (VCO), Phase Detector, and Phase-Lock Loop (PLL). The Frequency Synthesizer is also studied as an application of the PLL.

PREREQUISITES: Completion of Lab 1, "Equipment Familiarization".

REQUIRED EQUIPMENT

The following equipment is required to perform this experiment. It is assumed the student is familiar with the controls and functions of each item listed below.

1. Oscilloscope (dual trace)
2. Spectrum Analyzer (0 to 2 MHz minimum)
3. Signal Generator (CW and TTL capability)
4. 2 Frequency Counters (0 to 2 MHz minimum)
5. Digital Voltmeter (DVM) (-20 to +20 Vdc minimum)
6. Test Leads
7. DEGEM PS-MB-2/A Power Supply Board
8. DEGEM Boards Unit COM-5A/1
Unit COM-5A/2
Unit COM-5A/3
Unit COM-5B/2

REFERENCES

1. DEGEM Systems Ltd. Phase-Lock Loop and Frequency Synthesizer Courses COM-5A and COM-5B Theoretical Background Manual. DEGEM Systems Ltd., 1976.
2. DEGEM Systems Ltd. Phase-Lock Loop and Frequency Synthesizer Courses COM-5A and COM-5B Experiment and Technical Manual. DEGEM Systems Ltd., 1976.
3. DEGEM Systems Ltd. Phase-Lock Loop and Frequency Synthesizer Course COM-5. DEGEM Systems Ltd., 1976.

THEORETICAL BACKGROUND

SOURCE: Reference (1) or (3).

1. Chapter 1 - Voltage Controlled Oscillator
2. Chapter 2 - Phase Detector
3. Chapter 3 - Phase-Lock Loop
4. Chapter 5 - Programmable Frequency Divider
5. Chapter 6 - Frequency Synthesizer

Additional Background

The VCO frequency range ratio is defined as:

$$\text{Ratio} = f_{\text{MAX}} / f_{\text{MIN}} \quad (1)$$

where f_{MAX} = maximum frequency

f_{MIN} = minimum frequency

The conversion coefficient (K_d) of a phase detector is calculated from the following equation:

$$K_d = \Delta V_o / \Delta \phi_{\text{IN}} \quad (\text{volt/rad}) \quad (2)$$

where ΔV_o = Output voltage range

$\Delta \phi_{\text{IN}}$ = Corresponding input phase range

Frequency Division Ratio - The frequency division ratio of a frequency divider is defined as:

$$\text{Ratio} = f_{\text{IN}} / f_{\text{OUT}} \quad (3)$$

where f_{IN} = input signal frequency

f_{OUT} = output signal frequency

The phase-lock loop consists of a phase detector, low pass filter and a VCO. Figure 1 shows the block diagram for a phase-lock loop.

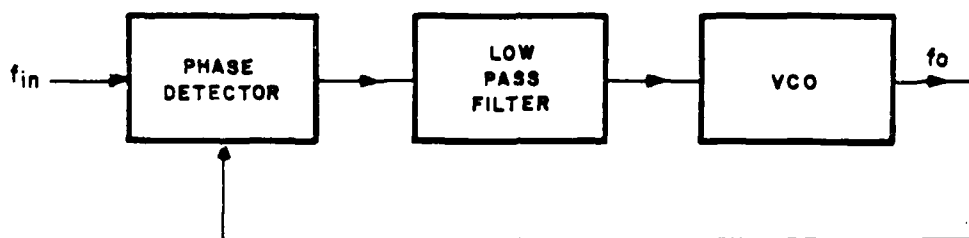


Figure 1. Block Diagram of the Phase-Lock Loop. (2:59)

DEGEM CIRCUIT BOARD DESCRIPTION

SOURCE: Reference (2).

Technical Description of Plug-In Units

- Unit COM-5A/1
- Unit COM-5A/2
- Unit COM-5A/3
- Unit COM-5B/2

EXPERIMENT PROCEDURE

General Instructions

WARNING

Turn the DEGEM Power Supply Board off before removing or inserting any plug-in boards. Damage to circuit components may result if the boards are changed while the power is on.

1. DO NOT turn the DEGEM PS-MB-2/A Power Supply Board on. Install the Unit COM-5A/1, 5A/2, 5A/3, and 5B/2 boards into the power supply board by pressing each unit into a power socket and tightening the hold-down screws on each end of the unit.
2. Turn the power supply board on. All plug-in units are internally powered and therefore need no external power connections. Adjust power supplies A and B to 12 Vdc measured by the meters on the power supply board.
3. Turn all of the remaining equipment on.

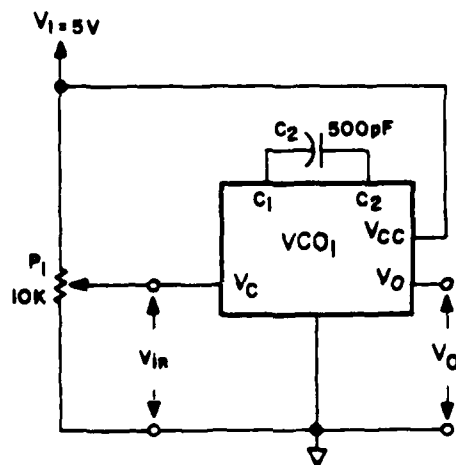
VCO Static Characteristics

Objective: To obtain a plot of input control voltage versus output frequency of the VCO.

1. Connect the circuit on Unit COM-5A/1 as shown in figure 2.

WARNING

The maximum control voltage to both VCOs is +5 volts. All ac and dc signals must remain below this maximum to prevent damage to internal circuit components.



COM 5-A UNIT 1

Figure 2. VCO Test Circuit. (2:52)

2. Connect a DVM to V_c and a frequency counter to V_o .
3. Set V_c to 0 Vdc by adjusting potentiometer P_1 .
4. Using the graph paper provided in the data sheet, plot the output frequency at V_o versus the input dc voltage at V_c . Label this curve as 500 pF. Also record the minimum and maximum frequencies of the VCO using this capacitance.
5. Replace capacitor C_2 with capacitor C_1 and plot the output frequency versus V_c on the same graph. Label this curve as 150 pF. Record the minimum and maximum frequencies on the data sheet.

6. Connect C_1 and C_2 so they are in parallel giving a total capacitance of 650 pF. Again plot the output frequency versus V_c and label this curve as 650 pF. Record the minimum and maximum frequencies on the data sheet.
7. Observe the plots made in this section and determine the linear range of the VCO for each capacitance. Record the minimum and maximum control voltages for this linear range along with the associated frequencies at these voltages.
8. Calculate and record the frequency range ratio for each capacitance using equation (1) in the theoretical background section using the minimum and maximum frequencies in the linear region.

Frequency Division and Digital Phase Detectors

Objective: To observe how flip-flops can serve as frequency dividers. Also to observe the operation of the exclusive-or and R-S flip-flop phase detectors.

1. Phase Shifter:

- a. Connect POWER IN on the Unit COM-5A/2 Phase Shifter to +12 Vdc. Also connect a 2 kHz TTL (0 to 5 Vdc square wave) signal from a signal generator to f_{IN} . Use a frequency counter and oscilloscope to make the measurements.
- b. Connect a dual trace oscilloscope to f_{REF} and the other channel to the first phase shifter tap ($-X/5$). Observe both waveforms and verify the phase shift between the signals. Verify the phase shifts for the other taps as well.

2. Frequency Division:

- a. Connect the circuit as shown in figure 3. Connect a frequency counter to the Q output of the flip-flop and verify that it is one-half the frequency of the f_{REF} frequency.
- b. Connect a second flip-flop as shown in figure 4 and verify that the output frequency is one-fourth that of the f_{REF} frequency.

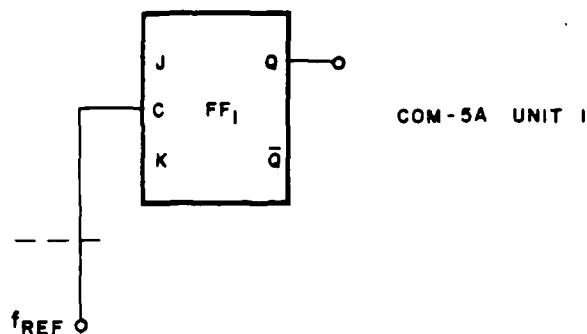


Figure 3. 1:2 Ratio Frequency Division Circuit. (2:55)

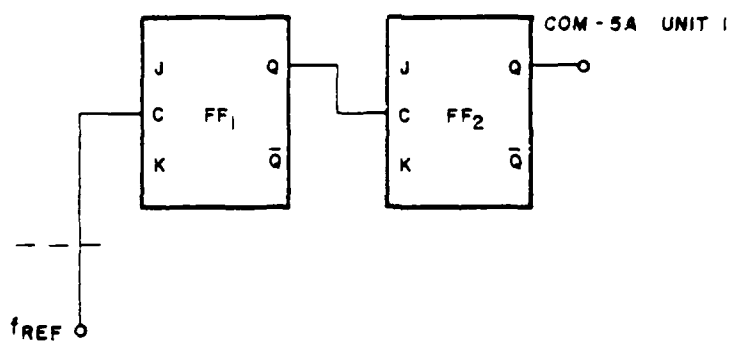


Figure 4. 1:4 Ratio Frequency Division Circuit. (2:55)

3. Exclusive-Or Gate used as a Phase Detector:

- a. Connect the circuit as shown in figure 5.

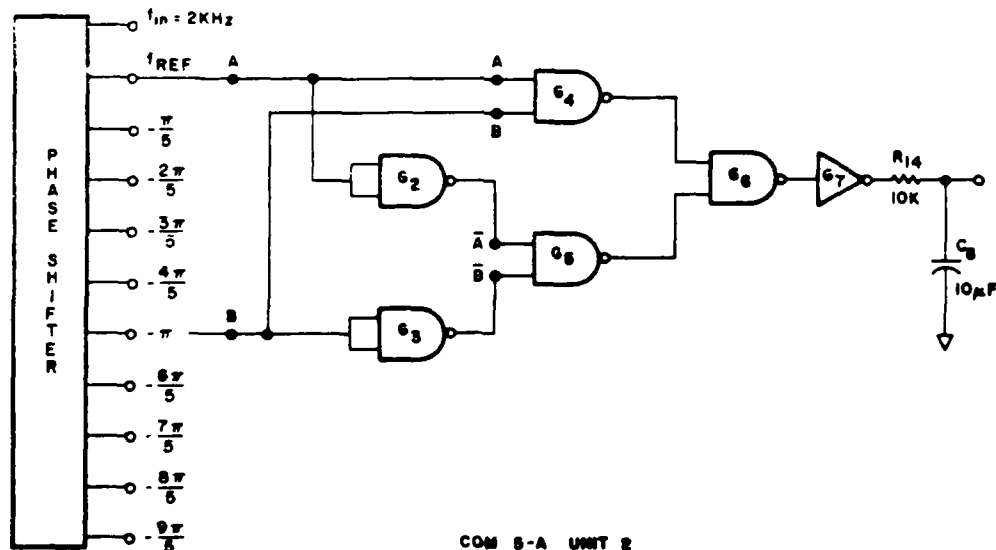


Figure 5. Exclusive-Or Phase Detector Circuit. (2:56)

- b. Connect a DVM to the output of the phase detector (C_5) and an oscilloscope to the output of the inverter G_7 . Record the output voltages for the different phase shifts on the data sheet and observe the phase shift differential waveform on the oscilloscope.
 - c. Calculate and record the conversion coefficient using equation (2) in the theoretical background section where ΔV_0 is the voltage difference between no phase shift and $-\pi$ phase shift. The $\Delta \phi_{IN}$ is then equal to π .
4. R-S Flip-Flop used as a Phase Detector:
 - a. Connect the circuit as shown in figure 6. Connect the point A to f_{REF} and B to the phase shifter taps.
 - b. Connect a DVM to the output of the phase detector (C_5) and an oscilloscope to the output of gate G_2 . Record the output voltages for the different phase shifts on the data sheet and observe the phase shift differential waveform on the oscilloscope.

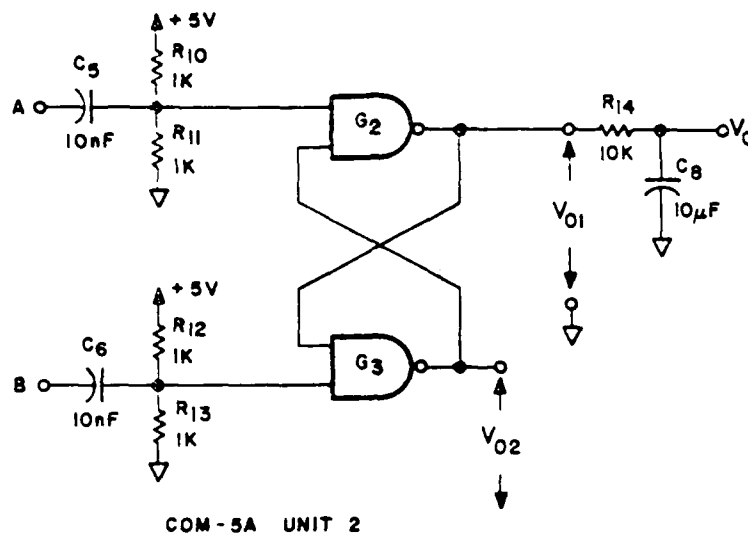


Figure 6. R-S Flip-Flop Type of Phase Detector. (2:57)

- c. Calculate and record the conversion coefficient using equation (2) in the theoretical background section where ΔV_0 is the voltage difference between no phase shift and $-9\pi/5$ phase shift. The $\Delta\phi_{IN}$ is then equal to $9\pi/5$.

Phase-Lock Loop

Objective: To observe the operation of the phase-lock loop and determine its locking and capture ranges along with its locking offset voltage.

1. Set-up:

- a. Connect the circuit shown in figure 7. The amplifier circuits on Unit COM-5A/3 are the low pass filter circuits, the gates G2 and G3 on Unit COM-5A/2 make up the R-S flip-flop phase detector, and the VCO is contained on Unit COM-5A/1.

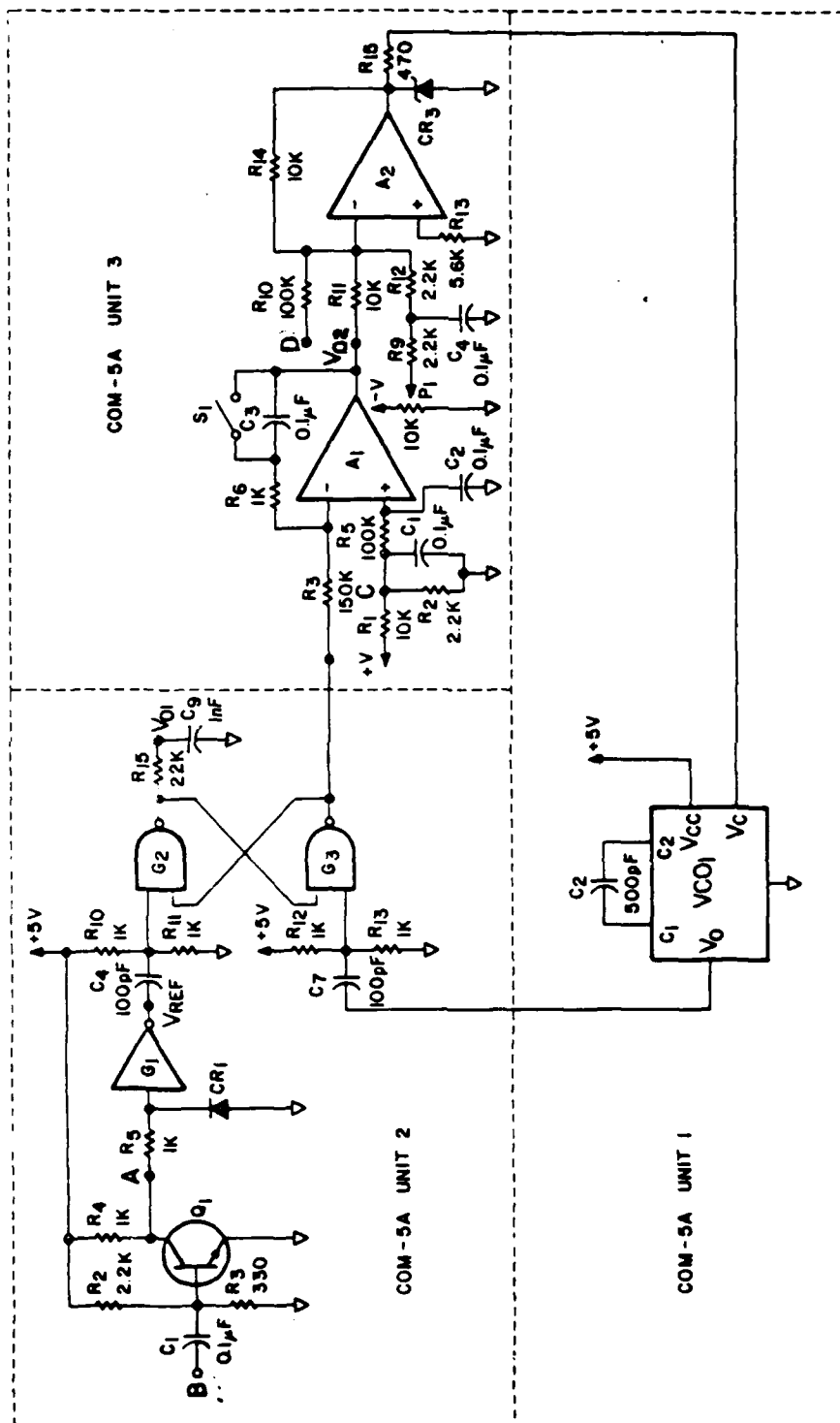


Figure 7. Phase-Lock Loop Circuit. (2:61)

- b. The type of input signal available will determine the input circuit structure to the phase detector on Unit COM-5A/2. The input circuit consists of the transistor Q₁ stage and gate G₁. The following steps describe the application of an input signal to the PLL for a TTL, bipolar square wave, and sine wave signal. Perform one step for the type of input signal available. On the data sheet, circle the type of signal used.
 - 1) TTL signal (0 to 5 Vdc) - Adjust the TTL signal to 500 kHz using a frequency counter. Remove the G₁ and Q₁ stages from the circuit and connect the signal to V_{REF} as shown in figure 7.
 - 2) Bipolar Square Wave (centered about 0 volts) - Adjust the bipolar square wave signal to 500 kHz and 2 V_{pp} using a frequency counter and oscilloscope. Remove the Q₁ stage from the circuit and connect the input signal to point B as shown in figure 7.
 - 3) Sine wave with no dc offset - adjust the sine wave to 500 kHz and 2 V_{pp} using a frequency counter and oscilloscope. Connect the input signal to point B as shown in figure 7.

2. Locking the PLL:

- a. Connect a frequency counter to the output of the PLL (V_o on VCO₁). Do not connect a frequency counter to the input signal.
- b. Turn potentiometer P₁ on Unit COM-5A/3 fully ccw and press switch S₁. After releasing S₁, the PLL attempts to lock its frequency onto the input signal frequency.
- c. If the PLL does not lock to 500 kHz, turn P₁ clockwise (increase) slightly and press S₁. Check the frequency counter for a lock on 500 kHz. Continue to increase P₁ and press S₁ until the PLL locks or exceeds 500 kHz.
- d. If the PLL frequency exceeded 500 kHz, reduce P₁ slightly and press S₁. Continue to vary P₁ and press S₁ until the PLL locks onto the 500 kHz input signal.

- e. When the PLL is properly locked, measure and record the input and output frequencies of the PLL using a frequency counter.
- f. Measure and record the VCO input control voltage (V_c on VCO₁) with a DVM and compare this voltage to the VCO characteristic curve drawn earlier.

4. Locking Range:

- a. To measure the locking range of the PLL, increase the frequency of the input signal while observing the frequency of the PLL output signal on a frequency counter. Determine and record the upper frequency where the PLL loses its lock on the input signal.
- b. After locking has been lost, the input frequency must be returned to approximately 500 kHz and S_1 pressed again. The PLL should lock after releasing S_1 .
- c. Decrease the input frequency until the PLL again loses its lock. Determine and record this lower frequency. The difference between the upper and lower frequency is the locking range.

5. Capture Range:

- a. To measure the capture range of the PLL, decrease the input frequency to about 400 kHz. Press S_1 and the PLL should lose lock on the input signal. If it doesn't, decrease the input frequency further and press S_1 .
- b. Increase the input signal frequency slowly and press S_1 occasionally until the PLL locks again onto the input signal. The PLL may lock at frequencies other than the input frequency and begin to track input frequency changes. If this happens, continue to press S_1 and vary the input frequency until the PLL locks properly. Determine and record the input frequency where locking can first be obtained.
- c. Increase the input frequency to about 600 kHz and press S_1 . Determine and record the upper capture frequency in the same manner as above by decreasing the input frequency.

6. Locking Offset Voltage:

- a. Disconnect the input signal from the PLL circuit. Disconnect R_{11} from the amplifier A_1 output on Unit CDM-5A/3 and connect R_{11} to the point between resistors R_1 and R_2 (Point C). Point C is a voltage level representing zero phase shift.
- b. Measure and record the dc voltage at the output of amplifier A_2 (at R_{10}) using a DVM. This is the locking offset provided by potentiometer P_1 to lock onto a 500 kHz signal.
- c. Reconnect R_{11} to the output of amplifier A_1 and also reconnect the input signal. Set the input signal to 500 kHz and press S_1 and the PLL should lock.
- d. Change the input frequency to 1 MHz and press S_1 . The PLL should loose its lock. Readjust the offset voltage using P_1 and press S_1 until the PLL locks onto the 1 MHz signal.
- e. Perform steps 6a and 6b again to determine the dc offset for locking onto the 1 MHz signal. Record this dc voltage on the data sheet.

Programmable Frequency Divider

Objective: To study two different methods of implementing a programmable frequency divider: one with a compelled initial state, and the other with a compelled final state.

1. Set-up for Method A (see 2:36):

- a. Assemble the circuit shown in figure 8.

NOTE

The gate G_5 shown in the figure is used if a bipolar square wave centered about 0 volts with 5 Vpp amplitude is used. If a TTL signal is available (0 to 5 V) then this gate should be removed.



Compelled Initial State. (2:72)

- a. Connect a frequency counter to V_{OUT} .

- c. Calculate and record the division ratio using equation (1) in the theoretical background section for each input binary number.
3. Set-Up for Method B (reference page 38 of the Theoretical Background Manual):
 - a. Connect the circuit shown in figure 9.

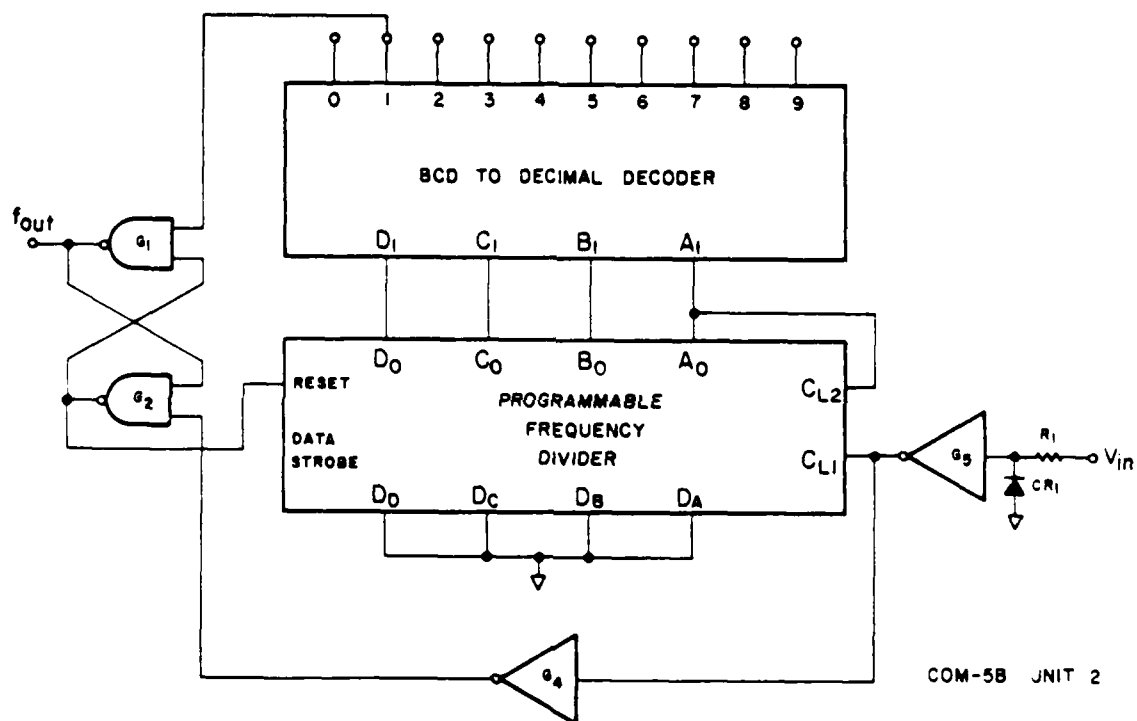


Figure 9. Programmable Frequency Divider with Compelled Final State. (2:73)

- b. Connect a 10 kHz (± 50 Hz), 5 Vpp TTL or bipolar square wave to the input of the frequency divider circuit as was described in the set-up section for Method A.
- c. Move the tap connected to the BCD to Decimal Decoder from 1 to 9, in each case measuring and recording the output frequency at four using a frequency counter.

- d. Calculate and record the division ratio using equation (3) in the theoretical background section for each tap position.

Frequency Synthesizer

Objective: To observe the operation of the frequency synthesizer using the phase-lock loop and final state programmable frequency divider.

1. Set-up:

- a. Assemble the circuit shown in figure 10. Connect four to CL₁ of the programmable frequency divider shown in figure 9. Also connect capacitor C₄ on Unit COM-5A/2 to the output of gate G₁ on this programmable frequency divider.
- b. Description of Circuit:
 - 1) The same PLL used previously is used again except that two VCOs are controlled instead of just one. The frequency range of the VCOs are different due to the attached external capacitors on each VCO. The desired VCO, and thus the desired frequency range, is selected by gates G₄ and G₆ on Unit COM-5B/2. Grounding the open terminal on G₄ will select VCO₂ and grounding the open terminal on G₆ will select VCO₁.

SPECIAL NOTE

When selecting VCO₁, VCO₂ must be disconnected from +5 Vdc to prevent interference with VCO₁.

- 2) The programmable frequency divider is used to select the desired frequency which is always an integer multiple of a reference frequency. The reference signal is a TTL square wave attached to C₇ on Unit COM-5A/2.
- 3) The output signal (TTL) at the desired frequency is provided at four (the output of gate G₇ on Unit COM-5B/2).

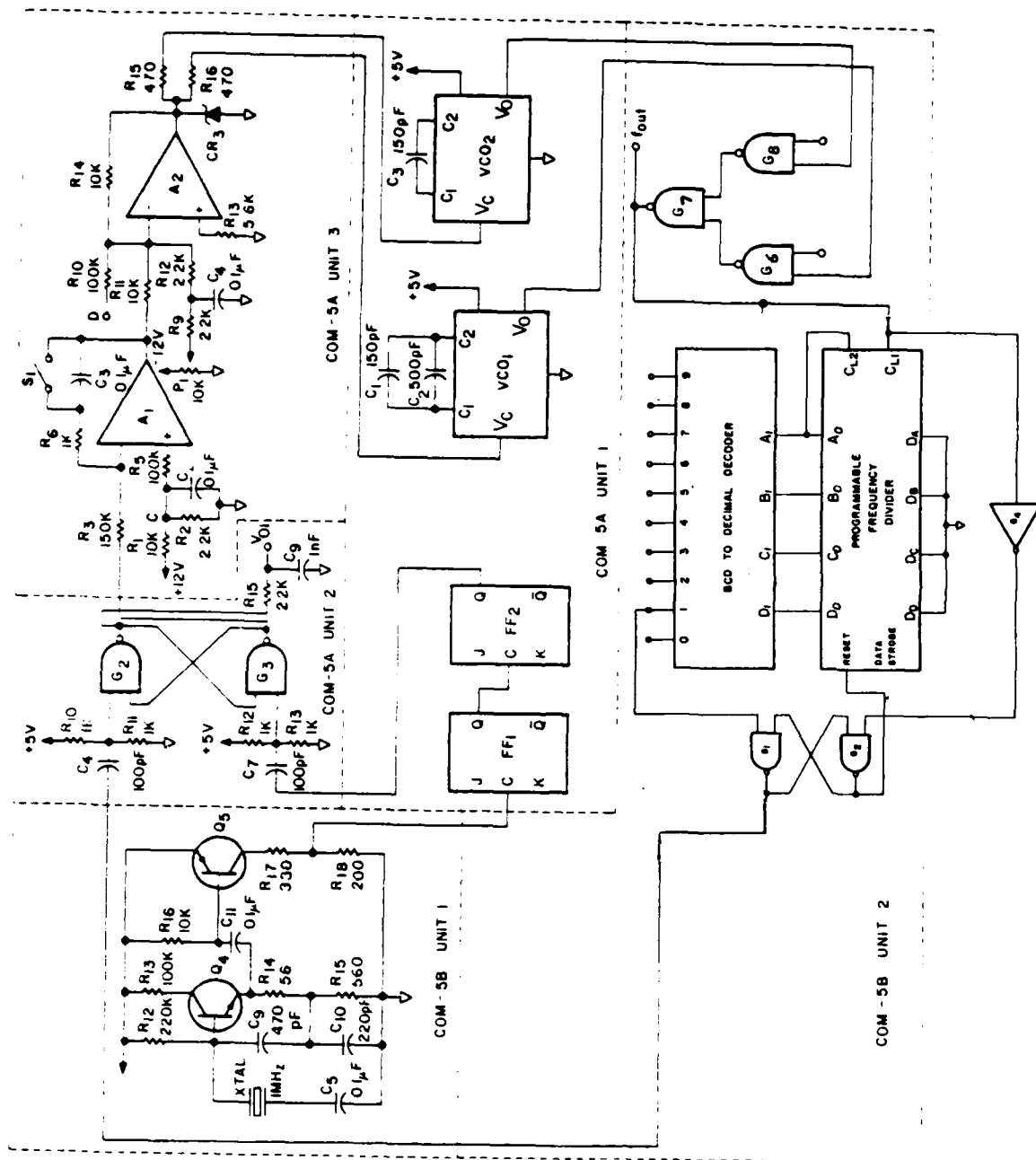


Figure 3. Frequency Synthesizer Circuit. (2:76)

- c. Generate a TTL (0 to +5 Vdc) 250 kHz square wave with a signal generator to be used as the reference signal. Connect this signal to C₇ on Unit COM-5A/2.

2. Locking the synthesizer:

- a. Connect a frequency counter to f_{IN} (capacitor C₇ on Unit COM-5A/2). Connect another frequency counter to the output of the frequency divider (output of G₁ on Unit COM-5B/2). The frequency synthesizer is locked when the output of the frequency divider is at 250 kHz.
- b. Disconnect VCO₂ on Unit COM-5A/1 from +5 Vdc (V₂). Also connect the open input terminal of G₆ on Unit COM-5B/2 to ground. This selects VCO₁.
- c. Connect the frequency divider tap (input to gate G₁) to the "1" position on the BCD to Decimal Decoder.
- d. Turn potentiometer P₁ on Unit COM-5A/3 fully ccw. Press S₁ and check the synthesizer for lock (i.e. 250 kHz at G₁ output on Unit COM-5B/2). If it is not locked, adjust P₁ slightly and press S₁. Continue this until the synthesizer locks at the reference frequency.

3. Operating the frequency synthesizer:

- a. Connect an oscilloscope to the output of the low pass filter circuit (A₁) on Unit COM-5A/3. Adjust the oscilloscope for dc operation with a vertical scale of 5 V/DIV. This signal will show the locking operation taking place. When the synthesizer is not locked, the output of this filter is -12 Vdc. When it is locked, the output is +12 Vdc. Disconnect the frequency divider tap and watch the oscilloscope trace. Reconnect the tap to position "1" and observe the dc level change to the locked position.
- b. Use table 1 below to make connections and observe the outputs of the frequency synthesizer. Note especially that for tap positions from "1" to "3", VCO₂ is disconnected from +5 Vdc. For positions "4" to "9" it is connected to +5 Vdc and is selected using gates G₄ and G₆ on Unit COM-5B/2. For each tap position, record the following:

- 1) Locked frequency at G_1 ($5B/2$) - adjust P_1 and press S_1 on Unit COM-5A/3 if necessary to get lock at 250 kHz.
- 2) Output frequency at G_7 ($5B/2$)
- 3) Division ratio between locked and output frequencies.
- 4) Time for the synthesizer to lock as measured on the oscilloscope connected to the A_1 output. To measure this, set the oscilloscope to dc coupled mode and 50 to 100 msec/DIV. Disconnect and reconnect the frequency divider tap to observe the locking time (time it takes for the A_1 output voltage to go from -12 Vdc to +12 Vdc).

Table 1. Frequency Synthesizer Operating Conditions.

Tap	VCO ₂	Input G_4	Input G_6
1	open	open	ground
2	open	open	ground
3	open	open	ground
4	+5 Vdc	ground	open
5	+5 Vdc	ground	open
6	+5 Vdc	ground	open
7	+5 Vdc	ground	open
8	+5 Vdc	ground	open
9	+5 Vdc	ground	open

STUDENT NAMES _____ DATE PERFORMED _____

Note: Indicate unit of measurement with each data entry.

VOLTAGE CONTROLLED OSCILLATOR (VCO)

	150 pF	500 pF	650 pF
Minimum Frequency	_____	_____	_____
Maximum Frequency	_____	_____	_____
Minimum Control Voltage	_____	_____	_____
Frequency	_____	_____	_____
Maximum Control Voltage	_____	_____	_____
Frequency	_____	_____	_____
Frequency Range Ratio	_____	_____	_____

DIGITAL PHASE DETECTORS

Exclusive-Or Gate:

Phase	DC Amplitude	Phase	DC Amplitude
0	_____	$-\pi$	_____
$-\pi/5$	_____	$-6\pi/5$	_____
$-2\pi/5$	_____	$-7\pi/5$	_____
$-3\pi/5$	_____	$-8\pi/5$	_____
$-4\pi/5$	_____	$-9\pi/5$	_____
Conversion Coefficient	_____		

R-S Flip-Flop:

Phase	DC Amplitude	Phase	DC Amplitude
0	_____	$-\pi$	_____
$-\pi/5$	_____	$-6\pi/5$	_____
$-2\pi/5$	_____	$-7\pi/5$	_____
$-3\pi/5$	_____	$-8\pi/5$	_____
$-4\pi/5$	_____	$-9\pi/5$	_____
Conversion Coefficient	_____		

PHASE-LOCK LOOP

Type of Input Signal Used (circle one):

	TTL	Bipolar Square Wave	Sine Wave
Locked Input Frequency	_____	_____	_____
Output Frequency	_____	_____	_____
VCO Control Voltage	_____	_____	_____
Locking Range Upper Freq	_____	_____	_____
Lower Freq	_____	_____	_____
Capture Range Lower Freq	_____	_____	_____
Upper Freq	_____	_____	_____
500 kHz Locking Offset	_____	_____	_____
1 MHz Locking Offset	_____	_____	_____

PROGRAMMABLE FREQUENCY DIVIDER - METHOD A (INITIAL STATE)

DECIMAL	D _D	D _C	D _B	D _A	f _{OUT}	RATIO
0	0	0	0	0	-----	---- : 1
1	0	0	0	1	-----	---- : 1
2	0	0	1	0	-----	---- : 1
3	0	0	1	1	-----	---- : 1
4	0	1	0	0	-----	---- : 1
5	0	1	0	1	-----	---- : 1
6	0	1	1	0	-----	---- : 1
7	0	1	1	1	-----	---- : 1
8	1	0	0	0	-----	---- : 1

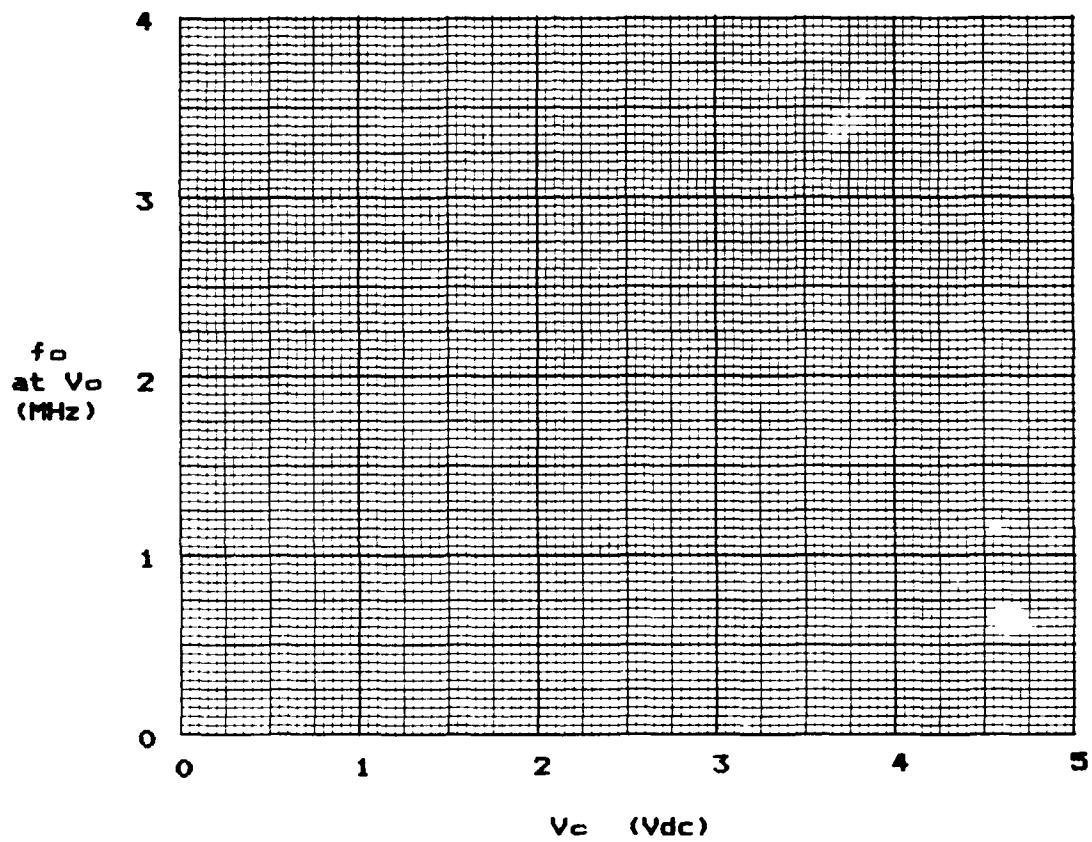
PROGRAMMABLE FREQUENCY DIVIDER - METHOD B (FINAL STATE)

TAP	f _{OUT}	RATIO	TAP	f _{OUT}	RATIO
1	-----	---- : 1	6	-----	---- : 1
2	-----	---- : 1	7	-----	---- : 1
3	-----	---- : 1	8	-----	---- : 1
4	-----	---- : 1	9	-----	---- : 1
5	-----	---- : 1			

FREQUENCY SYNTHESIZER OPERATION

TAP	LOCKED FREQ	OUTPUT FREQ	RATIO	LOCK TIME
1	-----	-----	----- : 1	-----
2	-----	-----	----- : 1	-----
3	-----	-----	----- : 1	-----
4	-----	-----	----- : 1	-----
5	-----	-----	----- : 1	-----
6	-----	-----	----- : 1	-----
7	-----	-----	----- : 1	-----
8	-----	-----	----- : 1	-----
9	-----	-----	----- : 1	-----

VCO CHARACTERISTIC CURVE



STUDENT NAMES _____ SAMPLE _____ DATE PERFORMED _____

Note: Indicate unit of measurement with each data entry.

VOLTAGE CONTROLLED OSCILLATOR (VCO)

	150 pF	500 pF	650 pF
Minimum Frequency	<u>800.1 kHz</u>	<u>308.3 kHz</u>	<u>225.1 kHz</u>
Maximum Frequency	<u>3248.6 kHz</u>	<u>1341.3 kHz</u>	<u>964.6 kHz</u>
Minimum Control Voltage	<u>3.5 Vdc</u>	<u>3.5 Vdc</u>	<u>3.5 Vdc</u>
Frequency	<u>1325 kHz</u>	<u>525 kHz</u>	<u>310 kHz</u>
Maximum Control Voltage	<u>5 Vdc</u>	<u>5 Vdc</u>	<u>5 Vdc</u>
Frequency	<u>3500 kHz</u>	<u>1500 kHz</u>	<u>1100 kHz</u>
Frequency Range Ratio	<u>2.642</u>	<u>2.857</u>	<u>3.548</u>

DIGITAL PHASE DETECTORS

Exclusive-Or Gate:

Phase	DC Amplitude	Phase	DC Amplitude
0	<u>0.051</u>	$-\pi$	<u>3.81</u>
$-\pi/5$	<u>0.753</u>	$-6\pi/5$	<u>2.93</u>
$-2\pi/5$	<u>1.463</u>	$-7\pi/5$	<u>2.18</u>
$-3\pi/5$	<u>2.18</u>	$-8\pi/5$	<u>1.463</u>
$-4\pi/5$	<u>2.93</u>	$-9\pi/5$	<u>0.753</u>
Conversion Coefficient	<u>1.197 V/rad</u>		

R-S Flip-Flop:

Phase	DC Amplitude	Phase	DC Amplitude
0	<u>0.044</u>	$-\pi$	<u>1.809</u>
$-\pi/5$	<u>0.391</u>	$-6\pi/5$	<u>2.17</u>
$-2\pi/5$	<u>0.742</u>	$-7\pi/5$	<u>2.53</u>
$-3\pi/5$	<u>1.096</u>	$-8\pi/5$	<u>2.91</u>
$-4\pi/5$	<u>1.451</u>	$-9\pi/5$	<u>3.29</u>
Conversion Coefficient		<u>0.574 V/rad</u>	

PHASE-LOCK LOOP

Type of Input Signal Used (circle one):

	TTL	Bipolar Square Wave	Sine Wave
Locked Input Frequency		<u>499.79 kHz</u>	
Output Frequency		<u>499.79 kHz</u>	
VCO Control Voltage		<u>3.46 Vdc</u>	
Locking Range Upper Freq		<u>1460 kHz</u>	
Lower Freq		<u>308 kHz</u>	
Capture Range Lower Freq		<u>449 kHz</u>	
Upper Freq		<u>519 kHz</u>	
500 kHz Locking Offset		<u>3.72 Vdc</u>	
1 MHz Locking Offset		<u>4.53 Vdc</u>	

PROGRAMMABLE FREQUENCY DIVIDER - METHOD A (INITIAL STATE)

DECIMAL	D _D	D _C	D _B	D _A	f _{OUT}	RATIO
0	0	0	0	0	<u>1.111</u> kHz	<u>9</u> : 1
1	0	0	0	1	<u>1.250</u> kHz	<u>8</u> : 1
2	0	0	1	0	<u>1.427</u> kHz	<u>7</u> : 1
3	0	0	1	1	<u>1.666</u> kHz	<u>6</u> : 1
4	0	1	0	0	<u>2.000</u> kHz	<u>5</u> : 1
5	0	1	0	1	<u>2.500</u> kHz	<u>4</u> : 1
6	0	1	1	0	<u>3.333</u> kHz	<u>3</u> : 1
7	0	1	1	1	<u>5.000</u> kHz	<u>2</u> : 1
8	1	0	0	0	<u>10.000</u> kHz	<u>1</u> : 1

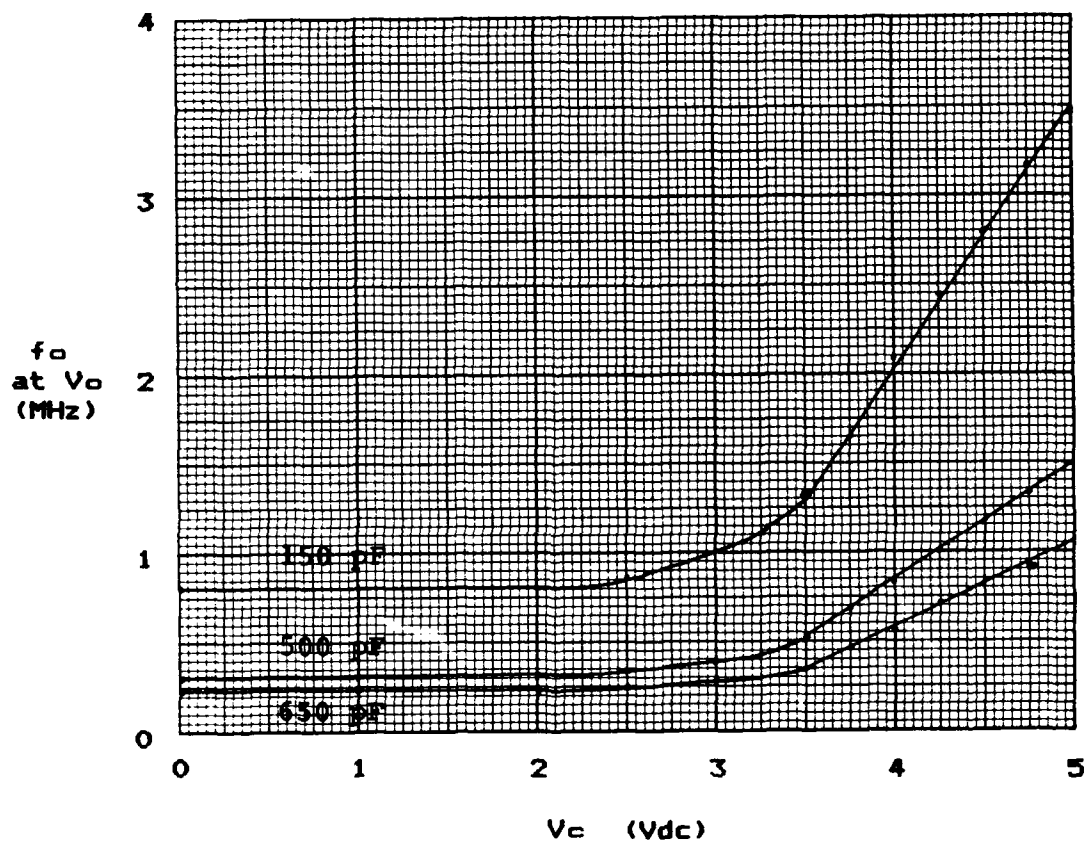
PROGRAMMABLE FREQUENCY DIVIDER - METHOD B (FINAL STATE)

TAP	f _{OUT}	RATIO	TAP	f _{OUT}	RATIO
1	<u>10.000</u> kHz	<u>1</u> : 1	6	<u>1.666</u> kHz	<u>6</u> : 1
2	<u>5.000</u> kHz	<u>2</u> : 1	7	<u>1.429</u> kHz	<u>7</u> : 1
3	<u>3.333</u> kHz	<u>3</u> : 1	8	<u>1.250</u> kHz	<u>8</u> : 1
4	<u>2.500</u> kHz	<u>4</u> : 1	9	<u>1.111</u> kHz	<u>9</u> : 1
5	<u>2.000</u> kHz	<u>5</u> : 1			

FREQUENCY SYNTHESIZER OPERATION

TAP	LOCKED FREQ	OUTPUT FREQ	RATIO	LOCK TIME
1	<u>250.0 kHz</u>	<u>250.0 kHz</u>	<u>1 : 1</u>	<u>200 ms</u>
2	<u>250.0 kHz</u>	<u>500.0 kHz</u>	<u>2 : 1</u>	<u>260 ms</u>
3	<u>250.0 kHz</u>	<u>750.0 kHz</u>	<u>3 : 1</u>	<u>500 ms</u>
4	<u>250.0 kHz</u>	<u>1000.0 kHz</u>	<u>4 : 1</u>	<u>200 ms</u>
5	<u>250.0 kHz</u>	<u>1250.0 kHz</u>	<u>5 : 1</u>	<u>240 ms</u>
6	<u>250.0 kHz</u>	<u>1500.0 kHz</u>	<u>6 : 1</u>	<u>280 ms</u>
7	<u>250.0 kHz</u>	<u>1748.6 kHz</u>	<u>7 : 1</u>	<u>320 ms</u>
8	<u>250.0 kHz</u>	<u>1998.0 kHz</u>	<u>8 : 1</u>	<u>380 ms</u>
9	<u>250.0 kHz</u>	<u>2248.2 kHz</u>	<u>9 : 1</u>	<u>460 ms</u>

VCO CHARACTERISTIC CURVE



APPENDIX J

Laboratory Experiment Number 7

Pulse Amplitude Modulation

The topics of this experiment include:

1. Simple and flat-topped sampling
2. Nyquist sampling
3. Time-division multiplexed pulse amplitude modulation
4. Cross-talk between multiplexed channels

OBJECTIVE: To familiarize the student with the principles and circuits of sampling, pulse amplitude modulation (PAM), and time division multiplexing (TDM).

PREREQUISITES: Completion of Lab 1, "Equipment Familiarization."

REQUIRED EQUIPMENT

The following equipment is required to perform this experiment. It is assumed the student is familiar with the controls and functions of each item listed below.

1. Oscilloscope (dual trace)
2. Spectrum Analyzer (0 to 2 MHz minimum)
3. 2 Signal Generators (CW capability)
4. Frequency Counter (0 to 2 MHz minimum)
5. Digital Voltmeter (DVM) (-20 to +20 Vdc minimum)
6. True RMS Voltmeter (100 kHz minimum bandwidth)
7. Test Leads
8. DEGEM PS-MB-1/A Power Supply Board
9. DEGEM Boards Unit COM-6A/1
Unit COM-6A/2
Unit COM-6A/3

REFERENCES

1. DEGEM Systems Ltd. Time Division Multiplexing: Sampling & Multiplexing, Pulse Code Modulation, & Delta Modulation Course COM-6. DEGEM Systems Ltd., 1976.

THEORETICAL BACKGROUND

SOURCE: Reference (1).

1. Chapter 2 - Sampling
2. Chapter 3 - Multiplexing

Additional Background

The Relative Crosstalk (RCT) between two Time Division Multiplexed-Pulse Amplitude Modulation (TDM-PAM) channels is defined as:

$$RCT = V_2 / V_1 \quad (1)$$

where V_2 = rms voltage of the output of the channel whose input is grounded.

V_1 = rms voltage of the output of the other channel.

DEGEM CIRCUIT BOARD DESCRIPTION

SOURCE: Reference (1).

Technical Description of Plug-In Units

- Unit COM-6A/1
- Unit COM-6A/2
- Unit COM-6A/3

EXPERIMENT PROCEDURE

General Instructions

WARNING

Turn the DEGEM Power Supply Board off before removing or inserting any plug-in boards. Damage to circuit components may result if the boards are changed while the power is on.

1. DO NOT turn the DEGEM PS-MB-1/A Power Supply Board on. Install the Unit COM-6A/1, 6A/2 and 6A/3 boards into the power supply board by pressing each unit into a power socket and tightening the hold-down screws on each end of the unit.
2. Turn the power supply board on. All plug-in units are internally powered and therefore need no external power connections.
3. Turn all of the remaining equipment on.

Simple Sampling

Objective: To observe the technique of simple sampling a waveform thus producing a PAM signal. Also to determine the frequency response of the reconstruction low pass filter and observe reconstruction of the original waveform from the PAM signal.

1. Low Pass Filter Response:

- a. Generate a 1 kHz, 1 Vpp sine wave from a signal generator using a frequency counter and oscilloscope to make the measurement. Connect the signal to the input of LPF₁ in Unit COM-6A/1.
- b. Connect the spectrum analyzer to the output of the LPF and observe the spectrum at baseband (0 kHz).
- c. Trace the frequency response of the filter on the spectrum analyzer by varying the input frequency.
- d. Determine and record the 3 dB and 6 dB points of the filter response curve. LPF₂ has the same frequency response and therefore does not need to be tested.

2. Sampling a Sine Wave (PAM):

- a. Assemble the circuit on Unit COM-6A/1 as shown in figure 1. Connect a 1 kHz, 2 Vpp sine wave to the input of the circuit. Use a frequency counter and oscilloscope to measure the signal.

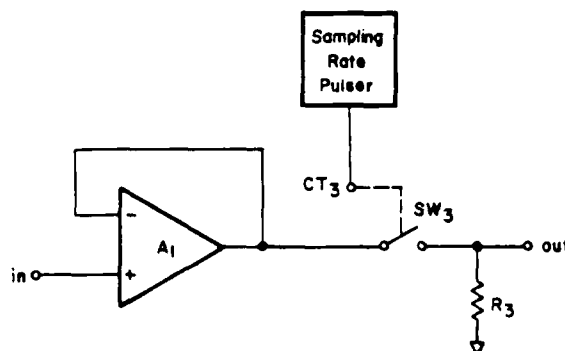


Figure 1. Sampling Circuit. (1:121)

- b. Connect a frequency counter and oscilloscope to the Sampling Rate Pulser output. Set the pulser frequency to 4 kHz with a 10% duty factor (25 μ sec) pulse width.
 - c. Connect the dual trace oscilloscope to the input and output signals of the sampling circuit. Also connect the spectrum analyzer to the output of the circuit.
 - d. Trigger the oscilloscope off the input sine wave signal and adjust the input frequency slightly to get a steady sampled sine wave on the other channel. This is a PAM signal.
 - e. Observe the spectrum of the PAM signal at baseband with a horizontal scale of about 20 kHz/DIV in the linear mode.
 - f. Verify that there are frequency nulls at multiples of the inverse of the pulse width. Vary the pulse width slightly and notice the corresponding change in the frequency nulls.
 - g. Reduce the spectrum analyzer's horizontal scale to about 1 kHz/DIV so the individual sidebands around 0 Hz are distinctly visible.
 - h. Verify that there are frequency components at f_m (1 kHz), $f_s \pm f_m$ (3 kHz, 5 kHz) and $2f_s \pm f_m$ (7 kHz, 9 kHz).
 - i. Vary the input frequency and observe how the spectral components move relative to the sampling frequency. Also vary the sampling frequency and notice the effect.
3. Reconstruction of the Sampled Signal:
- a. Use the sampling circuit in figure 1 and set the sampling frequency to 10 kHz with a 10% duty cycle (10 μ sec) using a frequency counter and oscilloscope. Change the input to a 2 kHz, 2 Vpp sine wave.

- b. Connect LPF₁ to the output of the sampling circuit. Connect the oscilloscope to the input sine wave and to the output of the LPF. Also connect the spectrum analyzer to the LPF output.
- c. Observe the time domain signals triggered off the input sine wave signal. Observe the output spectrum at baseband with a horizontal scale of about 1 kHz/DIV in the linear mode.
- d. Observe the effects of varying the sampling frequency and pulse width. When the sampling frequency is reduced to a point where the second sideband ($f_s - f_m$) is passed by the LPF, a DSB-SC waveform will be formed at the output of the filter distorting the reconstructed signal.
- e. Reduce the sampling frequency to 4 kHz and notice how the f_m and $f_s - f_m$ components merge. The sine wave is now being sampled near the Nyquist rate. Adjust the input frequency slightly to get the best output sine wave from the LPF (i.e. so there is little or no amplitude variation or modulation). Measure and record the input sine wave frequency and the sampling frequency. The sampling frequency should be the Nyquist rate (i.e. twice the sine wave frequency).

Sample and Holding (Flat-Top Sampling)

Objective: To observe the generation of a PAM signal through sample and holding and through buffered sample and holding.

1. Unbuffered Sample and Hold Circuit:
 - a. Assemble the circuit shown in figure 2. Connect a 1 kHz, 1 Vpp sine wave from a signal generator to the input of the circuit. Set the sampling rate to 10 kHz with a 20 % duty factor (20 μ sec) pulse width.
 - b. Connect the dual trace oscilloscope to the input signal and output signal. Trigger the oscilloscope off the input signal. Observe both waveforms.

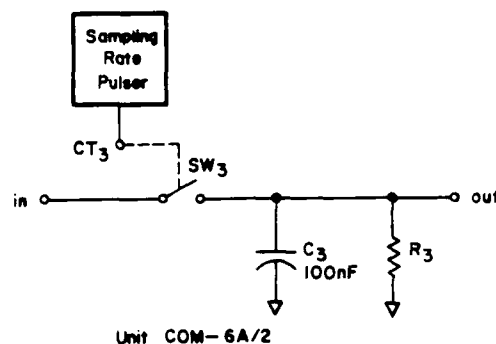


Figure 2. Unbuffered Sample and Hold Circuit. (1:123)

- c. Disconnect the load resistor R_3 and stabilize the output signal by varying the input signal frequency slightly.
- d. Connect the load resistor and observe its effect on the output waveform.
- e. Change the capacitor in the circuit to different values (1 nF, 10 nF) and observe the output. Compare outputs with and without the load resistor. Note on the data sheet how the output changes with decreased capacitance.
- f. Connect LPF₁ to the output signal and observe the LPF output on the oscilloscope, triggering off the input sine wave.
- g. Vary the capacitance of the sample and hold circuit and notice the effects on the output. Record which capacitance value gives the best demodulated output.

2. Buffered Sample and Hold Circuit:

- a. Connect the circuit as shown in figure 3. Connect a 1 kHz, 1 V_{pp} sine wave from a signal generator to the input of the circuit. Set the sampling rate at 10 kHz with a 20% duty factor (20 μ sec) pulse width.

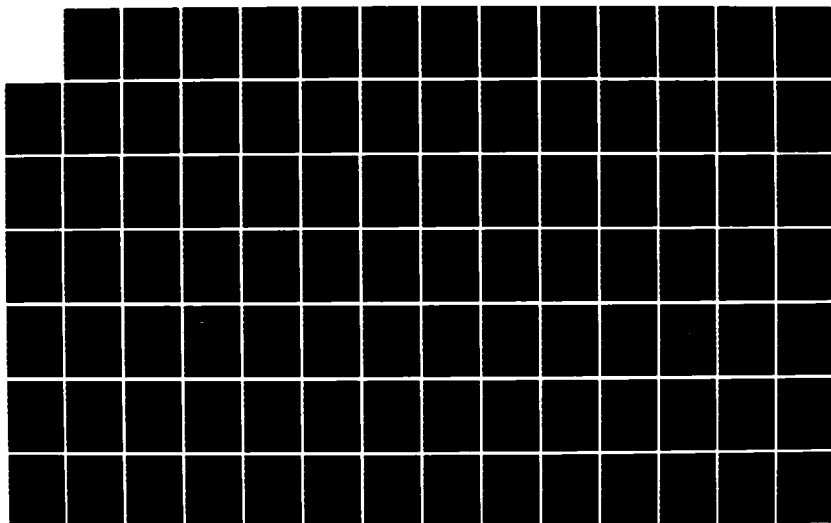
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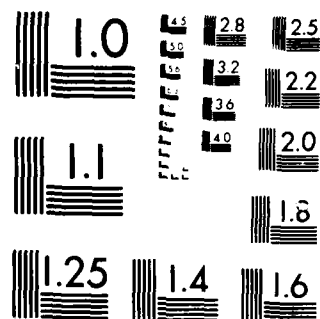
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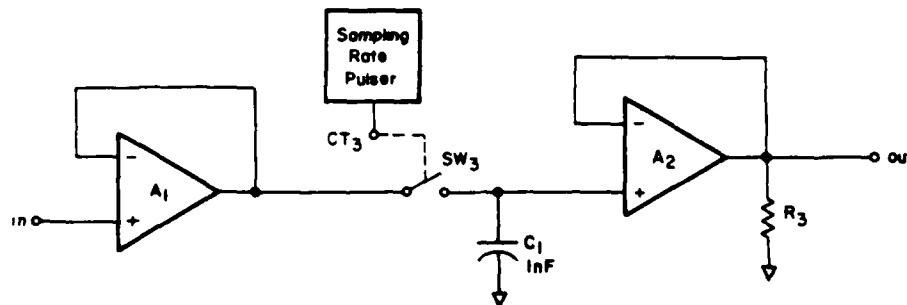
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Unit COM-6A/2

Figure 3. Buffered Sample and Hold Circuit. (1:124)

- b. Connect the dual trace oscilloscope to the input signal (trigger) and to the output of amplifier A₂. Observe both waveforms. Stabilize the output by varying the input frequency slightly.
- c. Observe the output signal for different storage capacitor values. Note that since the output buffer does not load the circuit significantly, the output waveform is similar to that obtained without the load resistor in the unbuffered case.
- d. Connect LPF₁ to the output signal and observe the input sine wave and the LPF output signal. Change storage capacitor values and record which capacitor gives the best demodulated signal.

Time Division Multiplexed PAM

Objective: To generate a TDM-PAM signal through simple sampling and flat-topped sampling. Also to demultiplex the TDM-PAM signal and observe the crosstalk between TDM channels.

1. Modulator Timing Counter:

- a. The modulator timing counter on Unit COM-6A/1 provides basic timing for the TDM system. To investigate the counter, connect the manual clock on Unit COM-6A/1 to the CL input of the counter.
- b. Advance the counter by pressing the manual clock and use an oscilloscope or DVM to check the logic state of each counter output. Notice that the high logic state (+5 Vdc) advances to the next output after pressing the manual clock. Also, only one output has a high logic state at a given time.
- c. Connect the 80 kHz output of the Clock Generator on Unit COM-6A/1 to the CL input of the counter in place of the manual clock. Connect channel one of the dual trace oscilloscope to the "0" output of the counter. Using the second channel of the oscilloscope, compare the other outputs to this "0" output. Notice a different relative time change for each output.
- d. Connect the reset input R on the counter to +5 Vdc. Check the logic levels of all the counter outputs. Notice that all have been cleared to a low logic level.
- e. With the 80 kHz Clock Generator signal attached to the counter CL input, disconnect the reset input from +5 Vdc. Measure and record the CL frequency.
- f. Connect a frequency counter to the "0" output. Since the reset input is not connected, the counter is a 10-stage counter and the outputs have 1/10th the CL frequency (8 kHz). Measure and record the "0" output frequency for the 10-stage counter.
- g. The counter can become an N-stage counter (N ranging from 1 to 10) by connecting the reset input to different counter outputs. Connect the reset input R to outputs "9" through "1" and in each case measure and record the frequency at the "0" output.

2. A TDM-PAM Multiplexer:

- a. Assemble the circuit shown in figure 4.

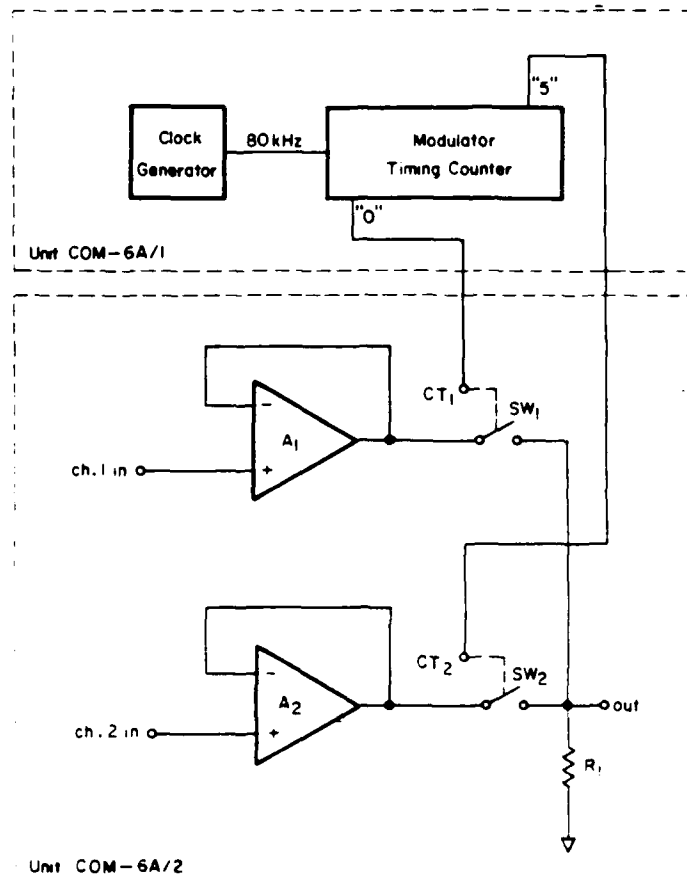
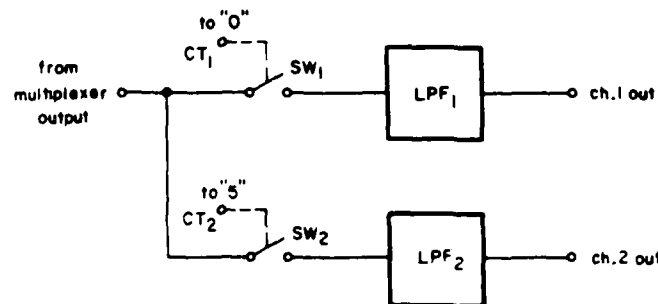


Figure 4. TDM-PAM Multiplexer. (1:127)

- b. Connect a 2 kHz, 6 Vpp sine wave from a signal generator (measured with a frequency counter and oscilloscope) to the ch. 1 input and ground the ch. 2 input. Connect the input sine wave and the output of the multiplexer circuit to a dual trace oscilloscope. Observe both waveforms triggering off the input sine wave.

- c. Adjust the input frequency slightly to obtain a steady output PAM signal.
 - d. Connect a 2 kHz, 2 Vpp sine wave from another signal generator to the ch. 2 input. Vary the input frequencies slightly to obtain a steady PAM signal, triggering externally off one of the input sine waves. This output signal is a TDM-PAM signal. Notice how the two channel signals are interlaced at the output.
 - e. Vary the ch 2. input frequency slightly and notice the effect on the output signal.
3. Demultiplexing the TDM-PAM Signal:
- a. Connect the circuit shown in figure 5 to the output of the TDM-PAM Multiplexer.



Unit COM-6A/1

Figure 5. TDM-PAM Demultiplexer. (1:128)

- b. Reset the input frequencies to obtain a steady TDM-PAM signal. Connect the dual trace oscilloscope, triggering off the Ch. 1 input, to the TDM-PAM signal and to the input of LPF1. Vary the input frequencies slightly to obtain steady traces on the oscilloscope. Vary the Ch. 1 signal generator amplitude and notice how the switch SW1 extracts only the information from Ch. 1.

- c. Connect the oscilloscope to the outputs of the LPFs. Observe the effects on both channel outputs when the input frequencies and amplitudes are varied. Notice that the outputs are not clean sine waves. Flat-topped sampling, as described next, will improve the output signal.
4. A TDM-PAM Multiplexer with Flat-Topped Sampling:
 - a. Assemble the circuit shown in figure 6. Connect a 1 kHz, 6 Vpp sine wave to the ch. 1 input and a 1 kHz, 2 Vpp sine wave to the ch. 2 input. Use two separate signal generators using a frequency counter and oscilloscope to make measurements.

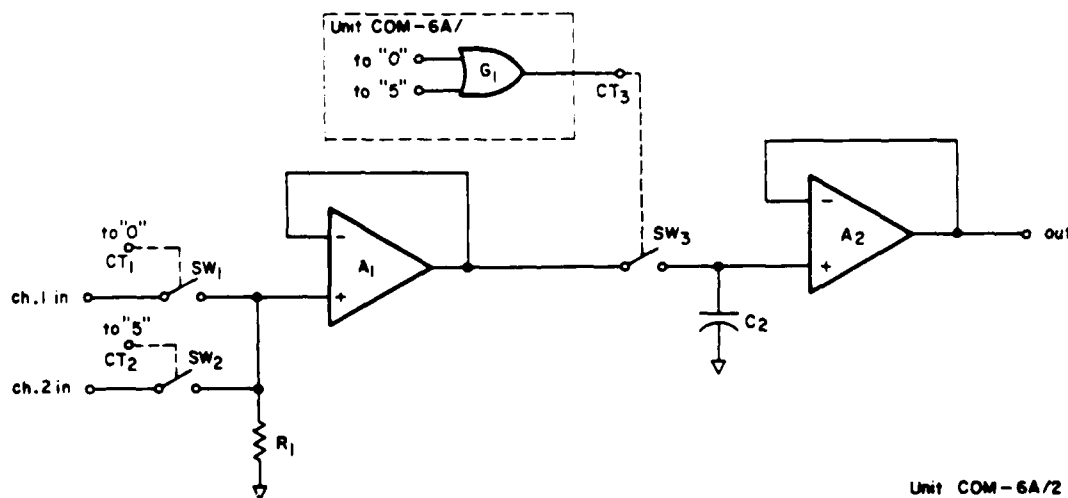


Figure 6. TDM-PAM Multiplexer with Flat-Topped Sampling. (1:128)

- b. Connect the ch. 2 input signal and the multiplexer output to a dual trace oscilloscope. Trigger off the input signal. Vary the input frequencies slightly to obtain a stable output. The output signal is again a TDM-PAM signal.

- c. Change the lines connected to "5" of the counter to different outputs of the counter. Notice how the duty cycle of the channel in the TDM signal changes.

5. Demultiplexing the TDM-PAM Signal:

- a. Repeat the same procedure used in step 3 above.
- b. Connect the counter reset input to different counter outputs to vary the sampling frequency. Make sure the sampling taps are in a position below the reset position. Observe the effect on the TDM-PAM signal and the outputs of the LPFs.

6. Crosstalk in TDM-PAM:

- a. Assemble the circuit shown in figure 7. The LPF consisting of R_2 and C_1 simulates the effects of a non-ideal channel.

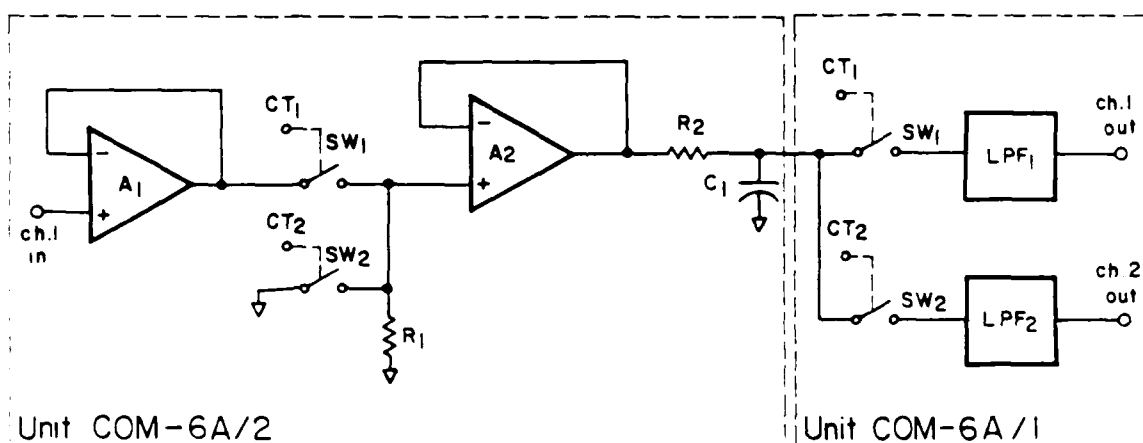


Figure 7. Crosstalk Demonstration Circuit. (1:129)

- b. Connect the 160 kHz signal from the Clock Generator to the CL input of the Modulator Timing Counter. Connect both CT_1 inputs to the "1" output of the counter and both CT_2 inputs to the "2" output.

- c. Connect a 2 kHz, 8 Vpp sine wave from a signal generator to the ch. 1 input using a frequency counter and oscilloscope to make measurements.
- d. Observe the ch. 1 and ch. 2 outputs simultaneously on the dual trace oscilloscope. Note that channel 1 is properly demultiplexed but channel 2 should not have any signal since the ch. 2 input is grounded. The signal present at the ch. 2 output is crosstalk from channel 1. Measure and record the RMS voltage of the ch. 1 and ch. 2 outputs using a True RMS Voltmeter.
- e. Move the CT₂ connections to the "3" output of the counter to give one guard band between the channels. Notice that the crosstalk is reduced. Again measure and record each channel's output RMS voltage.
- f. Calculate and record the relative crosstalk for zero and one guard band using equation (1) in the Theoretical Background section and the voltages measured above.
- g. Continue to increase the number of guard bands between the two channels and observe the effect on the ch. 2 output.

STUDENT NAMES _____ DATE PERFORMED _____

Note: Indicate unit of measurement with each data entry.

SAMPLING AND RECONSTRUCTION

Low Pass Filter 1 3 dB _____ 6 dB _____

Input Frequency _____

Sampling Frequency _____

SAMPLING AND HOLDING

Effect of Different Holding Capacitors _____

Unbuffered Capacitor for Best Output _____

Buffered Capacitor for Best Output _____

TDM-PAM

CL Frequency _____

RESET TAP	"0" FREQ	RESET TAP	"0" FREQ
Disconnected	_____	"5"	_____
"9"	_____	"4"	_____
"8"	_____	"3"	_____
"7"	_____	"2"	_____
"6"	_____	"1"	_____

CROSSTALK

GUARD BANDS	CH.1 OUTPUT VOLTAGE	CH.2 OUTPUT VOLTAGE	RELATIVE CROSSTALK
0	-----	-----	-----
1	-----	-----	-----

STUDENT NAMES SAMPLE DATE PERFORMED

Note: Indicate unit of measurement with each data entry.

SAMPLING AND RECONSTRUCTION

Low Pass Filter 1 3 dB 3.73 kHz 6 dB 4.30 kHz
 Input Frequency 2.025 kHz
 Sampling Frequency 4.049 kHz

SAMPLING AND HOLDING

Effect of Different Holding Capacitors There is less
holding for lower capacitance values.

Unbuffered Capacitor for Best Output C3Buffered Capacitor for Best Output No significant
difference

TDM-PAM

CL Frequency 80.663 kHz

RESET TAP	"0" FREQ	RESET TAP	"0" FREQ
Disconnected	<u>8.066 kHz</u>	"5"	<u>16.133 kHz</u>
"9"	<u>8.962 kHz</u>	"4"	<u>20.166 kHz</u>
"8"	<u>10.083 kHz</u>	"3"	<u>24.888 kHz</u>
"7"	<u>11.524 kHz</u>	"2"	<u>40.332 kHz</u>
"6"	<u>13.443 kHz</u>	"1"	<u>80.663 kHz</u>

CROSSTALK

GUARD BANDS	CH. 1 OUTPUT VOLTAGE	CH. 2 OUTPUT VOLTAGE	RELATIVE CROSSTALK
0	<u>251 mVrms</u>	<u>190 mVrms</u>	<u>0.76</u>
1	<u>251 mVrms</u>	<u>37.7 mVrms</u>	<u>0.15</u>

APPENDIX K

Laboratory Experiment Number 8

Pulse Code Modulation

The topics of this experiment include:

1. Pulse code modulation and demodulation
2. Linear and companded quantization
3. Analog-digital and digital-analog conversion

OBJECTIVE: To familiarize the student with the principles and circuits of Pulse Code Modulation (PCM) and Demodulation.

PREREQUISITES: Completion of Lab 1, "Equipment Familiarization".

REQUIRED EQUIPMENT

The following equipment is required to perform this experiment. It is assumed the student is familiar with the controls and functions of each item listed below.

1. Oscilloscope (dual trace)
2. Signal Generator (CW capability)
3. Frequency Counters (0 to 2 MHz minimum)
4. Digital Voltmeter (DVM) (-5 to +5 Vdc minimum)
5. Test Leads
6. DEGEM PS-MB-2/A Power Supply Board
7. DEGEM Boards Unit COM-6A/1
Unit COM-6A/2
Unit COM-6A/3
Unit COM-6B/1
Unit COM-6B/2
Unit COM-6B/3

REFERENCES

1. DEGEM Systems Ltd. Time Division Multiplexing: Sampling & Multiplexing, Pulse Code Modulation, & Delta Modulation Course COM-6. DEGEM Systems Ltd., 1976.

THEORETICAL BACKGROUND

SOURCE: Reference (1).

1. Chapter 4 - Pulse Code Modulation (PCM)
2. Chapter 6 - Companded PCM

Additional Background

The PCM modulator block diagram is shown in figure 1. The output consists of 4-bit PCM words where the most significant bit is a sign bit and the remaining bits represent the input amplitude.

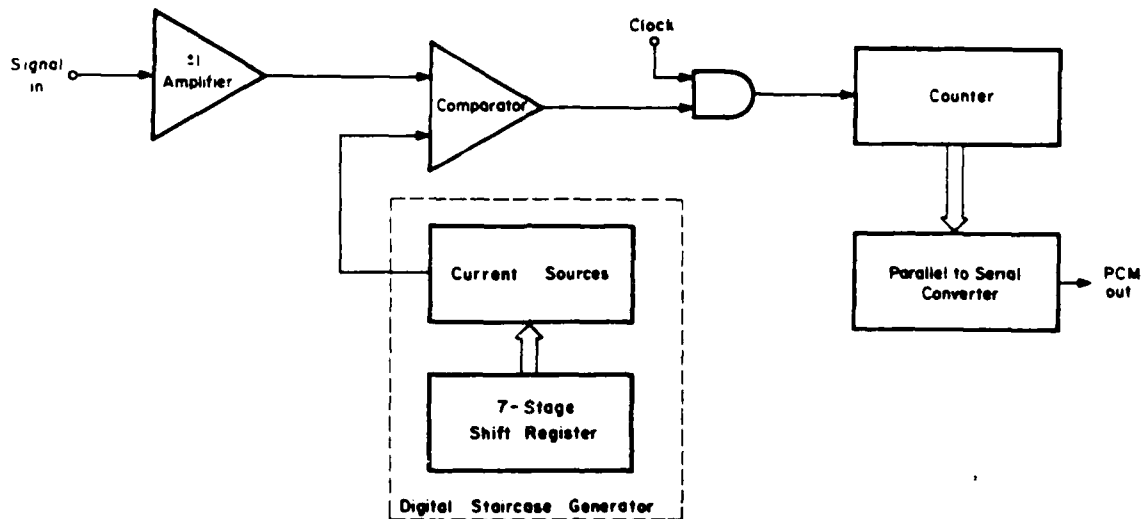


Figure 1. Block Diagram of PCM Modulator. (1:144)

Additional circuitry is used to create the timing signals for the PCM modulator. These timing signals were discussed in Chapter 4 of the required reading. The timing diagram presented in chapter 4 is shown in figure 2 for easy reference.

The block diagram of the PCM demodulator is shown in figure 3 below.

DEGEM CIRCUIT BOARD DESCRIPTION

SOURCE: Reference (1).

Technical Description of Plug-In Units

- Unit COM-6B/1
- Unit COM-6B/2
- Unit COM-6B/3

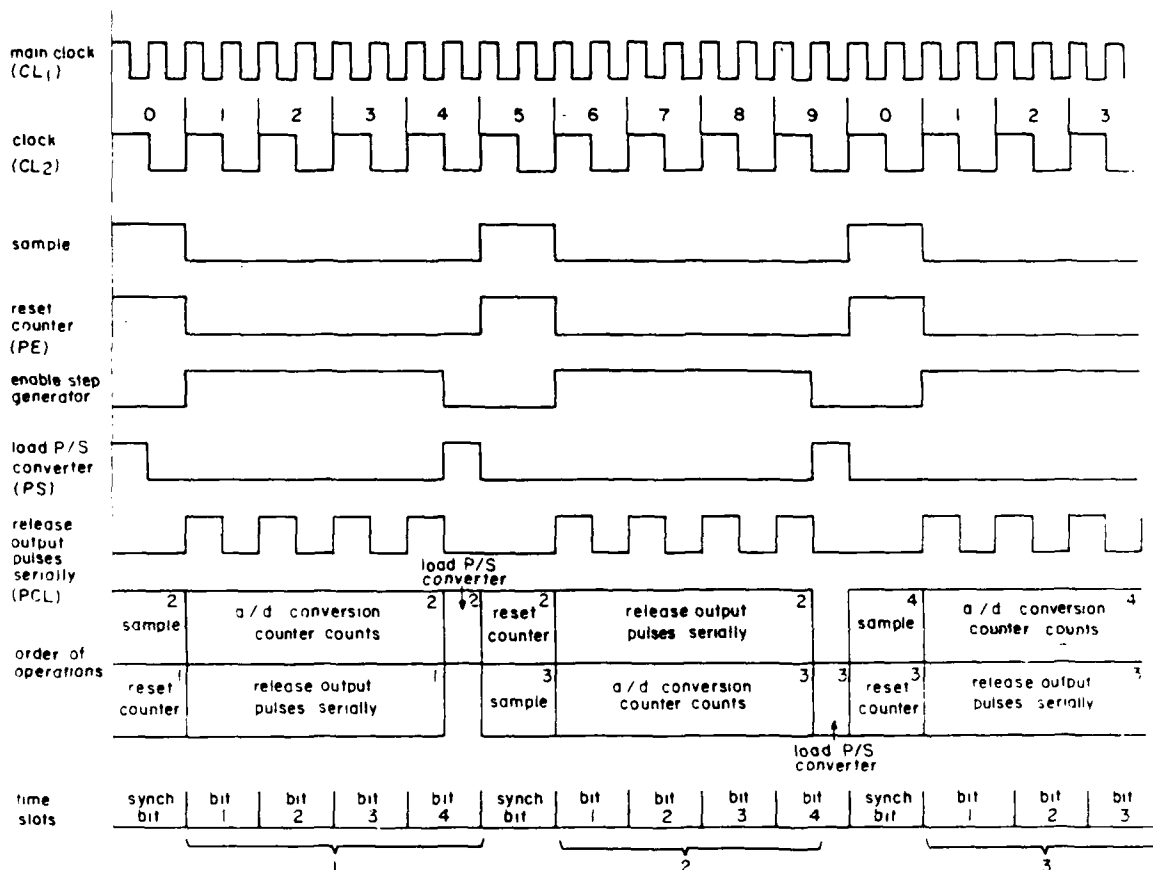


Figure 2. Improved PCM Modulator Timing Diagram. (1:61)

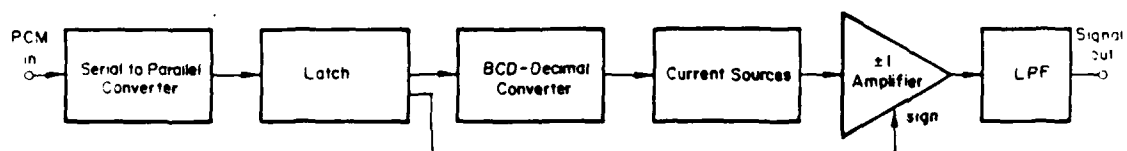


Figure 3. Block Diagram of PCM Demodulator. (1:149)

EXPERIMENT PROCEDURE

General Instructions

WARNING

Turn the DEGEM Power Supply Board off before removing or inserting any plug-in boards. Damage to circuit components may result if the boards are changed while the power is on.

1. DO NOT turn the DEGEM PS-MB-2/A Power Supply Board on. Install the Unit CDM-6A/1, 6A/2, 6A/3, 6B/1, 6B/2, and 6B/3 boards into the power supply board by pressing each unit into a power socket and tightening the hold-down screws on each end of the unit.
2. Turn the power supply board on. All plug-in units are internally powered and therefore need no external power connections. Adjust power supplies A and B to 12 Vdc measured by the meters on the power supply board.
3. Turn all of the remaining equipment on.

-IVI Amplifier

Objective: To study the operation of the -IVI amplifier, serving as an inverted full wave rectifier.

1. Assemble the circuit shown in figure 4. This circuit performs the operation of an inverted full wave rectifier.
2. Connect a 1 kHz, 2 Vpp sine wave from a signal generator to the input of the circuit. Use a frequency counter and oscilloscope to measure the input waveform.
3. Connect a dual trace oscilloscope to the input signal and the output of the Comp.1. Observe both waveforms triggering of the output signal. Notice that when the input sine wave is positive, the Comp.1 output is a logic "0" and vice versa.
4. Connect the output of the amplifier (output of SW1) to the oscilloscope in place of the Comp.1 output. Observe the inverted full wave rectified signal.

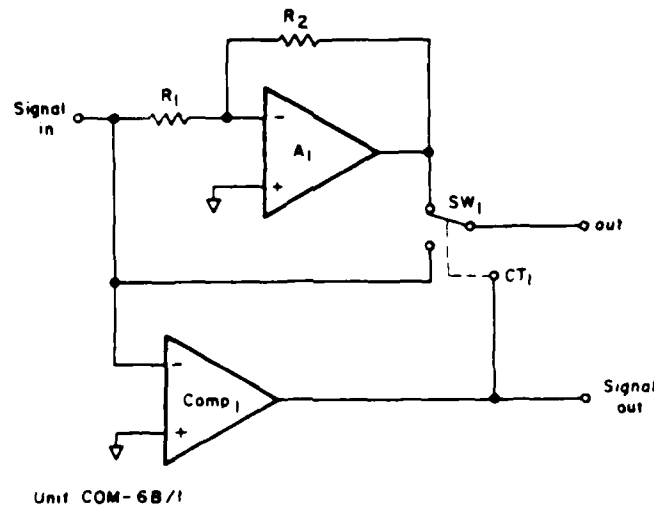


Figure 4. $-|V|$ Amplifier Circuit. (1:145)

5. Disconnect the Comp.₁ output from the CT₁ input and connect the Comp.₁ output to the input of the inverter gate (G₂) on Unit COM-6A/3. Connect the output of this gate to the CT₁ input. The effect of the sign indicator is now reversed by the inverter.
6. Observe the output rectified waveform and notice that it is now a positive full wave rectified sine wave.
7. Remove the inverter gate G₂ from the circuit and reconnect the Comp.₁ output to the CT₁ input.

Current Sources

Objective: To become familiar with the current sources that are part of the digital staircase generator.

1. Set the PCM mode switch on Unit COM-6B/1 to the Linear position.
2. Connect a DVM to R₃ on Unit COM-6B/1 set to read dc volts.

3. Connect the control input CI_1 on the set of current sources to +5 Vdc. Measure and record the R_s voltage. Change the PCM mode to Compressed and again measure and record the R_s voltage.
4. Add a jumper from CI_2 to +5 Vdc and again measure and record the R_s voltage for the Linear and Compressed modes. Do not disconnect CI_1 from +5 Vdc.
5. Continue to add jumpers between +5 Vdc and the other control inputs and record the R_s voltages for the Linear and Compressed modes.

Digital Staircase Generator

Objective: To study the characteristics of the digital staircase generator.

1. Connect the 40 kHz clock signal from the Clock Generator on Unit COM-6A/1 to the CL input of the Modulator Timing Counter located on the same board. Connect the R input of the counter to the "5" tap to generate a 5-stage counter.
2. Assemble the circuit as shown in figure 5. The "0" and "4" signals are provided by the Modulator Timing Counter on Unit COM-6A/1. The 40 kHz and 80 kHz signals are provided by the Clock Generator on that board.
3. Remove all current source control inputs from +5 Vdc. Connect the Q_1 through Q_7 outputs of the 7-stage Shift Register to the CI_1 through CI_7 inputs of the current sources.
4. Connect a dual trace oscilloscope to the 80 kHz signal and resistor R_s from the current sources. Draw the R_s waveform on the data sheet for Linear and Compressed PCM modes.

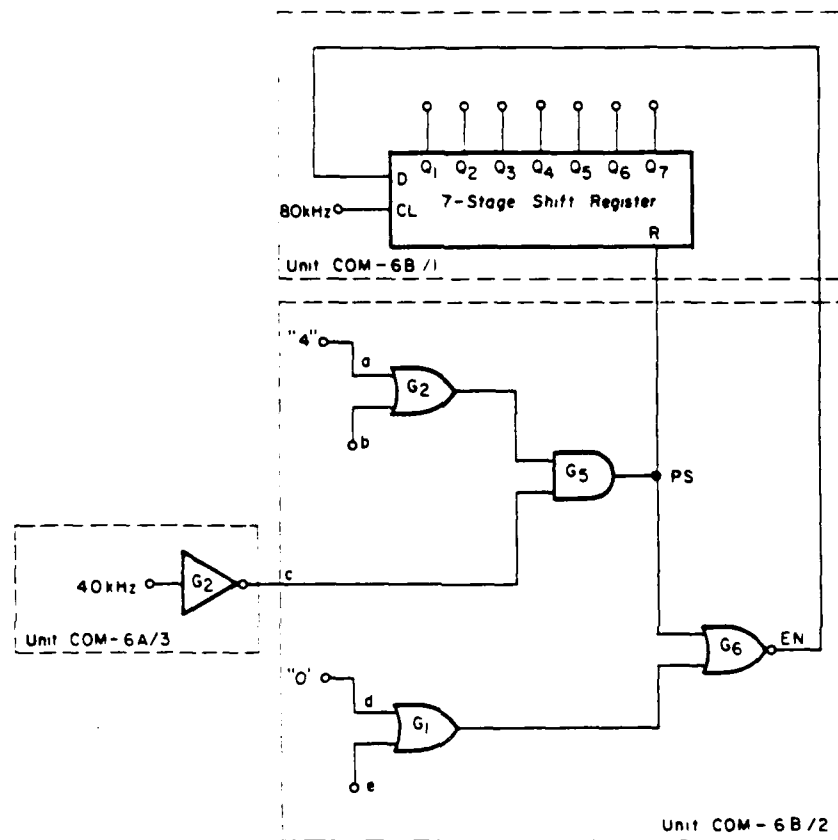


Figure 5. 7-stage Shift Register and Timing Circuits. (1:146)

Complete PCM Modulator

Objective: To observe the operation of the PCM modulator, study its timing characteristics, and determine its code-words with their respective input amplitude ranges.

1. Assemble the complete PCM modulator as shown in figure 6. Connect the control signals PS, EN, PCL, and PE to the inputs shown in the figure. The signal CO is not connected to anything.

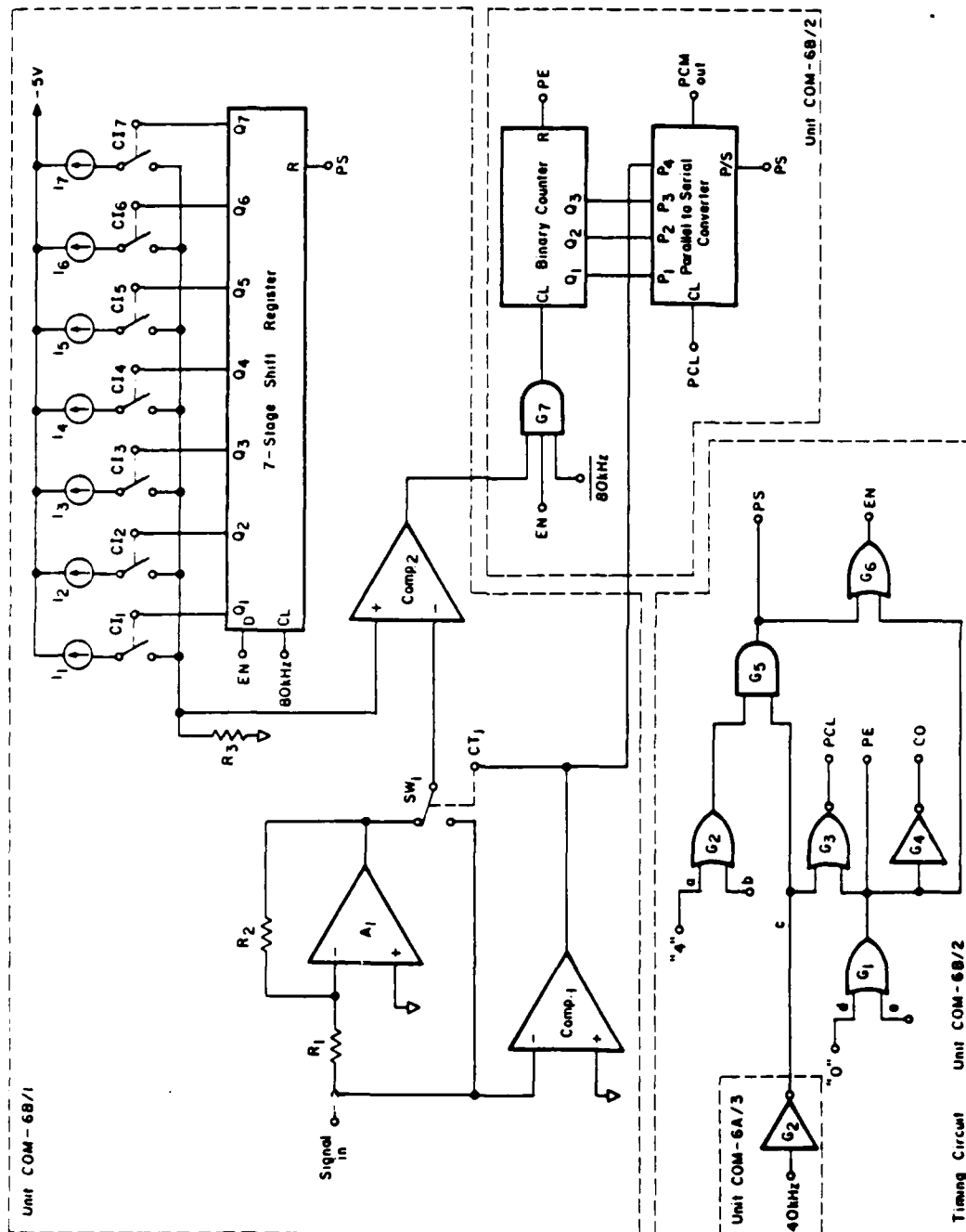


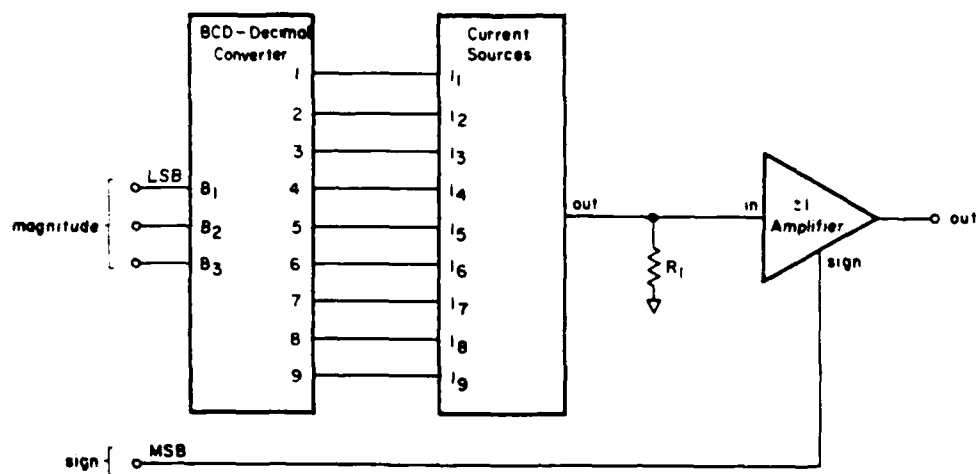
Figure 6. Complete PCM Modulator Circuit. (1:147)

2. Connect the dual trace oscilloscope to the different control signals (PE, EN, PS, and PCL) and to the clock signals (80 kHz and 40 kHz) to obtain a timing diagram of the signals. Draw the timing diagram of the control signals with reference to the 80 kHz and 40 kHz clocks on the provided data sheet.
3. Compare the timing diagram drawn to figure 2 in the theoretical background section. Do not continue until the function of each control signal is understood.
4. Connect a 0.001 Hz, 3.5 Vpp triangular wave from a signal generator to the input of the modulator circuit (Signal in). This signal will be used to determine the modulator code words and their respective input ranges.
5. Set the PCM mode to Linear.
6. Connect the dual trace oscilloscope to the PCL control signal and to the output of the modulator (PCM out). Trigger off the PCL signal.
7. Connect a DVM to the input signal set to measure dc voltage.
8. Observe the PCM codeword and the PCL signal on the oscilloscope. The PCM codeword bits are aligned with the four logic "1" pulses of the PCL signal. The MSB is the leftmost bit and is at a logic "1" when the input is less than 0 volts. The scan rate of the PCM codewords can be changed by varying the input triangular wave frequency slightly.
9. Observe the data codewords and determine and record their respective input voltage ranges (minimum and maximum input voltages) according to the data sheet.
10. Switch the PCM mode to Compressed and again determine and record the ranges for the PCM codewords.

D/A Converter

Objective: To study the operation of the D/A converter that is part of the PCM demodulator.

1. Connect the circuit as shown in figure 7. Set the demodulator in the LINEAR mode on Unit COM-6B/2.



Unit COM-6B /3

Figure 7. D/A Converter. (1:150)

2. Connect binary 4-bit words to the inputs B_1 through B_3 of the BCD-Decimal Converter and the sign input of the ± 1 Amplifier. An open connection is a logic "0" and a connection to +5 Vdc is a logic "1". For each binary word, measure the output dc voltage of the ± 1 Amplifier using a DVM. Record the voltages on the data sheet.
3. Repeat step 2 above for the EXPANDED mode.

Complete PCM Demodulator

Objective: To study the operation of the PCM demodulator.

1. Connect the complete PCM demodulator as shown in figure 8.
2. Connect the input of the demodulator to the PCM Out of the the modulator. Also connect the 40 kHz input to the 40 kHz signal of the Clock Generator on Unit COM-6A/1. Connect the Latch Cont. to the PS timing control signal on the modulator.

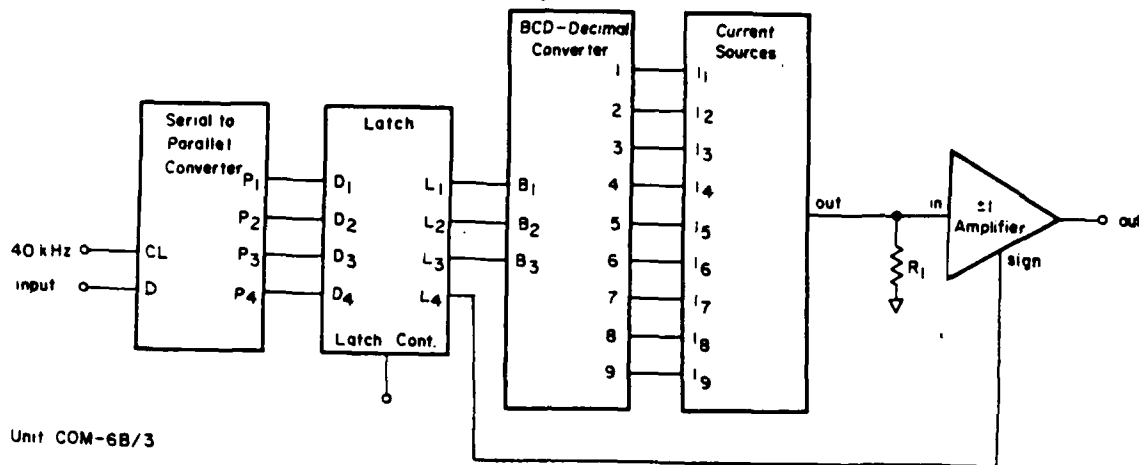


Figure 8. PCM Demodulator. (1:151)

3. Generate a 0.005 Hz, 3 Vpp triangular wave from a signal generator. Connect this signal to the input of the PCM modulator. Set the modulator and demodulator to the Linear mode.
4. Connect the modulator input signal and demodulator output signal to a dual trace oscilloscope. Set both oscilloscope channels in the ground mode and adjust the vertical position of the traces to the middle horizontal graticule line. Switch the channels to dc coupled and 500 mV/DIV.
5. Note how the input signal changes amplitude smoothly whereas the output signal changes amplitude abruptly.
6. Set the modulator to the Compressed mode and the demodulator to the Expanded mode. Observe both signals again. Then reset the modulator and demodulator back to the Linear modes.
7. Increase the input signal frequency to 100 Hz.
8. Observe the input and output signals. Vary the input amplitude and notice the affect on the output signal. Change the system to the Companded mode (modulator compressed and demodulator expanded) and again observe the signals.

9. Try different input signal waveforms (sine wave, square wave) and observe the signals in the Linear and Companded modes.
10. Connect a low pass filter on Unit COM-6A/1 to the demodulator output and observe the filtered output and the input on the oscilloscope for various amplitudes, frequencies, and waveforms.

Increased Frequency Response Using a Sample and Hold Circuit

Objective: To observe the effect of increasing the performance of the PCM system by using a sample and hold sampling circuit before coding the waveform.

1. Connect the circuit shown in figure 9 to the PCM modulator.

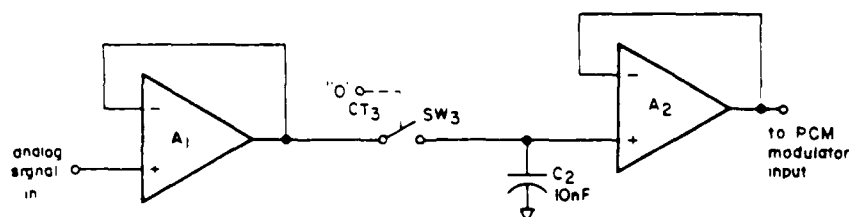


Figure 9. Sample and Hold Circuit. (1:152)

2. Connect the signal generator to the input of the sample and hold circuit and the output of the circuit to the PCM modulator input.
3. Again observe the demodulator output for different input waveforms, amplitudes, and frequencies. Observe the system in the Linear and Companded modes. Note that the system works better (less demodulated output distortion) for higher input frequencies than the system without the sample and hold circuit.

STUDENT NAMES _____ DATE PERFORMED _____

Note: Indicate unit of measurement with each data entry.

CURRENT SOURCES

CI ₁	CI ₂	CI ₃	CI ₄	CI ₅	CI ₆	CI ₇	R _s Voltage	
							Linear	Compress
+5	open	open	open	open	open	open	-----	-----
+5	+5	open	open	open	open	open	-----	-----
+5	+5	+5	open	open	open	open	-----	-----
+5	+5	+5	+5	open	open	open	-----	-----
+5	+5	+5	+5	+5	open	open	-----	-----
+5	+5	+5	+5	+5	+5	open	-----	-----
+5	+5	+5	+5	+5	+5	+5	-----	-----

DIGITAL STAIRCASE GENERATOR

LINEAR STAIRCASE

COMPRESSED STAIRCASE

PCM MODULATOR

CL₁
(80 kHz)CL₂
(40 kHz)

PE

EN

PS

PCL

PCM CODEWORDS

LINEAR

Codeword	Minimum Voltage	Maximum Voltage	Codeword	Minimum Voltage	Maximum Voltage
0111	-----	+5 Vdc	1000	-----	-----
0110	-----	-----	1001	-----	-----
0101	-----	-----	1010	-----	-----
0100	-----	-----	1011	-----	-----
0011	-----	-----	1100	-----	-----
0010	-----	-----	1101	-----	-----
0001	-----	-----	1110	-----	-----
0000	-----	-----	1111	-5 Vdc	-----

COMPRESSED

Codeword	Minimum Voltage	Maximum Voltage	Codeword	Minimum Voltage	Maximum Voltage
0111	-----	+5 Vdc	1000	-----	-----
0110	-----	-----	1001	-----	-----
0101	-----	-----	1010	-----	-----
0100	-----	-----	1011	-----	-----
0011	-----	-----	1100	-----	-----
0010	-----	-----	1101	-----	-----
0001	-----	-----	1110	-----	-----
0000	-----	-----	1111	-5 Vdc	-----

D/A CONVERTER

LINEAR

SIGN	B ₃	B ₂	B ₁	VOLTAGE	SIGN	B ₃	B ₂	B ₁	VOLTAGE
0	0	0	0	-----	1	0	0	0	-----
0	0	0	1	-----	1	0	0	1	-----
0	0	1	0	-----	1	0	1	0	-----
0	0	1	1	-----	1	0	1	1	-----
0	1	0	0	-----	1	1	0	0	-----
0	1	0	1	-----	1	1	0	1	-----
0	1	1	0	-----	1	1	1	0	-----
0	1	1	1	-----	1	1	1	1	-----

EXPANDED

SIGN	B ₃	B ₂	B ₁	VOLTAGE
0	0	0	0	_____
0	0	0	1	_____
0	0	1	0	_____
0	0	1	1	_____
0	1	0	0	_____
0	1	0	1	_____
0	1	1	0	_____
0	1	1	1	_____

SIGN	B ₃	B ₂	B ₁	VOLTAGE
1	0	0	0	_____
1	0	0	1	_____
1	0	1	0	_____
1	0	1	1	_____
1	1	0	0	_____
1	1	0	1	_____
1	1	1	0	_____
1	1	1	1	_____

STUDENT NAMES _____ SAMPLE _____ DATE PERFORMED _____

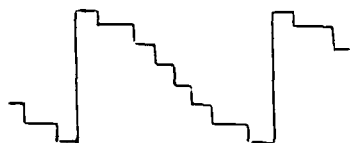
Note: Indicate unit of measurement with each data entry.

CURRENT SOURCES

CI ₁	CI ₂	CI ₃	CI ₄	CI ₅	CI ₆	CI ₇	R _s Voltage	
							Linear	Compress
+5	open	open	open	open	open	open	-0.210	-0.045
+5	+5	open	open	open	open	open	-0.419	-0.112
+5	+5	+5	open	open	open	open	-0.627	-0.211
+5	+5	+5	+5	open	open	open	-0.834	-0.359
+5	+5	+5	+5	+5	open	open	-1.035	-0.581
+5	+5	+5	+5	+5	+5	open	-1.224	-0.906
+5	+5	+5	+5	+5	+5	+5	-1.369	-1.397

DIGITAL STAIRCASE GENERATOR

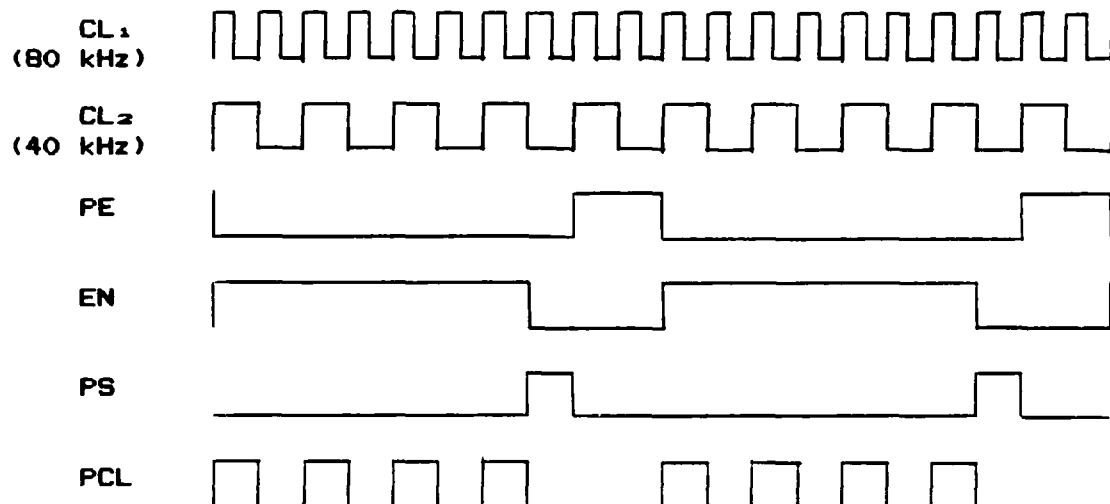
LINEAR STAIRCASE



COMPRESSED STAIRCASE



PCM MODULATOR



PCM CODEWORDS

LINEAR

Codeword	Minimum Voltage (V _{dc})	Maximum Voltage (V _{dc})	Codeword	Minimum Voltage (V _{dc})	Maximum Voltage (V _{dc})
0111	<u>1.46</u>	<u>+5 V_{dc}</u>	1000	<u>-0.38</u>	<u>0.00</u>
0110	<u>1.23</u>	<u>1.46</u>	1001	<u>-0.61</u>	<u>-0.38</u>
0101	<u>1.20</u>	<u>1.23</u>	1010	<u>-0.80</u>	<u>-0.61</u>
0100	<u>1.02</u>	<u>1.20</u>	1011	<u>-1.00</u>	<u>-0.80</u>
0011	<u>0.81</u>	<u>1.02</u>	1100	<u>-1.22</u>	<u>-1.00</u>
0010	<u>0.61</u>	<u>0.81</u>	1101	<u>-1.23</u>	<u>-1.22</u>
0001	<u>0.40</u>	<u>0.61</u>	1110	<u>-1.44</u>	<u>-1.23</u>
0000	<u>0.00</u>	<u>0.40</u>	1111	<u>-5 V_{dc}</u>	<u>-1.44</u>

COMPRESSED

Codeword	Minimum Voltage (Vdc)	Maximum Voltage (Vdc)	Codeword	Minimum Voltage (Vdc)	Maximum Voltage (Vdc)
0111	<u>1.48</u>	<u>+5 Vdc</u>	1000	<u>-0.13</u>	<u>0.00</u>
0110	<u>1.11</u>	<u>1.48</u>	1001	<u>-0.23</u>	<u>-0.13</u>
0101	<u>0.92</u>	<u>1.11</u>	1010	<u>-0.41</u>	<u>-0.23</u>
0100	<u>0.68</u>	<u>0.92</u>	1011	<u>-0.67</u>	<u>-0.41</u>
0011	<u>0.42</u>	<u>0.68</u>	1100	<u>-0.90</u>	<u>-0.67</u>
0010	<u>0.24</u>	<u>0.42</u>	1101	<u>-1.11</u>	<u>-0.90</u>
0001	<u>0.13</u>	<u>0.24</u>	1110	<u>-1.46</u>	<u>-1.11</u>
0000	<u>0.00</u>	<u>0.13</u>	1111	<u>-5 Vdc</u>	<u>-1.46</u>

D/A CONVERTER

LINEAR

SIGN	B ₃	B ₂	B ₁	VOLTAGE (Vdc)	SIGN	B ₃	B ₂	B ₁	VOLTAGE (Vdc)
0	0	0	0	<u>0.016</u>	1	0	0	0	<u>0.007</u>
0	0	0	1	<u>0.256</u>	1	0	0	1	<u>-0.214</u>
0	0	1	0	<u>0.481</u>	1	0	1	0	<u>-0.420</u>
0	0	1	1	<u>0.710</u>	1	0	1	1	<u>-0.630</u>
0	1	0	0	<u>0.928</u>	1	1	0	0	<u>-0.831</u>
0	1	0	1	<u>1.143</u>	1	1	0	1	<u>-1.029</u>
0	1	1	0	<u>1.375</u>	1	1	1	0	<u>-1.242</u>
0	1	1	1	<u>1.606</u>	1	1	1	1	<u>-1.454</u>

EXPANDED

SIGN	B ₃	B ₂	B ₁	VOLTAGE (V _{dc})	SIGN	B ₃	B ₂	B ₁	VOLTAGE (V _{dc})
0	0	0	0	<u>0.016</u>	1	0	0	0	<u>-0.007</u>
0	0	0	1	<u>0.063</u>	1	0	0	1	<u>-0.037</u>
0	0	1	0	<u>0.133</u>	1	0	1	0	<u>-0.101</u>
0	0	1	1	<u>0.235</u>	1	0	1	1	<u>-0.195</u>
0	1	0	0	<u>0.398</u>	1	1	0	0	<u>-0.344</u>
0	1	0	1	<u>0.638</u>	1	1	0	1	<u>-0.564</u>
0	1	1	0	<u>0.977</u>	1	1	1	0	<u>-0.876</u>
0	1	1	1	<u>1.574</u>	1	1	1	1	<u>-1.424</u>

APPENDIX L

Laboratory Experiment Number 9

Delta Modulation

The topics of this experiment include:

1. Delta modulation and demodulation
2. Integrating, adaptive, and current source delta modulation
3. Effects of slope-overloading

OBJECTIVE: To familiarize the student with the principles and circuits of Delta Modulation (DM) and Demodulation.

PREREQUISITES: Completion of Lab 1, "Equipment Familiarization".

REQUIRED EQUIPMENT

The following equipment is required to perform this experiment. It is assumed the student is familiar with the controls and functions of each item listed below.

1. Oscilloscope (dual trace)
2. Signal Generator (CW capability)
3. Frequency Counter (0 to 2 MHz minimum)
4. Digital Voltmeter (DVM)
5. Test Leads
6. DEGEM PS-MB-2/A Power Supply Board
7. DEGEM Boards Unit COM-6A/1
Unit COM-6C/1
Unit COM-6C/2
Unit COM-6C/3

REFERENCES

1. DEGEM Systems Ltd. Time Division Multiplexing; Sampling & Multiplexing, Pulse Code Modulation, & Delta Modulation Course COM-6. DEGEM Systems Ltd., 1976.

THEORETICAL BACKGROUND

SOURCE: Reference (1).

Chapter 7 - Delta Modulation

Additional Background

The maximum input sine wave frequency (f_m) to prevent slope overload in a DM modulator is dependent on:

- step size of the modulator (Δ)
- sampling frequency (f_s)
- amplitude of the input signal (A)

with the following relationship.

$$f_m = \Delta f_e / 2\pi A \quad (1)$$

DEGEM CIRCUIT BOARD DESCRIPTION

SOURCE: Reference (1).

Technical Description of Plug-In Units

- Unit COM-6C/1
- Unit COM-6C/2
- Unit COM-6C/3

EXPERIMENT PROCEDURE

General Instructions

WARNING

Turn the DEGEM Power Supply Board off before removing or inserting any plug-in boards. Damage to circuit components may result if the boards are changed while the power is on.

1. DO NOT turn the DEGEM PS-MB-2/A Power Supply Board on. Install the Unit COM-6A/1, 6C/1, 6C/2, and 6C/3 boards into the power supply board by pressing each unit into a power socket and tightening the hold-down screws on each end of the unit.
2. Turn the power supply board on. All plug-in units are internally powered and therefore need no external power connections. Adjust power supplies A and B to 12 Vdc measured by the meters on the power supply board.
3. Turn all of the remaining equipment on.

Integrating Delta Modulator

Objective: To study the operation of the integrating delta modulator, including its step generator and integrator. Also to observe the effects of slope-overloading.

1. Step Generator Operation:

- a. Connect the POL. (polarity) input of the Step Generator on Unit COM-6C/1 to a logic "0" (-5 Vdc). Adjust the Step Gen. Balance Control (P₁) to its center position.
- b. Connect a DVM to the output of the Step Generator set to measure dc voltage.
- c. Connect control input ST₁ to +5 Vdc. Measure and record the output voltage. This is the step size for step ST₁.
- d. Disconnect ST₁ from +5 Vdc and connect ST₂ to +5 Vdc. Measure and record the output voltage (step size for ST₂).
- e. Repeat this same procedure to measure the step sizes for ST₃ and ST₄, never allowing more than one step control input to be connected to +5 Vdc at any one time.
- f. Connect POL. to a logic "1" (+5 Vdc) and repeat steps c through e above for the positive steps.

2. Integrator Operation:

- a. Assemble the integrator circuit shown in figure 1. The 20 kHz clock signal is available from the Clock Generator on Unit COM-6A/1.

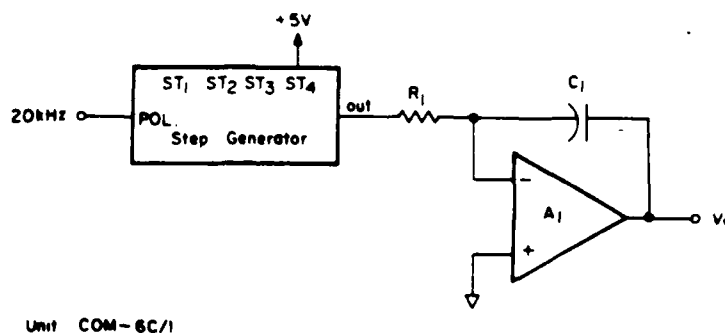
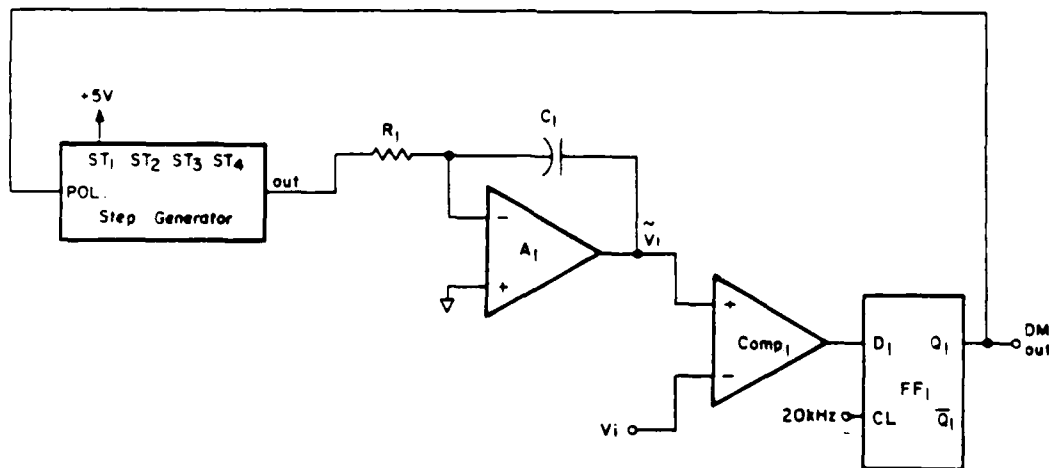


Figure 1. Test Circuit for Integrator. (1:162)

- b. Connect a dual trace oscilloscope to the POL. input and to the output of integrator A_1 . Observe both signals.
- c. Connect the other step control inputs of the Step Generator to +5 Vdc never allowing more than one control input to be connected to +5 Vdc. Observe the output waveform in each case and notice the step size change.

3. Integrating Delta Modulator:

- a. Assemble the integrating delta modulator shown in figure 2. The 20 kHz signal is available on Unit COM-6A/1.



Unit COM-6C/1

Figure 2. Integrating Delta Modulator. (1:163)

- b. Connect the input of the modulator (V_i) to ground and ST_2 on the Step Generator to +5 Vdc instead of ST_1 . Connect the oscilloscope to the 20 kHz signal

and to the output of the integrator. Observe both waveforms.

- c. Vary the Step Gen. Balance Control and notice the effect on the output of the integrator. If the up and down steps are balanced, the comparator waveform will appear as shown in figure 3(a). If the up and down steps are not equal, the waveform will appear as shown in figure 3(b) or 3(c).

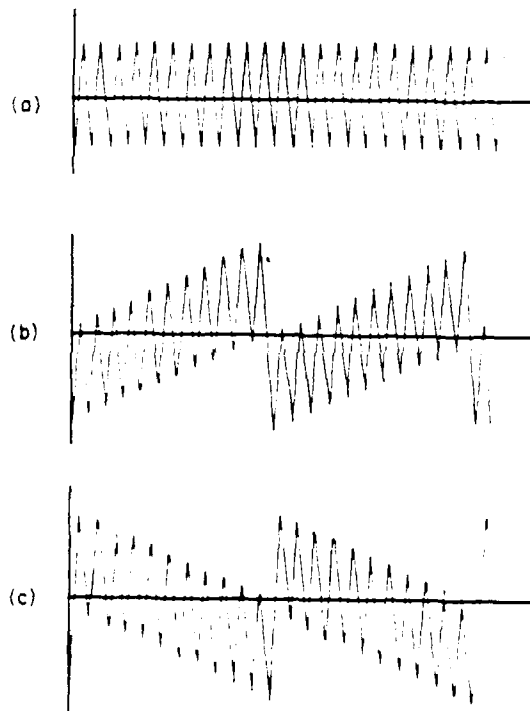


Figure 3. Integrator Output Waveforms. (1:164)

- d. It is easier to balance the Step Generator by observing the output of the comparator. Connect the oscilloscope to this output and vary the Step Gen. Balance Control. Adjust the control until a 50% duty cycle steady square wave is obtained. Connect the oscilloscope to the output of the integrator and notice that the waveform is a steady triangular wave as shown in figure 3(a).

- e. After adjusting the Step Gen. Balance Control properly, draw a timing diagram of the integrator output and the D_1 signal on the data sheet.

4. Square Wave Input:

- a. Replace the 20 kHz clock in figure 2 with an 80 kHz clock. This is now the sampling rate of the modulator.
- b. Connect the 20 kHz clock signal to the input of the modulator.
- c. Draw a timing diagram of the 80 kHz clock, 20 kHz clock, integrator output, comparator output, and DM out.
- d. Notice that after the integrator output exceeds the input amplitude, it starts a down slope on the next 80 kHz clock cycle. Also note that when the integrator output has a positive slope, the DM out signal is at logic "1" and vice versa.

5. Slope-overloading:

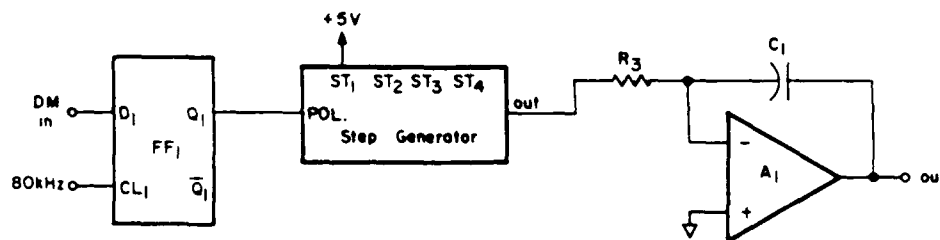
- a. Using equation (1) in the theoretical background section, calculate and record the maximum input frequency for a 3 Vpp (1.5 Vp) sine wave using the step size of that given by ST_2 of the Step Generator (average the positive and negative step sizes as recorded on the data sheet) and a sampling frequency of 80 kHz.
- b. Connect a 1 kHz (± 500 Hz), 3 Vpp sine wave from a signal generator to the input of the modulator, measured with an oscilloscope. Use step size ST_2 on the Step Generator.
- c. Connect the dual trace oscilloscope to the input and integrator output signals of the modulator. Trigger off the input signal. Observe both waveforms.
- d. Slowly increase the input frequency until slope over-overloading occurs (i.e. the integrator output no longer tracks the input sine wave). Determine and record the frequency where slope-overloading occurs using a frequency counter.

- e. Change the integrator resistor from R_1 to R_2 and again determine and record the input frequency where slope-overloading occurs.
- f. Change to the integrator resistor R_3 and determine and record the slope-overloading frequency.
- g. Vary the sample rate, step size, integrator resistors, and input amplitudes and notice the effect of these parameters on the integrator output signal.

Delta Demodulator

Objective: To observe the timing characteristics of the delta demodulator.

1. Assemble the demodulator as shown in figure 4.



Unit COM-6C/2

Figure 4. Delta Demodulator. (1:166)

2. Connect the 20 kHz clock signal to the DM input.
3. Draw a timing diagram of the 80 kHz clock signal, the 20 kHz input, Q_1 , and the integrator output. Notice that the demodulator is simply a DM modulator without a comparator.

DM Channel

Objective: To observe the output of the full DM system using the demodulator from the last section.

1. Connect the DM modulator output to the input of the DM de-modulator. The modulator and demodulator should use an 80 kHz clock, the integrating resistor R_1 , and the smallest step size (ST_1 connected to +5 Vdc).
2. Connect a LPF on Unit COM-6A/1 to the output of the demodulator.
3. Connect a 1 kHz, 3 Vpp sine wave to the input of the modulator measured with a frequency counter and oscilloscope.
4. Connect the dual trace oscilloscope to the input signal and to the output of the LPF. Observe both waveforms triggering off the input signal.
5. Vary the input amplitude and frequency and notice the effect on the output signal. Also change the step sizes on both the modulator and demodulator along with the integrating resistors.

Adaptive Delta Modulation

Objective: To investigate the technique of adaptive delta modulation, studying the step generator characteristics, modulator, and demodulator.

1. The Step Generator with Ring Counter:
 - a. Assemble the circuit shown in figure 5.

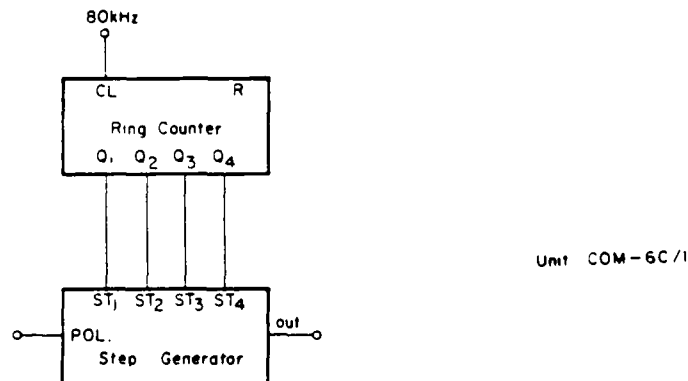


Figure 5. Step Generator Circuit. (1:169)

- b. Connect the POL. input of the step generator to -5 Vdc and draw a timing diagram of the 80 kHz clock, the four outputs of the ring counter, and the output of the step generator. Use an oscilloscope. Notice that the Ring Counter selects the step size.
- c. Change the POL. input to $+5$ Vdc and draw the output of the step generator on the same timing diagram.
- d. Connect a 10 kHz, 10 Vpp square wave from a signal generator to the reset input (R) of the Ring Counter. Observe the reset signal and the output of the step generator on the oscilloscope.
- e. Increase the input square wave frequency and notice how the output steps are "chopped off" when the reset signal changes to $+5$ Vdc.

2. Complete Modulator:

- a. Connect the complete adaptive delta modulator as shown in figure 6.

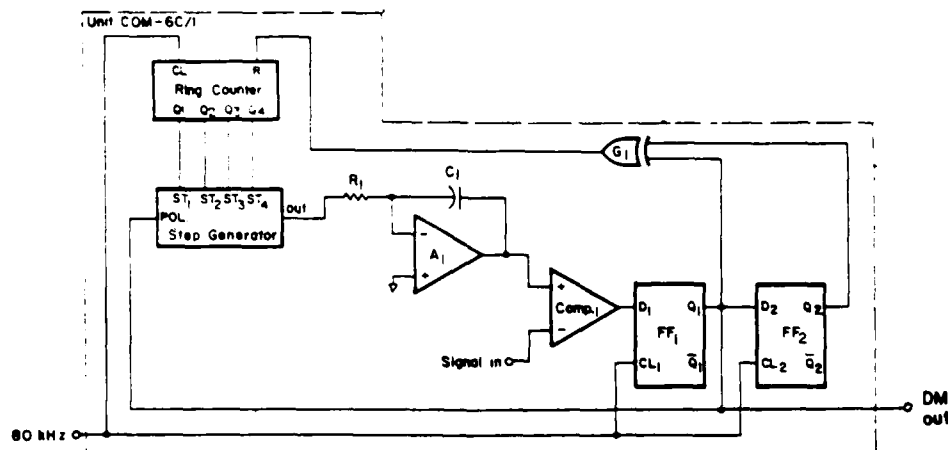


Figure 6. Adaptive Delta Modulator. (1:170)

- b. Connect a 20 kHz signal from the Clock Generator on Unit COM-6A/1 to the input of the modulator.

- c. Draw a timing diagram of the 80 kHz clock and signals at Signal in, R, POL., D₁, and the integrator output.
- d. Notice the different step sizes used in the integrator output signal. Change the input to a 10 kHz clock signal and again observe the integrator output. Notice the additional steps used.

3. Complete Adaptive Delta Channel:

- a. Connect the demodulator circuit shown in figure 7 to the modulator (i.e. DM out of the modulator to DM in of the demodulator).

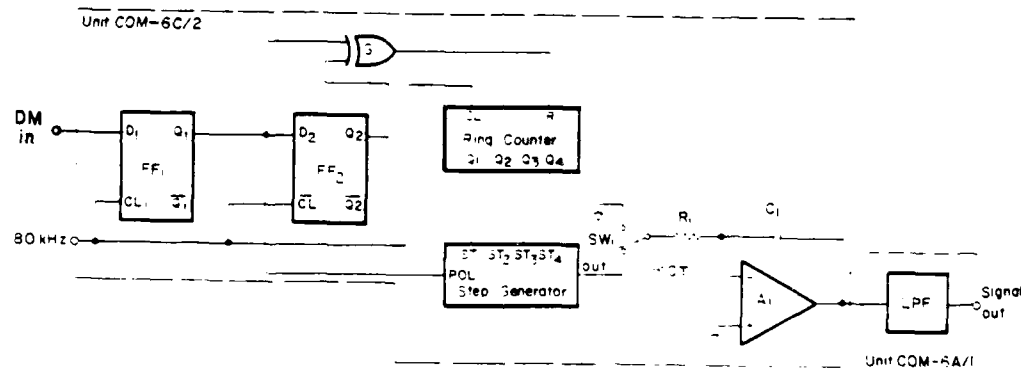


Figure 7. Adaptive Delta Demodulator. (1:171)

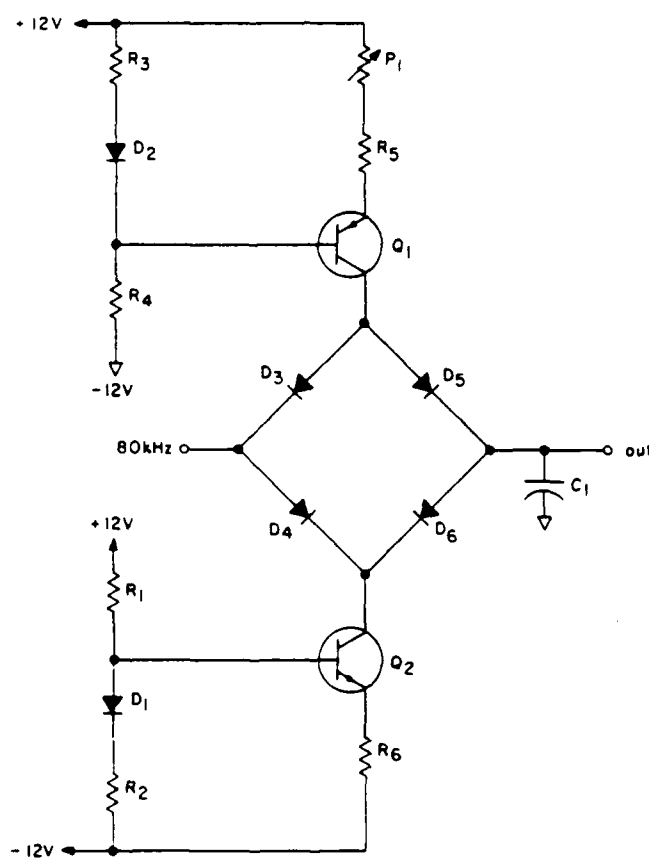
- b. Connect a 1 kHz, 1 Vpp sine wave from a signal generator to the input of the modulator. Use a frequency counter and oscilloscope to measure the input signal.
- c. Observe the output of the LPF on the oscilloscope for different integrating resistors and input frequencies. Also connect the oscilloscope to the input of the LPF and notice the variety of step sizes used.

Current Source Delta Modulation

Objective: To observe the delta modulation system using switched current sources.

1. Switched Current Sources:

- a. Connect the circuit shown in figure 8.



Unit COM-6C/3

Figure 8. Switched Current Sources. (1:174)

- b. Observe the output at capacitor C_1 and notice that it is the same type of waveform obtained from the integrator of the non-adaptive delta modulator. Stabilize the output by adjusting potentiometer P_1 which balances the current sources.

2. Complete Delta Modulator:

- a. Connect the circuit as shown in figure 9.

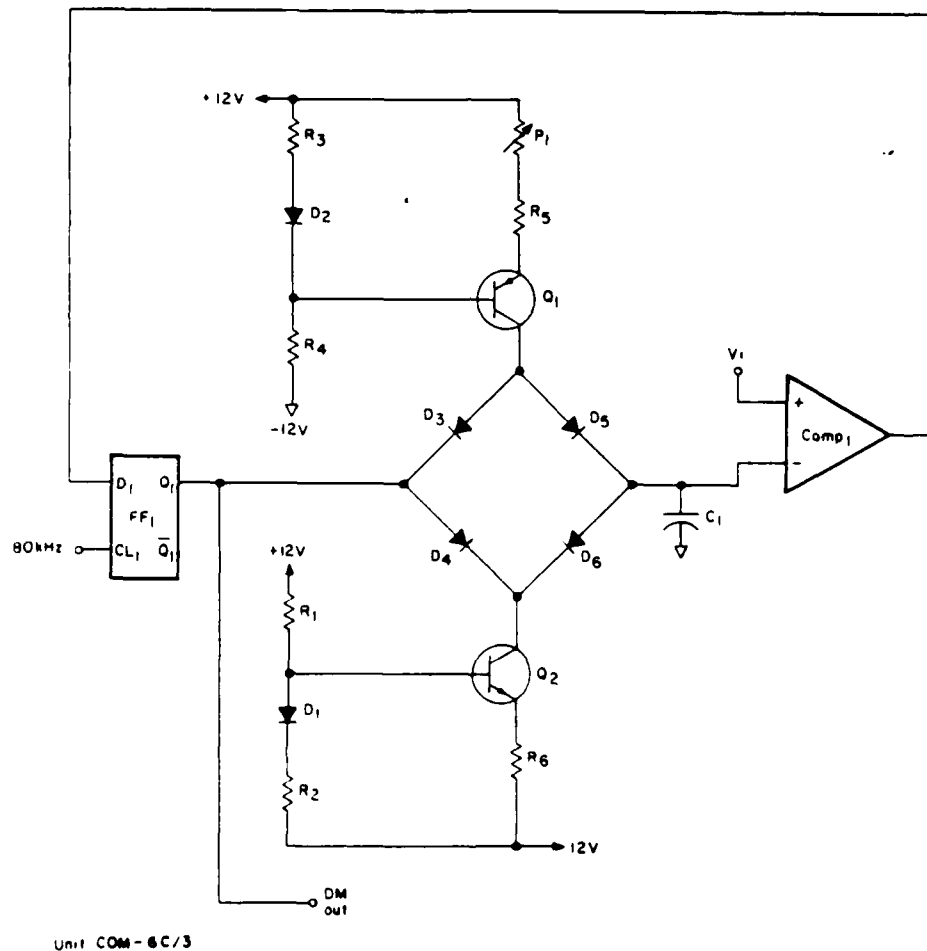
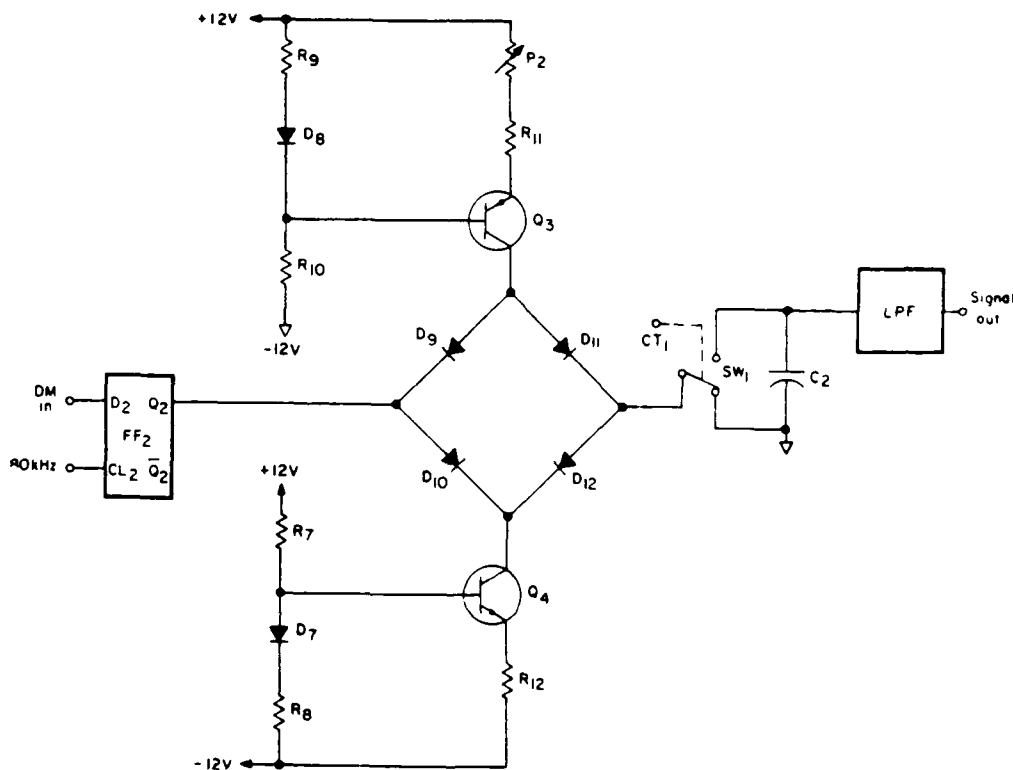


Figure 9. Delta Modulator. (1:175)

- b. Connect a 1 kHz, 3 Vpp sine wave from a signal generator to the input of the modulator (Vi). Connect the C₁ signal and DM out to the dual trace oscilloscope. Trigger off the C₁ signal.
- c. Notice that DM out has more logic zeros for the down slope of the C₁ signal than the up slope. Increase the input frequency up to a point just before slope overloading and notice the distribution of ones and zeros in the DM out signal.

3. Complete DM Channel:

- a. Assemble the delta demodulator shown in figure 10 and connect DM in to DM out of the modulator. Use one of the LPFs found on Unit COM-6A/1 for the output filter.



Unit COM-6C/3

Figure 10. Delta Demodulator. (1:176)

- b. Connect the control of SW₁ (CT₁) to +5 Vdc to connect the demodulator output signal to the LPF.
- c. Use a 1 kHz, 3 Vpp sine wave from a signal generator as an input signal to the modulator. Use a frequency counter and oscilloscope measure the signal.
- d. Observe the output of the LPF for different input amplitudes and frequencies.

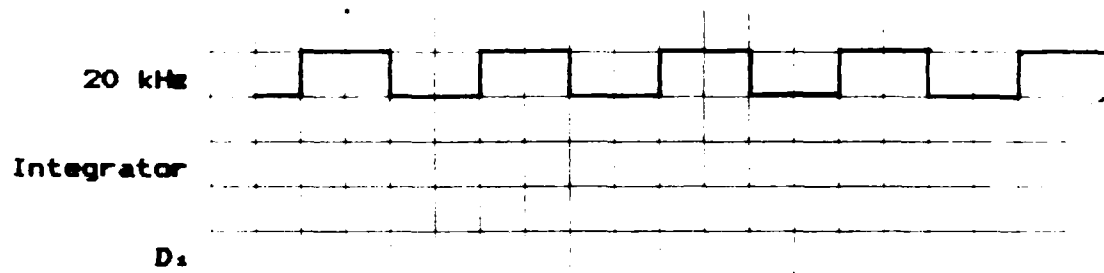
STUDENT NAMES _____ DATE PERFORMED _____

Note: Indicate unit of measurement with each data entry.

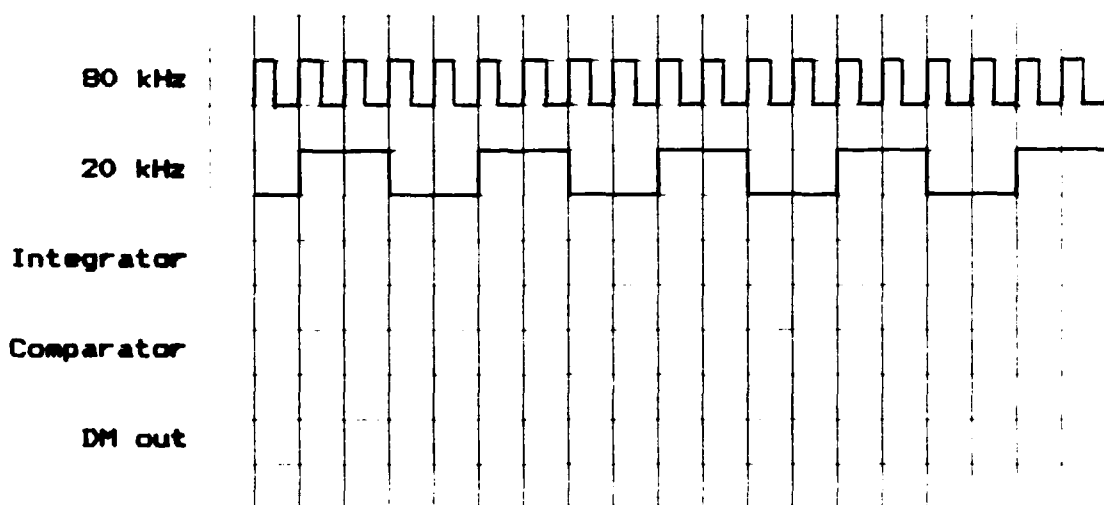
STEP GENERATOR

	ST ₁	ST ₂	ST ₃	ST ₄
Output Voltage (-)	_____	_____	_____	_____
(+)	_____	_____	_____	_____

TIMING DIAGRAM 1



TIMING DIAGRAM 2



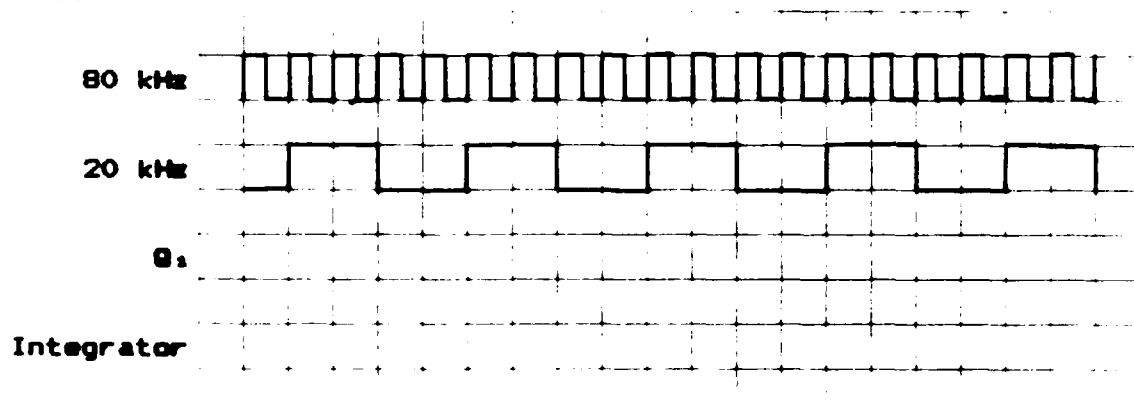
SLOPE-OVERLOADING

Max Frequency (theoretical) _____

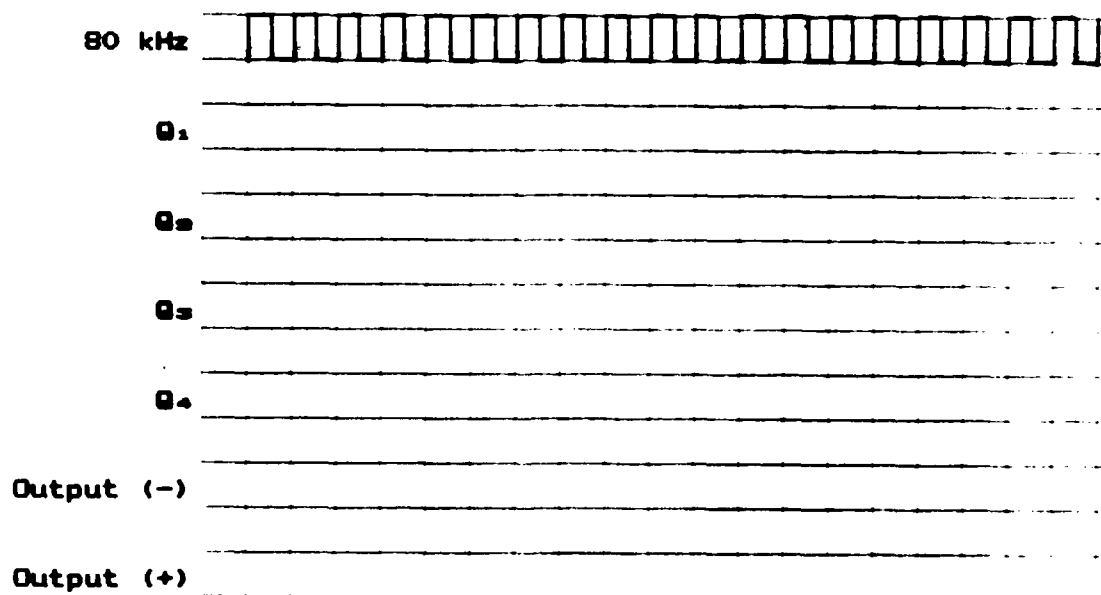
 R_1 R_2 R_3

Max Frequency _____

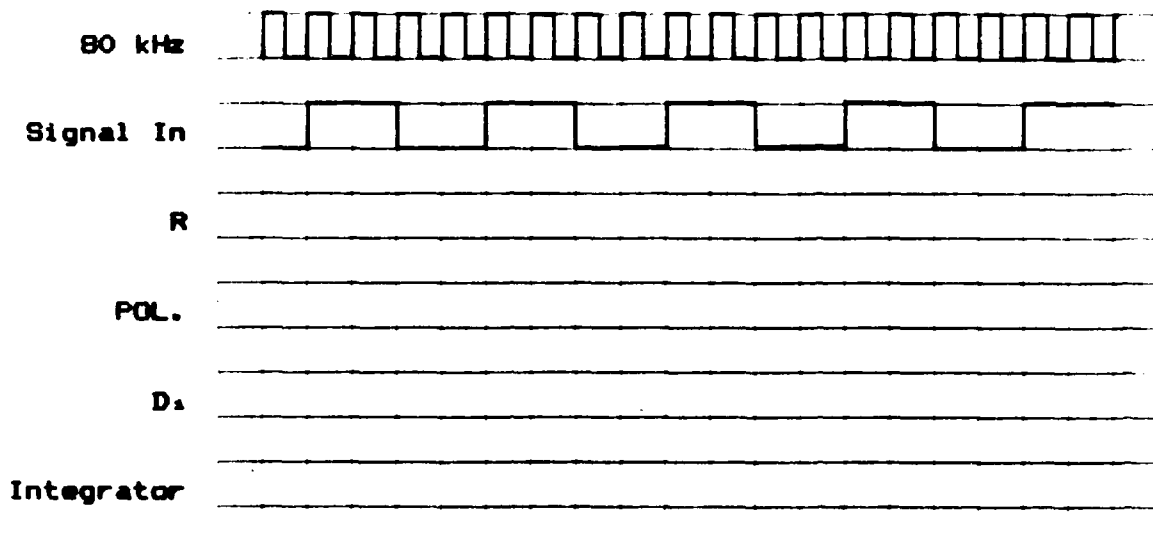
DEMODULATOR



ADAPTIVE DELTA MODULATION



ADAPTIVE MODULATOR



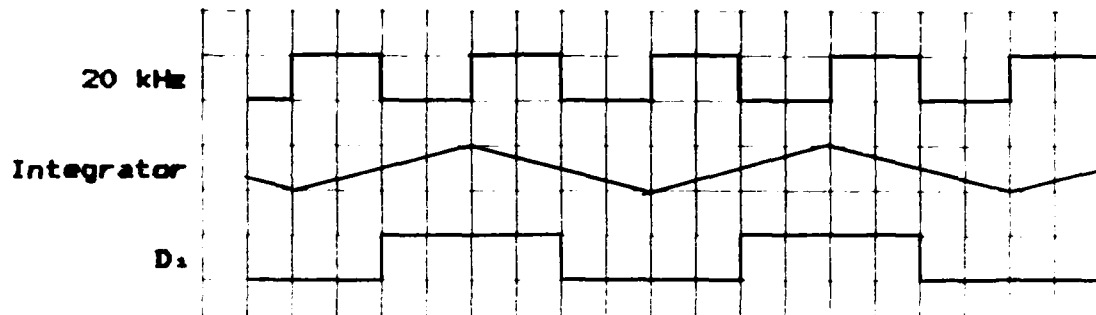
STUDENT NAMES SAMPLE DATE PERFORMED

Note: Indicate unit of measurement with each data entry.

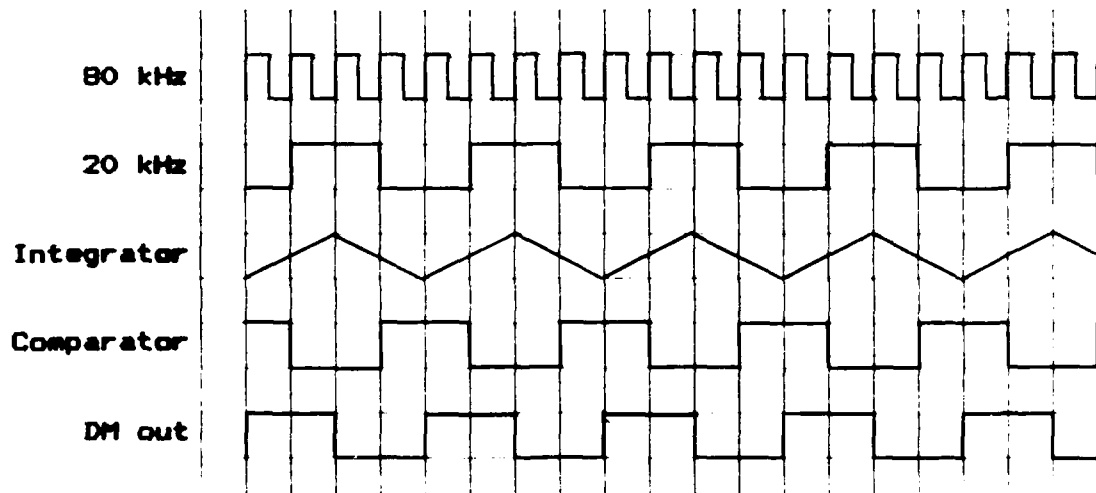
STEP GENERATOR

	ST ₁	ST ₂	ST ₃	ST ₄
Output Voltage (-) (V _{dc})	<u>-0.462</u>	<u>-0.931</u>	<u>-1.860</u>	<u>-3.67</u>
(+)	<u>0.486</u>	<u>0.968</u>	<u>1.900</u>	<u>3.61</u>

TIMING DIAGRAM 1



TIMING DIAGRAM 2

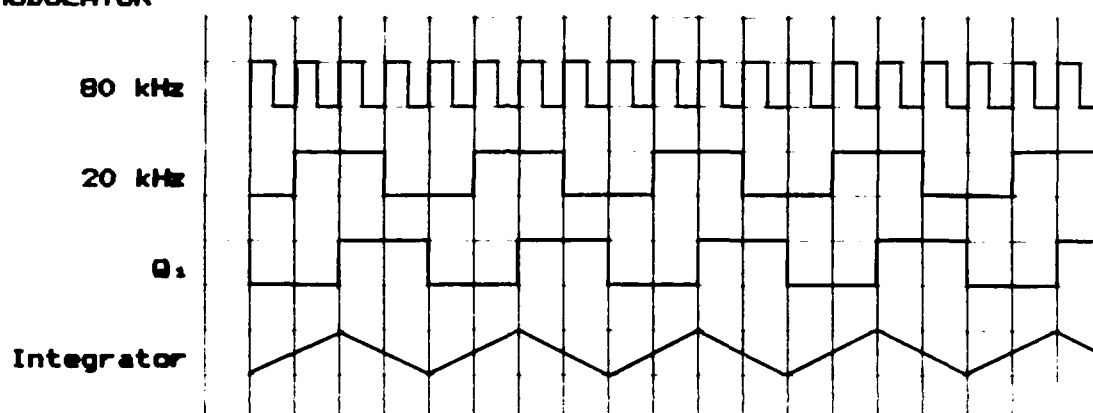


SLOPE-OVERLOADING

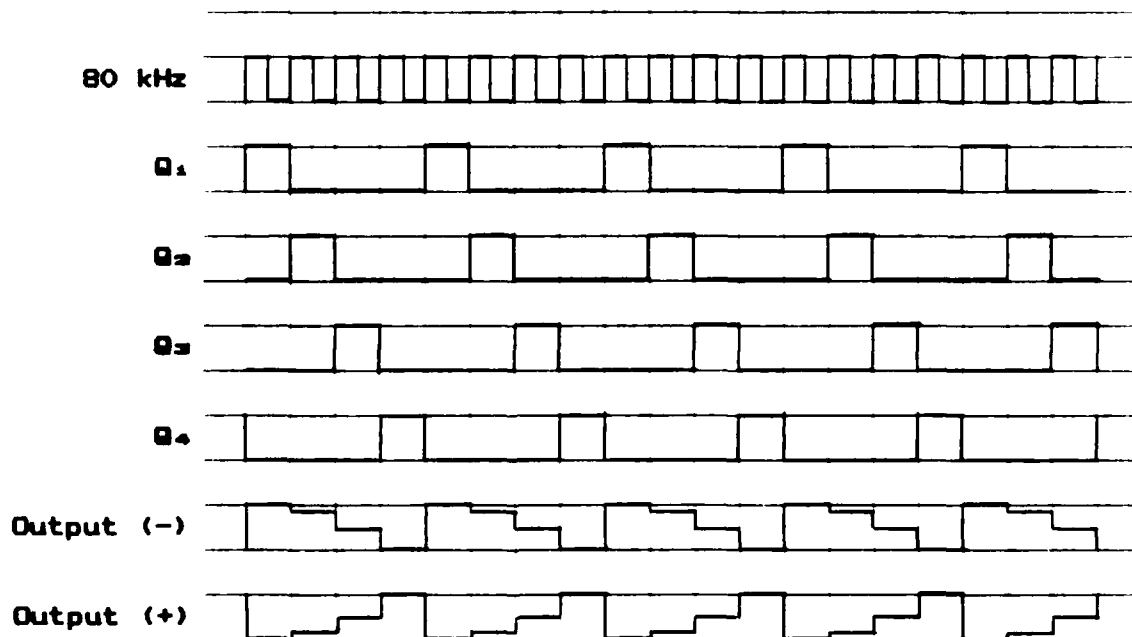
Max Frequency (theoretical) 8.06 kHz

	R_1	R_2	R_3
Max Frequency	<u>2.34 kHz</u>	<u>1.10 kHz</u>	<u>0.58 kHz</u>

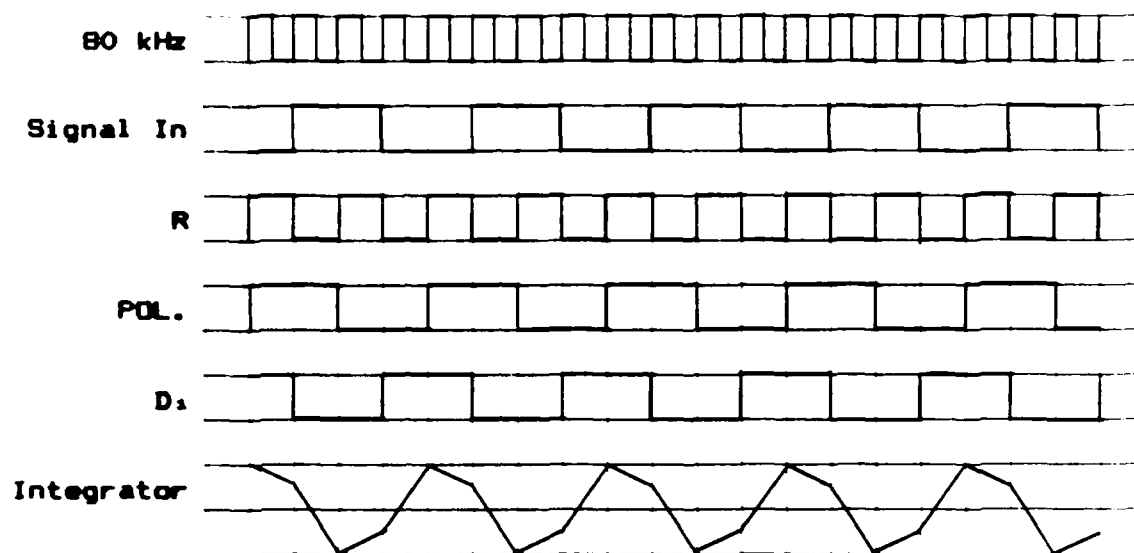
DEMODULATOR



ADAPTIVE DELTA MODULATION



ADAPTIVE MODULATOR



APPENDIX M

Laboratory Experiment Number 10

Amplitude Shift Keying

This experiment investigates the performance characteristics (bit error rate versus input signal-to-noise ratio) of binary and biternary amplitude shift keying.

OBJECTIVE: To familiarize the student with the modulators, demodulators, and performance measurements of Binary and Baternary Amplitude Shift Keying (ASK).

PREREQUISITES: Completion of Lab 1, "Equipment Familiarization".

REQUIRED EQUIPMENT

The following equipment is required to perform this experiment. It is assumed the student is familiar with the controls and functions of each item listed below.

1. Oscilloscope (dual trace)
2. Spectrum Analyzer (0 to 2 MHz minimum)
3. Digital Voltmeter (DVM) (0 to 2 Vdc minimum)
4. True RMS AC Voltmeter (700 kHz minimum bandwidth)
5. Test Leads
6. DEGEM PS-MB-1/A Power Supply Board with Service Unit PU-253 installed
7. DEGEM Rack Expansion Unit
8. DEGEM Boards DIGICOM-2/1
DIGICOM-2/2
DIGICOM-2/3

REFERENCES

1. DEGEM Systems Ltd. Theory and Modern Practice of Digital Communication Course DIGICOM. DEGEM Systems Ltd., 1982.
2. DEGEM Systems Ltd. Amplitude Shift Keying (ASK) Course DIGICOM-2. DEGEM Systems Ltd., 1981.

THEORETICAL BACKGROUND

SOURCE: Reference (1).

Chapter 5 - Amplitude Shift Keying

Additional Background

Measurement of Signal-to-Noise Ratio:

The signal-to-noise ratio (S/N) of a signal is calculated by the following equation:

$$(S/N) = 20 \log_{10} (V_s/V_n) \quad (1)$$

where V_s = RF Signal RMS Voltage

V_n = Noise Signal RMS Voltage

The values of V_s and V_n are measured at the output of a summing network, that adds a noise signal to an RF signal, as follows:

- Measuring V_s : With only an RF signal input (noise input terminal grounded), measure the output RMS voltage of the network using a true RMS voltmeter.
- Measuring V_n : With only a noise signal input (RF input terminal grounded), measure the output RMS voltage of the network using a true RMS voltmeter.

Biternary Coding:

Biternary coding is used to add one bit of memory to a binary sequence. This is done by appropriately filtering the input binary sequence, resulting in a multi-level signal. Figure 1a shows the coded waveform of two consecutive "ones" and figure 1b shows the waveform for four consecutive "ones". The resultant waveforms are generated at the output of the coding filter.

Decoding of a biternary sequence is accomplished by using two comparators set at different thresholds and a J-K flip-flop. Figure 2 shows this decoder and figure 3 illustrates typical waveforms for the system.

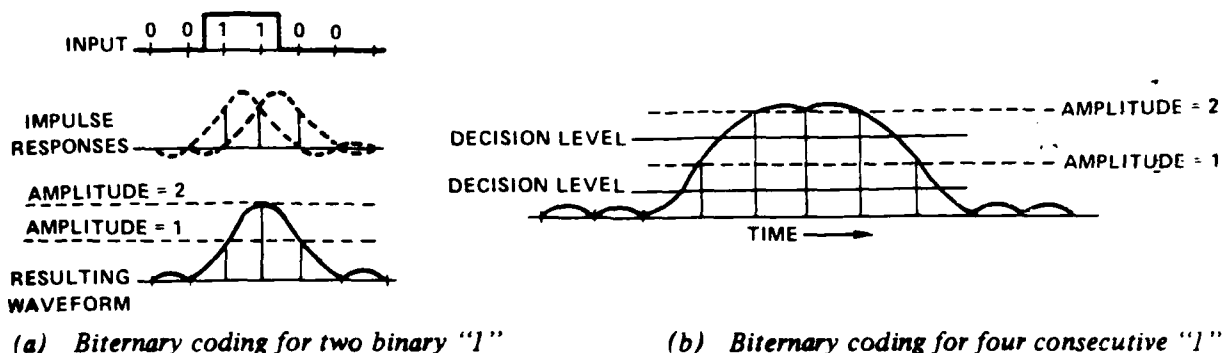


Figure 1. Examples of Biternary Coding. (1:109)

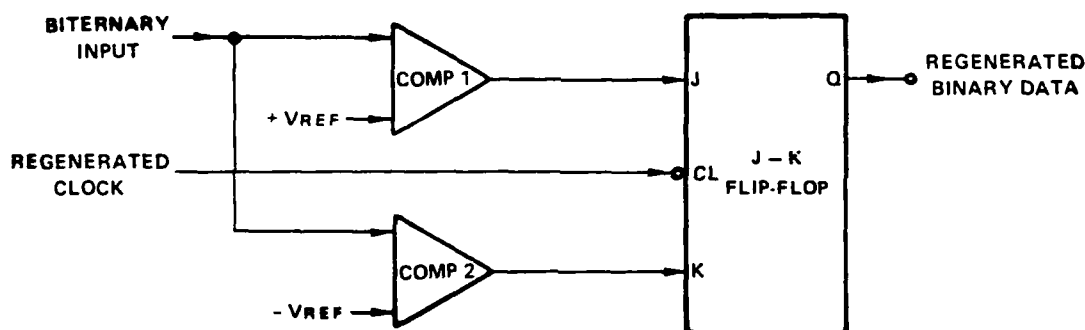


Figure 2. Biternary Decoder. (1:109)

The decoding rule is as follows:

- If the sampled amplitude is below the lower threshold, a "zero" is decoded.
- If the sampled amplitude is above the upper threshold, a "one" is decoded.
- If the sampled amplitude falls between the upper and lower thresholds, the inverse of the preceding bit is decoded.

The biternary system requires a 2.1 dB better signal-to-noise ratio to achieve the same bit error performance as an ideal binary ASK system.

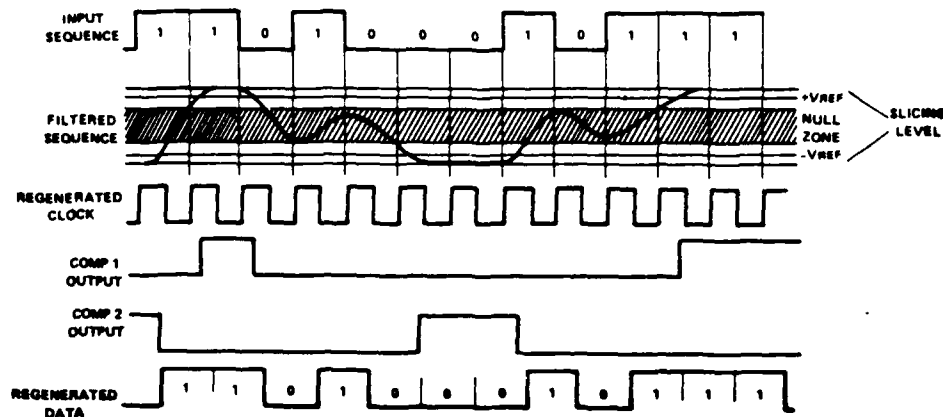


Figure 3. Typical Waveforms for the Biternary System. (1:109)

DEGEM CIRCUIT BOARD DESCRIPTION

SOURCE: Reference (2).

Appendix - Pages 45-47 - Functional Description of Service Unit For DIGICOM - Model PU-253

EXPERIMENT PROCEDURE

General Instructions

WARNING

Turn the DEGEM Power Supply Board off before removing or inserting any plug-in boards. Damage to circuit components may result if the boards are changed while the power is on.

1. DO NOT turn the DEGEM PS-MB-1/A Power Supply Board on. This power supply board should contain the Service Unit PU-253. Attach the Rack Extension Unit to the power supply board in the horizontal position by connecting the power sockets firmly.

2. To ensure minimum noise and signal crosstalk, connect the following wires between the power supplies on the front panel of the power supply board.
 - Power Supply A (-) to Power Supply B (+)
 - Power Supply B (+) to Power Supply F (COMMON)
 - Power Supply F (COMMON) to Chassis Ground
3. Install the DIGICOM-2/1, 2/2, and 2/3 boards into the Rack Expansion Unit by pressing each board into a power socket and tightening the hold-down screws on each end of the board.
4. Turn the power supply board on. All plug-in units are internally powered and need no external power connections.
5. Turn all of the remaining equipment on.

ASK Modulator

Objective: To examine the ASK modulator and properties of the ASK signal.

1. Set the Data Generator rate at 16 kbps on the PU-253 with a sequence length of 15. Connect DATA OUT to SIGNAL IN of the modulator on DIGICOM-2/1, and connect the 512 kHz sine wave carrier signal on PU-253 to the CARRIER IN.
2. Connect a dual trace oscilloscope to SIGNAL IN and ASK OUT of the ASK modulator. Trigger the oscilloscope externally from the SYNC OUT signal of the Data Generator on PU-253.
3. Adjust the % MOD control on the modulator board to obtain a 100% modulated signal. Note that the output signal is a pulsed waveform with the pulses corresponding to "ones" of the data stream. If the pulses correspond to "zeros", turn the % MOD control cw until the signal pulses correspond to the "ones".
4. Connect the spectrum analyzer to the output of the modulator and observe the spectrum at 512 kHz. This is the spectrum of a pseudo-random pulsed signal.

5. Vary the data rate of the Data Generator and notice the change in the frequency domain trace of the pulsed signal.
6. Change the sequence length to 255 and observe the frequency domain trace.
7. Change the data rate and sequence length back to 16 kbps and 15 respectively.

ASK System

Objective: To calibrate the receiver for optimal performance.

1. Assemble the ASK system shown in figure 4. Do not connect the dashed lines shown in the figure.
2. Receiver Calibration:
 - a. Turn the Noise Generator on PU-253 off and turn the CARRIER+NOISE AMP control of the Summing Network fully ccw.
 - b. Connect the True RMS Voltmeter to the output of the Summing Network and set the output amplitude to 50 mVrms by adjusting the SIGNAL AMP control.
 - c. Set the IF Bandwidth to NARROW.
 - d. Disconnect both oscilloscope probes from the circuit. Set both channels for 200 mV/DIV and align both traces vertically so they coincide.
 - e. Connect channel one (dc coupled) of the oscilloscope to the output of the envelope detector on DIGICOM-2/3 and channel two (dc coupled) to V ref. 3 of the NRZ Regenerator. Externally trigger the oscilloscope from the 16 kHz clock signal of the Clock and Carrier Generator on PU-253.

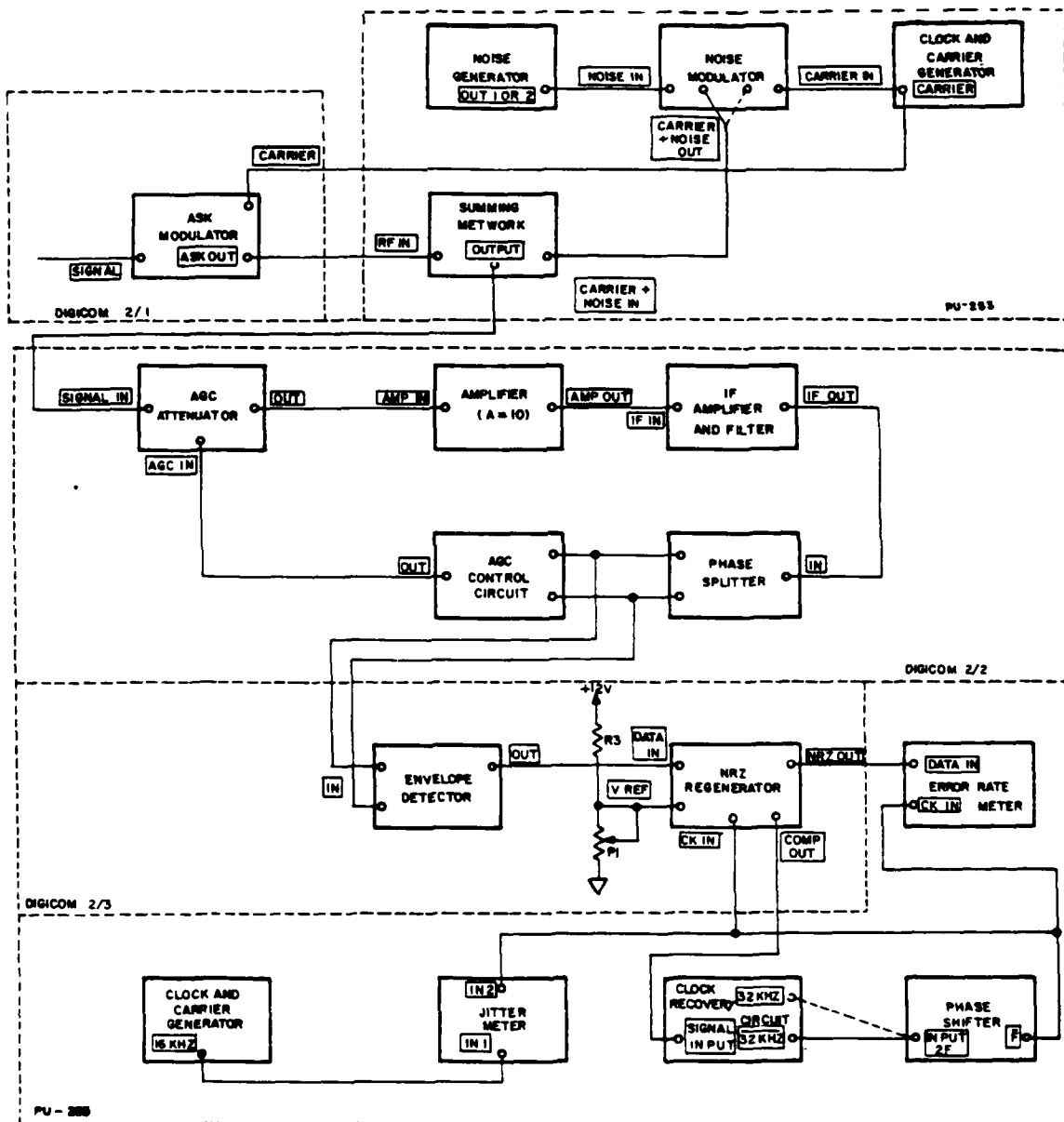


Figure 4. ASK System. (2:26)

- f. Display the eye diagram (channel one signal) as shown in figure 5. Set the decision threshold (channel two signal) to the maximum horizontal opening, by adjusting P_1 on DIGICOM-2/3, as shown in the figure.

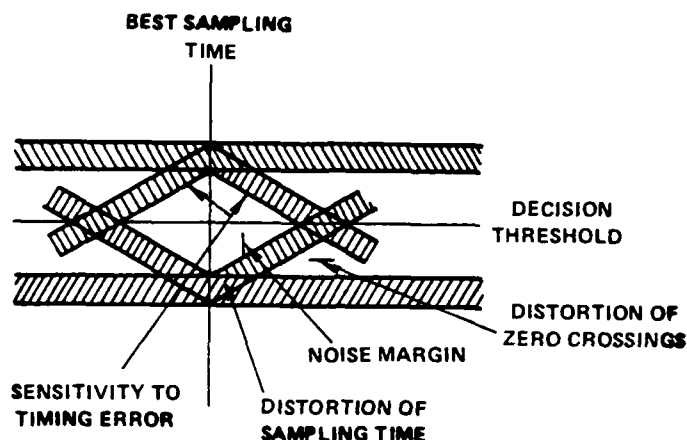


Figure 5. Binary Eye Diagram. (1:105)

- g. Connect channel two of the oscilloscope to CK IN of the NRZ Regenerator. Make certain the Clock Recovery Circuit on PU-253 is in sync with the data signal. If it is not, press RESET several times until sync is achieved.
- h. Observe the eye diagram on channel one and the CK IN signal on channel two. Adjust the PHASE SHIFTER control on PU-253 until the rising edge of the CK IN signal is set at the maximum vertical opening of the eye diagram as shown in figure 5. This sets the optimal sampling point of the receiver.
- i. Set the Error Rate Meter in the 10^{-4} NORMAL mode on the PU-253. Make sure that there are no errors indicated. If there are, readjust the decision threshold and the sampling point as described above.
- j. Connect channel one of the oscilloscope to DATA OUT of the Data Generator and channel two to OUT of the NRZ Regenerator. Trigger the oscilloscope external-

ly from SYNC OUT of the Data Generator. Make sure that the input and output data sequences are the same. There may be a one bit shift between the two sequences.

Performance of Binary ASK in White Noise

Objective: To measure the bit error rate versus input signal-to-noise ratio of the binary ASK system in bandlimited white noise.

1. Set the IF BANDWIDTH to WIDE.
2. Connect the True RMS Voltmeter to the output of the Noise Generator on PU-253 and turn the Noise Generator on. Set the output noise signal to 150 mVrms by adjusting the Noise Amplitude control.
3. Connect the True RMS Voltmeter to the output of the Summing Network. Disconnect RF IN from ASK OUT and ground the RF IN terminal. Set the Carrier+Noise signal to 10 mVrms by adjusting the CARRIER+NOISE AMP control. Reconnect the RF IN terminal to ASK OUT. The output of the Summing Network now has a 50 mVrms to 10 mVrms signal-to-noise ratio, or 14 dB using equation (1) of the theoretical background section.
4. Make certain the Clock Recovery Circuit is in sync with the data signal.
5. Use the Bit Error Meter on PU-253 in the 10^{-4} mode where the number of the errors shown on the meter reflects an error rate of that number times 10^{-4} .
6. Average at least ten error samples and record the bit error rate for a S/N ratio of 14 dB on the data sheet in the Binary column.
7. Decrease the S/N ratio by increasing the RMS amplitude of the NOISE+CARRIER in steps according to the data sheet. Use the same procedure as described in step 3 above. For each S/N ratio, measure and record the average bit error rate for at least ten samples.
8. Plot the Bit Error Rate versus S/N ratio on the provided semi-log paper. Label this curve as Binary ASK.

Partial Response ASK System

Objective: To examine and calibrate the biternary, partial response receiver.

1. Test Circuit Setup:

- a. Modify the test circuit as shown in figure 6. Do not connect the dashed lines shown in the figure. In this test circuit, the Biternary Regenerator is used instead of the NRZ Regenerator. A biternary filter is also added to the input of the ASK Modulator.
- b. Connect the 32 kHz clock to the Jitter Meter instead of the 16 kHz clock.
- c. Change the input signal to 32 kbps with a sequence length of 15.

2. Biternary Signal:

- a. Connect the dual trace oscilloscope to the input and output of the biternary filter in front of the ASK Modulator. Trigger the oscilloscope externally from the SYNC OUT of the Data Generator. Observe both waveforms.
- b. Compare the output waveform of the envelope detector to the analog waveform that was shown in figure 3. The waveforms are not identical since the data sequences are different. But notice on the oscilloscope that the coding of two or more consecutive "ones" has a higher amplitude than the coding of a single "one" preceded by a "zero". There may be a one to two bit delay in the output waveform.
- c. Change the input data rate and observe the different output waveforms. Notice that the best data rate for the biternary signal is 32 kbps since there are three distinct decision regions for this data rate. Return the data rate to 32 kbps.

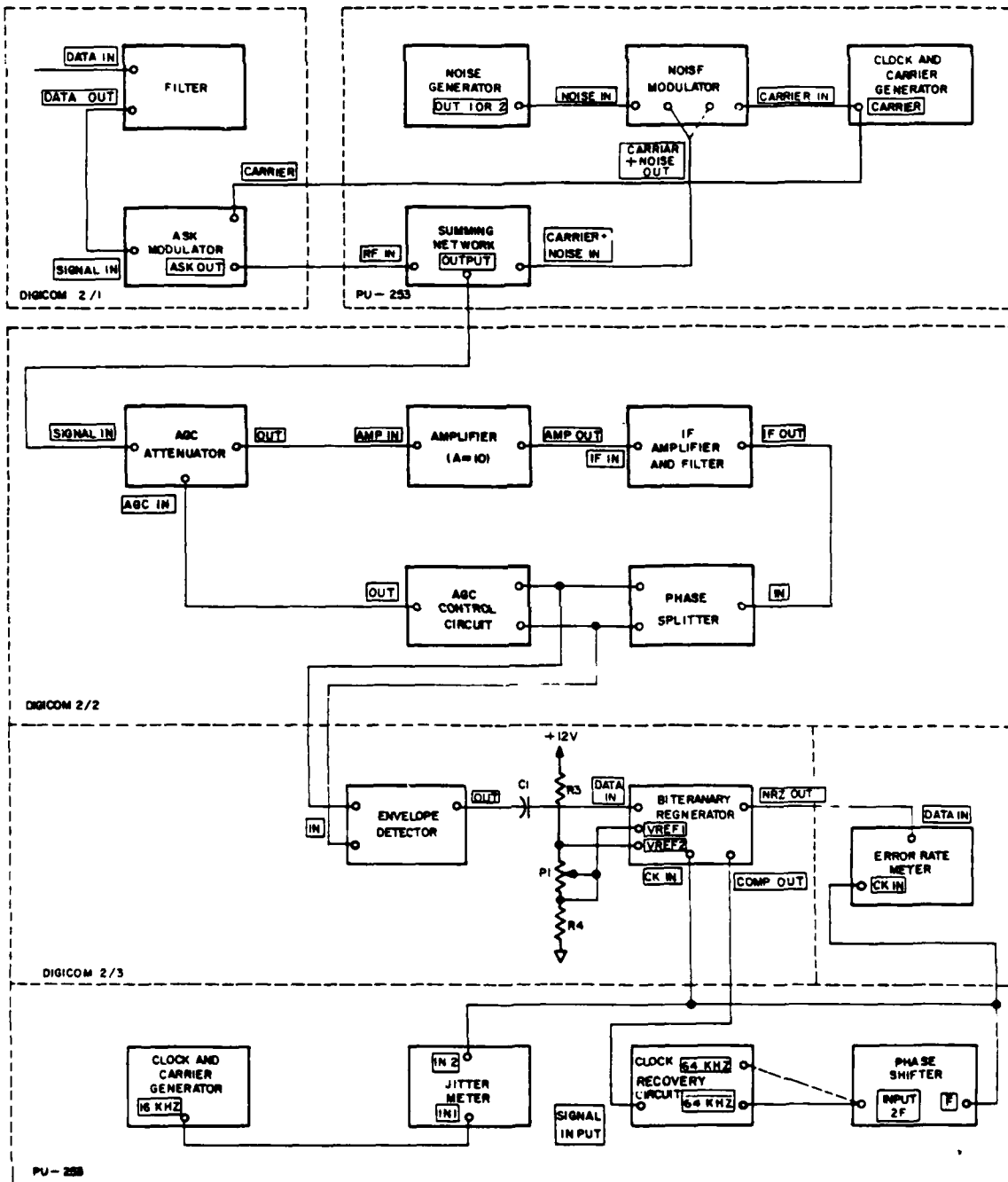


Figure 6. Biternary ASK System. (2:38)

3. Receiver Calibration:

- a. Turn off the Noise Generator.
- b. Connect channel one of the oscilloscope to the envelope detector output on DIGICOM-2/3. Set the channel for ac coupled and 200 mV/DIV. Trigger the oscilloscope externally from the 32 kHz clock signal and obtain the biternary eye diagram as shown in figure 7.

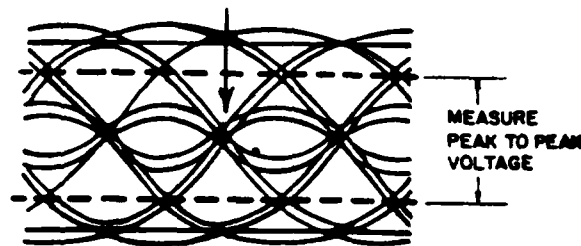


Figure 7. Biternary Eye Diagram. (2:34)

- c. Measure the peak-to-peak voltage on the oscilloscope between the threshold levels as shown in figure 7.
- d. Connect a DVM between V ref. 1 and V ref. 2 on the Biternary Regenerator. Set the voltage difference between these two points to the voltage measured above.
- e. Connect channel two to CK IN of the Biternary Regenerator and make sure that the Clock Recovery Circuit is locked.
- f. Adjust the rising edge of the CK IN signal to the point indicated by the arrow in figure 7 by adjusting the Phase Shifter Control on PU-253.
- g. Make sure there are no errors indicated on the Error Rate Meter.
- h. Connect the oscilloscope to the input and output data signals of the ASK system. Trigger the oscilloscope externally from SYNC OUT of the Data Generator. Observe both waveforms and confirm that they are identical except for a shift of about two bits.

Performance of Biternary ASK in White Noise

Objectives: To measure the bit error rate versus input signal-to-noise ratio of the biternary ASK system in bandlimited white noise.

1. Repeat the same error rate procedure as was outlined in the performance section for the binary system. Make certain the RF signal (without noise) is set to 50 mVrms.
2. Plot the bit error performance data on the same graph used for the binary system data. Label this curve as Biternary ASK. Notice the difference in performance between the two systems.

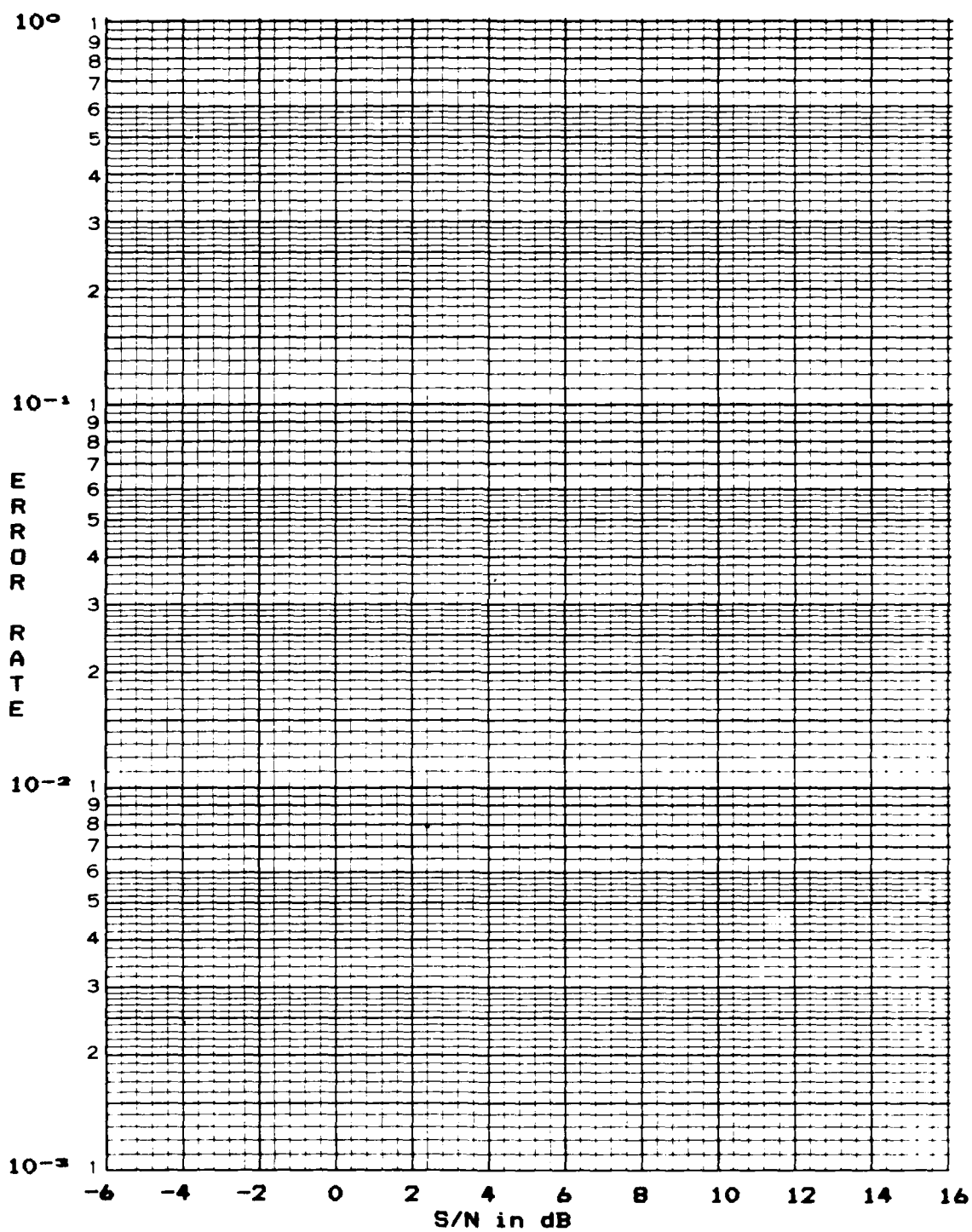
STUDENT NAMES _____ DATE PERFORMED _____

Note: Indicate unit of measurement with each data entry.

PERFORMANCE:

Signal Amplitude = 50 mVrms

NOISE AMPLITUDE (mVrms)	S/N (voltage ratio)	S/N (dB)	BIT ERROR RATE BINARY	RATE BITERNARY
10	5.00	13.98	_____	_____
15	3.33	10.46	_____	_____
20	2.50	7.96	_____	_____
25	2.00	6.02	_____	_____
30	1.67	4.44	_____	_____
35	1.43	3.10	_____	_____
40	1.25	1.94	_____	_____
45	1.11	0.92	_____	_____
50	1.00	0.00	_____	_____
55	0.91	-0.83	_____	_____
60	0.83	-1.58	_____	_____



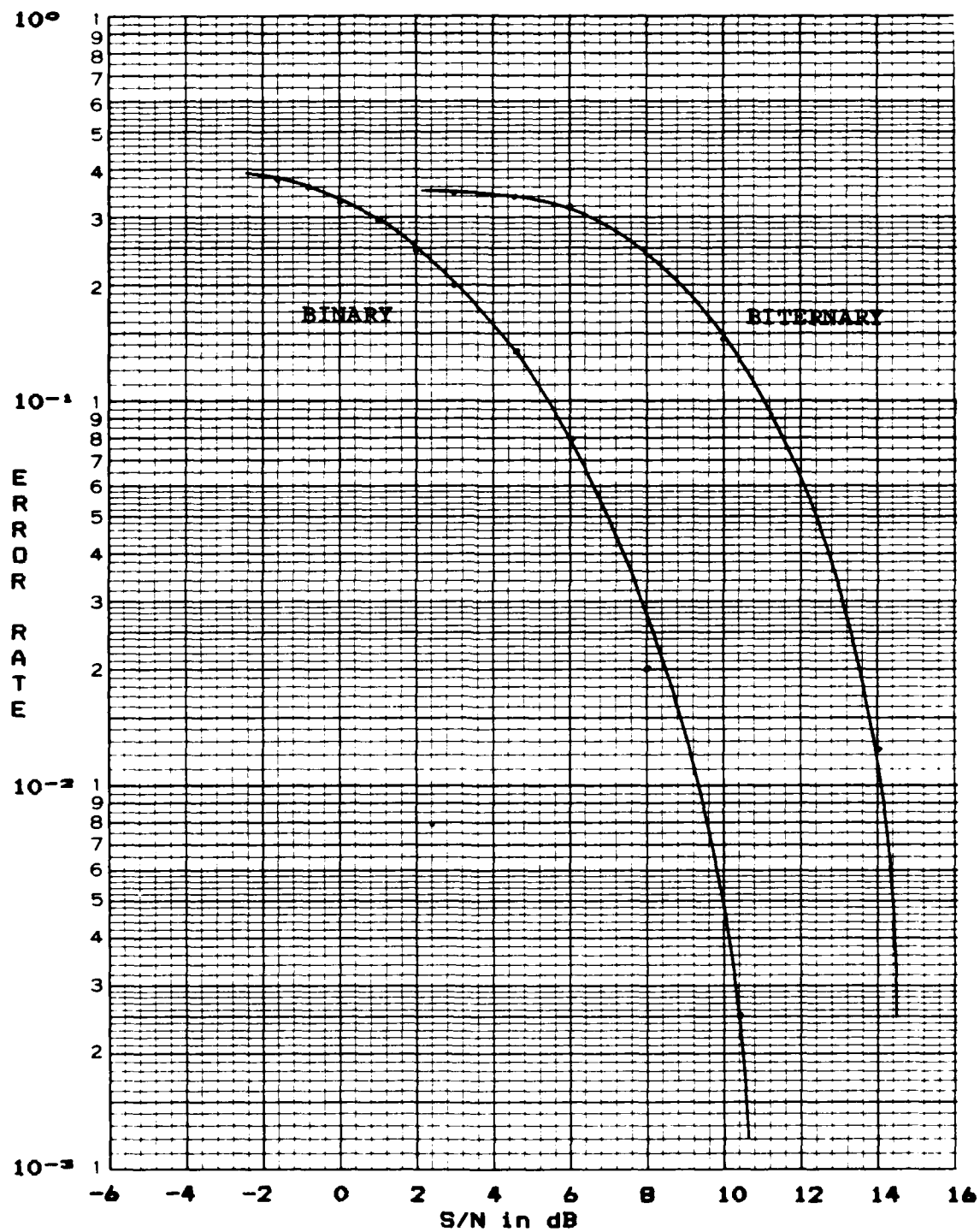
STUDENT NAMES _____ SAMPLE _____ DATE PERFORMED _____

Note: Indicate unit of measurement with each data entry.

PERFORMANCE:

Signal Amplitude = 50 mVrms

NOISE AMPLITUDE (mVrms)	S/N (voltage ratio)	S/N (dB)	BIT ERROR RATE	
			BINARY (10^{-3})	BITERNARY (10^{-3})
10	5.00	13.98	0.00	12.2
15	3.33	10.46	2.47	246
20	2.50	7.96	20.3	314
25	2.00	6.02	77.6	337
30	1.67	4.44	135	347
35	1.43	3.10	195	No Lock
40	1.25	1.94	245	
45	1.11	0.92	292	
50	1.00	0.00	324	
55	0.91	-0.83	357	
60	0.83	-1.58	382	



APPENDIX N

Laboratory Experiment Number 11

Phase Shift Keying

This experiment investigates the performance characteristics (bit error rate versus input signal-to-noise ratio) of binary and differential phase shift keying and carrier recovery in noise.

OBJECTIVE: To familiarize the student with the modulators, demodulators, and performance measurements of Binary and Binary Differential Phase Shift Keying (PSK).

PREREQUISITES: Completion of Lab 1, "Equipment Familiarization".

REQUIRED EQUIPMENT

The following equipment is required to perform this experiment. It is assumed the student is familiar with the controls and functions of each item listed below.

1. Oscilloscope (dual trace)
2. Spectrum Analyzer (0 to 2 MHz minimum)
3. True RMS AC Voltmeter (700 kHz minimum bandwidth)
4. Test Leads
5. DEGEM PS-MB-1/A Power Supply Board with Service Unit PU-253 installed
6. DEGEM Rack Expansion Unit
7. DEGEM Boards DIGICOM-3/1
DIGICOM-3/2
DIGICOM-3/3

REFERENCES

1. DEGEM Systems Ltd. Theory and Modern Practice of Digital Communication Course DIGICOM. DEGEM Systems Ltd., 1982.
2. DEGEM Systems Ltd. Phase Shift Keying (PSK) Course DIGICOM-3. DEGEM Systems Ltd., 1981.

THEORETICAL BACKGROUND

SOURCE: Reference (1).

Chapter 6 - Phase Shift Keying

Additional Background

Measurement of Signal-to-Noise Ratio:

The signal-to-noise ratio (S/N) of a signal is calculated by the following equation.

$$(S/N) = 20 \log_{10} (V_s/V_N) \quad (1)$$

where V_s = RF Signal RMS Voltage

V_N = Noise Signal RMS Voltage

The values of V_s and V_N are measured at the output of a summing network, that adds a noise signal to an RF signal, as follows:

- Measuring V_s : With only an RF signal input (noise input terminal grounded), measure the output RMS voltage of the network using a true RMS voltmeter.
- Measuring V_N : With only a noise signal input (RF input terminal grounded), measure the output RMS voltage of the network using a true RMS voltmeter.

DEGEM CIRCUIT BOARD DESCRIPTION

SOURCE: Reference (2).

Appendix - Pages 55-57 - Functional Description of
Service Unit For DIGICOM - Model PU-253

EXPERIMENT PROCEDURE

General Instructions

WARNING

Turn the DEGEM Power Supply Board off before removing or inserting any plug-in boards. Damage to circuit components may result if the boards are changed while the power is on.

1. DO NOT turn the DEGEM PS-MB-1/A Power Supply Board on. This power supply board should contain the Service Unit PU-253. Attach the Rack Extension Unit to the power

supply board in the horizontal position by connecting the power sockets firmly.

2. To ensure minimum noise and signal crosstalk, connect the following wires between the power supplies on the front panel of the power supply board.
 - Power Supply A (-) to Power Supply B (+)
 - Power Supply B (+) to Power Supply F (COMMON)
 - Power Supply F (COMMON) to Chassis Ground
3. Install the DIGICOM-3/1, 3/2, and 3/3 boards into the Rack Expansion Unit by pressing each board into a power socket and tightening the hold-down screws on each end of the board.
4. Turn the power supply board on. All plug-in units are internally powered and need no external power connections.
5. Turn all of the remaining equipment on.

PSK Modulator

Objective: To examine the PSK modulator and properties of the PSK signal. Also to study the operation of the differential encoder

1. **Operation:**
 - a. Set the Data Generator rate at 16 kbps on the PU-253 with a sequence length of 15. Connect DATA OUT to DATA IN of the PSK Modulator on DIGICOM-3/1.
 - b. Connect the 512 kHz sine wave carrier signal on PU-253 to the input of the Carrier Phase Shifter on DIGICOM-3/1. Connect the Carrier Phase Shifter output to the PSK Modulator CARRIER IN.
 - c. Connect the dual trace oscilloscope to the input and output of the Carrier Phase Shifter. Vary the CARRIER PHASE control and observe the change in carrier phase at the output between zero and 180 degrees.

- d. Connect the dual trace oscilloscope to DATA IN and PSK OUT of the PSK modulator. Trigger the oscilloscope externally from the SYNC OUT signal of the Data Generator on PU-253.
 - e. Vary the MODULATION BALANCE control of the PSK Modulator and observe how the PSK signal changes. Adjust the MODULATION BALANCE control until the PSK signal is balanced (i.e. there is no amplitude change from bit to bit).
 - f. Observe the transition between a "zero" and "one" bit of the PSK signal closely on the oscilloscope to notice the phase transition. Vary the CARRIER PHASE control of the Carrier Phase Shifter and notice that the point at which the phase shift occurs can be changed. Adjust the CARRIER PHASE control so the phase shift changes between the top of the sine wave (+90 degrees) and the bottom of the sine wave (-90 degrees).
 - g. Connect the spectrum analyzer to PSK OUT and observe the spectrum of the PSK signal at 512 kHz. Use the LINEAR mode on the analyzer. Change the input data rate and observe the effect on the PSK signal spectrum.
 - h. Change the sequence length on the Data Generator and observe the effect on the spectrum of the PSK signal.
2. Differential Encoder:
- a. Set the Data Generator for a 16 kbps data rate with sequence length of 15.
 - b. Connect the DATA OUT of the Data Generator to NRZ IN of the DPSK Encoder on Unit DIGICOM-3/1. Connect the 16 kHz clock signal from the Clock and Carrier Generator on PU-253 to the clock input of the DPSK Encoder.
 - c. Connect the dual trace oscilloscope to the 16 kHz clock signal and NRZ IN of the encoder. Trigger the oscilloscope externally from SYNC OUT of the Data Generator. Draw a timing diagram on the data sheet of the input data with reference to the clock signal.

- d. Connect the dual trace oscilloscope to the NRZ IN and output of the encoder. Draw a timing diagram of the output with reference to the input.
- e. Note that whenever the input is a "one", the output of the encoder changes phase (changes the logic level) and for input "zeros", the output phase does not change.

Carrier Recovery for Coherent Detection of Binary PSK Signals

Objective: To examine the performance of the carrier recovery system in the presence of noise.

1. Connect the circuit as shown in figure 1. Connect the Clock and Carrier Generator 512 kHz sine wave carrier to CARRIER IN of the PSK Modulator on DIGICOM-3/1 and also to CARRIER IN of the Noise Modulator on PU-253.

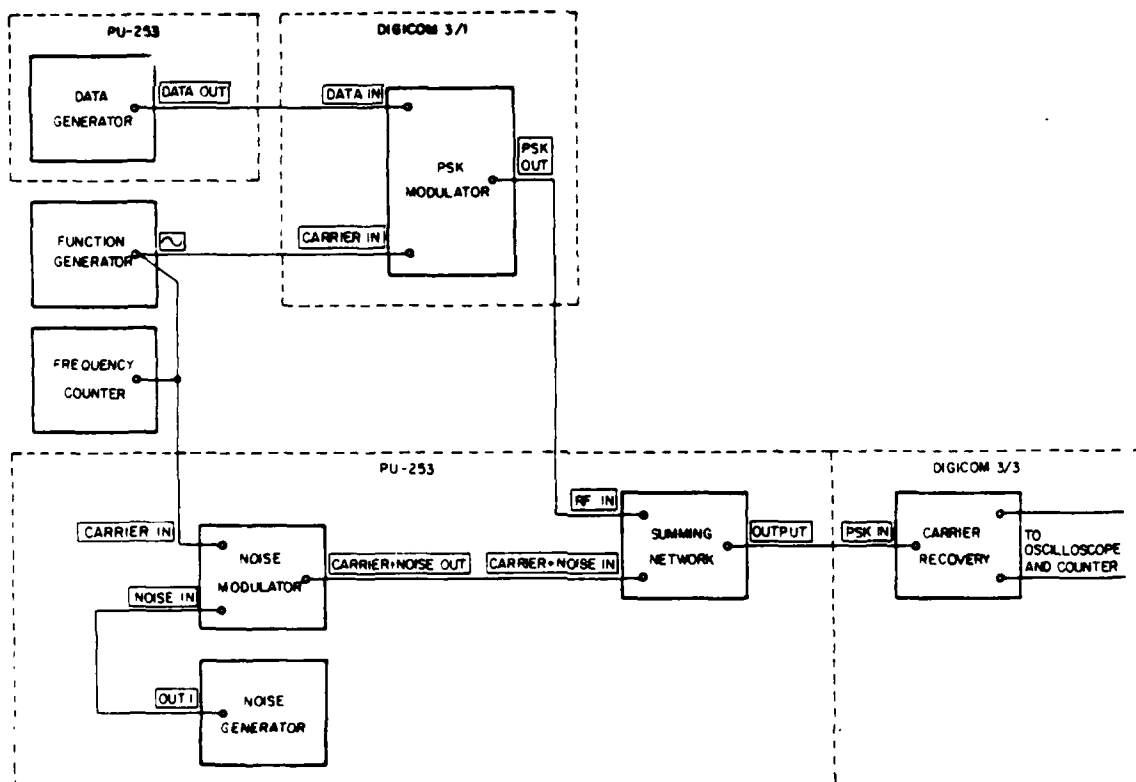


Figure 1. Setup for Carrier Recovery Circuit. (2:20)

2. Select a data rate of 16 kbps and a sequence length of 15 at the Data Generator.
3. Disconnect the CARRIER+NOISE input from the Summing Network and ground this input terminal. Connect the True RMS Voltmeter between ground and the output of the Summing Network. Using the SIGNAL AMP control, adjust the signal to 50 mVrms.
4. Connect the True RMS Voltmeter to the OUT 1 of the Noise Generator and adjust the output to 150 mVrms.
5. Reconnect the CARRIER+NOISE OUT of the Noise Modulator to the CARRIER+NOISE IN of the Summing Network. Turn the CARRIER+ NOISE AMP control fully ccw.
6. Connect the dual trace oscilloscope to the CARRIER IN of the PSK Modulator and to the top output of the Carrier Recovery Circuit on DIGICOM-3/3. Observe both waveforms, trigger from the Carrier Recovery Circuit output.
7. Adjust the Carrier Recovery Circuit PHASE SHIFTER control so that the zero crossings of the carrier sine wave and recovered square wave coincide.
8. Disconnect and reconnect the input signal of the Carrier Recovery Circuit at least 20 times, in each case noting whether the output square wave is in or out of phase with the carrier sine wave. Calculate and record the percentage of the time that the output is in phase with the carrier.
9. Slowly increase the CARRIER+NOISE AMP control while watching the oscilloscope. Notice that as the noise level increases, the phase of the output waveform starts to change with relation to the carrier until the recovery circuit fails to lock.
10. Adjust the noise level to the point where the circuit just starts to loose lock (i.e. when output phase changes start to occur).
11. Connect the True RMS Voltmeter to the output of the Summing Network. Disconnect RF IN from PSK OUT of the modulator and ground RF IN. Measure the amplitude of the CARRIER+NOISE on the voltmeter.

12. Use equation (1) in the theoretical background section to calculate the S/N ratio in decibels. (Note: The RF signal is 50 mVrms without noise). Record the S/N ratio on the data sheet. This is the minimum S/N ratio required to recover the carrier.

PSK SYSTEM

Objective: To calibrate the receiver for optimal performance.

1. Construct the PSK system as shown in figure 2. Do not connect the dashed lines in the figure.

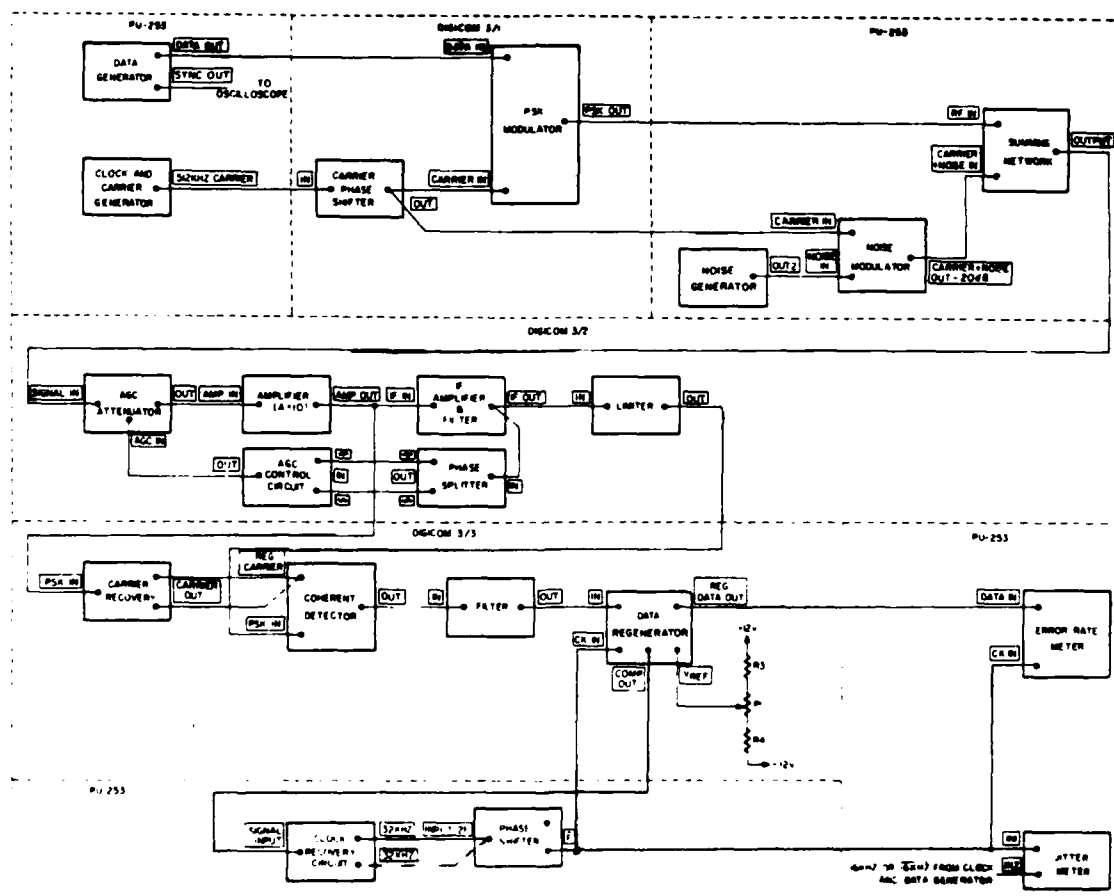


Figure 2. PSK System. (2:42)

2. Since the Carrier Recovery Circuit loses lock quickly with added noise, the system will be analyzed assuming perfect carrier recovery. Therefore, instead of connecting the input of the Carrier Recovery Circuit to the output of the amplifier, as shown in figure 2, connect its input to the CARRIER IN of the PSK Modulator.
3. Receiver Calibration:
 - a. Turn the Noise Generator on PU-253 off and turn CARRIER+ NOISE AMP of the Summing Network fully ccw.
 - b. Connect the True RMS Voltmeter to the output of the Summing Network and set the output amplitude to 50 mVrms by adjusting the SIGNAL AMP control.
 - c. Set the IF Bandwidth to WIDE. Connect the dual trace oscilloscope to the CARRIER IN of the modulator and to the top output of the Carrier Recovery Circuit on DIGICOM-3/3.
 - d. Adjust the PHASE SHIFTER control on DIGICOM-3/3 until the recovered carrier square wave is exactly 180 degrees out of phase with the modulator carrier. If the signals are in phase, disconnect and reconnect the Carrier Recovery Circuit input signal several times until the signals are 180 degrees out of phase.
 - e. Disconnect both oscilloscope probes from the circuit. Set both channels for 1 V/DIV and align both traces vertically so they coincide.
 - f. Connect channel one (ac coupled) of the oscilloscope to the output of the filter on DIGICOM-3/3 and channel two (dc coupled) to V ref. of the Data Regenerator. Externally trigger the oscilloscope from the 16 kHz clock signal of the Clock and Carrier Generator on PU-253.
 - g. Display the eye diagram (channel one signal) as shown in figure 3. Set the decision threshold (channel two signal) to the maximum horizontal opening, by adjusting P₁ on DIGICOM-3/3, as shown in the figure.

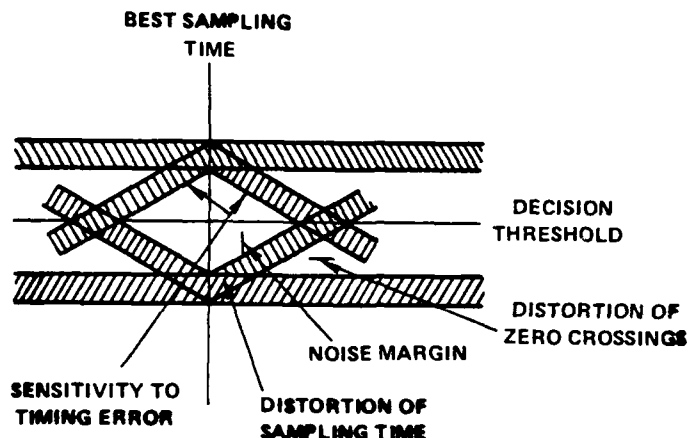


Figure 3. Binary Eye Diagram. (1:105)

- h. Connect channel two of the oscilloscope to CK IN of the Data Regenerator. Make certain the Clock Recovery Circuit on PU-253 is in sync with the data signal. If it is not, press RESET several times until sync is achieved.
- i. Observe the eye diagram on channel one and the CK IN signal on channel two. Adjust the PHASE SHIFTER control on PU-253 until the rising edge of the CK IN signal is set at the maximum vertical opening of the eye diagram as shown in figure 3. This sets the optimal sampling point of the receiver.
- j. Connect channel one of the oscilloscope to DATA OUT of the Data Generator and channel two to OUT of the NRZ Regenerator. Trigger the oscilloscope externally from SYNC OUT of the Data Generator. Make sure that the input and output data sequences are the same. There may be a two bit shift between the two sequences. If the sequences are inverted, disconnect and reconnect the Carrier Recovery Circuit input several times until the sequences are not inverted.
- i. Set the Error Rate Meter in the 10^{-4} NORMAL mode on the PU-253. Make sure that there are no errors indicated. If there are, readjust the decision threshold and the sampling point as described above.

Performance of Coherent Binary PSK in White Noise

Objective: To measure the bit error rate versus input signal-to-noise ratio of the binary PSK system in bandlimited white noise.

1. Connect the True RMS Voltmeter to the output of the Summing Network. Disconnect RF IN from PSK OUT and ground the RF IN terminal. Set the Carrier+Noise signal to 10 mVrms by adjusting the CARRIER+NOISE AMP control. Reconnect the RF IN terminal to PSK OUT. The output of the Summing Network now has a 50 mVrms to 10 mVrms signal-to-noise ratio, or 14 dB using equation (1) of the theoretical background section.
2. Make certain the Clock Recovery Circuit is in sync with the data signal.
3. Use the Bit Error Meter on PU-253 in the 10^{-4} mode where the number of the errors shown on the meter reflects an error rate of that number times 10^{-4} .
4. Average at least ten error samples and record the bit error rate for a S/N ratio of 14 dB on the data sheet in the Binary column.
5. Decrease the S/N ratio by increasing the RMS amplitude of the NOISE+CARRIER in steps according to the data sheet. Use the same procedure as described in step 2 above. For each S/N ratio, measure and record the average bit error rate for at least ten samples.
6. Plot the Bit Error Rate versus S/N ratio on the provided semi-log paper. Label this curve as Binary PSK.

Binary Differential PSK System

Objective: To construct the binary differential PSK system.

1. Construct the circuit shown in figure 5 but do not connect the dashed lines shown in the figure.
2. As before, make a direct connection between the PSK modulator CARRIER IN and the input of the Carrier Recovery Circuit. Also connect F (inverted) to CK IN of the Differential Decoder instead of the F signal.

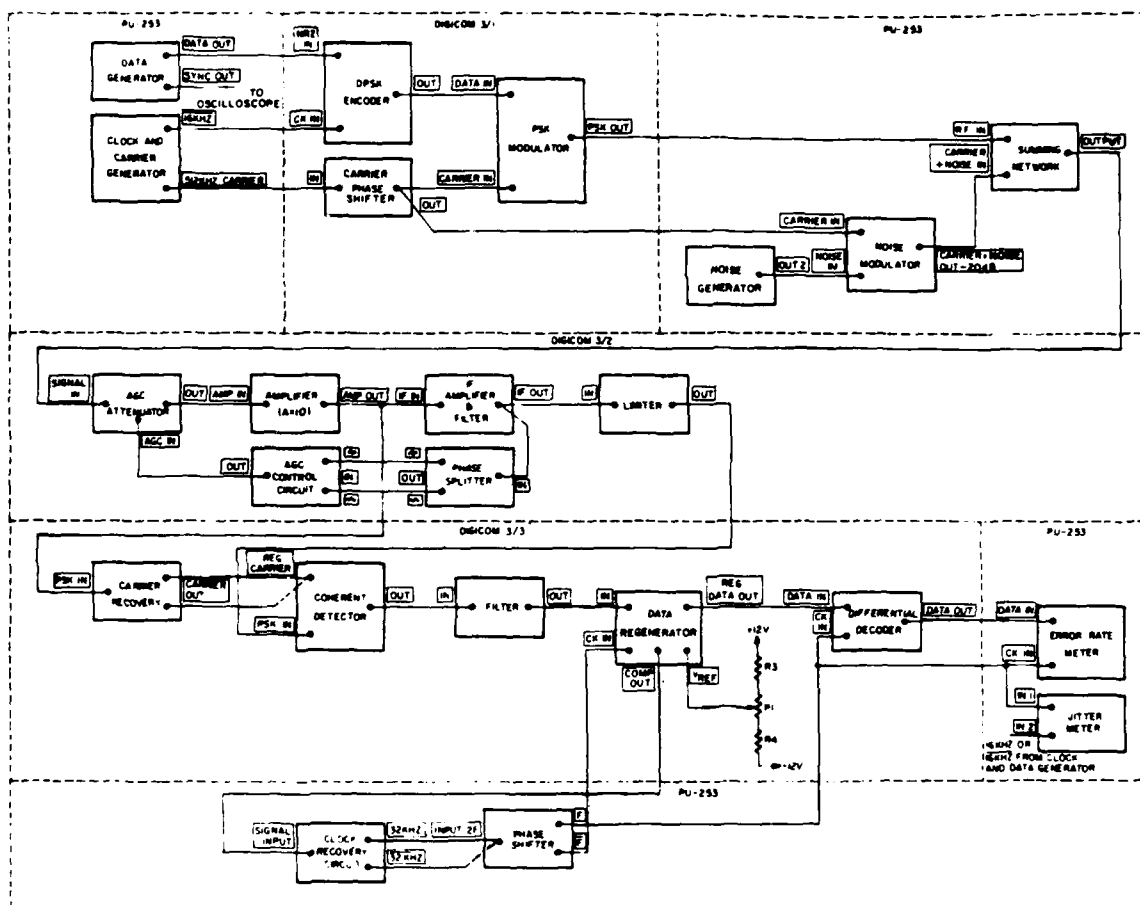


Figure 4. DPSK System. (2:50)

Performance of Binary DPSK in White Gaussian Noise

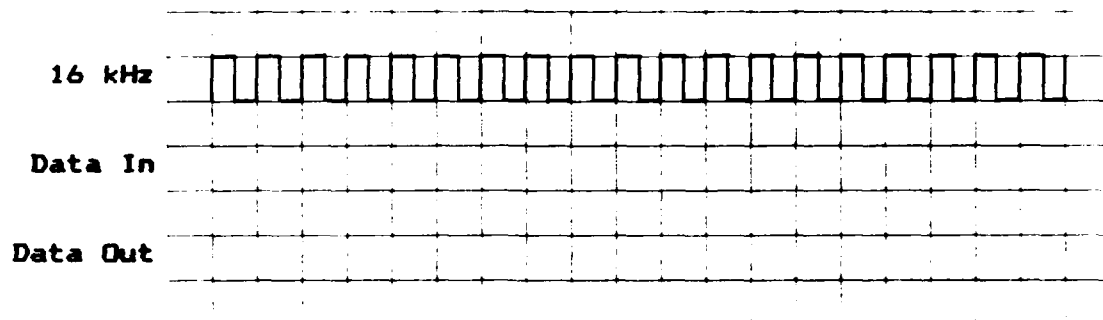
Objective: To measure the bit error rate versus input signal-to-noise ratio of the binary DPSK system in bandlimited white noise.

1. Repeat the same error rate procedure as was outlined in the performance section for the binary system.
2. Plot the bit error performance data on the same graph used for the binary system data. Label this curve as DPSK. Notice the difference in performance between the two systems.

STUDENT NAMES _____ DATE PERFORMED _____

Note: Indicate unit of measurement with each data entry.

DPSK ENCODER:



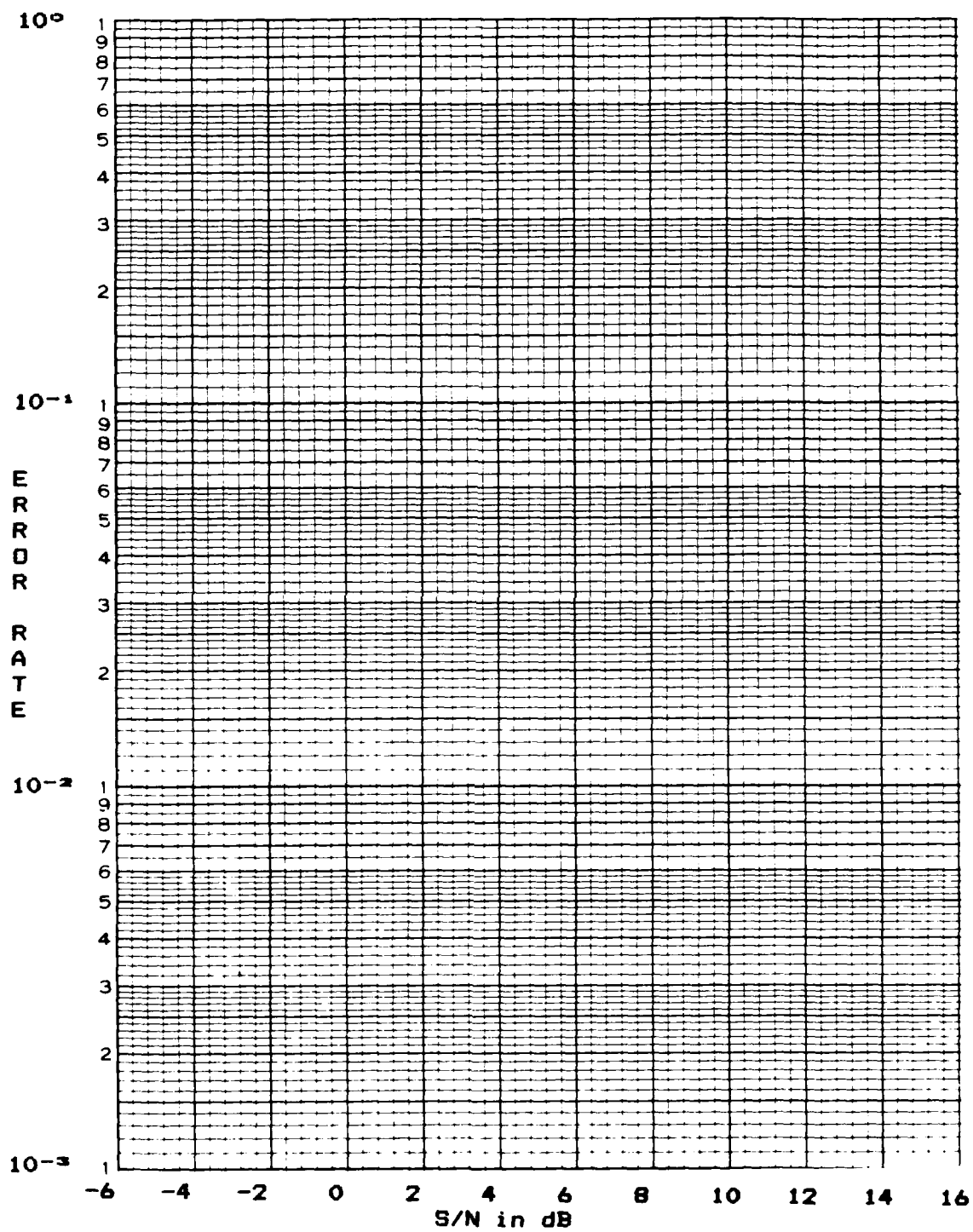
CARRIER RECOVERY CIRCUIT:

Percentage In Phase _____ Minimum S/N Ratio _____

PERFORMANCE:

Signal Amplitude = 50 mVrms

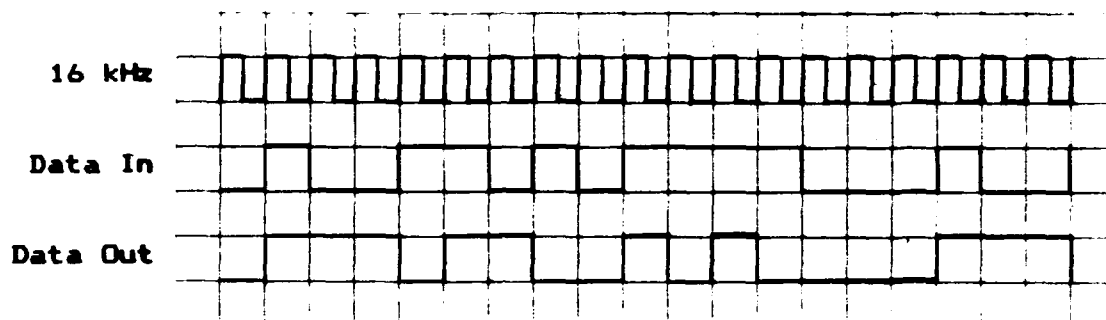
NOISE AMPLITUDE (mVrms)	S/N (voltage ratio)	S/N (dB)	BIT ERROR RATE	
			BINARY	DPSK
10	5.00	13.98	-----	-----
15	3.33	10.46	-----	-----
20	2.50	7.96	-----	-----
25	2.00	6.02	-----	-----
30	1.67	4.44	-----	-----
35	1.43	3.10	-----	-----
40	1.25	1.94	-----	-----
45	1.11	0.92	-----	-----
50	1.00	0.00	-----	-----
60	0.83	-1.58	-----	-----
70	0.72	-2.92	-----	-----
80	0.63	-4.08	-----	-----
90	0.55	-5.10	-----	-----
100	0.50	-6.02	-----	-----



STUDENT NAMES _____ SAMPLE _____ DATE PERFORMED _____

Note: Indicate unit of measurement with each data entry.

DPSK ENCODER:



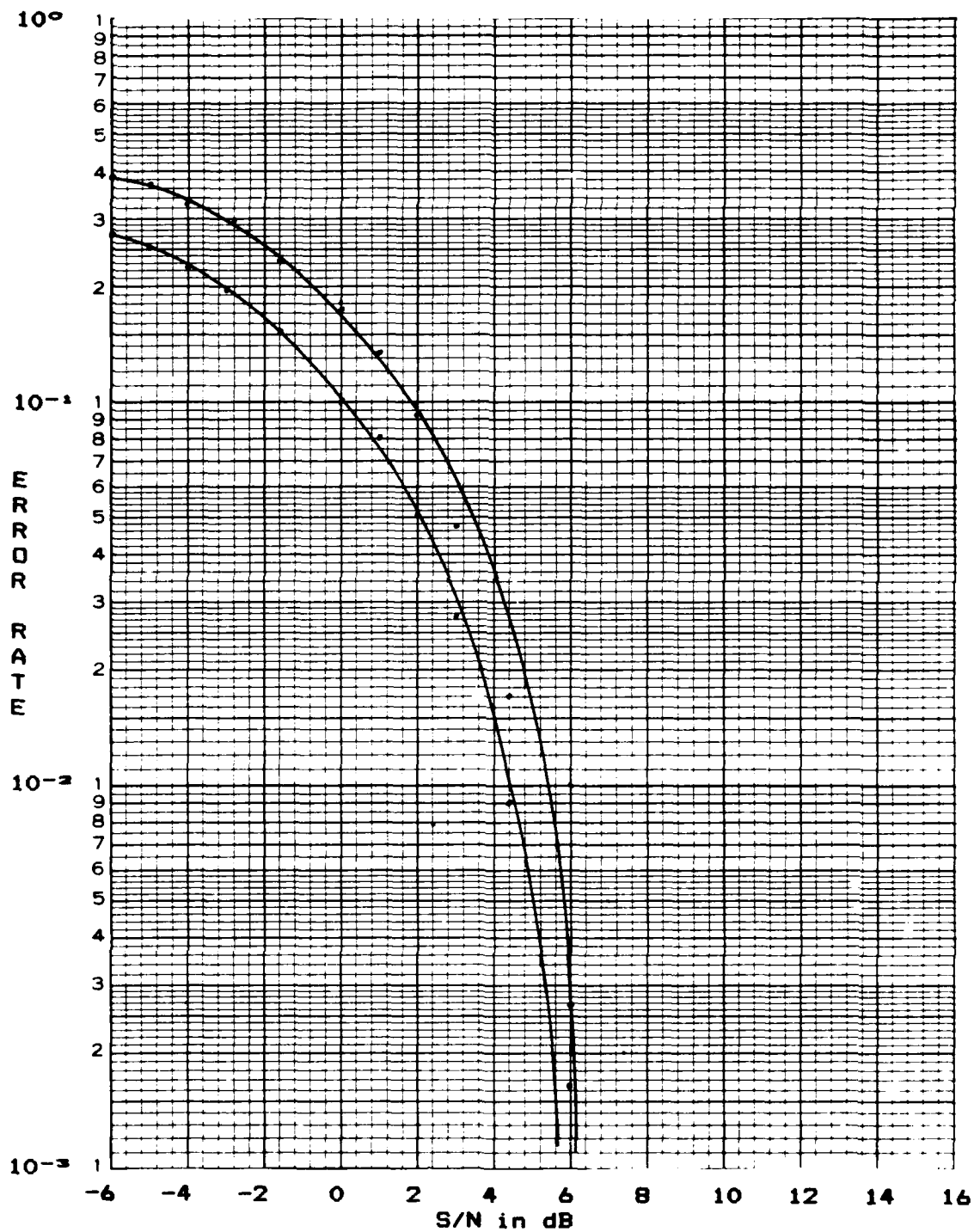
CARRIER RECOVERY CIRCUIT:

Percentage In Phase 50% Minimum S/N Ratio 16.14 dB

PERFORMANCE:

Signal Amplitude = 50 mVrms

NOISE AMPLITUDE (mVrms)	S/N (voltage ratio)	S/N (dB)	BIT ERROR RATE	
			BINARY (10^{-3})	DPSK (10^{-3})
10	5.00	13.98	0.00	0.00
15	3.33	10.46	0.00	0.00
20	2.50	7.96	0.20	0.30
25	2.00	6.02	1.62	2.66
30	1.67	4.44	9.05	16.8
35	1.43	3.10	27.8	48.6
40	1.25	1.94	51.0	93.9
45	1.11	0.92	81.1	134
50	1.00	0.00	103	177
60	0.83	-1.58	152	245
70	0.72	-2.92	190	297
80	0.63	-4.08	225	333
90	0.55	-5.10	252	363
100	0.50	-6.02	276	384



APPENDIX O

Laboratory Experiment Number 12

Frequency Shift Keying

This experiment investigates the performance characteristics (bit error rate versus input signal-to-noise ratio) of binary and biternary frequency shift keying.

OBJECTIVE: To familiarize the student with the modulators, demodulators, and performance measurements of Binary and Baternary Frequency Shift Keying (FSK).

PREREQUISITES: Completion of Lab 1, "Equipment Familiarization".

REQUIRED EQUIPMENT

The following equipment is required to perform this experiment. It is assumed the student is familiar with the controls and functions of each item listed below.

1. Oscilloscope (dual trace)
2. Spectrum Analyzer (0 to 2 MHz minimum)
3. Frequency Counter (0 to 2 MHz minimum)
4. Digital Voltmeter (DVM) (0 to 2 Vdc minimum)
5. True RMS AC Voltmeter (700 kHz minimum bandwidth)
6. Test Leads
7. DEGEM PS-MB-1/A Power Supply Board with Service Unit PU-253 installed
8. DEGEM Rack Expansion Unit
9. DEGEM Boards DIGICOM-4/1
DIGICOM-4/2
DIGICOM-4/3

REFERENCES

1. DEGEM Systems Ltd. Theory and Modern Practice of Digital Communication Course DIGICOM. DEGEM Systems Ltd., 1982.
2. DEGEM Systems Ltd. Frequency Shift Keying (FSK) Course DIGICOM-4. DEGEM Systems Ltd., 1981.
3. DEGEM Systems Ltd. Amplitude Shift Keying (ASK) Course DIGICOM-2. DEGEM Systems Ltd., 1981.

THEORETICAL BACKGROUND

SOURCE: Reference (1).

Chapter 7 - Frequency Shift Keying

Additional Background

Measurement of Signal-to-Noise Ratio:

The signal-to-noise ratio (S/N) of a signal is calculated by the following equation.

$$(S/N) = 20 \log_{10} (V_s/V_N) \quad (1)$$

where V_s = RF Signal RMS Voltage

V_N = Noise Signal RMS Voltage

The values of V_s and V_N are measured at the output of a summing network, that adds a noise signal to an RF signal, as follows:

- Measuring V_s : With only an RF signal input (noise input terminal grounded), measure the output RMS voltage of the network using a true RMS voltmeter.
- Measuring V_N : With only a noise signal input (RF input terminal grounded), measure the output RMS voltage of the network using a true RMS voltmeter.

Biternary Coding:

Biternary coding is used to add one bit of memory to a binary sequence. This is done by appropriately filtering the input binary sequence, resulting in a multi-level signal. Figure 1a shows the coded waveform of two consecutive "ones" and figure 1b shows the waveform for four consecutive "ones". The resultant waveforms are generated at the output of the coding filter.

Decoding of a biternary sequence is accomplished by using two comparators set at different thresholds and a J-K flip-flop. Figure 2 shows this decoder and figure 3 illustrates typical waveforms for the system.

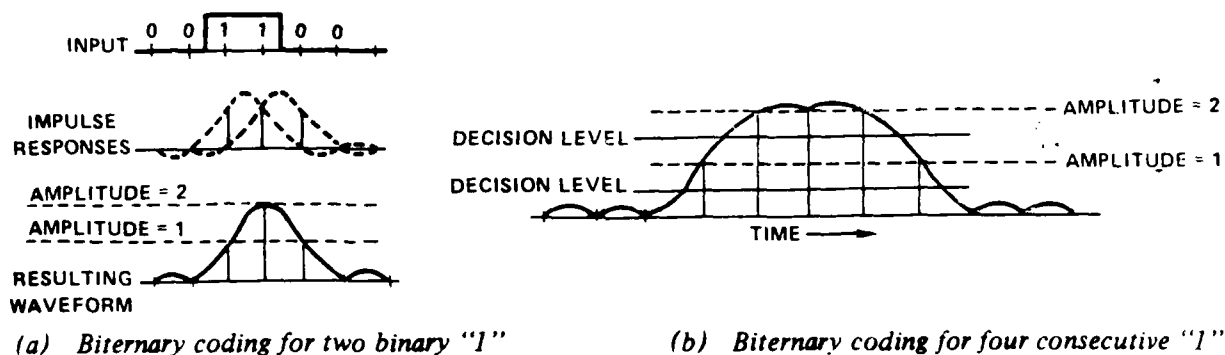


Figure 1. Examples of Biternary Coding. (1:109)

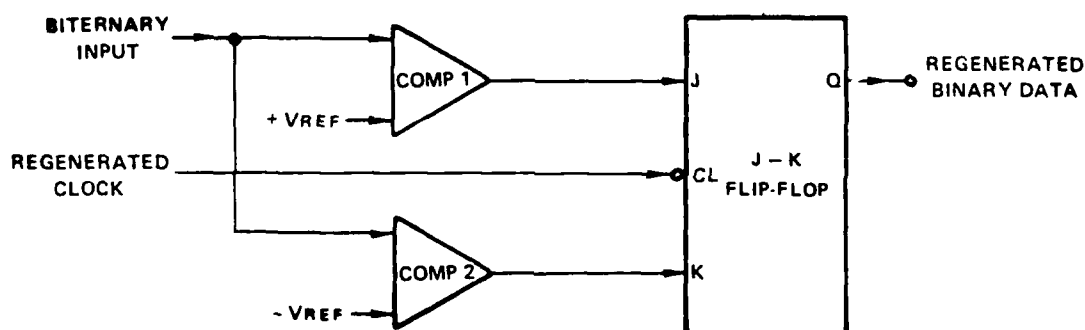


Figure 2. Biternary Decoder. (1:109)

The decoding rule is as follows:

- If the sampled amplitude is below the lower threshold, a "zero" is decoded.
- If the sampled amplitude is above the upper threshold, a "one" is decoded.
- If the sampled amplitude falls between the upper and lower thresholds, the inverse of the preceding bit is decoded.

The biternary system requires a 2.1 dB better signal-to-noise ratio to achieve the same bit error performance as an ideal binary FSK system.

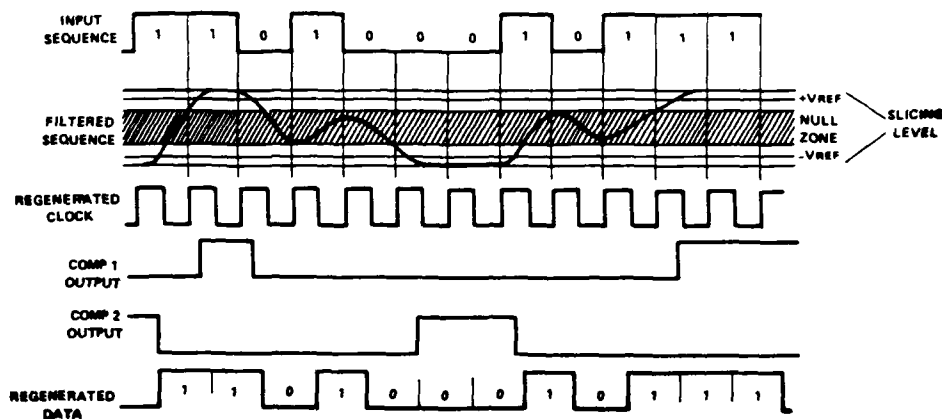


Figure 3. Typical Waveforms for the Biterinary System. (1:109)

DEGEM CIRCUIT BOARD DESCRIPTION

SOURCE: Reference (2).

Appendix - Pages 49-51 - Functional Description of Service Unit For DIGICOM - Model PU-253

EXPERIMENT PROCEDURE

General Instructions

WARNING

Turn the DEGEM Power Supply Board off before removing or inserting any plug-in boards. Damage to circuit components may result if the boards are changed while the power is on.

1. DO NOT turn the DEGEM PS-MB-1/A Power Supply Board on. This power supply board should contain the Service Unit PU-253. Attach the Rack Extension Unit to the power supply board in the horizontal position by connecting the power sockets firmly.

2. To ensure minimum noise and signal crosstalk, connect the following wires between the power supplies on the front panel of the power supply board.
 - Power Supply A (-) to Power Supply B (+)
 - Power Supply B (+) to Power Supply F (COMMON)
 - Power Supply F (COMMON) to Chassis Ground
3. Install the DIGICOM-4/1, 4/2, and 4/3 boards into the Rack Expansion Unit by pressing each board into a power socket and tightening the hold-down screws on each end of the board.
4. Turn the power supply board on. All plug-in units are internally powered and need no external power connections.
5. Turn all of the remaining equipment on.

FSK Modulator

Objective: To examine the FSK modulator and properties of the FSK signal.

1. Assemble the circuit shown in figure 4 but do not connect point A to DC IN.

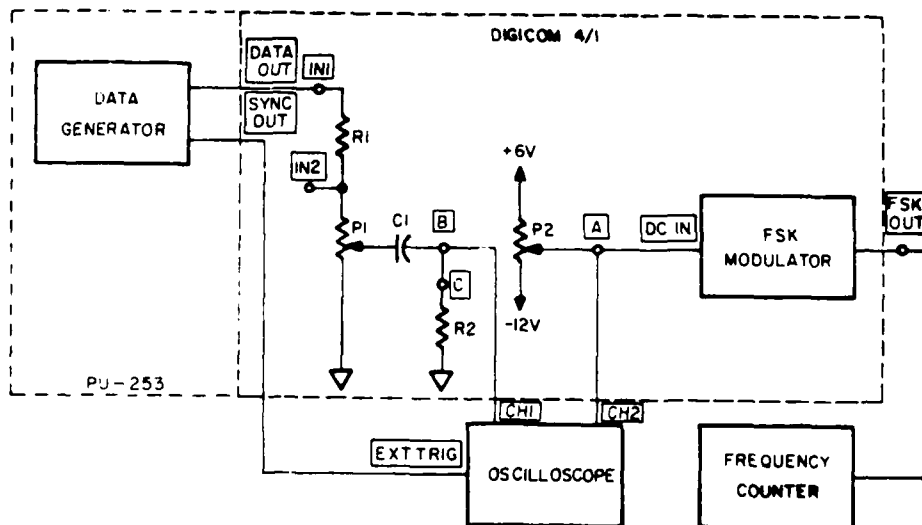


Figure 4. Calibration of the FSK Modulator. (2:15)

2. Select a data rate of 16 kbps and a sequence length of 15 on the Data Generator on PU-253.
3. With the DC IN of the FSK Modulator open, set the center frequency of FSK OUT to 512 kHz by adjusting the CENTER FREQUENCY ADJUSTMENT potentiometer. Use the frequency counter to measure the signal. Measure and record the dc voltage at DC IN using a DVM.
4. Calibrate the FSK Modulator for ± 5.8 kHz frequency deviation as follows.
 - a. Disconnect both oscilloscope probes from the circuit.
 - b. Set both channels for 1 V/DIV in the DC coupled mode.
 - c. Connect a DVM to point A and set the dc voltage to the same voltage measured at DC IN in step 3 above by adjusting P_2 . Connect point A to DC IN and also to channel two of the oscilloscope. Check the output frequency of the modulator for 512 kHz with the frequency counter.
 - d. Use the oscilloscope vertical position controls so that both channel traces coincide.
 - e. Connect channel one to point B.
 - f. Turn P_2 until the output frequency of the modulator is 512 kHz $\pm$ 5.6 kHz. Record this frequency on the data sheet.
 - g. Adjust P_1 until the top of the data signal on channel one coincides with the dc level on channel two.
 - h. Adjust P_2 until the dc level on channel two coincides with the bottom of the data signal on channel one.
 - i. Measure and record the output frequency of the modulator using the frequency counter. The difference between this frequency and that measured in step f above is the peak frequency deviation of the modulator for the input data signal.

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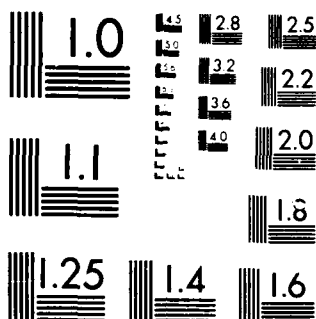
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- j. Disconnect points A and C from the circuit and connect point B directly to DC IN.
5. Connect the spectrum analyzer to FSK OUT and observe the FSK spectrum at 512 kHz with 5 kHz/DIV. Notice the effect of changing the sequence length to 255.
6. Return the sequence length to 15 and vary the input data signal frequency. Notice how the bandwidth increases significantly for higher input frequencies, which is typical of an FM system. Return the data rate to 16 kbps.
7. Do not change the positions of potentiometers P₁ and P₂ on DIGICOM-4/1 for the remainder of the experiment.

FSK System

Objective: To calibrate the receiver for optimal performance.

1. Assemble the FSK system shown in figure 5. Do not connect the dashed lines shown in the figure.
2. Receiver Calibrations:
 - a. Turn the Noise Generator on PU-253 off and turn the CARRIER+NOISE AMP control of the Summing Network fully ccw.
 - b. Connect the True RMS Voltmeter to the output of the Summing Network and set the output amplitude to 50 mV_{rms} by adjusting the SIGNAL AMP control.
 - c. Set the IF Bandwidth to NARROW.
 - d. Disconnect both oscilloscope probes from the circuit. Set both channels for 200 mV/DIV and align both traces vertically so they coincide.
 - e. Connect channel one (ac coupled) of the oscilloscope to the output of the filter on DIGICOM-4/3 and channel two (dc coupled) to V ref. 3 of the NRZ Regenerator. Externally trigger the oscilloscope from the 16 kHz clock signal of the Clock and Carrier Generator on PU-253.

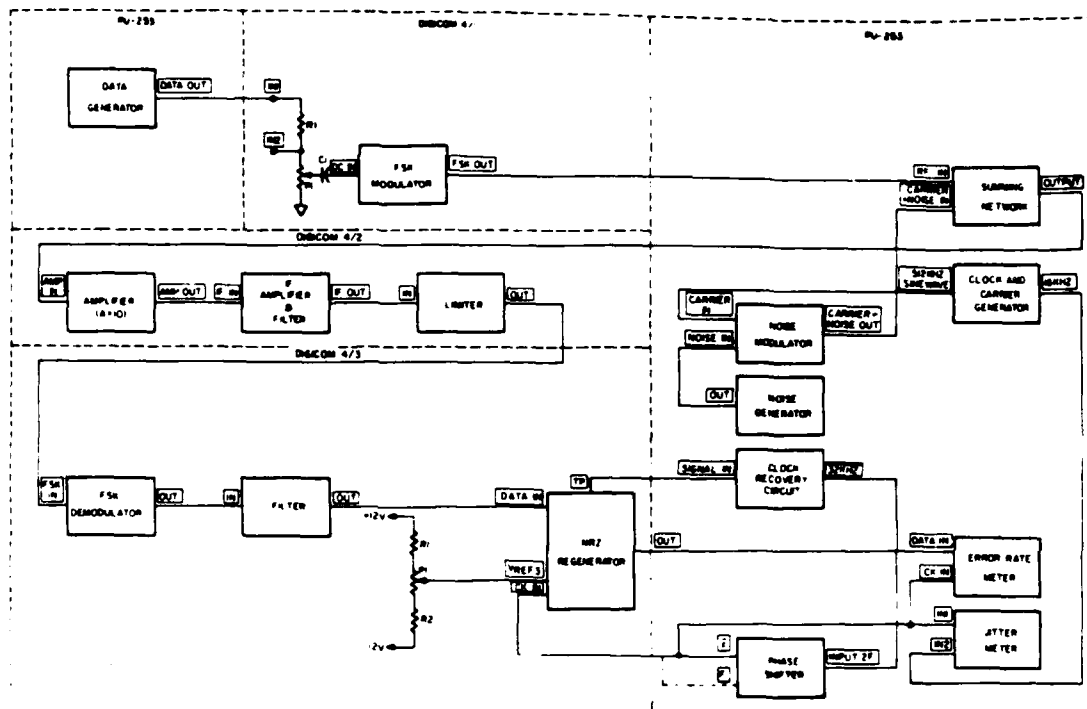


Figure 5. FSK System. (2:34)

- f. Display the eye diagram (channel one signal) as shown in figure 5. Set the decision threshold (channel two signal) to the maximum horizontal opening, by adjusting P_1 on DIGICOM-4/3, as shown in the figure.
- g. Connect channel two of the oscilloscope to CK IN of the NRZ Regenerator. Make certain the Clock Recovery Circuit on PU-253 is in sync with the data signal. If it is not, press RESET several times until sync is achieved.
- h. Observe the eye diagram on channel one and the CK IN signal on channel two. Adjust the PHASE SHIFTER control on PU-253 until the rising edge of the CK IN signal is set at the maximum vertical opening of the eye diagram as shown in figure 6. This sets the optimal sampling point of the receiver.

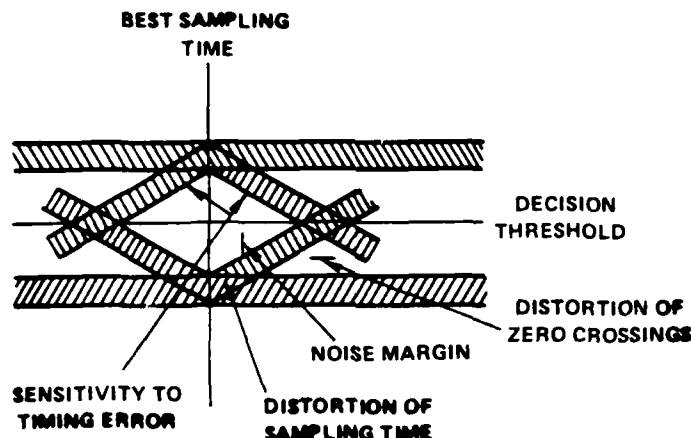


Figure 6. Binary Eye Diagram. (1:105)

- i. Set the Error Rate Meter in the 10^{-4} NORMAL mode on the PU-253. Make sure that there are no errors indicated. If there are, readjust the decision threshold and the sampling point as described above.
- j. Connect channel one of the oscilloscope to DATA OUT of the Data Generator and channel two to OUT of the NRZ Regenerator. Trigger the oscilloscope externally from SYNC OUT of the Data Generator. Make sure that the input and output data sequences are the same. There may be a two bit shift between the two sequences.

Performance of Binary FSK in White Noise

Objectives: To measure the bit error rate versus input signal-to-noise ratio of the binary FSK system in bandlimited white noise.

1. Set the IF BANDWIDTH to WIDE.
2. Connect the True RMS Voltmeter to the output of the Noise Generator on PU-253 and turn the Noise Generator on. Set the output noise signal to 150 mVrms by adjusting the Noise Amplitude control.

3. Connect the True RMS Voltmeter to the output of the Summing Network. Disconnect RF IN from FSK OUT and ground the RF IN terminal. Set the Carrier+Noise signal to 10 mV_{rms} by adjusting the CARRIER+NOISE AMP control. Reconnect the RF IN terminal to FSK OUT. The output of the Summing Network now has a 50 mV_{rms} to 10 mV_{rms} signal-to-noise ratio, or 14 dB using equation (1) of the theoretical background section.
4. Make certain the Clock Recovery Circuit is in sync with the data signal.
5. Use the Bit Error Meter on PU-253 in the 10^{-4} mode where the number of the errors shown on the meter reflects an error rate of that number times 10^{-4} .
6. Average at least ten error samples and record the bit error rate for a S/N ratio of 14 dB on the data sheet in the Binary column.
7. Decrease the S/N ratio by increasing the RMS amplitude of the NOISE+CARRIER in steps according to the data sheet. Use the same procedure as described in step 3 above. For each S/N ratio, measure and record the average bit error rate for at least ten samples.
8. Plot the Bit Error Rate versus S/N ratio on the provided semi-log paper. Label this curve as Binary FSK.

Partial Response FSK System

Objective: To examine and calibrate the biternary, partial response receiver.

1. Test Circuit Setup:

- a. Modify the test circuit as shown in figure 7. Do not connect the dashed lines shown in the figure. In this test circuit, the Biternary Regenerator is used instead of the NRZ Regenerator. A biternary filter is also added to the input of the FSK Modulator.
- b. Connect the 32 kHz clock to the Jitter Meter instead of the 16 kHz clock.

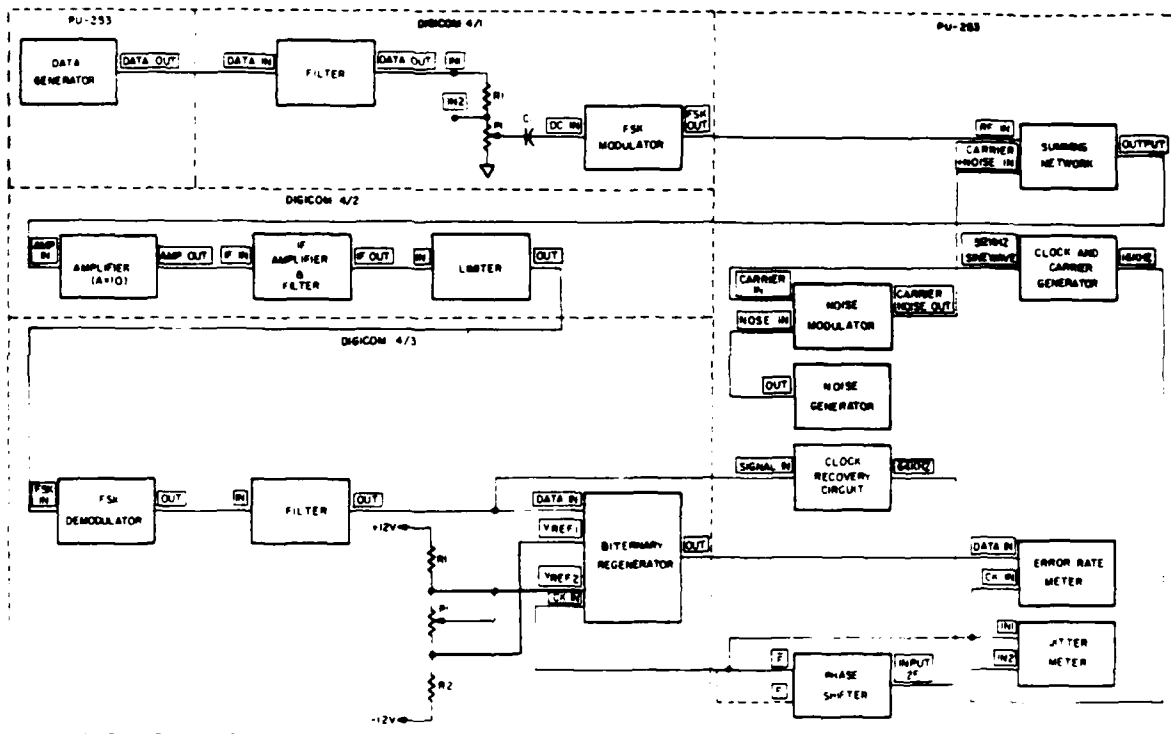


Figure 7. Biternary FSK System. (2:42)

- c. Change the input signal to 32 kbps with a sequence length of 15.

2. Biternary Signal:

- a. Connect the dual trace oscilloscope to the input and output of the biternary filter in front of the FSK Modulator. Trigger the oscilloscope externally from the SYNC OUT of the Data Generator. Observe both waveforms.
- b. Compare the output waveform of the filter to the analog waveform that was shown in figure 3. The waveforms are not identical since the data sequences are different. But notice on the oscilloscope that

the coding of two or more consecutive "ones" has a higher amplitude than the coding of a single "one" preceded by a "zero". There may be a one to two bit delay in the output waveform.

- c. Change the input data rate and observe the different output waveforms. Notice that the best data rate for the biternary signal is 32 kbps since there are three distinct decision regions for this data rate. Return the data rate to 32 kbps.

3. Receiver Calibration:

- a. Turn off the Noise Generator.
- b. Remove both oscilloscope probes from the circuit. Set channel one in the ac coupled mode and channel two in the dc coupled mode. Set both channels for 200 mV/DIV and align both traces vertically so they coincide. Trigger the oscilloscope externally from the 32 kHz clock signal.
- c. Connect channel one to the filter output on DIGICOM-4/3 and channel two to V ref. 2. Adjust P₁ on DIGICOM-4/3 until the channel two dc level is set at the upper threshold position as shown by the upper dotted line in figure 8.

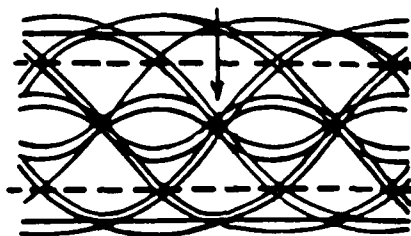


Figure 8. Biternary Eye Diagram. (3:34)

- d. Connect channel two to V ref. 1 and confirm that the dc level is at the lower threshold position.

- e. Connect channel two to CK IN of the Biterinary Regenerator and make sure that the Clock Recovery Circuit is locked.
- f. Adjust the rising edge of the CK IN signal to the point indicated by the arrow in figure 8 by adjusting the Phase Shifter Control on PU-253.
- g. Make sure there are no errors indicated on the Error Rate Meter.
- h. Connect the oscilloscope to the input and output data signals of the FSK system. Trigger the oscilloscope externally from SYNC OUT of the Data Generator. Observe both waveforms and confirm that they are identical except for a shift of about two bits.

Performance of Biterinary FSK in White Noise

Objective: To measure the bit error rate versus input signal-to-noise ratio of the biterinary FSK system in bandlimited white noise.

1. Repeat the same error rate procedure as was outlined in the performance section for the binary system.
2. Plot the bit error performance data on the same graph used for the binary system data. Label this curve as Biterinary FSK. Notice the difference in performance between the two systems.

STUDENT NAMES _____ DATE PERFORMED _____

Note: Indicate unit of measurement with each data entry.

MODULATOR:

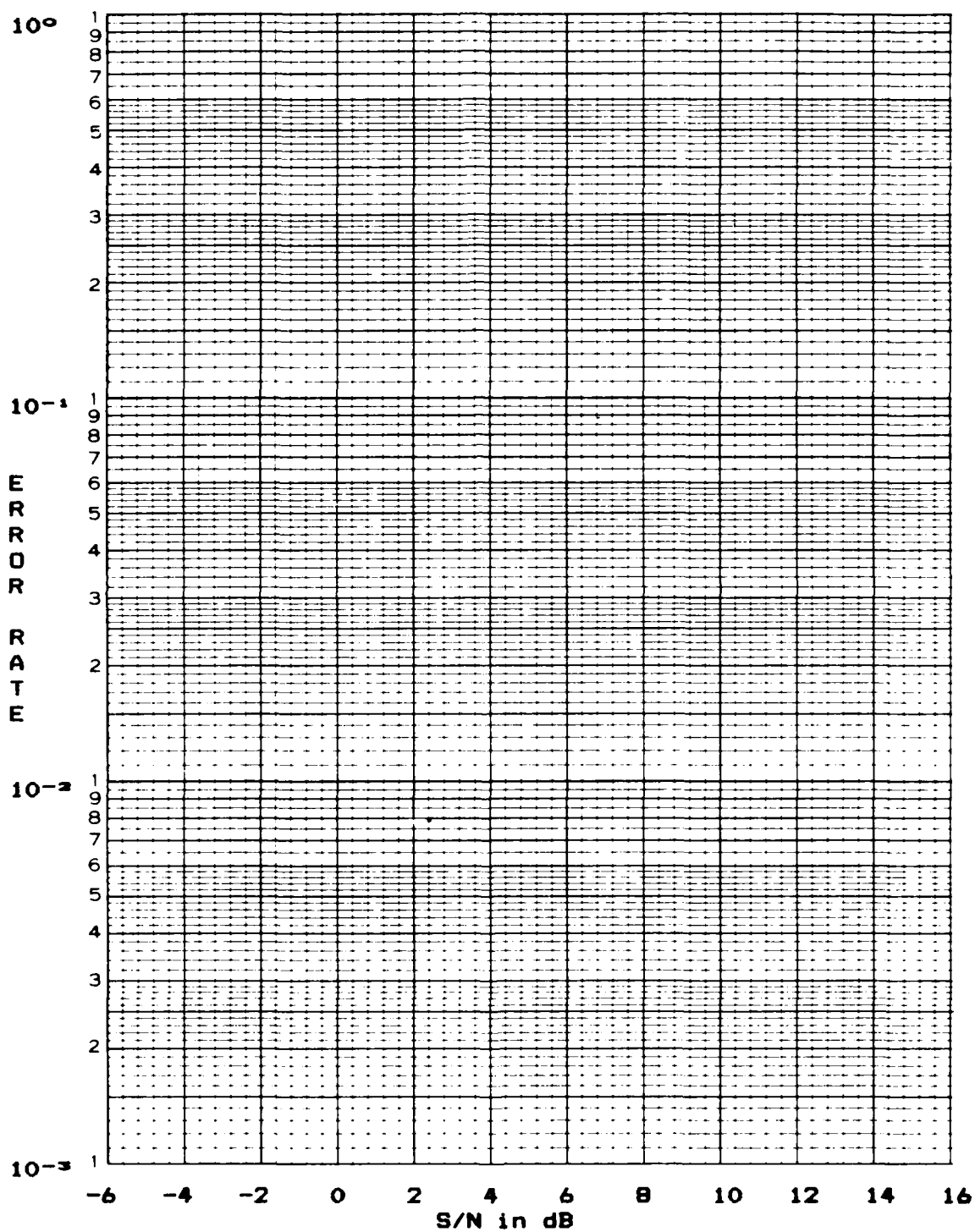
DC IN Voltage (Vdc) _____ Lower Out. Freq _____

Upper Out. Freq _____

PERFORMANCE:

Signal Amplitude = 50 mVrms

NOISE AMPLITUDE (mVrms)	S/N (voltage ratio)	S/N (dB)	BIT ERROR RATE BINARY	BIT ERROR RATE BITERNARY
10	5.00	13.98	_____	_____
15	3.33	10.46	_____	_____
20	2.50	7.96	_____	_____
25	2.00	6.02	_____	_____
30	1.67	4.44	_____	_____
35	1.43	3.10	_____	_____
40	1.25	1.94	_____	_____
45	1.11	0.92	_____	_____
50	1.00	0.00	_____	_____
60	0.83	-1.58	_____	_____
70	0.72	-2.92	_____	_____
80	0.63	-4.08	_____	_____
90	0.55	-5.10	_____	_____
100	0.50	-6.02	_____	_____



STUDENT NAMES _____ SAMPLE _____ DATE PERFORMED _____

Note: Indicate unit of measurement with each data entry.

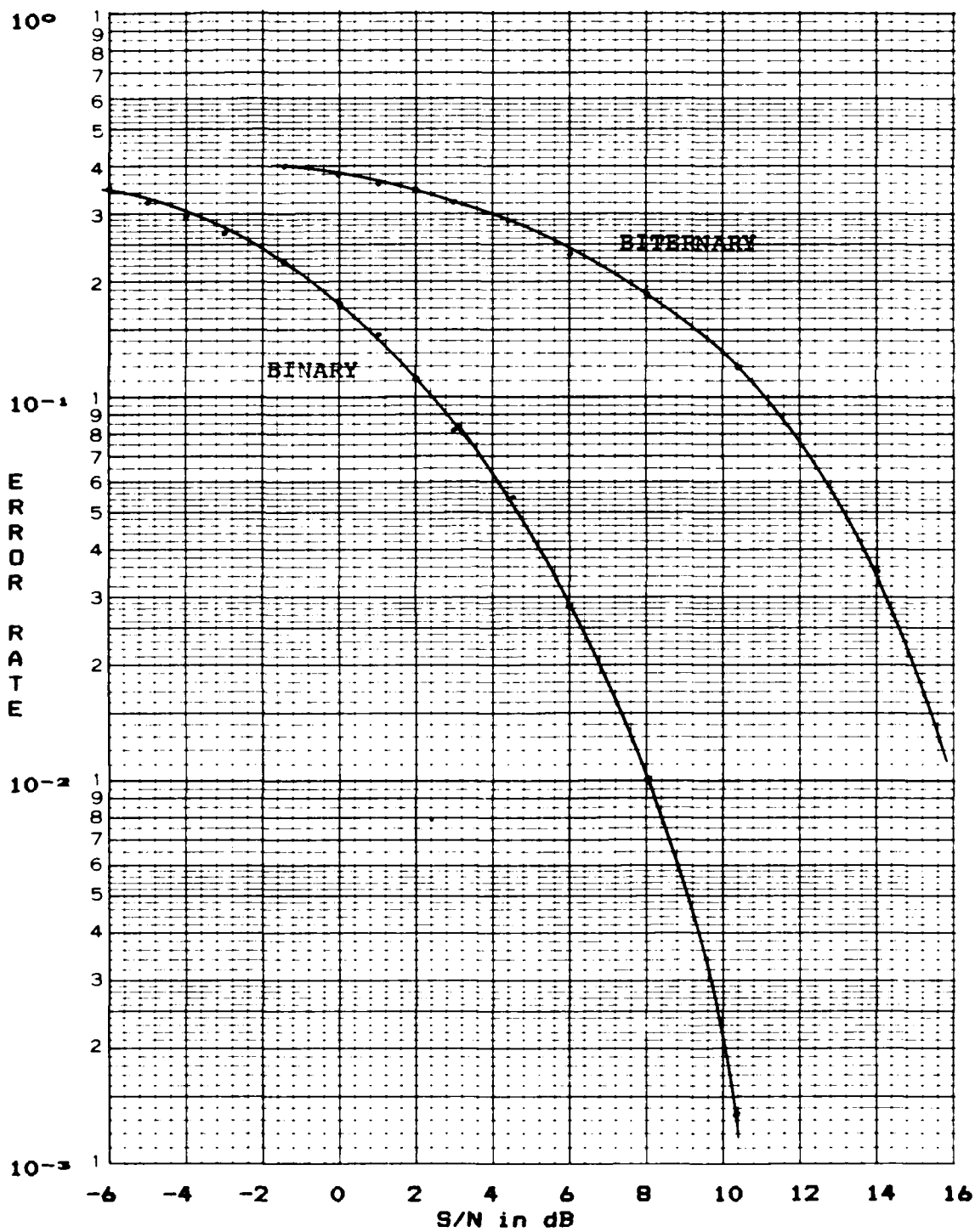
MODULATOR:

DC IN Voltage (Vdc) -3.23 Lower Out. Freq 506.4 kHz
 Upper Out. Freq 518.6 kHz

PERFORMANCE:

Signal Amplitude = 50 mVrms

NOISE AMPLITUDE (mVrms)	S/N (voltage ratio)	S/N (dB)	BIT ERROR RATE BINARY (10^{-3})	BIT ERROR RATE BITERNARY (10^{-3})
10	5.00	13.98	0.00	35.2
15	3.33	10.46	1.30	123
20	2.50	7.96	10.3	186
25	2.00	6.02	28.4	237
30	1.67	4.44	54.0	289
35	1.43	3.10	81.0	309
40	1.25	1.94	114	349
45	1.11	0.92	144	360
50	1.00	0.00	175	379
60	0.83	-1.58	225	398
70	0.72	-2.92	263	No Lock
80	0.63	-4.08	295	
90	0.55	-5.10	322	
100	0.50	-6.02	349	



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VITA

First Lieutenant Jerome B. Thompson was born on 27 May 1961 in Milwaukee, Wisconsin. He graduated from high school in Grafton, Wisconsin and attended the Milwaukee School of Engineering from which he received the degree of Bachelor of Science in Electrical Engineering in May 1983. Upon graduation, he entered the USAF Officer Training School at Lackland Air Force Base, San Antonio, Texas and received his commission on 9 September 1983. He immediately entered active duty being assigned to the Air Force Institute of Technology. He worked as the AFIT Alternate Safety Officer until entering the School of Engineering in June 1984.

Permanent Address: 1611 North Pine Street
Grafton, Wisconsin 53024

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This study was a development of a series of experiments for an electronics communications laboratory. These experiments were designed to reinforce theoretical courses offered in the Air Force Institute of Technology Electrical Engineering Core Communications Sequence in the form of demonstrations or laboratory exercises.

The experiments were developed under the criteria of investigating a significant number of analog and digital communication system concepts with a minimum amount of experimentation time. Extensive use of a spectrum analyzer was included in many of the experiments.

The topics covered in the experiments include: amplitude modulation; frequency modulation; balanced modulator; single sideband modulation; phase-lock loop and frequency synthesizer; pulse amplitude modulation; pulse code modulation; delta modulation; amplitude shift keying; phase shift keying; and frequency shift keying.

The results of this study indicated that many more system concepts could be included in laboratory exercises, such as spread spectrum communications, time and frequency division multiplexing, and computer oriented testing and analysis.

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