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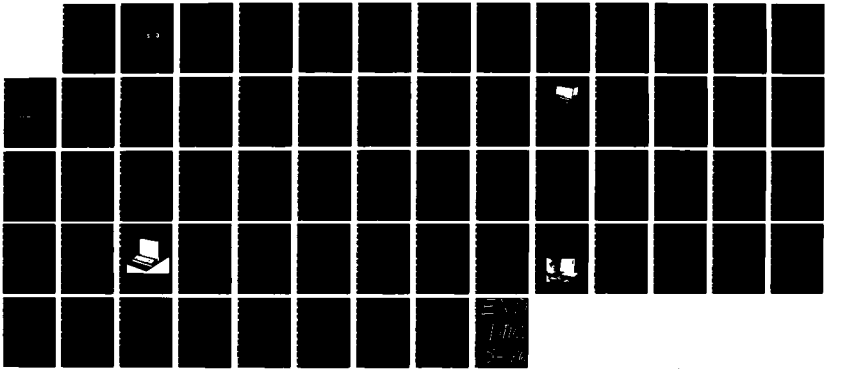

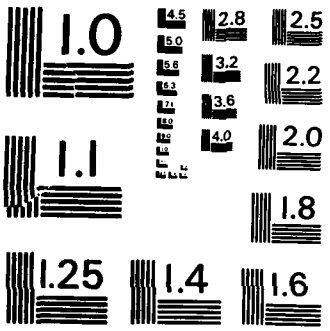

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February 1986

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J. C. Bussert

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By means of design for testability (DFT) techniques, the NOSC Test Technology Office (Code 936) evaluated testability improvements in a state-of-the-art printed-circuit board. Data were gathered to provide a direct comparison among various testability figure of merit (TFOM) tools.

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ACRONYMS AND ABBREVIATIONS

ATPG	Automatic Test Program Generator
ATE	Automatic Test Equipment
BIT	Built-in Test
CAD	Computer-Aided Design
CAE	Computer-Aided Engineering
CAT	Computer-Aided Testability
COPTR	Controllability-Observability-Predictability-Testability Report
DFT	Design for Testability*
DTA	Daisy Testability Analyzer
FI	Fault Isolation
IRAD	Independent Research and Development
ITFOM	Inherent Testability Figure of Merit
LOGMOD	Logic Model
LONGMOD	Longendorfer Model
MILMOD	Military Model
PCB	Printed-Circuit Board
RADC	Rome Air Development Center
SCOAP	Sandia Controllability/Observability Analysis Program
STAMP	System Testability Analysis Maintenance Program
TFOM	Testability Figure of Merit
UUT	Unit Under Test*

* In this report UUT and DFT will also mean the original circuit and testability modified design, respectively.

OVERVIEW

This document is a logical follow-up to NOSC TD 743 (July 1984) comparing testability figure-of-merit (TFOM) tools on a simple small scale integration (SSI) circuit board. This new comparison is based upon a state-of-the-art board with four Advanced Micro Device (AMD) AM2901 microprocessors. This more clearly represents the test challenge facing today's engineers since only tools able to handle thousands of nodes are really useful. TFOM tools used in the previous comparison not used in this comparison are the Longendorfer Model (LONGMOD), the Inherent Testability Figure of Merit (ITFOM), and the Sandia Controllability/Observability Analysis Program (SCOAP). LONGMOD cannot handle over 200 nodes; the problems causing ITFOM to provide an improper figure of merit have not been remedied; and SCOAP is the basis of the Daisy and CALMA software used in this new comparison. The DETEX Systems Inc. LOGMOD, Arinc Research Corporation STAMP, Rome air Development Center (RADC) printed-circuit board (PCB) checklist, and military standard on testability (MIL-STD-2165) Appendix B are all rerun in this new TFOM comparison.

The modeling of the existing board configuration referred to as unit under test (UUT) and a modified design for test (DFT) version is continued as before with one major methodology change. In the previous comparison, DFT changes were made before the TFOM runs. In this comparison, all TFOM UUT outputs are reviewed and used in the redesign process. This represents a more realistic application by an engineer in the early design phase who is seeking advice from the TFOMs on how to improve his design's testability by noting the problem areas. The TFOMs are compared as to how they provide remedial steps and focus on specific problem areas. The engineer may still use his expertise in electronics to determine the different impact of a "clock," ambiguity groups requiring additional gates, and other data input ambiguity groups that are not harmful to the testability. Some algorithms will be more advisory than others or will point out different types of DFT program areas.

As before, the TFOMs are in three generic groups with unique limitations and advantages inherent. The checklists are low cost, manual, and simplistic. The logic models have circuit topology, but regard everything as a block with inputs and outputs. Finally, the most detailed SCOAP algorithms require model libraries of the devices and most nearly simulate the circuit devices.

By studying the circuitry and looking for DFT problems, before running the TFOMs, possible areas of redesign were anticipated. The tristate and clock parallel inputs make isolation or control of the four bit-slice microprocessors impossible. With the entire circuit running data in and out at 4 MHz, the associated chips were also changing with no selective control allowed. A few large internal fanouts and feedback loops were noted that would cause ambiguity problems with no observability. A good test engineer could predict the obvious modifications to resolve these severe test problems, but, unfortunately, many board designers do not have their input during the early design phase. An overview of the five-page schematic breakdown of this circuit is shown in figure 1. Note the fanout of data and serious feedback problems, especially in sheet five, which has the four 2901 microprocessors. The DFT design enhancements consisted of breaking feedback loops going into sheets three, five, and

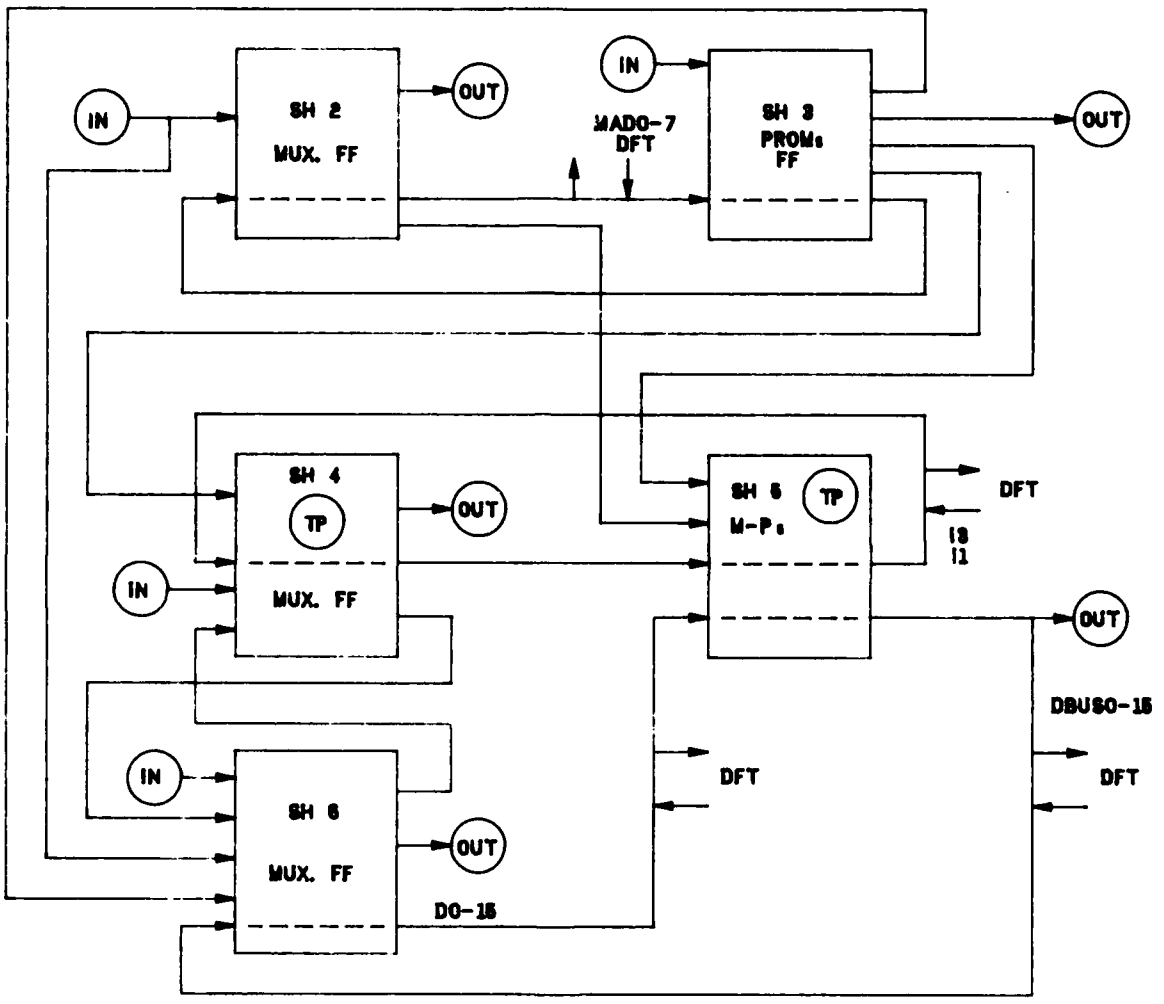


Figure 1. Interschematic sheet signal flow with DFT enhancements indicated.

six, and adding test points on sheets 4 and 5. The clock and tristate signals are sent to all four 2901s without any method to separate the microprocessors or gate the signals selectively. These signals were gated as DFT modifications, which are not shown on figure 1.

The actual schematics are proprietary designs and cannot be reproduced in this report. However, the design technology is summarized in table 1, which lists all of the integrated circuit (IC) chip types, functions, and number of occurrences. The complexity of the schematic is demonstrated in figure 2, which shows a computer-aided design (CAD) workstation overview of sheet three of the five sheets. This page reveals no signals, pins, chip types, or other possibly sensitive information, but does clearly show the density of the schematic devices.

The UUT has 16 types of chips for a total population of 44 ICs. The card has 135 input/output edge pins, 42 of which are unloaded and considered test points. All the ICs are standard 5400 transistor-transistor logic (TTL) chips from a Fairchild TTL book except for four 2901A microprocessors, a Motorola Look-ahead carry generator, and a National 256 x 8 programmable read-only memory (PROM).

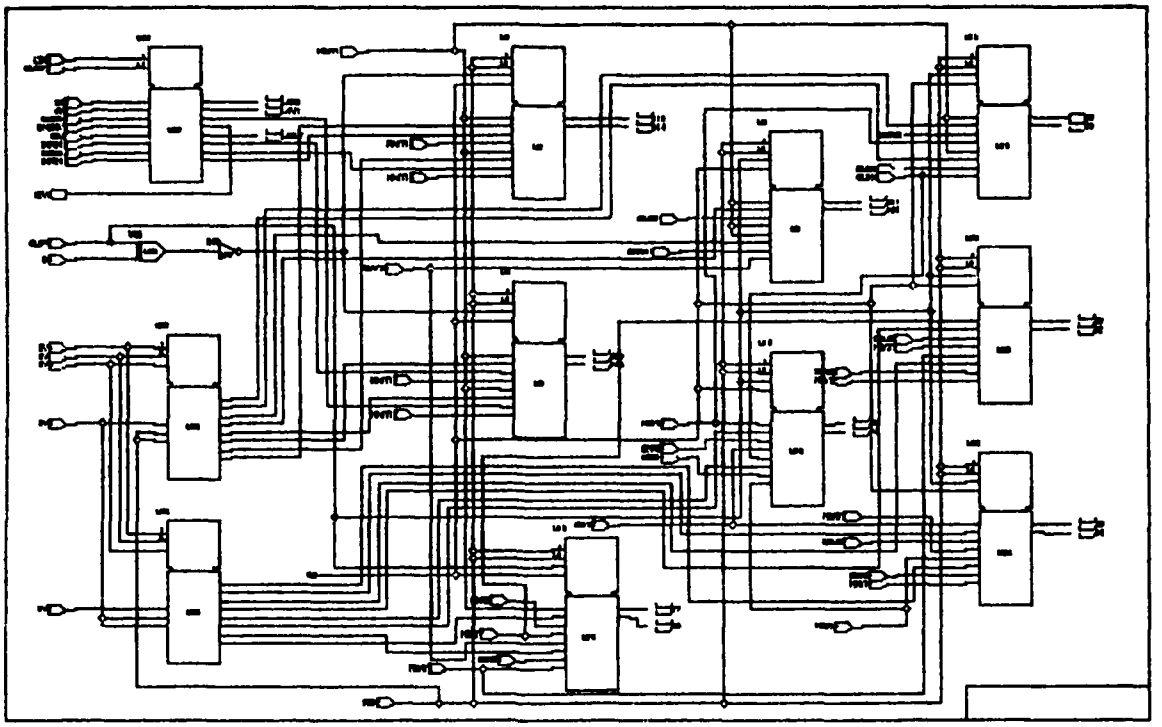
Some limitations to the scope of this study were self-imposed, but are noted here because the potential TFOM user may desire to use additional features. The two logic-modeling tools have inherent fault isolation (FI) and diagnostic data outputs as well as life-cycle cost information such as mean time to repair (MTTR), FI time, and maintainability. Rather than demonstrate these data, output formats were restricted to DFT and figure-of-merit (FOM) numbers. The CAD workstations and dynamic timing and functional analysis software are important to the designer and test engineer, but again, inclusion would have extended far beyond the TFOM comparison goal.

Various technical articles discuss using automatic test program generators (ATPGs), such as LASAR and HITS as TFOM tools, and "after the fact" they can measure testability. However, the intent of DFT is to measure testability early while changes can be easily made before manufacturing the circuit. By the time that test programs are required for automatic test equipment (ATE), the design is in production, making changes difficult and costly. Therefore, ATPGs are not included in this comparison.

The designer should note that many variations are possible in TFOM measures and in their differences in utility and application to a given circuit design. The designer should approach a single TFOM output cautiously to avoid misleading or wrong conclusions. For example, the designer might look at test point utilization frequency instead of noting the necessity for fault isolation. TFOMs must be kept in context and properly interpreted. TFOMs are best used to obtain options for changes, since TFOMs are only windows into the system being analyzed. A single TFOM is attractive, but the complexity of the topic may make the single TFOM unattainable. As ARINC wrote in a letter, "It is options that count, not number."

Table 1. Summary of the 16 chip types used in the circuit.

CHIP	FUNCTION	POPULATION
54LS153	Dual 4-input MUX	9
54S182	Look-ahead carry generator	1
54LS253	Dual 4-input MUX	3
54LS471 2	National 256 x 8 PROM	5
AMD2901A	Microprocessor (AMD)	4
54LS377	Octal D flip-flop	6
54LS157	1-of-8 decoder/DEMUX	2
54LS00	Quad 2-input NAND gate	2
54LS86	Quad 2-input EXCL OR gate	2
54LS04	HEX inverter	1
54LS02	Quad 2-input NOR gate	1
54LS138	1-of-8 decoder/DEMUX	2
54LS158	Quad 2-input MUX	2
54174	HEX D flip-flop	2
LS154	1-of-16 decoder/DEMUX	1
54273	8-bit register	1
	Total	44



```
                ############
                ############
G:1 M:1 T:CU  #:ON
01 ◀SHEET MENU▶
02 ADD SYMBOL                17 MIRROR ITEM
03 ADD DYNAMIC               18 ROTATE ITEM
04 ADD HIERARCHY             19 DELETE ITEM
05 DRAG SYMBOL               20 LIST ITEM
06 ADD NET                   21 ◀AREA OPERATIONS▶
07 NAME NET                  22 ADD MATRIX
08 ROUTE NET                 23 COPY AREA
09 REROUTE NET               24 MOVE AREA
10 SHOW NET                  25 ROTATE AREA
11 ADD BUS                   26 DELETE AREA
12 ADD BUSTAP                27 LIST AREA
13 REPLACE SEGMENT           28 ◀SHEET TEXT MENU▶
14 DELETE SEGMENT            29 ◀SHEET MANAGEMENT▶
15 COPY ITEM                 30 ◀MISC COMMANDS▶
16 MOVE ITEM
```

Figure 2. CAD overview of sheet four of five sheets comprising the circuit (top). Note sheet menu (bottom).

1.0 CHECKLISTS

Checklists are a low-mix TFOM approach, requiring no schematic capture, net lists, or central processing unit (CPU) time. The RADC PCB checklist is limited to digital-circuit board applications, whereas MIL-STD-2165 Appendix B covers analog, digital, and hybrid applications from module to system level. The RADC list has fixed items and weighting, whereas Appendix B allows subjective inclusion or rejection of items and freedom to assign weighting values. Although at the low-mix pencil and paper level of TFOM tools, the checklists include very "smart" questions that can point out DFT problem areas if consciously applied by a knowledgeable test engineer or technician.

1.1 MIL-STD-2165 APPENDIX B

The unofficial MIL-STD-XXX checklist was used in the previous comparison. In January 1984, the MIL-STD-2165, "Testability Program for Electronic Systems and Equipments," was officially issued. The 11-page Appendix B, "Inherent Testability Checklist," was retained with a few added and deleted items. Table 2 lists the 10 major sections and the number of items in each. Figure 3 shows the first page as a sample. The 114 items include many topics not related to grading the "inherent testability" of a circuit design before production. MIL-STD-2165, paragraph 50.1, "Procedures for Use of the Appendix B Table IV Checklist," allows the user to delete items "which are not applicable to the design," "additional testability criteria to Table IV," and assign desired "weighting factors (WT) to each item" with concurrence "from the requiring authority." For this circuit, nearly two-thirds (or 76) of the items were deleted as not relevant to estimating the testability of this design.

Table 2. MIL-STD-2165 Appendix B functional breakdown.

Section	Items
Mechanical Design	12
Partitioning	9
Test Control	12
Test Access	9
Parts Selection	4
Analog Design	18
Digital Design	16
Built-In Test (BIT)	21
Test Requirements	5
Test Data	8

The weighting factor of most items was "1," with about 16 important items, such as feedback, fanouts, or control, increased to "10." The important items on internal and external fanouts require some intensive schematic node counting. The node fanout sheet provided with the RADC checklist (in the next section) is ideal for itemizing this crucial data. The UUT TFOM for this circuit was 20.9 of a possible 100, which indicates a poor testability design. Critics of Appendix B point out that adjusting the weighting factors and retaining many items for "free points" could easily raise the

Table IV. Inherent Testability Checklist

	WT	Total Number	Number Meeting Criteria	Score	WT Score
Mechanical Design					
Is a standard grid layout used on boards to facilitate identification of components?					
Is enough spacing provided between components to allow for clips and test probes?					
Are all components oriented in the same direction (pin 1 always in same position)?					
Are standard connector pin positions used for power, ground, clock, test, etc., signals?					
Are the number of input and output (I/O) pins in an edge connector or cable connector compatible with the I/O capabilities of the selected test equipment?					
Are connector pins arranged such that the shorting of physically adjacent pins will cause minimum damage?					
Is defeatable keying used on each board so as to reduce the number of unique interface adapters required?					
When possible, are power and ground included in the I/O connector or test connector?					
Have test and repair requirements impacted decisions on conformal coating?					
Is the design free of special set-up requirements (e.g., special cooling) which would slow testing?					

Figure 3. MIL-STD-2165 Appendix B sample checklist.

score 20 to 30 points without making any circuit design changes. The weights should be assigned before the detailed design. Appendix B, if intelligently and honestly used by the test or design engineer, can point out serious testability problems, such as high-fanout, ambiguity problems, and clock or control difficulties. One of the most serious and common DFT design problems is feedback loops. This was true on the simple SSI UUT last year and the complex microprocessor UUT this year. Feedback is mentioned in one checklist item directly, but redundant items, partitioning, and fanout items can correlate with feedback in this design. By changing the design based upon the identified problems and maximizing weight values, the DFT TFOM increases to 35.7. This is still an unacceptable score, considering the actual increase in testability and control of this circuit. If built-in test (BIT) was in the chip or circuit design, such as set-scan, there are 21 items in the BIT checklist section that could possibly enhance the TFOM WT score. Although the MIL-STD-2165 checklist is one of the least automated tools for measuring testability, it does include many questions that can point out design deficiencies and reward good test design changes. Most complex software algorithms cannot detect all of these DFT problems now. Values for BIT features and differentiating clock and reset lines from "normal data" lines are good examples. This checklist performed much better than last year, within the limitations of honesty and integrity of the user. It is still difficult to achieve a target TFOM figure by redesign alone.

1.2 RADC PCB CHECKLIST SHEET

Rome Air Development Center Technical Report (RADC-TR-79-327) of January 1980 "An Objective Printed Circuit Board Testability Design Guide and Rating System," includes a PCB testability evaluation score sheet (figure 4).

Figure 5 shows the filled-in PCB evaluation sheet. The four positive factors, B1 through B4, total only 34.5 of the possible 100 rating, before the negative N1-N30 factoring. Forty-five points were lost in B3 and B4 because there was over 50% sequential chips and over 1,801 gates. In fact, over 80% of the chips were sequential, and over 7,000 gates were on this UUT. In the negative N factors, 40 points were subtracted for nonsocketed microprocessors and 35 for redundant-logic ambiguity groups. With a total negative score of -169.3 points, the net total testability rating was -137.8. Any PCB rating from 0% to -100% is rated "impossible to test without extreme cost penalties." This UUT was selected because of parallel control signals to the four microprocessors and its high-gate technology, so a poor score was expected. It is disturbing that if the microprocessor and UUT did have comprehensive self-test and BIT, the score would still be around -50%. The only BIT credit is in N24 redundant-logic penalty. The basic B and negative N factors seem to dictate that any design using very large scale integration (VLSI) or microprocessors will have a net score of -50% or worse, even with BIT, and would be rated as untestable. This could be unacceptable by government design criteria during the MIL-STD testability FOM negotiations.

An associated node accessibility score sheet (figure 6) is also used. The top portion of figure 6 shows the number of accessible edge-pin fanouts of connected chips. The lower portion shows the number of internal nodes with chip fanouts. The accessible fanout nodes of over eight paths were +5V, grounds, and clock

FACTOR	DESCRIPTION	SCORE	POSSIBLE RATING	ACTUAL RATING	COMMENTS
B1	Percent Nodes Accessible		30%		
B2	Proper Documentation		25%		
B3	% of Sequential Ckts		25%		
B4	PCB Complexity Count		20%		
	Total Basic Score		100%		
N1	Monostable Ckt		-%/Inst		
N2	Counters (Pkgs x Stgs)		-%/Inst		
N3	Max. No. Function Blocks/ Node (No Access)		-%/Inst		
N4	Max. No. Function Blocks/ Node (Accessible)		-%/Inst		
N5	Seq. Supply Voltages		-10%		
N6	Non-Remov. Memories		-%/Inst		
N7	Non-Rem. Buried Memory		-%/Inst		
N8	Removable Complex Part		-%/Inst		
N9	Non-Rem. U-Proc, VLSI		-10%/Inst		
N10	Init. of Seq. CKTS		-%/Inst		
N11	Ext. Loading Req'd		-5%		
N12	Different Logic Types		-%/Inst		
N13	Buried Seq. Logic		-%/Inst		
N14	I/O Pins Distinguished		-3%		
N15	Excess Warm-up Time		-3%		
N16	Tolerance		-%/Inst		
N17	High Power		-%/Inst		
N18	Critical Frequency		-5%		
N19	Clock Lines		-20%		
N20	Ext. Test Equipment		-%/Inst		
N21	Environmental		-10%		
N22	Adjustments		-%/Inst		
N23	Complex Signal Inputs		-%/Inst		
N24	Redundant Logic		-%/Inst		
N25	No. of Logic Voltages		-1%/L.V.		
N26	No. of Power Supplies		-1%/P.S.		
N27	Schematic Connectives		-20%		
N28	I/O Pin – Schematic		-5%		
N29	Dual Pin Designations		-3%/Inst		
N30	Symbols on Schematic		-5%		
	Total Negative Score				
	Net Total Score				

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Figure 4. PCB testability evaluation score sheet (courtesy Rome Air Development Center).

FACTOR	DESCRIPTION	SCORE	POSSIBLE RATING	ACTUAL RATING	COMMENTS
B1	Percent Nodes Accessible		30%	12	15
B2	Proper Documentation		25%	19.5	
B3	% of Sequential Ckts		25%	0	4 DFT
B4	PCB Complexity Count		20%	0	
	Total Basic Score		100%	31.5	34.5
N1	Monostable Ckt		-%/Inst	0	
N2	Counters (Pkgs x Stgs)		-%/Inst	0	
N3	Max. No. Function Blocks/ Node (No Access)		-%/Inst	5.4	5.2
N4	Max. No. Function Blocks/ Node (Accessible)		-%/Inst	5.6	5.2
N5	Seq. Supply Voltages		-10%	0	
N6	Non-Remov. Memories		-%/Inst	0	
N7	Non-Rem. Buried Memory		-%/Inst	50	
N8	Removable Complex Part		-%/Inst	0	
N9	Non-Rem. U-Proc, VLSI		-10%/Inst	40	
N10	Init. of Seq. CKTS		-%/Inst	-1.7	
N11	Ext. Loading Req'd		-5%	-5	
N12	Different Logic Types		-%/Inst	-3	
N13	Buried Seq. Logic		-%/Inst	-.6	-.1
N14	I/O Pins Distinguished		-3%	-3	
N15	Excess Warm-up Time		-3%	0	
N16	Tolerance		-%/Inst	0	
N17	High Power		-%/Inst	0	
N18	Critical Frequency		-5%	-2	
N19	Clock Lines		-20%	-3	-1
N20	Ext. Test Equipment		-%/Inst	0	
N21	Environmental		-10%	0	
N22	Adjustments		-%/Inst	0	
N23	Complex Signal Inputs		-%/Inst	-15	
N24	Redundant Logic		-%/Inst	-35	-29
N25	No. of Logic Voltages		-1%/L.V.	0	
N26	No. of Power Supplies		-1%/P.S.	0	
N27	Schematic Connectives		-20%	0	
N28	I/O Pin – Schematic		-5%	0	
N29	Dual Pin Designations		-3%/Inst	0	
N30	Symbols on Schematic		-5%	0	
	Total Negative Score			-169.3	-160.2
	Net Total Score			-137.8	-125.7

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Figure 5. PCB testibility evaluation score sheet with DFT results (score sheet courtesy Rome Air Development Center).

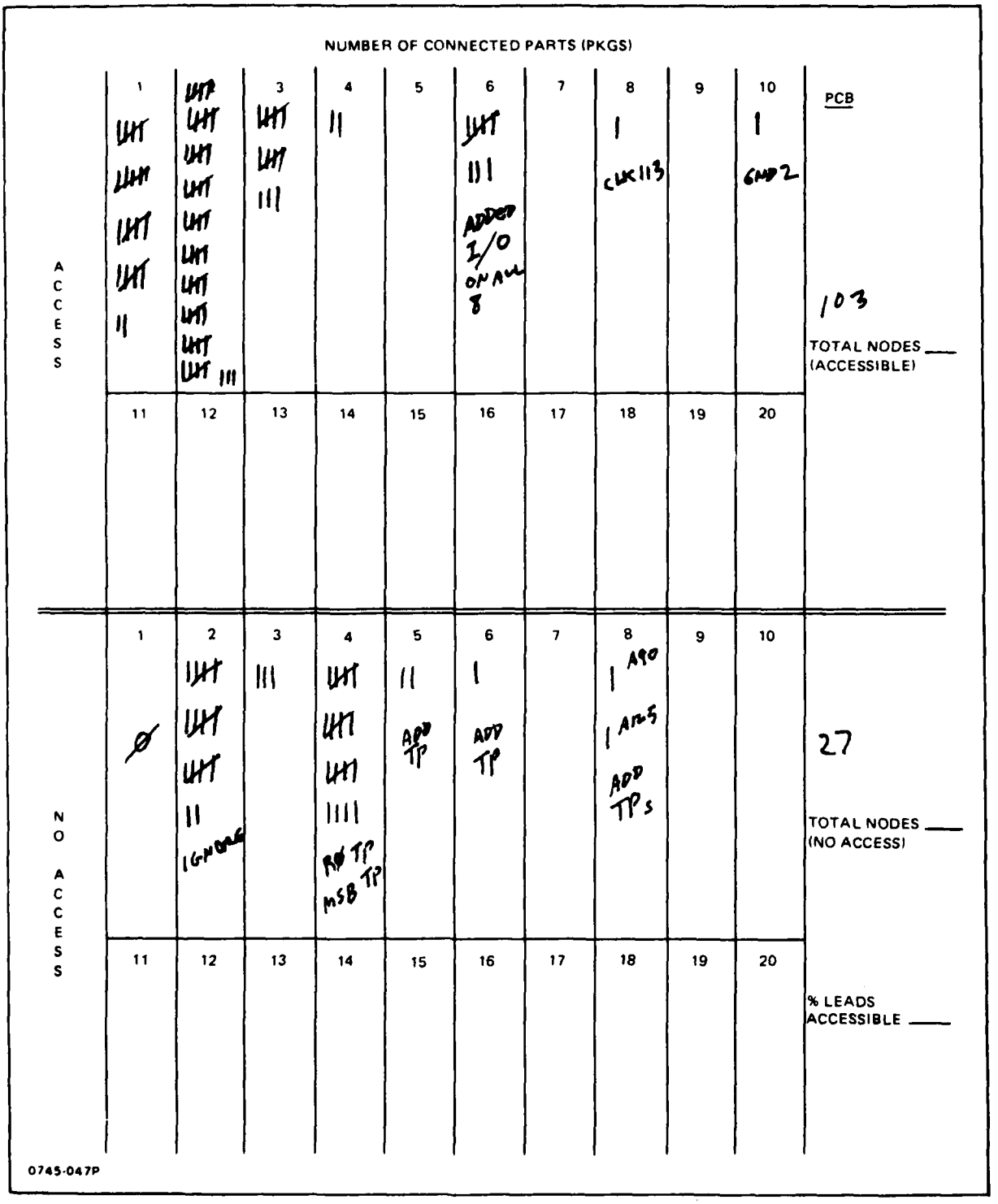


Figure 6. Node accessibility score sheet with DFT results (score sheet courtesy Rome Air Development Center).

functions. Naturally, the embedded fanouts, from three up to eight packages, were more rigorous test challenges.

Northrop wrote a software program for the RADC PCB checklist on the Osbourne microcomputer as an independent research and development (IRAD) project. NOSC agreed to distribute this program (Consolla-Danner Model (CODMOD), to DoD and contractors for easier implementation of the checklist, and NOSC translated the program to an IBM format for more universal use. The CODMOD program performed well on an earlier simple TTL board consisting mostly of combinational gates. The program was difficult for a user to enter and number complex ICs in several items such as Basic 4, Negative 2, and Negative 9. The program mixed the terms "IC packages," "sequential ICs," and "IC type numbers." Users found these terms ambiguous and difficult to understand without making personal assumptions or guessing intended meanings. The RADC list did not have this problem. The flaw in the CODMOD program code was the limit of six or less complex ICs. Since this board had 38 sequential ICs of 12 types, the message "too many complex ICs, must modify program" printed. Clarifying the questions to be more specific and changing computations to allow larger circuits would make the CODMOD software program a useful alternative to filling in checklists and using a hand calculator.

In either case, the user should list and number the complex IC types, inputs, gates, and inverters from chip-specification sheets before going through the PCB checklist. The RADC Node Accessibility Score Sheet, (figure 6) is a useful supplement to the MIL-STD-2165 checklist, which also has questions on fanouts requiring this same circuit evaluation process.

After the DFT modifications were made to the circuit, there was minimal impact on the basic factors, with B1 node accessibility increasing from 38 to 42 and the total basic score moving from 31.5 to 34.5. Since VLSI and microprocessors were included in Basic B4 and Negative N9 items, the DFT improvements impact on scoring will be detailed.

In the N1-30 negative factors, N3 inaccessible node count (only counting 4 or more fanout cases) went from -5.4 to -5.2 and N4 from -5.6 to -5.2. The addition of inputs/outputs to the microaddress 0-7 lines and the microprocessor D1-12 inputs knocked the embedded logic penalty from -.6 to -.1. The added control on clock and tristate to the 2901s changed N19 from -3 to -1, although the clock to other sequential devices was still not controlled. The N24 parallel logic is a serious problem in this circuit, and only tristate and clock (to the microprocessors) of the 14 noted were controlled. Possibly, the inputs/outputs added at microaddress 0-7 lines and data in 1-12 lines allow minor help in some manner. Thus, N24 goes from -35 to -29. Overall, the TFOM changed from -137.8 to -125.7. Due to the built-in "sequential penalties," probably no modern circuit could get above -100, which is considered as "impossible to test without extreme cost penalties."

2.0 LOGIC MODELS

Logic model systems for testability are applicable to analog, digital, or hybrid applications. They can be modeled at the system, subsystem, module, or even component level. An inherent limitation of this broad applicability is that every "item" is a box with inputs and outputs. This means that an AND gate or a motor is the same as a microprocessor. Naturally, the same applies to the importance of the interconnect lines between the "boxes." In other words, the clock or tristate signal lines are no more important to test than one of many input data lines. However, disclosure of the operational design for testability purposes should consider all hardware equally. Once the ambiguity groups are reduced, a weighting of possible test nodes importance can drive the isolation strategy.

Logic models have considerable success and validity other than testability, including logistics, fault isolation, integrated diagnostics, and maintainability. The logic model algorithms are of varying sophistication and validity although the input methodology of dependencies are similar. Both LOGMOD and STAMP claim the exclusive ability to analyze multiple simultaneous failures. The logic model features of inputting failure rate, test times, skill level, or other maintenance goals were not used in this task, but are available in LOGMOD and STAMP.

2.1 LOGMOD

LOGMOD, short for logic modeling, is a computerized maintenance and fault-isolation algorithm, proprietary to DETEX Systems, Inc. Ralph DePaul, the president and founder of DETEX, developed the concept in the early 1960s. The technique was revised to provide testability outputs, which are inherent to the fault-isolation tool methodology. The basic LOGMOD output, from which other data are derived is a structured and organized form of a disciplined knowledge base that contains all interrelationships of functional elements. This structure is commonly shown for small data bases in the form of a graphic staircased dependency chart.

The LOGMOD programs are written in Fortran 77 and may be hosted on any mainframe or minicomputer having a Fortran 77 compiler. In addition, they can be hosted on microcomputers, such as the IBM PC (XT or AT) and the WICAT-150, having suitable memory, compilers, and linkers. Figure 7 shows the WICAT-150 workstation. The WICAT-150 has a Motorola 68000 processor that runs at 8 MHz. Mass storage includes a Winchester disk drive with up to 39 megabytes and a 5-1/4 inch floppy disk drive for backup. DETEX will lease its LOGMOD computer programs for use on computers or work stations similar to those mentioned above at the customer's site. Training is available for users at DETEX. Various services and large companies have used LOGMOD for FI and DFT applications over the years.

Based upon lessons learned from the 1984 LOGMOD circuit modeling, a different method was used to label the components. The initial LOGMOD input of items, signals, and dependencies have to be coded and entered for the basic configuration of interconnects. The LOGMOD dependency input format is basically that an output signal (A#) is formed by the item (I#) and the inputs (A#s) that make up the output. This year, item labeling included chip and pin-number identity

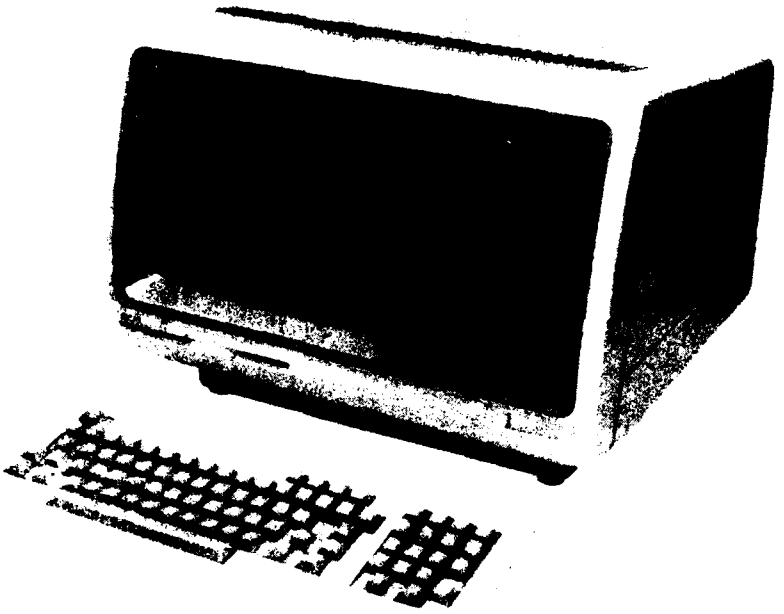


Figure 7. WICAT-150 workstation (courtesy WICAT Systems).

to help quick, schematic correlation. For example, U22 pin 31 was I2231. The program sees each "I number" as a separate item, which makes an eight-output multiplexer appear as eight items instead of one. To obtain a one-to-one correspondence between items and actual components, the entry data were revised to omit the pin numbers. The resultant ambiguity groups then matched the number of components or items in the design, one-to-one.

The initial computer LOGMOD output for the design is a staircased dependency chart whose top is at the upper left. Feedback loops are indicated by horizontal lines projecting to the right. For this complex, five-page schematic, the staircase, or management diagram, was 3.8 feet in height at the top and 19 feet across at the base. The horizontal lines projected indicated the possible involvement of a number of steps to "deloop" the input knowledge base by other LOGMOD software, *automatically combining items. When the knowledge base is successfully delooped* the programs generate the desired testability report.

The LOGMOD testability documentation is greatly broadened in scope and detail compared to the product run for the 1984 TFOM comparison. Figure 8 shows the contents of the delivered LOGMOD testability report. Each section has a user-friendly explanation of the terms, a description of the data, and an explanation of how to use the information. LOGMOD has eliminated some of its unique terms and tried to be more understandable to people who have not been LOGMOD trained. Events that are final outputs of a chain or function were termed "terminal events" by LOGMOD in 1983. Now they are called "system/ equipment performance test requirements or

LOGMOD TESTABILITY REPORT CONTENTS

1) INHERENT FAULT ISOLATION FIGURE OF MERIT
2) AMBIGUITY GROUP RECAP
3) AMBIGUITY GROUP COMPOSITION
4) ITEM INVOLVMENT RATIO(S)
5) MTTI AND MTTR
6) HIERARCHY FOR BIT/BITE CANDIDATES
7) SYSTEM/EQUIPMENT INPUT(S)
8) SYSTEM/EQUIPMENT PERFORMANCE TEST REQUIREMENTS

Figure 8. LOGMOD testability report contents (1985 report).

Section 8." For a quick equipment status, if all the events are good, the entire circuit or system can be considered good, so these must all be on output edge pins On the first model run, 14 internal nodes were used in this section, which pointed out modeling flaws This is a handy, quality assurance check of the model input accuracy. The problems were mostly on two-way signals between the four 2901s, which was corrected by adding some equate terms. LOGMOD is not bidirectional for signal flow without special tricks by the user.

As shown in figure 1, LOGMOD agreed with other TFOMs in the pinpointing of three DFT problem areas. The feedback loop from sheet-5 microprocessors back to sheet 4 and back to the microprocessors was not highlighted by other TFOMs. But LOGMOD delooping focused on this area, so the two lines were broken as a "what if?" game to see the impact on testability. The improvement was significant, so this DFT change was included in all of the TFOMs, even though LOGMOD was the only tool that pointed it out. Due to limited space, all eight sections of the UUT and DFT model outputs are not illustrated in this document. The LOGMOD testability report (not including the dependency graph) is about 40 pages. The inherent fault-isolation figure of merit (IFIFOM) describes the capability to isolate to specific ambiguity group sizes. It is sensitive to feedback loops that require hardware redesign to reduce the ambiguity group size to the fault-isolation goal. Figure 9 shows the UUT and DFT IFIFOM and ambiguity group recaps Notice that the fault isolation to one component increased from 54.9% to 96.1%, and the largest ambiguity group decreased from 140 items (inflated due to device pin numbers) to 10 items in the IFIFOM. The ambiguity group recap is another view of the same data based upon the number of occurrences of each ambiguity group.

INHERENT FAULT-ISOLATION FIGURE-OF-MERIT TABLE (UUT)

AMBIGUITY GROUP SIZE	INDIVIDUAL INDICATOR	CUMULATIVE IND.
1	54.921	54.921
2	.635	55.556
140	44.444	100.000

INHERENT FAULT-ISOLATION FIGURE-OF-MERIT TABLE (DFT)

AMBIGUITY GROUP SIZE	INDIVIDUAL INDICATOR	CUMULATIVE IND.
1	96.129	96.129
2	0.645	96.774
10	3.226	100.000

AMBIGUITY GROUP RECAP (UUT)

AMBIGUITY GROUP SIZE	OCCURRENCE(S)	CUMULATIVE OCC(S).
1	173	173
2	1	174
140	1	175

AMBIGUITY GROUP RECAP (DFT)

AMBIGUITY GROUP SIZE	OCCURRENCE(S)	CUMULATIVE OCC(S).
1	298	298
2	1	299
10	1	300

Figure 9. IFIFOM and ambiguity groups for UUT and DFT.

The beginning of the four-page 140 item UUT printout of ambiguity group items appears at the top of figure 10. Below it is the DFT printout listing the ambiguity groups of 2 and 10 items. The modeling of items with pin number (top) and without pins (bottom) is obvious in these printouts. The misleading ambiguity items of the U8 chip in the 140-item listing is noticeable.

Item involvement ratio is a calculation of the relative testability importance of each ambiguity group to other ambiguity groups given all possible malfunctions. The greater its ratio, the higher the involvement count for the ambiguity group. The top portion of figure 11 shows the original UUT item ratios and the bottom portion shows the results after the DFT modifications. The pages decreased from six to two, again due to the deletion of item pins. The higher counts and leverage values are indications of increased testability.

The 1983 LOGMOD DFT printout information most useful to the design engineer was the "Design Hierarchy for TP Candidates." This listed in top-down sequence the optimum nodes to place test points, including leverage percentage for each. This is a product that is most useful for DFT, replacing the old ad hoc best-guess for where to add test points. The new LOGMOD printout retitles this information "Hierarchy for BIT/BITE Candidates." Every hardware ambiguity group is faulted, forming a set of unique test strategies to isolate faults. A tally is made every time a node is required for observation or measurement. This count of activity provides the leverage value. The top portion of figure 12 shows the first of four pages for UUT test point or BIT candidates. The lower portion shows the total BIT candidate list for the DFT circuitry model. The last two report sections are model inputs and outputs. The DETEX schedule for adding programs to LOGMOD is shown in figure 13.

2.2 STAMP

ARINC Research Corporation has completely upgraded the System Testability Analysis Maintenance Program (STAMP). The program was expanded from a 200-node Apple II version to a 2,048-node test model on a Hewlett-Packard H-P 1000 A900. The H-P 1000 can handle up to 10,000 elements if required. The TFOM measures have increased from 8 measures on the Apple, to 23 measures on the Hewlett-Packard program.

The amplified selection of STAMP TFOMs is described by Dr. Randy Simpson in his AUTOTESTCON-84 paper, "Experience Gained in Testability Design Trade-offs." ARINC retains possession of the software and requires it be used only by ARINC personnel on a government-contract basis. (There are reported modifications to this policy.) Due to coast-to-coast distance, informal basis, and software rehosting, initial data input until final output took several months. The user-friendly printout analysis which was so helpful in last year's DFT comparison, was not available on the H-P 1000 in 1984 and 1985. The new STAMP report does not include a table of contents, but does include a report index. Table 3 lists the 16 header sections. Nine had output data on the complex circuit. Seven were not used.

AMBIGUITY GROUP(S) CONTAINING 140 ITEM(S) (UUT)

	ITEM(S)	ASSOCIATED NODE(S)
I3905	D FF HEX U39	A24 OUT INST BUS 4
I609	D FF OCTAL U6	
I2704	2-IN MUX U27	
I1702	D FF OCTAL U17	
I3513	2-IN NOR U35	
I3815	D FF HEX U38	
I2806	EXCL OR U28	
I839	U8-39 DATABUS 11	
I907		
I832	U8-32 CARRY PROP	
I835	U8-35 CARRY GEN	
I836	U8-36 DATABUS 8	
I837	U8-37 DATABUS 9	
I838	U8-38 DATABUS 12	
I811	U8-11 F=0 OUT	
I319	8-BIT REGISTER	
I131	U1-31 MSB OUT	
I1536	U15-36 DATABUS 4	
I1537	U15-37 DATABUS 5	
I2005	D FF OCTAL U20	
I2511		
I4207		
I133	U1-33 CN+4 OUT	

AMBIGUITY GROUP(S) CONTAINING 2 ITEM(S) (DFT)

	ITEM(S)	ASSOCIATED NODE(S)
I44	DUAL 4-IN MUX	A226 U44-9 OUT
I40	DUAL 4-IN MUX	

AMBIGUITY GROUP(S) CONTAINING 10 ITEM(S) (DFT)

	ITEM(S)	ASSOCIATED NODE(S)
I30	HEX INVERTER U30	A222 U30-10 OUT
I29	EXCL OR U29	
I21		
I1	MICROPROC 2901A	
I25	8-IN MUX U25	
I8	MICROPROC 2901A	
I20	D FF OCTAL U20	
I44	DUAL 4-IN MUX	
I22	MICROPROC 2901A	
I15	MICROPROC 2901A	

Figure 10. High-ambiguity groups for UUT (top) and DFT (bottom).

ITEM INVOLVEMENT RATIO(S) (UUT)

	ITEM(S)	COUNT	LEVERAGE
I51	C9 FILTER +5V1	2	.635
I54	C5 FILTER +5V2	2	.635
I59	R4 +5V2	2	.635
I1808		2	.635
I66	R11 BUFF +5V2	2	.635
I4407		2	.635
I3403	NAND	1	.317
I3411	NAND	1	.317
I3012	HEX INVERTER U30	1	.317
I61	R5 +5V2	1	.317
I50	C7 FILTER +5V1	1	.317
I3805	D FF HEX U38	1	.317
I3810	D FF HEX U38	1	.317
I3812	D FF HEX U38	1	.317
I62	R6 +5V2	1	.317
I52	C8 FILTER +5V3	1	.317
I53	C10 FILTER +5V3	1	.317
I55	C6 FILTER +5V2	1	.317
I3510	2-IN NOR U35	1	.317
I3608	NAND U36	1	.317
I3611	NAND U36	1	.317
I3603	NAND U36	1	.317

ITEM INVOLVEMENT RATIO(S) (DFT)

	ITEM(S)	COUNT	LEVERAGE
I7	PROM U7	14	4.516
I8	MICROPROC 2901A	10	3.226
I15	MICROPROC 2901A	10	3.226
I1	MICROPROC 2901A	9	2.903
I4	PROM U4	8	2.581
I11	PROM U11	8	2.581
I14	PROM U14	8	2.581
I18	PROM U18	8	2.581
I22	MICROPROC 2901A	8	2.581
I32	DEMUX U32	8	2.581
I33	DEMUX U33	8	2.581
I3	8-BIT REGISTER	8	2.581
I6	D FF OCTAL U6	8	2.581
I10	D FF OCTAL U10	8	2.581
I13	D FF OCTAL U13	8	2.581
I17	D FF OCTAL U17	8	2.581
I38	D FF HEX U38	6	1.935
I20	D FF OCTAL U20	6	1.935
I39	D FF HEX U39	6	1.935
I34	NAND	4	1.290
I30	HEX INVERTER U30	4	1.290

Figure 11. LOGMOD item involvement ratios for UUT and DFT. Portion of seven-page listing for UUT at top. Portion of three-page listing for DFT at bottom.

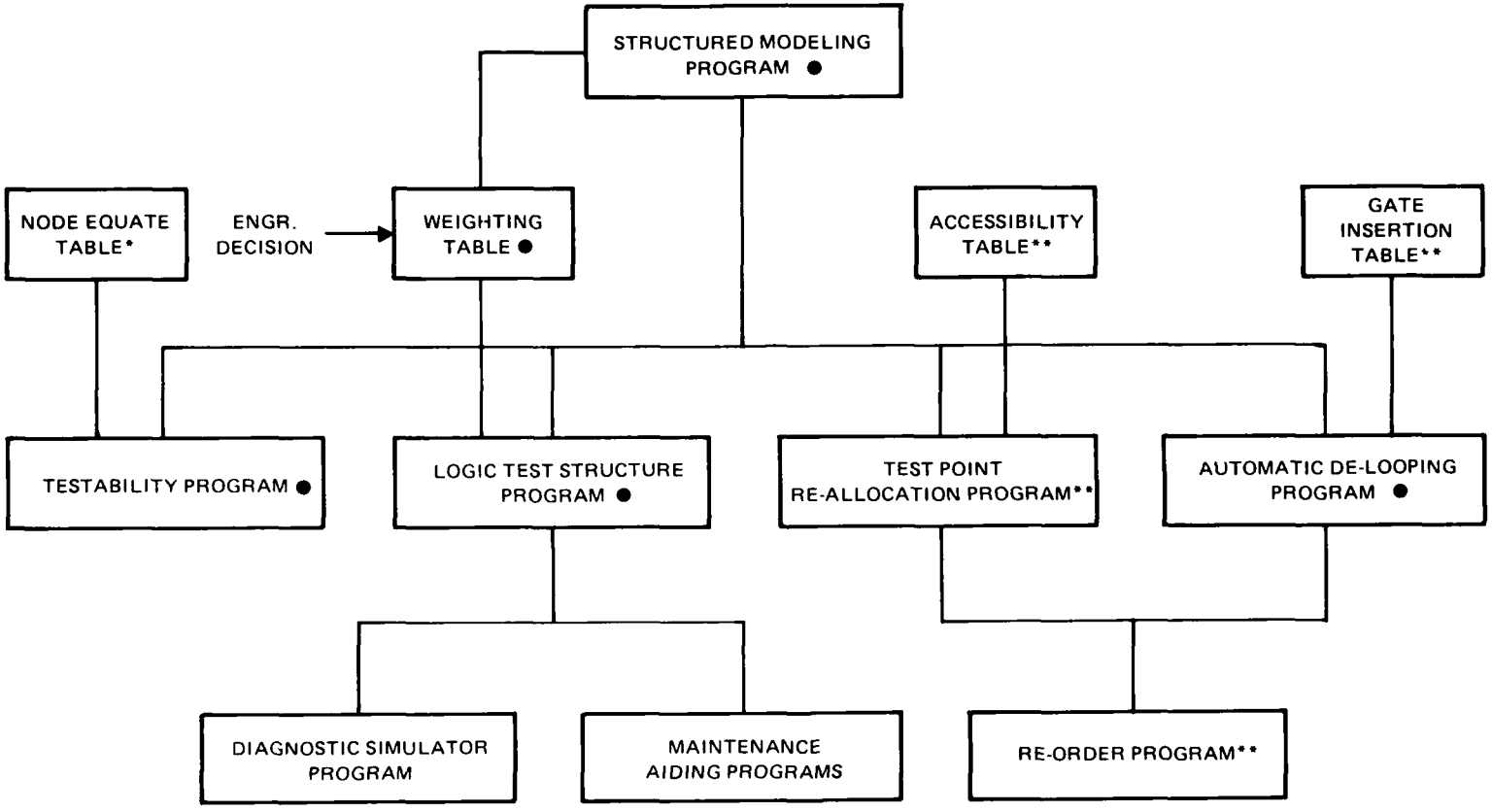
HIERARCHY FOR BIT/BITE CANDIDATES (UUT)

NODE	TITLE	COUNT	LEVERAGE
A3	GND 2	310	2.796
A379		276	2.489
A24	OUT INST BUS 4	275	2.480
A374		246	2.219
A161	U34-6 RESET OUT	237	2.137
A250	U32-7 OUT	235	2.119
A254	U33-12 OUT	234	2.110
A2	GND 1	197	1.777
A255	U33-11 OUT	185	1.668
A136	U34-3 OUT	179	1.614
A227	U22-11 F=0 OUT	175	1.578
A135	GND 3	170	1.533
A31	IN MEM DATA 3	168	1.515
A37	IN MEM DATA 2	168	1.515
A40	IN MEM DATA 1	168	1.515
A56	IN SENS 2	168	1.515
A62	IN SENS 1	168	1.515
A30	IN MEM DATA 4	167	1.506
A32	IN MEM DATA 11	167	1.506
A33	IN MEM DATA 9	167	1.506
A34	IN MEM DATA 10	167	1.506
A35	IN MEM DATA 8	167	1.506

HIERARCHY FOR BIT/BITES CANDIDATES (DFT)

NODE	TITLE	COUNT	LEVERAGE
A141	C7 PATH	88	4.772
A58	TP I6	65	3.525
A222	U30-10 OUT	60	3.254
A266	U12-9 OUT	45	2.440
A90	TP DA	43	2.332
A704	MP CLOCK	39	2.115
A55	TP I5	35	1.898
A136	U34-3 OUT	33	1.790
A219	U30-2 OUT	32	1.735
A263	U9-7 OUT	32	1.735
A124	TP 12	31	1.681
A103	TP 14	29	1.573
A121	TP 18	29	1.573
A701	TRISTATE	28	1.518
A140	+5V2 PULL UP	27	1.464
A106	TP 10	26	1.410
A175	+5V3	25	1.356
A118	TP 17	24	1.302
A705	MP CLOCK	24	1.302
A265	U12-7 OUT	23	1.247
A76	TP A2	20	1.085
A95	TP CNA	20	1.085

Figure 12. LOGMOD hierarchy of BIT/BITE candidates for UUT and DFT. Portion of four-page listing for UUT at top. Portion of one-page listing for DFT at bottom.



NOTES

● PRESENTLY AVAILABLE IN LOGMOD PROGRAMS
*LOGMOD PROGRAMS PRESENTLY IN PROCESS
**LOGMOD PROGRAMS PLANNED FOR COMPLETION IN 1986
□ OPTIONAL LOGMOD PROGRAMS

Figure 13. DETEX schedule for adding programs to LOGMOD.

Table 3. STAMP report index of sections.

Redundancy Table

Ambiguity Table

Subsignature Table

Testability Measures

Feedback Loops

Excess Tests

Fault-Tree Input

Untestable Tests*

Known Good Tests*

Known Bad Tests*

Consistency Checks*

Associated Test Groups*

Forced Path*

Weighting*

Component Ambiguity Groups

Fault-Tree Table

All Done Statistics Path = 3604. Num = 130. Avg = 27.723. Max Path = 71. Min Path = 3.

* Not used

Several parts of the printout provided unexpected benefits to designers. One portion, called "ambiguity table components" (figure 14), included a list of 45 items that were RTOK (retest ok). This list of other components in the printout provides a quality control (QC) feature for the dependency inputs. The listed components were not observed in the total observability model, because these items (primarily filter capacitors or edge pins) were not included in the dependency inputs. This means that they should either be added to the dependencies or deleted from the model as extraneous. This is a useful input QC to check input accuracy, not provided by some other TFOMs. STAMP is the only TFOM to tackle the false-alarm problem in its circuit analysis. This is an important field problem in current technology systems.

Another useful DFT output was the list of "other tests." These were signals that were duplicative and, if on edge pins, could provide possible edge pins to use for additional observable test points when needed. On the total observability model there were many tests, which is to be expected in such an idealistic input (an observable point at every output pin of every device). Surprisingly, three "other tests" were retained on the "actual pin" model. Two turned out to be model input errors and the third was one of three ground pins tied together for the third +5 volt sources ($+5V_3$). This provided another model QC check. The 2-line printout of 23 TFOM measures required considerable verbal clarification by ARINC staff.

The TFOM outputs challenged the goal of not using fault isolation (FI), diagnostics, and other field-user parameters in this up-front "design testability" analysis. The 23 TFOM measures listed in table 4 include 6 multiple-failure-situation outputs in addition to the single-fault measures. Since the STAMP printout includes them, and they are of use to a DFT engineering analysis, the single-fault and multiple-fault FOMs are all included in this section

Briefly, the measures with hidden failure (HF), false failure (FF), and false alarm tolerance (FAT) are multiple-failure items. When completed, the new STAMP will include analysis of the FOMs, graphic fault-tree and failure-analysis outputs, automated failure-mode effects criticality analysis (FMECA) for single and multiple faults, and component grouping Longer range 1986 STAMP plans include CAD/CAM front-end interface. The 160-characters-per-second printer was a 1985 limitation in the H-P 1000 STAMP, but a 400-lines-per-minute printer is being sought in 1985.

ARINC is also developing an extension of STAMP to be used as a fault-isolation maintenance aid. The Weighted Repair Assistance Program-Learning Extension (WRAPLE) is the prototype program.

Although LOGMOD and STAMP both print out "fault trees," the STAMP printout of "fault-tree table" (figure 15) columns of step #/test #, good step #, and "bad" item or component group were easier to understand than the "waterfall" tree of dependency events printed out by LOGMOD, unless a user had attended a LOGMOD training class.

Testability Report

File Name: NOSTE
File Description: TEMP
File Date: 04/03/85

Redundancy Table

Test	Other Tests
A376	A79
A238	A218
	A275
	A276
	A277
	A278
	A280
	A217
	A220
	A221
	A222
	A223
	A225
	A281
	A285
	A286
A226	A101

Ambiguity Table

Comp	Other Comps
I4	I11
	I12
	I1303
	I14
	I15
	I16
	I18
	I19
	I2009
	I21
	I23
	I24
	I25
	I32
	I33
	I40
	I41

Figure 14. STAMP report printout of redundancy and ambiguity tables.

Table 4. Summary of STAMP UUT and DFT TFOM outputs.

Measure	Original UUT		Modified DFT
Isolation Level (IL)	.3299		.8620
Feedback-Modified Isolation Level (FMIL)	.5485		.8944
Test Leverage (TL)	.3173		.9321
Nonredundant Test Leverage (NRTL)	.2919		.8937
Feedback-Modified Test Leverage (FMTL)	.4852		.9296
Test Uniqueness (TU)	.9200		.9587
Test Redundancy (TR)	.0800		.0413
Test Feedback Dominance (TFBD)	.0880		.0437
Component Feedback Dominance (CFBD)	.4010		.0407
Nondetected Percentage (ND)	.1904	NDP	.1018
Hidden-Failure Measure (HF)*	.148	HFM	.5455
Input-Modified Hidden-Failure Measure (IMHF)	.048	IMHFM	.4410
Percent Hidden-Failure Measure (SHF) PHFM*	.0224		.0405
Input-Modified Percent Hidden-Failure Measure (MSHF) IMPHFM*	.0017		.0197
False-Failure Measure (FF) FFM*	.0357		.0000
Input-Modified False-Failure Measure (IMPF) IMFFM*	.0400		.0000
Dependency (D) DEP	.3071		.0613
Test Interdependency (TI) TIDEP	.2534		.0587
Test Dependency (TD) TDEP	.3242		.0587
False-Alarm Tolerance (FAT)*	.2555		.0588

* multiple-fault FI measures

Table 4. Summary of STAMP UUT and DFT TFOM outputs (Continued)

Measure	Original UUT	Modified DFT
Theoretical Minimum TL (THEOMINTL)	.0219	.0199
Theoretical Maximum TL (THEOMAXTL)	.9975	.9977
External Dependency (ED)	.1066	EXPD .1900

* multiple-fault FI measures

```
Test  103   Label = (TE103)  A276
Dependencies:
(TE3)     A2              (TE187)  A285          (TE266)  A55
(TE267)   A103            (TE269)  A124          (TE279)  A106
(TE365)   A700            (TE366)  A703          (TI27)   A67
(TI43)    A8264           (TI44)   A8265         (TI45)   A8266
(TI72)    A8234           (TI73)   A8235         (TI78)   A8263
(CP169)   I835

Test  104   Label = (TE104)  A288
Dependencies:
(TE3)     A2              (TE132)  A219          (TE266)  A55
(TE267)   A103            (TE269)  A124          (TE271)  A121
(TE273)   A58             (TE279)  A106          (TE365)  A700
(TE366)   A703            (TI27)   A67           (TI72)   A8234
(TI73)    A8235           (CP158)  I821

Test  105   Label = (TE105)  A291
Dependencies:
(TE3)     A2              (TE306)  A57           (TE307)  A66
(TE308)   A76             (TE309)  A59           (TE310)  A81
(TE311)   A99             (TE312)  A51           (TE313)  A54
(TE365)   A700            (TE366)  A703          (TI27)   A67
(CP157)   I809

Test  110   Label = (TE110)  A283
Dependencies:
(TE3)     A2              (TE187)  A285          (TE266)  A55
(TE267)   A103            (TE269)  A124          (TE279)  A106
(TE365)   A700            (TE366)  A703          (TI27)   A67
(TI43)    A8264           (TI44)   A8265         (TI45)   A8266
(TI72)    A8234           (TI73)   A8235         (TI78)   A8263
(CP165)   I811

Test  111   Label = (TE111)  A369
Dependencies:
(TE3)     A2              (TE132)  A219          (TE266)  A55
(TE267)   A103            (TE269)  A124          (TE271)  A121
(TE273)   A58             (TE367)  A701          (TE368)  A704
(TI27)    A67             (TI72)   A8234         (TI73)   A8235
(CP172)   I1516

Test  112   Label = (TE112)  A370
Dependencies:
(TE3)     A2              (TE306)  A57           (TE307)  A66
(TE308)   A76             (TE309)  A59           (TE310)  A81
(TE311)   A99             (TE312)  A51           (TE313)  A54
(TE367)   A701            (TE368)  A704          (TI27)   A67
(CP173)   I1508

Test  113   Label = (TE113)  A277
Dependencies:
(TE3)     A2              (TE188)  A286          (TE266)  A55
(TE267)   A103            (TE269)  A124          (TE279)  A106
(TE367)   A701            (TE368)  A704          (TI27)   A67
(TI46)    A8267           (TI47)   A8268         (TI48)   A8269
(TI49)    A8270           (TI72)   A8234         (TI73)   A8235
(CP181)   I1532
```

Figure 15. STAMP dependency list printout.

The "ambiguity table" (figure 14) had one item, a +5V resistor, with the highest count (157) of "other components." The next highest ambiguity number item was another +5V resistor, with 75 components. Twenty-seven other items had only one or two components.

The "subsignature table" (figure 16) listed 39 components with 84 "other components." This large table needs to be filtered for related or high-frequency failure items to aid the circuit design. Otherwise, it lumps 39 signals into a large ball that would require annotating all of them on a schematic, then trying to break it up, as with a feedback loop. Of course, due to the chip-pin identity, the 84 "other components" signals are really on 24 hardware components. "Feedback loops" has one big loop with 11 A#s and 158 I#s, which is 49 hardware items. The "component ambiguity groups" listed 29 ambiguity groups, mostly consisting of 2 or 3 components, but there were two large groups. "Group 1" listed 76 components (47 hardware pieces) and "group 92" listed 158 lines or 49 hardware items.

The UUT and DFT STAMP output TFOMs are summarized in table 4. The 23 STAMP outputs can be somewhat esoteric when printed on the STAMP printout. Published articles by Dr. Simpson and personal memos and conversations with ARINC personnel have been used to briefly explain the outputs and their meaning on this particular complex circuit. Figures 17 and 18 show the STAMP TFOM printout for UUT and DFT models, respectively. The full H-P 1000 STAMP testability report generator is expected to have 300 rules in the program, based upon these 23 output TFOMs. These outputs are categorized under the headings of single-failure, multiple-failure, and internal measures. Groups of two or three describe the same function from different viewpoints and will be grouped accordingly.

Single-Failure Measures

a. Isolation Level (IL) (previously termed component leverage) and Feedback-Modified IL (FMIL) work together and vary from 0 to 100%. The original UUT can isolate (IL) 33% of the component groups due to feedback loops, and ambiguities outside of feedback loops increase the FMIL to 55%. Note that the breaking up of feedback loops raised the IL to 86%.

b. Test Leverage (TL) (previously termed test point leverage), Nonredundant Test Leverage (NRTL), and Feedback-Modified Test Leverages (FMTL) correlate and vary from zero to infinity. TL is a ratio of the number of tests to the number of elements. The 32% UUT TL is reasonable and increases to 93% by the addition of test points, called tests in STAMP. There were only about 3% redundant tests, the difference between NRTL and TL. The UUT FMTL is one-third larger than TL when feedback-loop redundancies are removed. The TL and FMTL for DFT are nearly equal, so that any redundant tests are outside of feedback loops. Note that FMTL doubled test leverage in the DFT board.

Subsignature Table

Comp	Other Comps
I1006	I2903
	I3704
	I344
	I4305
I1005	I2903
	I3704
	I343
	I4305
I1002	I2903
	I3704
	I342
	I4305
A807	I300
	I2207
A809	I297
	I2409
A810	I314
	I1209
A808	I299
	I2309
A811	I303
	I1609
I1009	I2903
	I3704
	I345
	I4305
A812	I304
	I1607
I1012	I2604
	I2607
	I2609
	I2612

Figure 16. STAMP subsignature table printout.

```
                    I322
                    I323
                    I324
                    I325
                    I326
                    I57
                    I76
                    I81
                    I99
                    I2612
                    I3012
                    I3403
                    I3805
                    I3810
                    I3812

*I3805              I54
                    I2612

*I3810              I51
                    I76

*I3812              I66
                    I99
```

SUBSIGNATURE TABLE (64 PAGES LONG, DOZEN 1-PAGE EACH)

* Leading asterisk indicates a False Failure indication is possible

PIN OBSERV MOSC SYSTEM 2 DEC

DEC 84

Testability Measures

IL	FMIL	TL	NRTL	FMTL	TU	TR	TFBD	CFBD	NDP
.3299	.5485	.3173	.2919	.4852	.9200	.0800	.0880	.4010	.1904
PHFM	IMPHFM	FFM	IMFFM	DEP	TIDEP	TDEP	FAT	THEOMINTL	THEOMAXTL
.0224	.0017	.0357	.0400	.3071	.2534	.3242	.2555	.0219	.9975

Feedback Loops

Loop	Tests and/or Comps
1	A153
	A166
	A167
	A171
	A172
	A173
	A174
	A78
	A77

(1 LOOP WITH 3 PAGES OF I# A#)

Figure 17. STAMP UUT TFOM report printout. Note portion of subsignature table at top.

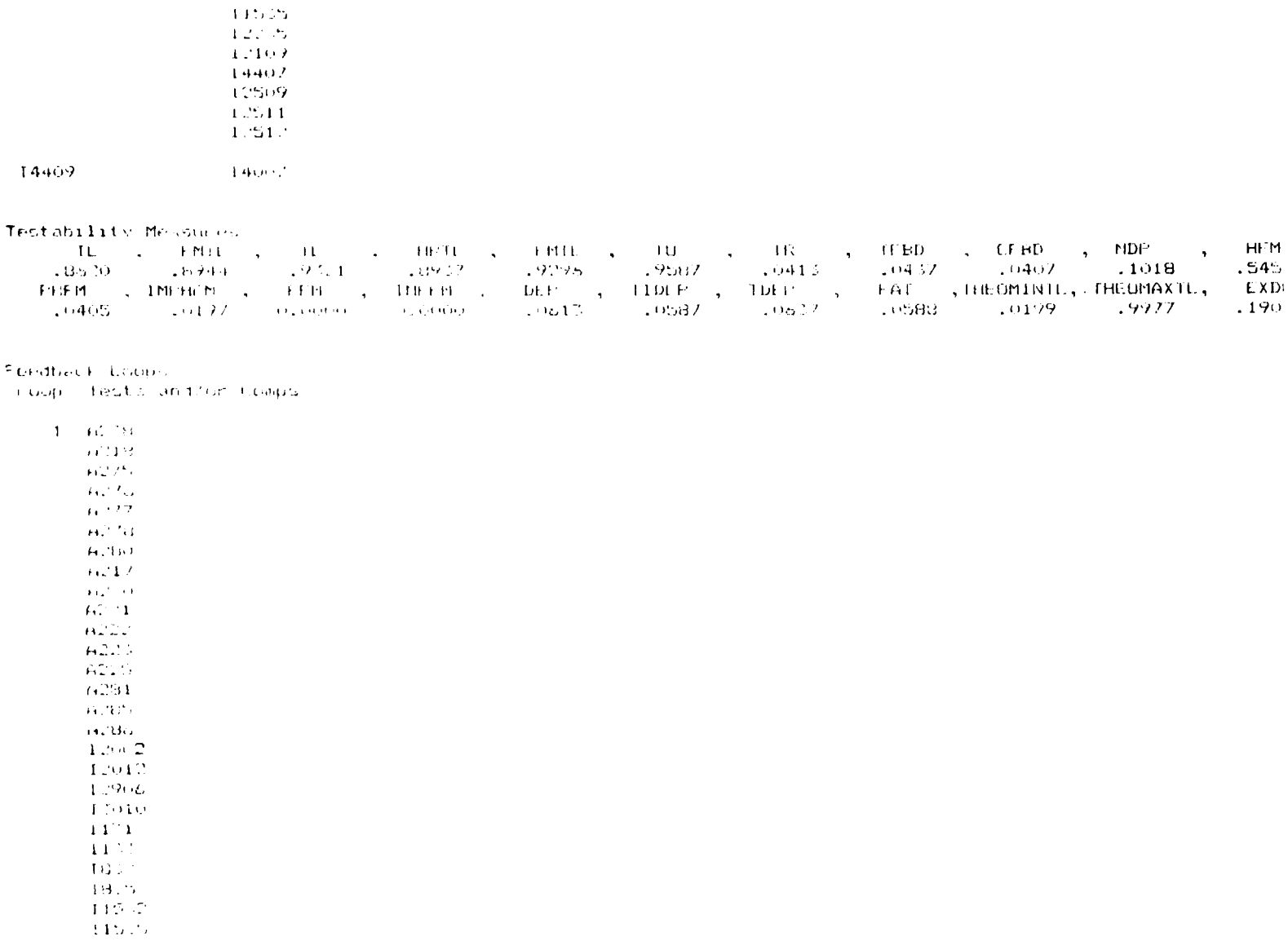


Figure 18. STAMP DFT TFOM report printout. Note portion of subsignature table at top.

c. Test Uniqueness (TU) and Test Redundancy (TR) vary from 0 to 100% and are complementary to each other. Note that TR decreased from 8% to 4% on the DFT board. Nearly 96% is close to the ideal TU of 100%.

d. Test Feedback Dominance (TFBD) and Component-Feedback Dominance (CFBD) indicate the percentage of tests or components tied up in feedback loops. The TFBD decreased from 8% to 4% after loops were broken up. The percentage of components in feedback loops decreased sharply from 40% to only 4% in the DFT circuit.

e. Nondetection Percentage (NDP) is a straightforward percentage of components not tested, which is similar to test coverage. NDP decreased from 19% to 10% in the DFT circuit.

f. External Dependency (ED) is a ratio of the number of circuit inputs to the number of elements, which correlates with fault isolation. The ED increase from 10% to 19% is a "penalty" of possible external fault sources by adding test points.

Multiple-Failures Measures

These measures include all "mathematically" possible occurrences and should be pruned by the engineer to include only related or high-failure pairs. Only the last two cases are significant to fault isolation.

a. Hidden-Failure Measure (HFM) and Input-Modified HFM (IMHFM) give the percentage of elements that can have multiple or hidden failures. The addition of a special test to unmask the hidden failure would appear as a redundant test TR, but is needed for the multiple-failure situation. IMHFM is smaller because it eliminates inputs, which are independent of the circuit. The HFM increase from 15% to 55% for the DFT circuit is not good, but is a trade-off for high single-failure fault isolation. The high HFM will have little impact on maintainability in this circuit. Even with the inputs deleted, 44% of the elements, if failed, could have hidden failures, up from 4% on the UUT.

b. Percent Hidden-Failure Measure (PHFM) and Input-Modified PHFM (IMPHFM) measure what percentage of elements are hidden by a failure. PHFM increased from 2% to 4% for the DFT circuit. By not including inputs, IMPHFM decreased to .0017, which increased over a factor of 10 to 1.9% for the DFT. Inputs were included because failures may take out inputs in a multiple-failure chain

c. False-Failure Measure (FFM) and Input Modified FFM (IMFFM) are the percentage of multiple-failure items that could indicate that a different (good) element had failed. It is the ratio of the number of false-failure combinations to the number of elements that can be falsely identified. The DFT changes took both values to zero, which means a low false-alarm rate and good field testability

Internal Measures

a. Dependency (DEP) is a measure of the density of higher order dependencies and, along with the next two measures, predict test-program set difficulties. Test Interdependency (TIDEP) measures the functionality of testing, and Test Dependency (TDEP) measures component loading on the average test. The 7% spread between TIDEP and TDEP on the UUT indicates that additional testing is badly needed. The decrease to 1.5% for the DFT indicates that the right things were done. Note that DEP always lies between TIDEP and TDEP values and DFT values on ambiguities decreased from 25-32% to about 6%, for good fault isolation.

b. False-Alarm Tolerance (FAT) tries to indicate false alarms by downstream dependencies or feeds or the number of tests available to confirm a failure. Since a larger FAT value helps avoid false alarms, the decrease in FAT from 25% to under 6% by eliminating feedback loops means the DFT system is less FA tolerant.

c. The last two of the 23 STAMP measures are Theoretical Minimum TL (THEOMINTL) and Theoretical Maximum TL (THEOMAXTL). If exceeded, these indicate that tests are underspecified or overspecified, respectively. It is uncommon that either value would be exceeded by TL numbers, but an AUTOTESTCON example has TL exceed maximum TL.

If the 23 STAMP TFOMs seem exhaustive, an ARINC presentation on STAMP testability analysis also discussed "component leverage" as the percentage of components being uniquely fault-isolatable (observability) and "test point leverage" as a relative measure of the degree to which the test point set meets theoretical fault-isolation limits (controllability). Modified values were also listed, and these are in the 23 current STAMP TFOMs. TL is the same measure as test point leverage, but the algorithms differ, as they do for component leverage and IL values.

3.0 CAE WORKSTATION SCOAPS

The Sandia Controllability/Observability Analysis Program (SCOAP) algorithm performed well in the previous comparison, but had library CMOS primitive model limitations. Some CAE workstation vendors are including modified versions of SCOAP in their software packages for up-front testability analysis of CAD/CAE designs. Daisy workstations include the Daisy Testability Analyzer (DTA) package, and GE/CALMA workstations include the Controllability-Observability-Predictability-Testability Report (COPTR) package. Both have improved the basic SCOAP with top-down modeling and large device-model libraries of common IC types. Unfortunately, due to prerelease software, entry errors, or lack of entry documentation, the initial DTA and COPTR reports were invalid and could not be used to select DFT revisions. Later on, successful DTA and COPTR numbers and outputs were produced, details of which are in this section.

In mid-1985, after COPTR and DTA analyses were completed, GenRad released a HITAP software that also had controllability/observability (C/O) outputs, but it was too late to be included in this analysis. HITAP uses the same image description as HILO-3 and should run on the same workstations or VAX CPU. Since HITAP is based upon the Computer-Aided Measure For Logic Testability (CAMELOT) algorithm, the C/O outputs are not broken down into sequential and combinational.

3.1 DAISY DTA

Daisy Systems Corporation features the "Logician" CAD/CAE desk top workstation shown in figure 19. The Logician brain is an 8-MHz Intel 80286 16-BIT microprocessor. Local memory includes up to 16 MB dynamic RAM, 40 MB Winchester disk on-line (80 MB optional), and a 1-MB floppy disk. The operating system is the UNIX-like MAESTRO system. Table 5 lists the Daisy CAD/CAE software used in this schematic capture and testability analysis. The process used separate Logician graphic editors for components and drawings, with postprocessing by DANCE, DRINK, SIFT, and SOM software. Validation by the Daisy logic simulator program (DLS) ensures the design is ready for the Daisy Testability Analyzer (DTA) run. Figure 20 shows the Daisy Testability Analyzer processing flow.

The DTA is an improved and upgraded version of the SCOAP C/O algorithm. Table 6 lists the major SCOAP output measures. The DTA has a top-down functional capability, but due to the lack of partitioning or functional breakdown of the design, as shown in figure 1, it was inputted as a flat schematic. The Daisy model library was complete, and a functional model of the 2901 microprocessor was used in the DTA analysis. Complex models of some CAE vendors will not play on SCOAP-like programs due to SCOAP gate-level model limitations. The Daisy DTA will allow functional models, not necessarily at the gate level. The DTA demonstrated a powerful QC capability by detecting a drafting error in the drawing for the 54377 D-flip flop. The government circuit schematic showed a "clear," which the Daisy SIFT program stated could not toggle due to its connection to ground. The chip documentation verified that the drawing should have had "enable" at pin 1, which would then function normally. No other TFOM tool detected this drawing mistake.

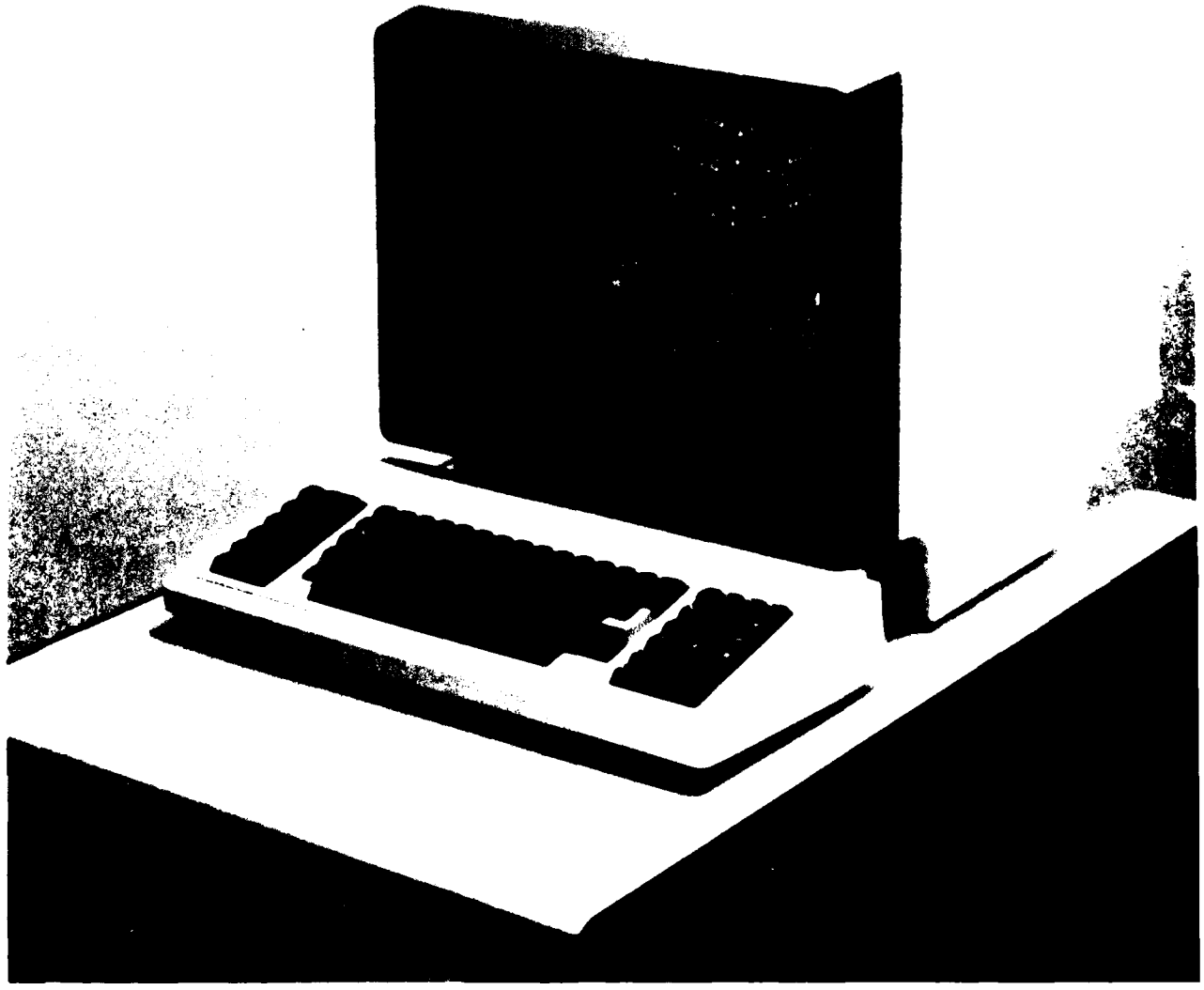


Figure 19. Daisy LOGICIAN workstation (courtesy Daisy Systems Corporation).

Table 5. Daisy CAD/CAE software

Software	Function
Daisy Network Connectivity Extractor (DANCE)	Syntax check and compiler.
Daisy Logic Simulator (DLS)	Validates design for DTA run
Daisy Revolving Linker (DRINK)	Syntax/connect hierarchy tree design.
Logician Component Editors	Produce component elements. graphics. parameters. pins.
Logician Drawing Editor (DED)	Create. modify block schematics. blocks. wires. bundles. components.
Simulator Intermediate File Translator (SIFT)	Assign names and timing.
Simulator's Object Module (SOM)	Label clock. inputs. Initialize.

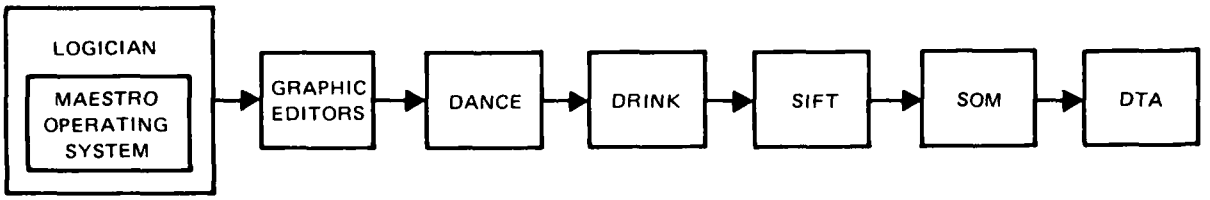


Figure 20. Daisy testability analyzer flow.

Table 6. SCOAP testability output values used in DTA and COPTR analysis.

CCØ	Combinational controllability of 0 state
CC1	Combination controllability of 1 state
SCØ	Sequential controllability of 0 state
SC1	Sequential controllability of 1 state
CO	Combinational observability
SO	Sequential observability

The initial DTA run was invalid with a large percentage of high number values on many nodes, but this was corrected later by changing a chip model and running a newer release of software. A problem with chip "internal nodes" printing also was experienced. It was desired at the board level to have only device-output nodes or edge pins observed, and this was done fairly well in later DTA runs. Unfortunately, the circuit DFT modifications had to be made before the final software release good runs, but the DTA outputs effectively pointed out nodes hard to control or observe and optimum test point locations.

The technique of entering the DFT revisions into DTA, such as adding inputs/outputs to break feedback loops before and after the 2901s, was easy. It consisted of small macro-edit lines, which can be added or deleted from the circuit easily. The ease of "what if?" analysis was favorable to interactive design modifications by the user. In fact, the changes were so friendly, a 54155 MUX chip was inserted as a "test" to break up and control the clock and tristate signals to the four 2901s. Figure 21 shows this CAD DFT change. Three separate gates or "items" were used to implement this on other tools. Naturally, adding a MUX chip would be the "real world" DFT approach, rather than the brute force approach of gates or switches for each 2901.

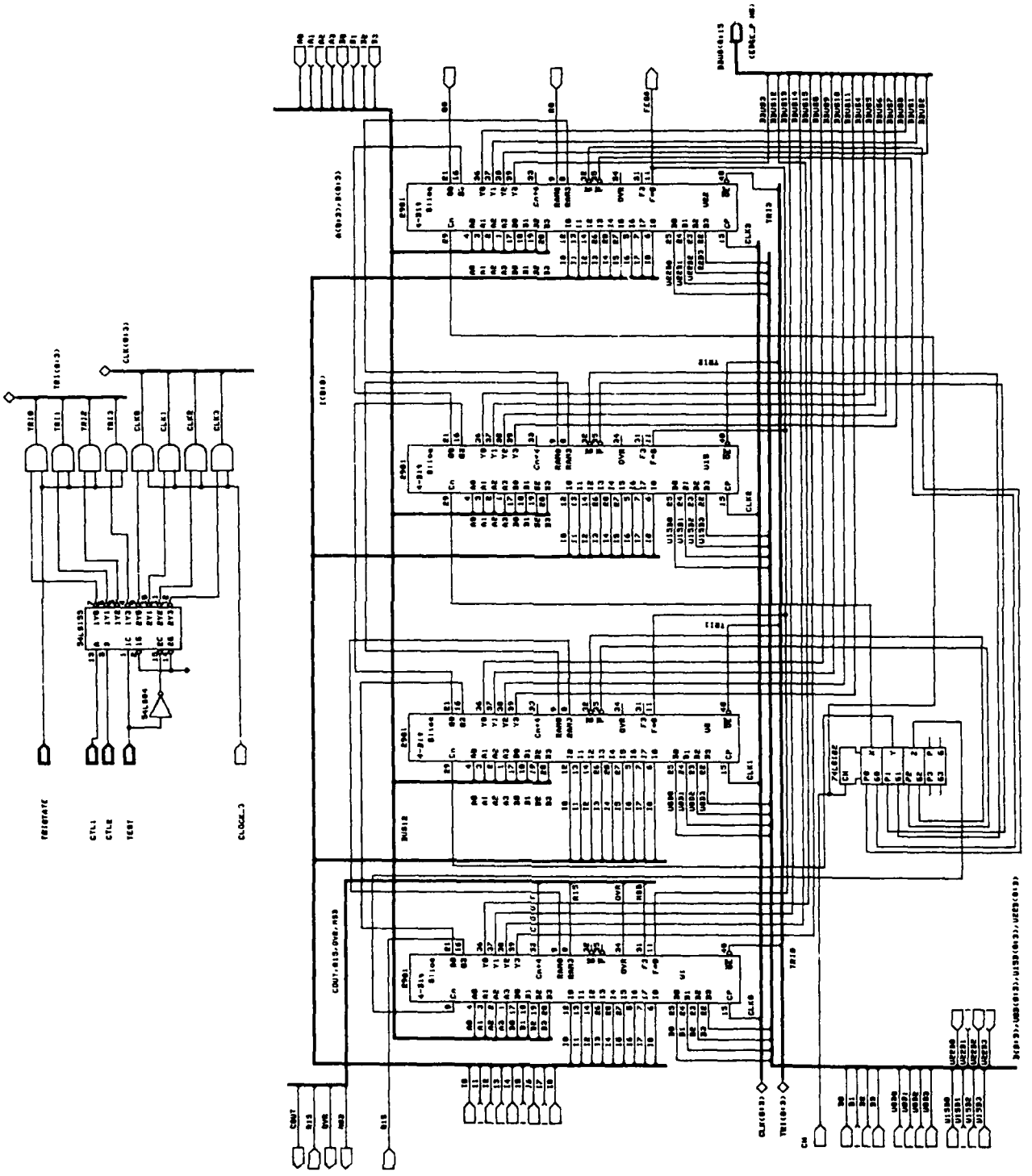


Figure 21. Daisy CAD with 54155 MUX added for clock and tristate control on microprocessors.

Figure 22 shows the summary C/O values for the initial UUT circuit, next the changes in values for the "manual" DFT version, and finally, the Daisy "optimal" DFT results.

The DTA has four options: "auto-insert" and "manual-insert" determine how the test changes are entered; "R-option" and "S-option" determine printout format.

1. "Auto-insert" analyzes the results of inserting a test point at each node. The operator must first specify how many test points are desired. Each node is analyzed individually and takes about a minute. In a complex circuit like this, with thousands of possible nodes, this takes up some CPU time. For example, the "auto-insert" of five test point nodes ran overnight. This is a very powerful tool though, since it would take months for an engineer to analyze the total circuit C/O impact of a test point at each separate node. The results are impressive considering only five test points were used for the optimal printout.

2. "Manual-insert" was run for comparison with the other DFT tools, using the same "benchmark" DFT changes. The DTA output did show tremendous improvements in the circuit testability

3. The "R-option" is the normal printout format and packs the information into a few pages. Figure 23 shows the "R-option" with the C/O values for individual nodes.

4. The "S option" sorts by C/O values in ascending numerical values, of one C/O value For all six C/O variables, six reports would be required. This would be desired if only one C/O value was of interest.

Comparison of the manual option and automatic option testability node differences is interesting as to the target nodes and design approaches. The "optimal input/output points" and correlation with the manual DFT modifications are as follows.

1. Auto-insert I3: same feedback break points were done manually.

2. Auto-insert XSIG41: input line to the MUX with microaddress 0-7 out, which was manually broken.

3. Auto-insert XSIG40: same as (2).

4. Auto-insert XSIG22: signal drives I5 to the 2901s, which was a feedback manually broken.

5. Auto-insert XSIG20: signal drives I3, similar to the first I3 auto-insert.

**** DTA TESTABILITY REPORT ****

	MAXIMUM VALUE	COUNT MAX VAL	AVERAGE VALUE	% IMPROVEMENT	COUNT UNTESTABLE
COMBINATIONAL Ø-CONTROLLABILITY (CCØ)	1ØØ4	2	98	Ø	3
COMBINATIONAL 1-CONTROLLABILITY (CC1)	1Ø98	2	236	Ø	3
SEQUENTIAL Ø-CONTROLLABILITY (SCØ)	3Ø	2	3	Ø	3
SEQUENTIAL 1-CONTROLLABILITY (SC1)	38	3	8	Ø	3
COMBINATIONAL OBSERVABILITY (CO)	3857	1	74Ø	Ø	21
SEQUENTIAL OBSERVABILITY (SO)	117	2	24	Ø	21
MEAN	-	-	179	Ø	-
STANDARD DEVIATION	-	-	156	Ø	-

**** DTA MANUAL TESTABILITY REPORT ****

	MAXIMUM VALUE	COUNT MAX VAL	AVERAGE VALUE	% IMPROVEMENT	COUNT UNTESTABLE
COMBINATIONAL Ø-CONTROLLABILITY (CCØ)	116	2	13	88	3
COMBINATIONAL 1-CONTROLLABILITY (CC1)	139	3	16	94	3
SEQUENTIAL Ø-CONTROLLABILITY (SCØ)	8	4	1	79	3
SEQUENTIAL 1-CONTROLLABILITY (SC1)	12	3	1	9Ø	3
COMBINATIONAL OBSERVABILITY (CO)	1385	1	57	93	21
SEQUENTIAL OBSERVABILITY (SO)	57	1	4	85	21
MEAN	-	-	15	92	-
STANDARD DEVIATION	-	-	19	88	-

THE MANUAL INSERT (INPUT OUTPUT I/O) NUMBER IS (16 2 26)

**** DTA OPTIMAL TESTABILITY REPORT ****

	MAXIMUM VALUE	COUNT MAX VAL	AVERAGE VALUE	% IMPROVEMENT	COUNT UNTESTABLE
COMBINATIONAL Ø-CONTROLLABILITY (CCØ)	21Ø	3	27	71	3
COMBINATIONAL 1-CONTROLLABILITY (CC1)	28Ø	3	38	83	3
SEQUENTIAL Ø-CONTROLLABILITY (SCØ)	16	2	1	69	3
SEQUENTIAL 1-CONTROLLABILITY (SC1)	14	3	2	75	3
COMBINATIONAL OBSERVABILITY (CO)	7Ø5	2	154	81	21
SEQUENTIAL OBSERVABILITY (SO)	57	1	9	67	21
MEAN	-	-	37	8Ø	-
STANDARD DEVIATION	-	-	53	66	-

Figure 22. DTA output measures for UUT (top), manual DFT (middle), and automated DFT (bottom).

	CC0	CC1	SC0	SC1	CO	SO
@DESIGN 1:~~U11G~~	~~219~~	~~487~~	~~6~~	~~14~~	~~-1~~	~~-1~~
@DESIGN 1:COUT	219	461	6	13	1234	34
@DESIGN 1:OVR	219	804	6	27	451	14
@DESIGN 1:MSB	220	669	6	19	450	14
@DESIGN 1:DBUS12	260	709	7	24	0	0
@DESIGN 1:DBUS13	260	709	7	23	0	0
@DESIGN 1:DBUS14	260	709	7	23	0	0
@DESIGN 1:DBUS15	260	709	7	20	0	0
@DESIGN 1:~~U15:P~~	~~170~~	~~416~~	~~5~~	~~12~~	~~2425~~	~~72~~
@DESIGN 1:~~U15:G~~	~~219~~	~~587~~	~~6~~	~~18~~	~~2254~~	~~66~~
@DESIGN 1:~~U15:CN4~~	~~219~~	~~503~~	~~6~~	~~15~~	~~-1~~	~~-1~~
@DESIGN 1:~~U15:OVR~~	~~219~~	~~829~~	~~6~~	~~28~~	~~-1~~	~~-1~~
@DESIGN 1:~~U15:P3~~	~~220~~	~~698~~	~~6~~	~~21~~	~~-1~~	~~-1~~
@DESIGN 1:DBUS4	260	738	7	24	0	0
@DESIGN 1:DBUS5	260	738	7	24	0	0
@DESIGN 1:DBUS6	260	738	7	24	0	0
@DESIGN 1:DBUS7	260	738	7	22	0	0
@DESIGN 1:~~XCMP178IX~~	594	390	18	11	1497	44
@DESIGN 1:XSIG240 U8-CN	1004	511	30	15	1497	44
@DESIGN 1:XSIG309 U1-CN	1004	681	30	20	1443	43
@DESIGN 1:~~XCMP178IP~~	~~-1~~	~~-1~~	~~-1~~	~~-1~~	~~-1~~	~~-1~~
@DESIGN 1:~~XCMP178IG~~	~~-1~~	~~417~~	~~-1~~	~~12~~	~~-1~~	~~-1~~
@DESIGN 1:XSIG190 U11-D07	309	1069	11	38	2034	71
@DESIGN 1:XSIG191 U11-D06	309	1098	11	38	2063	71
@DESIGN 1:XSIG192 U11-D05	309	1098	11	38	2063	71
@DESIGN 1:XSIG194 U8-RAM3	294	743	8	25	3689	117
@DESIGN 1:XSIG195 U11-D04	294	772	8	25	3857	117
@DESIGN 1:XSIG196 U11-D03	294	772	8	25	3277	95
@DESIGN 2:XSIG110	6	45	0	2	1362	39
@DESIGN 2:XSIG125	10	3	0	0	2554	84
@DESIGN 2:XSIG124	10	3	0	0	2591	84
@DESIGN 2:XSIG123	10	3	0	0	2631	85
@DESIGN 2:XSIG122	10	3	0	0	2504	79
@DESIGN 2:XSIG121	10	3	0	0	2114	69
@DESIGN 2:XSIG111	10	3	0	0	2109	63
@DESIGN 2:XSIG104	10	3	0	0	1829	54
@DESIGN 2:XSIG150	10	3	0	0	1447	43
@DESIGN 2:ISIG3	11	3	0	0	1813	57
@DESIGN 2:XSIG118	11	3	0	0	2154	67
@DESIGN 2:ISIG1	11	3	0	0	2398	75
@DESIGN 2:XSIG116	11	3	0	0	2504	79
@DESIGN 2:XSIG115	11	3	0	0	2480	80
@DESIGN 2:XSIG114	11	3	0	0	2591	84
@DESIGN 2:XSIG113	11	3	0	0	2631	85
@DESIGN 2:~~U20:PHONY~~	~~-3~~	~~-3~~	~~-1~~	~~-1~~	~~-1~~	~~-1~~
@DESIGN 2:~~U29:O1~~	~~-44~~	~~-5~~	~~-2~~	~~-0~~	~~1362~~	~~-39~~
@DESIGN 2:U8D3	102	134	4	6	1906	53
@DESIGN 2:U8D2	102	134	4	6	2033	59
@DESIGN 2:D1	58	92	2	4	1922	55
@DESIGN 2:D0	58	92	2	4	1927	61
@DESIGN 2:U15D1	103	134	4	6	1993	58
@DESIGN 2:U15D0	103	134	4	6	1882	54
@DESIGN 2:U15D3	103	134	4	6	1906	53
@DESIGN 2:U15D2	103	134	4	6	2033	59
@DESIGN 2:U8D1	102	134	4	6	1993	58
@DESIGN 2:U8D0	102	134	4	6	1956	58
@DESIGN 2:U22D1	103	134	4	6	1556	41
@DESIGN 2:U22D0	103	134	4	6	1215	31
@DESIGN 2:U22D3	103	134	4	6	1906	53
@DESIGN 2:U22D2	103	134	4	6	1800	49
@DESIGN 2:D3	58	92	2	4	1260	35
@DESIGN 3:~~XCMP2131PHONY~~	~~-2~~	~~41~~	~~-1~~	~~2~~	~~-1~~	~~-1~~
@DESIGN 3:XSIG188 U14-P01	79	33	2	0	8	2
@DESIGN 3:XSIG187 /	33	408	0	16	8	2

Figure 23. DTA UUT controllability/observability node values. Portion of three-page printout with highest values circled.

The DTA "auto insert" option makes intelligent nodal decisions on where to insert test points for the maximum effect on C O values. One problem, initially with Daisy, is the printout of the default signal alphanumeric jumble (XSIG#) in place of the chip-pin values entered on the schematic. This requires cross reference from DTA to the schematic with a "Logician DANCE" run listing all nodes in both titles.

3.2 CALMA COPTR

CALMA workstations have an enhanced version of SCOAP called Controllability-Observability Predictability Testability Report (COPTR). CALMA used version 2.1 TEGAStation software on the 32-bit APOLLO DOMAIN computer for this job. The workstation is shown in figure 24. A prerelease version of the TEGAStation Taskmaster was used because it had more user-friendly prompts and could run COPTR on the APOLLO workstation. TASKMASTER is the user interface, applications supervisor, and file manager used to keep track of generated files and coordinate design tools. Figure 25 shows a block diagram of the hierarchy of CALMA software used in this task, and table 7 lists the CALMA workstation hardware and software relevant to this CAE analysis job. The standard TEGAStation software, as used during this test, can compile and simulate a digital network of over 6,000 signals. The TEGAStation software can handle much larger networks by changing certain software parameters.

Figure 24. 32-bit Apollo workstation (courtesy Apollo Computers, Inc.).

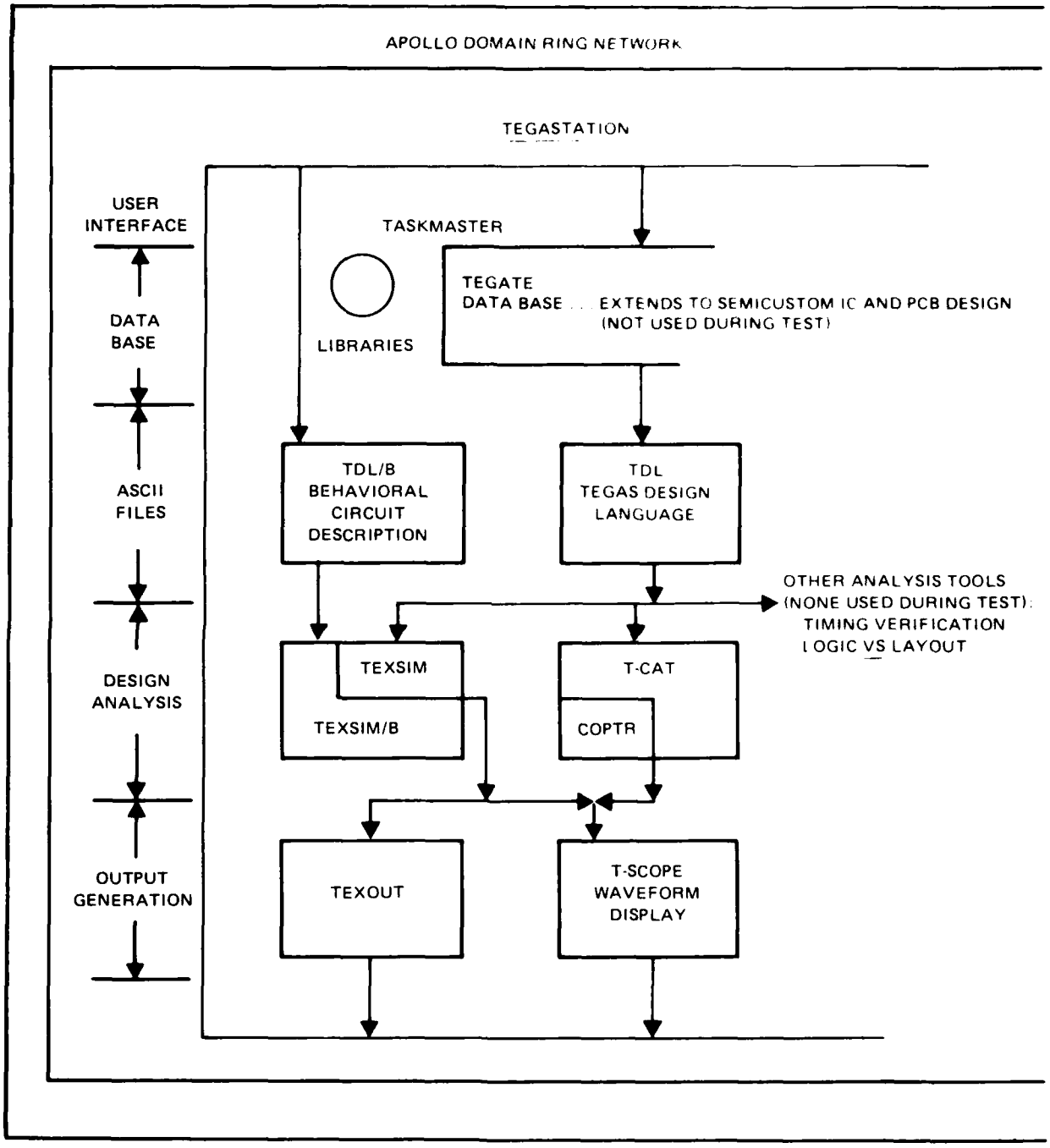


Figure 25. CALMA software hierarchy in COPTR.

Table 7. CALMA workstation hardware and software relevant to this CAE task.

Hardware/Software	Function
TEGATE	Schematic-capture program. Interfaces other products via TDL.
TEGAStation	Hardware workstation (Apollo-based).
TASKMASTER	Manages design tools of station.
TEGAS-5	TEGAS software family (for design, test simulation).
TEXSIM	TEGAS Extended Simulator.
TDL	TEGAS design language (for COPTR, TEXSIM, TEGAS-5).
COPTR	DFT C/O program used on TEGAS-5 preprocessor network description.
TCAT	Integrated test system.
DOMAIN	TEGAStation network of Apollo.
TEXSIMB	TEGAS extended simulator/behavioral.

The compacting and tight-spacing required to reduce original 44-inch by 34-inch E-drawings to 16-inch by 20-inch paper drawings is shown in figure 2.

Prerelease TEGATE 3.0, used at the start of this test period, could handle 3,000 items per circuit. The work-around procedure to this prerelease software limitation was to make up two additional CAD drawings with a block for each sheet with interconnections and signal inputs/outputs indicated. CALMA released TEGAStation 3.1 later during the test period, enabling the entire original 6-sheet schematic to be captured on a single network of 5,928 signals. Figure 26 shows these two block overviews and indicates the complexity and intersheet looping of the signal lines.

All 16 types of ICs on this circuit were in the CALMA chip library, but the 2901 microprocessor and PROM had to have functional models made to run on the COPTR analysis. This is a point that CAE users need to look into when vendors show all of the devices in their model libraries. The microprocessor and PROM models were algebraic representations in the TEGAS Design Language (TDL), which are usable on CALMA CAE programs, with the exception of COPTR. COPTR requires gate-level models and so it could not use the TDL models. A functional gate model was made up with a few dummy gates behind the PROM output pins and 100 gates behind each microprocessor output pin. These were not functionally accurate, but allowed the COPTR to run with approximate gate-level complexity

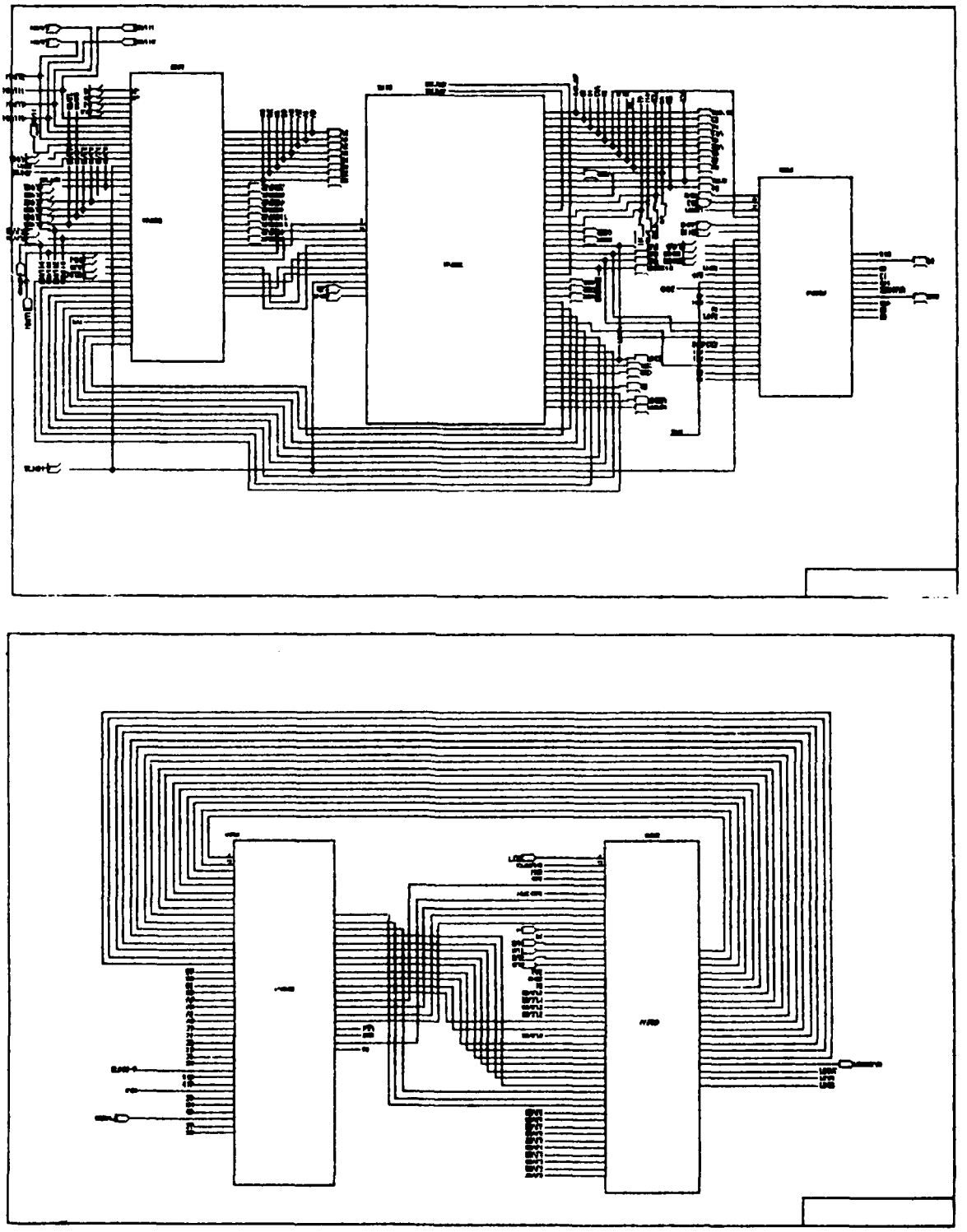


Figure 26. CALMA interconnect pages for five-sheet schematic (sheets 1, 2, and 3 at top, sheets 4 and 5 at bottom). Note complexity of intersheet signal routing.

models. TEGAStation releases 4.0 and beyond incorporate TDL/B behavioral models for these devices for simulation using TEXSIM/B.

The CALMA "TCAT user's manual" description of COPTR refers to the usual SCOAP observability and controllability of sequential and combinational devices, but adds two additional terms. In the COPTR printout, a right-hand column is titled "test," which is short for "testability." The CALMA literature explains that test generation requires a number of nodes to "be set to allow a sensitized value to be observed at a circuit output." This differs from "observability" because faulty and good circuits have different sensitized values, while observability only applies to a non-faulty circuit. Although the author agrees philosophically, in reality the "test" value in all cases equalled the "CO" column, and so therefore seemed a superfluous column. This turned out to be due to a bug, which has since been corrected in the released software. The "test" value will no longer always equal "CO." CALMA claims that "predictability" relates to controllability and that test observability combines observability and predictability of each element in the path.

TEGATE is the interactive schematic capture program software that creates and edits the design. When the schematic is complete, the design is translated into the TDL, which is an industry-standard network description language. When doing the test analysis and "what if?" games are to be tried on circuit changes, it is easier to do them by changing the TDL description, rather than add a gate or test point to the schematic and then recompile the entire TEGATE into TDL. If a gate or a test point is added to the schematic, it is not necessary to then recompile the entire TEGATE into TDL. Only the modified module (or sheet, in this case) actually needs to be translated into TDL and then recompiled.

A real problem for CAE users in the COPTR report is tailoring the printout to print only the nodes you want in a usable format. The TCAT program has many powerful commands to customize your printout as desired, but for the test engineer who rarely works on a CAE workstation it is a challenge. The TCAT command "names" is to allow the user to specify the preferred hierarchical level for signal names to be reported on. You only want the device external pinouts or gate outputs, but the COPTR crunches on all of the internal model gates. It takes perserverance to suppress or not print the "internal" gate values. Initial COPTR runs also printed many default labels on the printout, because special signal labels were not assigned on the schematic for lines between devices on the sheet. For example, the 14 microprocessor output pins each had 100 gates modeled internally to indicate gate complexity, and so the COPTR printout would print 1,400 node values per microprocessor.

The COPTR report can be requested in various format options, such as only printing out the "-1" nodes, which mean untestable, uncontrollable, or unobservable; a short COPTR such as for the UUT in figure 27, or a complete COPTR report, such as for the same UUT/DFT in figure 28. Note that the short COPTR had 24 unobservable nodes, compared to 1,880 for the same UUT circuit. The printout on -1 untestable nodes is good for debugging your schematic, finding errors in labels, chip types, wiring, etc. For example, unused chip pinouts can be indicated as such on the TDL, so that meaningless "-1s" can be eliminated.

4376	7	16	0	1	0	0	0	U37(4) :0
4377	7	15	0	1	0	0	0	U37(7) :0
4378	9	15	0	1	0	0	0	U37(9) :0
4379	9	15	0	1	0	0	0	U37(12) :0
4535	12	9	0	0	175	6	175	I3
4536	12	9	0	0	-1	-1	-1	I1
4587	11	21	0	1	156	5	156	D13
4588	11	21	0	1	152	3	152	D12
4590	6	6	1	1	0	0	0	U6(5) :0
4591	6	6	1	1	0	0	0	U6(6) :0

	CONTROLLABILITY				OBSERVABILITY				
CDT	COMBINATIONAL		SEQUENTIAL					FO.	
NUM	ZERO	ONE	ZERO	ONE	COMB.	SEQ.	TEST	NUM	DEVICE NAME
4594	6	6	1	1	0	0	0		U6(15) :0
5600	-1	102	-1	0	0	0	0		U8(36) :0
5700	-1	102	-1	0	0	0	0		U8(37) :0
5917	21	15	1	1	0	0	0		U40(7) :0B
5918	29	23	1	1	0	0	0		U41(9) :0B
5919	-1	-1	-1	-1	99	11	99		F-0 :B
5920	36	26	4	3	32	1	32		R15 :B
5921	38	28	4	3	30	1	30		U1.RAM0 :B
5922	23	17	1	1	6	0	6		U1.00 :B
5923	40	30	4	3	28	1	28		U8.RAM0 :B
5924	25	19	1	1	4	0	4		U8.00 :B
5925	42	32	4	3	26	1	26		U22.FAV :B
5926	27	21	1	1	2	0	2		U22.Q3 :B
5927	44	34	2	2	24	1	24		R0 :B

C O P T R S T A T I S T I C S

TOTAL ZERO COMBINATIONAL UNCONTROLLABLE NODES	31
TOTAL ONE COMBINATIONAL UNCONTROLLABLE NODES.	19
TOTAL ZERO SEQUENTIAL UNCONTROLLABLE NODES...	31
TOTAL ONE SEQUENTIAL UNCONTROLLABLE NODES....	19
TOTAL COMBINATIONAL UNOBSERVABLE NODES.....	24
TOTAL SEQUENTIAL UNOBSERVABLE NODES.....	24
TOTAL TEST UNOBSERVABLE NODES.....	24
AVERAGE ZERO COMBINATIONAL CONTROLLABILITY...	14
AVERAGE ONE COMBINATIONAL CONTROLLABILITY....	21
AVERAGE ZERO SEQUENTIAL CONTROLLABILITY.....	0
AVERAGE ONE SEQUENTIAL CONTROLLABILITY.....	0
AVERAGE COMBINATIONAL OBSERVABILITY.....	41
AVERAGE SEQUENTIAL OBSERVABILITY.....	2
AVERAGE TEST OBSERVABILITY.....	41

Figure 27. CALMA short COPTR report summary for UUT.

5924	25	19	1	1	4	0	4	U8.00 :B
5925	42	32	4	3	26	1	26	U22.FAV :B
5926	27	21	1	1	2	0	2	U22.Q3 :B
5927	44	34	2	2	24	1	24	RO :B
5928	17	11	0	0	-1	-1	-1	CN :B

C O P T R S T A T I S T I C S

TOTAL ZERO COMBINATIONAL UNCONTROLLABLE NODES	774
TOTAL ONE COMBINATIONAL UNCONTROLLABLE NODES.	654
TOTAL ZERO SEQUENTIAL UNCONTROLLABLE NODES...	774
TOTAL ONE SEQUENTIAL UNCONTROLLABLE NODES....	654
TOTAL COMBINATIONAL UNOBSERVABLE NODES.....	1880
TOTAL SEQUENTIAL UNOBSERVABLE NODES.....	1880
TOTAL TEST UNOBSERVABLE NODES.....	1880
AVERAGE ZERO COMBINATIONAL CONTROLLABILITY...	67
AVERAGE ONE COMBINATIONAL CONTROLLABILITY....	52
AVERAGE ZERO SEQUENTIAL CONTROLLABILITY.....	2
AVERAGE ONE SEQUENTIAL CONTROLLABILITY.....	0
AVERAGE COMBINATIONAL OBSERVABILITY.....	82
AVERAGE SEQUENTIAL OBSERVABILITY.....	14
AVERAGE TEST OBSERVABILITY.....	82

C O P T R S T A T I S T I C S

TOTAL ZERO COMBINATIONAL UNCONTROLLABLE NODES	747
TOTAL ONE COMBINATIONAL UNCONTROLLABLE NODES.	534
TOTAL ZERO SEQUENTIAL UNCONTROLLABLE NODES...	747
TOTAL ONE SEQUENTIAL UNCONTROLLABLE NODES....	534
TOTAL COMBINATIONAL UNOBSERVABLE NODES.....	1773
TOTAL SEQUENTIAL UNOBSERVABLE NODES.....	1773
TOTAL TEST UNOBSERVABLE NODES.....	1773
AVERAGE ZERO COMBINATIONAL CONTROLLABILITY...	61
AVERAGE ONE COMBINATIONAL CONTROLLABILITY....	47
AVERAGE ZERO SEQUENTIAL CONTROLLABILITY.....	2
AVERAGE ONE SEQUENTIAL CONTROLLABILITY.....	0
AVERAGE COMBINATIONAL OBSERVABILITY.....	63
AVERAGE SEQUENTIAL OBSERVABILITY.....	1
AVERAGE TEST OBSERVABILITY.....	63

Figure 28. CALMA long COPTR report summary for UUT (top) and DFT (bottom).

The COPTR performed in the expected SCOAP manner with high numbers for problem areas, low numbers for nonproblem sections, and 1 for untestable nodes. The DFT C/O values did decrease on the DFT circuit compared to the UUT circuit, although the improvement was not as marked as in other TFOM measures. There was some variation in the schematic capture approach and in the modeling of several device, as well as ground and B+ modeling techniques. The CALMA was an easier workstation to operate than the Daisy due to its easy menu formats. There seemed to be more commands to modify and vary the COPTR printout, although they are not quite as easy to master.

By the end of this job, there was 12 megabytes of disk space occupied by the original UUT and DFT sheets, plus a final "flat" schematic, or three sets of everything. The original software (8 months earlier) could not handle this large a circuit as one flat schematic, so sheets had been kept separate.

Although CALMA uses an industry-standard Apollo workstation and the common TEGAS family software, the schematic disks could not be used to run another Apollo-based TFOM, such as GenRad HITAP, unless CALMA's TEGAStation software was licensed on it. CALMA states that they support interfacing to other vendor's products, using a standard interface format with documented procedures to allow the user to build custom interfaces. An idea of program run time for CALMA software is available for this circuit with 5,894 signals, which includes internal device gate nodes. TEGAS compiled in less than 2 minutes, took 10 minutes to "link", 3 minutes to "generate faults", and 20 minutes for COPTR to compute. Naturally this does not include printout time.

4.0 SUMMARY

This section summarizes the available testability tools and methods compared in this report to help potential users choose the best tool for their needs. In response to the frequently asked question following this and the previous comparison, "Which method is best?" or "Which tool should I use?", the answer is a matter of user resources, time, degree of accuracy, type of logic, and so forth. "Trade-offs" are required. Some examples of factors that could be important to users will be noted, with the best choice of tools for those factors. No single TFOM tool is best for all users.

CAD - If the user has CAD workstations, the sophisticated SCOAP algorithm can be used in its workstation vendor copies. These include a full chip-model library. The circuit is already modeled on the CAD. Daisy and CALMA offered SCOAP in 1984, and others will follow.

Integrated Logistic Support - If Integrated Logistic Support and life-cycle cost data such as MTBF, MTTR, and maintainability information is desired, the LOGMOD and STAMP models should be considered, since they have strong credentials in that field, with more ILS history than testability.

Training/FI - If field fault-isolation or diagnostic uses are possible, including portable expert boxes for use in field troubleshooting, LOGMOD and possibly STAMP should be used. Adding user "prompts" makes these into training devices as well.

Quick-and-Cheap TFOM - If a TFOM is sought without contractor costs, negotiation times, or proprietary hassle, checklists will serve the purpose. The checklist TFOMs have obvious limitations, but for a fast FOM with some indications as to the problem area, they are fine. The RADC list is useful only for combinational digital applications.

Analog/Hybrid - Both NOSC benchmarks were digital UUTs, but for other than digital designs, the MIL-STD checklist, LOGMOD, and STAMP are recommended. The CAD model libraries are limited to digital applications although Sandia Labs in Albuquerque, which created SCOAP, claimed to have used it on analog nuclear plant applications. The MIL-STD-2165 items include analog and system factors.

TFOM Improvements - The pace of upgrades and improvements to existing TFOMs is encouraging. New improvements to CALMA TEGAS-5 software from version 2.1 to 3.0, a new Daisy software version of DTA, and enhancements to LOGMOD format and content occurred during the timeframe of this series of runs. STAMP has tripled TFOM measures and increased from 200 to 2,000 nodes.

Any TFOM tool is more methodical and structured than the old ad hoc methods, but an engineer or technician is needed to perform the input and analyze the output for proper DFT remedies. The TFOM-tool pros and cons for SSI and LSI are shown in table 8. Despite all of the changes and improvements, the same conclusion stated in NOSC TD 743 applies. No single TFOM tool is best for all users, but some tools are getting better and "smarter."

Table 8. Summary of TFOM pros and cons

TOOL	ADVANTAGES	LIMITATIONS	SSI	LSI
MIL-STD-2165	Free. Items cover everything.	Subjective items weight	X	X
PC IRAD	Easily programmed on PC. Printer. fast. neat.	Not available. Same MIL-STD Limitations	X	
RADC LIST	Free. Good on simple digital.	Unsatisfactory on complex digital. No credit for DFT and BIT.	X	X
PC IRAD	Easily programmed on PC. Printer. fast. neat.	Hard to use. Same RADC Limitations.	X	
LOGMOD	Good feedback loop identification. Good test point placement. Mature	Proprietary vendor. Graph hard to read.	X	X
STAMP	Analog. digital. system applications. 24 TFOM outputs.	Requires contractor use. Limited user documentation.	X	X
LONGENDORFER	TFOM each circuit area. Easily programmed on PC.	200-node limit.	X	
SCOAP	Good C/O data. Free. Mature. Wide usage.	CMOS primitive library	X	
ITFOM	SCOAP part worked	ITFOM result incorrect	X	
COPTR	Good model library. Hierarchical	Buy vendor CAE. Microprocessor. PROM models did not play.		X
DTA	Good model library. Hierarchical. Automatic test point placement	Buy vendor CAE. Default node names.		X

5.0 RECOMMENDATIONS

The publication of the NOSC TD 743 resulted in some TFOM product improvements, and several systems used on the complex microprocessor UUT were not available last year. This trend should continue, with more increasingly capable TFOM tools available each year to meet the DFT needs. "Lessons learned" type recommendations follow.

1. The RADC PCB checklist should add a 25% BIT section to the top B1-B4. The B3 and B4 weighting should be reduced by the use of BIT. Currently, there is no sensitivity or incentive to use BIT or VLSI. BIT and self-test should be rewarded. Another template for analog or hybrid would be useful. NOSC may begin work on this in 1986.

2. The MIL-STD-2165 checklist is too lengthy and subjective. It includes too many other disciplines. A more practical format would be separate checklists for digital, analog, and, possibly, systems applications. Some critical tests items should be mandatory with fixed weighting.

3. Although low-mix TFOMs, the "quick and dirty" checklists did point out DFT problems that the other software programs missed. The clock line problem is a good example. An expert system based upon design "rules" would be optimum, resulting in an interactive "smart" TFOM. The TFOM must realize the clock or tristate is different from other data lines.

4. Logic models need deeper insight than "a box" and "a line" level to note test criticality of complex or sequential "boxes" or clock and tristate "lines."

5. Due to the disadvantages of dealing with contractor proprietary software, the government needs a government-owned TFOM logic modeling algorithm. Note: NOSC put out a statement of work (SOW) for such a tool in 1984, called Computer-Aided Fault Isolation Testability (CAFIT) model, and work began in late FY 85.

6. Floppy disk programs with user prompts are advised for checklists to avoid using pencil and eraser, making math computations, and copying checklists. Desk top computers can be used to write floppy disk programs of the MIL-STD or RADC checklist, or even the Longendorfer TFOM algorithm.

7. Integrating TFOMs with other software can enhance the utility and accuracy of each individually for related tasks, such as developing test requirement document flowcharts or writing test programs. LASAR ATPG or SPICE circuit simulators can augment logic models with stimulus or dynamic timing information.

8. CAD vendors will claim that components in your design are in their model library, but sometimes it turns out that they are mathematical representations rather than gate level, and will not "play" on the testability program. Incompatible gate vs. function-level tools or models need to be interfaced to work together.

9. Although there are DFT reasons for logic models to be inputted with pinout data, it is recommended to delete or suppress the item pin numbers when the DFT process is completed. This will provide realistic FI and ambiguity group figures, since each "item-pin" is considered a separate item in the count.

10. CAD workstation testability printouts should use the chip, pin, and function labels entered on the schematic rather than the alphanumeric default "garbage" that must be translated on a cross-reference printout list.

CONTACT POINTS

Contact points for information or availability of TFOM tools are listed below:

TFOM TOOL	AVAILABLE FROM
MIL-STD-2165	Naval Publication Forms Center, Philadelphia, PA (no name) (215) 697-4834
RADC-TR-79-327	DTIC (ADA 082329), Alexandria, VA (no name) (202) 274-7633
LOGMOD	DETEX Systems, Inc., Villa Park, CA Ralph Depaul (714) 637-9325
STAMP	Arinc Research Corp., Annapolis, MD Dr. Randy Simpson (301) 266-4911
Daisy Test Analyzer	Daisy Systems Corp., Mountain View, CA (Sales Dept.) (415) 960-0123
COPTR	CALMA Company, Austin, TX Nancy Castelline (512) 339-0779
*HITAP	GENRAD Santa Clara, CA Jim Reddit (408) 727-4400

*HITAP was not available for evaluation in this comparison.

END

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