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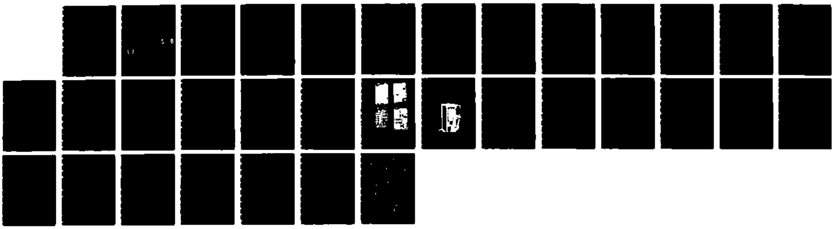

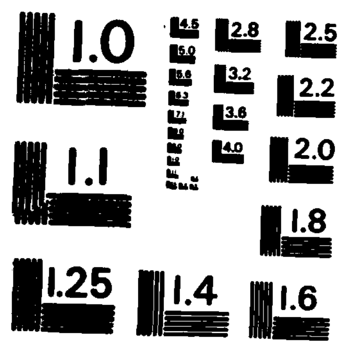

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TECHNICAL REPORT ARCCB-TR-86010

A HIGH SPATIAL RESOLUTION DIGITAL SYSTEM FOR ULTRASONIC IMAGING

AD-A166 741

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FEBRUARY 1986

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In recent years, the authors have investigated some of the fundamental theoretical physical limtations imposed on ultrasonic array performance. This has led to the extensive study of energy trapping as one means of enhancing the spatial confinement of element radiation in the array. In this report, we describe a system designed to explore the quality of the images produced by practical trapped energy mode, hybrid trapped energy mode, and other types of

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20. ABSTRACT (CONT'D)

arrays. The system implements a 256 channel parallel set of A/D and D/A converters for attachment to an arbitrary array. All 256 channels operate simultaneously at a maximum sampling frequency of 10 MHz. Hence, the total throughput of signal samples reaches 2.5 billion samples per second in a "burst" mode. The multiple-ported DRAM memory has 1×10^6 bytes of local high speed storage. Since all of the input and output signals are in digital form, a wide variety of image processing techniques can be employed. For example, from a single pulse, it is possible to reconstruct the two-dimensional hologram of the ultrasonic imaging using fast digital hardware. The images can also be prepared by pulse-echo techniques using the same system. Transmission from one portion of the array and monitoring the signal in another portion simultaneously to detect interelement coupling is possible. In this way, all of the key array parameters can be controlled and calibrated. Because of the D/A capability of the system, various signals can be transmitted from each array element, thereby permitting focusing and design of optimum probing signals.

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INTRODUCTION

This report describes a flexible system for generating acoustical images at high speed and with high resolution. The system has been designed to explore a wide variety of signal processing and image processing approaches, using different kinds of array technologies for the purpose of comparison (refs 1-15). One of the unique features of the system is the wide bandwidth, highly parallel data acquisition scheme used to send and receive signals for the array elements. The 256 channels can simultaneously digitize bursts of up to 488 (upgradable to 976) samples at up to a 10 MHz sampling frequency rate per channel. Therefore, the total maximum data transfer rate is 2.56 billion samples per second during each burst. The 256 output channels provide the ability to transmit independently selected waveforms to each array element. This produces a variety of programmable target illuminations, including pulses or tones, with focusing or without focusing. Because of the large number of input/output channels, dense spatial sampling of very large array apertures is possible leading to high spatial resolution.

In addition to the high spatial resolution of the 256 channel system, its parallel data acquisition capability permits the rapid capture of information sufficient to construct an entire image from a <u>single</u> transmitted pulse. For targets which are in motion, or in situations where extremely low total exposure to ultrasonic energy is important, this single pulse image acquisition feature can be extremely useful. To provide for a rapid image generation capability, the digitized signals are stored in multiported memories which provide for parallel computational access by an array of specialized Fast

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References are listed at the end of this report.

Fourier Transform (FFT) processor boards. With these parallel processors in place, a 30 frame persecond image generation rate is possible using digital holographic image reconstruction methods.

Although the entire system was not completed by the time this report was written, a prototype of each board has been constructed which permits us to make some observations about the feasibility of the design with regard to the cost of this approach, especially concerning the electromagnetic interference and noise problems encountered in electronic systems of this size.

ARCHITECTURE OF ACQUISITION SYSTEM

The overall architecture for the 256 channel data acquisition system is shown in Figure 1. The "front end" boards contain sufficient wideband (5 MHz) analog circuits for eight channels each, and provide for high voltage transmitter and low noise receiver electronics. The receiver circuits also contain programmable ramp amplifier circuits for each channel.

The conversion boards contain cost effective circuits for dealing with the wideband signals in each analog channel. To process the 5 MHz maximum frequency components, each channel must be able to sample at 10 MHz. The cost of a separate A/D and D/A converter for each of the 256 channels at this sampling rate and 10 bits of accuracy would be prohibitive. On the other hand, bulk CCD shift registers operating at 10 MHz are readily available at a much lower cost. These analog shift registers act as temporary storage for incoming or outgoing waveforms.

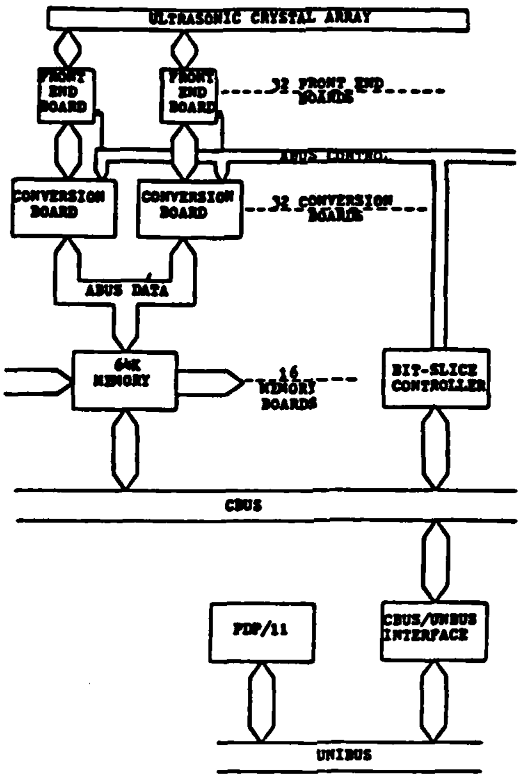

Figure 1. Overall system architecture showing parallel acquisition.

Once incoming 10 MHz data has been stored in analog form, the CCD shift registers can be clocked at a lower cost. As a further cost saving strategy, the CCD's are multiplexed in groups of eight channels through analog switches to a common sample and hold and analog to digital converter. The outgoing data is similarly demultiplexed to share the digital to analog converter for eight channels. Each CCD channel can be fed either by the DAC or the corresponding analog receiver signal after ramp amplification. Figure 2 shows the general organization of the converter board.

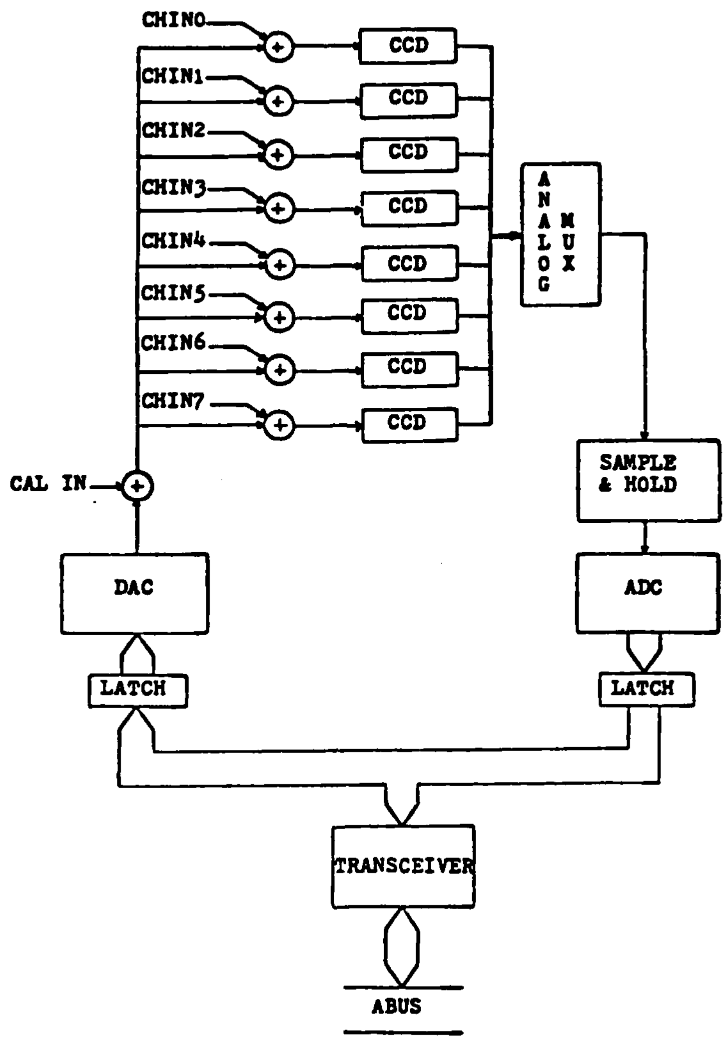

Figure 2. Organization of converter board showing eight channel multiplexing of CCD's to the A/D and D/A converters.

The 32 converter boards are interfaced in pairs bidirectionally to 16 separate multiple-sort 64K byte dynamic random access memories (DRAM's). These memories all share access to a common internal bus called the C-BUS which provides an addressing capability large enough to access any word in any 64K memory bank. The C-BUS provides an interface to a standard UNIBUS for connection to Digital Equipment Corporation computers (acting as a host) such as the PDP-11, LSI-11, or VAX. This interface provides for fast transfers to and from the UNIBUS in blocks of length up to 64K bytes in a direct memory acces (DMA) mode. This interface is illustrated in Figure 3. In that figure the small "t" denotes a tristate bus driver connection.

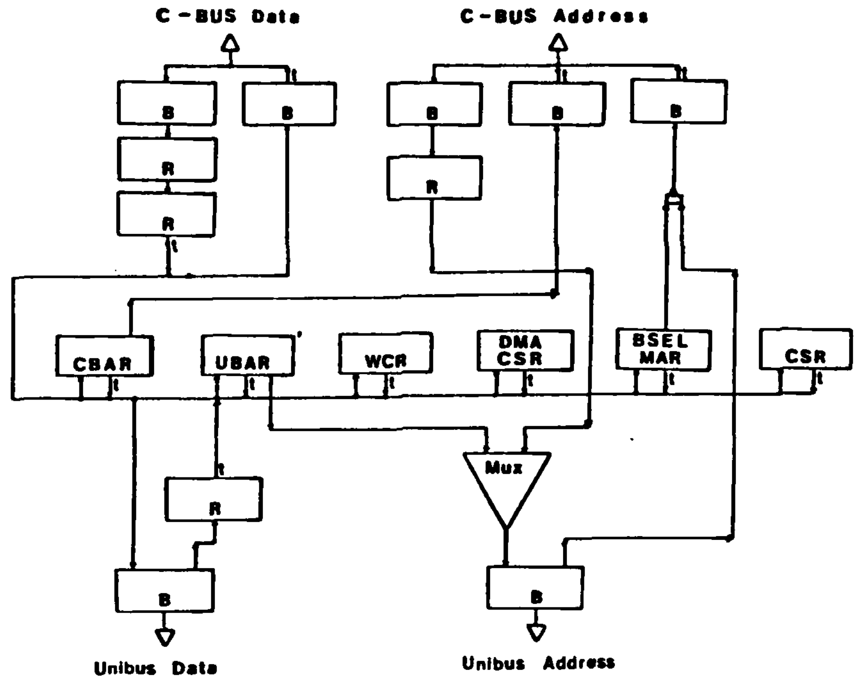

Figure 3. Register organization for C-BUS/UNIBUS interface including DMA features.

There are two main methods for the UNIBUS to access the C-BUS:

First, C-BUS memory and other devices on the C-BUS can be accessed from the UNIBUS, using the bank select and memory address register to map a portion of the UNIBUS addressing space. When this access method is used, the interface is essentially transparent to the UNIBUS, and the C-BUS becomes, in effect, an extension of the UNIBUS.

Second, to allow the UNIBUS processor to analyze and/or process C-BUS data without tying up the interface and the C-BUS, the data can be transferred between the two busses in blocks (using DMA). To accomplish this, the user sets up the C-BUS adddress, UNIBUS address, and word count registers, then uses the DMA control/status register to initiate the data transfer.

When this method is used, the interface becomes master of both the UNIBUS and the C-BUS for the duration of the data transfer. Also, there is an option which requires the interface to relinquish control of the UNIBUS periodically, allowing the UNIBUS to accomplish any essential operations such as DRAM refresh.

The interface can also be used to allow a C-BUS processor to access UNIBUS facilities. When this option is invoked, the interface becomes a slave on the C-BUS, but obtains mastership of the UNIBUS, allowing a C-BUS processor to access UNIBUS addressing space directly, as though the UNIBUS were simply another peripheral on the C-BUS. This option, known as "UNIBUS Intelligent DMA," renders the interface transparent to the C-BUS.

Finally, C-BUS to C-BUS DMA transfers are possible in this system. This is important for moving data from one block of memory to another, or in fact, simultaneously to all banks of memory.

From a control point of view, the interface has facilities which permit a C-BUS processor to cause an interrupt on the UNIBUS. Also, control of the C-BUS, normally held by the UNIBUS, can be granted to another processor on the C-BUS through the system control/status register.

In Figure 3 the bank select register BSEL determines which bank of memory (or other C-BUS device) is selected. The MAR determines which 16KB section of the 64KB memory is mapped into the UNIBUS address space 700000-737777 (octal).

The control and status register contains information about interrupt GRANT signals and other system status signals. The DMA transfers in the system are primarily from memory to memory. The starting C-BUS address for each block is in the CBAR and the corresponding UNIBUS starting address is the UBAR. The length of each block to be transferred is in the WCR.

Control for the data acquisition and bus management is handled by a high speed (10 MHz clock rate) bit-slice controller which executes a form of programming called microcode. Figure 4a illustrates this section of the architecture. Figure 4b shows how this is itself interfaced to the C-BUS in order to initially downline load microcode from the host computer into the writable control store which holds the program for sequencing the system's operations. One function of the bit-slice controller is to set up and manage DMA block transfers of memory. Other functions include the management of the transmission of waveforms, the count-down delay for reception of reflected waveforms, and the onset of ramp amplification of these waveforms.

Next, we observe in Figure 5 that an extra port is provided for each 64K memory bank. This port is provided to pass data through a set of latches to one of 16 parallel (FFT) processors.

The role of the FFT processors is to accelerate the generation of images by the method of digital holography. The FFT processors provide for a rapid transformation to the frequency domain for the 256 response waveforms. For one frequency (or several frequencies), a quasi-optical reconstruction can be implemented with an FFT operation in the spatial domain producing one "slice" through the image per transform.

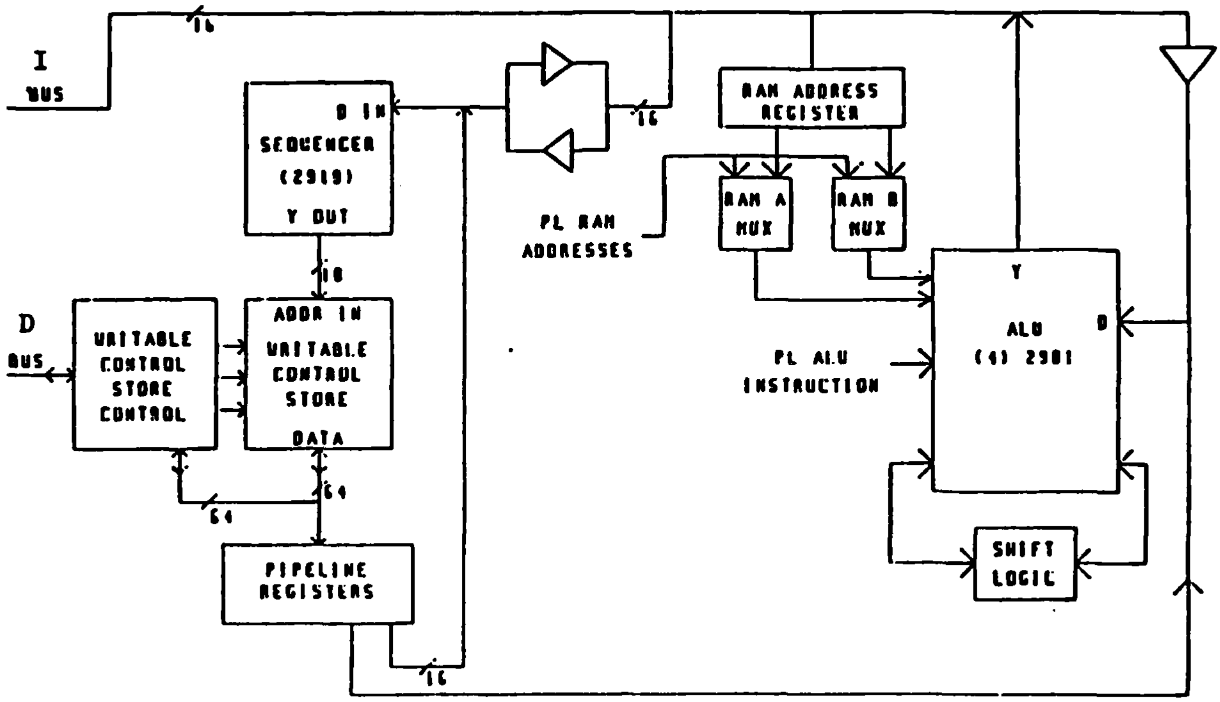

Figure 4a. Microsequencer for controlling data transfers and function selection.

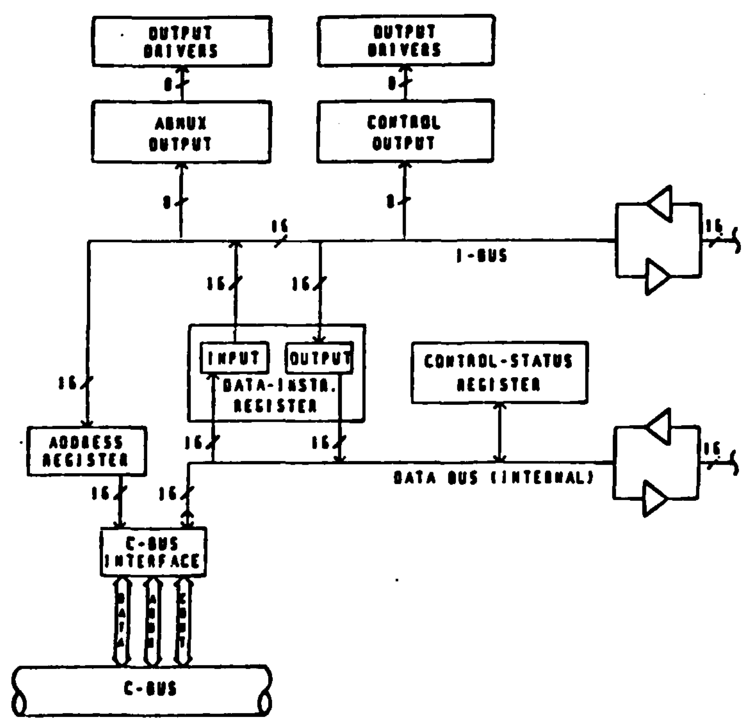

Figure 4b. Interface of microsequencer to C-BUS.

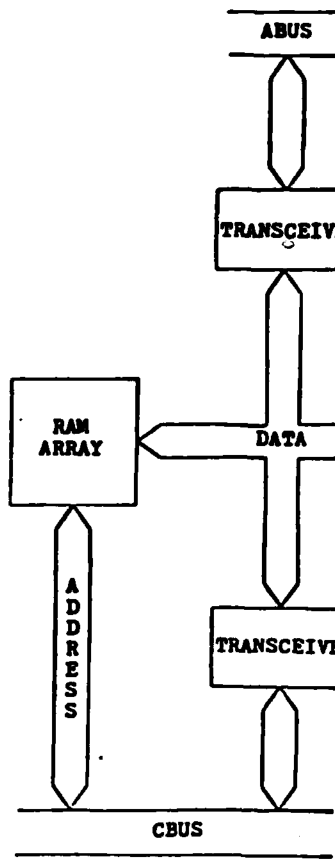

Figure 5. Connections for multiport memory showing C-BUS, A-BUS, and FFT access port.

The architecture of each FFT processor is based on the Advanced Micro Devices (AMD) 29500 family of bipolar integrated circuits designed for fast signal processing. Each FFT processor is also capable of performing a complex multiplication by a scaling factor designed to "backpropagate" the array of complex amplitudes and phases corresponding to each channel from the data acquisition system to a "slice" position in the image. Proper sequencing of these FFT processors is shared by the same bit-slice processor shown in Figure 1. This is due to the common sequence of microinstructions (SIMD architecture) executed by each FFT processor. Addressing of data in the 64K DRAM's is also handled by the bit slice-processor. Figure 6 shows the architecture of the typical FFT processor board. Final access to the image for display is handled by the DRAM port.

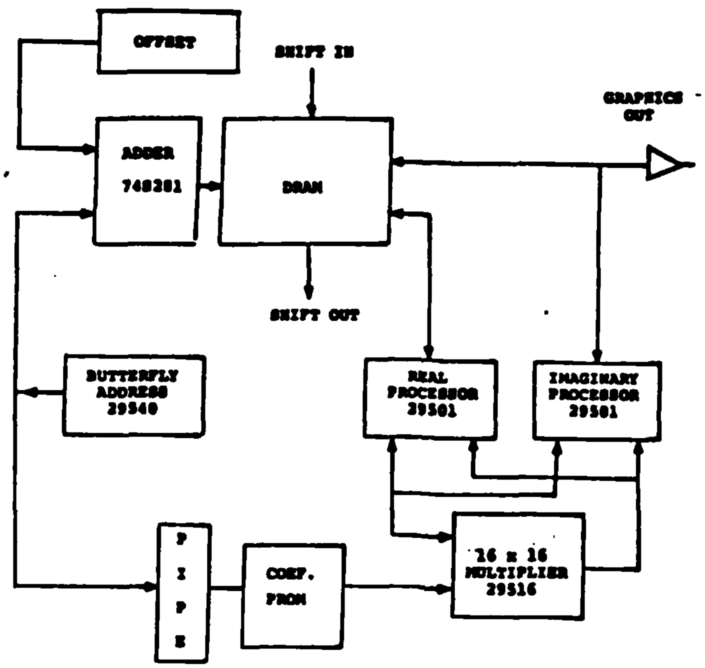

Figure 6. Fast Fourier Transform (FFT) processor (one of 16 such processors).

EXPERIENCE WITH PROTOTYPE DESIGNS

The overall organization of the equipment rack for the electronics in the system is illustrated in Figure 7. Prior to full system implementation, each unique piece of the system has been built in prototype form. This consisted of only seven DEC W9301 quad height cards, two for the bit-slice controller, and one each for the C-BUS/UNIBUS interface, the 64 KB DRAM, the CCD/CONVERTER, the Analog Interface, and FFT processor. Photographs of some of these are shown in Figure 8.

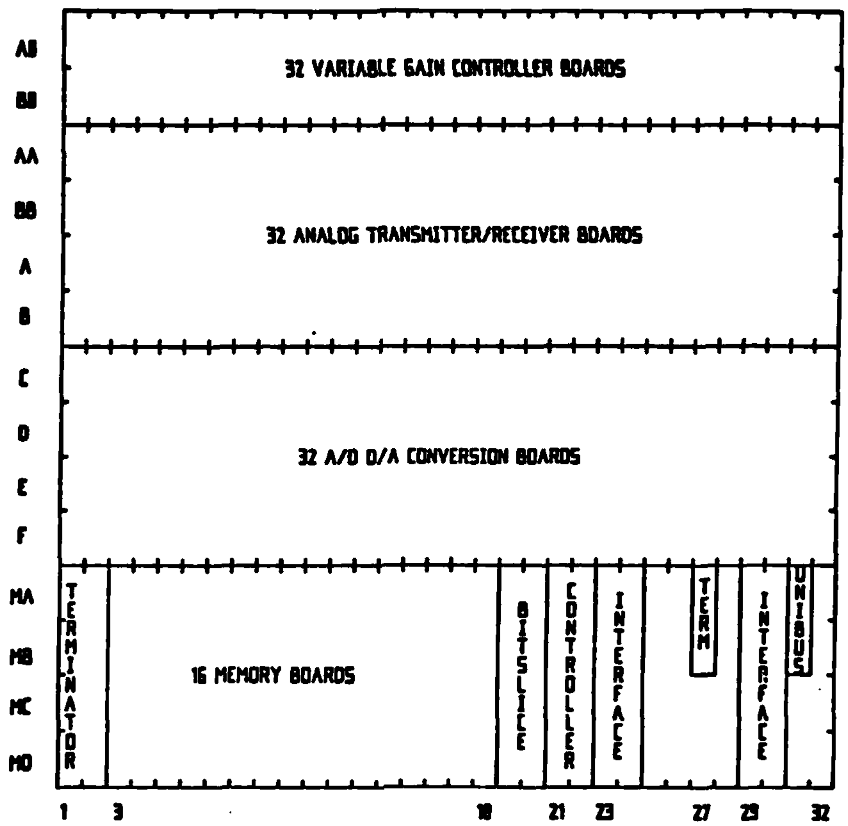

Figure 7. Rack organization for data acquisition portion of imager.

The only two parts of the design which have proved challenging are the analog channel circuit and the electromagnetic interference encountered in some parts of the system. Use of high speed logic, including advanced Schottky (AS) transistor transistor logic (TTL), and the AMD2900 series logic, creates a great deal of high frequency switching noise in the system. Also, the 100v peak transmitter signals in the analog section cause lower frequency interference. Finally, refresh cycles in the 16 DRAM cards cause large current surges which must be filtered from the power supplies.

Use of Multiwire[R] cards has helped to suppress electromagnetic interference. This is a result of the small diameter of the Multiwire

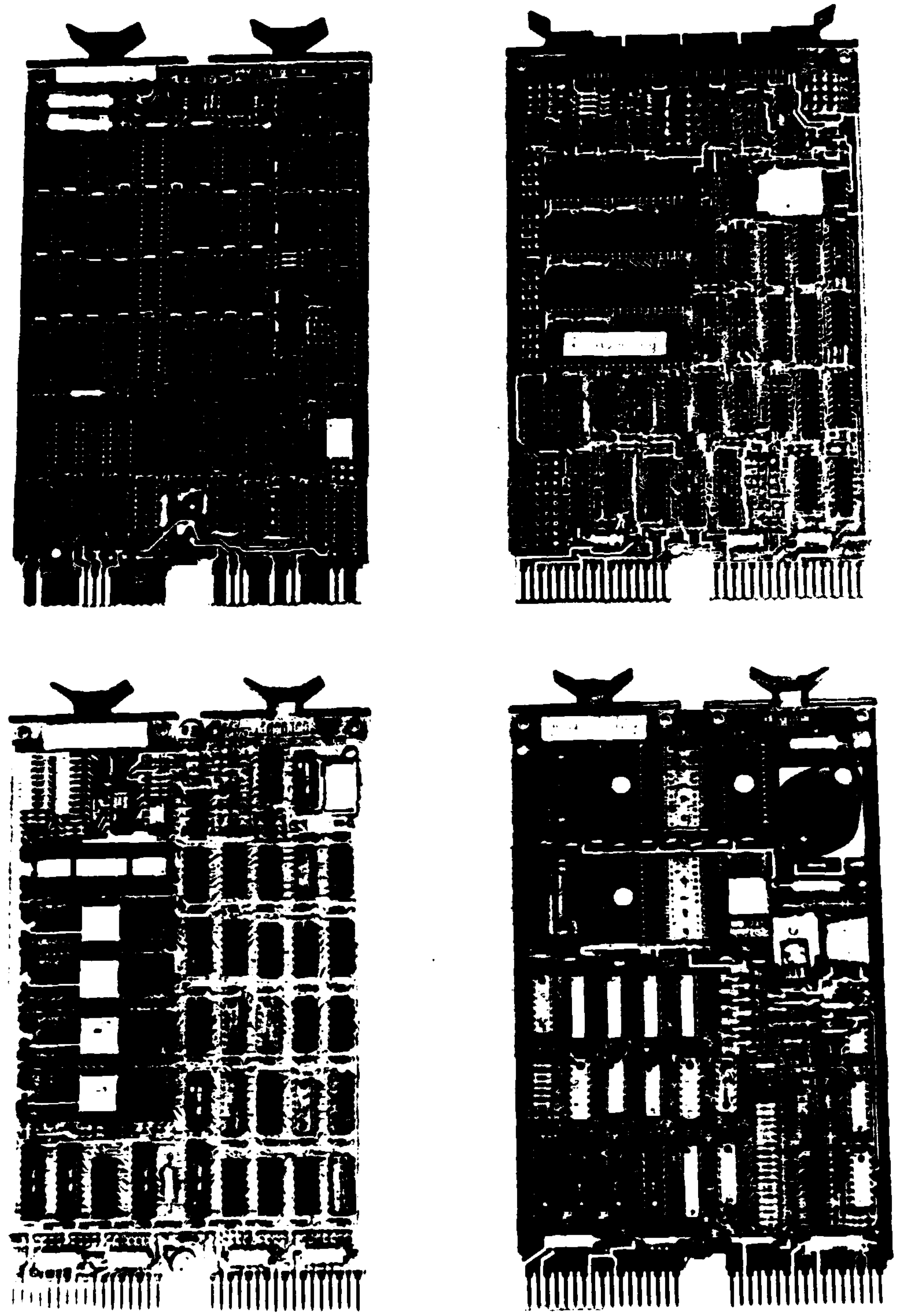

Figure 8. Photographs of several of the prototype boards.

interconnections and the extremely close spacing of these wires to the ground plane. A second recent innovation (by Rogers Corporation) is the emergence of special high capacitance/low inductance bypass capacitors which fit under each integrated circuit package. Similar HiC/LowL bus strips are used to distribute power supply voltages on cards. The lack of an adequate ground system in the backplane which serves to support the cards has also presented problems. These have been solved by using discrete micro coaxial cables. A photograph of the backplane assembly is shown in Figure 9.

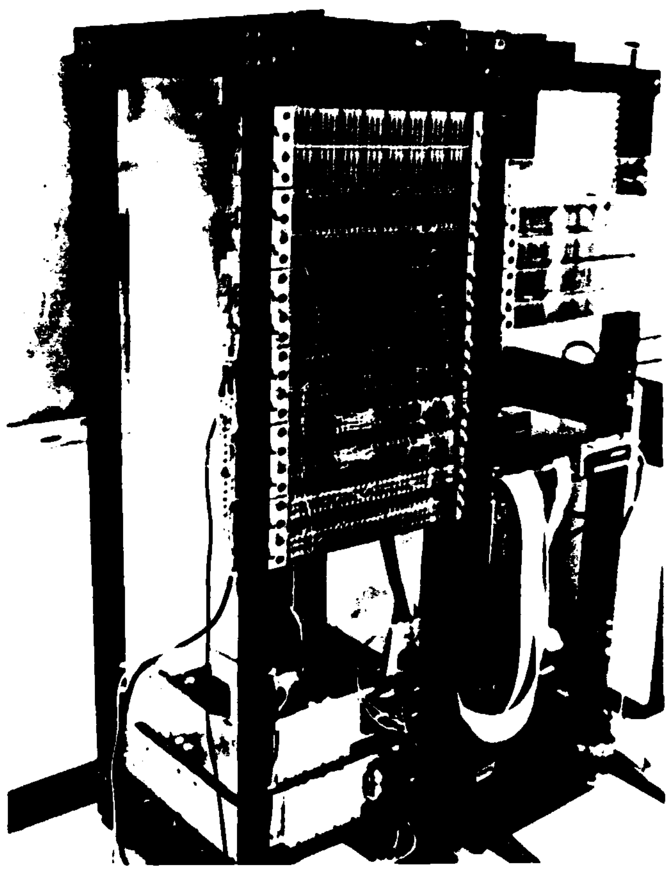

Figure 9. Photograph of rack and backplanes for imaging system.

DIGITAL FOURIER HOLOGRAPHY

The principles of digital Fourier holographic image reconstruction are well known (refs 16-18). However, implementation of these concepts in a real-time hardware embodiment suitable for use with electronic ultrasonic arrays has awaited the arrival of certain electronic innovations such as low noise bulk CCD's, the bipolar AMD 29,500 FFT signal processing parts; low cost, high precision, high frequency A/D and D/A converters, high speed analog switches, and very low cost 64KB DRAM memory.

The basic theory for digital holographic reconstruction involves the Fourier transform of the (monochromatic) spatial distribution of amplitude and phased U(x,z) of the backscattered wave field in an aperture at z = 0 (Figure 10). For a very large (infinite) aperture, this transform may be written using the notation given by Goodman (ref 19)

$$A_0\left(\frac{\alpha}{\lambda}\right) = \int_{-\infty}^{\infty} U(x,0)\ \exp\left\{-2\pi j\left(\frac{\alpha}{\lambda}x\right)\right\}dx \tag{1}$$

where λ is the wavelength. At an arbitrary distance $z \neq 0$ away from the aperture plane, the a similar transform can be defined.

$$A\left(\frac{\alpha}{\lambda};z\right) = \int_{-\infty}^{\infty} U(x,z)\ \exp\left\{-2\pi j\left(\frac{\alpha}{\lambda}x\right)\right\}dx \tag{2}$$

Inverting this equation, we obtain

$$U(x,z) = \int_{-\infty}^{\infty} A\left(\frac{\alpha}{\lambda};z\right)\ \exp\left\{+2\pi j\left(\frac{\alpha}{\lambda}x\right)\right\}\ d\,\frac{\alpha}{\lambda} \tag{3}$$

However, for U(x,z) to satisfy the wave equation, we must have

$$A\left(\frac{\alpha}{\lambda};z\right) = A_0\left(\frac{\alpha}{\lambda}\right)\ \exp\left\{\pm\frac{2\pi j}{\lambda}\sqrt{1-\alpha^2}\ z\right\} \tag{4}$$

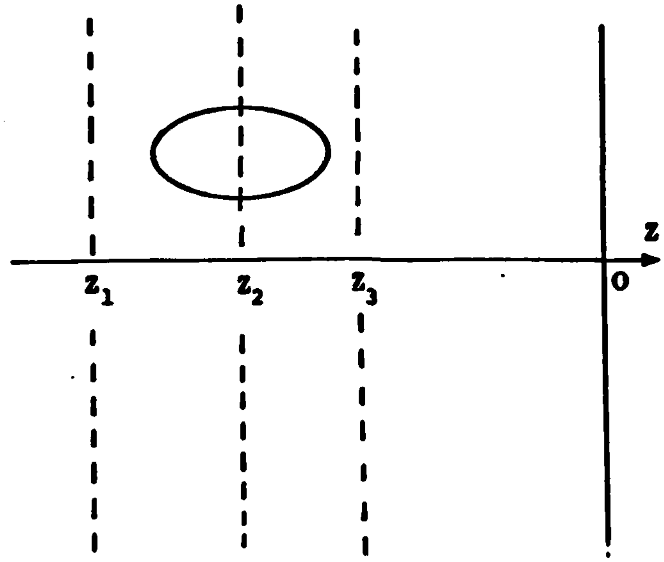

Figure 10. Geometry for backward wave propagation digital holography.

We hasten to point out that the choice of the sign in the above equation can be deduced when the propagating or evanescent waves are known to originate from a specific location in space. If all sources of the waves are located to the left of a given value of z (including the aperture at z = 0), we may safely pick the positive sign and therefore

$$U(x,z) = \int_{-\infty}^{\infty} A_0\left(\frac{\alpha}{\lambda}\right) \exp\left\{ \frac{2\pi j}{\lambda} \sqrt{1-\alpha^2}\, z\right\} \exp\left\{2\pi j \left(\frac{\alpha}{\lambda}\, x\right)\right\} d\, \frac{\alpha}{\lambda} \tag{5}$$

Hence, by Fourier transforming the distribution U(x,0) to obtain A_0 as shown in Eq. (1), multiplying by the phase factor

$$P(z) = \exp\left(\frac{2\pi j}{\lambda} \sqrt{1-\alpha^2}\, z\right) \tag{6}$$

for any z we can obtain U(x,z) for that value of z by the inverse transform of Eq. (5).

We recall that the positive sign in Eq. (6) can be chosen provided the sources of the waves are to the left of z. However, to actually image near a source (and perhaps behind it <u>further</u> to the left in z) one must be aware that the use of the plus sign in Eq. (4) can only represent the forward scattered component of the waves. Both forward and backward scattered waves are needed to satisfy the boundary conditions on the scattering surfaces of interest, and in these regions (refs 20-22)

$$A\left(\frac{\alpha}{\lambda}\,;\,z\right) = \overset{+}{A}_0\left(\frac{\alpha}{\lambda}\,;\,z\right)\exp\left\{+\frac{2\pi j}{\lambda}\sqrt{1-\alpha^2}\,z\right\} + \overset{-}{A}_0\left(\frac{\alpha}{\lambda}\,;\,z\right)\exp\left\{-\frac{2\pi j}{\lambda}\sqrt{1-\alpha^2}\,z\right\} \tag{7}$$

where

$$\overset{+}{A}_0\left(\frac{\alpha}{\lambda}\,;\,z\right) \quad \text{and} \quad \overset{-}{A}_0\left(\frac{\alpha}{\lambda}\,;\,z\right)$$

are the forward and backward scattered wave angular spectra which become functions of z as a line parallel to the x-axis at distance z passes through the source (which may be the surface of some object to be imaged).

The dependence of the forward and backward angular wave spectra on z is not in a simple form and depends on the precise nature of the source of the waves. This prevents an exact reconstruction of the image field near or behind sources with irregular shapes. Some of the distortions causing this effect are multiple scattering (ref 23) and shadowing (ref 24).

In spite of this difficulty, "images" can be constructed using the backward wave propagation procedure of substituting Eq. (4) into Eq. (3) with the positive sign only in the exponent of (4).

TIME FOR IMAGE GENERATION

The data acquisition time and time to move data blocks takes less than 4 ms. Transformation of the incoming data to the frequency domain takes 10 ms. Phase modulation takes 2 ms and the final image generation takes 6 ms. The use of the 16 FFT processors therefore makes image generation in 30 ms possible.

RESOLUTION

An estimate of the resolution of the system is determined by the focal spot size for the rectangular aperture shown in Figure 11. One can show that

$$s \cong \frac{\lambda}{2}\left(\frac{L}{D}\right) \qquad \ell \cong \left(\frac{L}{D}\right)^2 \tag{8}$$

are the lateral and depth resolutions. At 5 MHz in steel, $\lambda \cong 0.6$ mm. Hence, if the 256 element aperture spans six inches (15.24 cm) and L = 30 cm, we find that $s \cong 0.6$ mm, $\ell \cong 0.73$ mm.

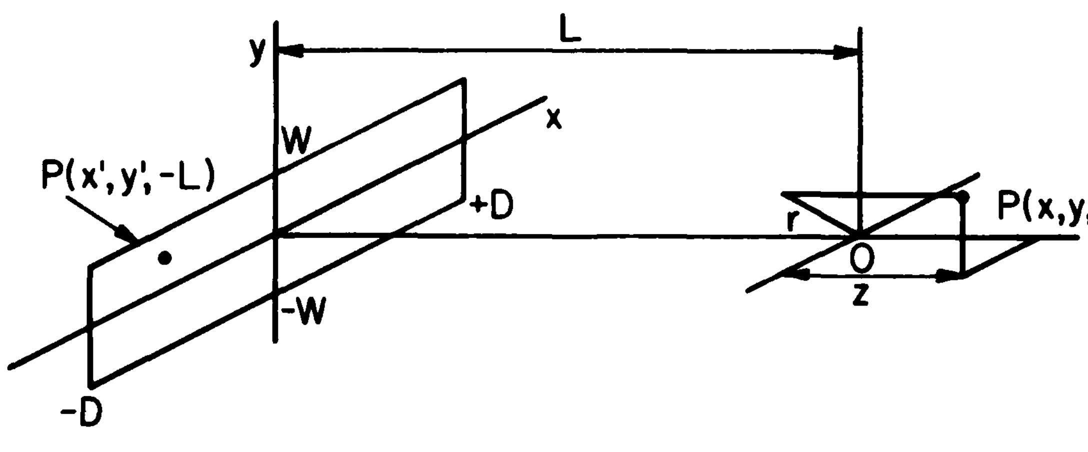

Figure 11. Geometry for aperture focusing.

CONCLUSIONS

An architecture for a high resolution 256 channel ultrasonic imaging system has been designed and partially prototyped. The architecture is capable of producing an image using a variety of reconstruction algorithms including digital holography (refs 25,26). With the use of 16 FFT parallel processor boards attached to the multiple-port DRAM's, the system is capable of generation of a 256 x 256 image in 1/30 second. Hence, single shot or video rate real-time imaging is possible.

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