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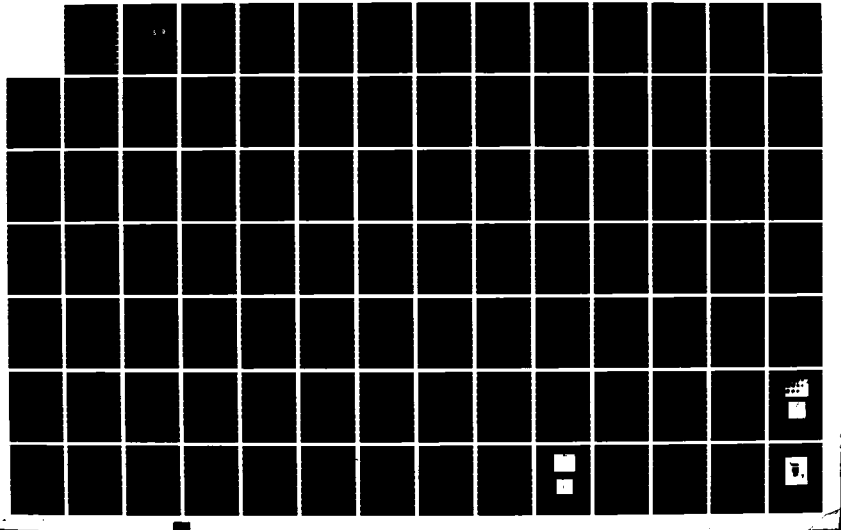

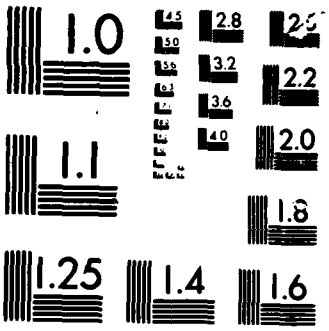
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MILLIMETER-WAVE HETEROJUNCTION TWO-TERMINAL DEVICES

N. S. Dogan
J. R. East
M. E. Elta
G. I. Haddad
Solid-State Electronics Laboratory
Department of Electrical Engineering
and Computer Science
The University of Michigan
Ann Arbor, MI 48109

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The objective of this study is to investigate the performance of heterojunction MITATT (mixed tunnel-avalanche transit-time) diodes at millimeter-wave frequencies. Along with the heterojunction MITATT diodes, GaAs double-drift IMPATT (impact ionization avalanche transit-time) diodes were also fabricated and their RF performance were evaluated.

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20. Abstract (cont.)

For the first time, millimeter-wave oscillations at 65 to 93 GHz frequencies were obtained from heterojunction MITATT diodes with strong tunneling characteristics. The power outputs and efficiencies of heterojunction MITATT diodes are comparable to the power outputs and efficiencies of the GaAs double-drift IMPATT diodes. The RF power level obtained from the heterojunction MITATT diodes is the best reported to date. A power output of 85 mW and RF conversion efficiency of 2.4 percent was achieved at 65 GHz.

Analytical models of the dc and small-signal characteristics of the heterojunction Read-type diode structures are presented that incorporate both tunneling and avalanche mechanisms for the carrier generation. An approximate large-signal analysis is developed to investigate the power and efficiency of heterojunction transit-time devices.

The fabrication processes developed for the millimeter-wave GaAs IMPATT and heterojunction MITATT diodes are given in detail. Various approaches used during the fabrication are studied comparatively and their relative advantages and disadvantages are discussed.

Millimeter-wave oscillator circuits used in this work employ a disk resonator to achieve frequency adjustment. The dc bias port uses a radial choke for RF termination.

The electrical characteristics (I-V and C-V) of the heterojunction MITATT and the double-drift GaAs IMPATT diodes are presented. The RF performance (the output power and the oscillation frequency) of the double-drift GaAs IMPATT diodes and the heterojunction MITATT diodes were measured in the V-band (60 GHz) and the W-band (94 GHz) circuits. Both the commercial ceramic package and the double-quartz standoff package were used and their effects on the RF performance of the diodes were investigated.

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LIST OF SYMBOLS

A^{**}	Effective Richardson constant ($A \cdot cm^{-2} {}^{\circ}K^{2}$).
A_T, B_T	Tunneling generation rate coefficients defined in Eqs. 2.18 and 2.19.
a_n, b_n, m_n	Electron avalanche impact ionization rate coefficients defined in Eq. 2.17.
a_p, b_p, m_p	Hole avalanche impact ionization rate coefficients defined in Eq. 2.16.
B_{tot}	Total device susceptance ($mho \cdot cm^2$).
C_1, C_2	Depletion region capacitances of Region 1 (GaAlAs) and Region 2 (GaAs) of the drift region of a hetero-junction device, respectively ($C \cdot cm^2$).
C_g	Generation region depletion capacitance ($C \cdot cm^2$).
D_n, D_p	Electron and hole diffusion coefficients, respectively (cm^2/s).
E	Electric field intensity (V/cm).
E_g	Energy of the semiconductor bandgap (erg).
E_M	Generation region electric field (V/cm).
f_o	Frequency of maximum negative conductance (Hz).
G_A	Avalanche generation rate ($cm^{-3} \cdot s^{-1}$).
G_T	Tunneling generation rate ($cm^{-3} \cdot s^{-1}$).
G_{TOT}	Total generation rate ($cm^{-3} \cdot s^{-1}$).
G_{tot}	Total device conductance ($mho \cdot cm^2$).
$\hbar$	Reduced Planck constant ($J \cdot s$).
I_{ind}	Induced current (A).
I_{inj}	Injected current (A).
I_R	Reverse bias current (A).
J_o	Optimum current density for maximum device negative conductance ($A \cdot cm^{-2}$).

J_{dc}	Dc current density ($A \cdot cm^{-2}$).
J_n, J_p	Electron and hole current densities, respectively ($A \cdot cm^{-2}$).
J_s	Total saturation current density ($A \cdot cm^{-2}$).
J_t	Tunnel current density ($A \cdot cm^{-2}$).
k	Boltzmann constant ($J \cdot {}^{\circ}K^{-1}$).
k, k_r, k_i	Defined by Eqs. 2.59 through 2.61.
L_a	Avalanche inductor in the generation region ($H \cdot cm^2$).
L_g	Tctal inductor of the generation region ($H \cdot cm^2$).
L_T	Tunnel inductor in the generation region ($H \cdot cm^2$).
ℓ_1	Length of GaAlAs region in the drift region of a heterojunction device (μm).
ℓ_2	Length of GaAs region in the drift region of a heterojunction device (μm).
M_A	Avalanche multiplication factor.
M_T	Tunnel-to-saturation-current ratio.
m'	Defined by Eq. 2.49.
m^*	Reduced effective mass (kg).
m_e^*	Electron effective mass (kg).
m_{lh}^*	Light hole effective mass (kg).
N_A, N_D	Acceptor and donor doping densities, respectively (cm^{-3}).
n, p	Electron and hole densities, respectively (cm^{-3}).
n	Ideality factor (used in Chapter III).
n'	Defined by Eq. 2.50.
n_1, p_1	Electron and hole densities in the conduction band when the single-level trap and fermi level are equal, respectively (cm^{-3}).
n_i	Intrinsic carrier density (cm^{-3}).

P_{dc}	Dc power (W).
P_{RF}	RF power (W).
q	Electronic charge (C).
R	Recombination rate ($cm^{-3} \cdot s^{-1}$).
R_a	Avalanche resistor in the generation region ($\Omega \cdot cm^2$).
R_D	Drift region resistance ($\Omega \cdot cm^2$).
R_T	Tunnel resistor in the generation region ($\Omega \cdot cm^2$).
S	Schottky contact area (cm^2).
T	Temperature (°K).
V_a	Applied voltage (V).
V_b	Built-in voltage of the p-n junction (V).
V_{dc}	Dc bias voltage (V).
V_f	Forward bias voltage (V).
V_g	Generation region voltage (V).
V_R	Reverse bias voltage (V).
V_{RF}	RF voltage (V).
v_n, v_p	Electron and hole velocities, respectively (cm/s).
v_{sat}	Saturated velocity of a carrier (cm/s).
w	Total active region width (μm).
w_1, w_2, w_3	Lengths of Regions 1, 2 and 3 shown in Fig. 2.3, respectively (μm).
X_D	Drift region reactance ($\Omega \cdot cm^2$).
x_a	Avalanche region width (μm).
x_g	Generation region width (μm).
Y_{tot}	Total device admittance ($mho \cdot cm^2$).
Z_D	Drift region impedance ($\Omega \cdot cm^2$).
Z_g	Generation region impedance ($\Omega \cdot cm^2$).
Z_{tot}	Total device impedance ($\Omega \cdot cm^2$).

α	Ratio of electron saturated velocities in GaAs and GaAlAs.
α'	Derivative of the impact ionization rate with respect to the electric field.
α_2	Defined in Eq. 2.106.
α_n, α_p	Electron and hole impact ionization rates, respectively (cm^{-1}).
β	Temperature coefficient ($°K^{-1}$).
γ	Defined in Eq. 2.81.
δ	Defined in Eq. 2.80.
ϵ_a	Avalanche region dielectric constant ($F \cdot cm^{-1}$).
ϵ_s	Semiconductor dielectric constant ($F \cdot cm^{-1}$).
η_n	Normalized power efficiency (percent).
η_p	Power efficiency (percent).
η_{rel}	Defined in Eq. 2.104.
θ_1	Drift region transit angle in GaAlAs (degrees).
θ_2	Drift region transit angle in GaAs (degrees).
θ_D	Drift region transit angle (degrees).
$\theta_{h_1}, \theta_{h_2}$	The injection angles for the first and second heterojunction interfaces (degrees).
θ_M	Phase angle of maximum injected current (degrees).
θ_{ov}	Overshoot transit angle (degrees).
θ_w	Phase angle width of the injected current pulse (degrees).
τ_g	Generation region transit time (s).
τ_{ho}, τ_{po}	Electron and hole minority carrier lifetimes, respectively (s^{-1}).
τ_{h_1}, τ_{h_2}	Transit times in Regions 1 and 2 (s).
τ_{ov}	Average overshoot time (s).
ϕ_{B_n}	Schottky-barrier height (V).

ω_a Avalanche resonance frequency ($rad \cdot s^{-1}$).

ω_g Generation region frequency ($rad \cdot s^{-1}$).

CHAPTER I. INTRODUCTION

1.1 Introduction

This study is concerned with the experimental and theoretical investigation of two-terminal millimeter-wave transit-time devices. The realization of negative resistance by utilization of transit-time effects was first proposed by Shockley[1] in 1954. Read,[2] in 1958, proposed a diode structure in which the negative resistance is caused by a combination of impact avalanche ionization and transit-time effects. Read's results predicted that this device is capable of producing microwave oscillations with an efficiency of 30 percent. The Read diode was successfully fabricated by Lee et al.[3] in 1965. At about the same time, a Si p-n junction diode, fabricated by Johnston et al.,[4] produced microwave oscillations. Since 1965, progress in the area of two-terminal transit-time devices has been very rapid. The progress achieved to date is mainly due to the improvements in the material preparation [such as molecular beam epitaxy (MBE)], circuit design, improved packaging and heat sink technology, and finally in the development of excellent theoretical models. The development of theoretical models has made a significant contribution to the understanding of the operating principles and the design of these devices. Two-terminal transit-time devices can operate in different modes which are determined by the generation mechanisms of the carriers.

Adlerstein and Statz[5] proposed a double-velocity transit-time diode (DOVETT) that is composed of two different materials with

different saturation velocities and characteristics. In the following, the basic properties of the IMPATT, MITATT and TUNNETT modes of operation and the properties of heterojunction diodes are presented.

1.2 Basic Properties of the IMPATT, MITATT and TUNNETT Modes

1.2.1 IMPATT Mode. The word IMPATT stands for impact ionization avalanche transit-time. The IMPATT mode is characterized by the injected current pulse lagging the RF voltage wave approximately 90 degrees. The device negative conductance is caused both by the avalanche multiplication process and by transit-time effects. The voltage and current waveforms shown in Fig. 1.1 give typical large-signal IMPATT operation. The operating frequency and the efficiency of the diode are

$$f_o \cong \frac{1}{2}\left(\frac{v_{sat}}{w - x_g}\right) \tag{1.1}$$

and

$$\eta \cong -\frac{2}{\pi}\left(\frac{V_{RF}}{V_{dc}}\right) , \tag{1.2}$$

where v_{sat} is the saturated velocity of the carriers in the drift region, w is the total active region width, x_g is the generation region width, V_{RF} is the magnitude of the RF voltage, and V_{dc} is the dc bias voltage.

IMPATT-mode diodes with various doping profiles, such as low-high-low, high-low, uniform, and single- or double-drift profiles, have been realized successfully. The double-drift profile is particularly very useful since both electrons and holes are utilized in

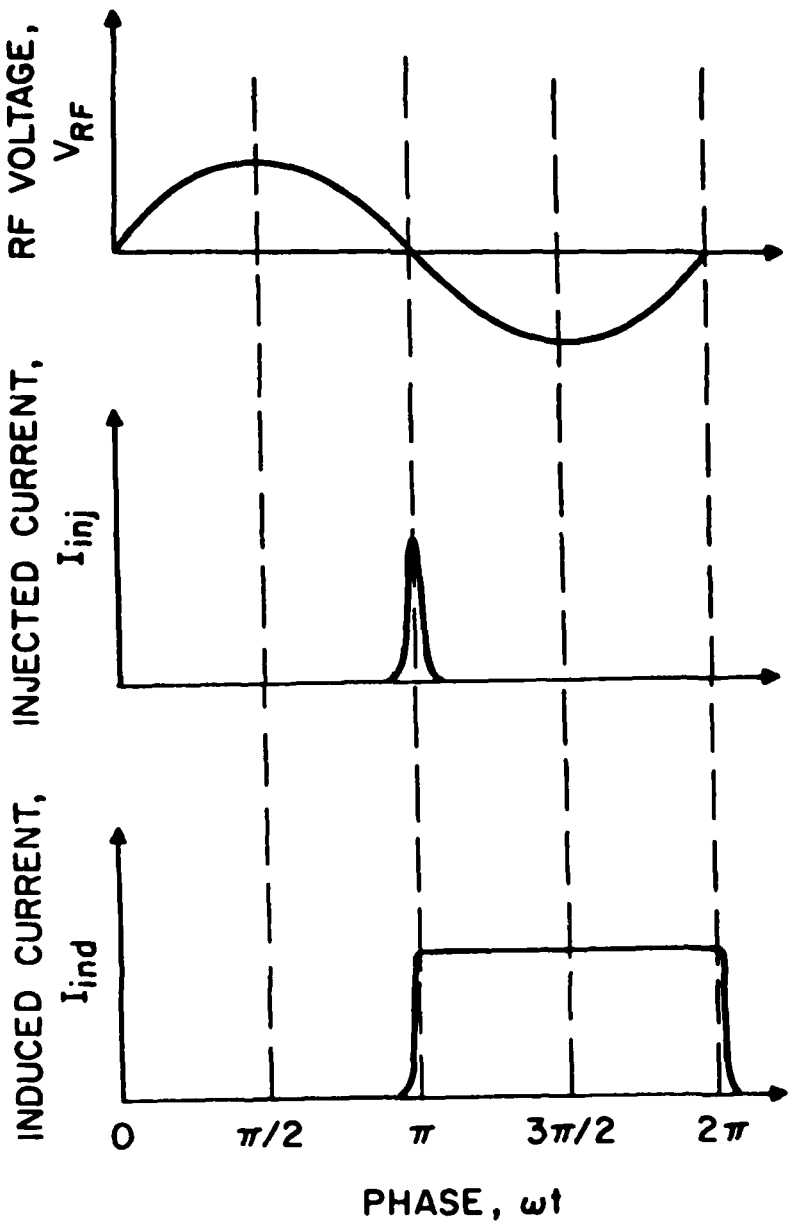


FIG. 1.1 VOLTAGE AND CURRENT WAVEFORMS FOR THE IMPATT MODE.

the operation of the diode. The total active region of the double-drift diode is approximately twice as long as that of the single-drift diode, which results in lower diode capacitance for the same diode area. For X-band and lower millimeter-wave frequencies the generation region width is small compared to the total active region width. This is not true for the higher millimeter-wave frequencies (such as 60 GHz and above) in which case the generation region width constitutes an appreciable portion of the total active region width.

The IMPATT mode has an intrinsically high noise level. This is due to the large avalanche multiplication factor that characterizes the IMPATT mode.

1.2.2 TUNNETT Mode. The TUNNETT (tunnel transit-time) mode of operation is characterized by the injected current pulse being approximately in phase with the RF voltage wave. The device negative conductance is caused only by the transit-time effects. The current and voltage waveforms are shown in Fig. 1.2. The operating frequency and the efficiency of the diode are

$$f_o \cong \frac{3}{4}\left(\frac{v_{sat}}{w - x_g}\right) \tag{1.3}$$

and

$$\eta \cong -\frac{2}{3\pi}\left(\frac{V_{RF}}{V_{dc}}\right) . \tag{1.4}$$

The preceding equations show that the efficiency and the negative resistance of TUNNETT diodes are very low compared to IMPATT diodes. Due to the need for very precise control of the doping

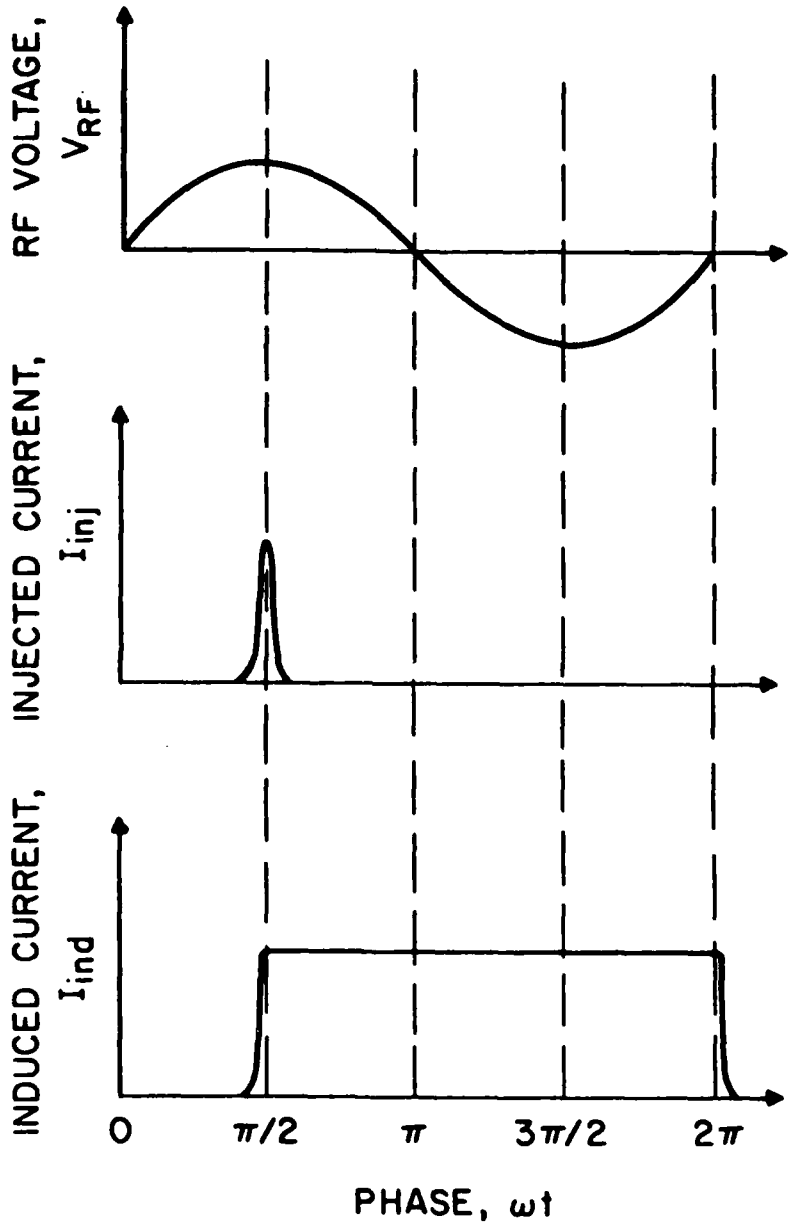


FIG. 1.2 VOLTAGE AND CURRENT WAVEFORMS FOR THE TUNNETT MODE.

profile and the low negative resistance achievable with TUNNETTs, it is very difficult to build them.

The TUNNETT diode has a low noise level since there is no multiplication of the basic noise mechanisms.

1.2.3 MITATT Mode. The MITATT (mixed tunnel-avalanche transit-time) mode of operation is characterized by the injected current pulse lagging the RF voltage wave approximately between zero and 90 degrees. The injection angle is between 90 and 180 degrees where the 90 degrees corresponds to the TUNNETT mode and the 180 degrees corresponds to the IMPATT mode. The avalanche multiplication factor is moderate which is less than the IMPATT mode avalanche multiplication factor. In the MITATT mode the initiating carriers are both thermally generated carriers and tunnel generated carriers. The efficiency and the negative resistance of MITATTs are lower than the values achievable with IMPATTs. On the other hand, the noise performance of MITATTs is expected to be superior to IMPATTs.

1.3 DOVETT (Double-Velocity Transit-Time) Devices

The DOVETT device incorporates a heterojunction between materials having different electric field saturated carrier velocities. Although the efficiency of the IMPATT diode can be improved with this approach, the most significant improvement can be achieved for TUNNETT diodes. The double-velocity transit-time devices can operate in the IMPATT, MITATT and TUNNETT modes. Figure 1.3 shows the current and voltage waveforms for the double-velocity transit-time device operating in the TUNNETT mode. The main difference between a conventional transit-time device and a double-velocity transit-time device is that the

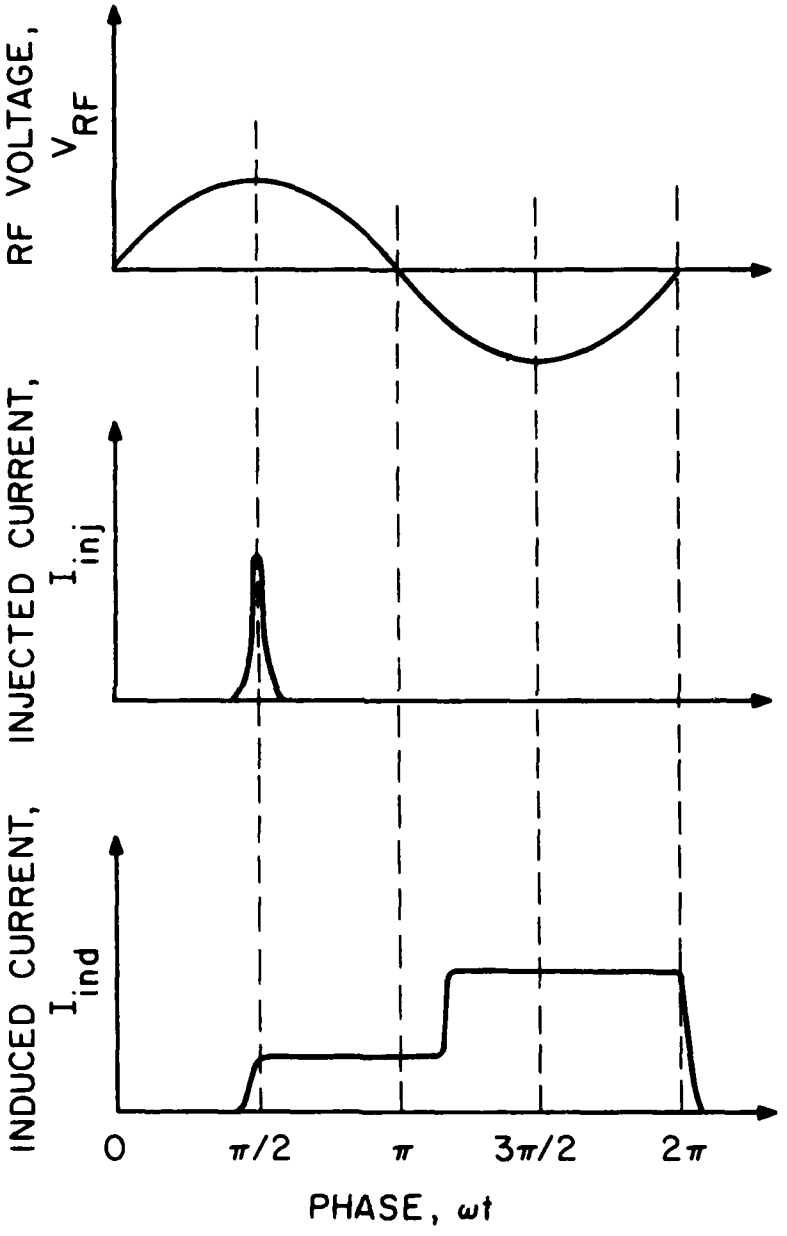


FIG. 1.3 VOLTAGE AND CURRENT WAVEFORMS FOR THE DOUBLE-VELOCITY TRANSIT-TIME DEVICE OPERATING IN THE TUNNETT MODE.

drift region incorporates a material layer near the generation region having a low saturated velocity. This requirement is satisfied by the $Ga_{0.6}Al_{0.4}As$-GaAs heterojunction structure. Immorlica and Pearson[6] investigated the velocity saturation in n-type $Ga_{1-x}Al_xAs$ single crystals. Their results indicate that for $x \cong 0.4$ the saturated velocity is the lowest value obtainable with this material with the value $v_{sat} \cong 2 \times 10^6$ cm/s. It is also known that for this Al concentration the single crystal material becomes an indirect bandgap material. Based on these results, the structure shown in Fig. 1.4 is proposed as a double-velocity transit-time device. In this structure the first GaAs layer constitutes the generation region. The first layer of the drift region is $Ga_{0.6}Al_{0.4}As$ followed by GaAs. The main advantages of using this structure for transit-time devices are as follows:

1. Due to the low saturated velocity in GaAlAs the induced current corresponding to this region is lower which improves the dc-to-RF conversion efficiency of the diode.

2. It is well known that the transient effects play an important role in the performance of millimeter-wave diodes. Monte Carlo and energy-momentum calculations at low electric field ($E < 20$ kV/cm) values show that an abrupt field change of a few kV/cm can lead to the charge traveling significant fractions of a micron at mean velocities significantly higher than the peak velocity of the static v(E) characteristics. This effect is called "velocity overshoot." Similarly, when the electric field is decreased abruptly, the carriers travel with lower mean velocities than the static velocity-electric field v(E) characteristics. This effect is called "velocity

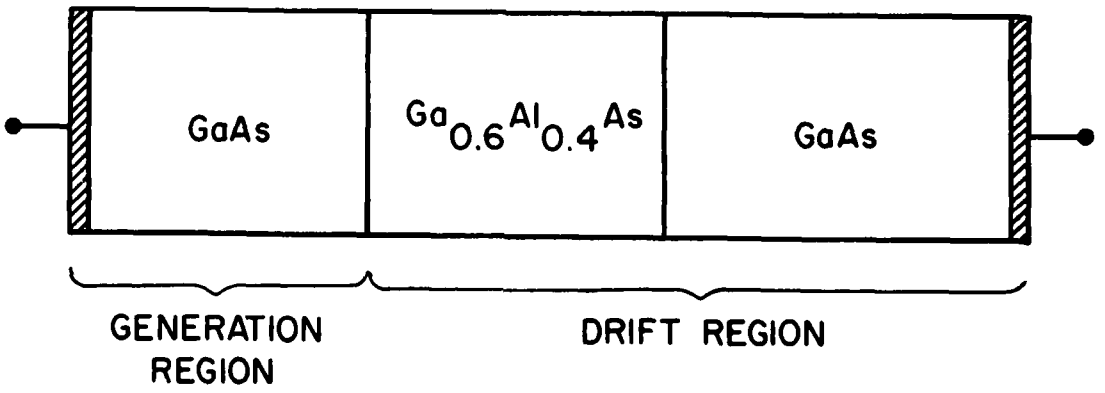


FIG. 1.4 PROPOSED DOUBLE-VELOCITY TRANSIT-TIME DEVICE.

undershoot." Similar behavior is expected when carriers go through heterojunction interfaces. When carriers enter the low-energy bandgap material from the high-energy bandgap material (i.e., from GaAlAs to GaAs) velocity overshoot occurs. Similarly, for the opposite case velocity undershoot occurs. The magnitude of the mean velocities and traveling distance are expected to depend on the initial energy of the carriers, local electric field strength, and the magnitude of the energy bandgap discontinuity. The local electric field in the heterojunction region of the IMPATT diode is usually very high (i.e., $E > 200$ to 300 kV/cm). This dominates the transient effects and the values of mean velocities and traveling distances corresponding to the overshoot and undershoot effects obtained from the low-field (i.e., $E < 20$ kV/cm) Monte Carlo analysis are invalid. Therefore, to assess the significance of the velocity overshoot and undershoot effects, detailed and accurate Monte Carlo or energy-momentum calculations must be developed that can handle the high electric field ($E > 200$ to 300 kV/cm) cases. If these effects are significant, they dominate the device performance and must be included in the design of these devices. These effects can be used to advantage to improve the efficiency of the diodes.

3. As reported by David et al.,[7] the ionization rates (α) in GaAlAs are much lower than the ionization rates in GaAs for the same electric field value. This property can be used to localize the generation region in IMPATT diodes. For the GaAs-GaAlAs-GaAs system, the generation region can be localized effectively to the GaAs region since the ionization contribution from the neighboring GaAlAs will be very low. This will also improve the performance of the diode.

1.4 State of the Art of IMPATT, MITATT and TUNNETT Diodes

The performance of IMPATT diodes is determined by several factors, such as the semiconductor material properties, doping profile, and series resistance (due to the undepleted active layer, the highly doped bulk layer, and the ohmic contact resistance). These are the inherent factors that are determined by the design criteria and the fabrication technology employed in the diode. The packaging techniques employed for mounting the diode into the waveguide circuit also affect the performance of the diode and this is one of the most challenging parts of IMPATT diode work. The lead inductance of the bonding strips and the package capacitance of the quartz standoffs or ceramic rings must be controlled (or specified) very accurately to improve the overall diode performance. Since the IMPATT diode is forced to dissipate a few watts to a few hundred watts of power on a small device area (typically 10^{-3} to 10^{-6} cm^2) the junction temperature under normal operating conditions is very high (500°K). Therefore, proper heat sinking (dissipation) must be provided.

Under large-signal operating conditions, the available negative resistance of the IMPATT diode is very low, typically less than $-1\ \Omega$. This is a very low impedance that must be matched to the load impedance that is two orders of magnitude higher for most circuits. This requires the design of a waveguide circuit capable of achieving the impedance transformation with low-loss and broadband characteristics.

Since the first successful fabrication of an IMPATT diode in 1965, rapid progress has been made in all of the areas mentioned previously, making the IMPATT diode a very useful component in system

and component design in microwave and millimeter-wave communication and guidance systems. The frequency of Si IMPATT diodes has been extended up to 423 GHz (submillimeter wave). The highest efficiency reported to date is 35.5 percent at 8.15 GHz with a low-high-low GaAs IMPATT diode structure. In terms of power output and efficiency, GaAs IMPATT diodes show better performance in CW operation for frequencies up to 60 GHz than do Si IMPATT diodes. However, GaAs IMPATT diodes have not worked well for frequencies higher than 100 GHz. Tables 1.1 and 1.2 show the state of the art of Si and GaAs diodes,[8] respectively.

Due to electronic limitations, the power and efficiency of GaAs and Si IMPATT diodes drop very quickly as the frequency of operation exceeds 200 GHz. For the upper end of millimeter-wave frequencies or in the submillimeter-wave region, the other alternative is to use tunneling effects (TUNNETTs and MITATTs). Nishizawa et al.,[9] for the first time, obtained oscillations in the 100 to 248 GHz frequency range from $p^+n^+nn^+$ GaAs diodes with strong tunneling reverse-bias characteristics. The measured power levels are not quantitative in their published results. Elta et al.[10] reported oscillations from MITATT GaAs diodes at 140 GHz with 3 mW output power. These are the only published results to date. The lack of more work on TUNNETT and MITATT diodes is due to the difficulties in the design and fabrication of these devices. TUNNETT and MITATT diodes are inherently low negative-resistance diodes and the series resistance further reduces the available negative resistance. Hence, the device-circuit impedance matching problem is

Table 1.1

State of the Art of Si IMPATT Diodes (Pao[8])

Frequency (GHz)	Power Output	Efficiency (Percent)	Mode	Structure*	No. of Diodes in the Package	Reference
8.5	6.8 W	11.8	CW	DD	1	Seidel et al.
8.9	6 W	12.2	CW	DD	1	Seidel et al.
10	1.7 W	10	CW	DD	1	Ying
11.5	2.8 W	13.2	CW	DD	1	Pfund et al.
12	7 W	12	CW	DD	1	Seidel and Niehaus
13.3	4.7 W	8	CW	SD	1	Swan
40.1	2.26 W	10.6	CW	DD	1	Midford and Bernick
50	1 W	14.2	CW	DD	1	Seidel et al.
55	1.6 W	11.5	CW	DD	1	Hirachi et al.
60.5	1.2 W	0	CW	DD	1	Midford and Bernick
68	0.5 W	8.7	CW	DD	1	Leistner
70	0.35 W	9.2	CW	DD	1	Howard et al.

*SD denotes a single-drift structure and DD denotes a double-drift structure.

(Cont.)

Table 1.1 (Cont.)

Frequency (GHz)	Power Output	Efficiency (Percent)	Mode	Structure*	No. of Diodes in the Package	Reference
77.7	1.014 W	8.1	CW	DD	1	Ino et al.
86	0.32 W	12	CW	DD	1	Gokgor et al.
91.9	0.98 W	3.6	CW	DD	1	Midford and Bernick
95	0.22 W	10	CW	DD	1	Gokgor et al.
132	86 mW	7.6	CW	SD	1	Gokgor et al.
140	110 mW	2	CW	SD	1	Chang et al.
170	60 mW	2	CW	SD	1	Chang et al.
185	78 mW	2.3	CW	SD	1	Ino et al.
202	50 mW	1.3	CW	SD	1	Ishibashi and Ohmori
220	50 mW	1	CW	DD	1	Midford and Bernick
228	33 mW	0.8	CW	DD	1	Midford and Bernick
285	> 0.5 mW	0.35	CW	SD	1	Ino et al.
295	4.5 mW	0.13	CW	SD	1	Ishibashi et al.
301	1.2 mW	--	CW	SD	1	Ishibashi and Ohmori

(Cont.)

Table 1.1 (Cont.)

Frequency (GHz)	Power Output	Efficiency (Percent)	Mode	Structure*	No. of Diodes in the Package	Reference
412	2.2 mW	0.47	CW	SD	1	Ishibashi et al.
8	28 W	4	1 μs 0.1%	SD	1	Gilden and Moroney
9.7	45 W	10	1 μs 10%	DD	1	Pfund and Curby
10.2	54 W	13	1 μs 10%	DD	1	Nagao et al.
16.5	11 W	12	0.8 μs 25%	DD	1	Pfund et al.
35	31 W	6.5	0.1 μs 1%	DD	1	Walker and Hing
65	5.3 W	5	0.1 μs 0.5%	DD	1	Freyer et al.
94	13 W	8	0.1 μs 0.5%	DD	1	Chang et al.
140	3 W	6	0.1 μs 0.25%	SD	1	Chang et al.
170	1.3 W	2.5	0.1 μs 0.25%	SD	1	Chang et al.
2.7	0.7 W	2	0.1 μs 0.25%	SD	1	Chang et al.

Table 1.2

State of the Art of GaAs IMPATT Diodes (Pao[8])

Frequency (GHz)	Power Output	Efficiency (Percent)	Mode	Structure*	No. of Diodes in the Package	Reference
5	11 W	22.4	CW	SD	4	Adlerstein et al.
5.7	11 W	21	CW	SD	4	Nishitani et al.
6.1	15 W	25	CW	Lo-Hi-Lo	1	Hirachi et al.
7.75	10 W	16	CW	DD-Read	4	Wallace et al.
8.15	8 W	35.5	CW	Lo-Hi-Lo	-	Kim and Matthei
9.6	5.8 W	28	CW	Lo-Hi-Lo	-	Kim and Matthei
10.5	4 W	30	CW	Lo-Hi-Lo	-	Kim and Matthei
11.1	5.3 W	24	CW	Lo-Hi	4	Grierson et al.
13.75	3.2 W	20.7	CW	Read-S	4	Kim et al.
19.6	3.1 W	18.6	CW	SD-Read	4	Berenz et al.
20	4 W	21	CW	DD-Read	4	Adlerstein et al.

*SD denotes a single-drift structure and DD denotes a double-drift structure. Read denotes a Read-type doping profile and S denotes a Schottky-barrier diode.

(Cont.)

further complicated and difficult to achieve. Figures 1.5 and 1.6 show the power-frequency performance of Si and GaAs IMPATT diodes, respectively.

1.5 Outline of the Present Study

The objective of this study is to investigate the experimental and theoretical characteristics of heterojunction (GaAs-$Ga_{0.6}Al_{0.4}As$-GaAs) and conventional GaAs two-terminal millimeter-wave transit-time devices.

In Chapter II analytical models of dc and small-signal characteristics for Read-type diode structures are given for heterojunction transit-time diodes operating in the IMPATT, MITATT, and TUNNETT modes. An approximate large-signal analysis is developed to investigate the power and efficiency of heterojunction diodes that includes overshoot effects. Based on this approximate large-signal model, a computer program was developed to calculate optimum device structures for maximum efficiency.

In Chapter III, a discussion of various processing steps involved in the fabrication of millimeter-wave GaAs IMPATT diodes is given. Ohmic contact and Schottky contact formation on GaAs are very important processing steps in the device and circuit fabrication. Their quality directly affects the device performance. The ohmic and Schottky contact characteristics used in this work are presented. Finally, the chemical etching and wafer thinning of GaAs used in this work is discussed in some detail.

In Chapter IV the fabrication processes developed during this work, namely proton isolation, mesa etching, integral packaging with

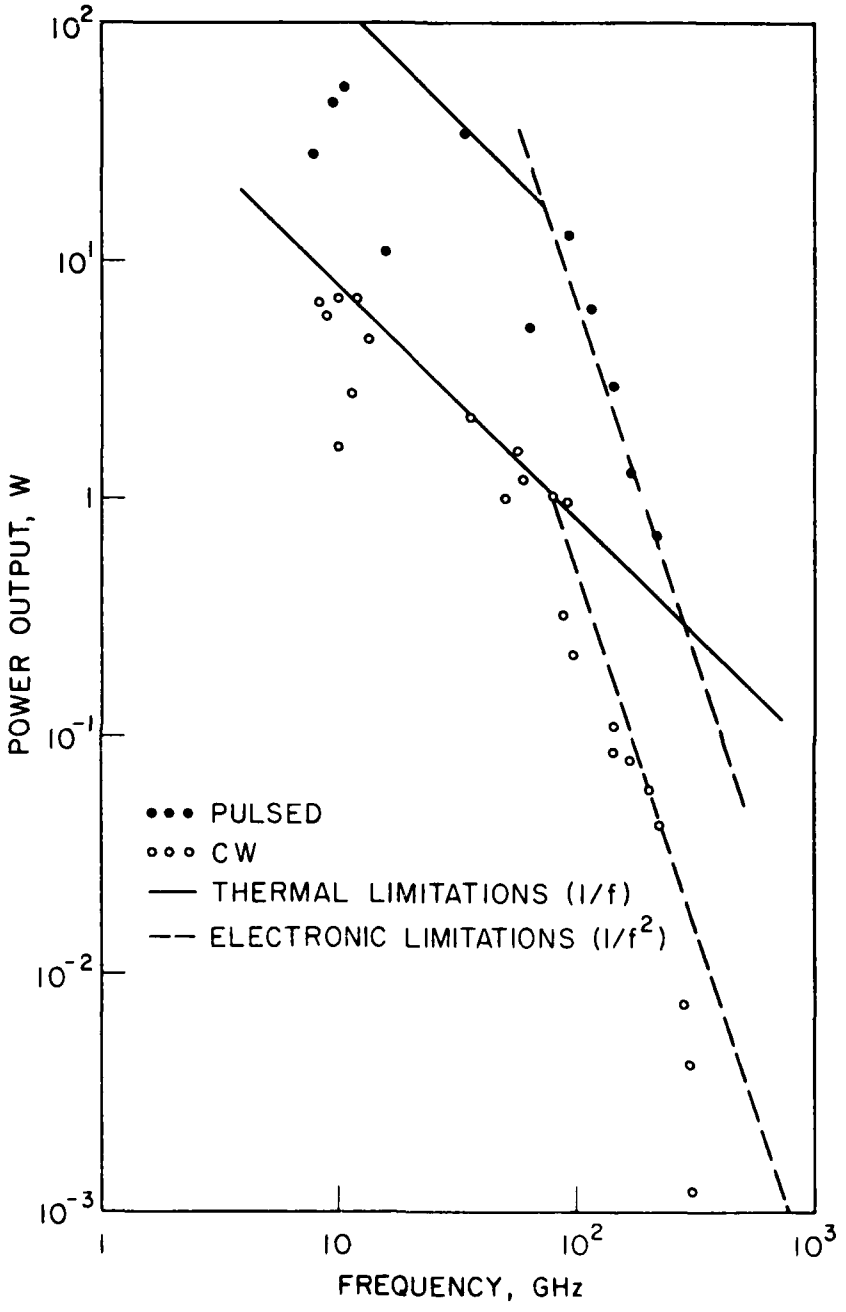


FIG. 1.5 STATE OF THE ART OF Si IMPATT DIODES. ("AO[8])

Table 1.2 (Cont.)

Frequency (GHz)	Power Output	Efficiency (Percent)	Mode	Structure*	No. of Diodes in the Package	Reference
20.3	2.7 W	18	CW	SD-Read	4	Berenz et al.
33	3 W	22	CW	DD-Read	1	Adlerstein and Moore
44.1	2.1 W	19	CW	DD-Read	1	Adlerstein and Chu
51.7	1.025 W	10.5	CW	DD	1	Ma et al.
53	0.7 W	11.2	CW	SD	1	Zhang and Freyer
60	1.24 W	11.4	CW	DD-Read	1	Adlerstein and Chu
150	3 mW	0.5	CW	TUNNETT	1	Elta et al.
8.3	35 W	20	1 μs 25%	DD	2	Berenz et al.
8.5	31 W	23	0.3 μs 30%	DD-Read	4	Wallace et al.
8.6	30 W	23	0.5 μs 10%	SD-Read	1	Hierl et al.
9.3	30 W	17	1 μs 10%	DD-Read	1	Berenz et al.
13	20.5 W	21	0.5 μs 10%	SD-Read	1	Hierl et al.
15.4	15 W	18	0.5 μs 10%	SD-Read	1	Hierl et al.
96	1 mW	--	Pulsed	SD	1	Schawarz and Bonek

(Cont.)

Table 1.2 (Cont.)

Frequency (GHz)	Power Output	Efficiency (Percent)	Mode	Structure*	No. of Diodes in the Package	Reference
200	1 mW	--	Pulsed	TUNNETT	1	Nishizawa et al.
338	10 mW	--	Pulsed	TUNNETT	1	Nishizawa et al.

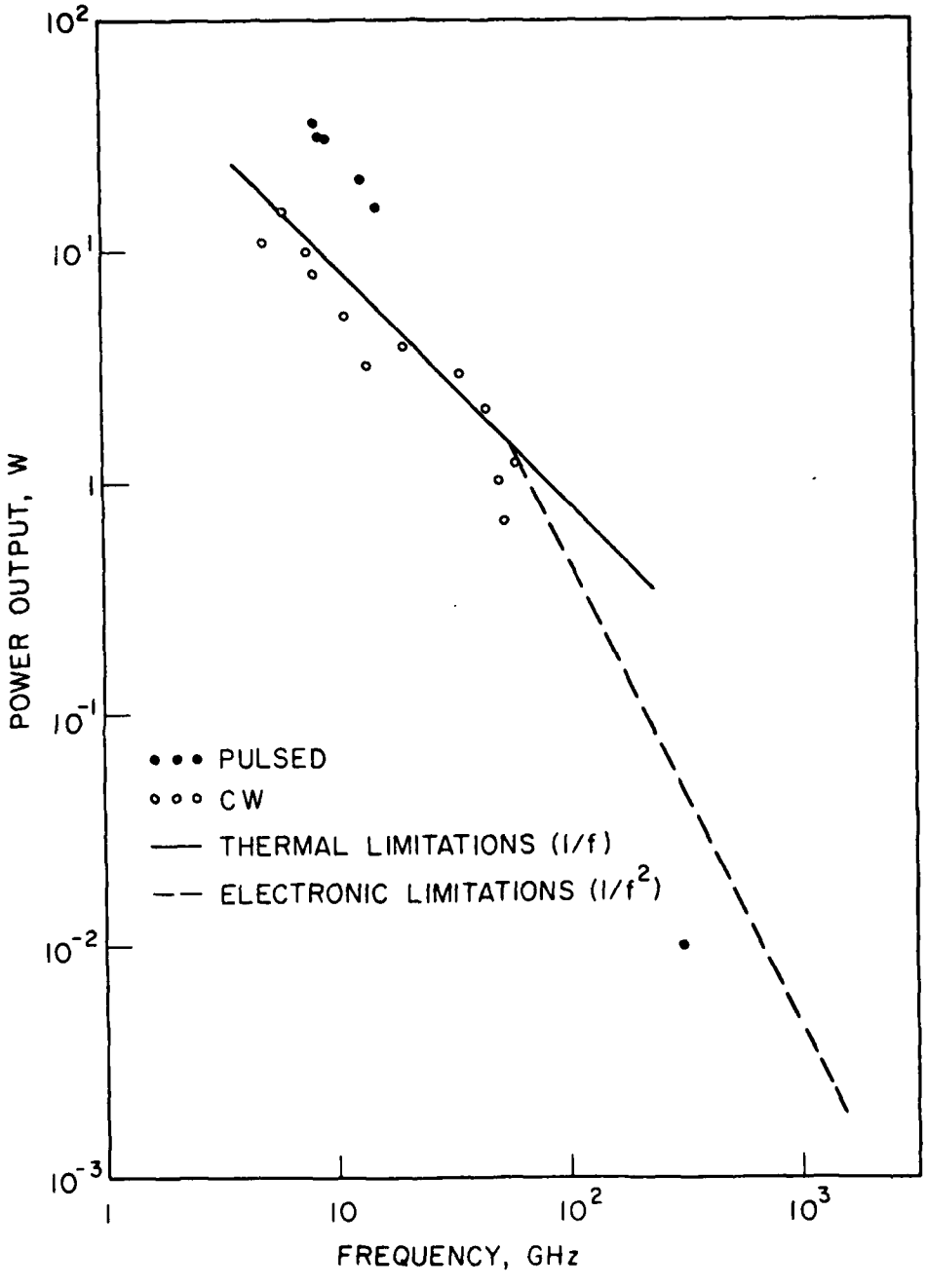


FIG. 1.6 STATE OF THE ART OF GaAs IMPATT DIODES. (PAO[8])

polyamide support, and selectively plated Au-Ag-Au integral heat sink formation, are presented in detail. These various approaches are compared and their advantages or disadvantages for potential application are discussed.

In Chapter V the waveguide circuit used in this work is presented. Other approaches to the design of waveguide circuits for millimeter-wave oscillators are reviewed. The packaging techniques of the diode chips and their effects on the performance of millimeter-wave oscillators are studied. Finally, the results of the RF performance of the diodes fabricated during this work are presented.

In Chapter VI a summary of the work is presented and suggestions for further study are given.

CHAPTER II. DC, SMALL-SIGNAL, AND APPROXIMATE LARGE-SIGNAL ANALYSIS OF HETEROJUNCTION TRANSIT-TIME DEVICES

2.1 Introduction

In this chapter analytical models for dc, small-signal, and approximate large-signal characteristics for Read-type double-velocity heterojunction transit-time devices are presented. The models developed here assume that the heterojunction interface is away from the generation region (i.e., the generation region is confined to the GaAs layer) and it only affects the drift region characteristics. The generation region and the drift region of the diode are treated separately such that the characteristics of IMPATT, MITATT and TUNNETT modes of operation can be obtained. Elta[11] derived dc and small-signal analytic models that incorporate both tunneling and avalanche breakdown mechanisms. Some of his results are stated here without going into detail. For a more detailed treatment, his work should be consulted. Following the dc and small-signal analysis, an approximate large-signal analysis is given that can be employed to determine the power and efficiency of the heterojunction diode. The analysis also includes overshoot effects.

2.2 Dc Analysis

2.2.1 The Tunnel Injection Current. The tunnel injection current of a reverse-biased p^+-n diode is determined by the physical parameters of the materials, such as band structure, bandgap, and effective masses of the electrons and holes. To obtain an appreciable tunnel injection current, the electric field at the junction

should be high which requires a highly doped region on the n-side ($n \cong 1 \times 10^{18}$ cm^{-3}) of the p^+-n junction. The direct tunnel current density in a p-n junction is given by the following equation:

$$J_t = \frac{\sqrt{2}\, q^3 m^{*1/2} V_a E}{4\pi^3 \hbar^2 E_g^{1/2}} \exp\left(-\frac{\pi m^{*1/2} E_g^{3/2}}{2\sqrt{2}\, qE\hbar}\right) , \qquad (2.1)$$

where E is the electric field intensity in the junction, E_g is the bandgap energy, V_a is the applied voltage, and m* is the reduced effective mass represented by

$$m^* = \frac{1}{(1/m_e^*) + (1/m_{lh}^*)} , \qquad (2.2)$$

where m_e^* is the electron effective mass and m_{lh}^* is the effective light hole mass. If E is approximated by the peak field of the p^+-n abrupt junction, it can be expressed as

$$E = \left(\frac{2qN_D(V_a + V_b)}{\varepsilon_o \varepsilon_s}\right)^{1/2} , \qquad (2.3)$$

where V_b is the built-in voltage of the junction, N_D is the donor density in the n layer, and ε_s is the relative dielectric constant of the material. Substituting Eq. 2.3 into Eq. 2.1 yields

$$J_t = B_1 \sqrt{V_a + V_b}\, V_a \exp\left(-\frac{B_2}{\sqrt{V_a + V_b}}\right) , \qquad (2.4)$$

where

$$B_1 = \frac{q^3}{2\pi^3 \hbar^2} \left(\frac{qm^* N_D}{\varepsilon_o \varepsilon_s E_g}\right)^{1/2} \qquad (2.5)$$

and

$$B_2 = \frac{\pi E_g}{4qh}\left(\frac{\varepsilon_o \varepsilon_s E_g m^*}{qN_D}\right)^{1/2} . \qquad (2.6)$$

The temperature coefficient β of the I-V characteristics is assumed to be given by

$$\beta = \frac{\Delta V}{V_{293°K}\Delta T} , \qquad (2.7)$$

where $\Delta V = V - V_{293°K}$ and $\Delta T = T - 293°K$. The sign of β is used to evaluate the injection mechanism in the junction. When the tunnel injection is dominant in the junction, β is negative. β for a p^+-n diode that is dominated by avalanche breakdown is positive.

2.2.2 Simple Mixed-Breakdown Model. In this analysis the drift-diffusion model, which consists of five fundamental equations, is used for the analysis of microwave transit-time diodes. Poisson's equation, the continuity equations for holes and electrons, and the transport equations for holes and electrons must be solved with the proper boundary conditions. In one dimension, these equations are:

$$\frac{\partial E}{\partial x} = \frac{q}{\varepsilon}(N_D - N_A + p - n) , \qquad (2.8)$$

$$\frac{\partial p}{\partial t} = -\frac{1}{q}\frac{\partial J_p}{\partial x} + G_T(E) + G_A(n,p,E) + R(n,p) , \qquad (2.9)$$

$$\frac{\partial n}{\partial t} = \frac{1}{q}\frac{\partial J_n}{\partial x} + G_T(E) + G_A(n,p,E) - R(n,p) , \qquad (2.10)$$

$$J_p = qv_p(E)p - qD_p(E)\frac{\partial p}{\partial x} \qquad (2.11)$$

and

$$J_n = qv_n(E)n + qD_n(E)\frac{\partial n}{\partial x} \quad , \tag{2.12}$$

where

$$G_A(n,p,E) = v_p(E)\alpha_p(E)p + v_n(E)\alpha_n(E)n \quad , \tag{2.13}$$

$$G_T(E) = A_T E^2 \exp(-B_T/E) \quad , \tag{2.14}$$

$$R(n,p) = \frac{pn - n_i^2}{\tau_{po}(n + n_1) + \tau_{no}(p + p_1)} \quad , \tag{2.15}$$

$$\alpha_p(E) = a_p \exp\left[-(b_p/E)^{m_p}\right] \quad , \tag{2.16}$$

$$\alpha_n(E) = a_n \exp\left[-(b_n/E)^{m_n}\right] \quad , \tag{2.17}$$

$$A_T = \frac{\sqrt{2}\, q^2 m^{*1/2}}{4\pi^3 \hbar^2 E_g^{1/2}} \quad , \tag{2.18}$$

$$B_T = \frac{\pi m^{*1/2} E_g^{3/2}}{2\sqrt{2}\, q\hbar} \quad , \tag{2.19}$$

E = the electric field intensity (V/cm),

q = the electronic charge (C),

ε = the dielectric constant ($F.cm^{-1}$),

N_D, N_A = the donor and acceptor densities, respectively (cm^{-3}),

p, n = the hole and electron densities, respectively (cm^{-3}),

J_p, J_n = the hole and electron current densities, respectively (A/cm^2),

G_A = the avalanche generation rate ($cm^{-3}.s^{-1}$),

G_T = the tunneling generation rate ($cm^{-3}.s^{-1}$),

R = the recombination rate ($cm^{-3}.s^{-1}$),

v_p, v_n = the hole and electron velocities, respectively (cm/s),

D_p, D_n = the hole and electron diffusion coefficients, respectively (cm^2/s),

α_p, α_n = the hole and electron impact ionization rates, respectively (cm^{-1}),

n_i = the intrinsic carrier density (cm^{-3}),

τ_{po}, τ_{no} = the hole and electron minority carrier lifetimes, respectively (s^{-1}),

p_1, n_1 = the hole and electron densities, respectively, in the conduction band when the single-level trap and fermi level are equal (cm^{-3}),

a_p, b_p, m_p = the hole ionization rate constants, and

a_n, b_n, m_n = the electron ionization rate constants.

In microwave device studies the recombination rate contributions to the current continuity equations are ignored. For the IMPATT mode of operation G_T is assumed to be zero. The electric field profile shown in Fig. 2.1 is assumed for the simple model where E_{M_o} is the generation region electric field, E_{d_o} is the drift region electric field, x_g is the generation region width, and x_d is the drift region width. It is assumed that both holes and electrons have equal ionization rates and saturated velocities for simplicity in the analysis. The total generation rate becomes

$$G_{tot} = G_T(E_M) + v_s\alpha(E_M)[n(x) + p(x)] \quad . \tag{2.20}$$

Neglecting the diffusion term, Eqs. 2.11 and 2.12 yield

$$J_{dc} = J_p + J_n = qv_s[n(x) + p(x)] \quad . \tag{2.21}$$

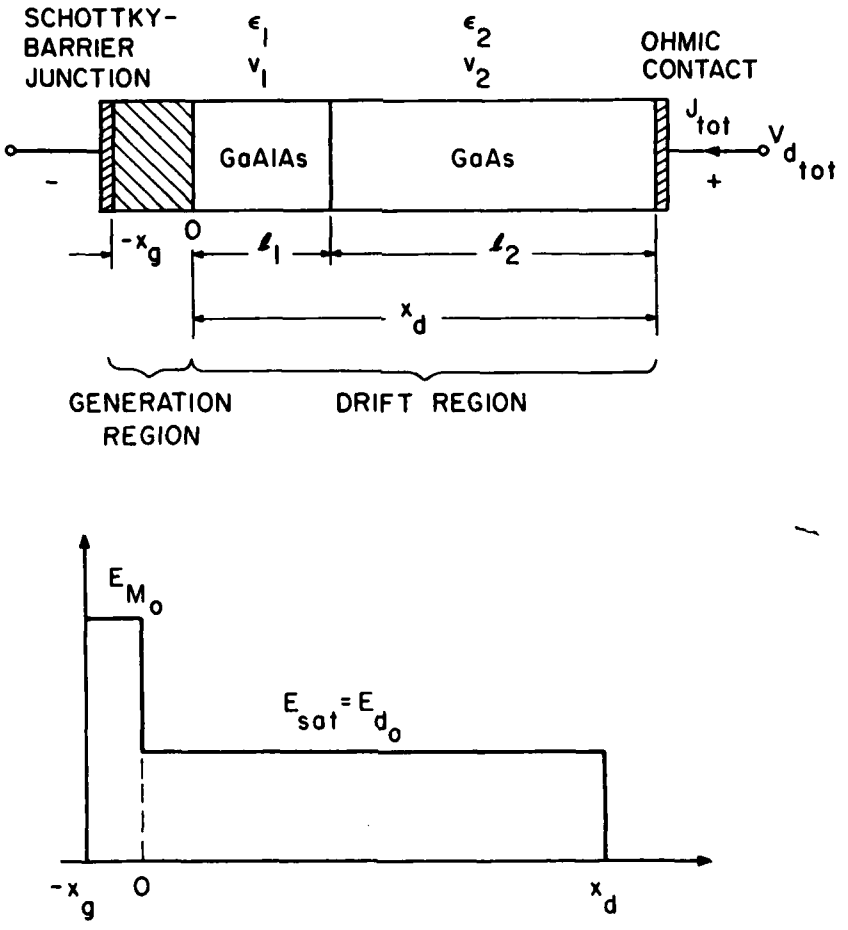


FIG. 2.1 DEVICE STRUCTURE AND ELECTRIC FIELD PROFILE.

Using Eq. 2.21 with the steady-state versions of Eqs. 2.9 and 2.10 gives

$$J_{dc} = \frac{J_s + qx_g G_T(E_{M_o})}{1 - \alpha(E_{M_o})x_g} \quad , \tag{2.22}$$

where J_s is the reverse saturation current density and E_{M_o} is the dc generation region electric field. For mixed breakdown, a multiplication factor can be defined as

$$M_{TA_o} \triangleq \frac{J_{dc}}{J_s} = (1 + M_{T_o})M_{a_o} \quad , \tag{2.23}$$

where

$$M_{T_o} = \frac{qx_g G_T(E_{M_o})}{J_s} \quad . \tag{2.24}$$

M_{T_o} is the tunneling-to-saturation-current ratio and

$$M_{a_o} \triangleq \frac{J_{dc}}{J_s + qx_g G_T(E_{M_o})} = [1 - \alpha(E_{M_o})x_g]^{-1} \quad . \tag{2.25}$$

The analysis of mixed breakdown presented here does not include the effects of "dead space" that are believed to be important for narrow generation regions (i.e., $x_g < 1000$ Å). A more detailed analysis is given by Elta.[11]

2.3 Small-Signal Analysis

The small-signal analysis presented in the following sections follows the approach developed by Gilden and Hines.[12] The current

and field are each composed of a dc part and a small ac variation:

$$J = J_o + J_a e^{i\omega t} \tag{2.26}$$

and

$$E = E_o + e_a e^{i\omega t} \quad , \tag{2.27}$$

where J_o and E_o are the dc values of current and field, respectively, and J_a and e_a are the amplitudes of the ac parts.

2.3.1 Generation Region Impedance of IMPATT Diodes. The impedance of the generation region for an IMPATT diode is calculated from the following equation:

$$\frac{dJ}{dt} = \frac{2J}{\tau}\left(\int_0^{x_g} \alpha \, dx - 1\right) \quad . \tag{2.28}$$

Equation 2.28 relates the current buildup to the ionization rate. Assuming a spatially uniform field in the avalanche region of width x_g yields

$$\frac{dJ}{dt} = \frac{2J}{\tau}(\alpha x_g - 1) \quad . \tag{2.29}$$

The ionization rate can also be approximated by

$$\alpha = \alpha_o + \alpha_a e^{i\omega t} = \alpha_o + \frac{d\alpha}{dE} e_a e^{i\omega t} \tag{2.30}$$

and so

$$\alpha x_g = \alpha_o x_g + \frac{d\alpha}{dE} x_g e_a e^{i\omega t} \tag{2.31}$$

$$= 1 + \frac{d\alpha}{dE} x_g e_a e^{i\omega t} \quad . \tag{2.32}$$

Selecting only the first-order ac terms yields

$$J_a = \frac{2\left(\frac{d\alpha}{dE}\right) x_g J_o e_a}{i\omega\tau_a} \quad . \tag{2.33}$$

The impedance per unit area of the avalanche region is

$$Z_a = \frac{i\omega\tau_a}{2\left(\frac{d\alpha}{dE}\right) J_o} \quad . \tag{2.34}$$

Z_a is, in fact, the impedance of an inductance of magnitude L_a given by

$$L_a = \frac{\tau_a}{2\left(\frac{d\alpha}{dE}\right) J_o} \quad . \tag{2.35}$$

This inductance is in parallel with the depletion-layer capacitance per unit area of the avalanche zone:

$$C_g = \frac{\varepsilon_a}{x_g} \quad . \tag{2.36}$$

The resonant frequency of the LC circuit is called the avalanche resonance frequency ω_a and is given by

$$\omega_a = \left[\frac{2\left(\frac{d\alpha}{dE}\right) x_g J_o}{\varepsilon\tau_a}\right]^{1/2} \quad . \tag{2.37}$$

The total impedance per unit area of the avalanche zone is given by

$$Z_g = \frac{i\omega\tau_a}{2\left(\frac{d\alpha}{dE}\right) J_o \left(1 - \frac{\omega^2}{\omega_a^2}\right)} \quad , \tag{2.38}$$

where τ_a is the carrier transit time across the avalanche zone and is expressed as

$$\tau_a = \frac{x_g}{v_{sat}} \quad . \tag{2.39}$$

2.3.2 Generation Region Impedance of MITATT and TUNNETT Diodes.

The analysis done previously by Elta[11] is followed and the results are stated here without going into detail. The small-signal equivalent circuit for the generation region of a MITATT diode is given in Fig. 2.2. The circuit elements of the equivalent circuit are given by

$$C_g = \frac{\varepsilon_a}{x_g} \quad , \tag{2.40}$$

$$R_a = \left(\frac{V_{go}}{J_o}\right)\left(\frac{1}{m'}\right)\left(\frac{1}{M_{a_o} - 1}\right) \quad , \tag{2.41}$$

$$R_T = \left(\frac{V_{go}}{J_o}\right)\left(\frac{1}{n'}\right)\left(\frac{M_{T_o} + 1}{M_{T_o}}\right) \quad , \tag{2.42}$$

$$L_a = \left(\frac{V_{go}}{J_o}\right)\left(\frac{\tau_g}{2m'}\right)\left(\frac{M_{a_o}}{M_{a_o} - 1}\right) \tag{2.43}$$

and

$$L_T = \left(\frac{V_{go}}{J_o}\right)\left(\frac{\tau_g}{2n'}\right)\left(\frac{M_{T_o} + 1}{M_{T_o}}\right) M_{a_o} \quad . \tag{2.44}$$

The total generation region circuit elements are

$$R_g \triangleq \frac{R_T R_a}{R_T + R_a} \tag{2.45}$$

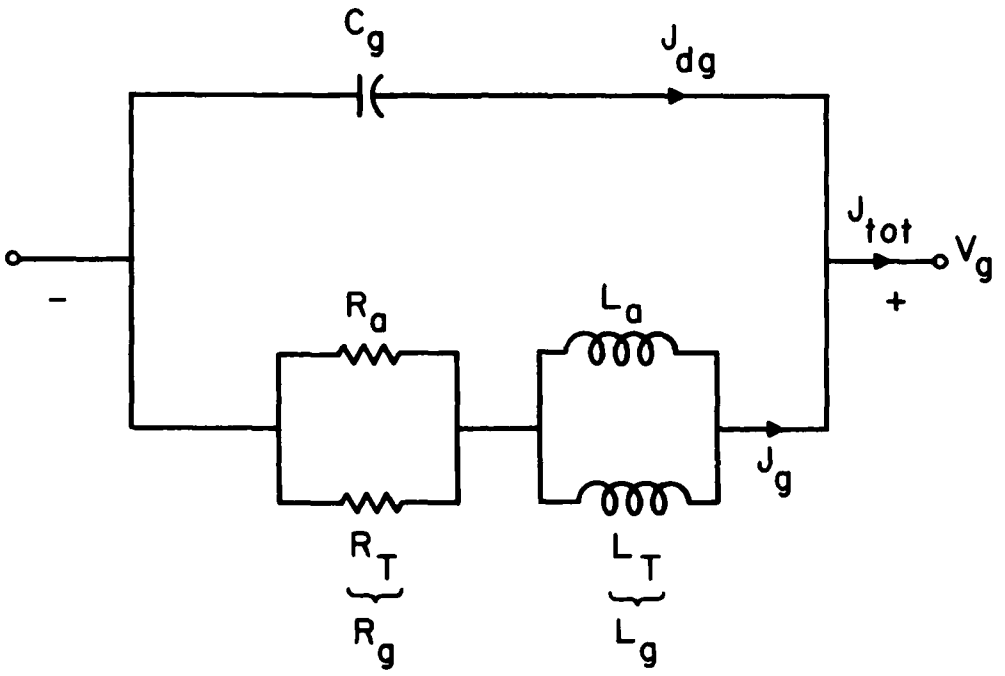


FIG. 2.2 SMALL-SIGNAL EQUIVALENT CIRCUIT OF THE GENERATION REGION.

and

$$L_g \triangleq \frac{L_T L_a}{L_T + L_a} \quad . \tag{2.46}$$

The generation region frequency is defined as

$$\omega_g^2 = \frac{1}{L_g C_g} \quad ,$$

where

$$\omega_g^2 = \left(\frac{1}{C_g \tau_g}\right)\left(\frac{J_o}{V_{go}}\right)\left(m' \frac{M_{a_o} - 1}{M_{a_o}} + n' \frac{M_{T_o}}{M_{T_o} + 1} \frac{1}{M_{a_o}}\right) \quad . \tag{2.47}$$

The various parameters in the preceding equations are

$$V_{go} = E_{m_o} x_g \quad , \tag{2.48}$$

$$m' = m\left(\frac{b}{E_{M_o}}\right)^m \tag{2.49}$$

and

$$n' = \frac{B_T}{E_{M_o}} + 2 \quad , \tag{2.50}$$

where m = 1 for Si and m = 2 for GaAs. The total generation region impedance for the mixed breakdown case is given by

$$Z_g = \frac{R_g + i\omega L_g\left[1 - \left(\frac{\omega}{\omega_g}\right)^2\right] - i\omega C_g R_g^2}{\left(1 - \frac{\omega^2}{\omega_g^2}\right)^2 + \omega^2 C_g^2 R_g^2} \quad . \tag{2.51}$$

2.3.3 Drift Region Impedance of Heterojunction MITATT Diodes.

The total ac current J in the drift zone is the sum of the displacement current and the particle or conduction current injected from the generation zone and can be expressed as

$$J_{tot} = J_c(x,t) + J_d(x,t) \quad . \tag{2.52}$$

The conduction current J_c in the drift zone is related to the injected particle current J_g as

$$J_c(x,t) = J_g\left(t - \frac{x}{v}\right) \quad . \tag{2.53}$$

Assuming a sinusoidal time dependence yields

$$J_c(x) = J_g e^{-i\omega x/v} \quad . \tag{2.54}$$

The ac drift field is given by

$$e(x) = \frac{J_d}{i\omega\varepsilon} \quad . \tag{2.55}$$

When Eq. 2.52 and 2.53 are used, $e(x)$ is given by

$$e(x) = \frac{1}{i\omega\varepsilon}\left(J_{tot} - J_g e^{-i\omega x/v}\right) \quad . \tag{2.56}$$

The injected particle current in the generation region is related to the total current as

$$\frac{J_g}{J_{tot}} = \frac{1}{\left(1 - \frac{\omega^2}{\omega_g^2}\right) + i\omega R_g C_g} \quad . \tag{2.57}$$

When Eq. 2.57 is used, $e(x)$ can be expressed as

$$e(x) = \frac{J_{tot}}{i\omega\varepsilon}\left(1 - \frac{1}{\left(1 - \frac{\omega^2}{\omega_g^2}\right) + i\omega C_g R_g} e^{-i\omega x/v}\right) . \qquad (2.58)$$

Defining $k = k_r + ik_i$ yields

$$k = \frac{1}{\left(1 - \frac{\omega^2}{\omega_g^2}\right) + i\omega C_g R_g} , \qquad (2.59)$$

where

$$k_r = \frac{1 - \frac{\omega^2}{\omega_g^2}}{\left(1 - \frac{\omega^2}{\omega_g^2}\right)^2 + \omega^2 C_g^2 R_g^2} \qquad (2.60)$$

and

$$k_i = -\frac{\omega C_g R_g}{\left(1 - \frac{\omega^2}{\omega_g^2}\right)^2 + \omega^2 C_g^2 R_g^2} . \qquad (2.61)$$

When Eq. 2.59 is used, Eq. 2.58 becomes

$$e(x) = \frac{J_{tot}}{i\omega\varepsilon}\left(1 - ke^{-i\omega x/v}\right) . \qquad (2.62)$$

The voltage across the drift region is obtained by integration of Eq. 2.62. The total current J_{tot} is independent of the distance (x):

$$\int_0^{x_d} e(x)\,dx = \tilde{v} = \frac{J_{tot}}{i\omega}\left[\int_0^{x_d} \frac{1}{\varepsilon}\left(1 - ke^{-i\omega x/v}\right) dx\right] . \qquad (2.63)$$

Evaluating Eq. 2.63 for the heterojunction device as shown in Fig. 2.1 yields the following:

$$Z_D = \frac{\tilde{v}}{J_{tot}} \quad . \tag{2.64}$$

Z_D is the drift region impedance with real and imaginary parts R_D and X_D, respectively:

$$Z_D = R_D + iX_D \quad , \tag{2.65}$$

where

$$Z_D = \frac{1}{i\omega C_D} - \frac{k}{\omega C_1} \frac{e^{-i\theta_1} - 1}{\theta_1} - \frac{k}{\omega C_2} \frac{e^{-i\theta_2} - 1}{\theta_2} e^{-i(\theta_1/\alpha)} \quad , \tag{2.66}$$

$$\theta_1 = \omega \frac{\ell_1}{v_1} \quad , \tag{2.67}$$

$$\theta_2 = \omega \frac{\ell_2}{v_2} \quad , \tag{2.68}$$

$$\alpha = \frac{v_2}{v_1} = \frac{\text{Electron saturated velocity in GaAs}}{\text{Electron saturated velocity in GaAlAs}} \quad , \tag{2.69}$$

$$C_1 = \frac{\varepsilon_1}{\ell_1} \quad , \tag{2.70}$$

$$C_2 = \frac{\varepsilon_2}{\ell_2} \tag{2.71}$$

and

$$C_D = \frac{C_1 C_2}{C_1 + C_2} \quad . \tag{2.72}$$

The first term in Eq. 2.66 is the depletion-layer capacitance of the drift region. The total impedance of the diode is

$$Z_{tot} = Z_D + Z_g \quad , \tag{2.73}$$

which is the sum of the drift and generation region impedances.

2.3.4 Small-Signal Analysis of Heterojunction IMPATT Diodes.

The small-signal impedance equations and dc analysis will be simplified considerably for an IMPATT heterojunction diode. The equations become more tractable for the calculation of the optimum current density for maximum device negative conductance. Therefore, this simple case was used for the analysis. For IMPATT diodes k becomes

$$k = \frac{1}{1 - \frac{\omega^2}{\omega_a^2}} \quad . \tag{2.74}$$

When Eq. 2.74 is substituted into Eq. 2.66 and is rewritten, the heterojunction IMPATT drift region impedance becomes

$$R_D = \frac{1}{\omega\left(1 - \frac{\omega^2}{\omega_a^2}\right)} \left\{ \frac{1 - \cos\theta_1}{C_1\theta_1} + \frac{\cos\left(\frac{\theta_1}{\alpha}\right) - \cos\left(\theta_2 + \frac{\theta_1}{\alpha}\right)}{C_2\theta_2} \right\} \tag{2.75}$$

and

$$X_D = -\frac{1}{\omega C_D} + \frac{1}{\omega\left(1 - \frac{\omega^2}{\omega_a^2}\right)} \left\{ \frac{\sin\theta_1}{C_1\theta_1} + \frac{\sin\left(\theta_2 + \frac{\theta_1}{\alpha}\right) - \sin\left(\frac{\theta_1}{\alpha}\right)}{C_2\theta_2} \right\} \quad . \tag{2.76}$$

$Z_D = R_D + iX_D$ is the drift region impedance. The generation region impedance is given in Section 2.3.1:

$$Z_g = \frac{i\omega\tau_a}{2\left(\frac{d\alpha}{dE}\right)J_o\left(1 - \frac{\omega^2}{\omega_a^2}\right)} \quad . \tag{2.77}$$

Equations 2.75 and 2.76 can be expressed as follows:

$$R_D = \frac{\delta}{\omega\left(1 - \frac{\omega^2}{\omega_a^2}\right)} \tag{2.78}$$

and

$$X_D = \frac{\gamma}{\omega\left(1 - \frac{\omega^2}{\omega_a^2}\right)} - \frac{1}{\omega C_D} \quad , \tag{2.79}$$

where

$$\delta = \frac{1 - \cos\theta_1}{C_1\theta_1} + \frac{\cos\left(\frac{\theta_1}{\alpha}\right) - \cos\left(\theta_2 + \frac{\theta_1}{\alpha}\right)}{C_2\theta_2} \tag{2.80}$$

and

$$\gamma = \frac{\sin\theta_1}{C_1\theta_1} + \frac{\sin\left(\theta_2 + \frac{\theta_1}{\alpha}\right) - \sin\left(\frac{\theta_1}{\alpha}\right)}{C_2\theta_2} \quad . \tag{2.81}$$

The optimum dc current density J_o for maximum device negative conductance can be calculated from the preceding equations. Once the avalanche and drift lengths are specified such that the optimum transit angle ($\theta \cong \pi$) is obtained and the desired operation frequency ω is specified, the avalanche resonance frequency ω_a can be derived which yields the maximum small-signal negative conductance. Since ω_a is related to J_o, the optimum dc current density J_o can be calculated. The generation region impedance is purely reactive thus

$$Z_g = iX_g \quad . \tag{2.82}$$

The device small-signal admittance is

$$Y_{tot} = G_{tot} + iB_{tot} \quad , \tag{2.83}$$

where

$$G_{tot} = \frac{R_D}{R_D^2 + (X_g + X_D)^2} \tag{2.84}$$

and

$$B_{tot} = -\frac{X_g + X_D}{R_D^2 + (X_g + X_D)^2} \quad . \tag{2.85}$$

Following this procedure, the optimum current density is given by

$$J_o = \frac{\frac{\varepsilon_a \omega^2}{2\alpha' v_d}}{1 + \left(\frac{\delta^2 \varepsilon_a^2 + (x_a + \gamma \varepsilon_a)^2}{\left(\frac{\varepsilon_a}{C_D} + x_a \right)^2} \right)^{1/2}} \quad , \tag{2.86}$$

where J_o is in A/cm^2, ε_a is the dielectric constant in F/cm, v_d is the saturated velocity in cm/s, x_a is the avalanche region length in cm, C_D is the depletion region capacitance in F/cm^2, ω is the operating frequency in Hz, and δ and γ are the defined constants in cm^2/F in Eqs. 2.80 and 2.81. The quantity α' is found by first determining ε_a, the field in the avalanche region, such that $\alpha(\varepsilon_a)x_a = 1$. Then $\alpha'(\varepsilon_a)$ is calculated from the ionization rate expression.

2.4 Power and Efficiency Analysis of Heterojunction Two-Terminal Devices

The voltage and current waveforms are idealized to obtain analytic expressions for the power and efficiency of GaAlAs-GaAs-GaAlAs and GaAlAs-GaAs systems. In the following sections, the GaAlAs-GaAs-GaAlAs system is referred to as "a double-heterojunction

device." Similarly, the GaAlAs-GaAs system is referred to as "a single-heterojunction device." In subsequent sections the effects of velocity overshoot and undershoot are examined.

2.4.1 Power and Efficiency of a Double-Heterojunction Device. The voltage and current waveforms are shown in Fig. 2.3 for the transit-time double-heterojunction diode. The angles θ_m and θ_w are the injection angle and the pulse width of the injection current, respectively. θ_D is the total drift transit angle. Since the induced current is directly proportional to the saturated velocities of the carriers in the drift regions, the current ratio in two different regions can be expressed as

$$\alpha = \frac{I_2}{I_1} = \frac{v_{2sat}}{v_{1sat}} , \tag{2.87}$$

where I_2 and v_{2sat} are the current and saturated velocity of electrons in Region 2 (GaAs) and I_1 and v_{1sat} are the current and saturated velocity of electrons in Region 1 (GaAlAs), respectively. The dc current is

$$I_{dc} = \frac{1}{2\pi} \int_0^{2\pi} I_{ind}(\omega t)\, d(\omega t) . \tag{2.88}$$

Evaluating Eq. 2.88 for the given waveforms in Fig. 2.3 results in

$$I_{dc} = \frac{1}{2\pi}\left[\frac{\theta_D}{\alpha} + \frac{\alpha - 1}{\alpha}(\theta_{h_2} - \theta_{h_1})\right] I_1 , \tag{2.89}$$

where θ_{h_1} and θ_{h_2} are the injection angles for the first and second heterojunction interfaces, respectively. These junction injection

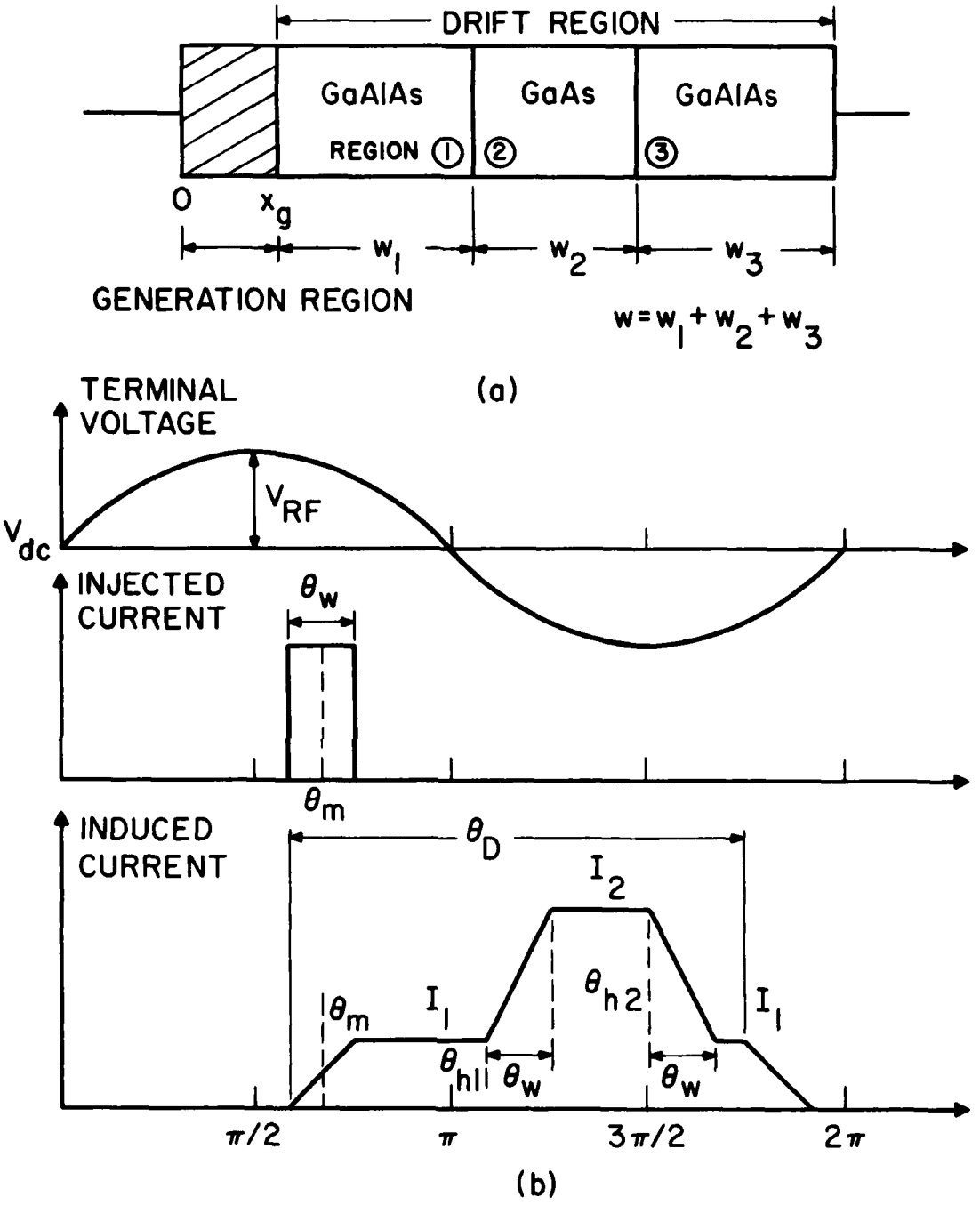


FIG. 2.3 (a) GaAlAs-GaAs-GaAlAs DOUBLE-HETEROJUNCTION TWO-TERMINAL TRANSIT-TIME DEVICE. (b) TERMINAL VOLTAGE, INJECTED CURRENT AND INDUCED CURRENT FOR THE DEVICE.

angles are given by

$$\theta_{h_1} = \theta_m - \frac{\theta_w}{2} + \omega\tau_{h_1} \tag{2.90}$$

and

$$\theta_{h_2} = \theta_{h_1} + \omega\tau_{h_2} \quad ,$$

where τ_{h_1} and τ_{h_2} are the transit times in Region 1 and Region 2, respectively, given by

$$\tau_{h_1} = \frac{w_1}{v_{1\,sat}} \tag{2.91}$$

and

$$\tau_{h_2} = \frac{w_2}{v_{2\,sat}} \quad , \tag{2.92}$$

where w_1 and w_2 are the lengths of the GaAlAs (Region 1) and GaAs (Region 2) layers, respectively.

The power efficiency is given by

$$\eta_p = \frac{P_{RF}}{P_{dc}} = \frac{V_{RF}}{V_{dc}} \eta_n \quad , \tag{2.93}$$

where P_{RF} is the RF power, P_{dc} is the dc power, and η_n is the normalized efficiency. P_{RF} and P_{dc} are given by

$$P_{RF} = \frac{1}{2\pi} \int_0^{2\pi} I_{ind}(\omega t) V_{RF} \sin(\omega t)\, d(\omega t) \tag{2.94}$$

and

$$P_{dc} = V_{dc} I_{dc} \quad . \tag{2.95}$$

Evaluating Eq. 2.94 for the waveforms given in Fig. 2.3 and substituting Eqs. 2.89 and 2.95 into Eq. 2.93 results in

$$\eta_n = \left| \frac{\sin \frac{\theta_w}{2}}{\frac{\theta_w}{2}} \right| \cdot \frac{\frac{1}{\alpha}[\cos \theta_m - \cos (\theta_D + \theta_m)] + \frac{\alpha - 1}{\alpha}\left[\cos \left(\theta_{h_1} + \frac{\theta_w}{2}\right) - \cos \left(\theta_{h_2} + \frac{\theta_w}{2}\right)\right]}{\frac{\theta_D}{\alpha} + \frac{\alpha - 1}{\alpha}(\theta_{h_2} - \theta_{h_1})} , \tag{2.96}$$

where θ_D is the drift transit angle given by

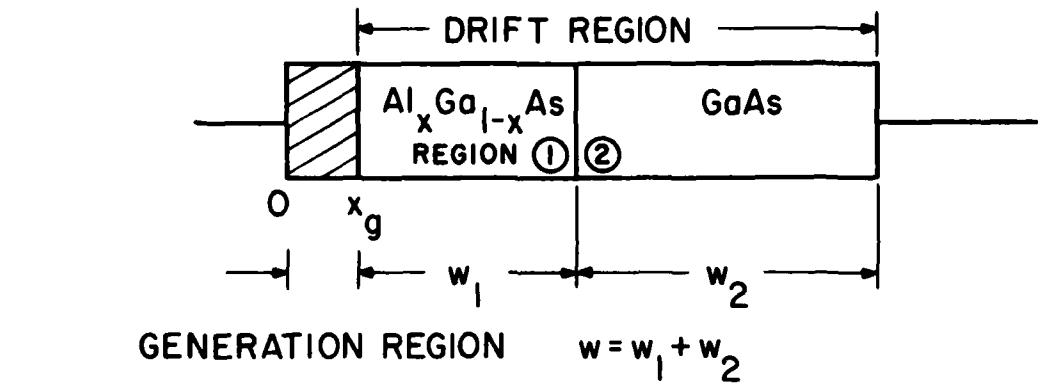
$$\theta_D = \frac{1}{v_{1sat}} [w_1 + \alpha(w_2 + w_3)] \quad . \tag{2.97}$$

For $\alpha = 1$ the familiar equation for a homojunction transit-time device is obtained:

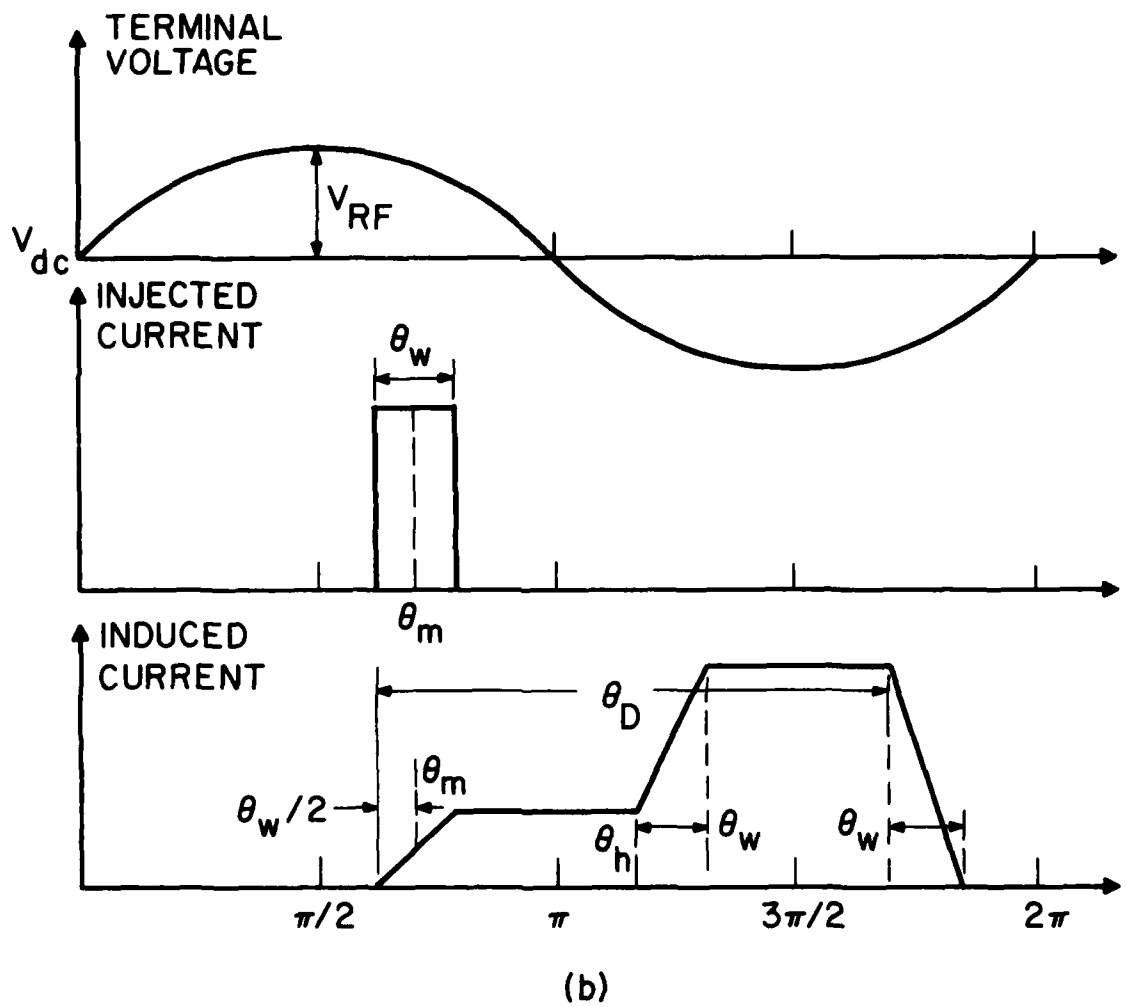
$$\eta_n = \left| \frac{\sin \frac{\theta_w}{2}}{\frac{\theta_w}{2}} \right| \left| \frac{\cos \theta_m - \cos (\theta_D + \theta_m)}{\theta_D} \right| \quad . \tag{2.98}$$

2.4.2 Power and Efficiency of a Single-Heterojunction Diode.

The voltage and current waveforms for the single-heterojunction diode are given in Fig. 2.4. The normalized efficiency can be obtained from the previous results by substituting θ_{h_1} and θ_{h_2}



(a)



(b)

FIG. 2.4 (a) GaAlAs-GaAs HETEROJUNCTION TWO-TERMINAL TRANSIT-TIME DEVICE. (b) TERMINAL VOLTAGE, INJECTION CURRENT AND INDUCED CURRENT FOR THE DEVICE IN (a), RESPECTIVELY. (α = 3)

as follows:

$$\theta_{h_1} = \theta_h \tag{2.99}$$

and

$$\theta_{h_2} = \theta_D + \theta_m - \frac{\theta_w}{2} \quad . \tag{2.100}$$

The power and efficiency of a single-heterojunction diode are obtained by substituting Eqs. 2.99 and 2.100 into Eq. 2.96:

$$\eta_n = \left(\frac{\sin\frac{\theta_w}{2}}{\frac{\theta_w}{2}}\right)\frac{\frac{1}{\alpha}\cos\theta_m - \cos(\theta_D + \theta_m) + \frac{\alpha - 1}{\alpha}\cos\left(\theta_h + \frac{\theta_w}{2}\right)}{\frac{1-\alpha}{\alpha}\left(\theta_h + \frac{\theta_w}{2} - \theta_m\right) + \theta_D} \quad , \tag{2.101}$$

where

$$\theta_h = \theta_m - \frac{\theta_w}{2} + \omega\frac{w_1}{v_{1sat}} \tag{2.102}$$

and

$$\theta_D = \frac{1}{v_{1sat}}\left(w_1 + \frac{w_2}{\alpha}\right)\omega \quad . \tag{2.103}$$

2.4.3 Calculation of the Optimum Drift Angles for Maximum Efficiency. In this section the numerical results obtained from a computer program that calculates the optimum angles and corresponding maximum efficiency are given. Since θ_m and θ_w can be considered constant for a given device and its mode of operation, the power efficiency is optimized to have a maximum value for the variables θ_{h_1}, θ_{h_2} and θ_D. The computer program calculates the optimum angles θ_{h_1}, θ_{h_2}, and θ_D and the corresponding maximum efficiency using the conjugate gradient method developed by Fletcher and Reeves.[13]

Table 2.1 gives the numerical results for TUNNETT, MITATT and IMPATT heterojunction diodes obtained from the computer program. The results show that the power efficiency for MITATT and TUNNETT diodes can be improved greatly if heterojunction diodes are used. The first set of data in Table 2.1 is for the idealized case where θ_w, the pulse width, is assumed to be zero. In the second set of data, the injection angles and pulse widths are taken from Elta.[11] The relative efficiency improvement is calculated as

$$\eta_{rel} = \frac{\eta_{hetero} - \eta_{homo}}{\eta_{homo}} , \qquad (2.104)$$

where η_{hetero} and η_{homo} are the normalized efficiencies of the heterojunction and homojunction transit-time devices, respectively. A heterojunction TUNNETT operating at 100 GHz would have a relative efficiency improvement of 83 percent in which the power efficiency is almost doubled for $\alpha = 3$.

Figure 2.5 gives the idealized current-voltage waveforms for single- and double-heterojunction TUNNETTs. The transit angle is $\theta_D = 3\pi/2$. The results show that the difference between the maximum power efficiencies of single- and double-heterojunction TUNNETTs is small, which suggests that there would not be much improvement in power efficiency by using double-heterojunction over single-heterojunction devices.

In conclusion, the optimum drift angles and corresponding maximum power efficiencies were calculated for single- and double-heterojunction diodes. The obtained numerical results can be used as a guideline for the design of heterojunction devices.

Table 2.1

Numerical Results for TUNNETT, MITATT and IMPATT Heterojunction Diodes

	Frequency (GHz)	Diode Mode	Injection Angle θ_m (Degrees)	Pulse Width θ_w (Degrees)	Drift Angle θ_D (Degrees)	Junction Angle θ_h (Degrees)	Normalized Efficiency $\alpha = 3$ (Heterojunction)	Normalized Efficiency $\alpha = 1$ (Homojunction)	Relative Efficiency Improvement Over Homojunction (Percent)
α=1	Ideal	IMPATT	180.00	0	133.5626	--	--	- 0.7246	15
α=3	Ideal	IMPATT	180.00	0	123.2198	236.7503	- 0.8366	--	
α=1	Ideal	TUNNETT	90.00	0	257.4526	--	--	- 0.2172	138
α=3	Ideal	TUNNETT	90.00	0	238.8700	211.1002	- 0.5170	--	
α=1	Ideal	MITATT	135.00	0	197.4531	--	--	- 0.4625	46
α=3	Ideal	MITATT	135.00	0	182.4843	222.4858	- 0.6758	--	
α=1	10	IMPATT*	180.00	75.0	133.5626	--	--	- 0.6740	15
α=3	10	IMPATT*	180.00	75.0	123.2198	199.2790	- 0.7781	--	
α=1	100	TUNNETT*	110.1509	75.0	231.1745	--	--	- 0.2978	83
α=3	100	TUNNETT*	110.1509	75.0	214.0381	178.3098	- 0.5442	--	
α=1	100	MITATT*	164.8453	93.0023	155.4120	--	--	- 0.5714	25
α=3	100	MITATT*	164.8453	93.0023	143.4385	185.2138	- 0.7016	--	
α=1	100	IMPATT*	180.00		134.0114	--	--	- 0.4982	35
α=3	100	IMPATT*	180.00		103.2965	222.1783	- 0.6714	--	

*Data taken from Elta.[11]

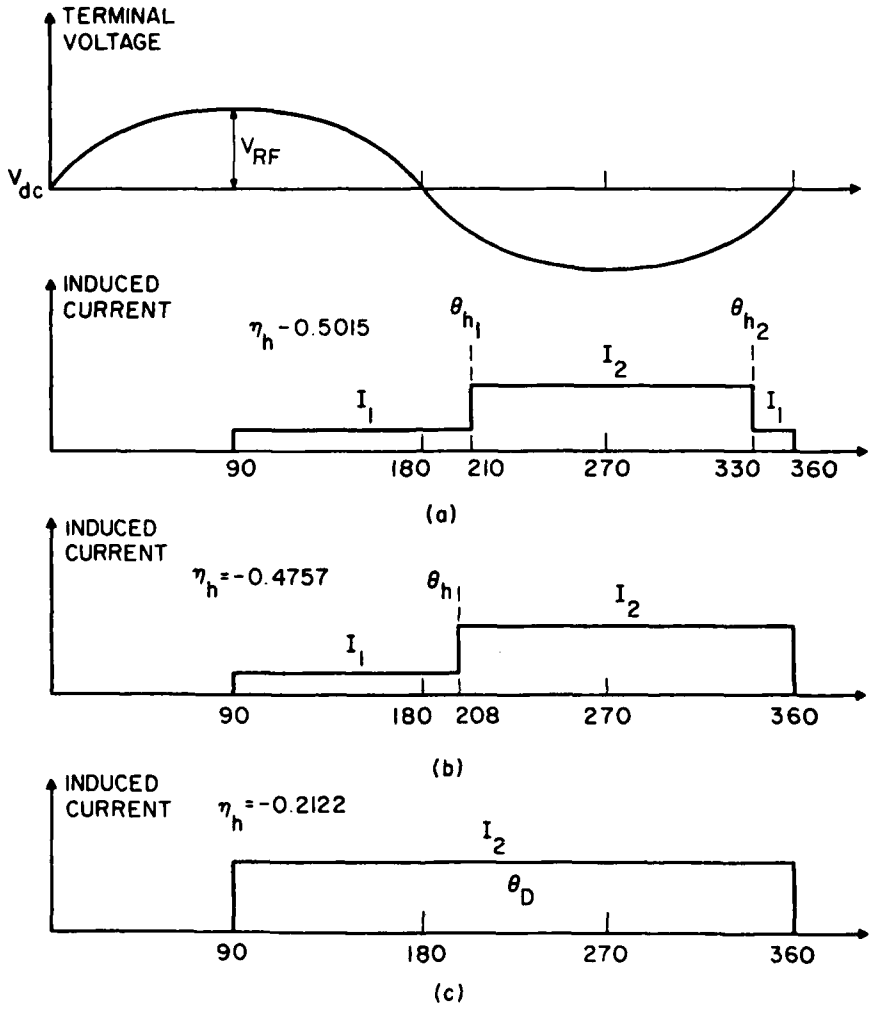


FIG. 2.5 THE IDEALIZED VOLTAGE AND CURRENT WAVEFORMS FOR (a) DOUBLE-HETEROJUNCTION TUNNETT, (b) SINGLE-HETEROJUNCTION TUNNETT, AND (c) MONOJUNCTION TUNNETT. THE OPTIMUM TRANSIT ANGLES ARE θ_{h_1} = 210, θ_{h_2} = 330, θ_h = 208, AND θ_D = 270 DEGREES. α = 3 WHERE $\alpha = (I_2/I_1)$. THE NORMALIZED MAXIMUM POWER EFFICIENCIES ARE η_h = - 0.5015, - 0.4757, AND - 0.2122, RESPECTIVELY.

2.5 Power and Efficiency Analysis for Heterojunction Two-Terminal Devices Including the Overshoot Effect

In the previous section, a simple and approximate power and efficiency analysis was given for double- and single-heterojunction devices. In this section, the overshoot effect is included in the previous analysis and a comparison is given between the two cases.

2.5.1 Power and Efficiency Analysis for Double-Heterojunction Devices Including the Overshoot Effect.

The voltage and current waveforms, including the velocity overshoot, are given in Fig. 2.6 and are idealized for simple analysis. The overshoot angle θ_{ov} is defined as

$$\theta_{ov} = \omega\tau_{ov} \quad , \tag{2.105}$$

where ω is the operating frequency in Hz and τ_{ov} is the average overshoot time in seconds. The induced current ratio of the overshoot and GaAlAs regions is defined as

$$\alpha_2 = \frac{I_3}{I_1} = \frac{v_{ov}}{v_{1sat}} \quad , \tag{2.106}$$

where v_{ov} is the overshoot velocity of the carriers and v_{1sat} is the saturated velocity of carriers in GaAlAs. Similarly, the induced current ratio of the GaAs and GaAlAs regions is defined as

$$\alpha_1 = \frac{I_2}{I_1} = \frac{v_{2sat}}{v_{1sat}} \quad , \tag{2.107}$$

where v_{2sat} is the saturated velocity of carriers in GaAs. The dc current is given by

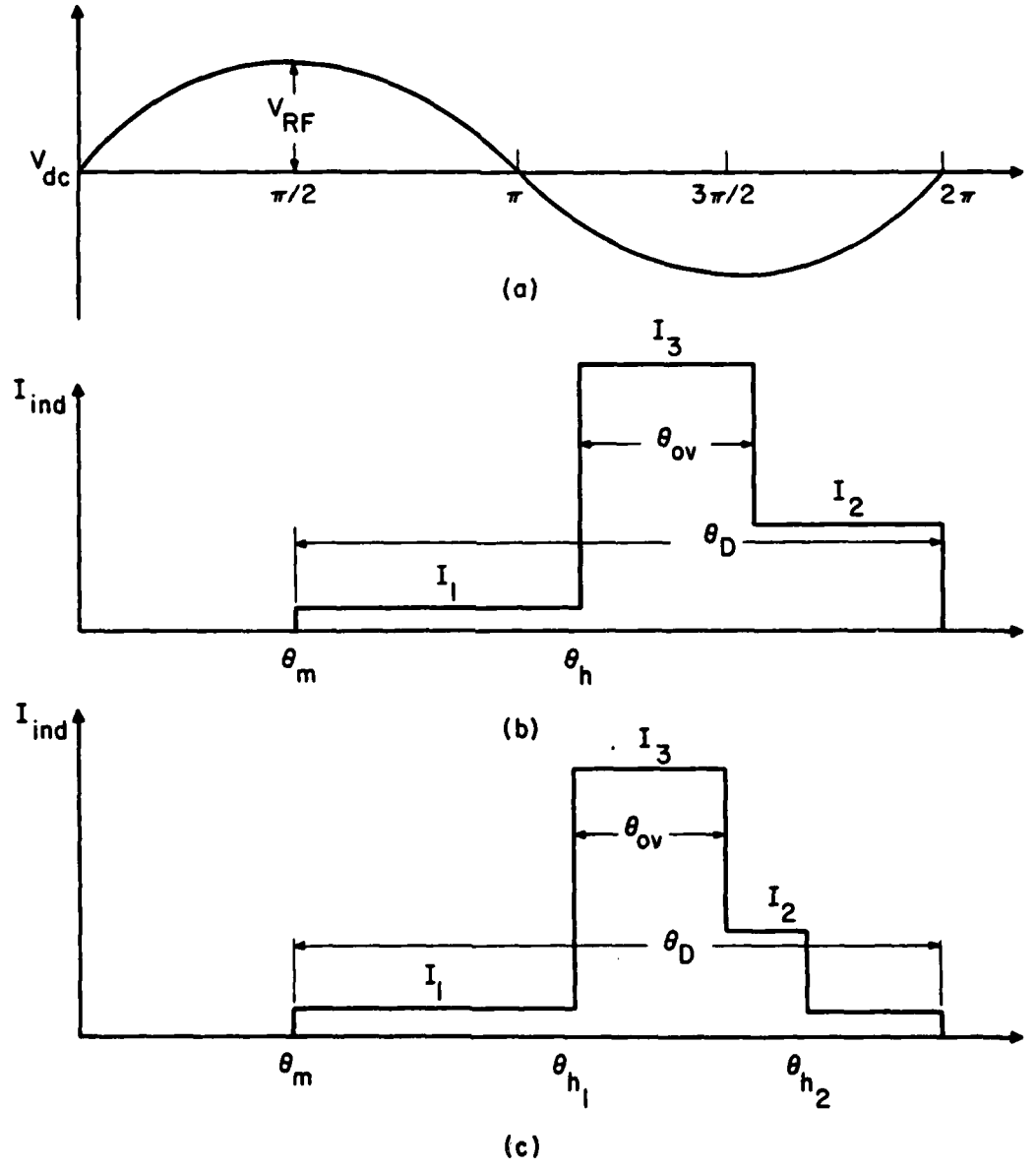


FIG. 2.6 IDEALIZED INDUCED CURRENT AND VOLTAGE WAVEFORMS. (a) APPLIED TERMINAL VOLTAGE, (b) INDUCED CURRENT FOR SINGLE HETEROJUNCTION, AND (c) INDUCED CURRENT FOR DOUBLE HETEROJUNCTION.

$$I_{dc} = \frac{1}{2\pi}\int_0^{2\pi} I_{ind}(\omega t)\, d(\omega t) \quad . \tag{2.108}$$

Evaluating Eq. 2.108 for the waveforms shown in Fig. 2.6 gives

$$I_{dc} = \frac{(1 - \alpha_1)(\theta_{h_1} - \theta_{h_2}) + (\alpha_2 - \alpha_1)\theta_{ov} + \theta_D}{2\pi} I_1 \quad , \tag{2.109}$$

where

$$\theta_{h_1} = \theta_m + \omega\tau_{h_1} \quad , \tag{2.110}$$

$$\theta_{h_2} = \theta_{h_1} + \omega\tau_{h_2} \tag{2.111}$$

and

$$\theta_D = \theta_{h_2} + \omega\tau_{h_3} - \theta_m \quad . \tag{2.112}$$

The transit times in various regions of the diode are given by the following equations:

$$\tau_{h_1} = \frac{w_1}{v_{1sat}} \quad , \tag{2.113}$$

$$\tau_{h_2} = \frac{w_2}{v_{2sat}} + \tau_{ov}\left(1 - \frac{\alpha_2}{\alpha_1}\right) \tag{2.114}$$

and

$$\tau_{h_3} = \frac{w_3}{v_{1sat}} \quad , \tag{2.115}$$

where w_1 is the length of the GaAlAs layer, w_2 is the length of the GaAs layer, and w_3 is the length of the GaAlAs layer. The dc and RF powers are given by

$$P_{dc} = V_{dc} I_{dc} \tag{2.116}$$

and

$$P_{RF} = \frac{1}{2\pi} \int_0^{2\pi} I_{ind}(\omega t) V_{RF} \sin(\omega t)\, d(\omega t) \quad . \tag{2.117}$$

The power efficiency is given by

$$\eta = \frac{V_{RF}}{V_{dc}} \eta_n \quad . \tag{2.118}$$

Evaluating Eq. 2.117 and substituting into Eq. 2.118 result in the normalized power efficiency given by

$$\eta_n = \frac{\left[\begin{array}{l} \cos\theta_m - \cos(\theta_D + \theta_m) + (\alpha_2 - 1)\cos\theta_{h_1} \\ + (1 - \alpha_1)\cos\theta_{h_2} + (\alpha_1 - \alpha_2)\cos(\theta_{h_1} + \theta_{ov}) \end{array}\right]}{(1 - \alpha_1)(\theta_{h_1} - \theta_{h_2}) + (\alpha_2 - \alpha_1)\theta_{ov} + \theta_D} \quad . \tag{2.119}$$

2.5.2 Power and Efficiency Analysis for a Single-Heterojunction Device Including the Overshoot Effect. Following the same type of analysis of the previous section and evaluating the power and efficiency expressions for the voltage-current waveforms given in Fig. 2.6a and b result in the normalized efficiency expression given by

$$\eta_n = \frac{\left[\begin{array}{l} \cos\theta_m - \alpha_1 \cos(\theta_D + \theta_m) + (\alpha_2 - 1)\cos\theta_h \\ - (\alpha_2 - \alpha_1)\cos(\theta_h + \theta_{ov}) \end{array}\right]}{(\alpha_1 - 1)(\theta_m - \theta_h) + (\alpha_2 - \alpha_1)\theta_{ov} + \alpha_1\theta_D} \quad , \tag{2.120}$$

$$\theta_h = \theta_m + \omega\tau_h \tag{2.121}$$

and

$$\theta_D = \theta_h + \theta_{ov}\left(1 - \frac{\alpha_2}{\alpha_1}\right) + \omega \frac{w_2}{v_{2sat}} \quad , \tag{2.122}$$

where

$$\tau_h = \frac{w_1}{v_{1sat}} \quad . \tag{2.123}$$

The parameters w_1 and w_2 are the drift region lengths of GaAlAs and GaAs, respectively.

2.5.3 Computer Program Results. A computer program was written for the optimization of the normalized efficiency for single- and double-heterojunction diodes. The junction angles θ_{h_1}, θ_{h_2} and θ_h and the drift angle θ_D are calculated for θ_m, θ_{ov} and α_1,α_2 as parameters. The presented results are for the TUNNETT mode of operation where θ_m = 90 degrees. Zero overshoot time corresponds to the previous case discussed earlier (no overshoot effects).

Figure 2.7 shows the variation of the normalized efficiency as a function of the overshoot time τ_{ov} for a single-heterojunction diode. As can be seen from Fig. 2.7, the normalized power efficiency becomes independent of α_1 (the saturated velocity ratios of GaAs and GaAlAs) for large overhoot times. In this calculation and others f = 100 GHz and τ_{ov} = 0 to 2.0 ps are assumed.

A similar analysis was carried out for the double-heterojunction diode and similar conclusions were obtained.

Figure 2.8 shows the variation of the normalized power efficiency η_n and the junction angle θ_h for different α_2 values for the

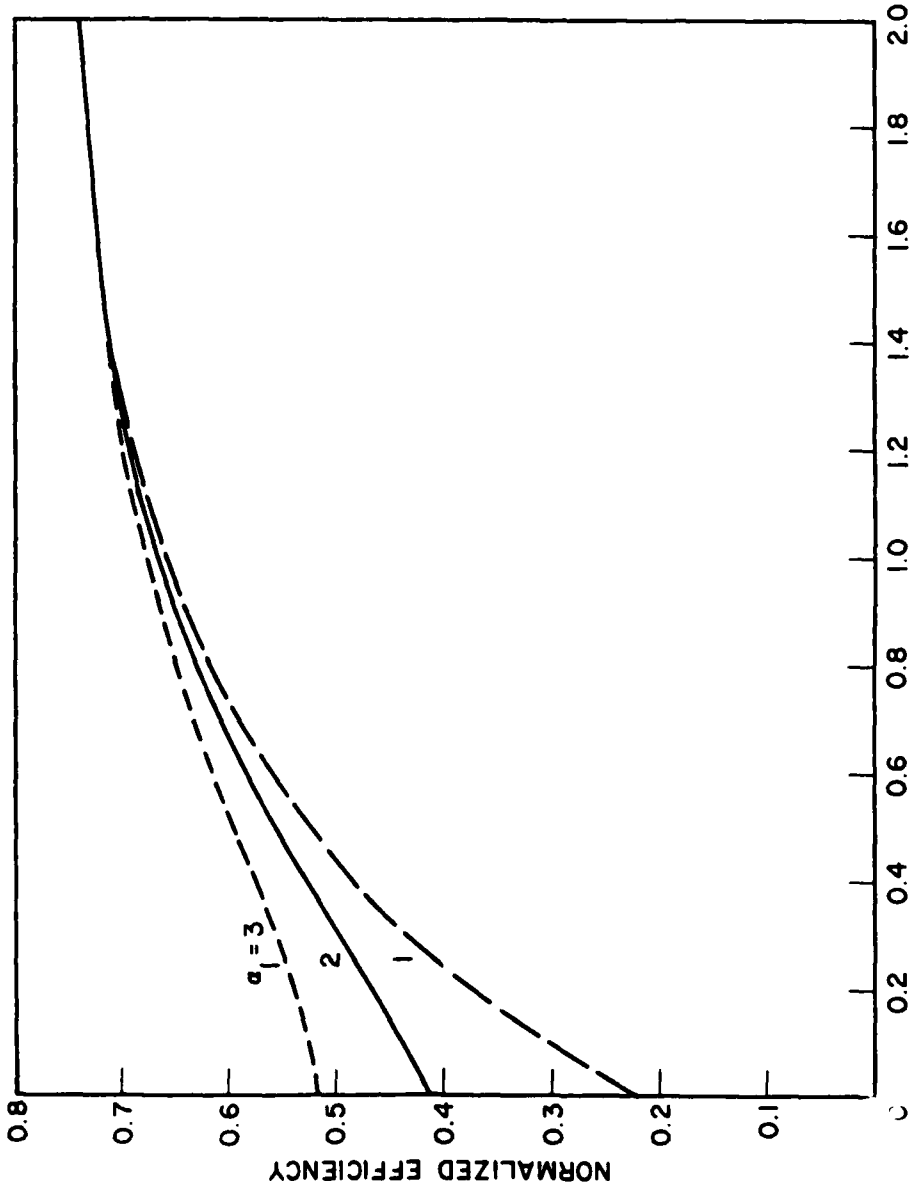
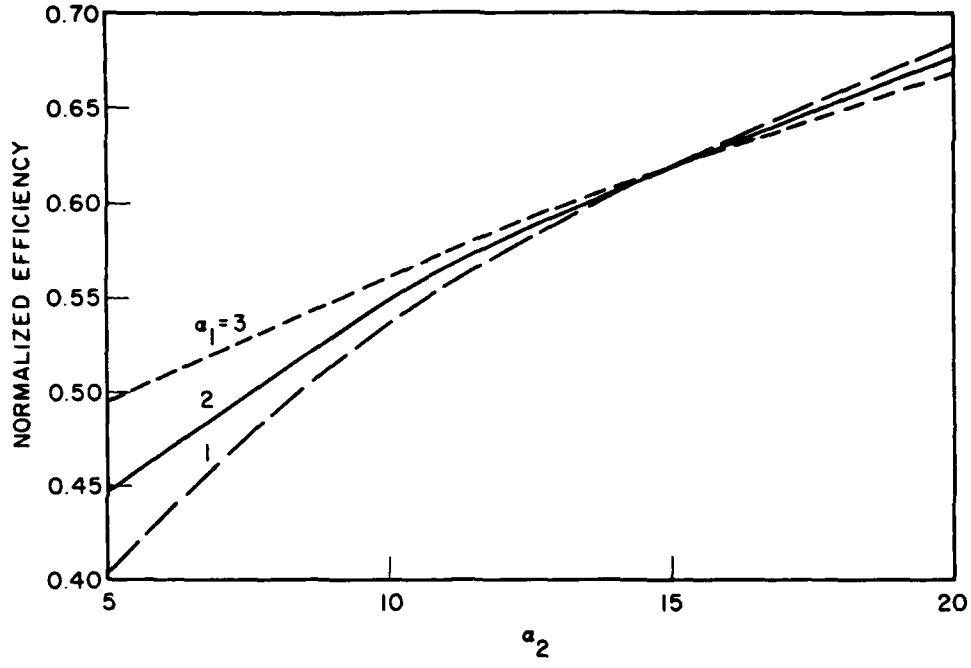
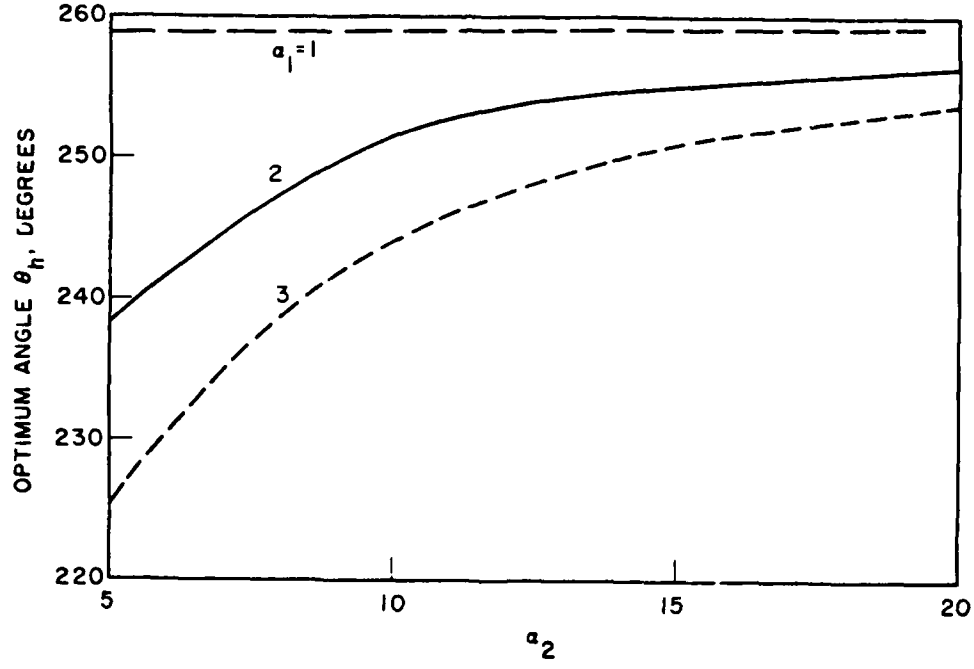


FIG. 2.7 NORMALIZED EFFICIENCY WITH τ_{ov}, α_2, AND α_1 AS PARAMETERS FOR A SINGLE-HETEROJUNCTION DIODE. (θ_h AND θ_D ARE OPTIMIZED



(a)



(b)

FIG. 2.8 (a) VARIATION OF NORMALIZED POWER EFFICIENCY AND (b) JUNCTION ANGLE θ_h WITH α_2 AS A PARAMETER FOR A SINGLE-HETEROJUNCTION DIODE.

single-heterojunction diode. For large values of α_2, the normalized efficiency η_n and the junction angle θ_h become independent of α_1. For this case the overshoot time was fixed at $\tau_{ov} = 0.6$ ps.

Figure 2.9 shows the results obtained for three different cases. Curve a shows the efficiency of the diode with overshoot effects considered in the design of the diode. Curve b shows the efficiency with θ_h chosen without considering the overshoot effect and the overshoot is present in the operation of the diode. Finally, curve c shows the efficiency without any optimization in the design at all. In conclusion, the velocity overshoot, if present in the device operation, changes the performance of the diode. It was shown that for large overshoot velocities and overshoot times the diode performance is dominated by the velocity overshoot effects. The diode performance is almost independent of α_1 (carrier saturated velocity ratio of GaAs and GaAlAs) for the heterojunction diodes.

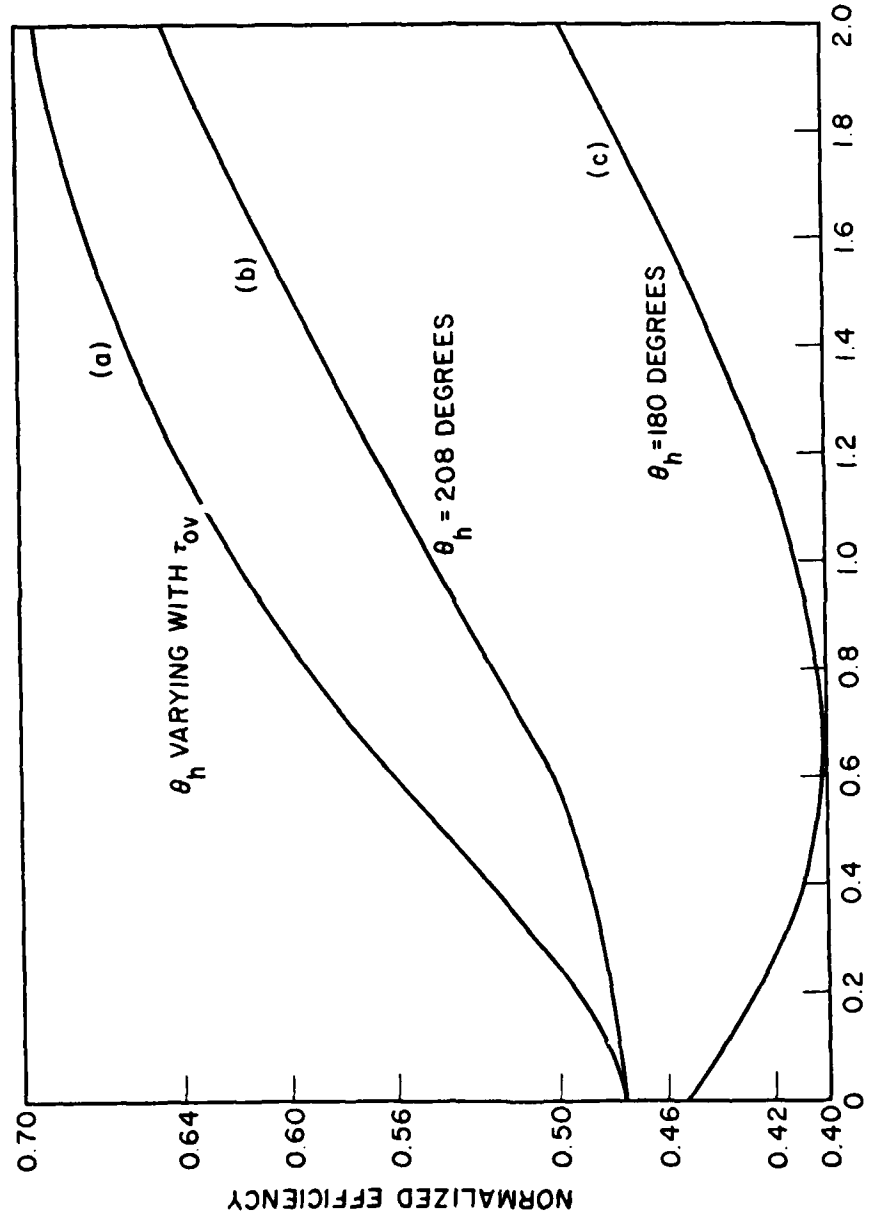


FIG. 4.3 VARIATION OF NORMALIZED POWER EFFICIENCY FOR A SINGLE-HETEROJUNCTION DEVICE FOR THREE DIFFERENT CASES. (a) θ_h IS OPTIMIZED INCLUDING OVERSHOOT EFFECTS, (b) θ_h = 208 DEGREES IS CHOSEN WITHOUT OVERSHOOT EFFECTS CONSIDERED AND OVERSHOOT IS PRESENT, AND (c) SAME AS (b) EXCEPT θ_h = 180 DEGREES.

CHAPTER III. PROCESS DEVELOPMENT FOR GaAs IMPATT DIODES

3.1 Introduction

In the previous chapters, the general structure and the theoretical performance of GaAs double-drift millimeter-wave IMPATT and GaAs-GaAlAs millimeter-wave MITATT diodes were presented. This chapter contains a discussion of the various processing steps involved in the fabrication of millimeter-wave GaAs IMPATT diodes. Previous fabrication processes developed during the 1970s are briefly discussed. Ohmic and Schottky contacts to GaAs are the most important steps for device fabrication. Their quality greatly influences the device performance. The first two sections of this chapter contain a discussion of these processes. In every semiconductor device fabrication at least one or more processing steps involve wet or dry chemical etching of the semiconductor material. Etching of GaAs and GaAlAs is discussed in a subsequent section. Finally, the proton bombardment developed during this work is presented in detail.

3.2 Earlier Fabrication Processes

The first successful Read IMPATT diode was fabricated by Lee et al.[3] in 1965. About the same time, Johnston et al.[4] reported obtaining microwave oscillations from a p-n junction diode. Due to technological difficulties in the growth of epitaxial layers and doping these layers to form a p-n junction, the earlier challenges were in the control of the doping profile and layer thicknesses. The first millimeter-wave diodes reported[14] had thick Si layers

that resulted in large parasitic resistance due to the skin effect. To reduce the parasitic resistance, a "dimple" was etched from the back side of the slice and a cup-shaped metallization was formed. Most earlier diodes were fabricated from Si followed by the introduction of GaAs IMPATT diodes. In GaAs IMPATTs the p^+ regions were formed by diffusing Zn into n-type material grown by either liquid or vapor-phase epitaxial growth. Diffusion of Zn into GaAs is a very unreliable process and it was very difficult to control the doping profile of the diodes. Recent developments in molecular beam epitaxy (MBE) and ion implantation have resulted in excellent doping profile control and material quality. Typical semiconductor material thicknesses for GaAs and Si millimeter-wave IMPATTs are of the order of 1 to 5 μm. This reduces the parasitic series resistance due to the n^+ bulk material and skin effects. An excellent collection of papers covering the earlier work in IMPATT diodes is presented by Haddad.[15]

3.3 Ohmic Contact Formation on GaAs

The quality of an ohmic contact for GaAs devices is one of the most significant factors affecting the performance of the devices. This is particularly true for small geometry devices, such as GaAs millimeter-wave IMPATTs and MESFETs. Rideout[16] provided an excellent theoretical treatment of ohmic contacts to GaAs. Ohmic contacts should have the following properties:

1. Low specific contact resistance.
2. Good surface morphology.
3. Reliability, long-term stability.

Specific contact resistivity largely depends on the doping concentration of the semiconductor material, alloying temperature and alloying cycle, and ohmic contact metallization used in the process.

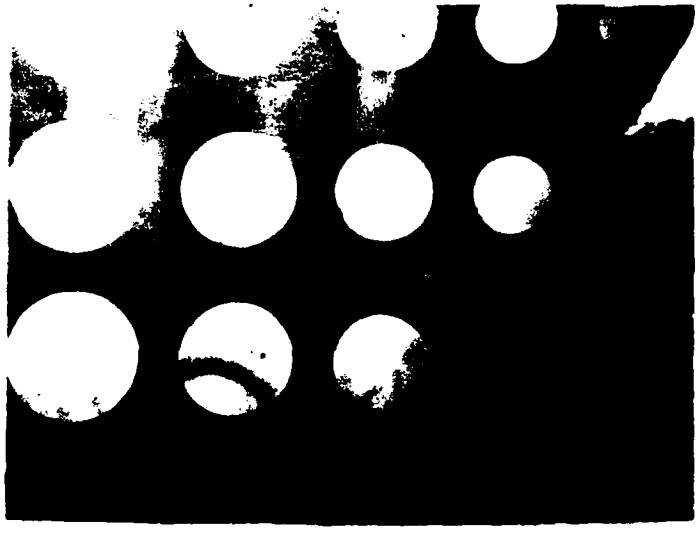
Surface preparation before the deposition of the contact metal also affects the quality of the ohmic contact. For n-type GaAs, a most commonly used and mature process is the Au-Ge/Ni/Au ohmic contact process. Wittmer et al.[17] studied the interaction of these three elements on heat treatment using an inert substrate. Their work and the work of many other researchers indicated that Ge diffuses into GaAs resulting in a highly doped n^+-layer very close to the metal contact interface. It is also speculated that Ni acts as a wetting agent. The typical alloying temperature is approximately 450°C and the alloying cycle is from 2 to 4 min. Recently IR lamp alloying was proposed by Gill et al.[18] as an alternative to conventional strip heater annealing. Mojzes[19] proposed a new "face down" alloying method to shorten the cooling cycle. His results have not improved the previous results obtained by the conventional alloying technique.

Since typical millimeter-wave IMPATT diodes have contact diameters approximately 20 to 35 μm, low specific contact resistance is very important to reduce the parasitic series resistance. For the reasons mentioned previously, the quality of the ohmic contacts was investigated prior to the IMPATT diode fabrication process. The specific contact resistance of the ohmic contact was evaluated by the method developed by Cox and Strack.[20] Circular patterns of Au-Ge/Ni/Au multilayer metals with varying diameters were formed

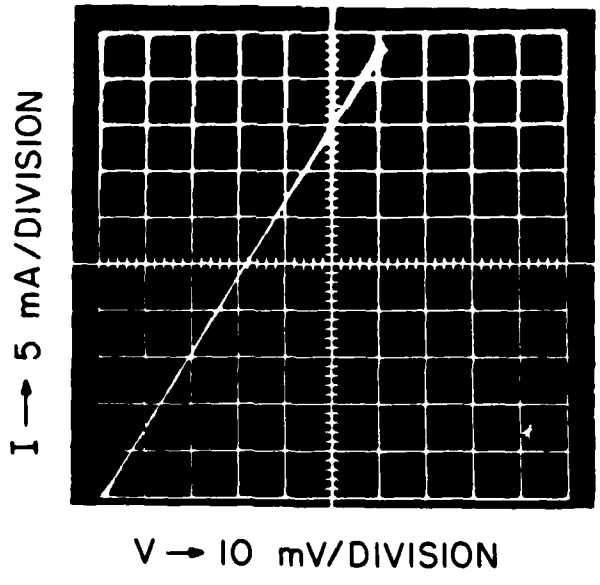
on n-n^+ GaAs substrates. The back side of the wafer was also metallized by a Au-Ge/Ni/Au ohmic contact that was a common ground to the circular ohmic contacts on the epitaxial side. The wafer was annealed at 475°C for 2 min under forming gas and the surface morphology after annealing was still smooth. A specific contact resistance ρ_c of 3×10^{-6} Ω-cm^2 was obtained by curve fitting the measured data. This compares favorably with the published state-of-the-art results. Figure 3.1a shows the ohmic dot patterns with different diameters and Fig. 3.1b shows the curve-tracer photograph of the I-V characteristic of the ohmic contact after alloying.

Since most GaAs semiconductor devices, such as MESFET and Schottky GaAs diodes, require an ohmic contact to n-GaAs there have been extensive studies of this contact during the last 15 years. This is certainly not true for ohmic contacts to p-type GaAs layers. The most common ohmic contact to a GaAs p-type layer is the Au-Zn (99:1) one which can be electroplated on the GaAs surface. The alloying temperature is higher for the Zn-Au ohmic contact which is typically 550°C. In the past, Zn diffusion was used to form a p^+-n junction on an n-GaAs epitaxial layer. Since p^+-layers can have concentrations close to 5 to 10 x 10^{18} cm^{-3}, Ti/Au metallization is used as an ohmic contact. This metal forms a tunneling type contact to the heavily doped p-layer near the diode surface. Such a contact behaves very much like an "ohmic contact."

In some cases, it is detrimental to the device characteristics to anneal the wafer at 475°C to form an ohmic contact. For example, most Schottky contacts deteriorate at high annealing temperatures. Under such circumstances, the low-temperature annealing reported by



(a)



(b)

FIG. 3.1 (a) FIVE-DOT ARRAY FOR MEASURING CONTACT RESISTANCE. (b) CURVE-TRACER I-V CHARACTERISTIC OF A DOT IN THE ARRAY.

Werthen and Scifres[21] can be used, compromising the specific contact resistance.

3.4 Schottky Contacts on n-GaAs

During the initial phase of this work, GaAs Schottky IMPATT and GaAs-GaAlAs heterojunction MITATT diodes were fabricated and tested. Since an electron-beam evaporator was not available at that time, Ti was deposited by sputtering. Schottky contacts should have the following desired characteristics:

1. Large barrier height.
2. Ideality factor close to one.
3. Thermal stability.
4. No reaction with the semiconductor.
5. Good surface adhesion.

Barrier height is determined by the metal used for the contact, doping level of the semiconductor, energy bandgap of the semiconductor, and surface preparation before the Schottky metallization. Thermal stability and the interaction of Schottky-barrier metallizations on GaAs were studied by Mukherjee et al.[22] Their results are presented next.

Platinum, among other materials, has the largest barrier height. The Pt and GaAs reaction starts to occur at 300°C, resulting in $PtAs_2$ and PtGa compound formation close to the interface. During this process some GaAs is consumed which is also called the "chew-in effect." This is detrimental to devices with thin active layers. After the compound formation on the metal-semiconductor interface,

$PtAs_2$ is responsible for the subsequent Schottky-barrier characteristics of this metallization.

Tantalum, molybdenum, and tungsten were also studied for Schottky contacts to GaAs. Although they are very stable up to 550°C, flaking and gold indiffusion limit their use as reliable Schottky-barrier metallizations.

Titanium, which is used in the fabrication throughout this work, was found to be stable against interdiffusion as well as oxidation up to 400°C. Both titanium arsenides and gallium-based compounds, such as TiAs, Ti_5As_3, Ti_2Ga_3 and Ti_5Ga_4, have been identified in annealed samples. Annealing conditions were found to affect the electrical stability of the Schottky diode. The presence of oxygen in the annealing furnace greatly degrades the electrical characteristics of the diode. Vacuum annealing is recommended to avoid such problems. In many applications Ti/Pt/Au metallization was found to be the most stable contact where platinum acts as a diffusion barrier against gold. Gold in GaAs acts as a recombination-generation center, causes short lifetimes, and leads to severe barrier-height degradation.[23] Sinha et al.[24] reported that annealing (or aging) in air leads to instabilities in the diodes and abnormally large leakage currents for Ti-GaAs Schottky-barrier diodes. This behavior was also observed in samples annealed under forming gas flow (95 percent N_2 and 5 percent H_2) in this laboratory. Although forming gas was flowing in the annealing furnace, there is a possibility that some amount of air or oxygen is present in the furnace. Another possibility is that the forming gas reacts with Ti at elevated temperatures. The end result

is that Ti-GaAs contacts should be annealed in a vacuum rather than in forming gas.

3.4.1 Surface Preparation for Metal-GaAs Contacts. Surface pretreatment before the deposition of contact metal on GaAs determines the quality of the metal-GaAs contacts. The interface between the GaAs and metal contact should be free of any impurities and contamination. Most chemical etchants leave behind some impurities even after DI rinsing and N_2 drying. If processing steps permit, the best way to obtain a clean interface is to etch the GaAs surface, DI rinse it, and blow it dry with nitrogen. Ammonium-hydroxide (NH_4OH) based etchants are reported to result in good interface properties compared to other chemical etchants. In some applications, such as very thin active layers, chemical etching of the GaAs surface would be prohibited. Miers[25] studied various surface pretreatments before the Schottky contact metallization. Both HCl, H_2SO_4-H_2O_2 and NH_4OH dip followed by DI rinse and N_2 drying were used and their effects on the ideality factor and barrier height were compared. NH_4OH rinse (1 NH_4OH:10 H_2O, dilute) was reported to be superior to other treatments. Throughout this work the following surface-pretreatment was followed:

1. Plasma descum in 0.4 Torr Ar and 0.1 Torr O_2 with 50 W RF power for 30 s.
2. (1 NH_4OH:10 H_2O) dip for 30 s.
3. DI rinse for 30 s.
4. N_2 dry.

This pretreatment of GaAs wafers was used before the deposition of ohmic and Schottky contact metallizations.

3.4.2 Schottky-Barrier Characterization of Ti-GaAs Contacts.

First, the ideality factor n and the barrier height ϕ_B were evaluated on a test sample. Most published results concerning the characteristics of the Schottky Ti-(n-GaAs) junctions were for evaporated Ti contacts and there was no available data on the characteristics of Ti contacts deposited by sputtering. Second, due to the fabrication process adopted in this work, the Schottky metal was deposited first and the ohmic contact metallization was deposited later in the process. Since the ohmic contacts must be annealed at 475°C for approximately 2 min, the Schottky metal should be stable during this annealing cycle. The CW operation at high power outputs and small diode areas for high-frequency operation results in considerable local heat dissipation at the metal-semiconductor interface which results in intermixing and eventual device failure. Therefore, it was essential to study the effect of thermal annealing on the electrical characteristics of the Ti/n-GaAs Schottky diodes used in this process.

The test sample used for the characterization of the Ti/n-GaAs Schottky contacts consisted of an epitaxial layer of $N_d = 4.2 \times 10^{16}$ cm^{-3} doping concentration and 0.8 μm epitaxial thickness over n^+ substrate. The entire n^+ back side of the wafer was metallized with evaporated Au-Ge/Ni/Au and the ohmic contact was annealed at 475°C for 100 s under forming gas flow (95 percent nitrogen and 5 percent hydrogen). Ti was sputtered on GaAs followed by Au evaporation using a lift-off process and 0.006-inch diameter Ti/n-GaAs Schottky contacts were achieved. The sample underwent various annealing cycles and the forward I-V characteristics were measured using a digital voltmeter and ammeter after each annealing cycle.

Figure 3.2 shows the forward I-V characteristics for each annealing cycle along with the measured ideality factors and the barrier heights. The data were analyzed in the framework of the Schottky thermionic emission model. The ideality factor n and the Schottky-barrier height ϕ_{B_n} (V) are

$$\phi_{B_n} = \frac{kT}{q} \ln \left(\frac{A^{**}T^2S}{I_s} \right) \tag{3.1}$$

and

$$n = \frac{q}{kT} \frac{\partial V_F}{\partial (\ln I_F)} , \tag{3.2}$$

where I_s is the intercept of the log I_F vs. V_F plot, A** is the effective Richardson constant and is assumed to be equal to 8.4 $A/cm^2{}^oK^{-2}$ for GaAs, S is the Schottky contact area, T is the temperature, k is the Boltzmann constant, and q is the electronic charge.

The ideality factor n and the Schottky-barrier height were calculated for the linear regions of the log I_F vs. V_F plot. From Fig. 3.2 it is observed that the n factor and the barrier height improved during annealing compared to the as prepared characteristics. It is also clear that there is not much change in the ideality factor but the barrier height improved appreciably after annealing.

Sinha et al.[24] measured the ideality factor, the barrier height, and the I-V characteristics of the evaporated Ti/n-GaAs Schottky diodes. Their results show that the ideality factor did not change and the barrier height increased only 0.02 V after annealing at 350°C. From Fig. 3.2 it is observed that the barrier height increased 0.176 V after annealing at 300°C while a slight improvement was obtained

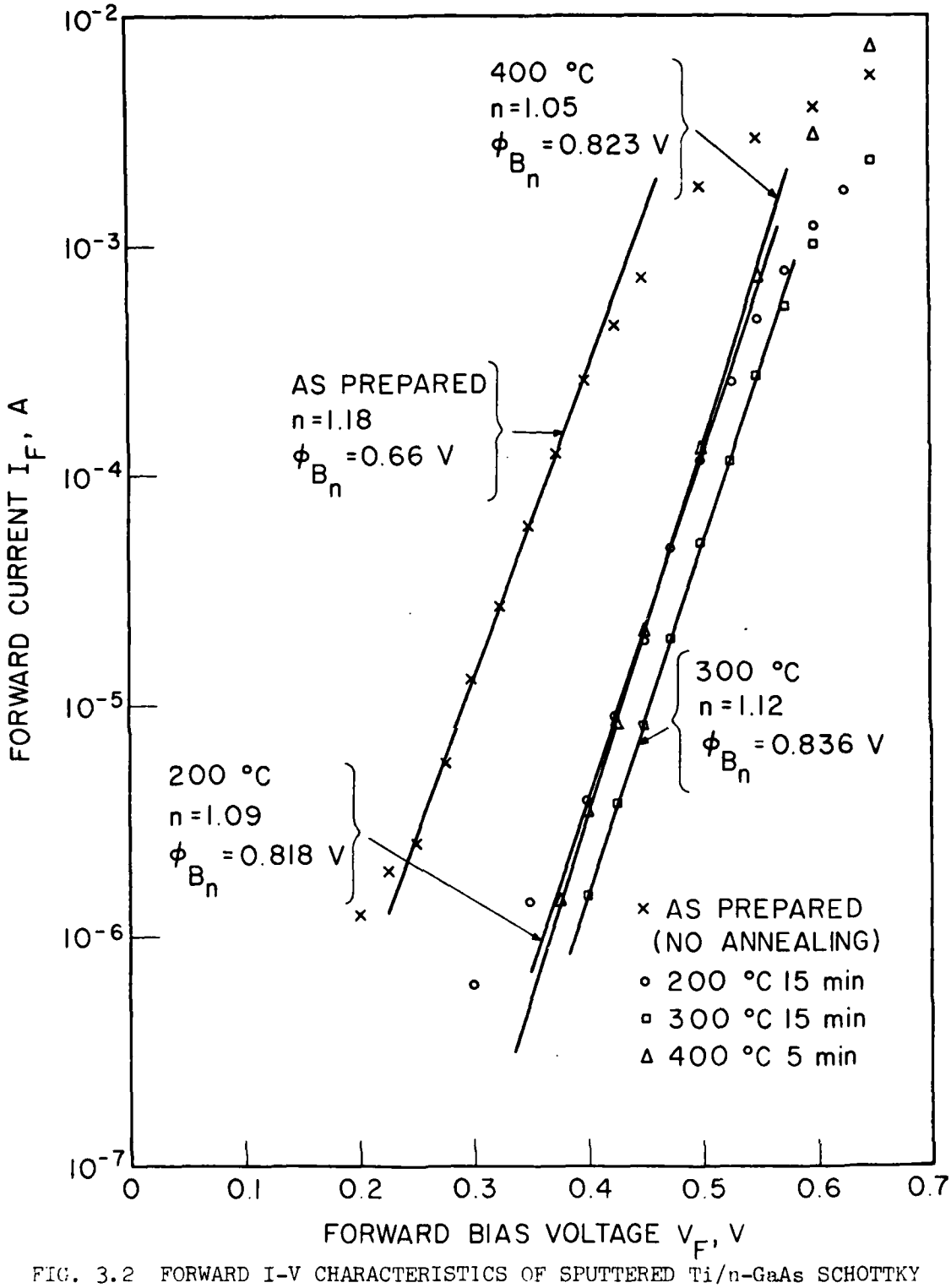


FIG. 3.2 FORWARD I-V CHARACTERISTICS OF SPUTTERED Ti/n-GaAs SCHOTTKY TEST DIODES (0.006-INCH DIAMETER) AND THEIR VARIATION WITH ANNEALING.

in the ideality factor. The low barrier height observed with Ti/n-GaAs Schottky contacts deposited by sputtering is believed to be due to surface damage on the GaAs during the sputtering process. This initial surface damage anneals at high temperatures resulting in an improvement of the barrier height. When the results obtained by Sinha et al.[24] are compared with this work, it is seen that the barrier heights of evaporated Ti/n-GaAs and sputtered Ti/n-GaAs are very close after annealing the samples at 300°C (ϕ_{B_n} = 0.84 V for evaporated Ti and ϕ_{B_n} = 0.836 V for sputtered Ti Schottky diodes).

Figures 3.3 and 3.4 show the forward I-V characteristics for each annealing cycle along with the measured ideality factors and the barrier heights for both evaporated and ion beam deposited Cr Schottky-barrier diodes, respectively. As seen in Fig. 3.4 the barrier height is very low for ion-beam deposited Cr Schottky contacts before any annealing process. This is believed to be due to the surface damage on the GaAs caused by argon ions, despite the fact that the lowest acceleration voltage was used to reduce the damage. Although the barrier height was improved after 400°C annealing, the diode characteristics are not good. Evaporated Cr Schottky diodes had the near perfect ideality factor n = 1.03 and were stable up to 400°C. Figure 3.5 shows the forward I-V and reverse I-V characteristics of evaporated Cr/n-GaAs diodes after 200°C annealing for 15 min.

3.5 Etching of GaAs for Device Fabrication

Fabrication of IMPATT diodes and other GaAs devices requires at least one etching process. In general, isolation and separation of individual devices are accomplished by wet chemical etching of the

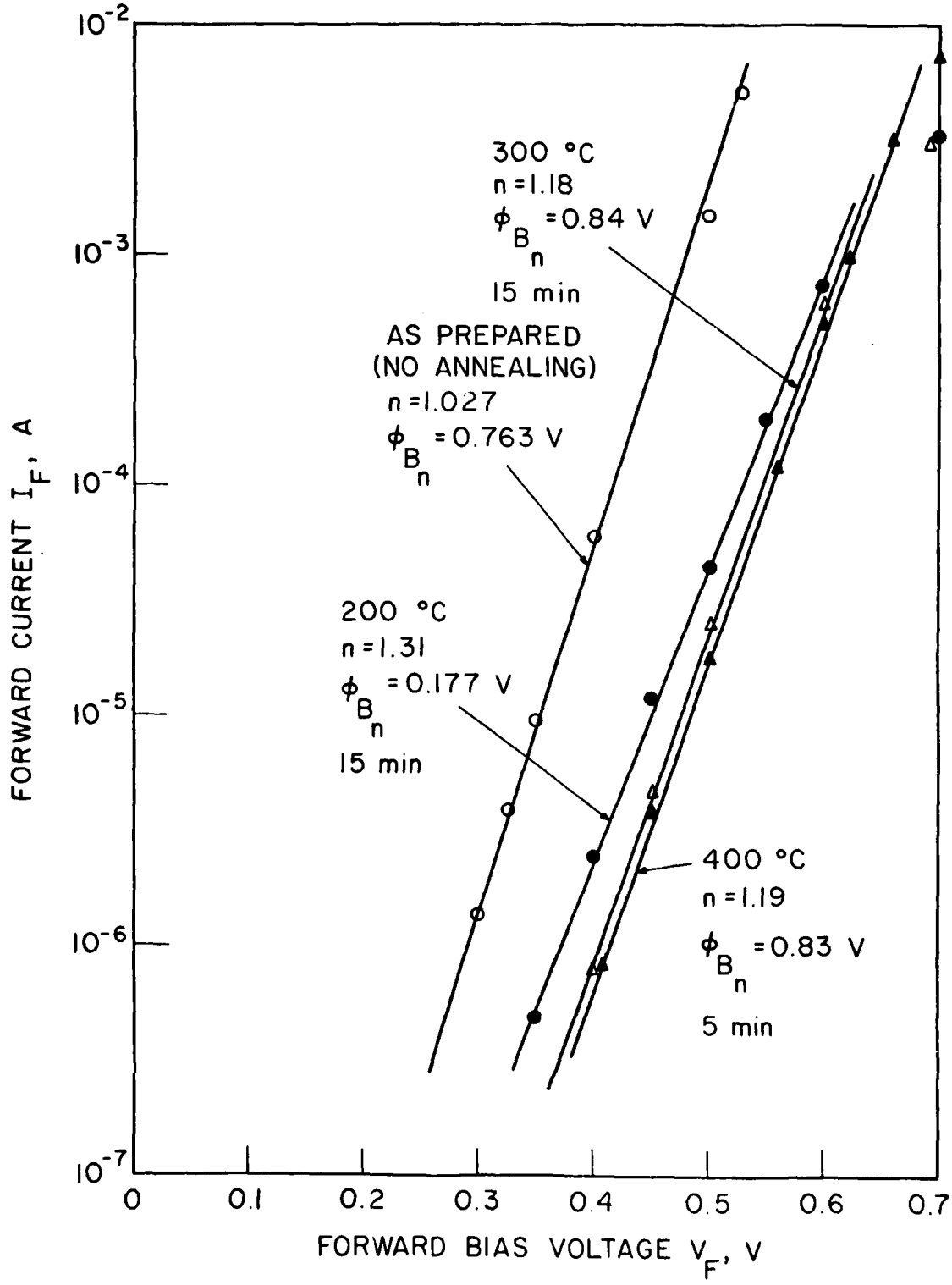


FIG. 3.3 FORWARD I-V CHARACTERISTICS OF EVAPORATED Cr/Cr/n-GaAs SCHOTTKY TEST DIODES (0.006-INCH DIAMETER) AND THEIR VARIATION WITH ANNEALING.

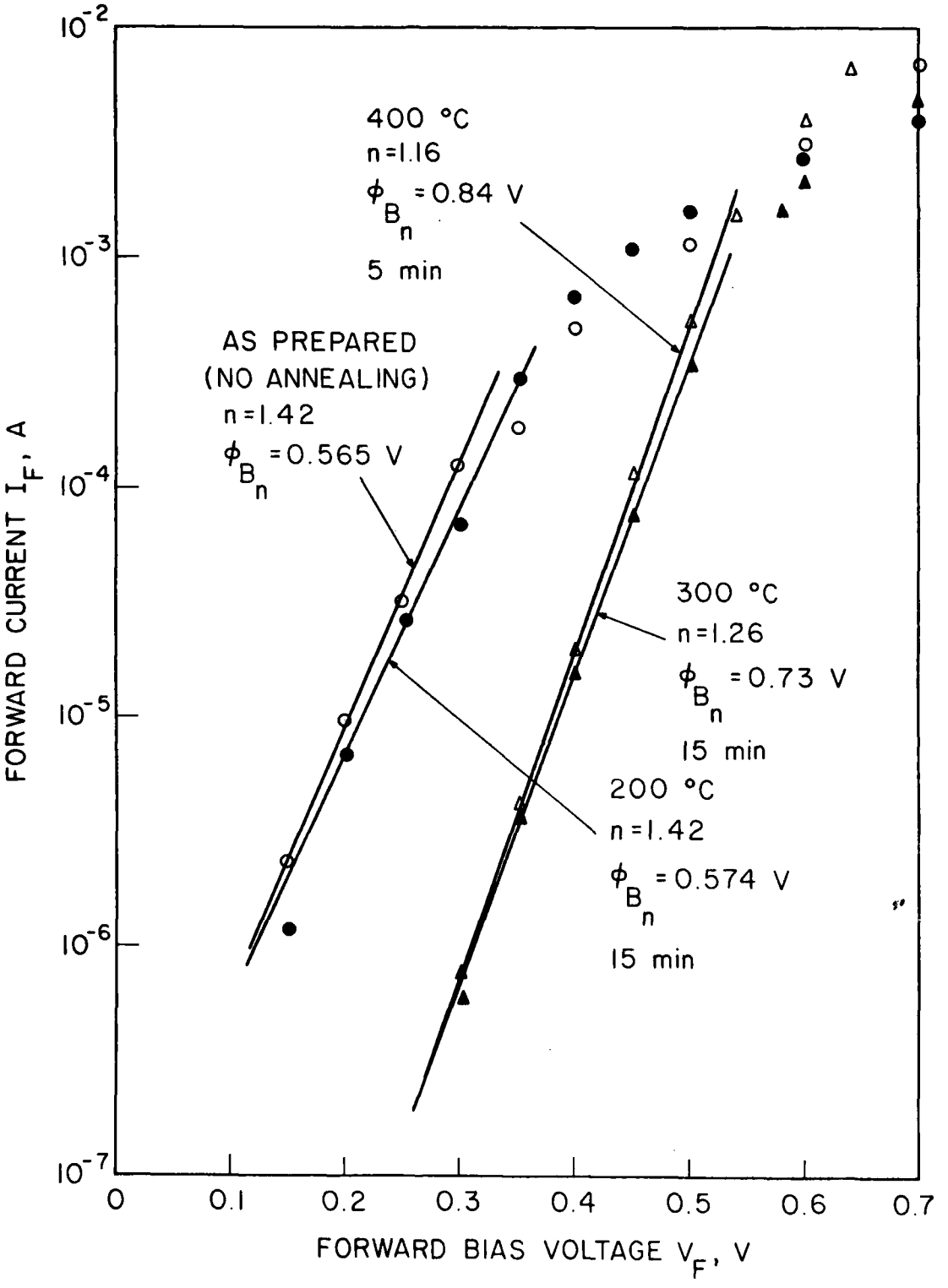
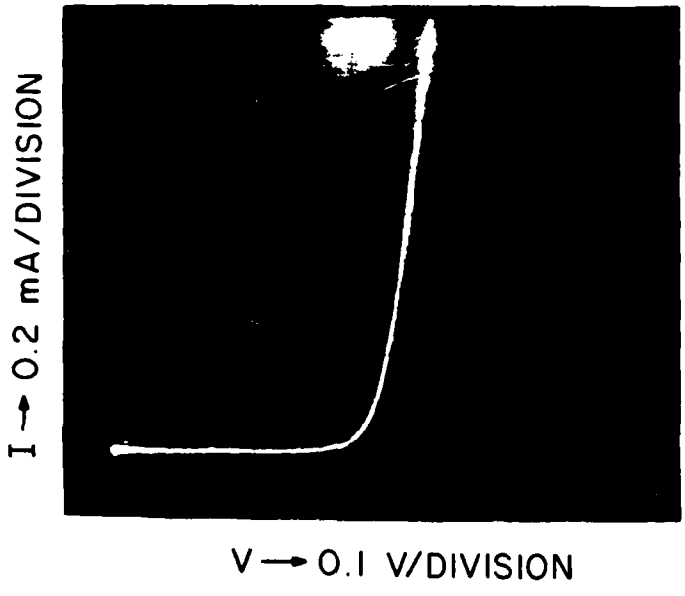
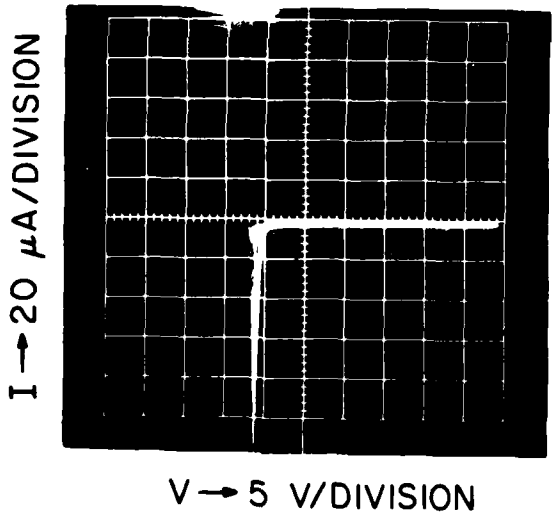


FIG. 3.4 FORWARD BIAS I-V CHARACTERISTICS OF ION BEAM DEPOSITED Cr/n-GaAs SCHOTTKY TEST DIODES (0.006-INCH DIAMETER) AND THEIR VARIATION WITH ANNEALING.



(a)



(b)

FIG. 3.7 (a) FORWARD I-V AND (b) REVERSE I-V CHARACTERISTICS OF SCHOTTKY DIODES (0.006-INCH DIAMETER) AFTER ANNEALING AT 200°C FOR 15 MIN.

GaAs material. Recently, new techniques are emerging and replacing the conventional etch processes developed for GaAs. In the following sections a general description of the chemical etchants used in this work is presented. Various dry etching processes (i.e., RIE) and their potential applications for the millimeter-wave two-terminal devices is discussed briefly. Finally, anodic etching of GaAs for precise control of the etching process is covered.

3.5.1 Wafer Thinning of GaAs. Due to the skin effect and parasitic resistance limitations, the required GaAs layer thickness for millimeter-wave IMPATT diodes is typically of the order of 2 to 7 μm. Therefore, the GaAs wafer must be thinned from 0.015 inch to approximately 2 to 7 μm. Most common methods for thinning GaAs wafers reported in the literature use mechanical abrasion. In this method, wafers are mounted on a stainless steel lapping fixture and lapped with a compound (commercial microgrit). This lapping and mounting process is repeated and wafer thickness uniformity is checked each time. To obtain better uniformity, as much as five to ten lapping and dismounting steps are needed. The major disadvantages of this method are:

1. The lapping and dismounting of the wafer is tedious, requiring longer processing time.

2. During lapping and dismounting, the GaAs wafer develops cracks and surface microcracks that are detrimental for the following processing steps and result in poor electrical characteristics (i.e., diode burnout at low bias currents).

3. Due to these limitations mentioned, wafer thinning by lapping is limited to diodes where GaAs layer thickness is greater than 7 to 10 μm.

The process developed during this work, which is explained in the following section, eliminates most of the problems mentioned. Since most MBE grown GaAs wafers are mounted with indium during epitaxial growth, their back side is covered by indium. After removal of the indium in HCl, it was observed that indium that reacts with GaAs remains on some portions of the surface. Complete removal of the indium and uniform surface was not possible by chemical removal. Therefore, brief lapping of the surface using a 10-μm grit compound was performed. The damage caused during lapping was removed by polishing the surface on a polishing wheel using 5 percent chlorine bleach and 95 percent DI water. After chemical-mechanical polishing, the GaAs surface is shiny and mirror smooth. The wafer was dismounted and rinsed in tricho-acetone-methanol.

3.5.2 Bubble Etching of GaAs Wafers. It is clear from the discussion in the previous section that etching of the GaAs wafer with uniformity and good surface quality is very important for the millimeter-wave GaAs device fabrication. The process described in this section was used successfully in device fabrication.

Most chemical wafer thinning of GaAs reported in the literature was intended for sample preparation for TE microscopy. Jet polishing and jet thinning reported by Unvala et al.[26] and Bicknell[27] result in a thick rim area around the periphery of the specimen that is useful for handling the thinned specimen. Jet etching certainly is not suitable for wafer thinning for device fabrication since it leaves a thick rim area around the periphery and only a small area can be

thinned uniformly (2 to 3 mm^2 typically). Bubble etching was used successfully by Stoller et al.[28] for thinning silicon wafers.

The apparatus used for the bubble etching of GaAs is shown in Fig. 3.6. A cross-sectional drawing of this apparatus is given in Fig. 3.7. In this process, CO_2 gas is bubbled up through the etching solution providing random agitation of the solution. The wafer to be thinned is mounted on a Teflon cup using paraffin wax. The Teflon cup moves randomly during etching, floating in the solution and the rising bubbles impinge upon the wafer surface.

First, a mixture of HF and H_4NO_3 (2:98 volume ratio) was used for wafer thinning of GaAs. Results were not satisfactory although it resulted in a reasonable etch rate for thinning the wafer and good thickness uniformity. The etch rate for this solution is 20 μm/min at room temperature. The resulting surface after etching has a coarse grainy structure which at first sight might be attributed to a high concentration of small precipitation particles. This behavior was also observed by Biedermann and Brack.[29] The precipitation of foreign material on the GaAs surface etched in a nitric acid-based etchant was also reported by Packard.[30] These precipitates were identified as As_2O_3.

Since a H_2SO_4:H_2O_2 solution was used successfully to etch GaAs in the past, the solution H_2SO_4:H_2O_2:H_2O (1:8:1 volume ratio) was tried in the bubble etching of GaAs. Unlike the HF:H_4NO_3 solution, this etchant provided a fast etch rate (25 μm/min), uniform wafer thinning, and excellent surface quality. The etch rate and surface quality do not depend on the doping concentration and particular dopant for this etching solution. Both n^+ and semi-insulating wafers

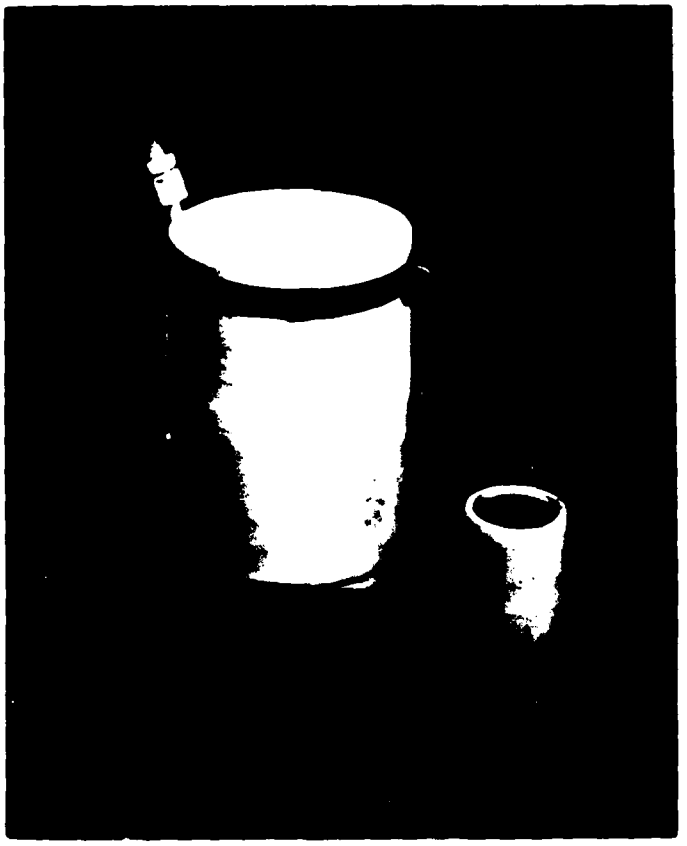
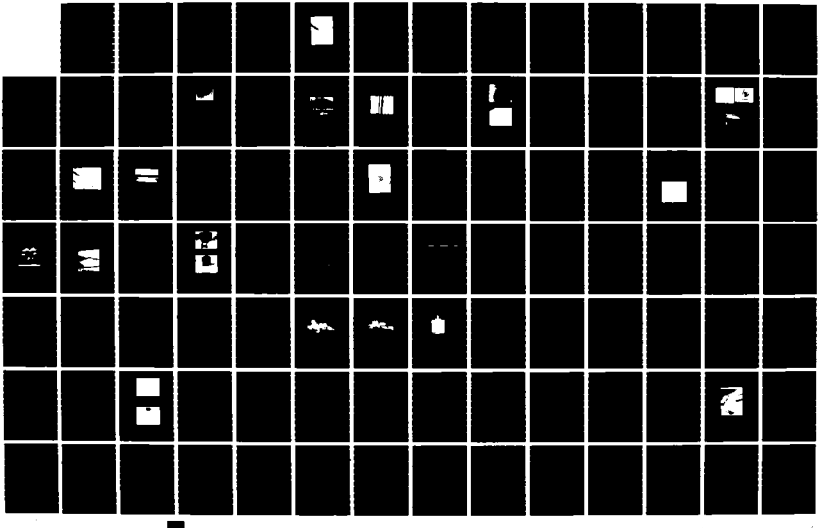
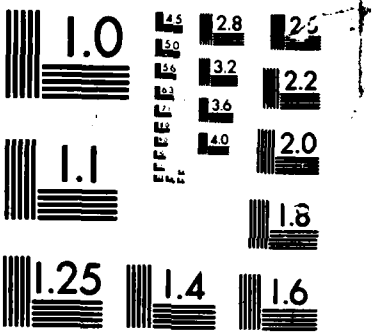


FIG. 3.6 THE APPARATUS USED FOR THE BUBBLE ETCHING OF GaAs. THE TEFLON BOAT ON WHICH THE WAFER IS MOUNTED IS SHOWN ON THE RIGHT SIDE.

AD-A168 985 MILLIMETER-WAVE HETEROJUNCTION TWO-TERMINAL DEVICES(U) 2/3
MICHIGAN UNIV ANN ARBOR SOLID-STATE ELECTRONICS LAB
N S DOGAN ET AL. MAY 86 020046-F N00014-82-K-2040
UNCLASSIFIED F/G 9/1 NL

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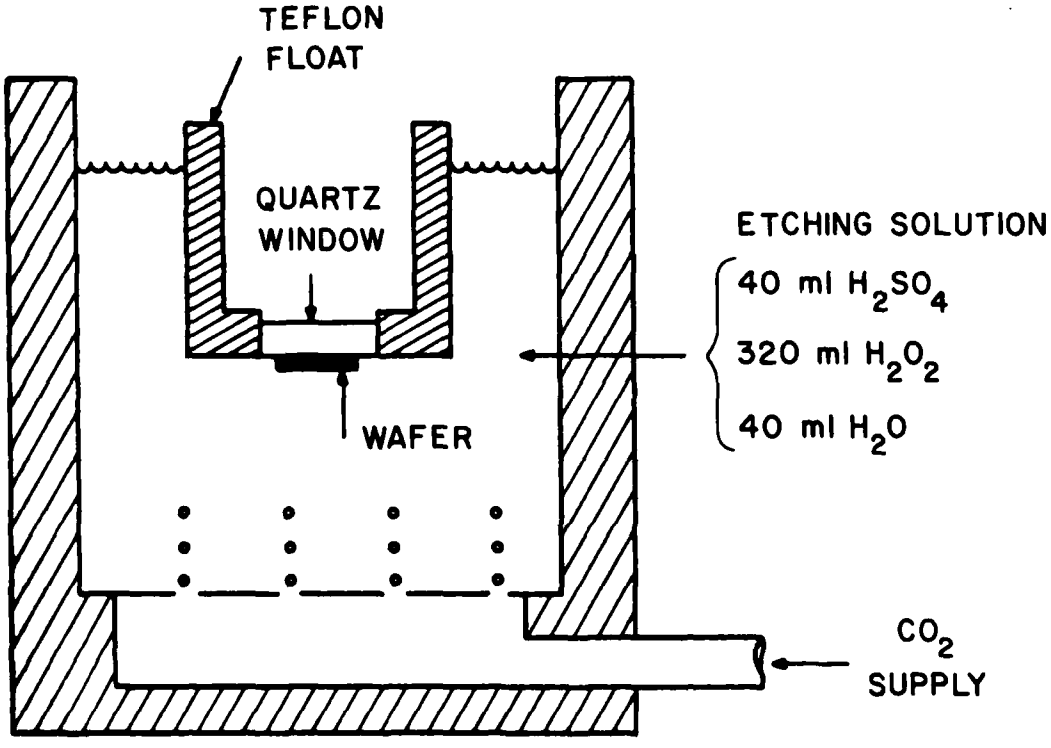


FIG. 3.7 CROSS-SECTIONAL DRAWING OF THE APPARATUS USED FOR GaAs ETCHING.

were etched and no difference in the etching characteristics were observed.

3.5.3 Mesa Etching of GaAs for Device Fabrication. The separation or isolation of individual devices require mesa etching. Most common etching solutions used for IMPATT diodes for mesa etching have been the $H_2SO_4:H_2O_2:H_2O$ etchant with various volume ratios. In this work a volume ratio of 5:1:1 was used as a slow etchant during wafer thinning and for final mesa etching. To obtain good electrical characteristics for the diode, the diode cross section should have a positive slope in all the other crystal plane directions. Table 3.1 shows the characteristics of the most common acid-hydrogen peroxide etchants[31] for GaAs. In an earlier portion of this work, $NH_4OH:H_2O_2:H_2O$ (3:1:15 volume ratio) etchant was used for mesa etching. As seen in Fig. 3.8 the mesa has a negative slope on certain crystal directions. The photoresist mask was a perfect circle and the resulting GaAs mesa after etching had a distorted shape. This etchant is certainly not acceptable for diode mesa etching.

3.5.4 Anodic Etching of GaAs. Since it is essential to control the doping profile of IMPATT and MITATT diodes very precisely to obtain proper breakdown characteristics, an anodic etching technique was employed. For any doping profile where the breakdown voltage increases as the anodization proceeds, the process can be made self-limiting by setting the anodization voltage at the desired breakdown voltage.

In this process GaAs is oxidized anodically and the oxide thickness grown on the GaAs surface is determined by the difference voltage between the applied voltage and the breakdown voltage of the GaAs epitaxial layer. The oxide grown anodically is stripped in

Table 3.1

Characteristics of Acid-Hydrogen Peroxide Etchants for GaAs (Shaw[31])

ACID	VOLUME RATIOS *	CONCENTRATION (mol l)		RATIO OF UNDERCUT TO ETCHED DEPTH			RELATIVE ANISOTROPY	ETCH RATE (100) ($\mu m\ min^{-1}$)	CROSS SECTIONAL PROFILES	
		ACID	H_2O_2	$<01\bar{1}>$	$<011>$	$<100>$			(011) SECTION	$(01\bar{1})$ SECTION
H_2SO_4	1 8 1	1 8	8 0	0 30	0 30	0 90	1 0	14 6		
H_2SO_4	1 8 40	0 36	1 6	0 89	0 68	1 2	0 55	1 2		
H_2SO_4	1 8 80	0 20	0 90	0 62	0 62	0 86	0 32	0 54		
H_2SO_4	1 8 160	0 10	0 47	0 71	0 71	0 93	0 27	0 26		
H_2SO_4	1 8 1000	0 018	0 079	0 82	0 76	0 95	0 22	0 038		
H_2SO_4	1 1 8	1 8	1 0	0 77	0 53	1 0	0 61	1 3		
H_2SO_4	4 1 5	7 1	1 0	0 49	0 29	0 70	0 83	5 0		
H_2SO_4	8 1 1	14 0	1 0	0 52	0 43	0 61	0 35	1 2		
H_2SO_4	3 1 1	11 0	2 0	0 44	0 44	0 53	0 19	5 9		
HCl	1 4 40	0 27	0 87	0 51	0 28	0 97	1 1	0 22		
HCl	1 1 9	1 1	0 89	0 22	0 18	0 37	0 69	0 20		
HCl	40 4 1	10 6	0 87	0 54	0 54	0 54	~0	>5 0		
HCl	80 4 1	11 2	0 46	0 7	0 7	0 7	~0	1 1		

* ACID (CONCENTRATED) H_2O_2(30%) H_2O

FIG. 4.- SCANNING ELECTRON MICROSCOPE PHOTOGRAPH OF THE GaAs MESA STRUCTURE ETCHED IN $NH_4OH:H_2O_2:H_2O$ (3:1:10). MAGNIFICATION IS 3000 WITH 45-DEGREE ANGLE VIEWING.

dilute HCl or dilute NH_4OH. The amount of GaAs etched during oxidation is 60 percent of the oxide layer thickness. If the breakdown and applied voltages are known, the amount of GaAs etched from the surface for each oxidation growth and removal can be calculated. If the applied voltage is set equal to the desired breakdown voltage the oxidation process stops automatically. Niehaus and Schwartz[32] published an excellent article on the physical process and experimental results of anodic etching of GaAs. Figure 9a shows the anodic etching apparatus used in this work. Figures 9b and c show the x-y plotter output during etching and typical breakdown voltage variation during anodic GaAs etching, respectively. The solution is a mixture of 100 ml H_2O:3 ml NH_4OH:3 gr tartaric acid and 250 ml propylene glycol. The current density used in this work is 1 mA/cm^2 and the growth rate of oxide is approximately 14.5 Å/V.

Much of the current at lower reverse bias voltages for MITATT diodes is due to tunneling. There is not a well-defined breakdown voltage as in IMPATT diodes. Appreciable reverse bias current flows for low values of reverse bias voltage and the breakdown characteristic is "soft." The anodization current was held constant and the breakdown voltage of the GaAs sample was observed with an x-y recorder during etching. Experimentally, it was observed that the breakdown voltage changes very rapidly as the n^+ layer is thinned by anodic etching. The breakdown voltage of the MITATT diode is very sensitive to the thickness of the n^+ layer. It is essential to stop the etching as soon as the initial breakdown voltage starts changing.

3.5.5 Dry Etching of GaAs. Reactive ion etching (RIE) has been used extensively as a pattern transfer process of high fidelity

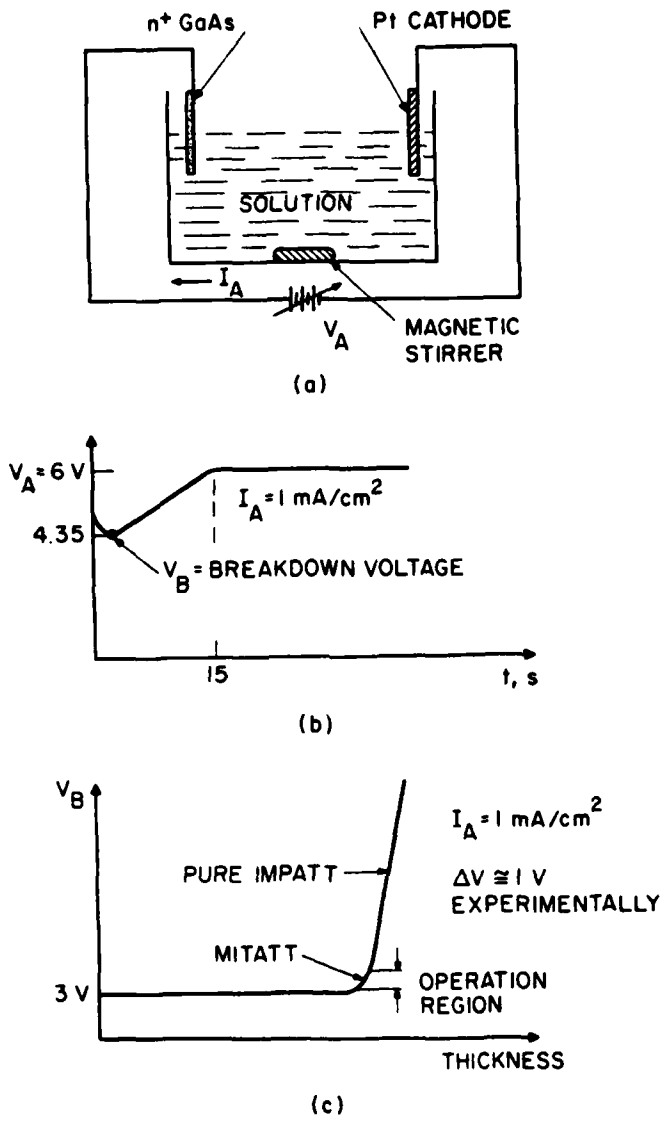


FIG. 3.9 ANODIC ETCHING OF GaAs. (a) ANODIC ETCHING APPARATUS, (b) x-y PLOTTER OUTPUT DURING ETCHING, AND (c) TYPICAL BREAKDOWN VOLTAGE VARIATION DURING ANODIC GaAs ETCHING INDICATING THE VARIOUS REGIONS.

and high resolution for the fabrication of silicon devices and structures. Recently, there has been strong interest in the application of RIE to III-V compound semiconductors for device processing. Several processes have already been demonstrated, including via holes for GaAs FETs and LED chip separation.[33] Donnelly et al.[34] investigated the temperature dependence and various physical processes of GaAs etching in a chlorine plasma. In the previous section, it was shown that most chemical etchants are isotropic and have different etching characteristics for each crystal plane. A severe undercut of the mask and enhanced chemical reactions on the metal-contact-semiconductor interface result in serious limitations for chemical etchants in certain applications. These problems can be eliminated if reactive etching is used as an alternative. Reactive ion etching is highly anisotropic and does not depend on crystal orientation. Enhanced reaction on the metal-semiconductor interface and undercutting are no longer limiting factors for device fabrication using a dry etching process. Hu and Howard[35] obtained etch rates greater than 1 μm/min and produced features having vertical sidewalls and a clean substrate surface. Very high etch rates (5 to 10 μm)/min with high aspect ratios (3$\frac{5}{}$ > 1) were obtained by Lincoln et al.[36] using ion beam assisted etching. The similar etch rates and profiles were also obtained for another important compound semiconductor, InP, in a chlorine-based plasma. All these developments will find applications in future developments of GaAs millimeter-wave devices and circuits.

Dry etching of GaAs using ion etching (milling) was tested in this laboratory. AZ 1375 photoresist postbaked at 1 0^{o}C was used as

an etch mask. Etch rates of 217 Å/min for GaAs and 87.5 Å/min for photoresist were obtained at 1000 V and 0.5 mA/cm^2 with 18-degree tilt angle operating conditions. In this process the only mechanism is the physical (mechanical) removal of the surface by argon ions and it is very slow.

The slope of the side walls can be adjusted by using proper pressure and power levels. It was reported that RIE etching results in slight surface damage, causing surface leakage currents. This can be remedied by etching the surface slightly in slow chemical etchants since, for the energies used in RIE, surface damage is very shallow (100 Å to 1000 Å).

3.5.6 Proton Isolation of GaAs Devices. Proton isolation was used in the past[37] for GaAs active devices such as MESFETs and IMPATTs. The basic principle in this technique is to implant a proton (hydrogen) or oxygen into GaAs. The range of proton penetration in GaAs is approximately 1 μm per 100 keV energy. The range data indicate that the range-energy relationship becomes significantly nonlinear for energies greater than 800 keV. The range-energy relation is almost linear below 800 keV. The range of protons in gold, often used as a bombardment mask, is approximately half the range of GaAs, 0.5 μm/100 keV. Thus, the minimum thickness of gold needed as a mask for 200 keV proton energy is 1 μm. Photoresist on the other hand can be used as a mask. The required photoresist thickness for 200 keV is approximately 5 μm.

To form high resistivity layers on GaAs with light doping ($N_D < 10^{16}$ cm^{-3}) and thin micron layers, a single dose of approximately 10^{13} cm^{-2} protons generally suffices to compensate the entire

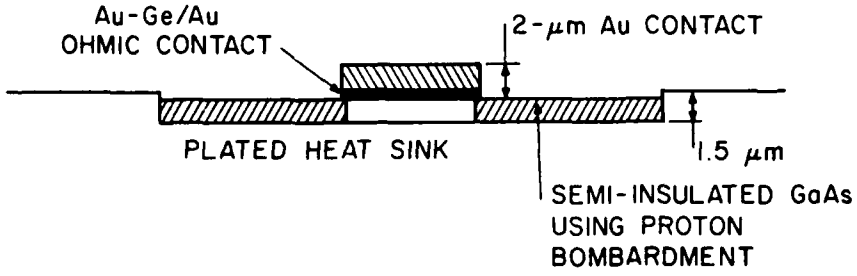
bombarded layer. Thicker layers or high concentration material often requires multiple-energy bombardment due to the nonuniformity with depth of single-energy bombardment. The process of proton bombardment creates both deep donors and deep acceptors since proton bombardment causes high resistivity in both n- and p-type GaAs.

The devices with complicated doping structures, such as double-drift hybrid or Read IMPATT diodes, require a very complex proton implantation schedule since n, p, n^+, and p^+ layers have different compensation requirements. In addition, millimeter-wave IMPATTs have very short layers due to the short transit time required for proper operation. For a given doping level, an optimum dose schedule exists that results in maximum resistivity. For example, a GaAs layer with $N_D = 1 \times 10^{16}$ cm^{-3} requires a 10^{13} cm^{-2} dose resulting in 10^8 (Ω-cm) maximum resistivity and a layer with $N_D = 1 \times 10^{18}$ cm^{-3} requires 5×10^{14} cm^{-2} with 2×10^7 (Ω-cm) maximum resistivity, without any postbombardment anneal. When the bombarded layers are annealed the resistivity changes. Samples with low-dose proton bombardments decrease in resistivity after annealing. Moderate-dose proton bombarded layers retain their initial resistivity up to 300 to 400°C annealing temperatures. Samples with high doping concentration ($N_D = 10^{18}$ cm^{-3}) and high proton dose ($10^{15} cm^{-2}$) have a different annealing behavior. Initial resistivity of bombarded layers is low and increases when annealed at 300 to 400°C. Foyt et al.[37] have measured the resistivity of low doping concentration GaAs layers proton bombarded with 10^{13} cm^{-2} dose. Donnelly and Leonberger[38] investigated the multiple-energy proton bombardment in n^+-GaAs and the annealing characteristics. The conclusion is that there

exists an optimum proton schedule (dose) for a given layer structure that must be determined experimentally.

Since the available ion implanter can go up to 200 keV, the GaAs layer thickness that can be insulated is limited to less than a thickness of 2 μm. For this reason the initial GaAs thickness must be 1.5 μm or less for most practical purposes to allow some tolerance in the device isolation. Figure 3.10 shows the proton guarded double-drift IMPATT diode and the proton implantation schedule used for the initial work.

It was observed that the initial reverse bias current before breakdown was 100 μA, which is high for IMPATT diodes. Postannealing the proton-isolated diodes at 300°C in forming gas (95 percent nitrogen and 5 percent hydrogen) for 30 min improved the leakage current by a factor of twenty (5 μA leakage current). This behavior was also reported by Donnelly and Leonberger.[38] From the annealing behavior it seems that the implant schedule used resulted in a high dose of protons resulting in a low resistivity semi-insulating layer.



(a)

IMPLANT SCHEDULE USED

2.5×10^{14} cm^{-2} at 50 keV

5.0×10^{14} cm^{-2} at 100 keV

7.5×10^{14} cm^{-2} at 150 keV

10^{15} cm^{-2} at 200 keV

(b)

FIG. 3.11 (a) PROTON ISOLATED GaAs IMPATT DIODE STRUCTURE AND (b) IMPLANT SCHEDULE USED FOR PROTON BOMBARDMENT.

CHAPTER IV. FABRICATION OF GaAs AND HETEROJUNCTION GaAs-GaAlAs MILLIMETER-WAVE DEVICES

4.1 Introduction

In the previous chapter, various processes developed for the fabrication of GaAs and GaAs-GaAlAs heterojunction millimeter-wave IMPATT and MITATT diodes were presented. In this chapter, the fabrication process developed during this work is given in detail.

Virtually all technological problems associated with fabrication of high-frequency IMPATT diodes can be attributed to the reduced dimensions of these devices. The active layer thicknesses are reduced for millimeter-wave diodes due to the short transit time at these frequencies. The diode area is also reduced to maintain reasonable impedance levels. For these reasons, the material preparation, fabrication process, and packaging of the devices become challenging technical problems. In the following sections, various fabrication processes developed to overcome the technical problems encountered during this work are presented.

4.2 Fabrication Process for Millimeter-Wave Diodes

In this section, the basic fabrication sequence used during the initial phase of this work is presented. The following steps were used in the process:

1. Mesa etching (0.006-inch diameter).
2. Border (rim) etching.
3. Schottky contact metallization (Ti-Au evaporation).

4. Gold heat sink plating.

5. Back side lapping with 10-μm grit compound.

6. Chemical-mechanical polishing.

7. Back side bubble etching (fast etch).

8. Slow back side etching.

9. Consequent wax cover and etch (slow etch).

10. Ohmic contact metallization and ohmic contact pattern definition.

11. Mesa etching (0.001- to 0.002-inch diameter).

12. Packaging.

Figure 4.1 shows the processing steps followed in this work.

4.2.1 Mesa Etching. After organic cleaning in trichloroethylene, acetone, and methanol, positive photoresist (AZ 1375) is spun onto the wafer at 4000 rpm for 30 s. After a 20-min prebake at 80°C, the photoresist is patterned using the mask shown in Fig. 4.2a. After post-baking at 120°C for 20 min, the wafer is then etched in $HCl:H_2O_2:H_2O$ (80:4:1) at 30 s intervals and the thickness of the mesa is monitored by the profile measurement for each etching interval until the desired mesa thickness is obtained. In this work, a mesa thickness of 1.5 to 4 μm is used. After etching, the photoresist is stripped in acetone leaving the circular mesa shown in Fig. 4.3a. Figure 4.3b is the profile of the mesa.

4.2.2 Border (Rim) Etching. Positive photoresist (AZ 1375) is spun and patterned using the mask shown in Fig. 4.2c. The same etchant used in the previous step (80:4:1) is used for border etching. After etching with few intervals and measuring the step with the surface

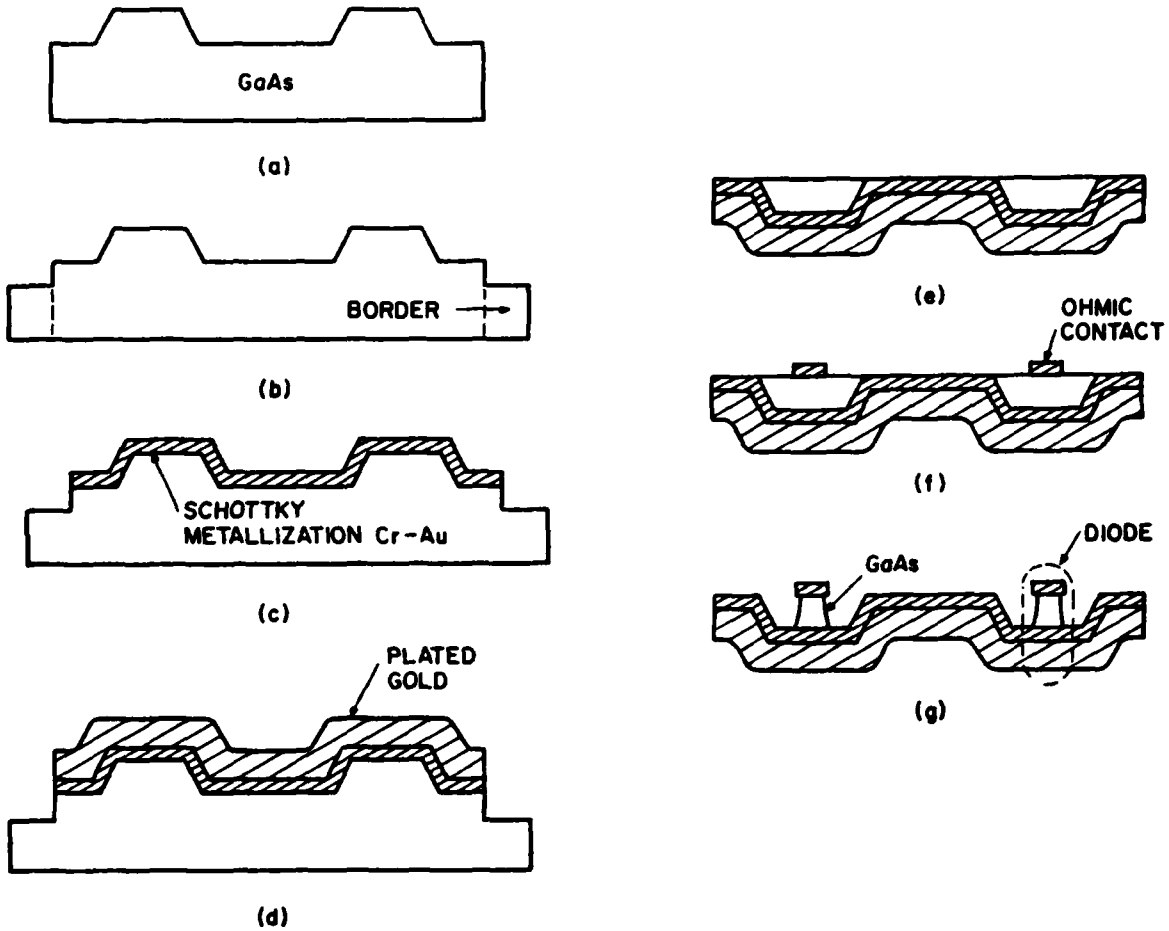


FIG. 4.1 TWO-TERMINAL HETEROJUNCTION DEVICE FABRICATION PROCESS. (a) MESA ETCH, (b) BORDER (RIM) ETCH, (c) SCHOTTKY CONTACT METALLIZATION, (d) GOLD HEAT SINK PLATING, (e) SLOW BACK SIDE ETCH UNTIL METALLIZATION IS SEEN, (f) OHMIC CONTACT, AND (g) DIODE IS COMPLETE AFTER MESA ETCH.

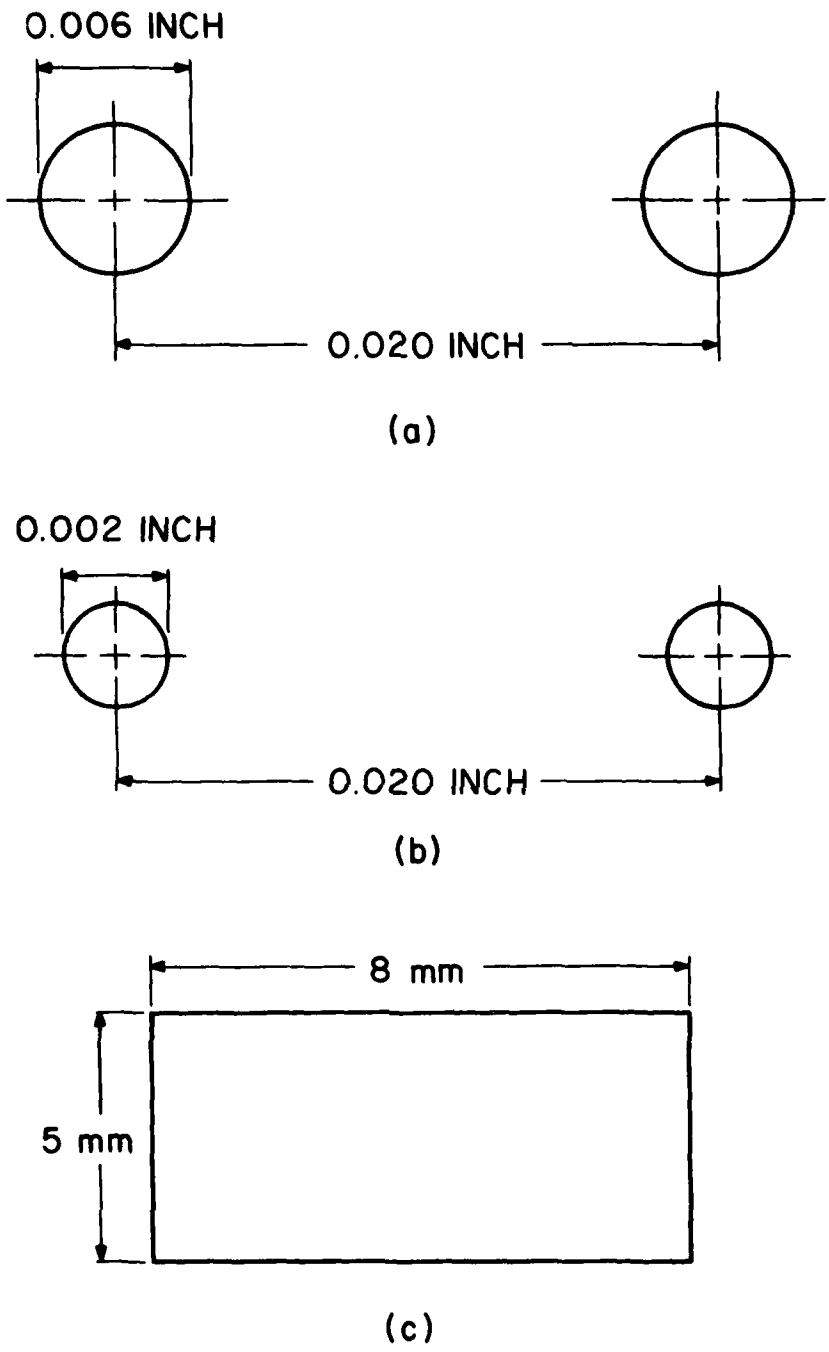
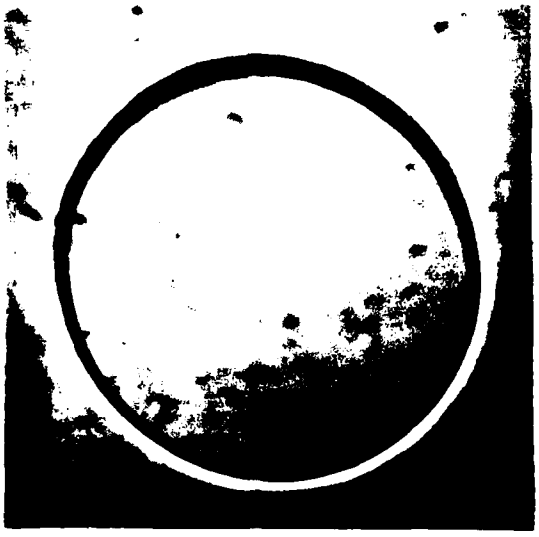
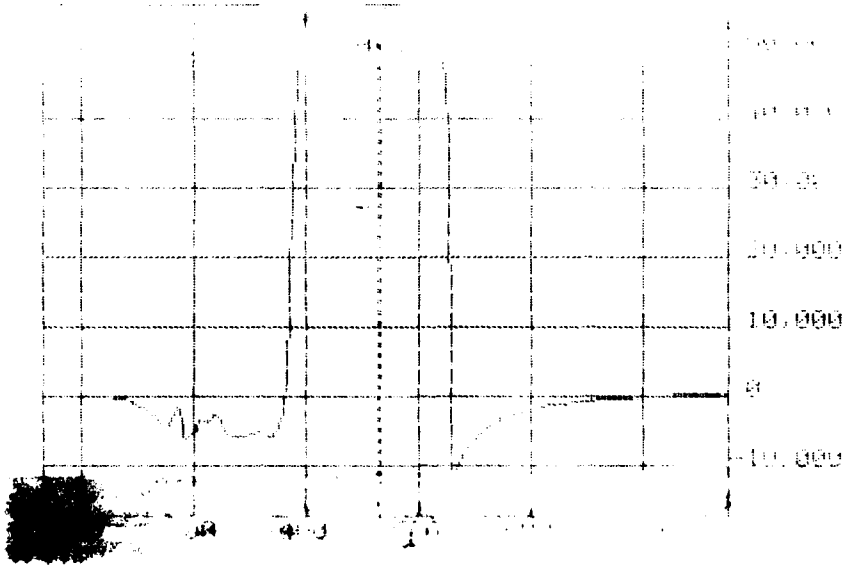


FIG. 4.2 TWO-TERMINAL DEVICE MASK SET. (a) MESA ETCH MASK, (b) OHMIC CONTACT MASK, AND (c) BORDER (RIM) ETCH MASK.



(a)



(b)

FIG. 4.3 (a) 5-μm MESA ETCH (400X MAGNIFICATION) AND (b) PROFILE OF MESA.

profiler, the border step is obtained with desired thickness (typically 3 to 5 μm). Figure 4.4 is a photograph of this step.

4.2.3 Schottky Contact Metallization. Since the electron beam evaporator was not available in the earlier portion of this work, Ti was sputtered followed by Cr and Au evaporation. Cr was used for adhesion purposes only. In the later work, Ti/Au was evaporated using the electron beam evaporator.

4.2.4 Gold Heat Sink Plating. Gold (30 μm thick) is plated over the metallized area. The back side is protected by postbaked photoresist. Figure 4.5 shows the gold-plated heat sink.

4.2.5 Back Side Lapping. Since most of the MBE grown GaAs wafers have indium on the back side after growth, the indium is removed by HCl and the front surface is protected by wax. The back side is rough due to the interaction of GaAs and indium. The wafer is mounted on a stainless steel lapping block and lapped using a 10-μm grit compound until the traces of indium are completely removed and a certain uniformity is obtained. The traces of lapping compound are then cleaned thoroughly with micro-soap and rinsed in DI water.

4.2.6 Chemical-Mechanical Polishing. After lapping with a 10-μm grit compound, the back side of the wafer is very rough. Using the same fixture (lapping block) the back side of the wafer is polished using the polishing wheel with a 5 percent chlorene bleach:95 percent DI water composition. Chemical-mechanical polishing removes any damage and results in a shiny, mirror smooth back surface.

4.2.7 Back Side Bubble Etching for Wafer Thinning. The wafer is mounted on a Teflon boat using paraffin wax. For fast etching (~1 μm/min) in a bubbler, $H_2SO_4:H_2O_2:H_2O$ (1:8:1) is used. The wafer

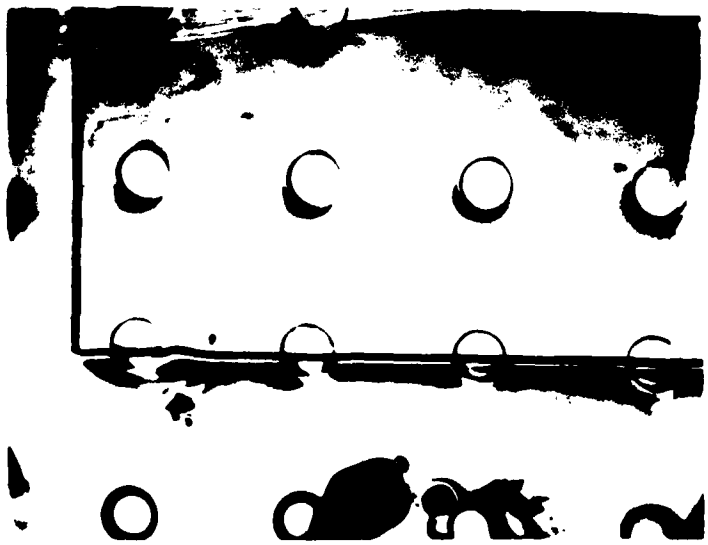


FIG. 4.4 BORDER (RIM) ETCH. BORDER ETCH IS 8 μm AND MESA IS 5 μm. (50X MAGNIFICATION)

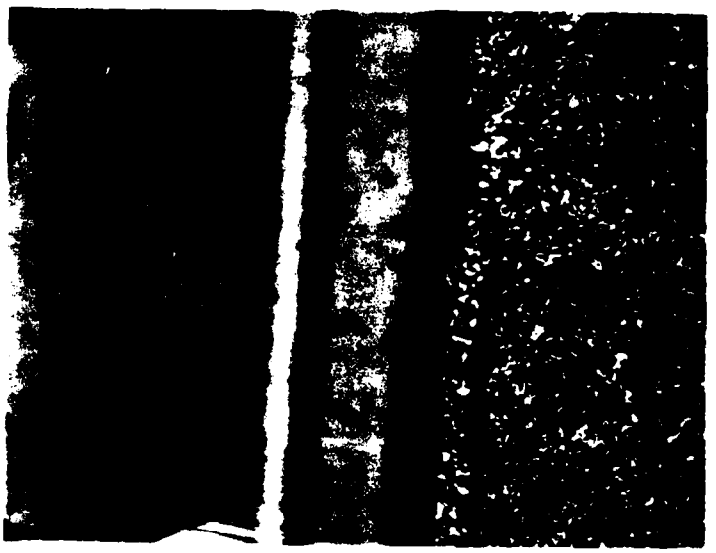


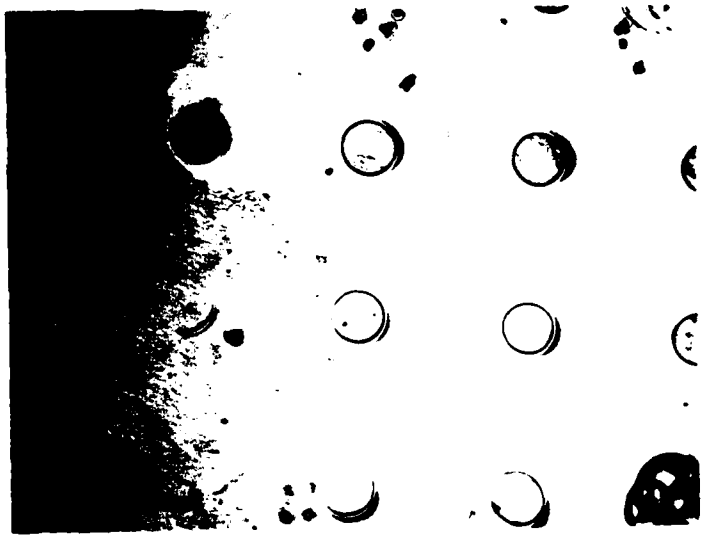
FIG. 4.5 PHOTOGRAPH OF GOLD-PLATED HEAT SINK. THE 0.006-INCH DIAMETER MESA RETAINS ITS SHAPE AFTER PLATING. THE GaAs RIM (BORDER) IS ALSO SEEN IN THE PICTURE NEXT TO THE GOLD HEAT SINK. (200X MAGNIFICATION)

is etched until the border starts disappearing indicating that the whole wafer is thinned up to the initial border mark etched in step 3. During wafer thinning, the border was carefully observed since the etch rate is very fast and the Teflon boat is rinsed in DI water immediately as soon as the border is observed to be disappearing.

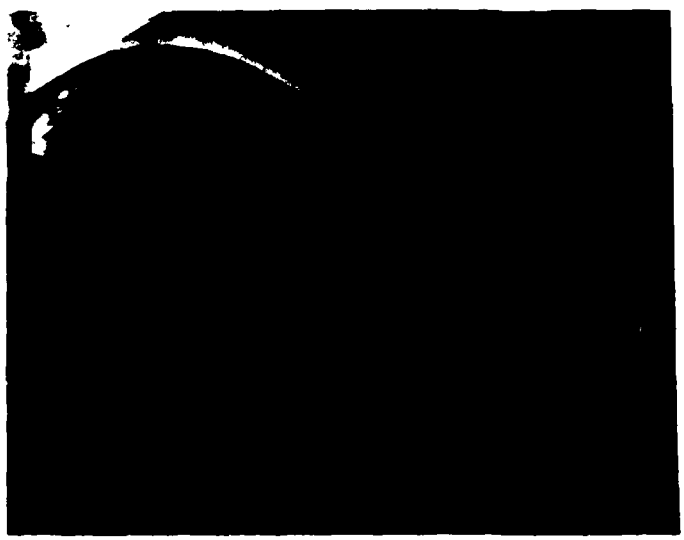
4.2.8 Slow Back Side Etching. After the border starts disappearing, etching is continued until the titanium is seen on the surface; $H_2SO_4:H_2O_2:H_2O$ (5:1:1 volume ratio) is used as a slow etchant.

4.2.9 Wax Cover and Etch. Since the wafer is not uniform in thickness before the chemical wafer thinning, one edge of the metallized surface appears first. As can be seen in Fig. 4.6, a portion of the metallization is exposed while the rest of the wafer is covered with GaAs. At this point, the exposed areas are covered with black wax and etching continues. This process is repeated until the surface is etched completely, leaving the GaAs pockets on the gold-plated heat sink.

The processing steps described so far are common to all the diodes fabricated with different techniques which are presented in the following sections. The first batch of diodes fabricated were mesa diodes. It was soon discovered that these diodes were not suitable for packaging with the available bonding tools and equipment in the laboratory. Typical diameters of the first diodes fabricated were 25 to 35 μm. The gold wire used for thermocompression bonding of the diode contact to the ceramic ring package was also 25 μm. Shorting and destruction of the diodes during thermocompression bonding were the problems encountered in the early phase of the work. Only one diode out of many was successfully bonded and tested in the



(a)



(b)

FIG. 4.7 AFTER BUBBLE ETCH FROM THE BACK SIDE (a) AND (b) SHOW THE EXPOSED SCHOTTKY METALLIZATION AND SOME GaAs LEFT ON THE SURFACE. (a) 50X MAGNIFICATION AND (b) 400X MAGNIFICATION. DARK AREAS ARE GaAs, LIGHT AREAS ARE Cr-Au METAL.

94-GHz circuit and operated at 86-GHz frequency. As reported by Bayraktaroglu and Shih,[39] the most critical step in the processing of an IMPATT diode is the device packaging. The diode fabrication process must be compatible with the available packaging technology. If the packaging capability is limited, as was the case in this work, the fabrication process must be developed accordingly. To solve this problem, beam lead (flying lead) diodes were fabricated. The beam lead diodes were very fragile to handle and the lead broke off during thermocompression bonding. Following this, "the integral packaging" technique employing polyamide as a support material was developed and had limited success. Finally, the proton isolation technique was used successfully and most of the RF measurement results reported in the following sections were obtained from these diodes.

4.3 Mesa Diodes

This is the most common type of diode used by leading research laboratories (i.e., Hughes and TRW). After wafer thinning and heat sink formation, the ohmic contact (Au-Ge/Ni/Au) metal layer is deposited (evaporated). To facilitate thermocompression bonding of the bonding ribbon to the diode contact, gold, a few microns thick, is either selectively plated or sputtered. Finally, the top contact is patterned and chemically etched to form the top ohmic contact, which also acts as a mask for final mesa etching. The sulfuric acid and hydrogen peroxide solution $H_2SO_4:H_2O_2:H_2O$ (5:1:1 volume ratio) is used for the mesa etching, which is the most commonly used etchant.

4.3.1 Mesa Diodes with Selective Gold Plating. The thin ohmic contact metallization causes shorting problems during the consequent

processing steps and bonding. To give mechanical support to the diode top contact, a selective gold plating process was developed. Figure 4.7 shows the process steps used in the contact formation. The process steps are:

1. Ohmic Contact Metallization. After rinsing the wafer in $NH_4OH:H_2O$ (1:3 volume ratio) and nitrogen drying, the entire front surface is covered by Au-Ge/Ni/Au evaporation without a mask. This step is shown in Fig. 4.7a.

2. Gold Plating over Ohmic Contacts. Circular 25- and 35-μm diameter AZ 1375 photoresist patterns are developed. Gold is then electroplated over these areas as shown in Fig. 4.7b.

3. Final Mesa Etching. After gold plating to a 6 to 8 μm thickness, the AZ 1375 photoresist is removed in acetone and unmasked gold etching is done for 30 s. This removes the unwanted field Au-Ge/Ni/Au layer over the surface. The ohmic contacts are then annealed at 475°C for 100 s under forming gas flow. Following the ohmic contact annealing, the final mesa etch is completed in $H_2SO_4:H_2O_2:H_2O$ (5:1:1 volume ratio) GaAs etchant for approximately 1 min. The final structure is shown in Fig. 4.7c. A scanning electron microscope (SEM) photograph of a 35-μm diameter Ti/n-GaAs Schottky diode is shown in Fig. 4.8. As seen in Fig. 4.8, the plated gold contact is porous and very soft. Therefore, the process was modified and the following process was used for most of the diodes reported in this work.

4.3.2 Mesa Diodes with Gold-Plated Contacts. The process steps are similar to the mesa diodes with selective gold-plated contacts presented previously. The new process steps are:

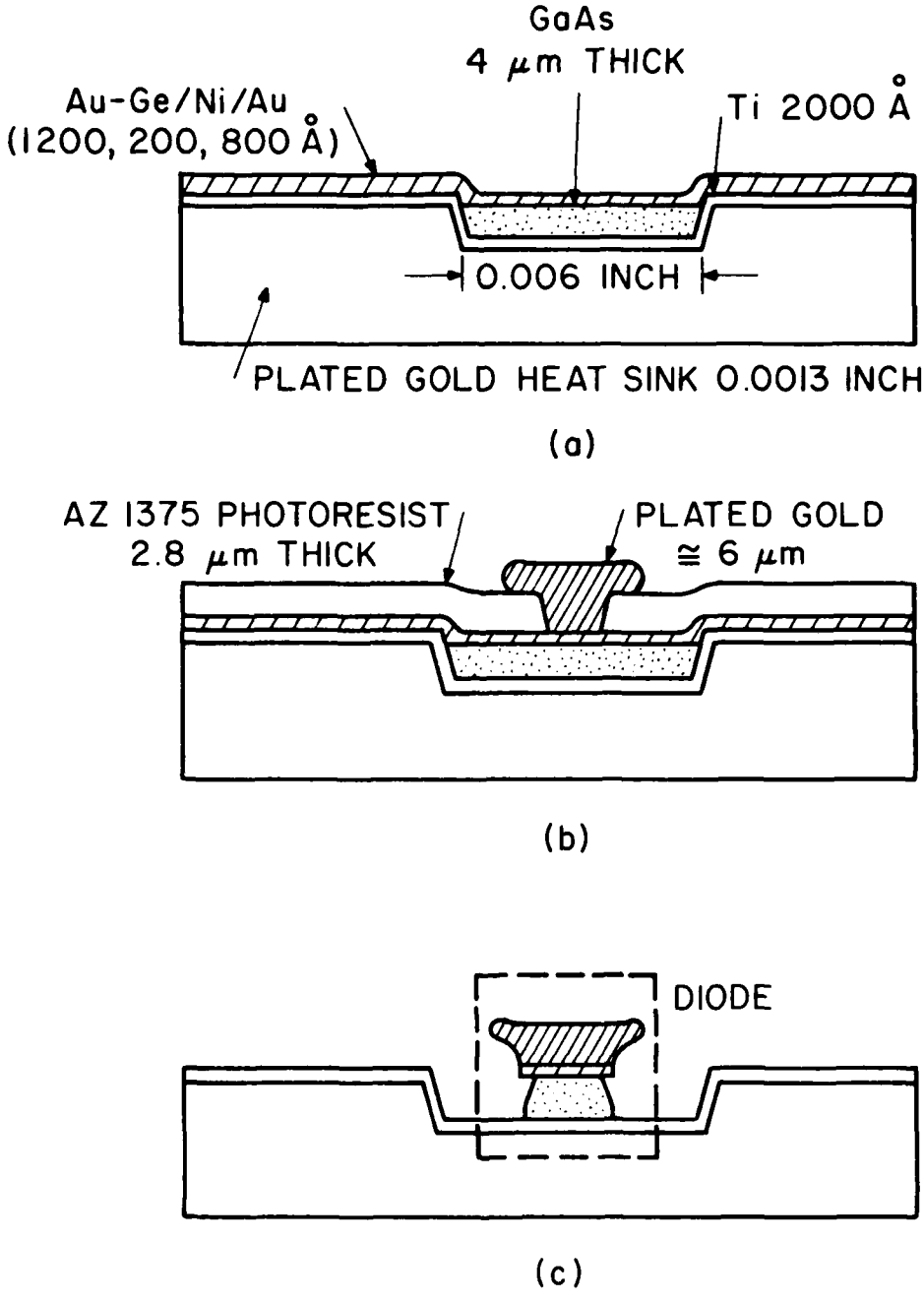
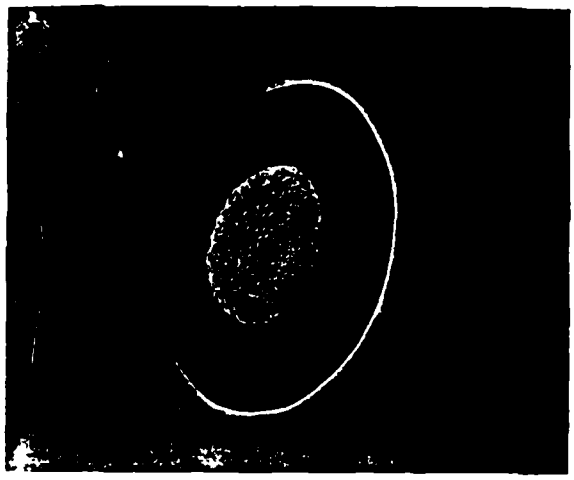
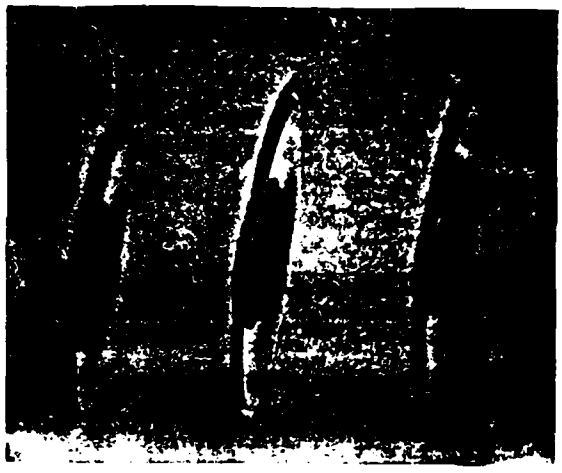


FIG. 4.7 PROCESS STEPS USED IN DEVICE FABRICATION.

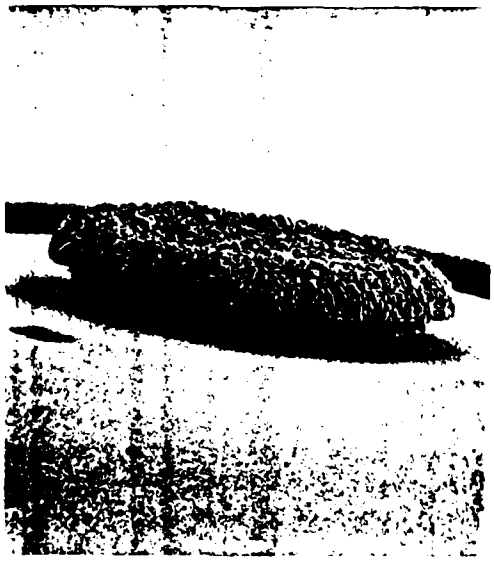
(a) AFTER Au-Ge/Ni/Au EVAPORATION, (b) WAFER AFTER Au PLATING, AND (c) FINAL MESA ETCHED IN (5:1:1) $H_2SO_4 : H_2O_2 : H_2O$.



(a)



(b)



(c)

1. Ohmic Contact Metallization. After rinsing the wafer in $NH_4OH:H_2O$ (1:3) and nitrogen drying, the entire front surface is metallized by evaporation of Au-Ge/Ni/Au in sequence.

2. Gold Plating. The evaporated Au-Ge/Ni/Au surface is gold plated or sputter deposited by 2 to 3 μm gold. This results in smooth soft gold for thermocompression bonding. This step is shown in Fig. 4.9a.

3. Final Mesa Etch. AZ 1375 is used for the definition of the ohmic contacts. Circular photoresist patterns 0.0015 inch in diameter are formed and the photoresist is postbaked at 120°C for 20 min. Following this, the gold-plated and ohmic contact layers are etched in C-35 gold etch for 3 min. The final mesa etch is completed in $H_2SO_4:H_2O_2:H_2O$ (5:1:1) GaAs etchant. An SEM photograph of a 35-μm diameter heterojunction GaAs/GaAlAs Schottky diode is shown in Fig. 4.10.

Since the chemical etchant $H_2SO_4:H_2O_2:H_2O$ (5:1:1) is highly isotropic, it results in a significant undercut and leaves a metal overhang around the diode edges.

Figure 4.11 is an SEM photograph of a 25-μm diameter GaAs diode. Significant undercut is clearly seen. This metal overhang would cause problems for the consequent processing steps or during thermocompression bonding resulting in shorting. The following process solves these problems. Due to time limitations the process proposed in Fig. 4.12 was not realized in the laboratory. The processing steps for this new process are:

1. Ohmic Contact Metallization. After rinsing the wafer in $NH_4OH:H_2O$ (1:3) and nitrogen drying, the entire front surface is metallized by evaporation of Au-Ge/Ni/Au in sequence.

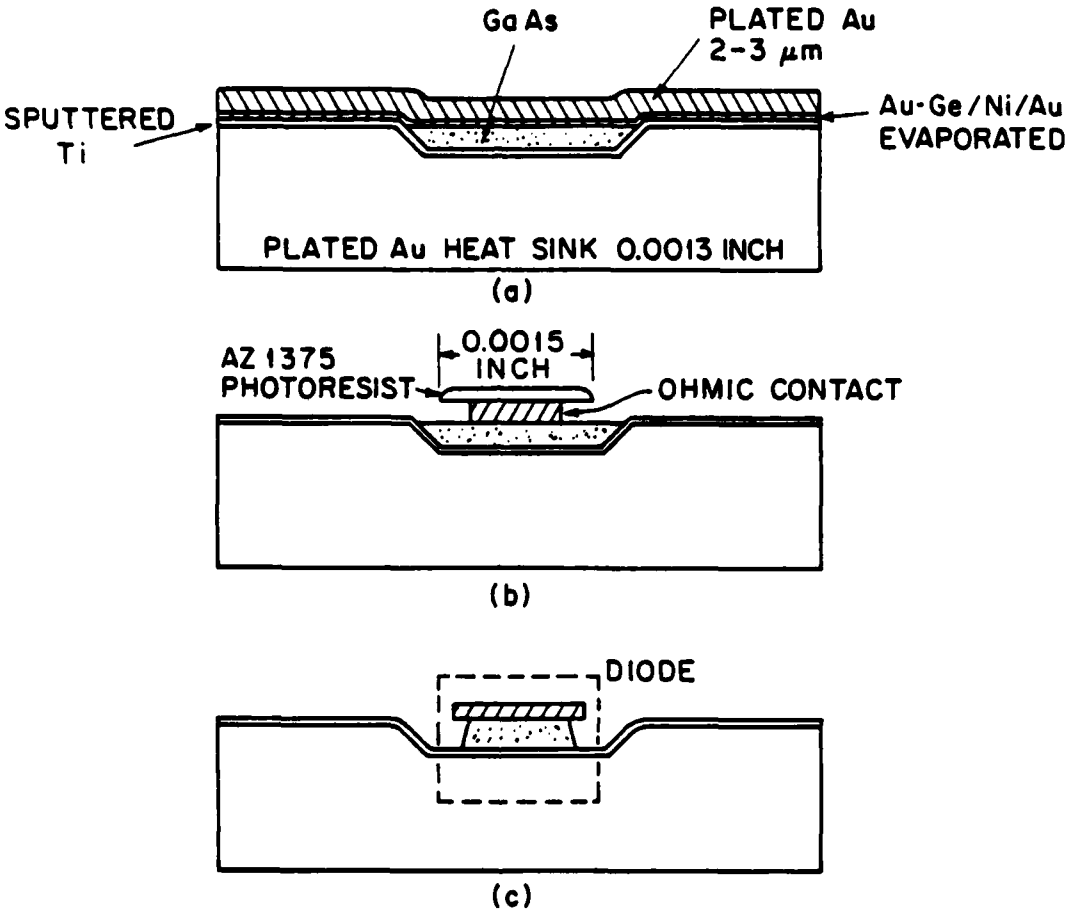


FIG. 4.9 PROCESS STEPS USED IN DEVICE FABRICATION. (a) AFTER Au-Ge/Ni/Au EVAPORATION AND GOLD PLATING, (b) OHMIC CONTACT DEFINITION, AND (c) FINAL MESA ETCH IN $H_2SO_4:H_2O_2:H_2O$ (5:1:1).

FIG. 4.10 HETEROJUNCTION GaAs/$Ga_{0.6}Al_{0.4}As$ MILLIMETER-WAVE DIODE. DIAMETER IS 0.0015 INCH. AS SEEN FROM THE PHOTOGRAPH, THE FINAL MESA ETCH IS NOT COMPLETED. (1000X MAGNIFICATION)

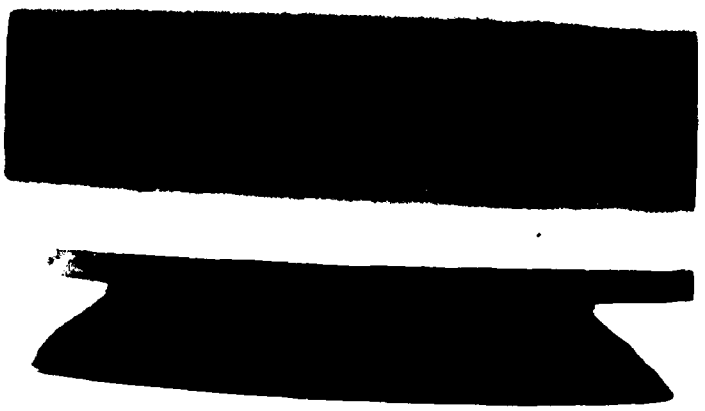


FIG. 4.11 SEM PHOTOGRAPH OF 25-μm DIAMETER GaAs DIODE. THE GaAs LAYER THICKNESS IS 3.3 μm AND THE CONTACT METAL LAYER THICKNESS IS 0.8 μm. (3500X MAGNIFICATION)

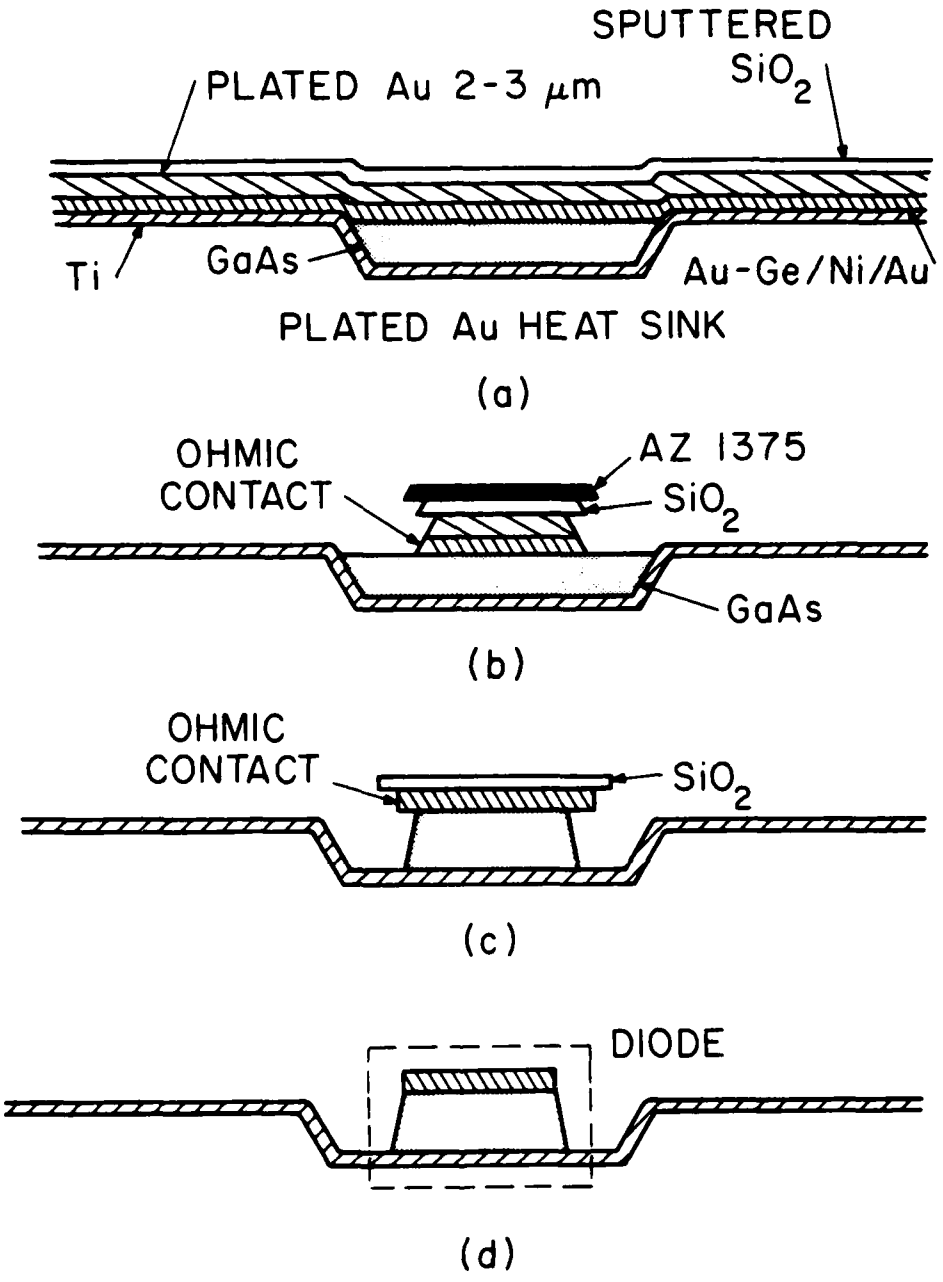


FIG. 4.12 PROCESS STEPS TO ELIMINATE THE METAL OVERHANG. (a) AFTER Au-Ge/Ni/Au EVAPORATION, GOLD PLATING, AND SiO_2 SPUTTERING; (b) SiO_2 AND OHMIC CONTACT DEFINITION; (c) FINAL MESA ETCH; AND (d) FINAL OHMIC CONTACT METAL OVERHANG ETCHING AND REMOVAL OF SiO_2.

2. Gold Plating. The evaporated Au-Ge/Ni/Au surface is gold plated or sputtered by 2 to 3 μm gold.

3. Contact Metal Patterning. The whole contact metal surface is covered by 0.3 to 0.5 μm sputtered SiO_2 and patterned by AZ 1375 photoresist. The SiO_2 is defined by etching in buffer HF. The contact metal is then etched in C-35 gold etchant using SiO_2 and AZ 1375 as a mask defining the top contact of the diode.

4. Final Mesa Etching. Since SiO_2 is not etched by $H_2SO_4:H_2O_2:H_2O$ (5:1:1) the SiO_2 mask stays on the top of the ohmic contact during final mesa etching. As before, the top contact metal is a mask for the final mesa etch in $H_2SO_4:H_2O_2:H_2O$ (5:1:1 volume ratio) standard GaAs etchant.

5. Final Overhang Metal Etching. Since SiO_2 stays on the ohmic contact metal, it is used as a mask to etch the overhang metal around the edges of the diode top contact. Since SiO_2 is transparent, the removal of the overhang metal in C-35 can be done very easily and inspected during the etching.

The process shown in Fig. 4.12 is self-aligned and very useful for millimeter-wave device fabrication.

4.3.3 Common Problems Associated with Mesa Diodes. It is well known that the metal-semiconductor interface is more chemically active and etches faster than the bulk semiconductor material in most chemical etchants. The annealed ohmic contacts are also susceptible to attack by certain chemical etchants. As an etching experiment, a Au-Ge/Ni/Au (1500 Å - 500 Å - 1000 Å) ohmic contact was patterned and annealed at 475°C for 90 s. After annealing, $HCl:H_2O_2:H_2O$

(80:4:1) etch was used for final mesa etching. As seen in the SEM picture (Fig. 4.13), the annealed ohmic contact was attacked by the etching solution. In another sample, the annealing cycle was omitted and final mesa etching was done right after the ohmic contact patterning in the same etchant. The ohmic contact was not attacked for the sample with no annealing. The same behavior was also observed with $H_2SO_4:H_2O_2:H_2O$ (5:1:1) GaAs etchant. Figure 4.13 also reveals that certain spots on the ohmic contact surface were attacked the most. The Au-Ge/Ni/Au ohmic contact "balled up" during the annealing cycle, which is common for annealed ohmic contacts to GaAs. The chemical composition of these "balled-up" regions is different from the rest of the ohmic contact surface. It appears that some chemical elements present in these regions are attacked by the chemical etchants. The results obtained in this work and other published results suggest that the final mesa etching should be performed before the ohmic contact annealing to avoid excessive ohmic-contact-semiconductor-surface etching. It was also reported by Vossen and Kern[40] that Ge is etched in dilute H_2O_2. The most common etchants for GaAs contain H_2O_2 in their composition. The Ge component of Au-Ge (88 percent Au and 12 percent Ge) eutectic material is susceptible to attack by most of these etchants, particularly after ohmic contact annealing.

At millimeter-wave frequencies the diode area must be small to maintain reasonable impedance levels. Typical diode diameters for the frequencies 44 to 94 GHz are in the range of 50 to 20 μm, which are smaller or the same size as the bonding ribbon (or wire) used for the thermocompression bonding. The small size often dictates

FIG. 4.13 SEM PHOTOGRAPH OF Au-Ge/Ni/Au (1500 Å - 500 Å - 1000 Å) OHMIC CONTACT DIODE ETCHED IN $HCl:H_2O_2:H_2O$ (80:4:1) GaAs ETCHANT AFTER OHMIC CONTACT ANNEALING AT 475°C FOR 90 s. CERTAIN SPOTS ON THE OHMIC CONTACT SURFACE WERE ATTACKED AND ETCHED AWAY BY THE ETCHING SOLUTION. (500X MAGNIFICATION)

sophisticated packaging techniques and special equipment, which are available only in a few advanced research laboratories. As reported by Ma et al.[41] and Masse et al.,[42] the optimum GaAs layer thickness is approximately 5 to 7 μm for millimeter-wave diodes. The initial ohmic contact diameter should be large, typically 50 to 75 μm to obtain some mechanical strength and ease for thermocompression bonding and packaging. After the thermocompression bonding of the diode to the package, the junction capacitance of the diode, measured near the breakdown voltage, is adjusted by etching the mesa to the desired size in situ, after which the diode is cleaned. In the following section the beam-lead diode fabrication process is presented.

4.3.4 Beam-Lead IMPATT Diodes. This process was developed as an alternative packaging technique. In this process the diode lead which will be used for the diode-to-quartz stand-off transition is fabricated along with the diode itself. First fabrication results show that this packaging without any dielectric support layer is extremely difficult to work with for small geometry, small area diodes. The lead comes off very easily under minimal stress. The ohmic contact diameter used for the beam-lead diode was 35 μm. This is very small compared to the other beam-lead diode fabrication process developed by Adlerstein and Chu.[43] The process steps used for the beam-lead diodes are:

1. After wafer thinning and GaAs pocket formation, Au-Ge/Ni/Au is evaporated and 2 to 3 μm gold is plated over the ohmic contacts. The ohmic contact is patterned with AZ 1375 photoresist and GaAs is etched in $H_2SO_4:H_2O_2:H_2O$ (5:1:1 volume ratio) resulting in 35-μm diameter and 3-μm thick mesa diodes.

2. After the mesa diode fabrication, the beam lead is formed by the following process. A support layer of photoresist, AZ 1375, is deposited and prebaked for 10 min at 80°C.

3. Using a 10-μm diameter contact hole mask the first layer photoresist is exposed and developed. The develcped photoresist pattern is postbaked at 120°C for 30 min.

4. A patterned photoresist surface is metallized by Cr-Au evaporation (Ti-Au metallization recommended).

5. A second photoresist layer is deposited and exposed with the beam-lead pattern mask. After developing the second layer photoresist is baked for 30 min at 80°C.

6. Gold (5 to 10 μm thick) is electroplated over the beam-lead pattern area.

7. The top layer photoresist is exposed and removed in AZ developer solution; consequently, Au and Cr are etched away.

8. The bottom layer photoresist is removed in acetone and the beam lead is formed over the mesa diode.

The processing steps for beam-lead diodes are illustrated in Fig. 4.14. The breaking of the beam lead from the top diode surface and the difficulty with packaging is believed to be due to the small geometry used in the work (i.e., 35-μm diode diameter and 10-μm beam-lead contact area to the diode). This technique is demonstrated to work well when the diode is 75 μm in diameter or larger.[43] The advantages of the beam-lead IMPATT diode is the low inductance due to large beam-lead width (typically 100 μm) and elimination of thermocompression bonding to the diode contact, which often causes

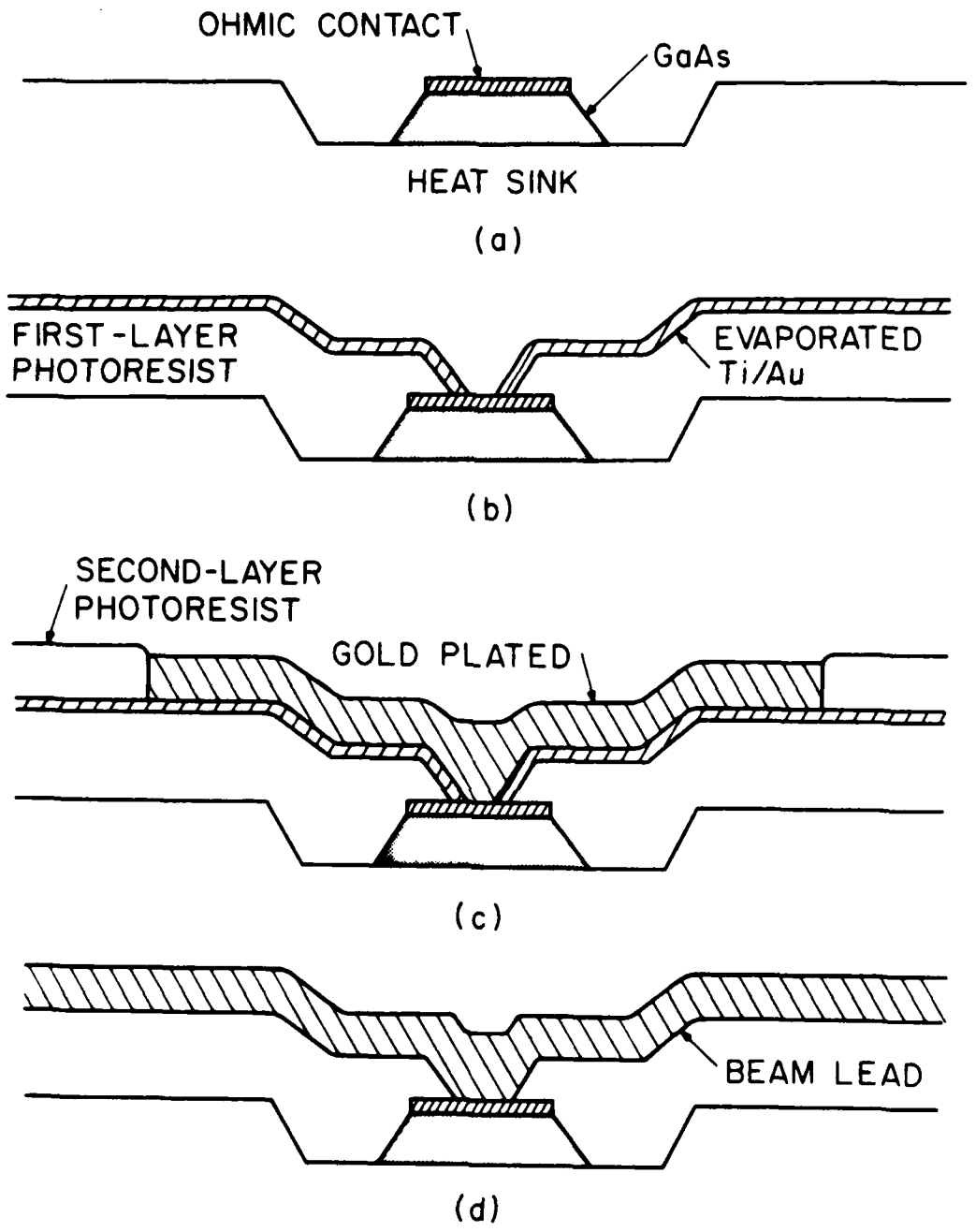
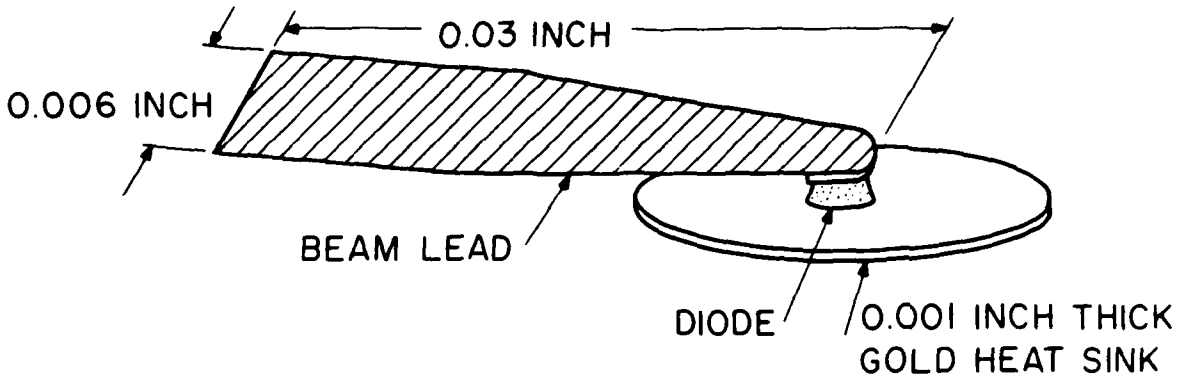


FIG. 4.14 BEAM-LEAD DIODE FABRICATION PROCESS. (a) MESA DIODE, (b) FIRST-LAYER PHOTORESIST PATTERN AND Ti/Au EVAPORATION, (c) SECOND-LAYER PHOTORESIST PATTERN AND GOLD ELECTRO-PLATING, AND (d) COMPLETED BEAM-LEAD DIODE.

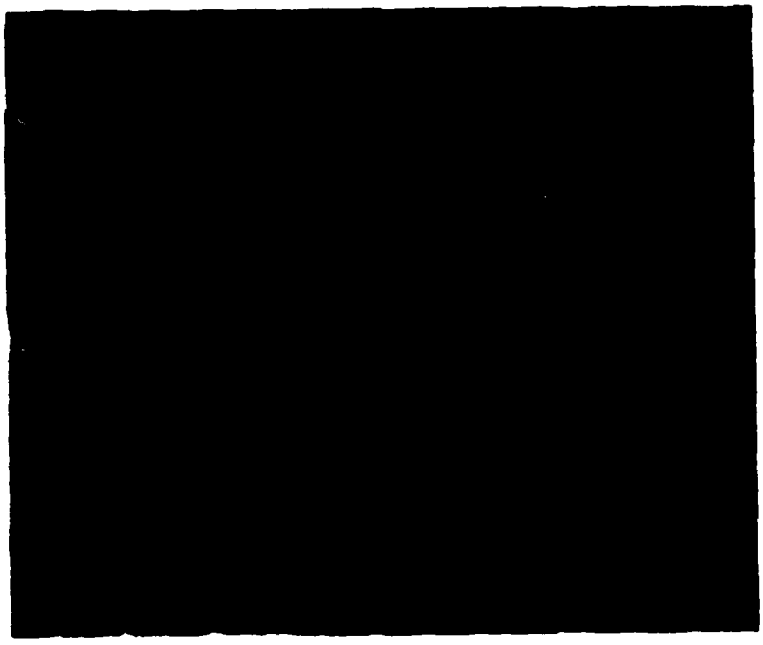
mechanical damage and is very difficult to work with. Figure 4.15 shows the SEM photograph of the beam-lead diode.

4.3.5 Polyamide Supported IMPATT Diodes. The difficulties associated with small geometry IMPATT diode fabrication and device packaging were discussed in the previous sections. To provide physical protection and mechanical strength to the diode, the polyamide supported diode process was developed and is referred to as the "integral packaging" technique. Bayraktaroglu and Shih[39] employed a similar process in their work. Before presenting the processing step of the "integral packaging" technique, it is worth discussing the dry etching of polyamide and its properties.

Polyamide can be deposited to any desired thickness (typically 1 to 50 μm) by spinning and multiple application to the wafer surface. It can also be fully cured at moderate temperatures (i.e., 350°C for 15 min). The dielectric constant for fully cured polyamide is reported to be approximately 3.8 ε_o. If the full curing temperature is to be avoided for certain applications, such as Schottky contact degradation, polyamide can be partially cured at lower temperatures, typically at 200 to 250°C for one hour. The partially cured polyamide still retains its flexibility and mechanical strength but is more lossy compared to the fully cured polyamide. All these features of polyamide suggest possible applications in microwave and millimeter-wave circuits. Although the polyamide film can be patterned in a positive photoresist developer solution using photoresist as a mask before it is cured, this is not suitable for fine pattern definition. Polyamide is usually patterned by etching in O_2 containing plasma. SiO_2 or silicon nitride are used as a mask for etching the polyamide in RIE or a plasma etcher.



(a)



(b)

FIG. 4.1 BEAM-LEAD DIODE. (a) BEAM LEAD STRUCTURE FABRICATED ALONG WITH THE DIODE AND (b) SEM PHOTOGRAPH OF THE BEAM-LEAD DIODE FABRICATED.

Since SiO_2 or silicon nitride is not etched in O_2 or O_2:Ar plasma, very thick (50 μm) polyamide can be etched by using a few thousand angstroms thick masking layer. The etch rate of polyamide in an RIE or a plasma etcher varies greatly with the pressure and power used during the etching. For high pressure and high power levels, the etch rates are 1 to 2 μm per minute while for low pressure and low power RIE etching the etch rate is 0.1 to 0.2 μm per minute. The RIE etching reported in this work resulted in vertical side walls with practically no undercut. In some applications, it is desirable to have a controlled slope for the side walls for metal coverage. This can be accomplished by adjusting the power and pressure used in the plasma etching. Egitto et al.[44] investigated the gas phase and surface phenomena responsible for etching polyamide in O_2-CF_4 RF plasma. In the following steps the "integral packaging" process for IMPATT diodes is presented. They are:

1. GaAs mesa IMPATT diodes are fabricated as explained in the previous sections.

2. After PI2555 polyamide is spun at 3000 rpm for 30 s, the sample is cured at 100°C for one hour, at 180°C for one hour, at 240°C for 10 min, and at 350°C for 15 min. This sequence fully cures the PI2555. The cured polyamide is resistant to HCl, trichloroethylene, acetone, methanol and most of the metal etchants.

3. The polyamide surface is covered by 2000 Å sputtered SiO_2 and the contact pattern is developed on the silicon dioxide.

4. The silicon dioxide is used as an etch mask and the polyamide is etched in O_2 plasma (RIE). The power and pressure used during etching are 120 W and 10 mTorr, respectively, resulting in 1500 Å per

min etch rate. The RIE etching of polyamide is highly anisotropic, which is shown in Fig. 4.16.

5. After the polyamide pattern is etched, the SiO_2 mask is removed in buffered HF (BHF).

6. The contact hole and the entire wafer surface is metallized by sputtering Ti and Au. A final Au contact is electroplated over the contact hole selectively using a 60-μm diameter photoresist pattern. After plating about 10 to 15 μm thick Au, the photoresist is removed and Au-Ti are etched from the surface.

The final structure of the polyamide supported diode and the SEM photograph of the contact hole etched in the polyamide is shown in Fig. 4.17.

The advantages of the "integral package" are that the polyamide gives mechanical support to the diodes and the bonding of the diode to the package is very easy. On the other hand, the diode fabrication process is more complicated and requires more processing steps. The polyamide support introduces additional parasitic capacitance to the diode junction capacitance. Unlike the mesa diodes, the diode area and junction capacitance cannot be adjusted by etching the diode after packaging. A final note is that this technique can be combined with the beam-lead process and both of their advantages can be utilized in the "polyamide supported beam-lead diodes." Instead of plating a contact over the contact hole the beam lead can be formed.

4.3.6 Proton Guarded (Isolated) IMPATT Diodes. The proton implantation technique for the isolation of GaAs devices was explained in the previous chapter. In this section, the application of the proton implantation to the fabrication of millimeter-wave IMPATT and

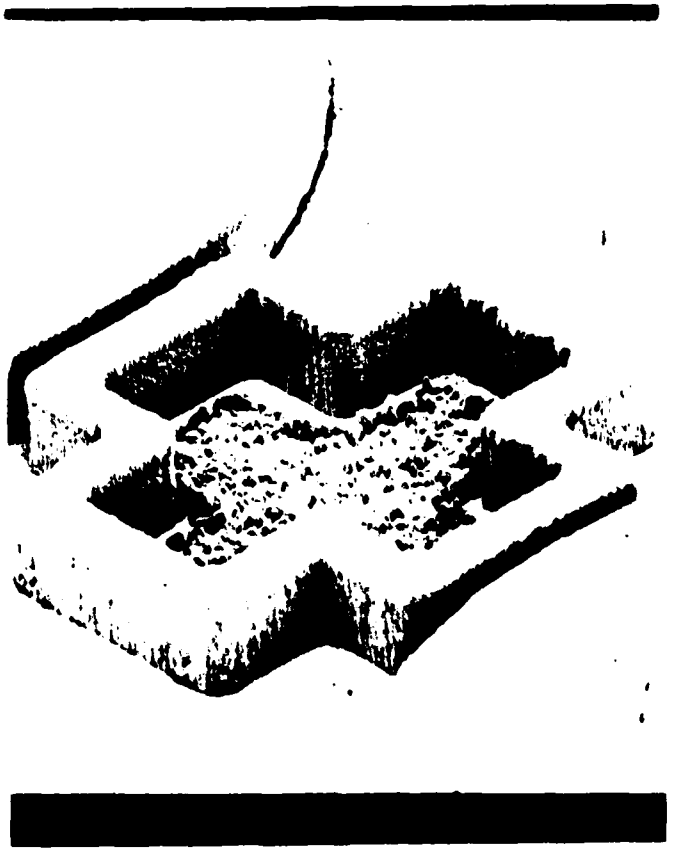
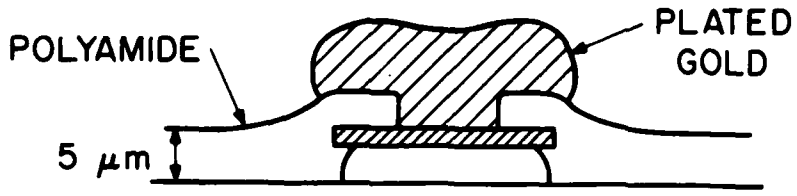
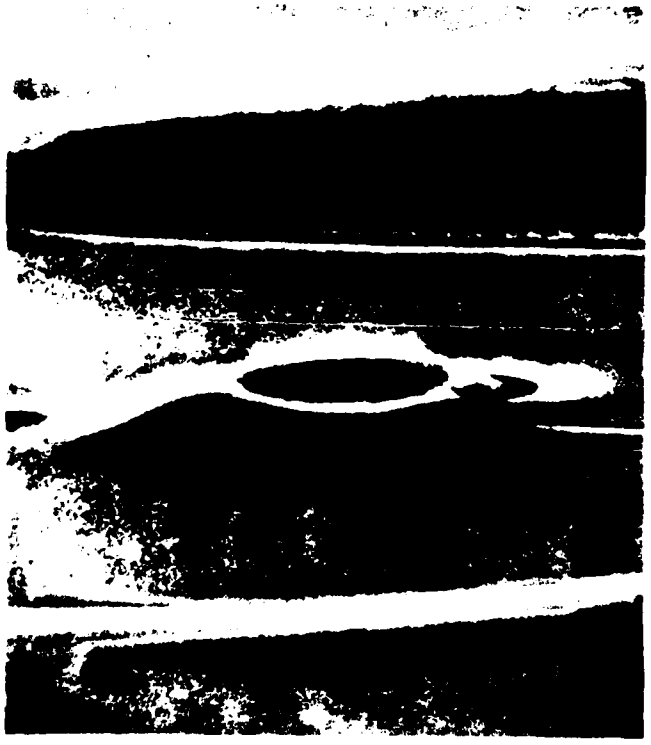


FIG. 4.16 THE SEM PHOTOGRAPH OF 15-μm THICK POLYAMIDE STRUCTURE AFTER RIE ETCHING AND Ti-Au SPUTTER DEPOSITION. MAGNIFICATION IS 370. IN THE PHOTOGRAPH, THE ALIGNMENT PATTERN IS SEEN BETWEEN THE TWO POLYAMIDE DIODES. THE WHITE COLORED LAYER IS THE SPUTTERED Au METALLIZATION.



(a)



(b)

FIG. 4.17 INTEGRAL PACKAGING OF DIODES. (a) POLYAMIDE PROCESS AND (b) 15-μm DIAMETER AND 5-μm DEEP CONTACT HOLE DEVELOPED ON POLYAMIDE USING REACTIVE ION ETCHING. (SEM MAGNIFICATION IS 1600X)

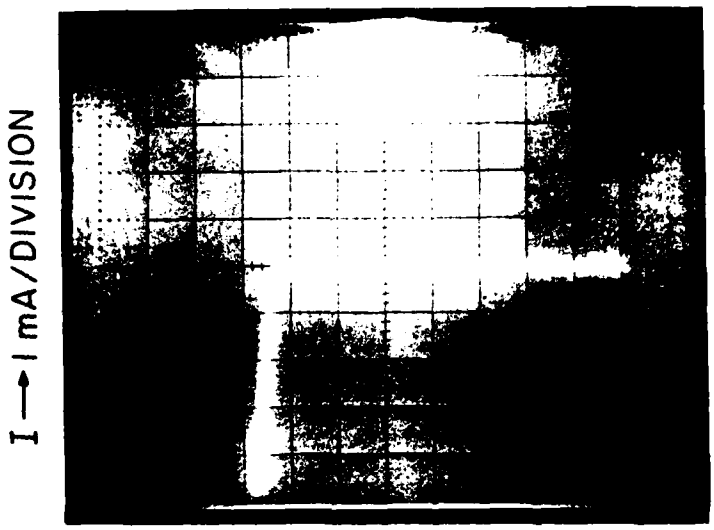
MITATT diodes is presented. Murphy et al.[45] developed proton-guarded IMPATT diodes for the frequency range between 36 and 40 GHz. The proton-guarded IMPATT diodes were single-drift GaAs Schottky diodes. Similar work was also done by Murphy et al.[46] for low-high-low GaAs IMPATT annular diodes at 3.0 GHz. Their results indicate that it is possible to obtain good performance in terms of efficiency, power levels, and heat dissipation with the proton-guarded (isolated) IMPATT diodes. It was reported by Murphy et al.[45] that the proton-guarded IMPATT diodes have superior power-sustaining capabilities (burn-out performance) compared to the conventional mesa diodes. This was also observed in this work.

Figure 3.10 shows the proton guarded double-drift GaAs IMPATT diode and the proton implantation schedule. After proton implantation, the sample was annealed at 300°C in forming gas for 30 min, which improved the large leakage current observed before the postannealing. Figure 4.18 shows the reverse-bias breakdown characteristic of the 20-μm diameter double-drift GaAs IMPATT diode. The room temperature breakdown voltage is 14.8 V for this particular diode. The reverse-bias leakage current increases linearly with the applied reverse bias voltage and reaches 4 μA before the breakdown.

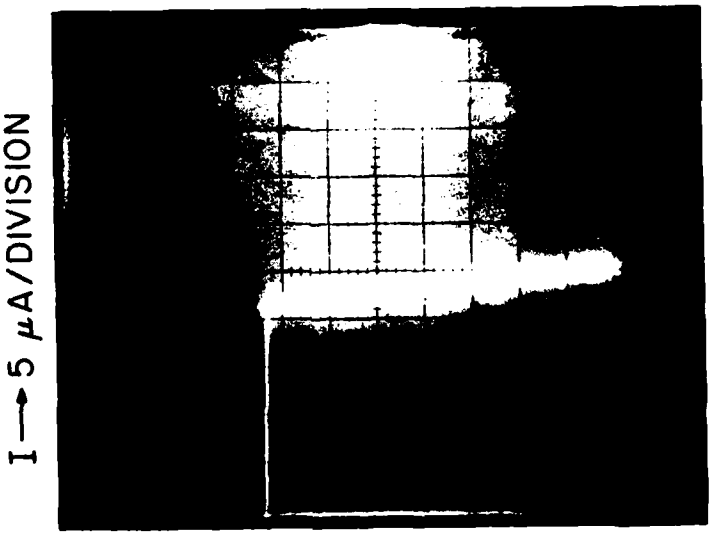
4.4 Separation of Individual Diodes

In this section, the separation of individual diodes for final device packaging is presented. Three different techniques were employed during this work.

4.4.1 Heat Sink Etching. As seen in Fig. 4.5, the GaAs 0.006-inch diameter mesa etched in the beginning of the fabrication



(a)



(b)

Fig. 4.18 THE REVERSE BIAS I-V CHARACTERISTICS OF THE 20-μm DIAMETER DOUBLE-DRIFT PROTON-GUARDED GaAs IMPATT DIODE.

process retains its shape after plating. The following steps are used in the process:

1. The wafer is mounted on a glass carrier with a wax.

2. AZ 1375 photoresist is spun on the surface and patterned.

3. Plated gold and evaporated Ti-Au is etched using the photoresist as a mask.

4. The photoresist is removed in acetone and individual diode chips floated by removing the wax in trichloroethylene followed by acetone, methanol and DI rinse.

Figure 4.19 shows the process steps for heat sink etching.

4.4.2 Selective Au-Ag Plating. The major disadvantage of the previous separation process is that etching of the thick plated gold (25 to 50 μm) takes a very long time and the photoresist is attacked at some spots resulting in pits in the heat sink. Second, this separation technique is limited to applications where a thin heat sink (25 to 50 μm) can be accommodated. For a thick plated heat sink (75 to 150 μm) this technique is certainly not useful.

The selective plating technique developed during this work eliminated most of the problems mentioned here. The following sequence is used in the formation of the heat sink:

1. AZ 1375 photoresist is patterned and gold (10 μm), silver (50 μm) and gold (10 μm) are plated in sequence.

2. The photoresist is removed in acetone and 3 μm gold plated over the whole surface.

3. The final silver layer (50 μm) is plated over the entire surface.

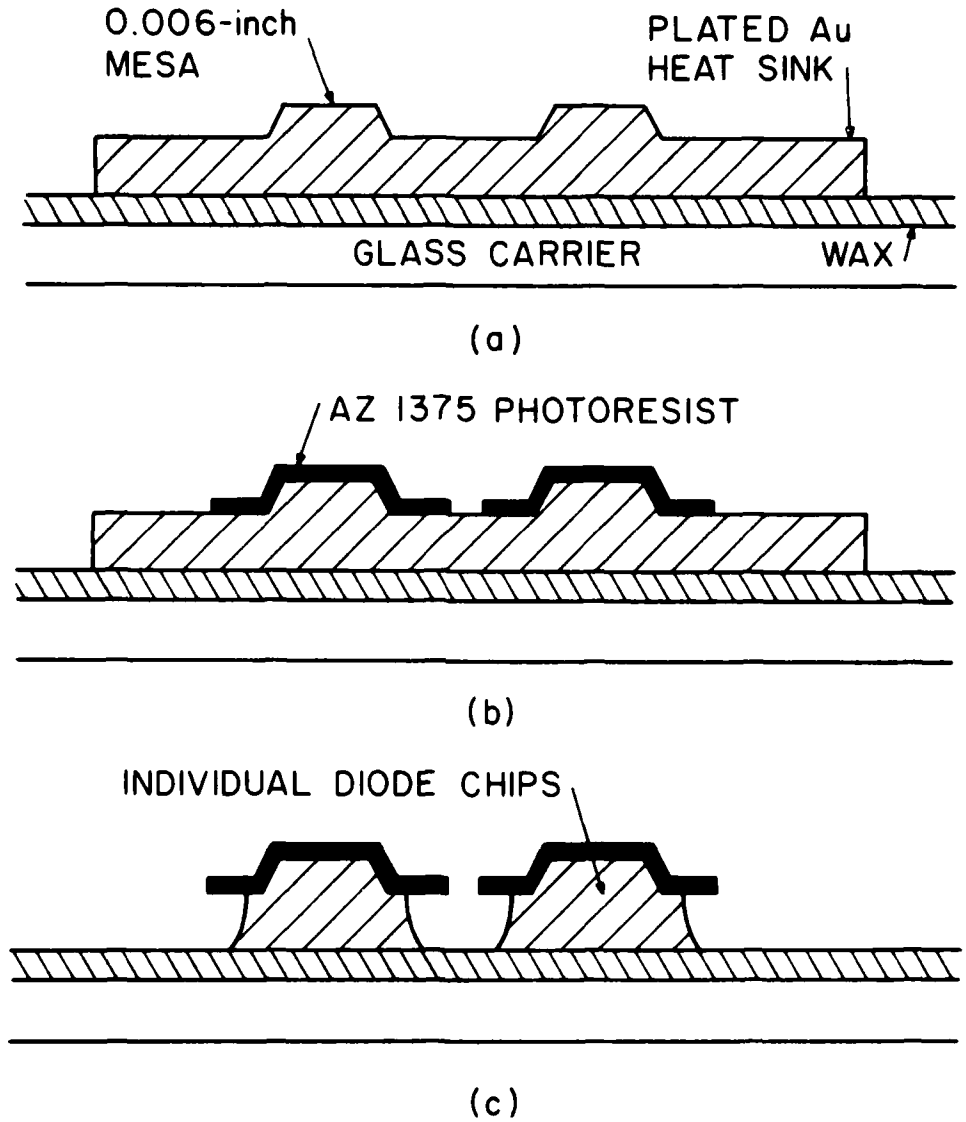


FIG. 4.19 (a) WAFER IS MOUNTED ON A GLASS CARRIER WITH A WAX. (b) AFTER PHOTORESIST PATTERNING. (c) AFTER GOLD ETCHING.

Figure 4.20 shows the selectively plated heat sink structure. For the separation of individual diodes the following steps are used:

1. The wafer is mounted on a glass carrier with a wax.

2. The silver is removed in HNO_3:H_2O (1:1) which etches silver with an etch rate approximately 10 μm/min.

3. A brief Au etch and Ti etch separate the individual diodes into small chips.

4. The wax is removed in trichloroethylene and the chips are cleaned in acetone, methanol and DI water.

4.4.3 Wafer Saw Cutting. A commerical wafer saw can be used to separate the individual diodes. Since a wafer saw was not available, individual diodes were separated with a razor blade under a microscope. This can only be done for wafers with 25 to 50 μm gold-plated heat sink since plated gold is very soft and can be cut with a razor blade.

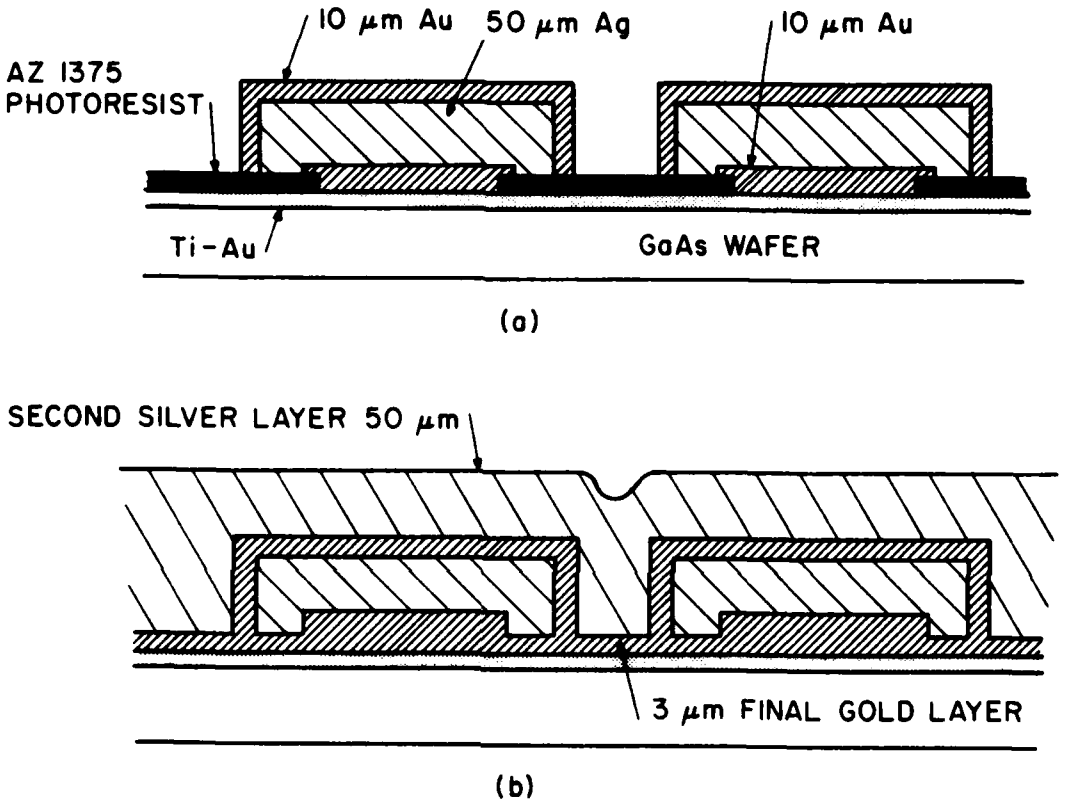


FIG. 4.20 SELECTIVE HEAT SINK PLATING. (a) AFTER SELECTIVE Au-Ag-Au PLATING. (b) AFTER Au-Ag PLATING OVER THE WHOLE SURFACE.

CHAPTER V. MILLIMETER-WAVE OSCILLATOR CIRCUITS AND DIODE DC AND RF CHARACTERISTICS

5.1 Introduction

In this chapter, the waveguide circuits for millimeter-wave two-terminal devices and the dc and RF characteristics of the diodes fabricated during this work are presented.

After a brief overview of commonly used millimeter-wave circuits, the equivalent circuit for the "coaxial-gap" mounting structure is given. A disk resonator circuit employing a radial choke in the bias port is used in this work and it is presented in a subsequent section. Following the discussion on the waveguide circuit, the packaging of the diodes and its effects on the device-circuit interactions are discussed.

The dc characteristics of the heterojunction MITATT and GaAs IMPATT diodes are presented in a subsequent section. Finally, the measurement setup used in the RF characterization of the diodes and the RF performance are presented.

5.2 Millimeter-Wave Oscillator Circuits

In the past, various types of oscillator circuits have been developed for millimeter-wave IMPATT diodes. Examples of basic types are shown in Fig. 5.1. They may be grouped into three basic types, such as (1) reduced height, (2) hat resonator (or disk resonator), and (3) coaxial waveguide cavity circuits. In each circuit, tuning elements are used to achieve optimum performance at a specified

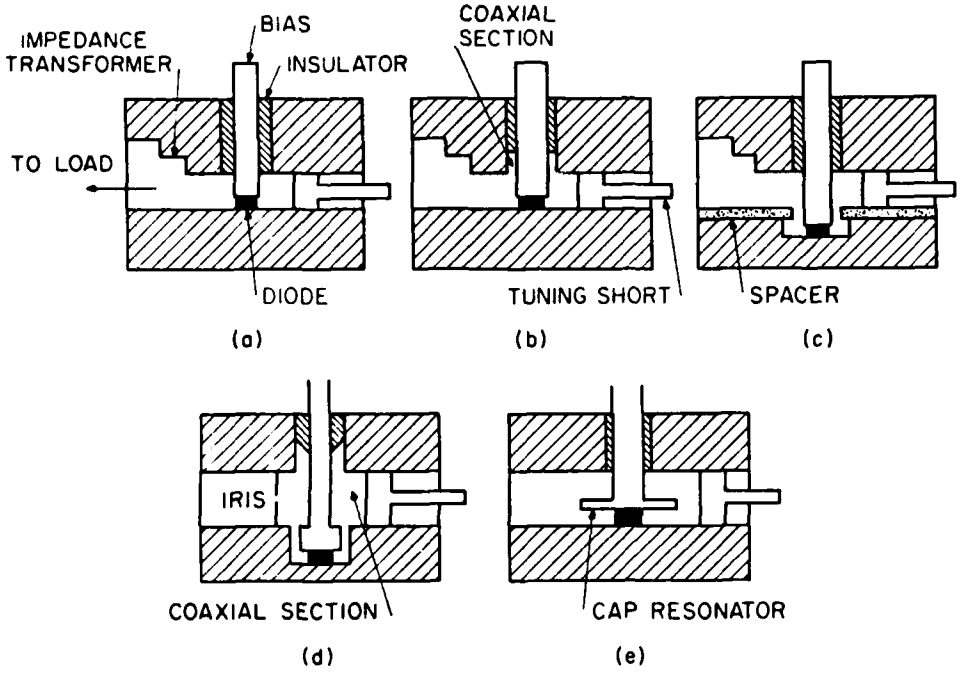


FIG. 5.1 EXAMPLES OF MILLIMETER-WAVE IMPATT OSCILLATOR CIRCUITS. (a) AND (b) REDUCED-HEIGHT WAVEGUIDE CIRCUITS, (c) COAXIALLY COUPLED REDUCED-HEIGHT WAVEGUIDE CIRCUIT, (d) CROSS-COUPLED COAXIAL-WAVEGUIDE CIRCUIT (KUROKAWA CIRCUIT), AND (e) HAT RESONATOR (OR DISK RESONATOR) WAVEGUIDE CIRCUIT.

frequency. The frequency tuning is accomplished by varying the disk resonator or the position of the moveable short. Of the three waveguide circuits, the reduced-height waveguide oscillator circuit is the most commonly used circuit at millimeter-wave frequencies. Millimeter-wave oscillator circuits should have the following desired characteristics:

1. Stability and protection against low-frequency instabilities (i.e., bias-circuit oscillations).

2. Low driving-point impedance characteristics for the diode-circuit impedance matching.

Figure 5.1a and b show the reduced-height waveguide oscillator circuits. The anodized insulator section can be moved up or down forming a coaxial section on the coaxial-waveguide interface. The adjustment of the insulator section in the bias line changes the driving-point impedance seen by the diode and the impedance matching can be accomplished by this adjustment.

Figure 5.1c shows the coaxially coupled reduced-height waveguide oscillator circuit. The impedance matching of the diode to the waveguide circuit is achieved by placing spacers of different hole diameter and thickness. Figure 5.1d shows the cross-coupled coaxial-waveguide oscillator circuit, which is also referred to as the "Kurokawa circuit." The matching is accomplished by the adjustment of the lengths of the waveguide and coaxial-line short-circuited sections. A tapered absorber is attached to the other end of the coaxial line for stabilization purposes. This circuit is more commonly used in power combiners. Finally, Fig. 5.1e shows the hat resonator (disk resonator) waveguide circuit that is also

used in this work. The detailed description of this circuit is presented in the following sections.

For the successful design of the millimeter-wave oscillator circuits the following analysis must be performed. First, a theoretical model describing the waveguide circuit and the driving-point impedance must be developed. Second, the package parasitic elements (i.e., bonding lead inductance and quartz or ceramic ring package capacitance) must be measured and chosen properly. Finally, the large-signal impedance characteristics of the diode must be determined using a simulation program. Once this analysis is established, the circuit dimensions and the package parasitic element values can be determined after few iterations to obtain the best diode-circuit impedance matching condition. The most basic structure that is equivalent to the various oscillator circuits presented in Fig. 5.1 is shown in Fig. 5.2. This mounting structure was investigated by Lewin[47] and Eisenhart.[48] While reasonable results may be obtained in some cases, Lewin's analysis does not take into account the dimensions of the coaxial aperture. Recognizing that the coaxial aperture dimensions have a significant effect, Eisenhart et al.[49] proposed that the coaxial aperture be modeled as a finite gap (which is called "the equivalent gap"). This equivalent gap was determined for the C-band and X-band waveguide circuits experimentally for certain coaxial-waveguide functions. Using this equivalent-gap concept and his model of the two-gap waveguide mount, Eisenhart obtained results for the waveguide structure shown in Fig. 5.2. The only theoretical model that does not need experimental measurement of the equivalent gap was developed by Williamson.[50] The theoretical expressions

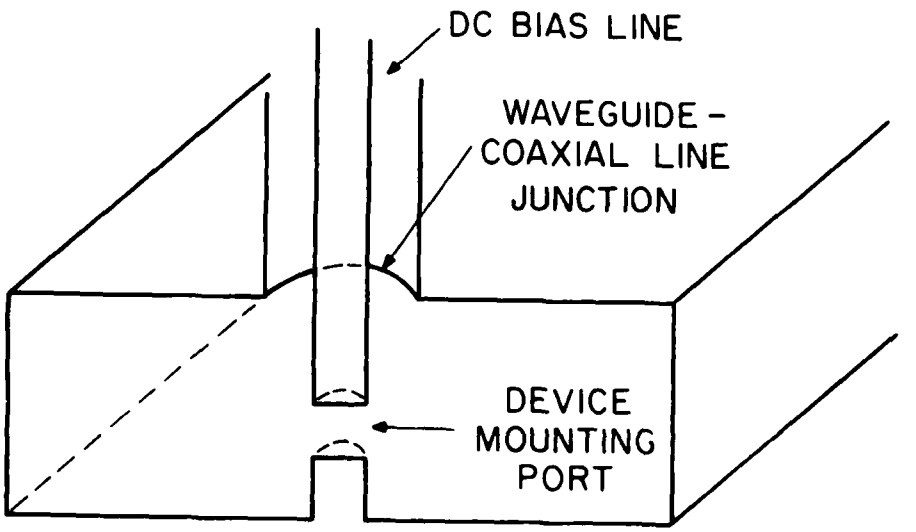


FIG. 5.2 A SECTIONAL VIEW OF THE TWO-GAP "COAXIAL-GAP" MOUNTING STRUCTURE.

obtained by Williamson yield results in excellent agreement with published experimental results. The equivalent circuit developed by Williamson is given in Fig. 5.3 for the "coaxial-waveguide" mounting structure presented earlier. The susceptances B_a, B_b, and B_c and reactances X_a, X_b and the transformer ratios R_1 and R_2 are given by Williamson.[50] Various termination conditions and the driving point impedances seen from the gap port can be calculated using his results.

5.3 Hat Resonator Waveguide Oscillator Circuit

In this section, the oscillator circuit used in this work is described. The circuit utilizes a radial choke in the dc bias port for an RF termination. For mechanical flexibility, a bellow is used with an OSM connector. This allows the testing of uncapped fragile structures such as quartz-standoff packaged diodes.

Although hat resonator waveguide circuits have been used successfully at millimeter-wave frequencies (30 to 100 GHz), they have not been analyzed and modeled successfully in terms of the theoretical calculations of the driving-point impedances. Groves and Lewis[51] reported a series of measurements at 10 GHz using a hat resonator waveguide circuit for Si IMPATT diodes. The effects of the cap diameter, cap height above the waveguide wall, contact-post diameter, and cap thickness on the oscillator performance were presented in their results. Döring and Seebald[52] measured the input impedance of the radial line in a waveguide at (3.5 to 5.5 GHz). Their results show that the radial line transforms the high impedance

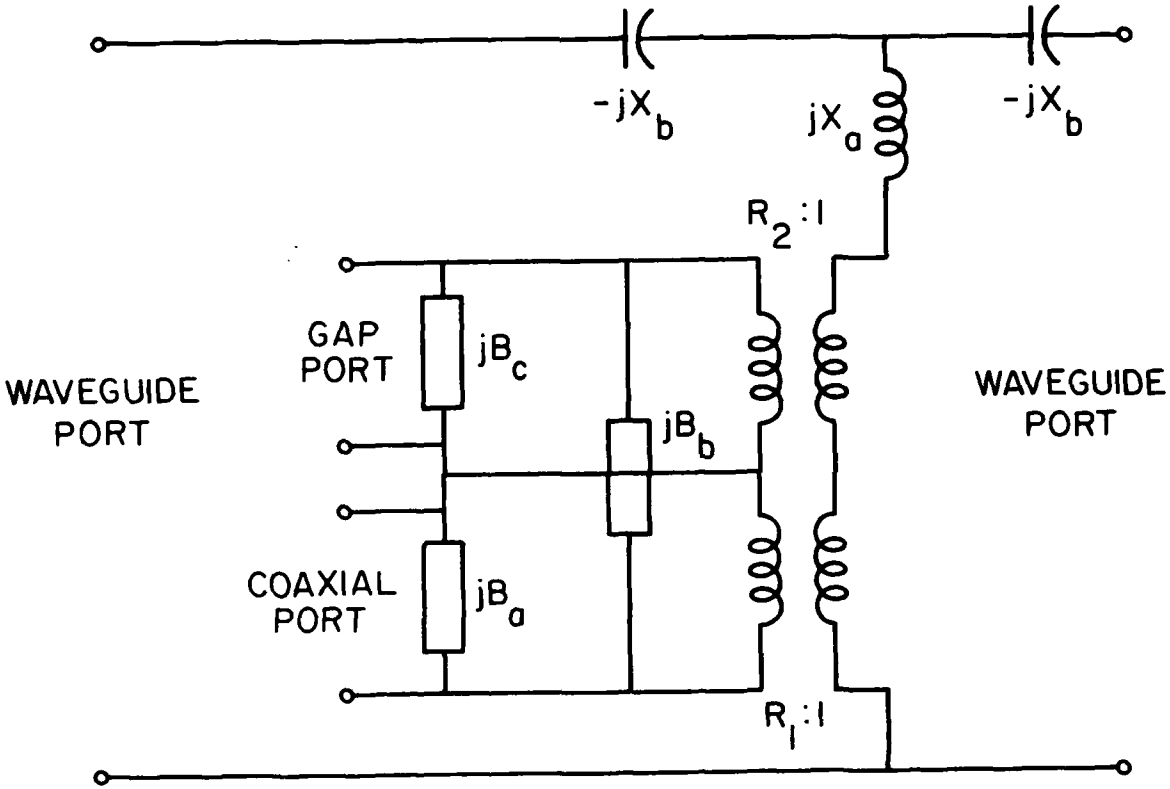


FIG. 5.3 EQUIVALENT CIRCUIT FOR THE MOUNT SHOWN IN FIG. 5.2 FOR THE CASE WHERE THE TE_{10} MODE IS THE ONLY PROPAGATING WAVEGUIDE MODE. (WILLIAMSON[50])

of the waveguide to a low impedance level, which is the desired characteristic for IMPATT diode mounting.

The cap resonator in this circuit has two useful functions. First, it acts as a resonating element and the cap diameter determines the oscillation frequency. This eliminates the multiple frequency operation of the oscillator circuit, which is a common problem in the inductive post mounting structures. Second, it acts as an impedance transformer facilitating the diode-circuit impedance matching.

In the following, the design of the circuit used in this work is presented. Since the WR-15 waveguide is used, the cavity dimensions of the oscillator circuit are chosen as 0.148 x 0.074 inch for the V-band oscillator. Figures 5.4 and 5.5 show the oscillator circuits used for V-band (50 to 75 GHz) and W-band (75 to 110 GHz) IMPATT diodes, respectively. The circuits are the same for both the V-band and the W-band frequencies except the dimensions have been scaled down for the W-band circuit. The dimensions of the cavity for the W-band oscillator are 0.1 x 0.05 inch. To obtain better mechanical performance and flexibility, these circuits employ precision bellows to minimize the force on the quartz-standoffs and SMA connectors in the dc bias section. A radial choke is used as a low-pass filter on the dc bias port. The coaxial line above the radial choke was terminated by a tapered lossy material. The important dimensions are shown in Figs. 5.4 and 5.5 for these circuits. The dimensions of the radial chokes and the quarter-wave sections of the coaxial lines were chosen for 60 and 94 GHz operating frequencies for the V-band and W-band oscillator circuits, respectively.

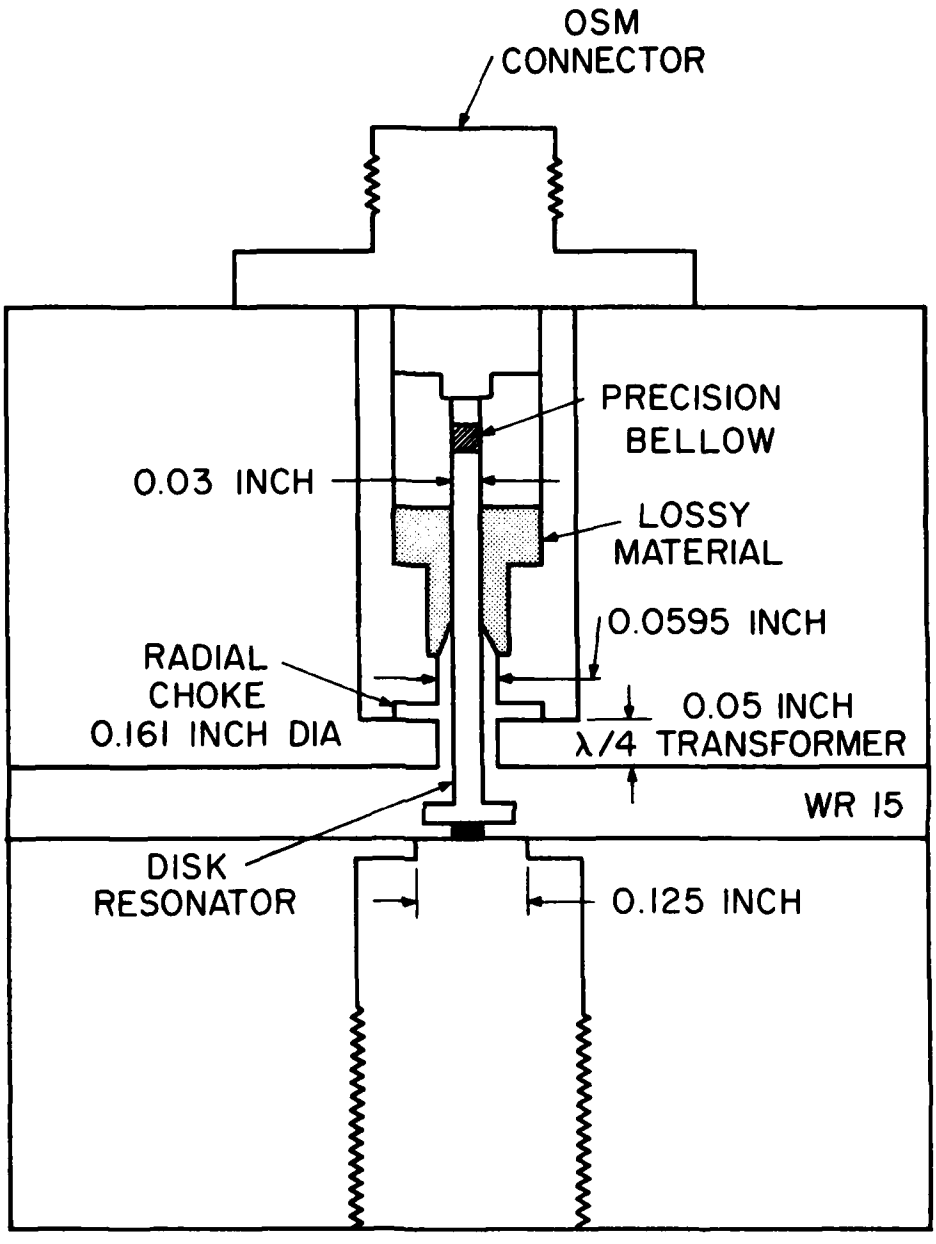


FIG. 5.4 THE CROSS SECTION OF THE V-BAND OSCILLATOR CIRCUIT. (60 GHz). THE DIMENSIONS IN THE FIGURE ARE FIVE TIMES THE ACTUAL SIZE.

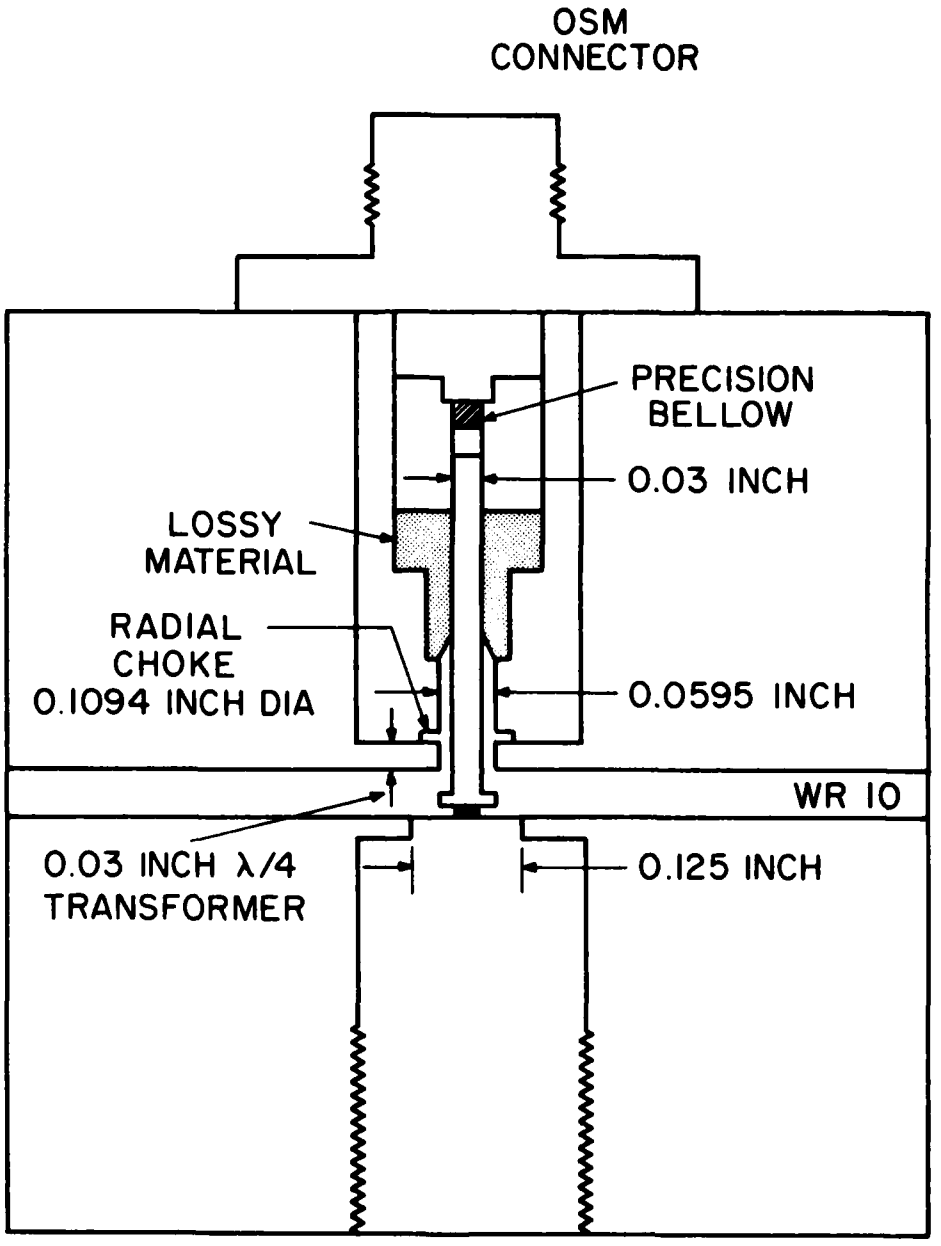


FIG. 5.5 THE CROSS SECTION OF THE W-BAND (94 GHz) OSCILLATOR CIRCUIT. THE DIMENSIONS IN THE FIGURE ARE FIVE TIMES THE ACTUAL SIZE.

The post diameter was chosen to be 0.03 inch for both the V-band and the W-band circuits. The thicknesses of the disk resonators were 0.02 inch. The disk resonator diameters were 0.12, 0.1 and 0.08 inch for the V-band circuit and 0.07, 0.06 and 0.05 inch for the W-band circuit. Besides the disk resonators, 0.03 inch diameter bias posts were also used in these circuits.

Figure 5.6 shows the V-band oscillator circuit. The piece on the left is the top piece of the circuit that includes the dc bias section. The mounted OSM connector and the 0.12 inch diameter disk resonator are clearly shown. Figure 5.6 also shows the bottom piece including the 0.1, 0.08 inch disk resonators, 0.03 inch bias post, brass diode mounting piece, and the back short.

Figure 5.7 shows the W-band oscillator circuit. The OSM connector with the bellow attached and the other parts are shown in the photograph. Finally, Fig. 5.8 shows the assembled V-band oscillator circuit with the 0.12-inch diameter disk resonator. The photograph reveals the quartz stand-off package in the mount.

5.4 Millimeter-Wave Measurement System

The measurement system used in this work is shown in Fig. 5.9. The measurement system includes an E-H tuner, a 0 to 50 dB variable attenuator, a wavemeter (frequency meter), a power detector, and a power meter. The E-H tuner is adjusted until maximum power is obtained for any dc bias condition. The oscillation frequency and the achieved power level are recorded for each dc bias value. Three different setups were used in the RF measurement of the fabricated diodes covering the frequency bands of Q (33 to

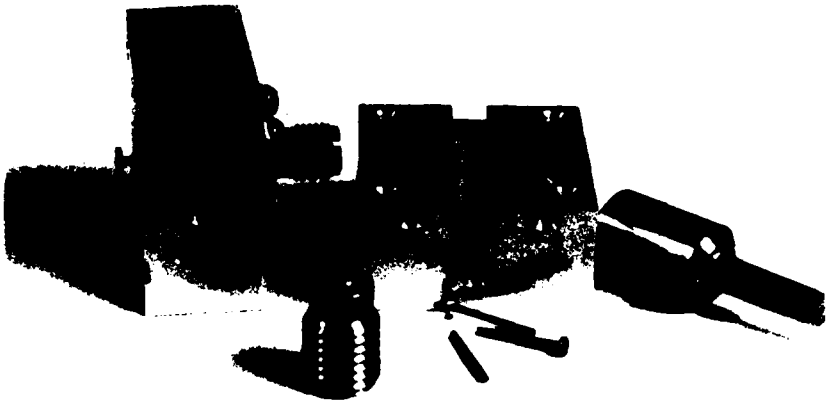


FIG. 5.6 THE V-BAND OSCILLATOR CIRCUIT. THE OSM CONNECTOR, DISK RESONATORS, BIAS POST, DIODE MOUNTING PIECE, AND BACK SHORT ARE SHOWN IN THE PHOTOGRAPH.

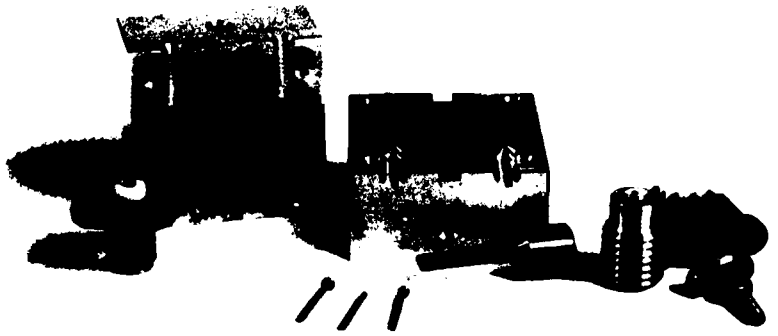


FIG. 5.7 THE W-BAND OSCILLATOR CIRCUIT. THE OSM CONNECTOR WITH THE PRECISION BELLOW ATTACHED AND THE OTHER PIECES ARE SHOWN IN THE PHOTOGRAPH.

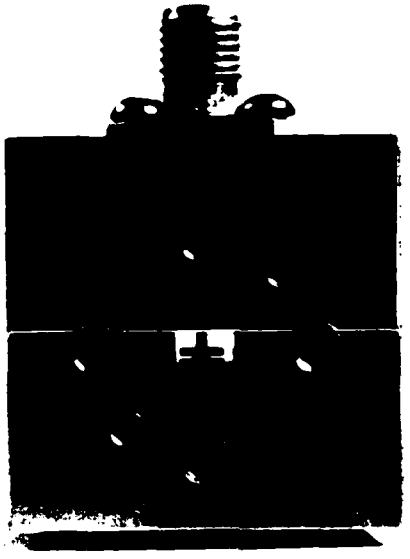


FIG. 5.8 THE ASSEMBLED V-BAND OSCILLATOR CIRCUIT WITH THE 0.12-INCH DIAMETER DISK RESONATOR. THE PHOTOGRAPH REVEALS THE QUARTZ STAND-OFF PACKAGE IN THE MOUNT. THE DIMENSIONS IN THE PHOTOGRAPH ARE TWICE THE ACTUAL SIZE.

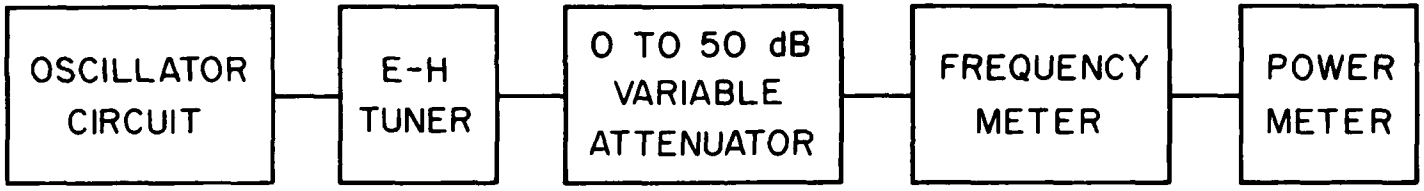


FIG. 5.9 POWER AND FREQUENCY MEASUREMENT SETUP.

50 GHz), V (50 to 75 GHz) and W (75 to 110 GHz). Therefore, it was possible to do measurements in the wide frequency spectrum (33 to 110 GHz) of the millimeter-wave frequency region. Most of the results reported in this work were obtained in the V-band (50 to 75 GHz) frequencies.

5.5 Electrical Characteristics of the Fabricated Diodes

In this section, the current-voltage (I-V) characteristics and the capacitance-voltage (C-V) characteristics of the diodes fabricated during this work are presented. The first diode successfully fabricated in the beginning of this work was a Ti/n-GaAs Schottky diode with a doping concentration of $N_D = 2.076 \times 10^{17}$ cm^{-3} and an epitaxial layer thickness of 0.35 μm on n^+-substrate. Figure 5.10 shows the semilogarithmic graph of the I-V characteristics of the 0.001-inch diameter Ti/n-GaAs Schottky diode. It is clear from the I-V characteristics that the reverse leakage current is very small. The RF performance of this diode is presented in a subsequent section.

5.5.1 The Current-Voltage Characteristics of the Heterojunction Diodes.

A series of measurements were obtained on an MBE-grown heterojunction wafer with the doping profile shown in Table 5.1. The wafer surface was etched and covered with wax sequentially to obtain different n^+-GaAs thicknesses over the wafer. The etchant used is PA11 ($NH_4OH:H_2O_2:H_2O$) which is a slow etchant (etch rate is approximately 30 Å/s). The steps on the wafer were measured using the surface profilometer. Over the wafer surface, after this etching process, the n^+-GaAs layer thickness varied as 1100,

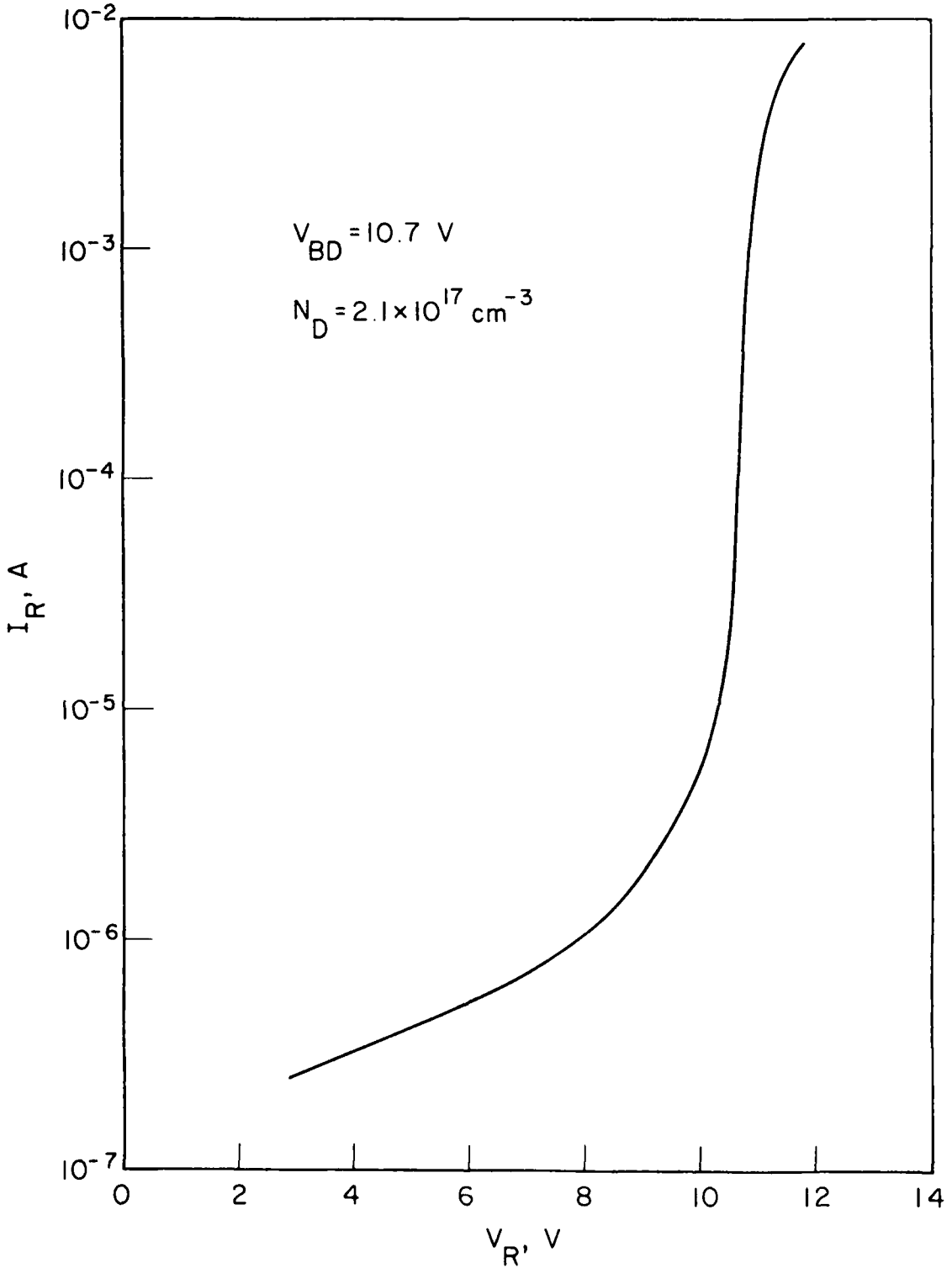
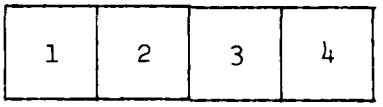


FIG. 5.10 REVERSE I-V CHARACTERISTICS OF 0.001-INCH DIAMETER Ti/n-GaAs MILLIMETER-WAVE DIODE.

Table 11

Heterojunction Wafer Doping Profile



Layer	Material	Thickness	Doping (cm^{-3})
1	GaAs	1500 Å	1×10^{18}
2	$Ga_{0.6}Al_{0.4}As$	825 Å	4×10^{16}
3	GaAs	2500 Å	4×10^{16}
4	GaAs	5000 Å	1×10^{18} (buffer)

850, 500, 400, 250, and 200 Å. In some portion of the wafer there was no n^+-GaAs present and the GaAlAs was etched slightly leaving only a 375 Å GaAlAs layer over the structure. Diodes from these different regions were probed and the electrical characteristics were obtained. The information gained from these diode characteristics was very valuable in the design of the p^+-n^+ heterojunction MITATT diode that worked successfully.

The reverse and forward I-V characteristics were measured using a curve tracer. From the measurement results the following can be concluded:

1. For 1100 and 850 Å n^+-GaAs diodes the breakdown voltage is 5.5 V. For the electric field to punch through to the buffer layer (n^+-GaAs), the minimum applied voltage needed is V_{PT_1} = 14 V and V_{PT_2} = 10 V, respectively. Thus, these diodes are nonpunch through and the drift region is not depleted. Breakdown takes place in the n^+ region. Figure 5.11 shows the reverse I-V characteristics of 1100 and 850 Å heterojunction diodes.

2. For the diodes with n^+ regions of 500, 400, 250, and 200 Å, the reverse bias current is due to tunneling for low to moderate reverse bias voltages. For large reverse bias voltages, the reverse bias current is due to avalanche breakdown. As seen in Fig. 5.12 the breakdown voltage increases gradually as the n^+ region thickness decreases for a fixed reverse bias current.

3. For the region where the n^+-GaAs is removed completely, the breakdown is purely avalanche dominated.

From these results it is clear that the thickness of the n^+-GaAs layer must be chosen properly for the design of mixed

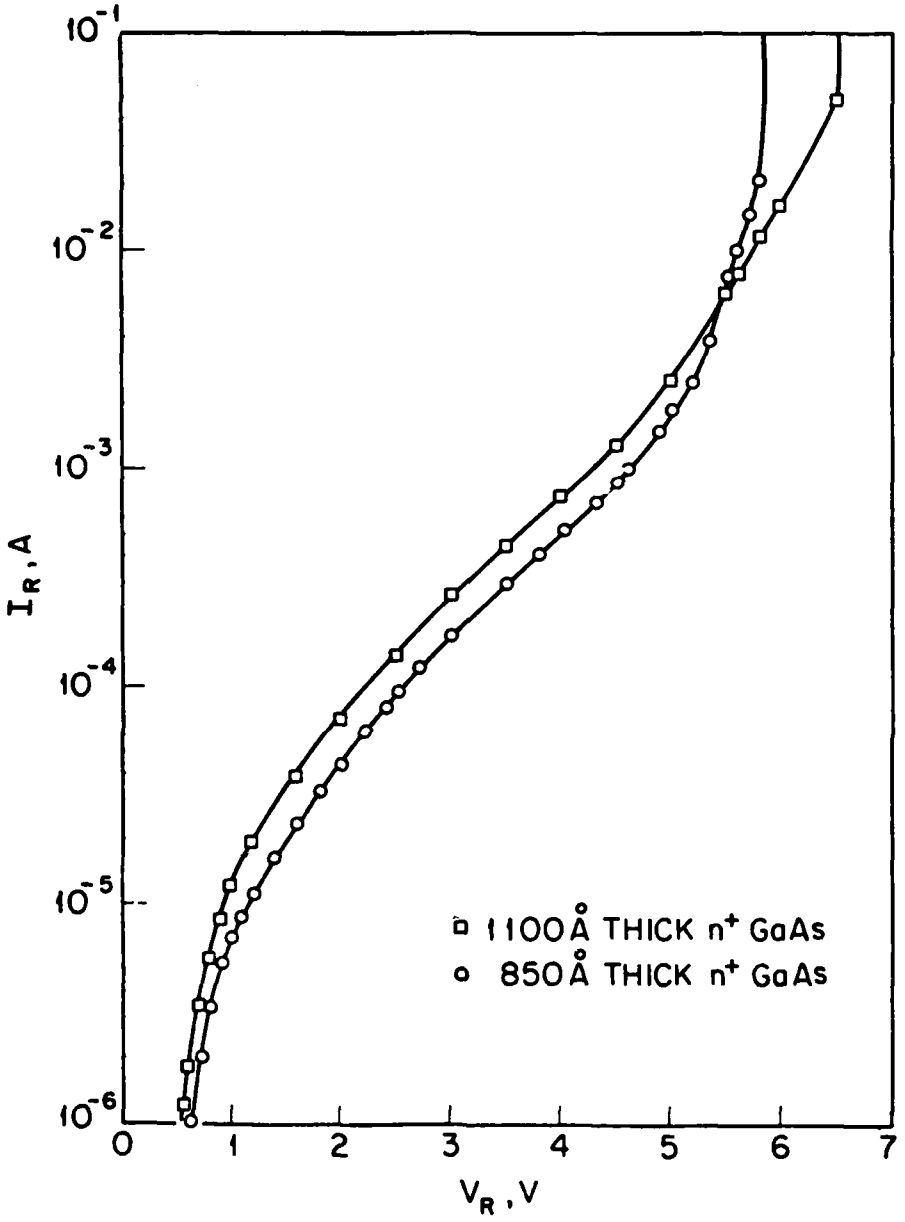


FIG. 5.11 REVERSE I-V CHARACTERISTICS OF 1100 Å AND 850 Å HETEROJUNCTION DIODES.

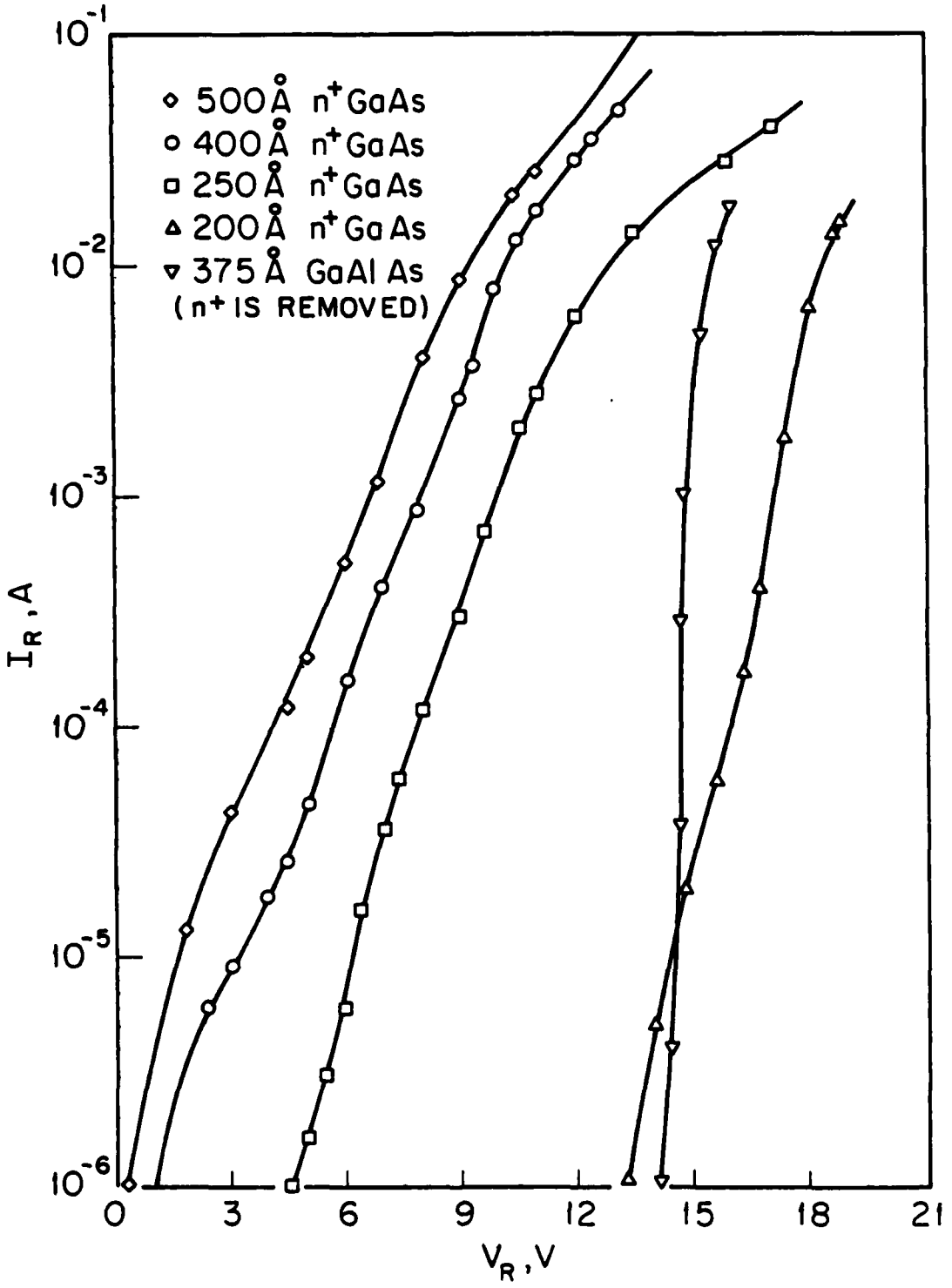
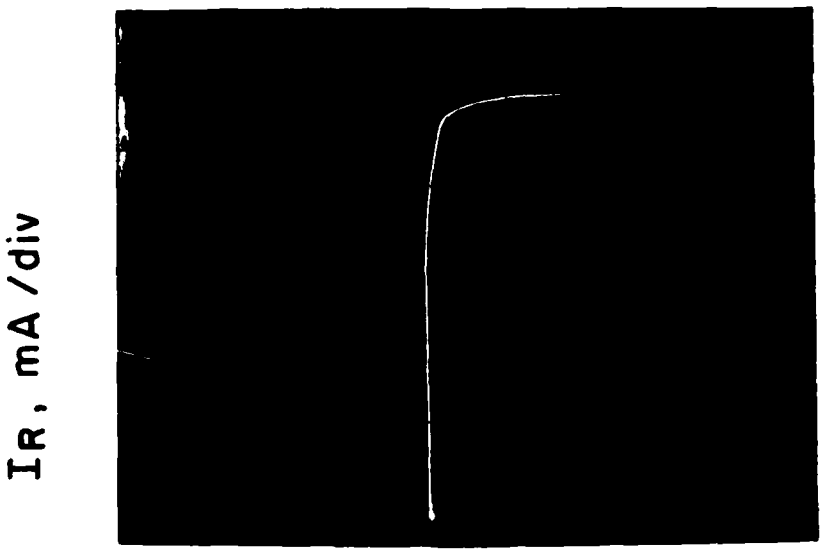


FIG. 5.12 REVERSE I-V CHARACTERISTICS OF HETEROJUNCTION DIODES.

tunnel-avalanche breakdown transit-time devices. If the n^+-GaAs layer thickness is greater than 850 Å, the breakdown takes place in the n^+ region and the lightly doped drift region is not depleted. For a high-low (n^+-n) structure, such as shown in Table 5.1, the n^+-layer thickness should be controlled to 600 to 750 Å for the proper operation of the transit-time device. Figure 5.13 shows the reverse I-V characteristics of 850 and 500 Å heterojunction diodes on the curve tracer.

5.5.2 The Capacitance-Voltage (C-V) Characteristics of the Heterojunction Diodes. The C-V characteristics were obtained using a multiple frequency LCR meter. This measurement system gives accurate data only when the reverse current is small (i.e., 200 μA or less). Therefore, accurate measurement of the depletion capacitance can be made only for small reverse bias voltages (less than 4 V) for the diodes with predominantly tunnel breakdown characteristics. The C-V profiles of different regions are given in Figs. 5.14 and 5.15.

5.5.3 The Current-Voltage Characteristics of p^+-n^+ Heterojunction MITATT Diodes. In Section 5.5.1 the characteristics of the Schottky heterojunction (Ti/n^+n GaAs) diodes were presented. The results showed that the proper operation of transit-time punch-through diodes with mixed tunnel-avalanche breakdown characteristics can be achieved if the thickness of the n^+-GaAs layer is chosen between 600 Å and 800 Å. Thus the structure shown in Fig. 5.16a was grown on the n^+-GaAs substrate by molecular beam epitaxy (MBE). The punch-through voltage for this structure is V_{pt} = 8.5 V. The typical operating voltage for the diode is approximately $V_{op} \cong 13$ V at 200 mA bias current. The electric field profiles for the



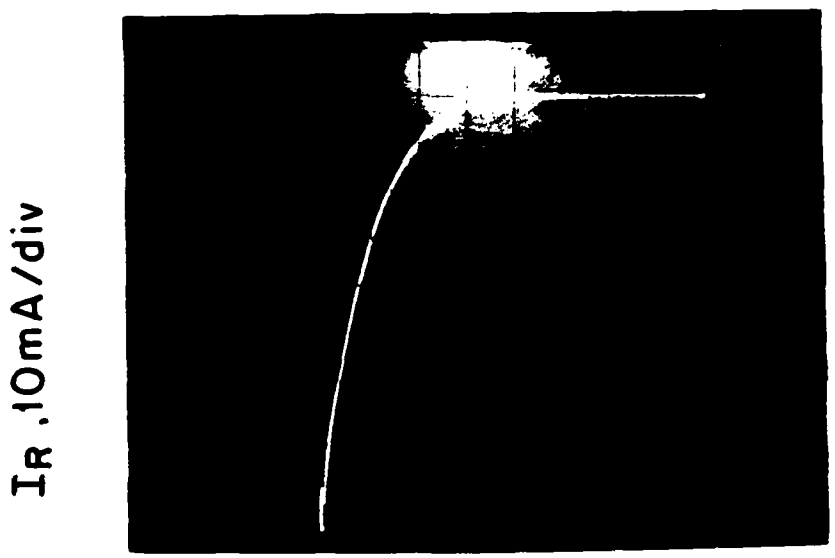


FIG. 5.13 REVERSE I-V OF 850 Å AND 500 Å HETEROJUNCTION DIODES.

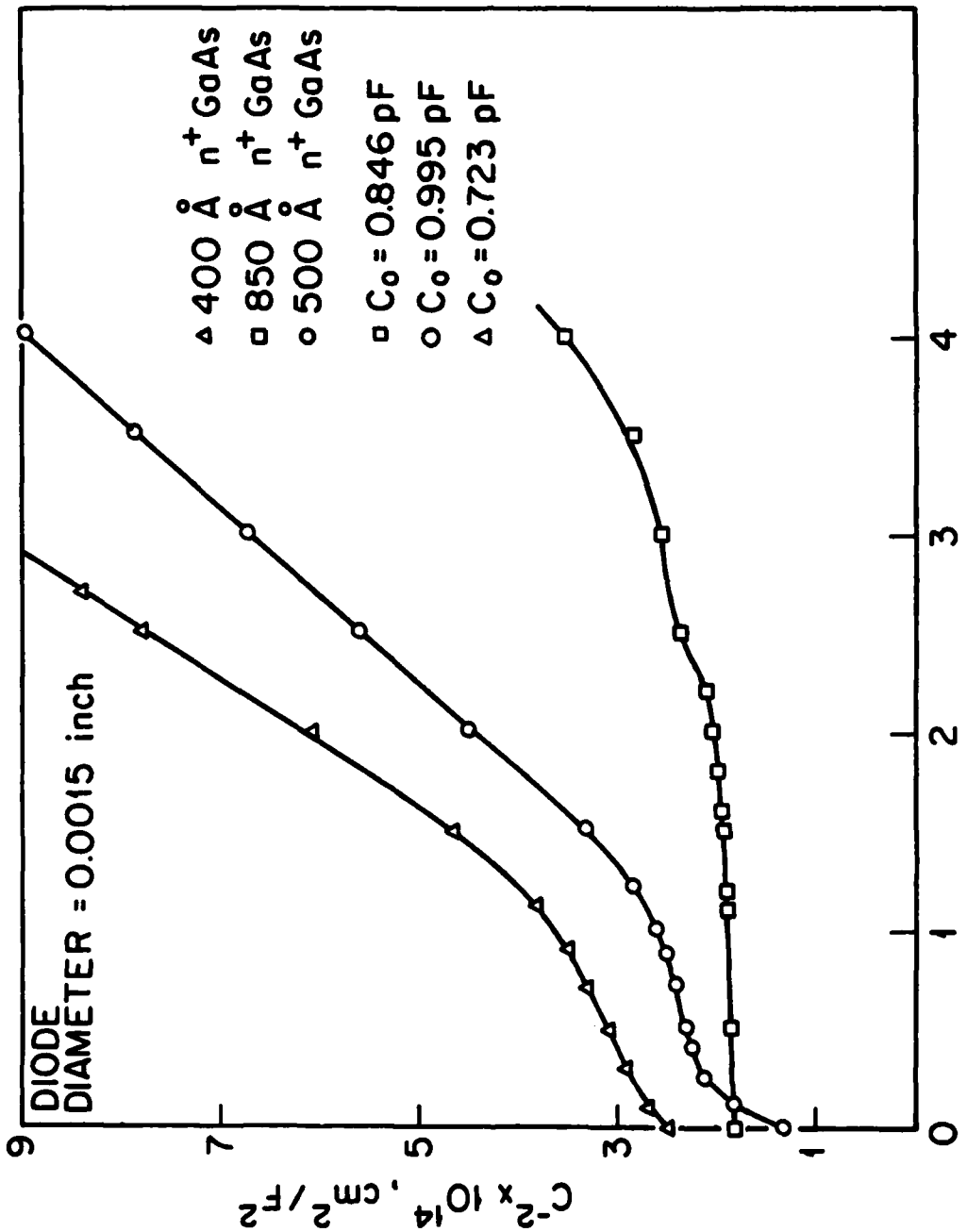


FIG. 5.14 C-V PLOT FOR HETEROJUNCTION DIODES.

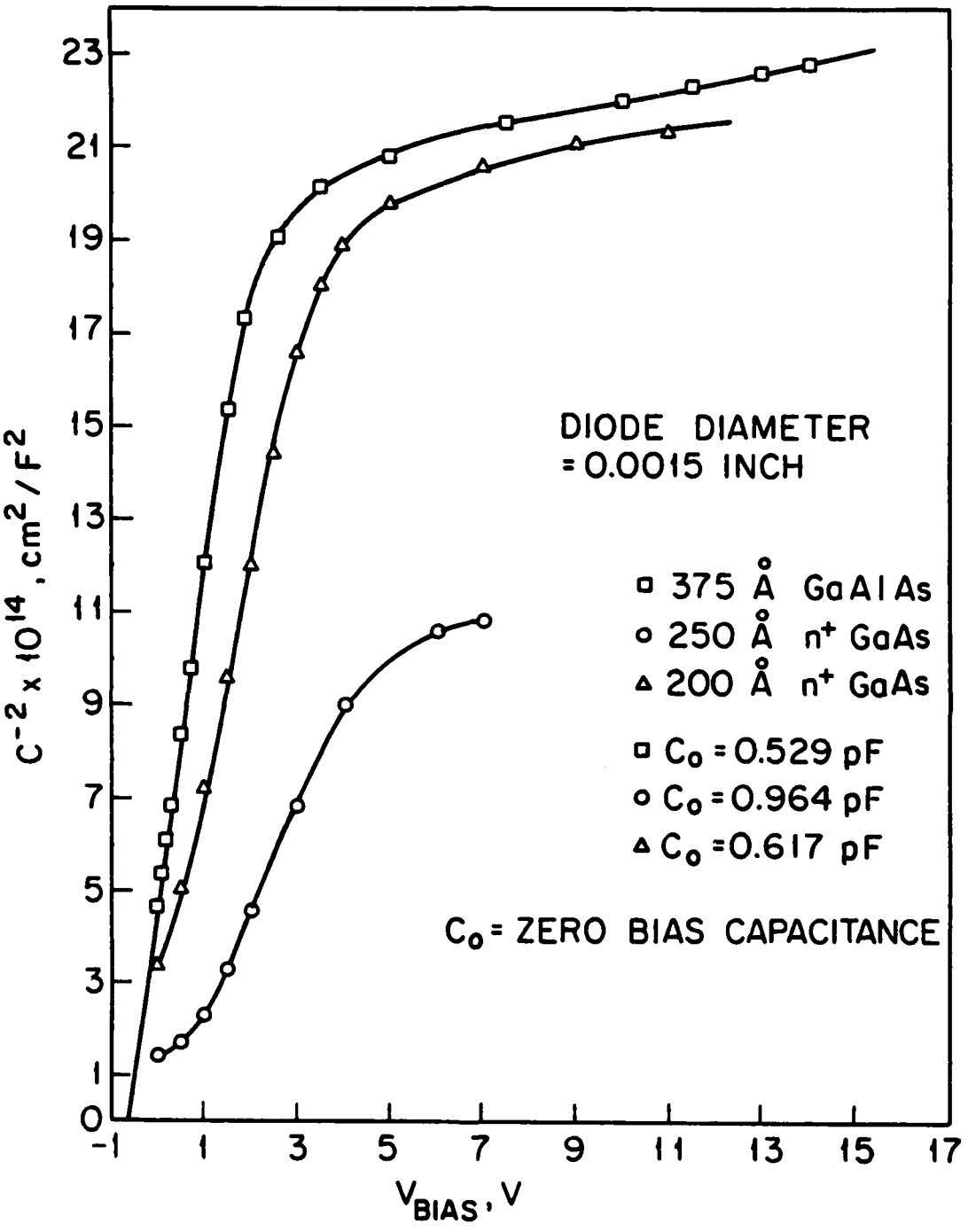


FIG 5.15 C-V PLOT FOR HETERO-JUNCTION DIODES.

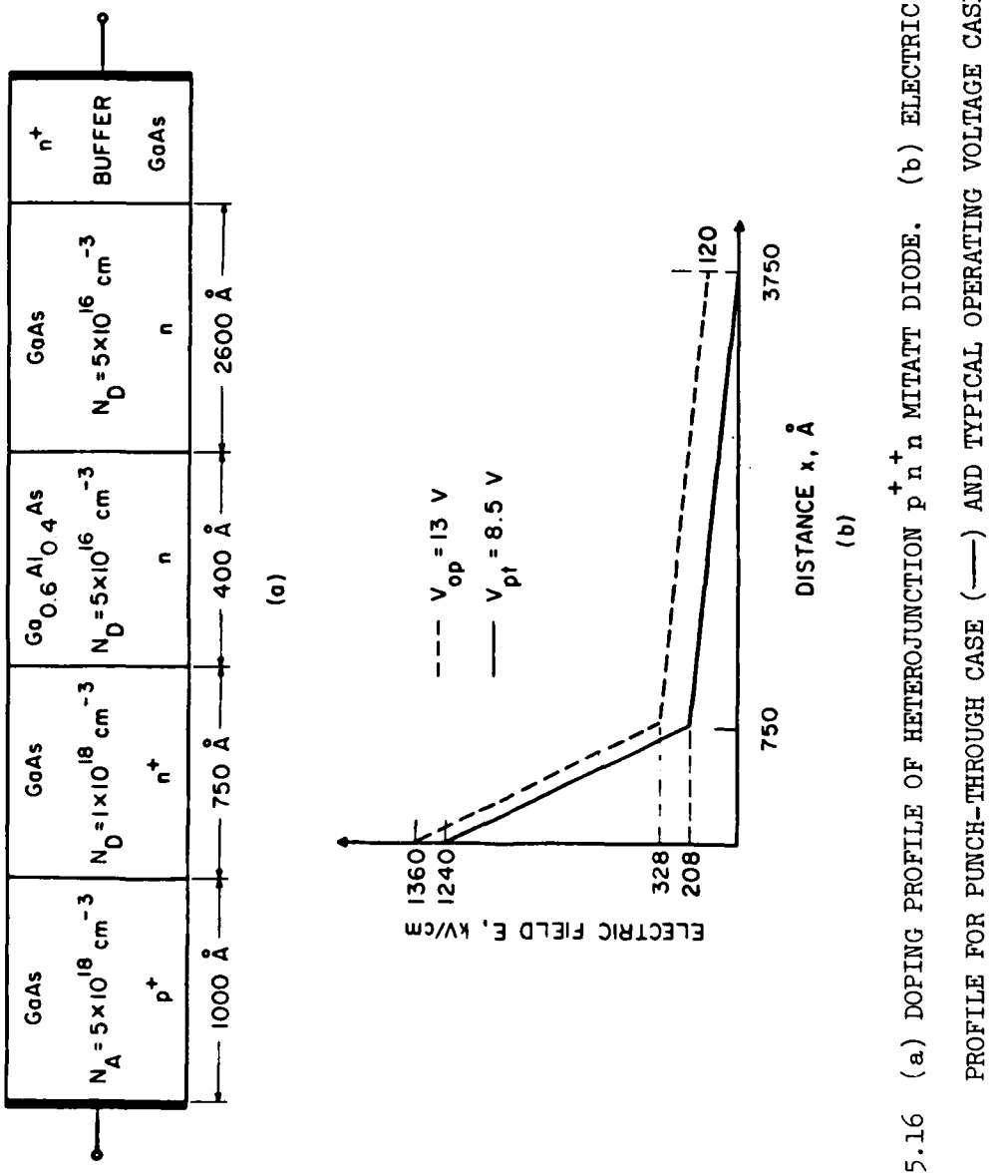


FIG. 5.16 (a) DOPING PROFILE OF HETEROJUNCTION p^+n^+ n MITATT DIODE. (b) ELECTRIC FIELD PROFILE FOR PUNCH-THROUGH CASE (——) AND TYPICAL OPERATING VOLTAGE CASE (---). THE PUNCH-THROUGH VOLTAGE IS V_{pt} = 8.5 V.

punch-through and operating values are shown in Fig. 5.16b. The maximum electric fields on the p^+-n^+ junction interface are 1.24 x 10^6 V/cm and 1.36 x 10^6 V/cm for V_{pt} = 8.5 V and V_{op} = 13 V, respectively. This electric field value ensures a significant tunneling current in the diode characteristics as seen in Figs. 5.17 and 5.18. Figure 5.18 is the semilogarithmic graph of the I-V characteristic that reveals that the breakdown mechanism changes from tunneling to avalanche for the reverse bias voltage of $V_R \cong 8$ V. Similar I-V characteristics were also reported by Nishizawa et al.[9] Figure 5.19 shows the doping profile around the p^+n^+n junction interface.

5.6 Packaging of Millimeter-Wave IMPATT and MITATT Diodes

Since the package acts as part of the oscillator circuit in millimeter-wave IMPATT and MITATT diode oscillators, it is desirable to have low parasitic package elements for better impedance matching between the circuit and the diode. Initially, ceramic commercial packages were used for the device packaging. Difficulties working with this package and large lead inductances and package parasitic capacitances yielded poor RF performance. For this reason, quartz standoffs were fabricated for packaging of millimeter-wave diodes.

Quartz is very fragile which requires extreme care during processing. Cleaning procedures before metallization are very important since poor surface cleaning leads to metal flaking or liftoff. Previous attempts to make quartz standoffs have shown that during sawing of the quartz with a wafer saw to the desired size the plated gold metal lifts off due to mechanical stress. To eliminate this problem the following process was used:

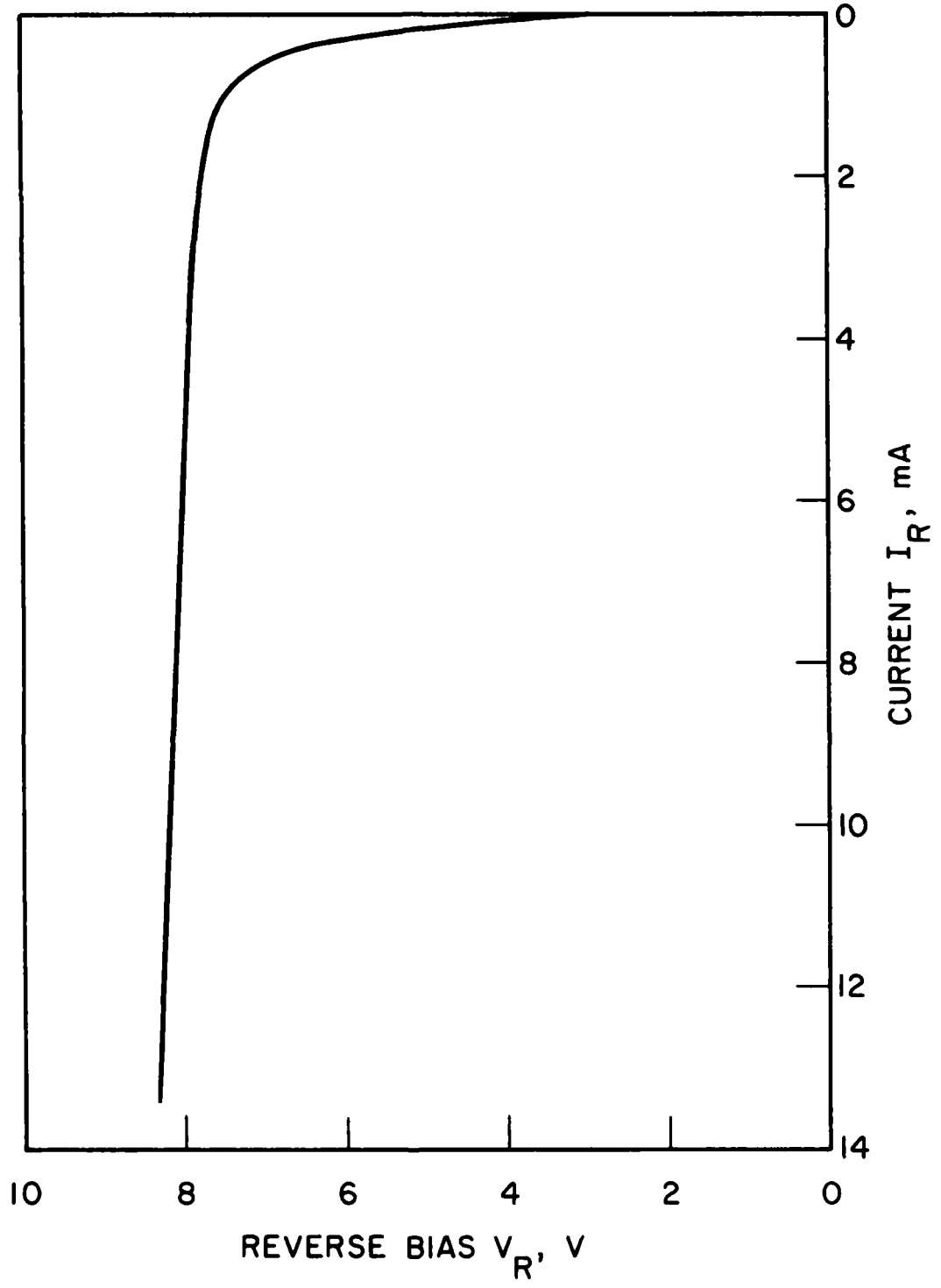


FIG. 5.17 REVERSE BIAS CHARACTERISTICS OF HETEROJUNCTION p^+n^+n MITATT DIODE. DIAMETER OF THE DIODE IS 20 μm.

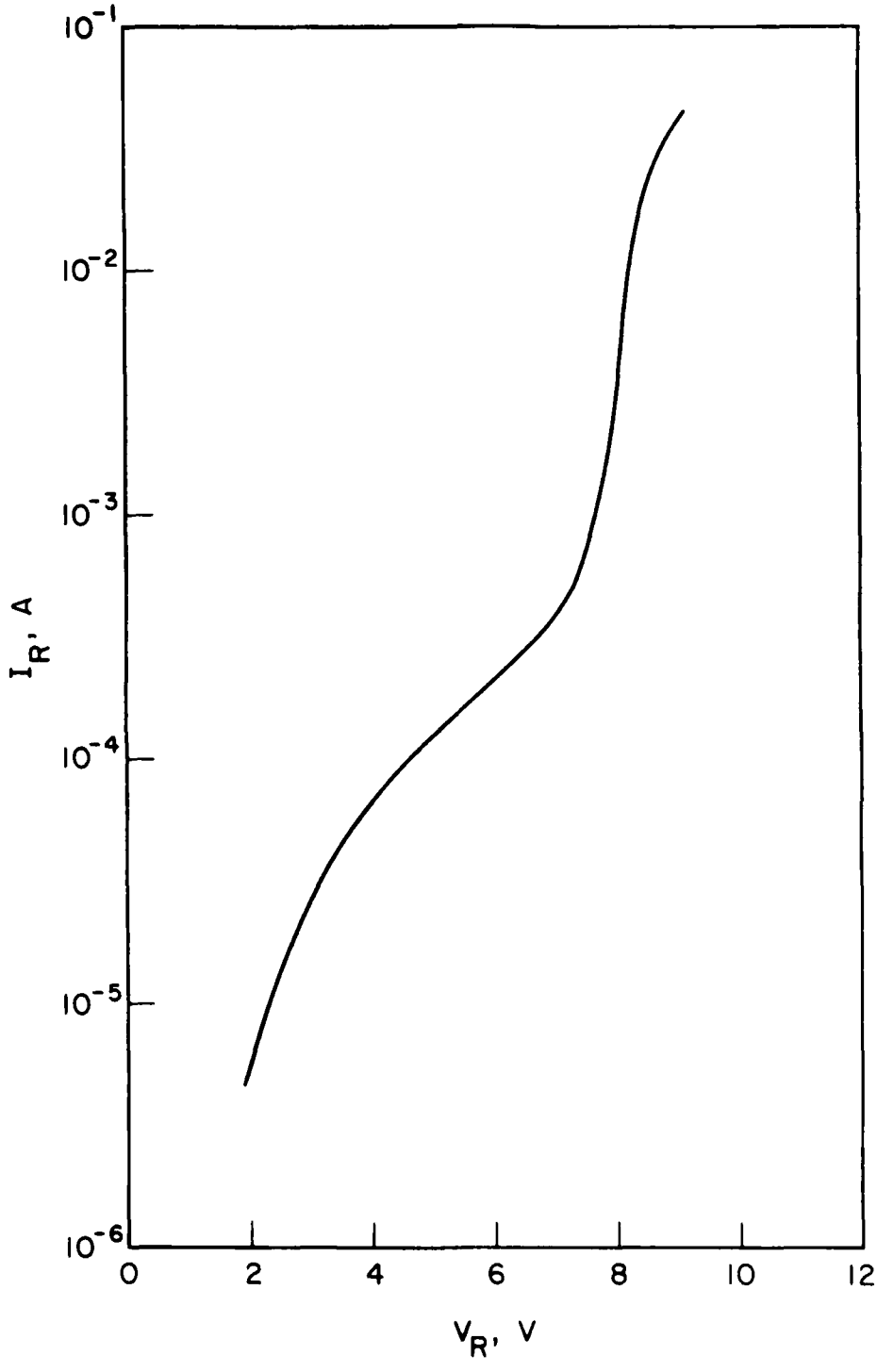


FIG. 5.18 REVERSE BIAS CHARACTERISTICS OF HETEROJUNCTION p^+-n^+ 20-μm DIAMETER DIODE ON SEMILOGARITHMIC GRAPH.

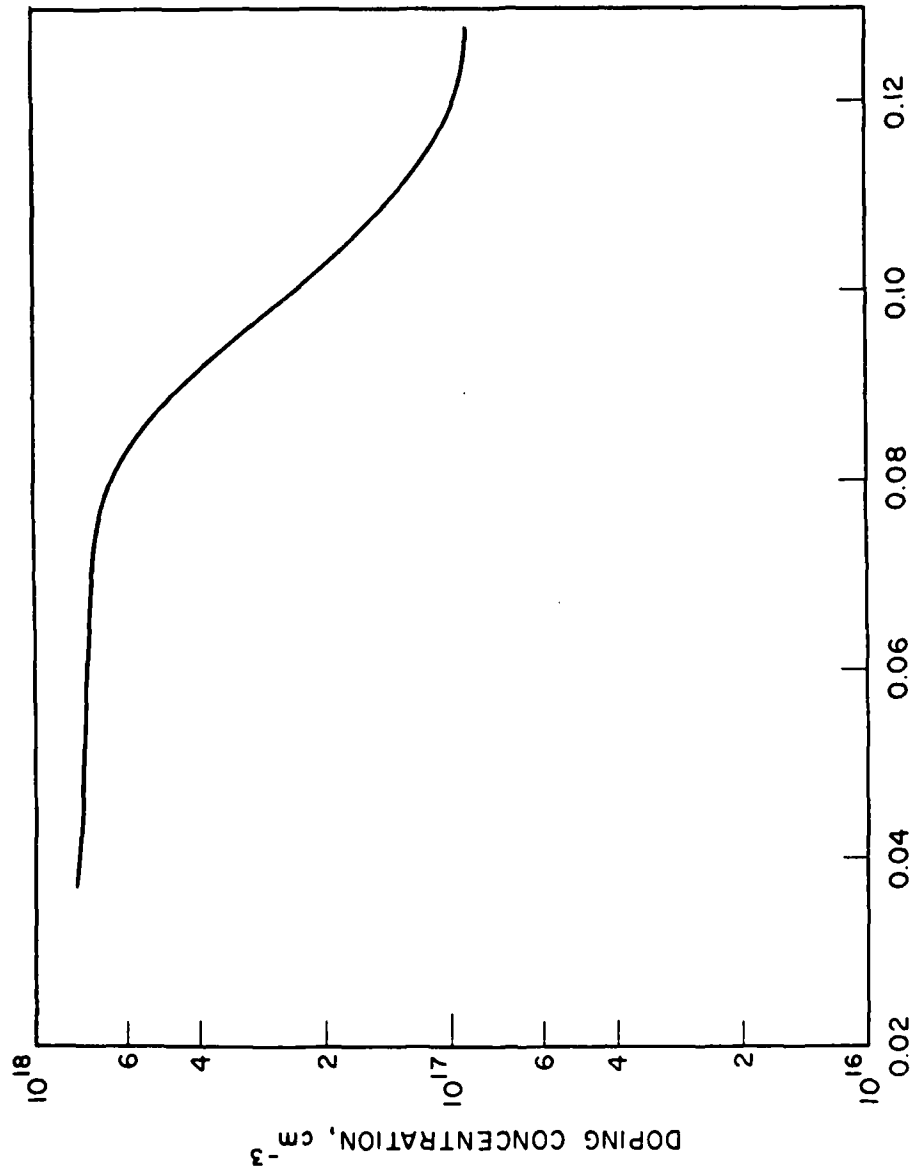


FIG. 5.19 DOPING PROFILE OF HETEROJUNCTION p^+n^+n DIODE NEAR THE INTERFACE.

1. Cr (100 Å) and Au (1000 Å) were evaporated on the surface after the quartz was cleaned.

2. Photoresist (AZ 1375) patterns were developed for selective gold plating on a 0.010 inch x 0.010 inch area. The distance between the plated gold patterns was 0.005 inch.

3. After plating 10 μm gold, the photoresist was removed in acetone and evaporated gold and chromium were etched using plated gold as a mask.

4. The same procedure was followed on the opposite side of the quartz surface and the photoresist patterns were aligned to the gold-plated patterns. This way both surfaces of the quartz were selectively metallized with good alignment.

5. The quartz standoffs were separated using a wafer saw with a 0.002-inch thick diamond blade.

Excellent yield and geometrical definition were obtained with this technique. No flaking and rough edges were observed, which is a common problem with other quartz standoffs. Figure 5.20 shows the dimensions of the quartz standoffs.

Most of the RF results reported in this work were obtained with double-quartz packages. In this mounting technique the quartz standoffs were mounted on both sides of the diode chip and a 0.0007-inch diameter wire was bonded to the quartz standoffs and the diode. Figure 5.21 shows a scanning electron microscope (SEM) photograph of the double-quartz-standoff package.

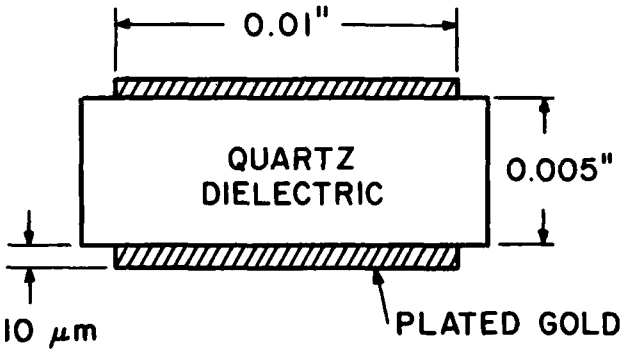


FIG. 5.20 QUARTZ STAND-OFFS FOR MILLIMETER-WAVE DIODE PACKAGING FABRICATED HERE.

FIG. 5.21 SCANNING ELECTRON MICROSCOPE (SEM) PHOTOGRAPH OF DOUBLE-QUARTZ-STANDOFF IMPATT DIODE FOR 60-GHz OPERATION. GOLD BONDING WIRE IS 0.0007-INCH DIAMETER. (140X MAGNIFICATION)

5.7 RF Measurement Results of Double-Drift 60-GHz IMPATT Diodes

In this section, the RF performance of the double-drift 60-GHz IMPATT diodes are presented. The large-signal simulation of this structure was investigated by El-Gabaly et al.[53] Their results indicate that the hybrid profile results in the same or better performance for 60- and 94-GHz IMPATTs compared to the double-Read structures. The doping profile configuration of the hybrid double-drift GaAs 60-GHz IMPATT diode is given in Fig. 5.22. The large-signal simulation results predict an operating voltage V_{op} = 21.52 V at J_{dc} = 16.0 kA/cm^2 dc current density. The measured operating voltage V_{op} = 20.1 V is somewhat lower but very close to the theoretical calculated value. The diodes were fabricated using the fabrication process described in Chapter IV with the proton-isolation technique. The room temperature breakdown voltage is V_{BD} = 15 V. The I-V characteristic of the diode was shown in Fig. 4.18.

The measurement results presented in the following were obtained in the V-band oscillator circuit shown in Fig. 5.6. The effects of various disk resonators in the oscillator performance were investigated. The diodes with varying diameters (20 to 35 μm) were also tested to see the effects of the diode area on the oscillator performance (such as power and frequency). In all the measurements a 1-μs pulse with 1 percent duty cycle was used. Figures 5.23 through 5.27 show the results obtained with different diameter diodes and disk resonators. From Figs. 5.23 through 5.25 it is seen that the oscillation frequency increases slightly as the disk resonator diameter is reduced. Similarly, for a smaller diode area the oscillator frequency increases and is shown in Fig. 5.27. All the

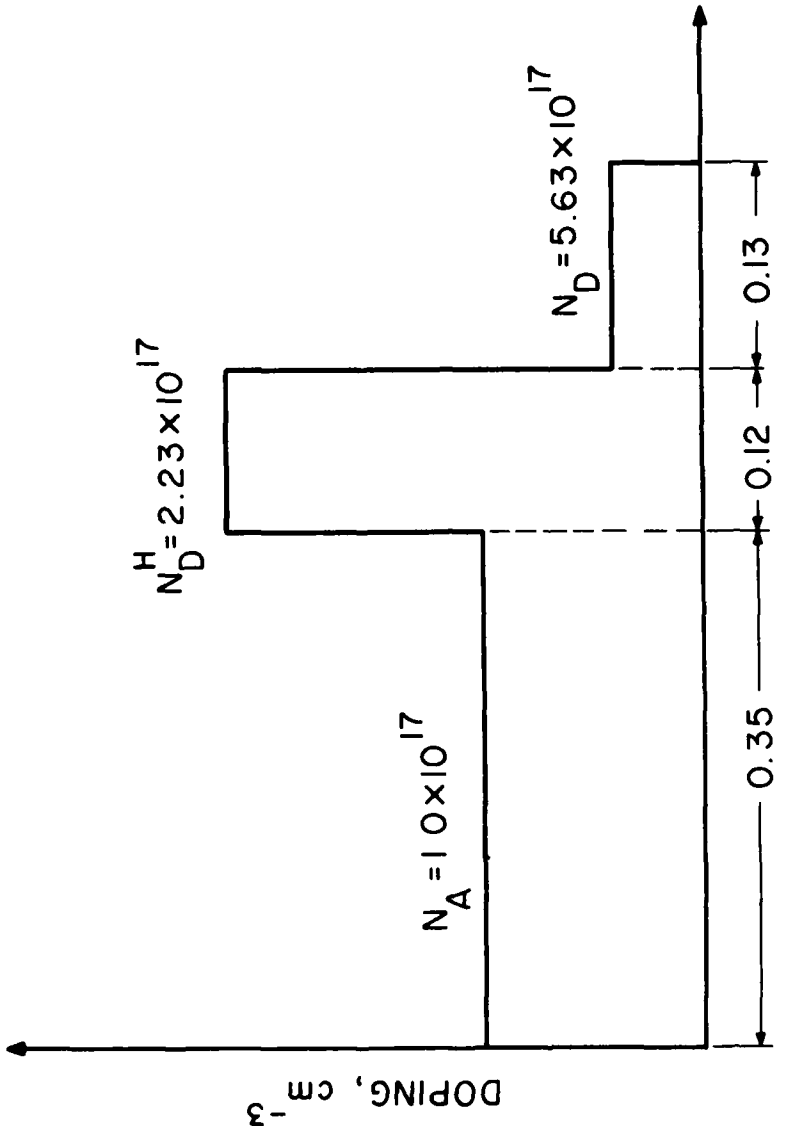


FIG. 5.22 DOPING PROFILE CONFIGURATION OF THE HYBRID DOUBLE-DRIFT GaAs 60-GHz IMPATT DIODE.

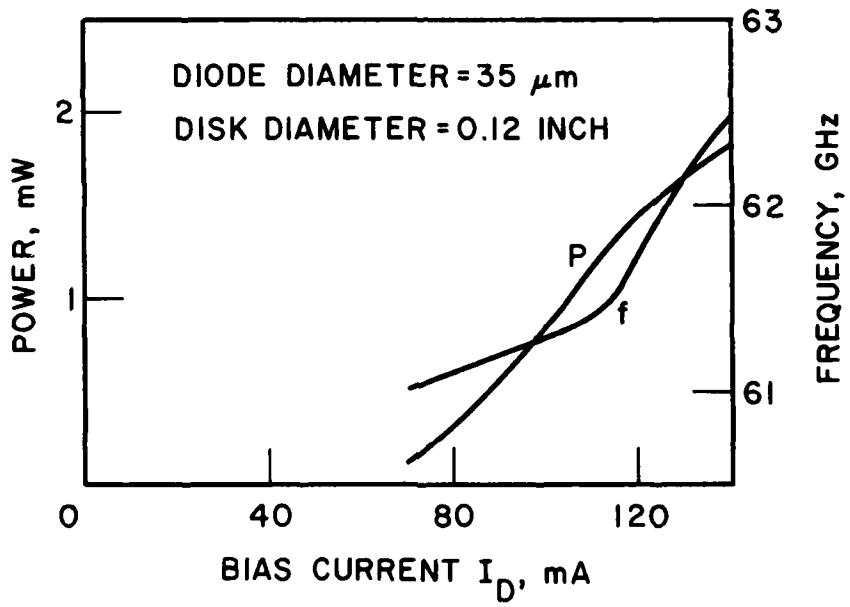


FIG. 5.23 PROTON-ISOLATED 60-GHz DOUBLE-DRIFT IMPATT DIODE WITH CERAMIC PACKAGE.

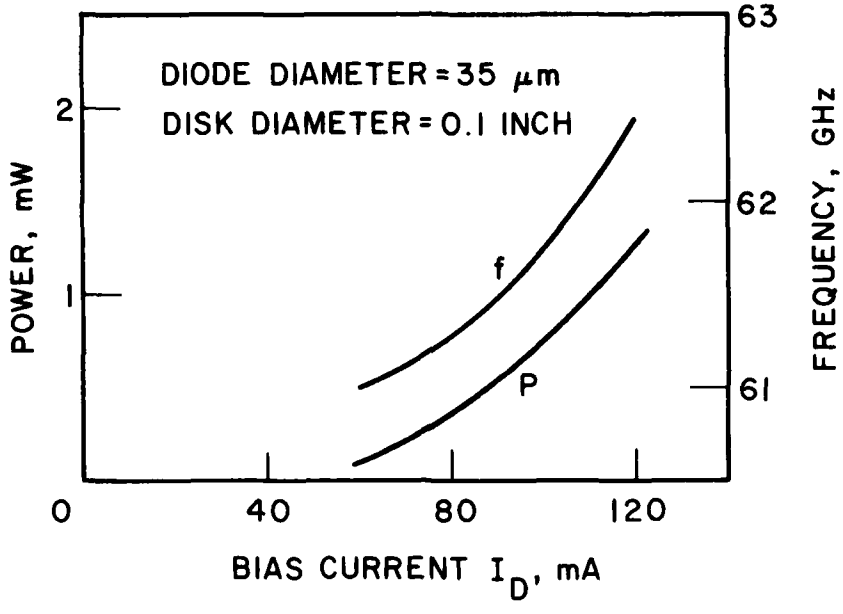


FIG. 5.24 POWER AND FREQUENCY OF 35-μm DIAMETER PROTON-ISOLATED 60-GHz DOUBLE-DRIFT IMPATT DIODE WITH CERAMIC PACKAGE.

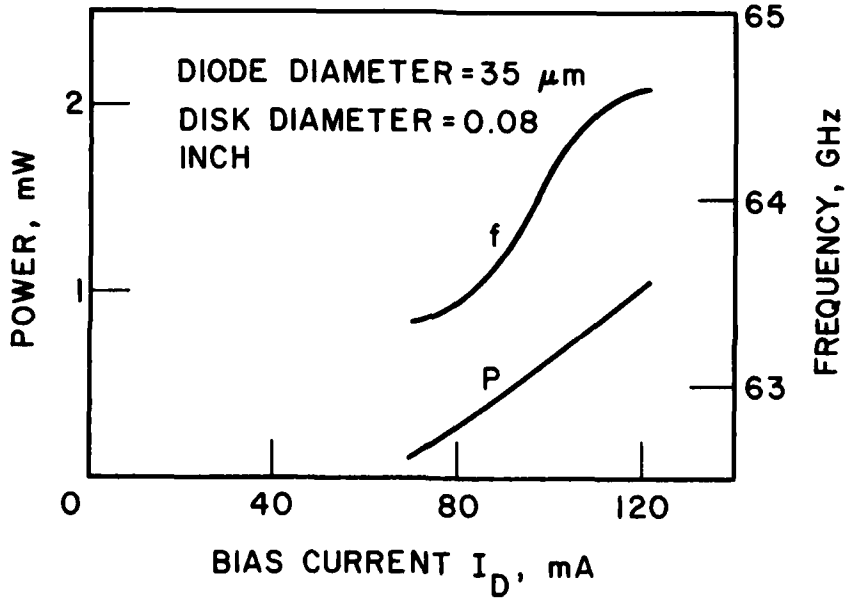


FIG. 5.25 PROTON-ISOLATED 60-GHz DOUBLE-DRIFT IMPATT DIODE WITH CERAMIC PACKAGE.

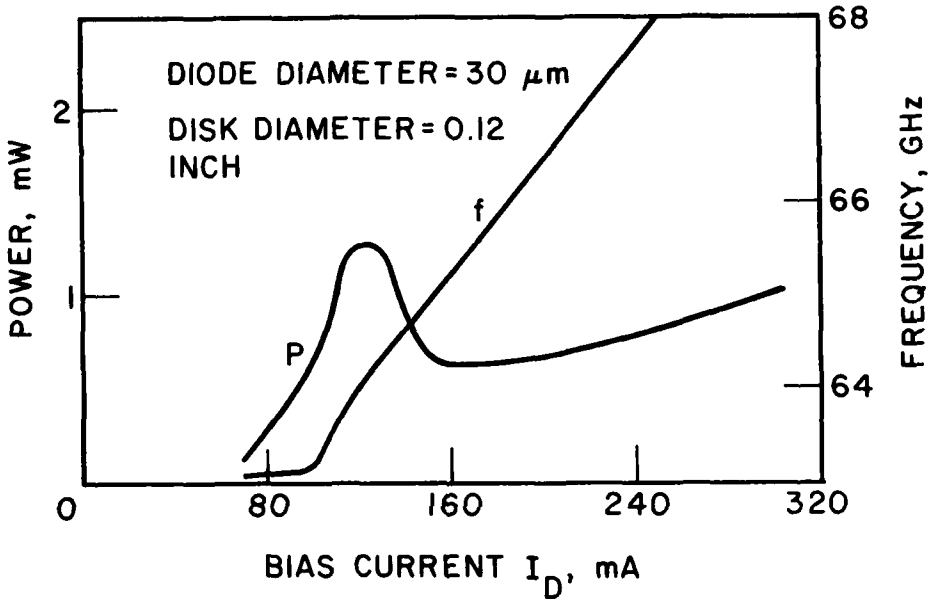


FIG. 5.26 PROTON-ISOLATED 60-GHz DOUBLE-DRIFT IMPATT DIODE WITH CERAMIC PACKAGE.

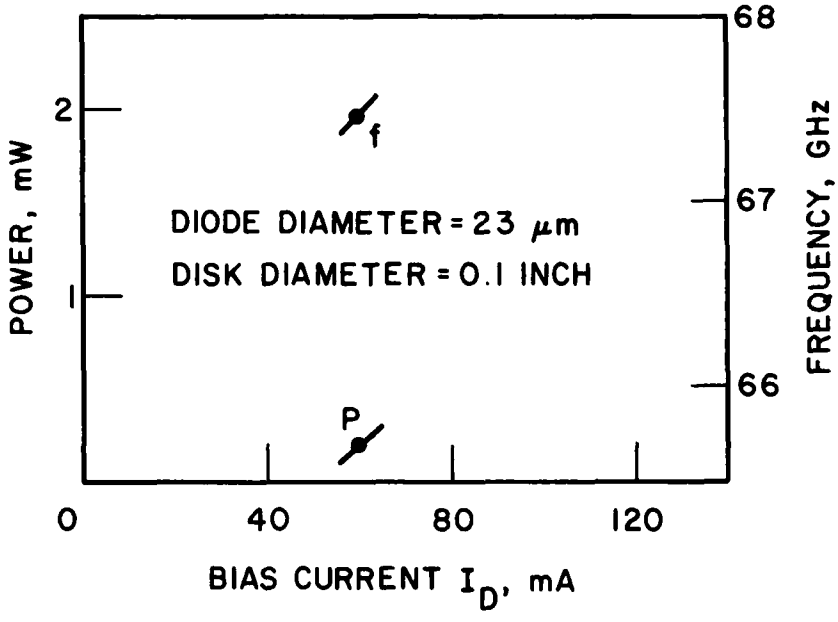
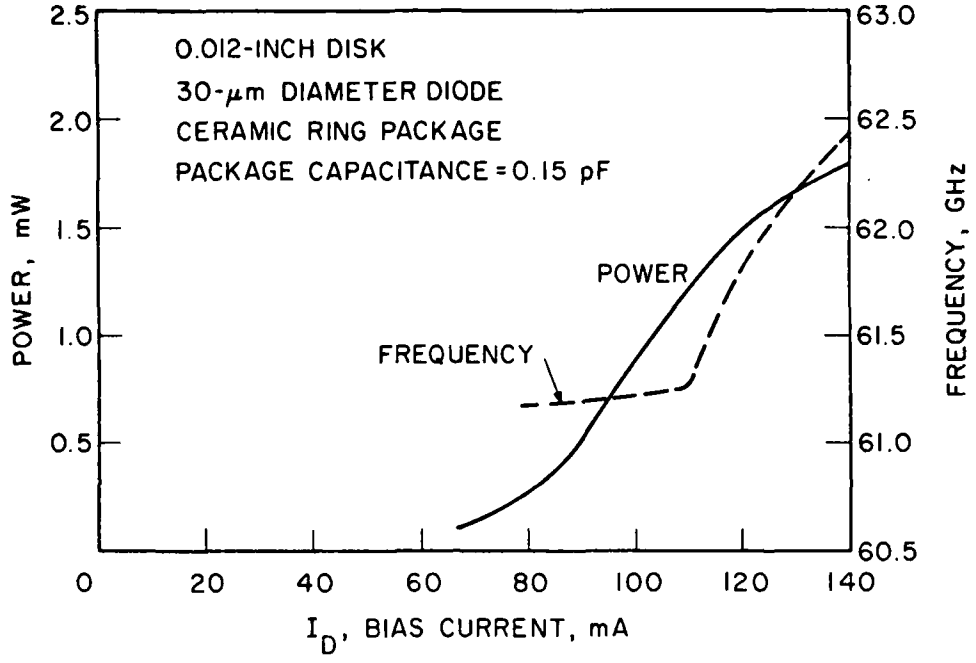


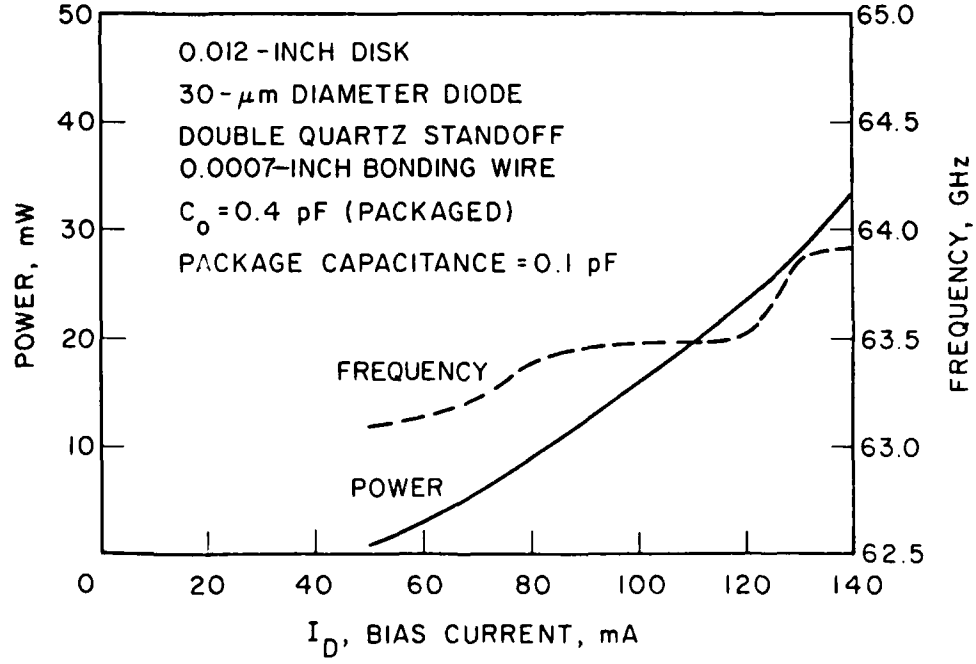
FIG. 5.27 PROTON-ISOLATED 60-GHz DOUBLE-DRIFT IMPATT DIODE WITH 23-μm DIAMETER SIZE PACKAGED WITH COMMERCIAL CERAMIC PACKAGE.

results presented in Figs. 5.23 through 5.27 were obtained with diodes packaged using ceramic packages. The RF power is very low with this packaging (typically 1 to 2 mW) technique. This is due to the large package parasitics. The results reported in the following were obtained from the diodes with the double-quartz packages. The diodes and the oscillator circuit are the same for both cases except for the packaging scheme. With the double-quartz standoff package the diodes produced approximately forty times more power compared to the ceramic package. This certainly shows the strong effect of the package on the diode RF performance.

Prior to the RF testing of the double-quartz standoff packaged diodes, the capacitance of the diode before and after packaging was measured. The measured package capacitance is 0.1 pF for the double-quartz package. The diode capacitance of the 30-μm diameter diode is C_o = 0.3 pF for zero bias, which drops to C_B = 0.2 pF before the breakdown. Similarly the zero bias capacitance of the 20-μm diameter diode is C_o = 0.2 pF, which drops to C_B = 0.12 pF before the breakdown. The performances of the hybrid double-drift 60-GHz GaAs IMPATT diodes in the new double-quartz standoff packages are shown in Figs. 5.28 through 5.30. Figure 5.28 shows comparatively the RF performance of a 30-μm diameter diode with the ceramic package and the double-quartz standoff package. Figure 5.29a shows the best performance so far obtained with these diodes. The diode burned out at a 200-mA bias current due to bias-circuit oscillation. The highest power obtained was 80 mW at 73 GHz. If the bias-circuit problem is solved, higher bias current can be used which would further increase the generated power. Figure 5.30 shows the RF performance of the 20-μm diameter



(a)



(b)

FIG. 5.28 DOUBLE-DRIFT 60-GHz IMPATT DIODE RF PERFORMANCE WITH (a) THE CERAMIC PACKAGE AND (b) THE DOUBLE-QUARTZ STANDOFF PACKAGE.

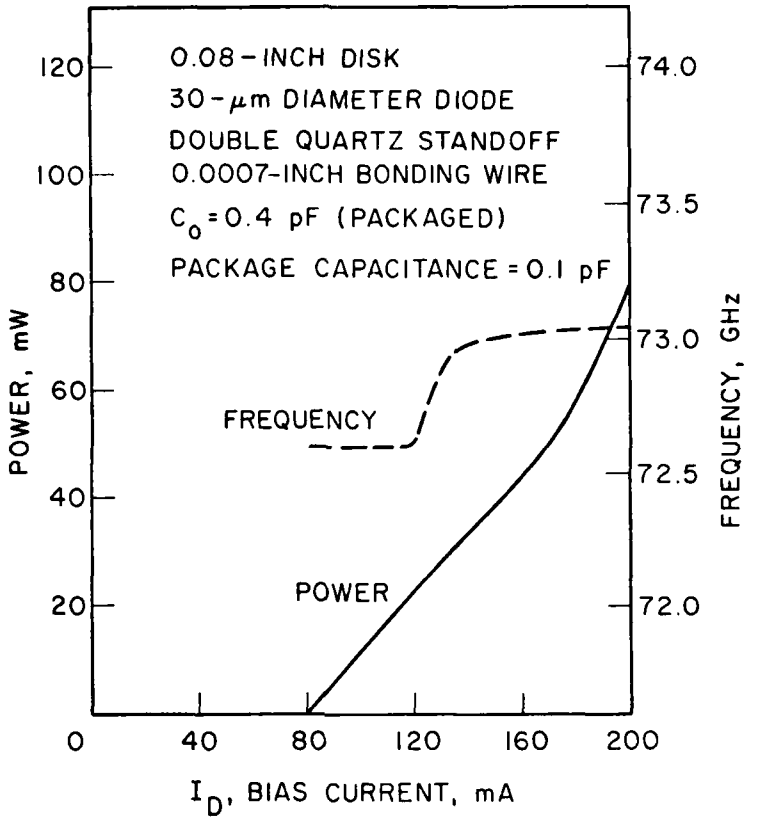


FIG. 5.29 DOUBLE-DRIFT PROTON-ISOLATED 60-GHz IMPATT DIODE RF PERFORMANCE. (a) 30-μm DIAMETER DIODE AND (b) 20-μm DIAMETER DIODE.

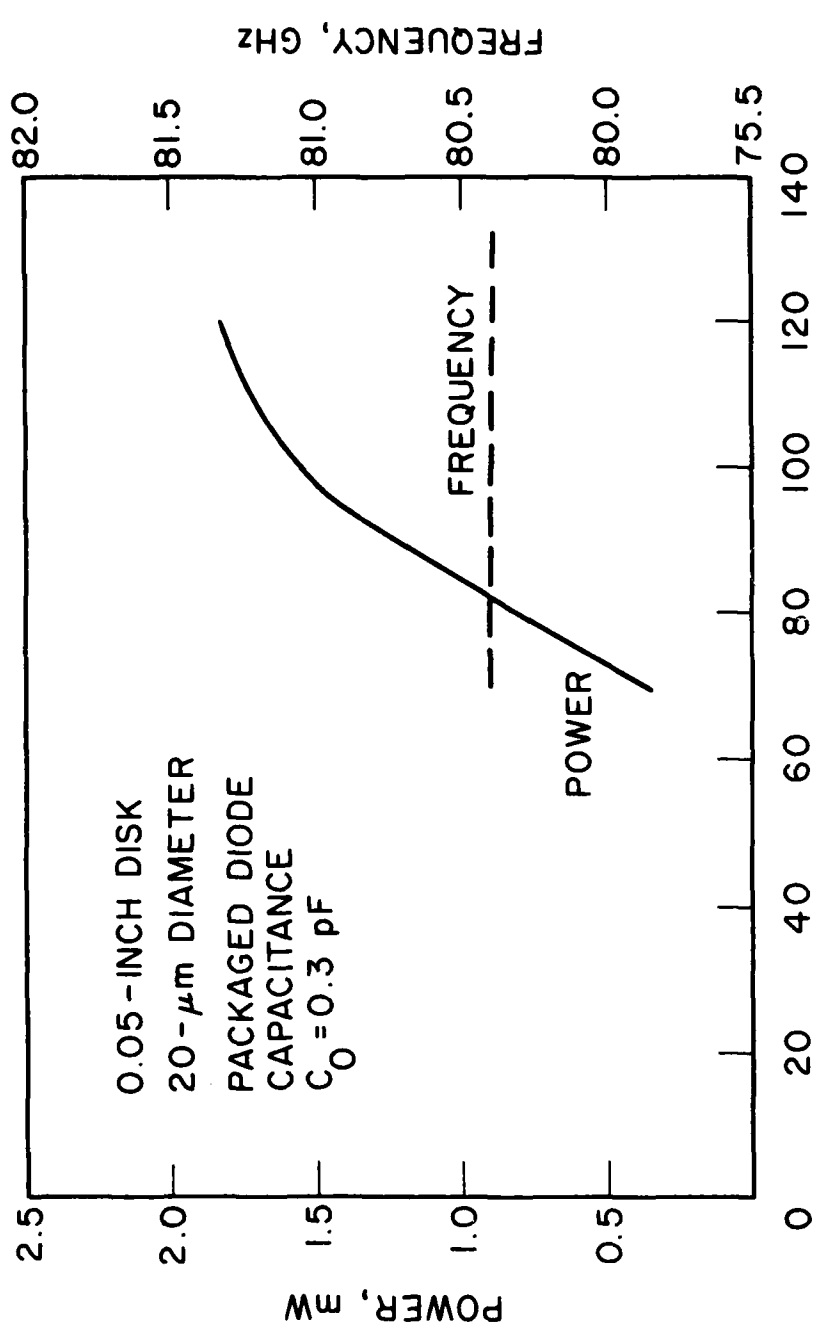


FIG. 5.30 DOUBLE-DRIFT 60-GHz IMPATT DIODE RF PERFORMANCE IN THE W-BAND (94 GHz) CIRCUIT. THE DOUBLE-QUARTZ STANDOFF PACKAGE WAS USED.

diode in the W-band (94 GHz) oscillator circuit. At 80.75 GHz, 1.8 mW was obtained.

5.8 RF Measurement Results of Heterojunction p^+n^+n MITATT Diodes

In this section, the RF performance of the heterojunction p^+n^+n MITATT diodes is presented. The doping profile and the I-V characteristics of the heterojunction MITATT diodes were given in the previous sections. The results presented in Figs. 5.31 and 5.32 were obtained in the V-band oscillator circuit. The diodes worked well with the 0.08-inch diameter resonators. As seen in Fig. 5.32, the oscillation frequency increases for the smaller area diode (20 μm diameter). Comparing the RF performance of the heterojunction MITATT diodes to the double-drift GaAs IMPATT diodes, the dc-to-RF power conversion efficiencies are very close (1.9 percent for the double-drift IMPATT and 1.46 percent for the heterojunction MITATT diodes). The capacitance of the heterojunction MITATT diode is 1.6 times larger than the double-drift IMPATT diode for the equal diode area since the depletion-region length is shorter for the single-drift diodes compared to the double-drift diodes. When this factor is taken into account the RF performance of the heterojunction MITATT diode is comparable to the double-drift GaAs IMPATT diode. Adlerstein and Chu[43] obtained a dc-to-RF power conversion efficiency of 12 percent from a similar double-Read doping profile at 60 GHz. The circuit used in this work had several problems. The most serious limitation was that the bias-circuit oscillation was observed at J_{dc} = 16 kA/cm^2 current density. This limits the dc bias to 3 to 4 W. Typical published dc input powers for the GaAs IMPATT diodes are

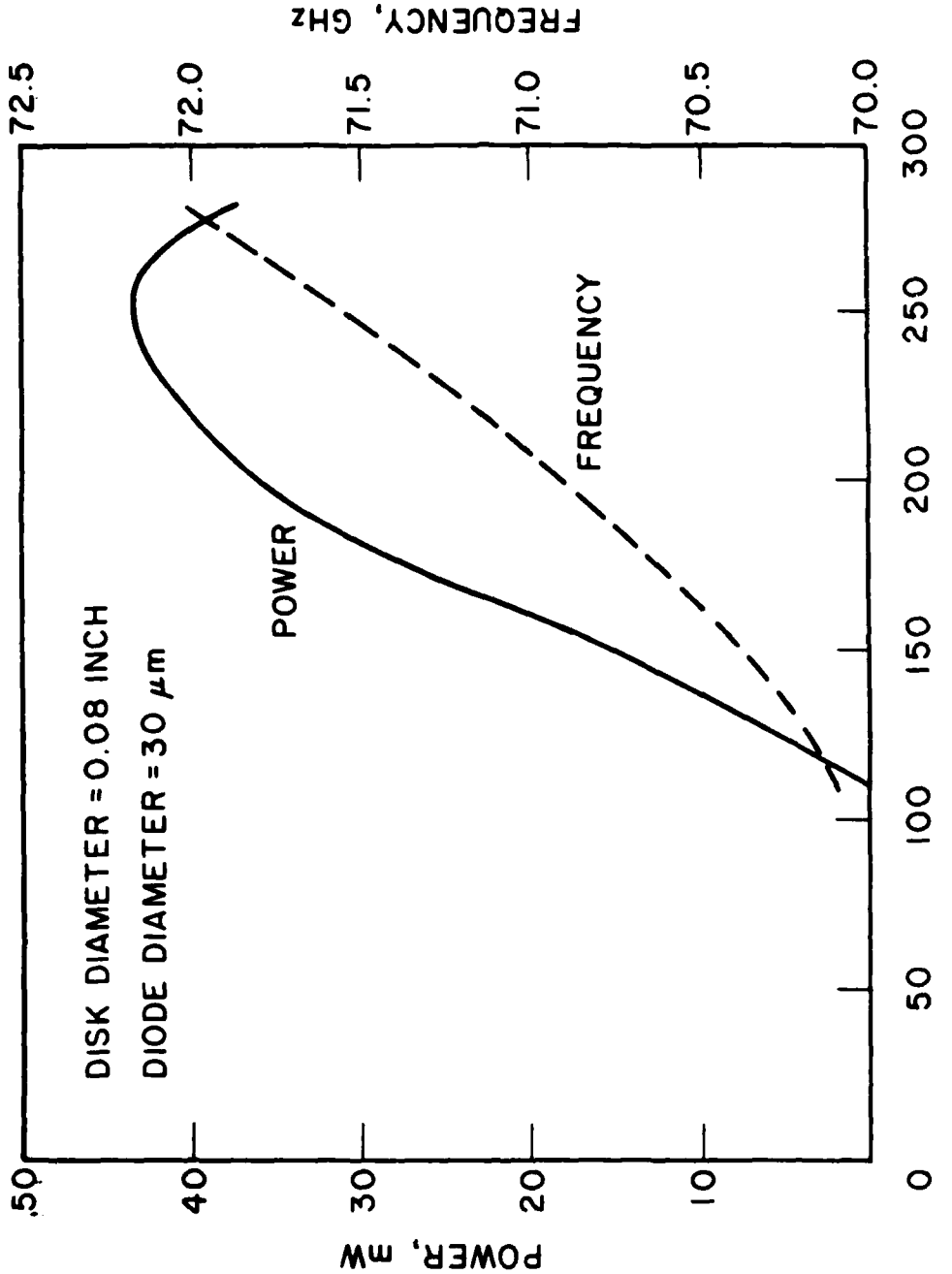


FIG. 5.31 $p^+ n n^+$ HETEROJUNCTION MITATT DIODE RF PERFORMANCE.

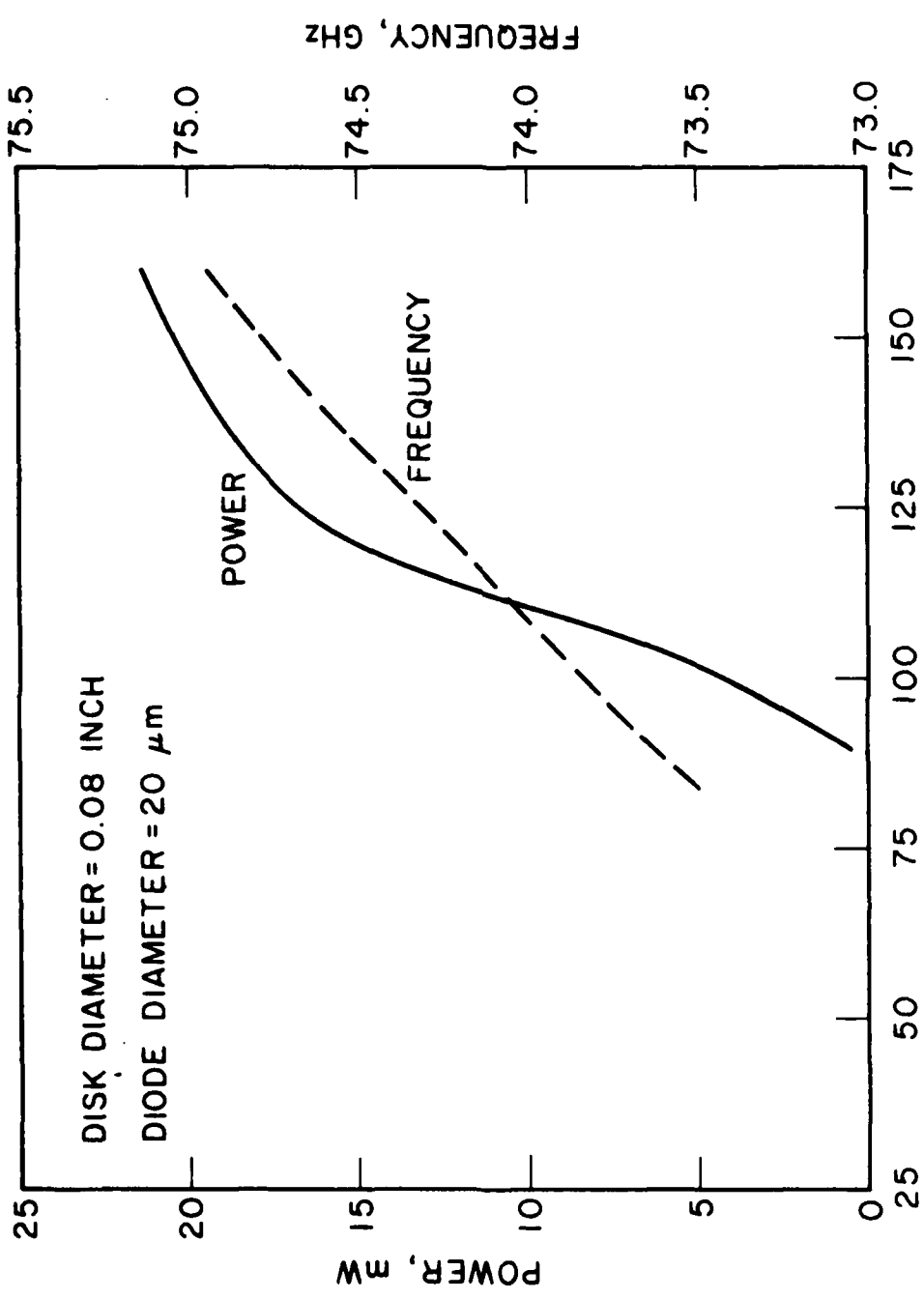


FIG. 5.32 p^+nn^+ HETEROJUNCTION MTATT DIODE RF PERFORMANCE.

8 to 12 W for the reported high-efficiency and high RF power performance. With improved circuit design and packaging, the results obtained in this work can be improved further and much better performance can be obtained. The most important result obtained in this work is that comparable RF performance was obtained with the heterojunction MITATT diode as compared to the double-drift GaAs IMPATT diode. The generation region length for the heterojunction MITATT diode is very short (less than 700 Å), as can be seen from the electric field profile in Fig. 5.16. This suggests that the heterojunction MITATT diode would have applications in the upper millimeter-wave frequencies (100 to 300 GHz) with anticipated low noise performance.

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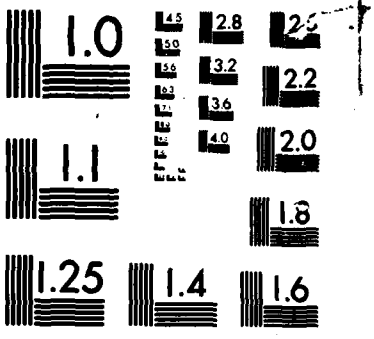
1.0
1.1
1.25
1.4
1.6
1.8
2.0
2.2
2.8
3.2
3.6
4.0

CHAPTER VI. CONCLUSIONS AND SUGGESTIONS FOR FUTURE WORK

6.1 Conclusions

The objective of this study was to investigate the performance of heterojunction MITATT diodes as low-noise power sources at millimeter wavelengths. Both theoretical and experimental investigations were carried out to achieve this objective.

In Chapter II analytical models of dc and small-signal characteristics of heterojunction Read-type diode structures were presented that incorporate both tunneling and avalanche mechanisms. The small-signal equivalent circuit was developed for both the generation region and the drift region. An approximate large-signal analysis was developed to investigate the power and efficiency of heterojunction transit-time devices.

In Chapter III various processes used in the fabrication of millimeter-wave GaAs IMPATT and heterojunction GaAs-$Ga_{0.6}Al_{0.4}As$ MITATT diodes were presented. Ohmic and Schottky contacts to GaAs were characterized and their quality, investigated. Since the fabrication of millimeter-wave two-terminal devices involves at least one or more chemical etching processes, the characteristics of the chemical etchants used in this work were discussed in detail. Finally, the proton bombardment developed during this work and the annealing characteristics of the proton bombarded layers were presented.

In Chapter IV the fabrication processes developed for millimeter-wave GaAs IMPATT and heterojunction MITATT diodes were

given in detail. The active layer thicknesses are reduced for millimeter-wave diodes due to the short transit time at these frequencies. The diode area is also reduced to maintain reasonable impedance levels. For these reasons, the material preparation, fabrication process, and packaging of these diodes become challenging technical problems. Various fabrication processes developed to overcome these problems were studied comparatively and their relative advantages and disadvantages were discussed. Finally, "the integral packaging" of these devices using a polyamide dielectric layer as a support and the process steps for the integral package were presented.

In Chapter V the waveguide circuits for the millimeter-wave two-terminal devices and the dc and RF characteristics of the diodes fabricated during this work were presented. A brief overview of the commonly used millimeter-wave circuits was given in the beginning of the chapter. A disk resonator circuit employing a radial choke in the bias port was used in this work. The cross section of the V-band (60 GHz) and the W-band (94 GHz) oscillator circuits were presented in Figs. 5.4 and 5.5 showing the important dimensions in the circuit. The measurement system used in the RF characterization of the diodes was given which includes an E-H tuner, a variable (0 to 50 dB) attenuator, a frequency meter, and a power meter. The electrical characteristics (I-V and C-V) of the heterojunction MITATT diodes and the double-drift hybrid GaAs IMPATT diodes were given in a subsequent section. The results of the I-V characteristics of heterojunction Schottky diodes with different n^+ layer thicknesses indicated that the proper operation of the transit-time device can

be obtained if the thickness of the n^+ layer is chosen to be in the range of 600 to 750 Å. This requires the precise control of the doping concentration and the thickness of the n^+ layer. In subsequent sections the RF performance of the double-drift hybrid IMPATT and the heterojunction MITATT diodes were presented. The effects of various disk resonators on the oscillator performance were investigated. Diodes with varying diameters (20 to 35 μm) were also tested to see the effects of the diode area on the oscillator performance. The highest RF power obtained in this work was 80 mW at 73 GHz with 1.9 percent power efficiency from the double-drift GaAs IMPATT diodes. The heterojunction MITATT diode produced 43.65 mW at 71.5 GHz with 1.46 percent power efficiency. The capacitance of the heterojunction MITATT diode was 1.6 times larger than the capacitance of the double-drift GaAs IMPATT diode. When this factor is taken into account, the RF performance of the heterojunction MITATT diode is comparable to the double-drift GaAs IMPATT diode. It is believed that the limitations on the RF output power and the power efficiency observed in this work (low RF power and low efficiency) are due to the circuit design and packaging. Bias-circuit oscillations were observed at J_{dc} = 16 kA/cm^2 current density during the testing of the double-drift GaAs IMPATT diodes. With proper circuit and device packaging the RF output power and the efficiency of the diodes can be improved.

The most important result obtained in this work is that comparable RF performance was obtained from the heterojunction MITATT diodes with strong tunneling characteristics as compared to the double-drift GaAs IMPATT diodes. The heterojunction MITATT diodes are expected to perform well in the upper millimeter-wave

frequencies (100 to 300 GHz) since the generation region length is very short (less than 700 Å). The strong tunneling characteristics observed in these diodes should result in low noise in the oscillator characteristics.

6.2 Suggestions for Further Study

This work demonstrated for the first time millimeter-wave frequency oscillations at 70 to 73 GHz from heterojunction MITATT diodes with strong tunneling characteristics. The power levels obtained are the best ever reported for a heterojunction device. Along with the heterojunction MITATT diodes, double-drift GaAs IMPATT diodes were also fabricated and their performance was compared. Additional topics that need further exploration are given as follows:

1. Theoretical models for the calculation of the dc and large-signal RF performance of the heterojunction mixed tunnel-avalanche transit-time diodes at millimeter-wave frequencies. This is necessary for the optimum design of the diodes.

2. More experimental work is needed to investigate the effects of various parameters on the diode RF performance, such as the doping concentration (5×10^{17} to 5×10^{18} cm^{-3}) and the thickness (500 to 1000 Å) of the n^+ region adjacent to the Schottky or p-n junction and the Al fraction in GaAlAs.

3. Extension of this work into the upper millimeter-wave frequencies (100 to 300 GHz) and submillimeter-wave frequencies.

4. Measurement of the noise performance of heterojunction MITATT diodes and its variation with weak to strong tunneling characteristics.

5. Theoretical and experimental millimeter-wave circuit studies. These would include alternative circuit designs at millimeter-wave frequencies using microstrip and fin lines.

6. Monolithic integration of the MITATT and IMPATT diodes into the expanding area of monolithic microwave integrated circuits (MMICs) and monolithic millimeter-wave integrated circuits (M^3ICs). This would increase the performance and capabilities of the M^3ICs since most high-performance GaAs MESFETs and HEMTs have limitations at millimeter-wave frequencies at 60 GHz and above.

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None

Publications

Blakey, P. A., East, J. R., Elta, M. E. and Haddad, G. I., "Implications of Velocity Overshoot in Heterojunction Transit-Time Diodes," Electronics Letters, vol. 19, No. 14, pp. 510-512, 7 July 1983.

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