AD-A169 605 A NEW ION IMPLANT MONITOR ELECTRICAL TEST STRUCTURE(U) 1/1
STANFORD UNIV CA DEPT OF ELECTRICAL ENGINEERING
A MCCARTHY 1986

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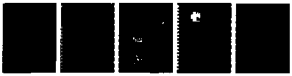

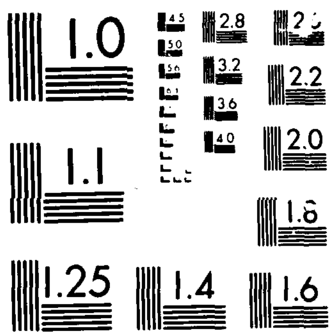
1.0
2.8
3.2
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2.0
1.1
1.8
1.25
1.4
1.6

A new Ion Implant Monitor Electrical Test Structure

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This is a student paper.

Introduction

In this paper, a new Ion Implant Monitor test structure and measurement method is reported. A direct measurement of the sheet resistance of the implanted species is employed. This monitor has the advantage of unambiguous verification of the electrical performance of the layer. The proposed method has a high spatial resolution, approximately 300um between measurements and has been shown to have resolution down to at least 7×10^{11} /cm^2. The technique does not suffer from the problem of compensation for non-infinite planes associated with wafer edges as in four point probe measurements. Voltage measurements are directly converted to sheet resistance, thus measurements may be performed rapidly.

Structure Description and preparation.

The structure is implemented on a wafer of opposite polarity to the type of implant being measured. The plane and profile view is shown in fig. 1. Only Boron implant measurements are reported in this paper. Three inch wafers of a high resistivity phosphorous doped Silicon, in the range 10-20 ohm-cm, were selected. A thermal oxide layer of 1000 Angstroms thickness was grown. 5000 Angstroms of undoped Polycrystalline Silicon was deposited to act as a blocking layer. Mask number one was used, fig. 1a, to define probe pad areas by etching openings in the Poly. A moderate energy heavy dose of Boron of 1×10^{16} /cm^2 was implanted through the oxide. Mask number two was used to define the cross-bridge areas for the second implant, fig. 1b. After a second Polysilicon etch and resist strip the wafers were ready for implantation and stored until time of use. The procedure following the second implant was standard: the wafers were annealed in an Argon ambient at 900C for thirty minutes, and the oxide was stripped. Measurements were performed using a standard parametric system and automatic wafer probe with no special probes or software.

Results

Wafers were implanted with doses in the range 7×10^{11} /cm^2-1×10^{16} /cm^2. Wafer maps of the results taken from wafers implanted with doses of 1×10^{13} /cm^2, 1×10^{12} /cm^2 and 7×10^{11} /cm^2 are shown in fig. 2, 3 and and 4 respectively. The standard deviations are 2.2, 2.2 and 2.7% respectively, which is very good for low doses. A plot of measured sheet resistance versus dose, shown in fig. 5, agrees well with previously published data.

For each dose one wafer was selected to measure data within a square die area of approximately .5cm on a side. On each wafer twenty eight sites on each of three die were measured. The die lay on a diagonal of about 60mm in length on the three inch wafer. In the case of the 1×10^{13} /cm^2 dose, the die area was approximately .25cm on a side, the number of test sites was twenty per die and the diagonal length was about 50mm. A summary of the within-chip measurements is given in Table 1. The standard deviations are very tight as expected. The initial heavy implant was also monitored. It can be seen from the table that it was multi-modal in the range 110-140 ohms/square and this does not affect the low dose measurements.

Conclusions

A new electrical ion implant monitor has been presented, and tested for measuring implant doses as low as 7×10^{11} /cm^2. The technique employs the Van der Pauw structure to measure the sheet resistance of implanted layers. It is a direct confirmation of the electrical performance of the implant. The spatial resolution is an order of magnitude greater than currently available implant monitoring systems. This permits the possibility of measuring statistics within a die area. The measurement does not require compensation for non-infinite planes at wafer edges, and no special hardware or software is required other than a standard automatic parametric system.

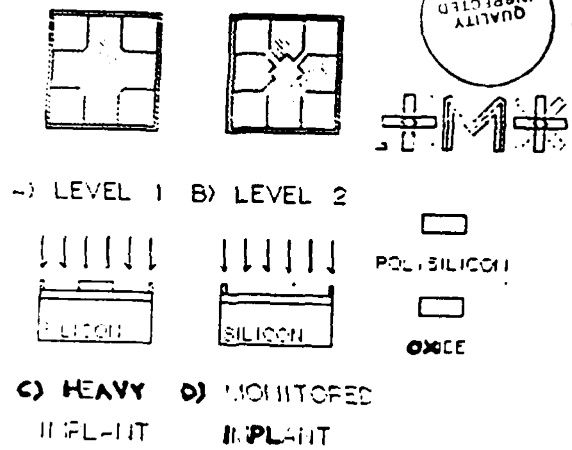

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FIGURE 1

Wafer Map
St Dev PLOT N23 Rs 1E13 STANFORD

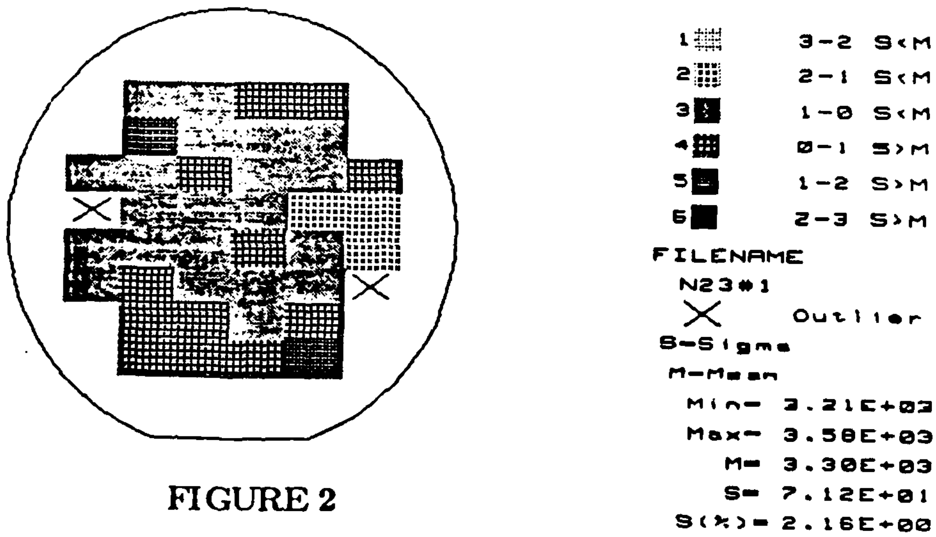

FIGURE 2

Wafer Map
St. Dev. PLOT N14 1E12 Rs STANFORD

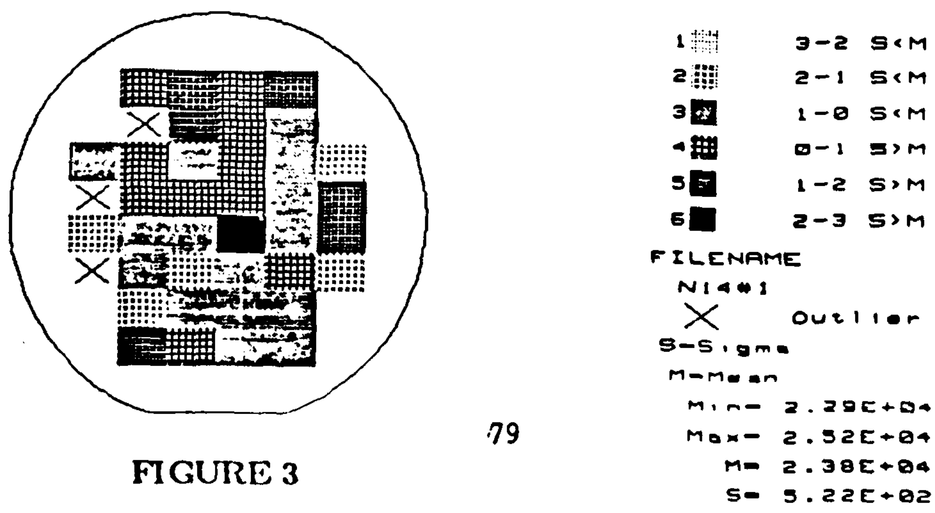

FIGURE 3

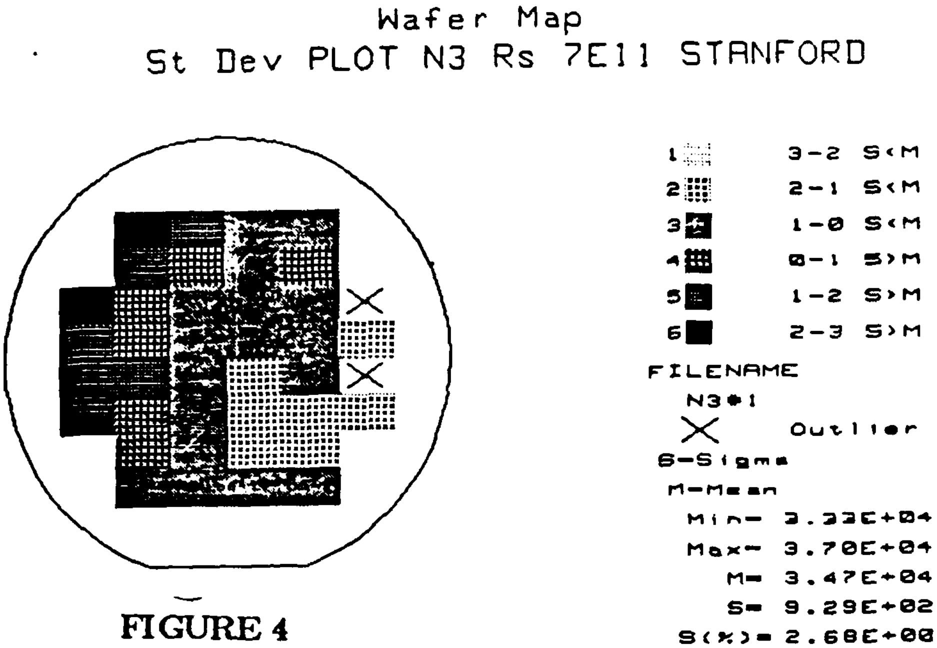

FIGURE 4

FIGURE 5 Dose versus Sheet Resistance

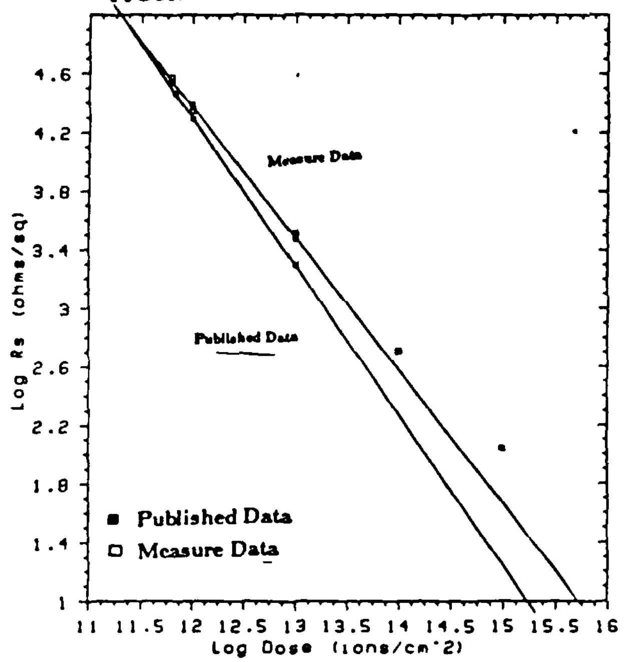

TABLE 1

Within chip measurements						
Dose	Wafer Upper Left	St. Dev.	Wafer Center	St. Dev.	Wafer Lower Right	St. Dev.
ions/cm²	Ω/□	%	Ω/□	%	Ω/□	%
1e15	126.0	10.0	115.0	5.0	114.0	3.0
	kΩ/□		kΩ/□		kΩ/□	
1e13*	3.1	1.5	3.1	0.8	3.1	0.7
1e12	28.9	1.7	27.2	1.1	27.5	0.8
7e11	42.1	1.1	40.0	1.2	40.5	1.8

* **50mm diagonal on a three inch wafer**

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