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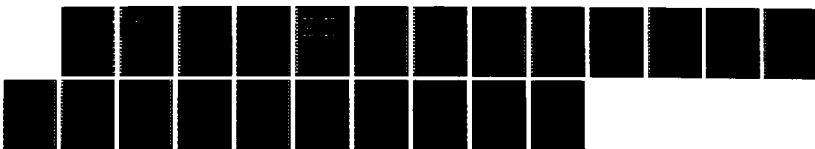
REPORT ON AN INTERLABORATORY ELECTROMIGRATION  
EXPERIMENT(U) STANFORD UNIV CA H SCHAFFT ET AL. JUN 86

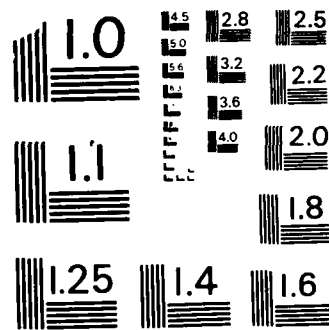
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REPORT ON AN INTERLABORATORY ELECTROMIGRATION EXPERIMENT

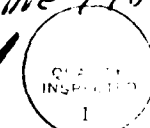
by  
Harry Schafft, Tammy Grant, and John Mandel  
National Bureau of Standards  
Gaithersburg MD 20899

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June 1986

*Attorney file*

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Electromigration is a metallization failure mechanism that is of concern for VLSI reliability. Ambiguities exist in the electromigration characterization of metallizations. These ambiguities are, in general, due to the different test structures and measurement methods used and to the incomplete reporting of the results from such characterizations.

An interlaboratory experiment has been organized to address this problem. The purpose of the experiment is to assess the reproducibility of electromigration characterizations and to establish the technical base needed to develop guidelines for the design of electromigration test structures, for methods to measure the median-time-to-failure ( $t_{50}$ ) of metallizations, and for reporting characterization measurements. Fourteen laboratories have volunteered to participate in the experiment.

A test chip, NBS-42, was designed for this experiment and is shown in Fig.1. Each quadrant of the chip has five test-line structures for electromigration stress tests and is intended to be packaged separately. Quadrants 1 through 3 have structures with straight test lines that have designed lengths of 400, 800, and 1200  $\mu\text{m}$ , respectively. The structures in quadrant 4 have 1200- $\mu\text{m}$  long test lines with right-angle turns. These different structures will allow a determination of any dependences of  $t_{50}$  on test line length and on right-angle turns.

The basic features of the electromigration test structures are illustrated in Fig. 2. This structure is a four-terminal device for making Kelvin resistance measurements. It is designed to detect open-circuit and short-circuit failures caused by electromigration. Initially, only unpassivated, single-level-metal structures will be tested for open-circuit failures. Subsequent experiments with passivated structures will be used to detect short-circuit failures between adjacent lines and between two metal levels.

NBS-42 test chips were fabricated on six three-inch wafers by sputter depositing Al 1%Si on oxidized silicon, wet etching the metallization, and annealing the metallization in forming gas for 20 minutes at 450°C. The mean sheet resistance and the mean electrical linewidth were determined to be 36.8  $\text{m}\Omega/\text{square}$  and 3.10  $\mu\text{m}$ , respectively. This was based on the results of measurements of cross bridge test structures at 10 locations on each of the six test wafers. The mean resistance of the structure with the 400- $\mu\text{m}$  test line was determined to be 5.07  $\Omega$  from a similar set of measurements. The mean metallization thickness was determined to be 0.86  $\mu\text{m}$  based on profilometer measurements at five locations on each of the wafers.

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AND SECURITY REVIEW (DASD-PA)  
DEPARTMENT OF DEFENSE

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# REPORT ON AN INTERLABORATORY ELECTROMIGRATION EXPERIMENT

by

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Electromigration is a metallization failure mechanism that is of concern for VLSI reliability. Ambiguities exist in the electromigration characterization of metallizations. These ambiguities are, in general, due to the different test structures and measurement methods used and to the incomplete reporting of the results from such characterizations.

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The ratio of the standard deviation to the parameter mean (coefficient of variation) was determined from the above measurements to estimate the uniformity of the above parameters. The test structure resistance and the metallization sheet resistance, width, and thickness were determined to be uniform to within seven percent between wafers and within three percent on a wafer. The resistance, sheet resistance, and linewidth were determined to be uniform to within one percent in a quadrant grouping of the five test structures.

Each participating laboratory was sent test parts from one wafer to avoid the effect of possible wafer-to-wafer variations of  $t_{50}$ . Every laboratory was asked to stress two sets of 20 test structures to open-circuit failure: one set to be stressed at a current density of 1.0 and the other at 2.5 MA/cm<sup>2</sup>. [n.b. M = million] These two stress levels were selected to determine if the repeatability of  $t_{50}$  measurements is affected by significant Joule heating, which occurs at the higher current density. Most of the laboratories volunteered to perform tests on packaged parts. Three volunteered to perform tests at the wafer level.

Each laboratory was instructed to use its own method to determine  $t_{50}$  for each of the two sets of test parts provided. Each laboratory was also asked to report its results with a detailed description of the method used and to provide a copy of the calculations used to obtain the results reported. To evaluate repeatability of  $t_{50}$  measurements, all  $t_{50}$  data from the participating laboratories are compared to those of the reference laboratory (NBS).

The following results will be reported:

- o An estimate of the between-laboratory repeatability of  $t_{50}$  and sigma measurements, where each laboratory uses its own measurement method but where all use equivalent test structures.
- o An estimate of the within-laboratory repeatability of  $t_{50}$  and sigma measurements using one test method and equivalent structures.
- o An estimate of the interwafer variation of  $t_{50}$  measurements for wafers from the same metallization lot.
- o The effect of Joule heating on the repeatability of  $t_{50}$  measurements.
- o The effect of test-line length on  $t_{50}$  and sigma measurements.

Acknowledgments:

Portions of this work were supported by the Defense Advanced Research Projects Agency (ARPA Order NO. 3882). Packaging and other services were provided by the MOSIS system, University of Southern California/Information Sciences Institute.

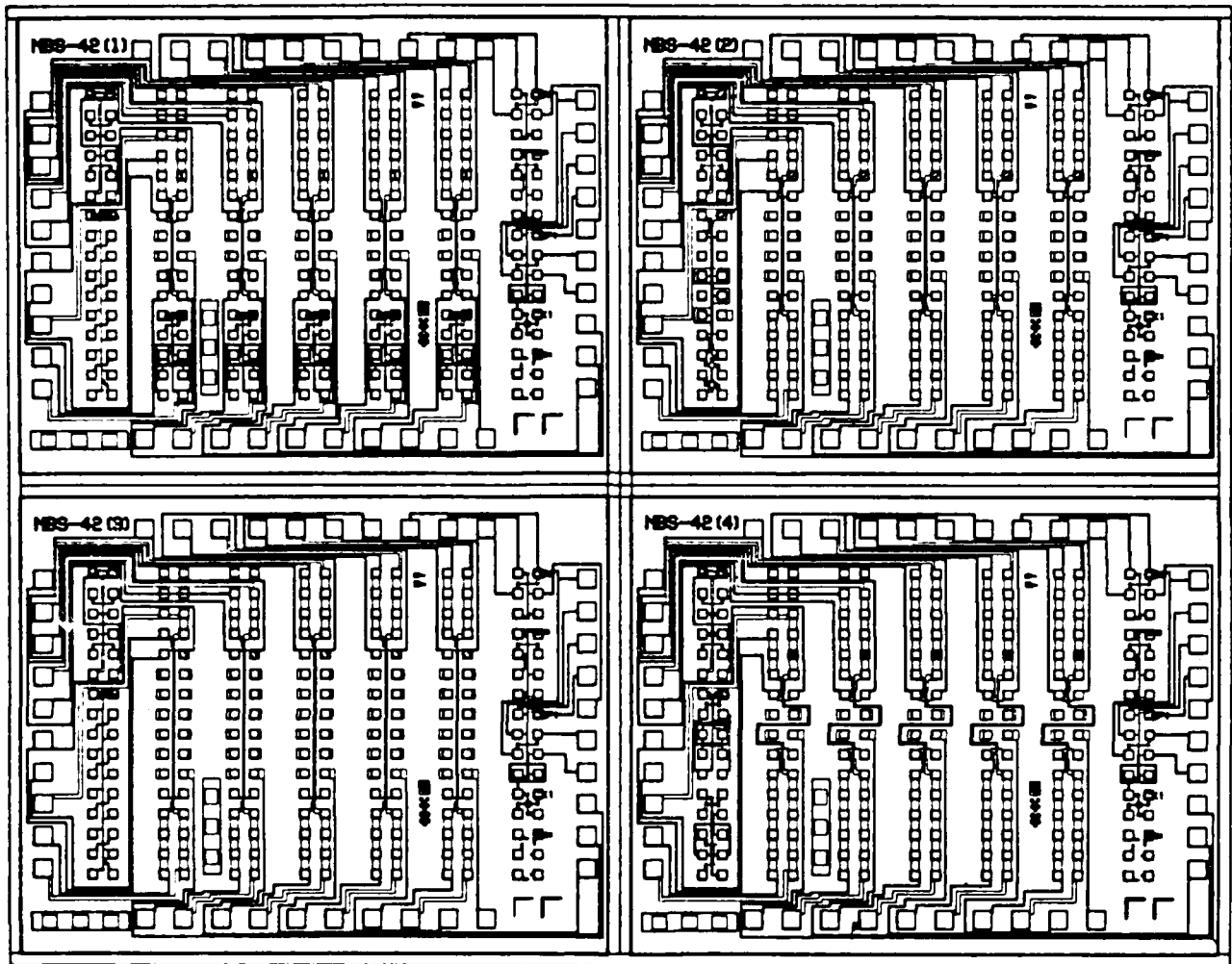


Fig 1. Two-level mask drawing of NBS-42 test chip (7.64 by 9.68 mm) where the lighter line is the metal and the other is the passivation level. Each quadrant has five centrally-located electromigration test structures.

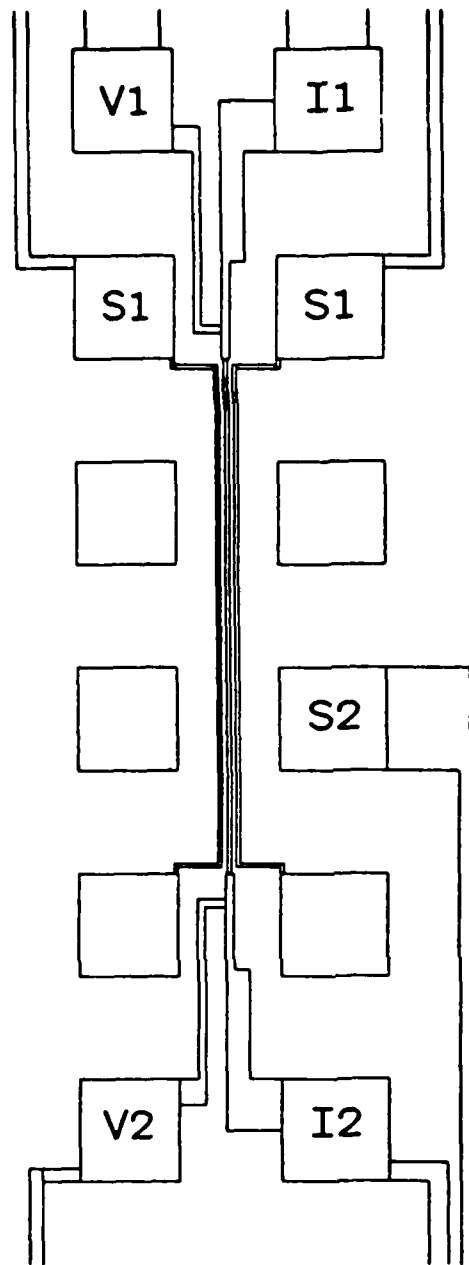


Fig. 2. Metal-level mask drawing of the electromigration test structure with a 400- $\mu\text{m}$  long test line. Current through the test line is provided by pads I1 and I2. Voltage measurements and open-circuit failure detection of the test line are made with contacts V1 and V2. Short-circuit failure to the adjacent-running lines is detected with pad S1. Pad S2 can be used, with a second-level metal, to detect short-circuit failure between the test line and an overlying metal stripe (not shown).

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## Interlaboratory Electromigration Experiment

### PURPOSE

- o ASSESS REPRODUCIBILITY OF ELECTROMIGRATION CHARACTERIZATIONS
- o BROADEN TECHNICAL BASE FOR DEVELOPMENT OF GUIDELINES FOR:
  - design of test structures
  - measurement of t50
  - characterization of metallizations
  - report of characterization results

## Interlaboratory Electromigration Experiment

### PARTICIPATING LABORATORIES

1. Burroughs Corp., San Diego CA  
Paul Giotta
2. General Electric Co., Syracuse NY  
Donald La Combe
3. Hewlett-Packard Laboratories, Palo Alto CA  
Paul Merchant and Henry Chiang
4. IBM, Essex Junction NY  
Dennis Bouldin
5. IBM, Hopewell Junction NY  
James Lloyd
6. IBM Thomas J. Watson Research Center, Yorktown Heights NY  
Thomas Kwok
7. Intel Corporation, Aloha OR  
Jose Miaz and Babak Sabi
8. Motorola, Austin TX  
Ed Travis
9. Sandia Laboratories, Albuquerque NM  
James Arzigian
10. Signetics Corp., Sunnyvale CA  
Janet Towner
11. Syracuse University, Syracuse NY  
James Schwarz
12. Texas Instruments, Houston TX  
Steve Lepkowski and P. B. Ghate
13. United Technologies Microelectronics Center  
Malcolm Garren
14. University of Florida, Gainesville FL  
Rolf Hummel

## Interlaboratory Electromigration Experiment

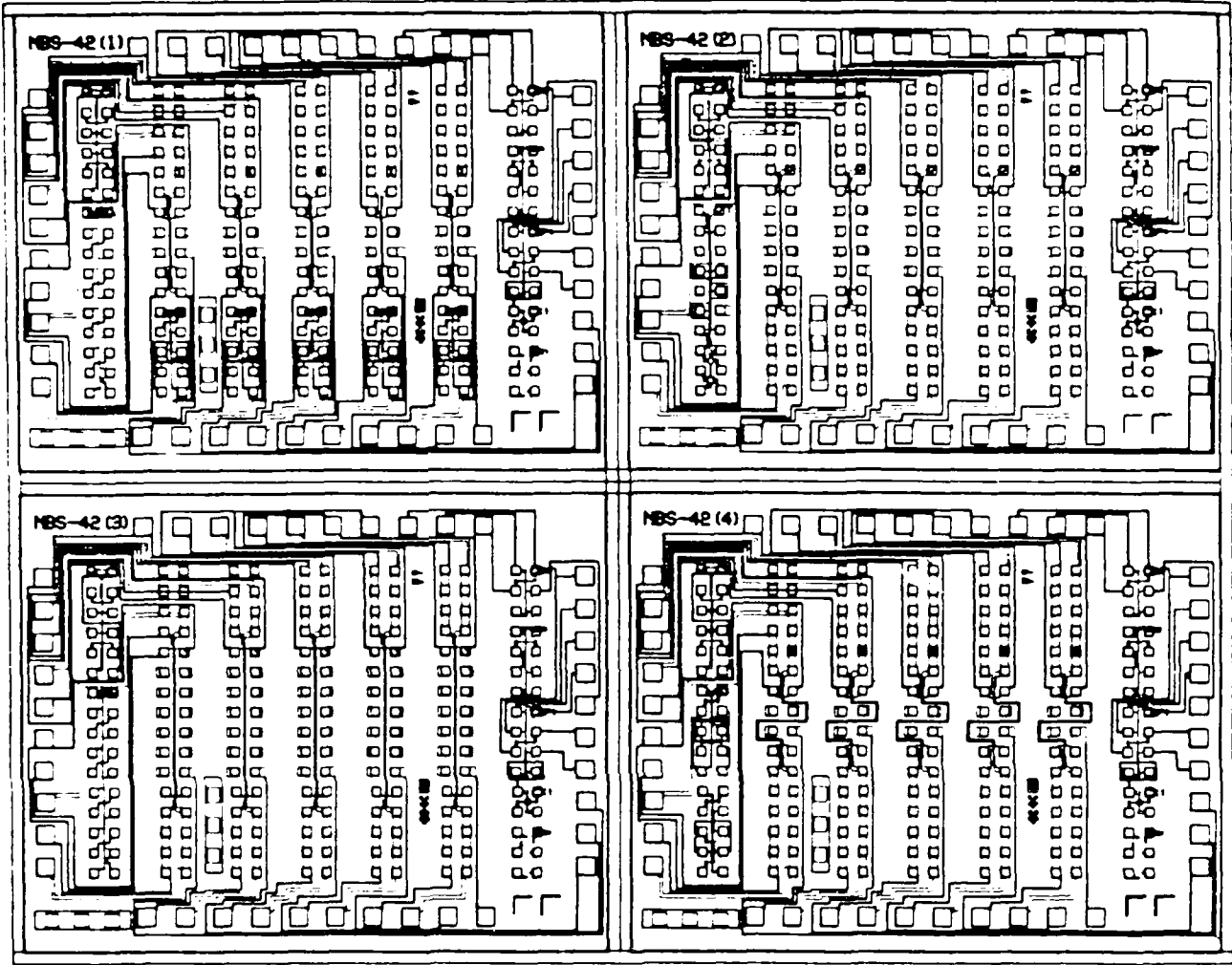
### FIRST PHASE

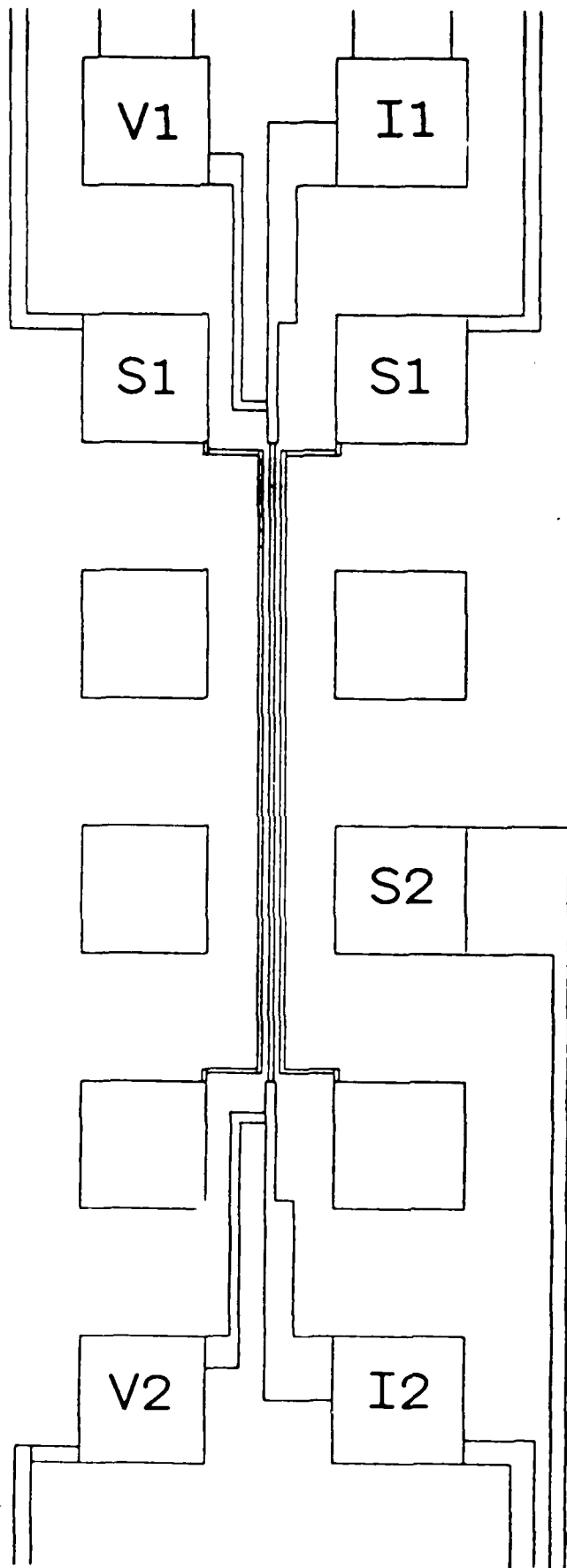
- o UNPASSIVATED AL 1%Si METALLIZATION
- o TEST PARTS FROM ONE METALLIZATION LOT
- o LABS STRESS EQUIVALENT TEST PARTS:
  - 20 parts at  $J = 1.0 \text{ MA/cm}^2$  and  $T(\text{oven}) = 175 \text{ deg C}$
  - 20 parts at  $J = 2.5 \text{ MA/cm}^2$  and  $T(\text{oven}) = 150 \text{ deg C}$
- o LABS USE OWN METHOD TO DETERMINE T50
- o LABS NORMALIZE DATA:
  - $T(\text{metallization}) = 175 \text{ DEG C}$
- o NBS SERVES AS REFERENCE LABORATORY

## Interlaboratory Electromigration Experiment

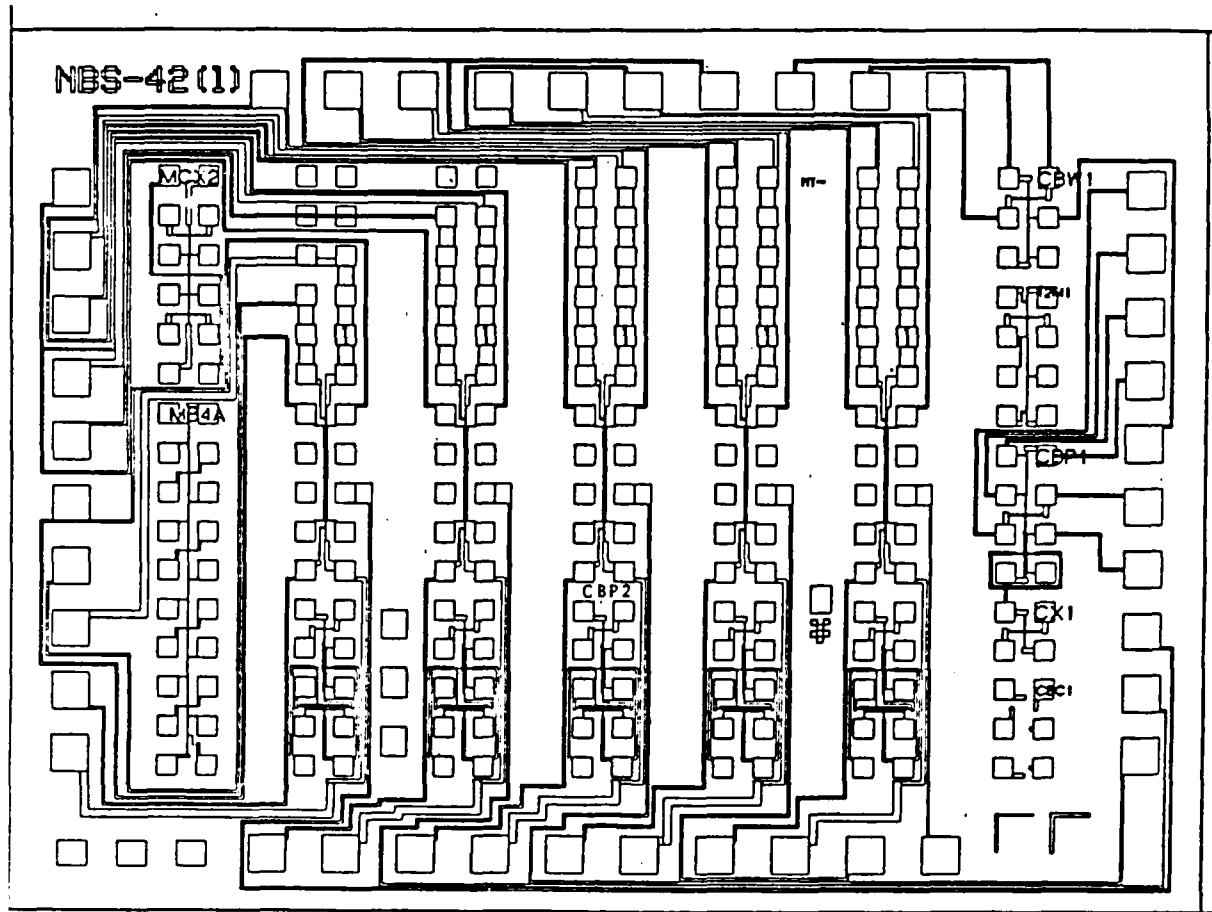
### EXPECTED OUTCOMES

- BETWEEN-LABORATORY REPEATABILITY
  - Equivalent Test Parts (packaged parts, chips, sectors)
  - Same stress levels
  - Different Methods
- WITHIN-LABORATORY REPEATABILITY
  - Equivalent test parts
  - One method
- INTERWAFER VARIATION OF T50 AND SIGMA
- EFFECT OF JOULE HEATING ON REPEATABILITY
- EFFECT OF TEST-LINE LENGTH ON T50 AND SIGMA
- EFFECT OF CURRENT DENSITY ON ACTIVATION ENERGY
- COMPILATION OF TEST METHODS USED





BASIC ELECTROMIGRATION TEST STRUCTURE



QUADRANT 1 OF ELECTROMIGRATION TEST CHIP (NBS 42)

## Interlaboratory Electromigration Experiment

### PARAMETER GRAND MEANS AND ESTIMATES OF PARAMETER UNIFORMITY FOR THE LOT OF SIX TEST WAFERS

PARAMETER	GRAND MEAN	PARAMETER UNIFORMITY WITHIN		
		LOT	WAFER	QUADRANT
RESISTANCE, R, of test structure	5.07 ohm	7.2%	3.3%	0.9%
SHEET RESIS- TANCE, R <sub>s</sub> , of metallization	36.8 milliohm/□	1.2%	2.7%	0.5%
LINewidth, w, of metallization	3.10 microns	6.9%	2.0%	0.6%
THICKNESS, t <sub>m</sub> , of metallization	0.86 microns	1.8%	2.7%	--
THICKNESS, t <sub>ox</sub> , of oxide	1.56 microns	0.6%	0.9%	--

# Interlaboratory Electromigration Experiment

## PARAMETER MEANS FOR WAFER LOT

### LINEWIDTH

PARAMETER	MEAN VALUE (microns)
w	3.003
wp - w	0.092
wp	3.095
wp(h) - wp(v)	0.141
wp(h)	3.236

### LINE SEPARATION

PARAMETER	MEAN VALUE (microns)
s(v)	4.047
s(v) - s(h)	0.389
s(h)	3.656

### TEST STRUCTURE RESISTANCE

PARAMETER	MEAN VALUE (ohms)
R(400)	5.07
R(800)	9.81
R(1200)	15.05
R(1200 <sup>^</sup> )	14.11

MEASUREMENT OF ACTIVATION ENERGY  
AT TWO LEVELS OF CURRENT DENSITY

J (MA/cm*2)	T1(metall.) (deg C)	T2(metall.) (deg C)	Delta T (deg C)	Q (eV)
1.0 (1)	179	218	39	0.495
2.5 (2)	144	185	41	0.502

- (1) 40 test structures used to determine t50 at T1 and at T2.  
(2) 35 test structures used to determine t50 at T1 and at T2.

RESULT:  $Q(J=2.5 \text{ MA/cm}^2) - Q(J=1.0 \text{ MA/cm}^2) = 0.007 \text{ eV}$

CONCLUDE: Activation energy is not a function of current density.

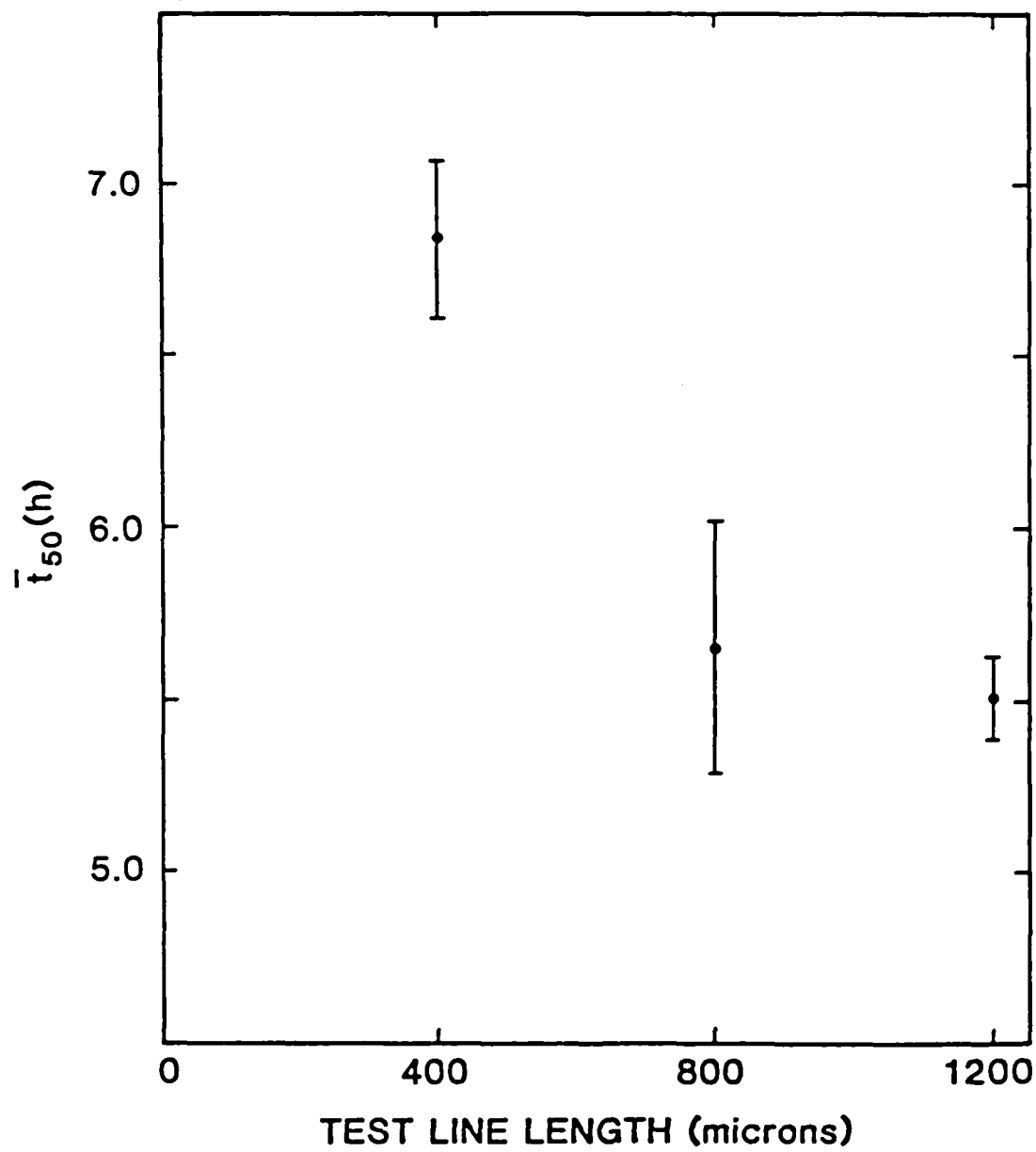
laboratory Electromigration Experiment

RESULTS FROM THREE t50 DETERMINATIONS(1) FOR STRUCTURES WITH  
400, 800, AND 1200 MICRON TEST LINES

	L=400 microns		L=800 microns		L=1200 microns	
	t50N(2) (h)	sigma	t50N (h)	sigma	t50N (h)	sigma
	7.31	0.26	5.50	0.31	5.26	0.26
	6.68	0.24	5.10	0.26	5.64	0.24
	6.53	0.29	6.36	0.25	5.63	0.27
<u>Sigma:</u>		0.27		0.27		0.25
<u>t50N (h):</u>	6.84		5.65		5.51	
<u>sd (h):</u>	0.41		0.64		0.22	
<u>sd/t50N:</u>	6.0%		11.3%		4.0%	

ESTIMATED WITHIN-LABORATORY REPEATABILITY: 0.46 h (7.7%)

- 
- (1) 20 structures used per t50 determination, per test-line length.  
Stress conditions:  $J = 2.5 \text{ MA/cm}^2$  and  $T(\text{oven}) = 150 \text{ deg C}$ .
- (2) Normalized to a metallization temperature of 175 deg C and a test  
line area of 2.71 microns squared.



## Interlaboratory Electromigration Experiment

### INTERWAFER VARIATION OF T50 AND SIGMA

WAFER	J=1.0 MA/CM*2		J=2.5 MA/CM*2	
	T50 <sub>n</sub> (1) (h)	SIGMA	T50 <sub>n</sub> (1) (h)	SIGMA
1	33.74	0.31	6.41	0.27
2	33.90	0.36	5.97	0.25
3	34.24	0.30	5.52	0.25
4	33.35	0.35	6.50	0.23
5	30.47	0.36	5.39	0.32
7	27.78	0.27	5.74	0.24
8	31.37	0.37	5.51	0.35
MEAN	32.12	0.33	5.86	0.27
SD	2.38	0.04	0.45	0.05
SD/MEAN	7.4%		7.7%	

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(1) T50 normalized to:

1. metallization temperature of 175 deg. Celsius and
2. test-line area of 2.58 microns squared.

Interlaboratory Electromigration Experiment

BETWEEN-LABORATORY REPRODUCIBILITY

$$J = 2.5 \text{ MA/CM}^2$$

LAB ID	LABORATORY		REFERENCE		$\frac{T50n(\text{LAB})}{T50n(\text{REF})}$
	T50n(1) (h)	SIGMA	T50n(1) (h)	SIGMA	
C	3.55	0.29	5.64	0.24	0.63
D	3.00	0.35	5.64	0.24	0.53
A	6.53	0.3	6.76	0.27	0.97
A(2)	5.77	0.32	6.76	0.27	0.85
O	4.44	0.34	6.11	0.23	0.73
W	0.85	0.45	6.11	0.23	0.14
J	4.32	0.41	5.64	0.24	0.77
P	7.0	0.31	5.52	0.25	1.27
E	4.95	0.30	5.52	0.25	0.83

$$J = 1.0 \text{ MA/CM}^2$$

LAB ID	LABORATORY		REFERENCE		$\frac{T50n(\text{LAB})}{T50n(\text{REF})}$
	T50n(1) (h)	SIGMA	T50n(1) (h)	SIGMA	
A	40.28	0.4	35.70	0.31	1.13
A(2)	38.52	0.4	35.70	0.31	1.08
O	32.22	0.32	30.39	0.35	1.06
W	20.5	0.26	30.39	0.35	0.68
J	25.6	0.42	27.88	0.27	0.92
P	29.0	0.35	34.24	0.30	0.85
E	32.92	0.36	34.24	0.30	0.96

- (1) T50 normalized to a metallization temperature of 175 deg. Celsius.  
 (2) Alternative means of determining metallization temperature and independent readings of t50's and sigmas from charts.

## Interlaboratory Electromigration Experiment

### SUMMARY

- o PARAMETER UNIFORMITY:
  - Metallization Sheet Resistance and Thickness
    - Over a Wafer: 3 %
    - Within Wafer Lot: 3 %
  - Metallization Linewidth
    - Over a Wafer: 3 %
    - Within Wafer Lot: 8%
  
- o ACTIVATION ENERGY: 0.50 eV (not dependent on J)
  
- o WITHIN-LABORATORY REPEATABILITY of T50: 8 %
  
- o T50 is a FUNCTION of TEST LINE LENGTH below about 800 microns
  
- o INTERWAFER VARIABILITY OF T50: 8 %
  
- o BETWEEN-LABORATORY REPEATABILITY
  - For  $J = 1.0 \text{ MA/CM}^2$  Stress:
    - Generally Within One-Laboratory Repeatability Limits
  - For  $J = 2.5 \text{ MA/CM}^2$  Stress:
    - Variable, But Generally No Worse Than a 2:1 Difference
  - Number of Sources for Variability Noted

END

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