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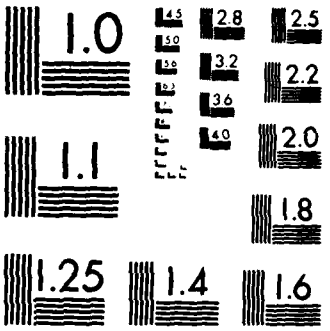

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Two Step Oxidation Processes in Silicon

by

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TWO STEP OXIDATION PROCESSES IN SILICON

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ABSTRACT - We have studied dielectric breakdown characteristics of thin (~ 10nm) silicon dioxide films grown on silicon under the following conditions: (A) Standard oxidation process with the oxide grown at 800 ^{o}C; (B) Annealing the oxides at 1000^{o}C in argon for 30 minutes after going through step (A); (C) Two - Step oxidation, i.e., 800^{o}C - 4 nm followed by 1000^{o}C anneal for 30 minutes in argon and a final oxidation at 800^{o}C to grow a total of 9 nm; (D) Growth of oxide at 1000^{o}C. The results show that (B) and (C) have comparable dielectric breakdown strengths, indicating that high temperature annealing has the same advantage as the two-step oxidation in improving the dielectric strength of silicon dioxide. High resolution transmission electron micrographs show that the interface structures are fairly similar in all the cases indicating that the interface smoothness as observed in the transmission electron micrographs are not directly responsible for the dielectric breakdown. Our observations of the protrusions at the Si/SiO_2 interface may also possibly explain the high values of the refractive index which has earlier been attributed to a monolayer of non-stoichiometric SiO_x at the Si/SiO_2 interface.

I.INTRODUCTION

Due to the ever increasing demand for reducing the dimensions of electronic components, integrated circuits and chips, the need for highly reliable and long lasting gate material has been tremendously felt. Possibly next to silicon, silicon dioxide has the most significant research input by virtue of its (i) compatibility with silicon related processes, (ii) ease with which it can be grown or deposited and (iii) agreeable dielectric strength. As the physical dimensions of the integrated circuit chips are reduced, the required oxide thickness also needs to be reduced as is deduced from scaling considerations [1]. Thus, for sub-micron dimensions, reliable and durable thin oxides are needed. The practical limits of the oxide thickness are essentially governed by factors like the tunneling leakage current, field-induced degradation and dielectric breakdown. In fact, the dielectric breakdown decides the lowest limit of the thickness to be at 9.5 nm for a 5-volt operation (field = 5.26MV/cm) [2].

Recently, there has been several papers [3-6] in the literature proposing new methods for growing thin oxides. These oxides have been characterized as better than dry or dry-wet-dry processes. All the new methods involve two steps. While Chen and Cheng [3] have proposed a partial-TCE (trichloro ethylene) technique involving a low temperature dry oxidation followed by a high temperature dry oxidation with an appropriate amount of TCE, Nulman et. al. [4] have utilized a two-step rapid thermal processing with the first step at 800^{o}C for 30 seconds followed by a higher second temperature step with a duration between 5-30 seconds. In this case, heating was provided by tungsten-halogen lamps. Breakdown voltages of 13.8 MV/cm have been reported for these oxides. Such high values of the breakdown voltage compare very well with thermally grown oxides at low pressure [7].

A method for forming thin and good quality gate oxides using two-step oxidation processes was reported earlier by Hashimoto et. al. [8]. This process consisted of initial oxida-

tion at low temperature with low HCl concentration followed by HCl treatment at high temperature in a mixture of N_2, O_2 and HCl gases. Such oxides were shown to have reduced defect density. In recent years, the two-step oxidation process has undergone several modifications. One such modification has been reported by Bhattacharya et. al. [5]. Their method [5] involves the growth of 3 to 4 nm of oxide at 900 or 950°C followed by an annealing step at 1050°C for 1h in Ar and then followed by the growth of additional oxide at 900 or 950°C to a final thickness of 8 to 9 nm. This method has been shown to yield oxides of better integrity with a tight distribution in breakdowns yielding low defect densities of less than 5 cm^{-2} and intrinsic breakdown field of 12 MV/cm. The two-step oxidation process has been shown to result in very smooth Si/SiO_2 interfaces [9]. Bhattacharya et. al. [5,9] have attributed the improvement in breakdown characteristics to the reduction in roughness of the interface. The purpose of this investigation is to examine the correlation of the interface roughness with the resulting dielectric breakdown during the two-step oxidation proposed by Bhattacharya et. al. [5]. Here, we report such studies of the two-step oxidation. The oxides were grown at temperatures below that of the viscous flow and the subsequent annealing step was chosen at T = 1000°C in order to observe the influence of the viscous flow.

II . EXPERIMENTAL PROCEDURES

In this study, several p-type Czochralski grown single crystal silicon wafers of <100> orientation and 2 ohm-cm. resistivity were used. Wafers were cleaned using conventional cleaning procedures including the RCA technique followed by a HF dip and thorough rinsing with DI water. Thin oxides (8-9 nm) were grown thermally in dry oxygen. The following four sets of samples were prepared ; Set A was a standard oxidation process with the oxide grown at 800°C. Set B involved annealing the samples after going through process A, at 1000°C for 30 minutes in argon. Set C consisted of the two-step oxidation, i.e., 800°C - 4 nm followed by 1000°C anneal for 30 minutes in argon (the samples

gain ~1 nm) and a final oxidation at 800°C to grow a total of 9 nm. Set D involved the growth of oxides at 1000°C. Ultra-high pure oxygen (H_2O < 0.5ppm) was used in the oxidation process.

For breakdown measurements, specimens were prepared by evaporating 700nm of aluminium on the oxide through a metal mask to form Al dots of 32 mil in diameter. The oxide was removed from the back of the wafers, and aluminium was evaporated for a back contact. Post-metal annealing was done in forming gas (10% H_2 gas in N_2) at 450°C for 30 minutes. A Rucker and Kolls automatic prober stepper model 682 was utilized for the breakdown measurements. Voltages were measured for threshold currents of 10 μA. Oxide thickness measurements were made employing a research quality ellipsometer. These measurements were carried out at different points on the wafer and the thicknesses were found to be within 2% . A refractive index value of 1.465 for SiO_2 was used in these evaluations. The thicknesses were also measured by high-frequency capacitance-voltage measurements and transmission electron microscopy. A combination of mechanical and ion beam polishing methods were used to produce cross section samples for high resolution transmission electron microscopy (HREM). High resolution phase contrast images of the interface were taken at scherzer optimum defocus value of 65 nm and <110> orientation using a JEOL (200 CX) TEM at 200 KV with a 0.27 nm point to point resolution.

III . RESULTS & DISCUSSION

In Table 1, the summary of the oxide breakdown voltage characteristics are presented. As can be seen in the table, the annealing step (Set B) has brought about an increase in the breakdown field from 10.5 MV/cm (Set A) to 13.5 MV/cm. The breakdown field remains unchanged at the end of the two-step oxidation process (Set C). Also, defect densities for all the samples were found to be almost equal.

Figure 1 shows a phase contrast transmission electron image of the Si/SiO_2 interface at the end of the two-step oxidation process (set C) illustrating the thickness of the oxide. The

results of the HREM studies of all the sets A - D are presented in figure 2. As can be seen in figures (2a) and (2d), there does not seem to be any clear difference in the amount of roughness/undulations at the Si/SiO_2 interface. The protrusions of the crystalline silicon atoms into the amorphous SiO_2 remain very much alike.

The fact that fewer protrusions are observed after a 1000^0C anneal for 30 minutes in argon in figure 2b (intermediate step) may be explained by the oxidation of silicon (protrusions) by excess oxygen or traces of oxygen or water in argon at high temperatures. This may also be due to the tendency of the high temperature to lower the surface energy of the asperities by increasing the radius of curvature of the asperities thus resulting in a smoother interface. In our studies, we define a rough (or smooth) interface by the presence (or absence) of protrusions at the interface. At the completion of the two-step oxidation process (figure 2c), although the high temperature anneal brings about a decrease in the stress, additional oxide growth is expected to increase the stress. However, as has been pointed out by Carim and Bhattacharya [9], the oxidation is for a short period and thus may not contribute significantly to asperity formation. As can be seen in the micrographs (figures 2b & 2c), there is not any clear evidence of the superiority of the two-step oxidation process (figure 2c) as claimed by Bhattacharya et.al. over a single-step oxidation followed by a high temperature anneal (post-oxidation anneal) (figure 2b). If post-oxidation anneal results in the formation of hillocks and pits (protrusions of Si into SiO_2 and vice-versa), as seen in the micrographs of Carim and Bhattacharya [9], the absence of either of these after a two-step oxidation is hard to expect unless the second step has a preferential way of forming an oxide getting rid of hillocks and pits. We do not know of any such preferences. The other possibility may involve the realignment of the silicon atoms and the SiO_2 molecules during the two-step process in order to minimize the interfacial free energy.

The results of the electrical measurements (Table 1) indicate that the results are not different for devices after the intermediate annealing step and those at the end of the two-

step oxidation process. The breakdown voltage improves considerably after the intermediate annealing step and remains almost the same after two-step oxidation. The values of the breakdown field of 13 MV/cm obtained here are higher than the 12 MV/cm obtained by Bhattacharya et. al. [5]. It may be pointed out here that, actually, some of the devices of Bhattacharya et. al. were of large area - 0.032 cm^2, with the result that a 10 μA threshold current may not be sufficient enough to define a breakdown voltage. Afterall, at breakdown fields of 12 MV/cm, the Fowler-Nordheim tunneling current in SiO_2 could be as high as 0.1 $Amp.cm^{-2}$. Thus, test currents of 10 μA will be limiting the voltage.

For quite some time, it has been believed that a non-stoichiometric silicon rich oxide, SiO_x, about 0.4-0.7 nm thick with an index of refraction of 2.5 - 2.8 exists at the Si-SiO_2 interface [10,11]. Its thickness is known to depend on the temperature at which the oxide was grown [10] and decreases with increase in temperature. This monolayer transition layer has been confirmed by XPS (X-ray Photoluminescence Spectroscopy) measurements to consist of a chemical distribution of sub-oxide states, Si_2O, Si_2O_3 and SiO, which can give rise to unsaturated bonds and discrete electronic states [12-14]. The protrusion of silicon atoms into the SiO_2 (as can be seen in our micrographs) can also contribute to increased refractive index at the Si/SiO_2 interface.

It may be noted here that the micrographs (Fig. 2(a-d)) do not show any sign of crystallinity in the SiO_2 which are believed to cause secondary breakdowns [15] at fields of 1-3 MV/cm. This is understandable by virtue of the low temperatures involved in our process. Since the protrusions of the silicon atoms into the SiO_2 are confined to a few atomic layers at the interface, we expect the high value of the refractive index (2.5 - 2.8) to be possibly due to the intermixing of Si and SiO_2 at the interface. Such an intermixing will reduce in thickness with increase in temperature of growth (at high temperatures) explaining thereby the results of Taft and Cordes [10]. Henzler and Marienhoff [16], utilizing high resolution low energy electron diffraction (LEED) technique reported the presence of steps at the

Si/SiO_2 interface, in agreement with our work. They attribute the step distributions to (1) inhomogenities at the interface (like protrusions) or (2) the oxidation and annealing mechanisms involving a combination of slow and fast diffusion along the interface. A symmetry of undulations has also been considered as a posibility. A need to optimize the distributions for better device performance has been pointed out. Our results of the structural measurements confirm the presence of protrusions at the Si/SiO_2 interface. However, our electrical measurements do not give any direct evidence of the correlation of protrusions to better device performance except for the fact that, atleast in thin oxides, protrusions may account for reduced SiO_2 thickness thus causing breakdowns at lower voltages or fields. Annealing does help in reducing the protrusions possibly by oxidizing the silicon atoms closest to or within the interface thus assuring a uniform oxide thickness and hence improving the breakdown characteristics. Annealing would also permit a reduction in the stress. The results of the breakdown fields for various sets of samples are compared with the data available in the literature [17-21]. Such a comparison is presented in figure 3. As shown in figure 3, post-oxidation has all the advantages of the two-step oxidation process. It is hard to correlate the advantages of the two-step oxidation to the very specific requirements of improved breakdown characteristics. Our findings of inherent advantages with post-oxidation anneal are in complete accord with those of Nulman [21]. At present, it is believed that protrusions are more pre-dominant at low processing temperatures, because of increased stresses. This also explains the reasons for the high quality of SiO_2 films grown at high temperatures.

IV . CONCLUSIONS

Our studies of the two-step oxidation process show that post-oxidation annealing has the same advantages as that of the two-step oxidation . The advantages are essentially in improving the breakdown characteristics of SiO_2. At least for device purposes, post-oxidation annealing seems to be sufficient for obtaining reliable oxides. Our microstructural studies based on high resolution transmission electron microscopy indicate that two step oxidation and post-oxidation processes lead to similar interface structure with protrusions of the silicon atoms at the Si/SiO_2 interface. These observations are in accord with those that follow from high resolution low energy electron diffraction. The protrusions of the silicon atoms into the oxide seem to throw some light on the possible contributions to the large values of the refractive index and high dielectric strength at the Si/SiO_2 interface.

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TABLE 1 - Dielectric breakdown characteristics of the sets of samples considered in this study.

Process	Oxide thickness(nm)	Breakdown field(MV/cm)
Set A ;		
800^{o}C	9	10.5
Set B ;		
800 - 1000^{o}C	9	13.5
Set C;		
800-1000-800^{o}C	9.2	13.5
Set D;		
1000^{o}C	10	11.5

The area of the MOS devices (dots) were typically ~ 0.00519 cm^{2}.

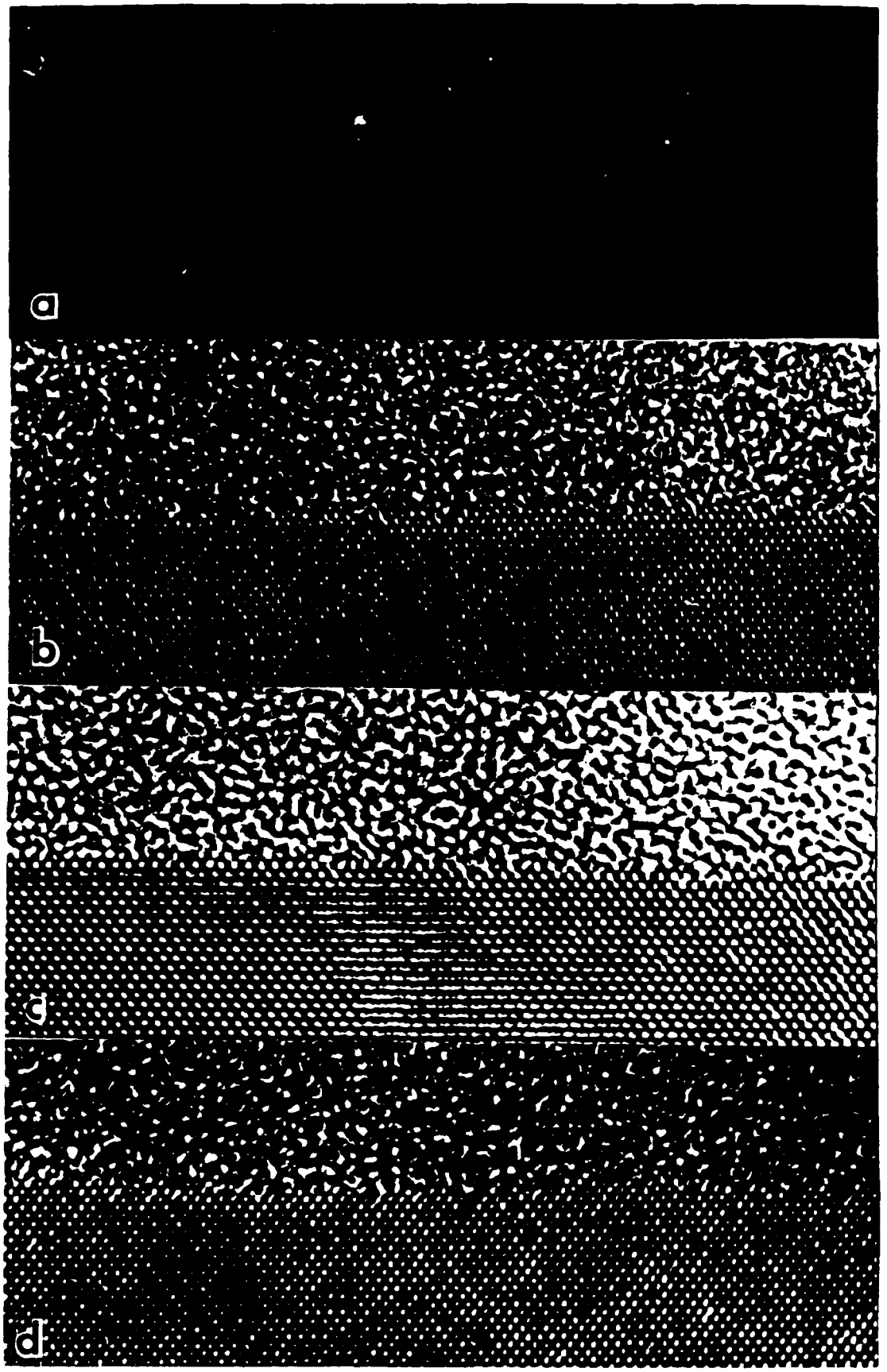
FIGURE CAPTIONS

FIGURE 1 - Low magnification transmission electron micrograph of the Si/SiO_2 interface of Set C at the end of the two-step oxidation process to illustrate the oxide thickness.

FIGURE 2 - High resolution transmission electron micrographs of the Si/SiO_2 interface ; (a) Set A; grown at $800^{o}C$, (b) Set B; $1000^{o}C$ anneal for 30 minutes in argon after (a), (c) Set C; two - step oxidation : 800 - 1000 - 800 ^{o}C, and (d) Set D; grown at $1000^{o}C$.

FIGURE 3 - Breakdown fields versus oxide thickness. Data are from Osburn [18], Harari [19], Iwamatsu [20], Nulman [22]. Our results are compared with the rest of the data cited from the literature.

Fig. 1


a
b
d
d

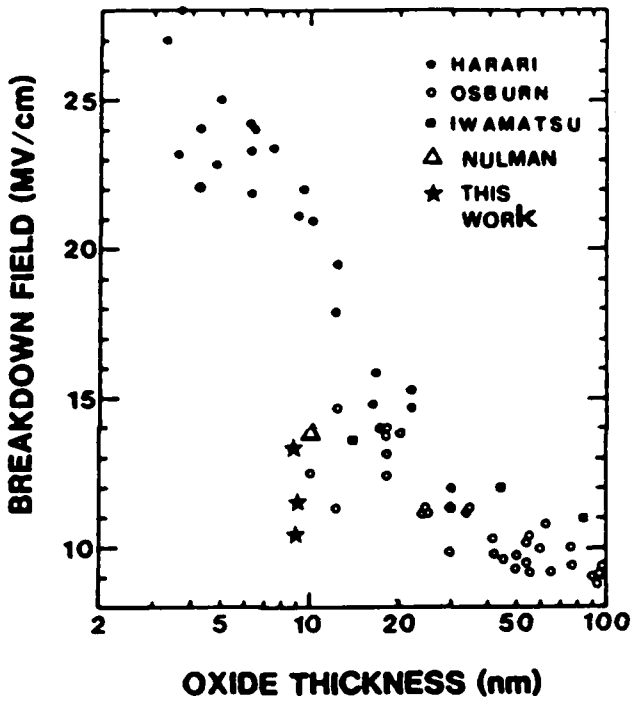

BREAKDOWN FIELD (MV/cm)
25
20
15
10
2
5
10
20
50
100
OXIDE THICKNESS (nm)
HARARI
OSBURN
IWAMATSU
NULMAN
THIS WORK

Fig. 3

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