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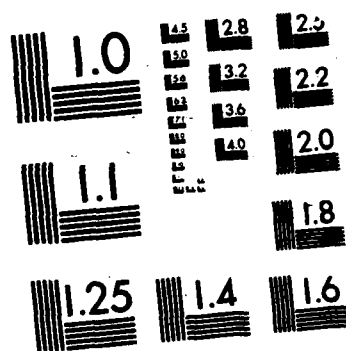# THE EFFECT OF OPERATING FREQUENCY IN THE RADIATION INDUCED BUILDUP OF TRAPPED HOLES AND INTERFACE STATES IN MOS DEVICES

Timothy Daryl Stanley

July 1986

Final Report

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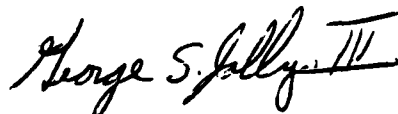
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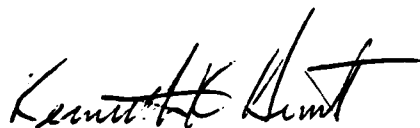
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The amount of threshold voltage shift in MOS devices caused by ionizing radiation is strongly dependent on the bias voltage applied to the gate of the MOS device both during and after the radiation. Past experimenters found that n-channel MOSFETs alternately biased "off" and "on" did not have a threshold voltage shift that corresponded to the average bias, but the observed shift was more positive than the shift for either the continuously "on" or "off" bias conditions. In the work presented here, over 200 test transistors, built in a radiation hardened $4/3 \mu m$ process, were irradiated at various operating frequencies, temperatures and bias voltages in an effort to understand the observed effect. The contributions of trapped holes and interface states on the observed threshold voltage shifts were determined through subthreshold current measurements. This research demonstrated the source of this anomalous alternating bias effect on the radiation response of MOS devices is reduced hole trapping and increased interface state (over)

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buildup in n-channel MOS devices. In p-channel devices, reduced hole trapping is the primary source of this effect. This effect results when holes, trapped at the oxide-silicon interface during the "on" half of the cycle, are annihilated by radiation-produced electrons pulled into the trapped hole space charge during the "off" bias portion of the cycle. The annihilated holes close to the interface appear to cause interface state formation. A simple one-dimensional computer model that predicts the observed effect is developed. Also, an explanation for the increased hole trapping in "off" biased n-channel parts at low doses is given. Since failure in low dose rate environments has been shown to result from interface state buildup, alternating bias testing may be the worse case for testing MOS devices for application in space systems.

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CHAPTER I

INTRODUCTION

The majority of very large scale integrated circuits use
Metal-Oxide-Semiconductor (MOS) Field Effect Transistor (FET)
technology because it has very high input impedance, a simple
structure, and low static power consumption. The technology is,
however, sensitive to ionizing radiation [1]. Large scale circuits
built in other technologies, such as the bipolar technologies, are
also sensitive to ionizing radiation when used in large scale
circuits, due to parasitic MOS devices that are formed between
transistors under passivation and interlevel dielectric layers.
Therefore, applications that require the large scale integration and
the low power of MOS technologies, but operate in radiation
environments (i.e., satellites), require reductions in the radiation
sensitivity of MOS devices.

The basic source of the radiation sensitivity of MOS technologies
is the buildup of charge in the insulating layers of the device.
These layers are typically silicon dioxide and vary from thin (300 Å)
gate oxides to thick (10 um) interlevel and passivation oxides. The
charge buildup in the oxide shifts the threshold voltage that must be
applied to invert the semiconductor surface under the oxide, turning
the transistor on. Parasitic MOS devices must not turn on in a large
scale circuit or leakage paths between circuit elements will occur.
Gate oxide MOS devices in large scale circuits are the active elements
in the circuits and therefore must be able to switch the channel

current off and on for the circuit to function. Therefore, the turn-on or threshold voltage of gate oxide MOSFETs cannot be allowed to shift too much or failures can occur where MOSFETs cannot be turned on or where they cannot be turned off.

The amount of threshold voltage shift which a given radiation dose causes in a MOS device is a function of how the oxide was produced, its history after production, the thickness of the oxide, the electric field across the oxide during the radiation and the rate at which the dose is given. The electric field across the oxide during the radiation determines the yield of charge produced in the oxide by a given dose as well as the final position of the charge. The radiation dose rate dependence of threshold voltage shift is due to the instability of the radiation produced charge in the oxide. The oxide production process, plus the history and the thickness of the oxide, are important because they determine defects, impurities and stress in the oxide and at the oxide-semiconductor interface. The oxide thickness also governs the collection volume for the radiation-produced charge as well as second order effects like stress at the oxide-semiconductor interface. Through care in production, large scale devices have been built in MOS technologies that can survive total ionizing radiation doses of over 1 Mrad(Si).

The major thrust of this research is investigation of an anomalous alternating bias effect reported in 1981 [2]. The effect was an unexplained positive shift in the radiation induced threshold voltage change in n-channel MOSFETs that were alternately biased with 10 volts and 0 volts applied to the gate. The expected shift was

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between the shift for a static +10 volt and a static 0 volt bias. The observed shift was more positive than either the on or off shift. These results are given in figures 1.1 and 1.2. At the time of this observation, the shift of the n-channel transistors into depletion mode operation was the failure mode of concern. So the observed effect was not investigated further. Since that time, a failure mode called "rebound" has been observed that occurs because of positive shifts in the threshold voltage [3]. Also, techniques to separate the contributions to the threshold voltage shift from trapped holes and interface states by using the subthreshold I-V characteristics have been developed [4]. Through application of this past work in new experiments, the author has shown the anomalous alternating bias effect to be due to radiation enhanced annealing of trapped holes and enhanced buildup of interface states. These findings provide increased understanding of the mechanisms of trapped hole annealing and interface state formation. A computer code based on a simplified model is shown to predict the observed effect. The implications of the investigated effect on testing of microelectronics for application in space radiation environments are discussed.

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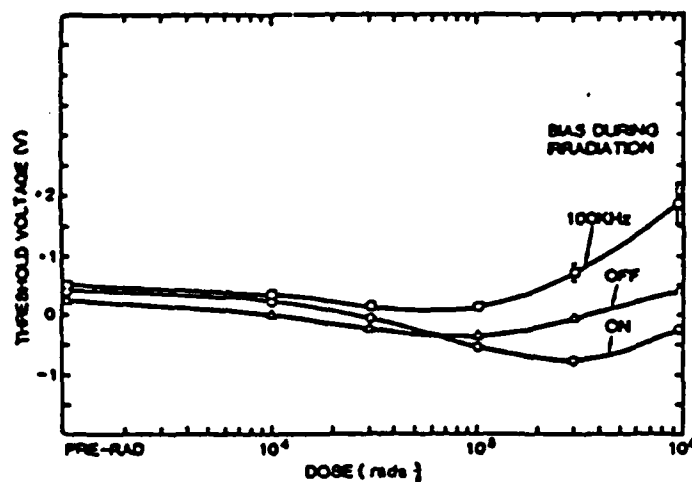
Figure 1.1 N-channel threshold voltage verses dose for transistors biased "on," "off," or switched between "on" and "Off" at 100 KHz durring irradiation from Dressendorfer [2]
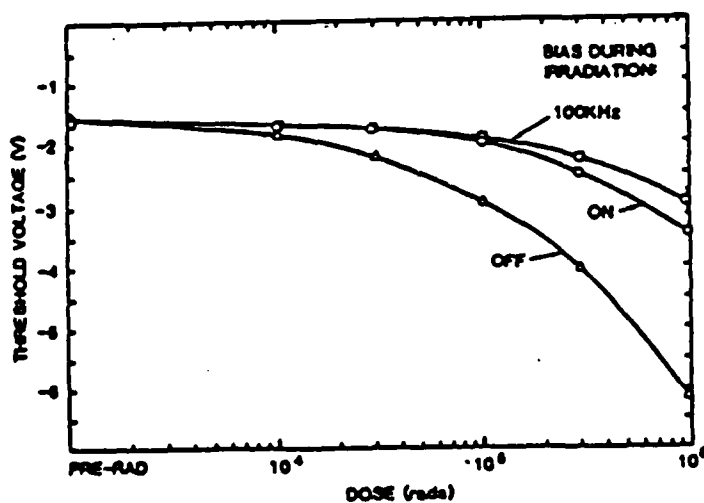
Figure 1.2 P-channel threshold voltage verses dose for transistors biased "on," "off," or switched between "on" and "off" at 100 KHz durring irradiation from Dressendorfer [2]

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CHAPTER II

RADIATION EFFECTS IN MOS DEVICES

Ionization

Ionization, caused by high energy electrons in silicon, is the source of the charge that builds up in the oxide regions during irradiation of MOS devices [1]. Some radiation sources directly bombard the device with high energy electrons. Others, including gamma radiation, produce the high energy electrons inside the MOS device through Compton scattering of silicon and oxygen electrons by the gamma ray photons. Each ionization event is the elevation of an electron from the valence band in the silicon dioxide to the conduction band, leaving behind a hole in the valence band (see figure 2.1). Thus, each ionization event produces an electron-hole pair. Even though the bandgap in silicon dioxide is only 9 eV, the average energy consumed for each ionization event is 18 eV [5].

Initial Recombination

The probability of recombination of the electron hole pairs shortly after creation is a strong function of the electric field stress across the oxide. In the presence of a strong electric field, the electrons and holes are separated, whe, if the field is weak, they tend to recombine. The yield of electron-hole pairs from initial recombination increases linearly with the electric field until a maximum yield is reached at a field of approximately 1Mv/cm [5].

Electrons are about six orders of magnitude more mobile in silicon dioxide than holes [6]. The electrons produced by ionizing

```
/////// METAL ///////
                             /////////////////////
       SiO₂                  + - + - + - + - + -
                             - + - + - + - + - +
                             + - + - + - + - + -
::::::::Si::::::::::          + - + - + - + - + -
                             :::::::::::::::::::::
```

a) Pre-irradiation.   b) Immediately After Radiation
No Charge in Oxide.   Burst. Electron Hole Pairs
                                Produced in Oxide.

```
/////////////////////        /////////////////////
    +     -     +                +         +
+     -     +     -           +         +
      -     +     -                 +
    +     -     +                +         +
:::::::::::::::::::::         :::::::::::::::::::::
```

c) After Initial Recombin-   d) After Electron Transport.
ation. The Greater The   T= approximately 1ps
Bias The Less The Initial
Recombination

```
/////////////////////        /////////////////////



+ + +  +  + + +               + - + -    + + -
:::::::::::::::::::::         :::::::::::::::::::::
```

e) After Hole Transport   f) Hole Annealing and Inter-
To the Si-SiO₂   Face State Buildup.
Interface. Holes
Trapped. T=1ms-1s

```
/////////////////////        /////////////////////



 -  -  -  -   -  -
:::::::::::::::::::::         :::::::::::::::::::::
```

g) Hole Annealing Complete.   h) After Complete Anneal Of
Interface State Buildup   Trapped Holes And Interface
Maximum. Rebound Condition.   States.

Figure 2.1   Radiation Effects In MOS Devices.

radiation exit the oxide through drift and diffusion in a picosecond time frame. The holes drift and diffuse through the oxide in a dispersive transport process until they are either trapped or exit the oxide. The hole transport mobility is a strong function of temperature and the processing of the oxide. At very low temperatures (77 °K), the hole mobility goes to essentially zero [7].

Hole Trapping

The traps for the holes are located within 50 $\overset{\circ}{A}$ of the silicon-oxide interface [8]. The fraction of the holes that are ultimately trapped is the major difference between oxides that are sensitive to radiation (soft oxides) and insensitive (hard) oxides. A soft oxide may trap as much as 50% of the holes while in radiation hardened oxides, only a few percent get trapped [9]. The trapped holes cause a negative shift in the threshold voltage of a MOS device and are one of the primary sources of radiation induced shift in the threshold voltage of MOS devices.

The probability of trapping for holes is shown by Dozier and Brown to be a function of the applied electric field, falling off as $E^{-1/2}$ [10]. This hole trapping dependence on field, coupled with the dependence of hole yield from recombination on field, results in a trapped hole dependence on field that increases as $E^{1/2}$ reaching a maximum at E=0.58 Mv/cm and then falling off as $E^{-1/2}$. Figure 2.2 shows this functional dependence. In this figure, Dozier and Brown plot the flat band voltage shift as a function of field applied during irradiation. Since no distortion occurred in their C-V curves indicating interface state buildup, the flat band voltage shift should

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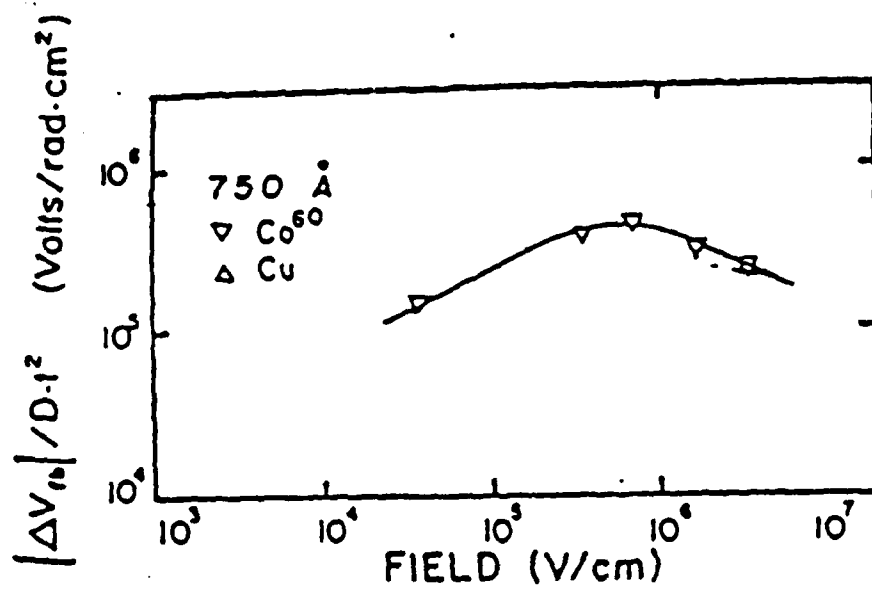
Figure 2.2 Trapped hole yield as a function of applied field from Dosier and Brown[10].

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be a good measure of the trapped hole yield.

Interface State Buildup

The other major source of radiation induced charge buildup in MOS devices is through radiation-induced interface state formation [11]. The interface states are either electrically charged or neutral, depending on the location of the fermi energy level in the silicon band gap. There are many models of interface state formation in the literature. A common feature of several of the models is a two step process that involves hole transport through the oxide as a first step. In one model, the second step is the transport of hydrogen to the interface [12]. This model is based on the observed dependence of radiation induced buildup of interface states on bias and timing. Supporting this model is the observation that increased hydrogen in the oxide results in increased radiation induced interface states [13]. However, it is difficult to understand why hydrogen annealing reduces interface state density before radiation, but increases it after radiation.

In the "Bond-Strain Gradient Model", the hole trapping event breaks a strained bond in the bulk SiO_2 [14]. The resulting defect is transported to the interface along strain gradients in the oxide. At the interface, the broken or dangling bond becomes an interface state. The experiments of Ma et. al. that show the dependence of interface state buildup on the thickness of the metal also support the bond-strain-gradient model [15]. Electron paramagnetic resonance (EPR) experiments have shown interface states to be dangling silicon bonds pointing out into the oxide from the silicon called P_b centers [16].

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In another model illustrated in figure 2.3, a strained oxygen-silicon bond in the SiO_2 near the oxide-silicon interface is broken by a hole trapping event [17]. The oxygen atom then relaxs to a position of lower energy. An electron then annihilates the trapped hole but the oxygen atom does not return to its original position. A dangling silicon bond now exists at the $Si-SiO_2$ interface that is an interface state. This model, by Lai of IBM, is based on experiments in which holes were avalanche injected into an oxide and trapped. A substantial flat band voltage shift resulted but few interface states were produced. The holes were annihilated by injecting electrons into the oxide and interface states were produced. The experiments by Johnson, et. al., support this model and show that holes trapped in SiO_2 at low temperatures are ultimately replaced by an equivalent number of interface states after being warmed and stored for a long period of time [18]. The general feature of the Lai model, that annihilated trapped holes somehow result in interface states, is adapted as a basic assumption for the model of this work, although it is clearly acknowledged that hydrogen and strain play a major role in interface state formation. A recent paper by Sabnis of Bell Telephone Laboratories, based on the observation of interface state buildup during hole annealing, also supports a casual relationship between trapped hole annihilation and interface state production [19].

The interface states in n-channel MOS devices are negatively charged when the MOS device is turned on and tend to compensate for trapped holes at the interface. Thus, n-channel MOS devices that build up similar numbers of trapped holes and interface states would have little change in threshold voltage with radiation dose if the

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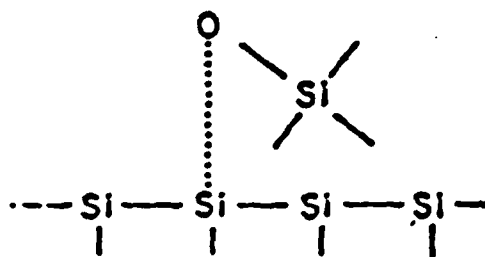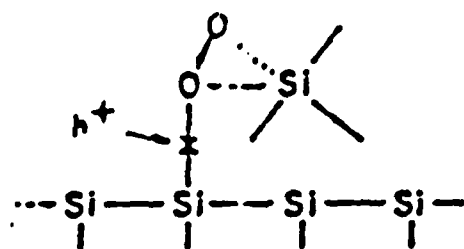
Figure 2.3   A strained O-Si bond at the SiO_2-Si interface is broken through trapping a hole.   The Oxygen atom moves to possition of lower strain.   The trapped hole is neutralized by an electron capture leaving a dangling Si bond that is an interface state from Lai [17].

trapped holes and interface states were stable with time. But the holes are detrapped with time in a phenomenon called annealing while interface states do not anneal except at temperatures above 200 [3].

Annealing And Rebound

Annealing causes the observed threshold voltage shift in MOS transistors to be sensitive to the radiation dose rate. If a MOSFET is radiated at a high dose rate, the hole trapping will dominate at early times since interface states take time to form. If the MOSFET is radiated at a low dose rate, holes will anneal at the same rate that they are formed. Since the interface states do not anneal they continue to build up. With time, the circuit fails because of the excess buildup of negative charge in the oxide of n-channel MOS devices due to the interface states. The hole trapping causes n-channel devices to fail due to an inability to turn off. The failure for interface state buildup would be an inability to turn the device on. Since the radiation induced threshold voltage shift in n-channel MOS devices is initially negative due to hole buildup and then becomes positive as interface state buildup occurs, the failure from interface states has been called "rebound" [3] and "super recovery." [20] This rebound failure is expected to be the dominant failure mechanism in space.

Dressendorfer, et. al. [2] reported that MOSFETs that were alternatingly switched between the "on" and "off" states at a 100KHz rate had a more positive threshold voltage shift than devices biased continuously in either the "on" or "off" state. Since the average bias from a 50% duty cycle square wave is halfway between "on" and

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"off", the expected result was a shift halfway between the "on" and "off" shifts. At the time of these experiments, rebound failure was not of concern, so this effect was not investigated. Since the alternating bias threshold voltage shift is positive from the static bias shifts, the cause of the alternating bias effect is either a reduction in hole trapping, increased interface state build up, or a combination of the two. Since rebound failure is due to interface state buildup and since alternating biases potentially cause greater interface state buildup, a thorough investigation into this effect was warranted.

Several experimenters have produced interface states through hole and electron injection into the oxide through avalanche injection [21,22,23,24]. Others, investigating alternating bias applied between the source and drain of MOS devices, showed the creation of interface states through "hot" electron injection into the SiO_2 [25,26,27]. These experiments used high alternating voltage stress at the pinch-off point near the drain for the charge injection. While these experiments are interesting, they provide little insight into the effect reported by Dressendorfer since his experiment used too low of voltages to avalanche inject carriers. Also, alternating bias experiments by Ackermann [28] and Roeske [29] showed that this effect was not observed in metal gate 4000 series commercial CMOS components. Nordstrom showed that irradiated metal gate MOSFETs have much less interface state "turn-around" in the threshold voltage than poly-silicon gate MOSFETs [30].

The technique used by Schwank [3] to observe the "rebound"

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condition in a MOS device was to annihilate trapped holes by tunneling electrons from the silicon into the trapped holes at 100 °C with a 10 V positive bias on the gate. Neamen [31] shows the importance of this tunneling in the radiation response of MOS devices exposed for long periods of time in the low dose environment of space. Saks, et. al. [32] showed that tunneling can prevent trapped hole accumulation in very thin oxide MOS devices. The annealing of the trapped holes that are normally compensated by interface states results in the large positive shift in the threshold voltage of n-channel MOSFETs typical of rebound.

Another source of electrons that could anneal the trapped hole space charge could be the photo-electrons produced in the oxide by the ionizing radiation. In experiments on 4000 series metal gate CMOS parts, Habing and Schafer showed that the parts quickly annealed when irradiated in an unbiased condition [33]. Experimenters with silicon-on-sapphire (SOS) MOSFETs have found that "back channel leakage" caused by radiation produced trapped holes in the sapphire could be quickly reduced by continuing the irradiation with the bias removed [34]. Dantas and Gauthier showed that trapped charge in the oxide of parasitic MOSFETs in bipolar circuits also quickly annealed when the device was irradiated with no bias applied [35]. This annealing of trapped holes by radiation produced electrons, coupled with the resulting increased buildup in interface states predicted by the "Lai" model that form the basis for the model to be presented.

Measurement Of Interface States

Several techniques have been used to measure interface state

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build up following irradiation. These include: C-V measurements on MOS capacitors; subthreshold I-V measurements; and charge pumping. The C-V technique is the traditional method used in interface state research but requires complex equipment and MOS capacitors rather than functioning transistors.

An interface state measurement technique usable on MOS transistors is the charge pumping technique [36]. This technique uses the charging and discharging of interface states to produce a current proportional to the interface state density. The technique is implemented by tying the source and drain of an MOS transistor together and then applying a slight reverse bias between this connection and the substrate through a current meter. A high frequency square wave is then applied between the gate and the substrate. The resultant current, which flows against the applied reverse bias, is proportional to the interface state density. This current results when interface states, which were filled from channel charge supplied from the source-drain contact, dump their charge into the bulk silicon as the voltage on the gate shifts the semiconductor surface from inversion into accumulation. The charge pump current is equal to the product of the square wave frequency, the area of the MOSFET channel, the electron charge, and the interface state density. The charge pump current is normally measured at several frequencies so that extrapolation of the current versus frequency curve to zero allows any reverse biased leakage current to be subtracted out. This is a relatively straight forward technique, but since an alternating bias effect is being investigated, the application of the alternating

bias in the charge pumping technique would potentially obscure the results of these experiments.

The method chosen to separate the hole trapping from the interface state formation in this research was the subthreshold conductance technique described by Winokur [4]. This technique uses the subthreshold I-V characteristics of transistors to measure the interface state density and the hole trapping. The method has the advantage that the threshold voltage data and the interface state data can be obtained during the same I-V measurement but the measured currents are on the order of 10 pA.

Two subthreshold techniques were used in this research. In one technique, the subthreshold relationship given by Sze [37] is used to obtain the portion of the threshold voltage shift due to interface states. This relationship gives the change of interface state density as a function of the change in the subthreshold slope and is shown in equation 2.1 as:

$$S = (k*T/q)(\ln 10)(1+Cd/Ci) \qquad (2.1)$$

where S is the subthreshold slope of the I-V curve in mV/decade in current, Cd is the depletion capacitance, and Ci is the oxide capacitance. If interface states are present, then their capacitances would add in parallel with the depletion capacitance so that Cd in the above equation would be replaced by Cd+Cit where Cit is the capacitance due to interface states. The subthreshold slope will change with dose as interface states buildup. When S after irradiation is subtracted from S before irradiation Then:

$$del\ S = (k*T/q)(\ln 10)(del\ Cit/Ci) \qquad (2.2)$$

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but

$$Cit=q*Dit \quad\quad (2.3)$$

Substituting and solving for del Dit yields

$$del\ Dit=del\ S*Ci/(k*T*ln10) \quad\quad (2.4)$$

The change in threshold voltage due to interface states (del Vit) would just be:

$$del\ Vit=del\ Dit/Ci=del\ S/(k*T*ln10) \quad\quad (2.5)$$

The contribution to the threshold voltage shift from oxide trapped charge (del Vot) is obtained by subtracting the voltage shift due to interface states from the shift in threshold voltage since:

$$del\ Vth=del\ Vot + del\ Vit \quad\quad (2.6)$$

The threshold voltage is obtained by extrapolating the square root of drain current vs gate voltage to zero current. The corresponding gate voltage is the threshold voltage.

The other subthreshold technique extrapolates the subthreshold I-V curves to the "midgap" current value. At midgap there is no contribution to the voltage shift from interface states since they are in the neutral condition. Therefore, the shift in gate voltage at the midgap current is due just to hole trapping. Therefore

$$del\ Not=del\ Vmg*Ci/q=del\ Vot*Ci/q \quad\quad (2.7)$$

where del Not is the change in trapped holes, and del Vmg is the radiation induced change in the subthreshold voltage required to produce the midgap current. The voltage shift due to interface states is just the threshold voltage shift minus the shift due to trapped holes.

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CHAPTER III

EXPERIMENTAL PROCEDURE

Device Characterization Techniques

Pre- and post-radiation characteristics in both saturation and subthreshold regions of operation were obtained on an HP4145 parameter analyzer. The information on voltage steps and current measurements was passed from the HP4145 to an HP computer (9816 or 9836) for storage on floppy disks over an HPIB interface. The HP computer was also used to set up the HP4145 over the HPIB bus. Remarks on the disk stored with the I-V data included the lot and wafer number of the device under test as well as the dose information. The file names used for data storage were the device number prefixed by the dose.

As a general rule, the voltage on the gate on the n-channel devices was swept from +3 volts to -3 volts in 100 steps with 10 volts applied to the drain. The source and p-well contacts were tied together for all measurements on n-channel devices. The measurements were made in a small electromagnetically shielded box so that the currents could be measured down to 10^{-11} ampere range before reaching the noise and leakage limits of the measurement. For p-channel devices, the gate voltage was swept from -5 volts to +5 volts in 100 steps with -10 volts applied to the drain. Because of the large shifts in interface states and trapped holes caused by the radiation, the testing voltages often had to be adjusted following large doses and annealing experiments. The substrate and source were tied to ground.

Each device characterization took approximately two minutes so that as much as one hour could have lapsed from the time the first sample was characterized and the time the last sample was characterized. To check for annealing effects during characterization, the first pair of MOSFETs tested was recharacterized after the completion of the tests to see how much shift had occured during the testing. Since the transistors were not biased and at room temperature while waiting to be tested, minimal shifts were expected. The experiments confirmed this expectation with shifts of only a few hudreths of a volt for the recharacterized devices.

MOS Devices Used

The transistors used in these experimental investigations were n and p-channel MOSFET test transistors on SA3000 die (the Sandia National Laboratory radiation hardened version of the Intel 8085 microprocessor). These circuits use 4 micron minimum feature sizes with 3 micron channel lengths in a CMOS process with approximately 450 Å gate oxide thickness. The MOS transistors are four terminal devices without any static protection on the gate contact. The die were mounted in 24 pin ceramic dual in-line packages. The transistors were on reject SA3000 die but from wafers that had normal yield so that the individual test transistors were expected to be good. During preradiation characterization, the devices were screened for functionality and gate leakage current. Leaky and non-functional transistors were not used. Since the die were from a high reliability fabrication facility and the experiments did not generally require long time stress at elevated temperatures and biases, mobile ion

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contamination was not considered to be a possible problem in these experiments.

The transistors used in each experiment were from the same lot and wafer, but several different processing lots, wafers, and packaging lots were used in this research program. Most of the MOSFETs used in these experiments were fabricated using essentially the standard radiation hardened 4/3 micron process of Sandia National Laboratories. One group of devices were deliberately processed in a minimum hydrogen process to reduce the radiation caused interface state buildup.

Radiation Sources

The radiation source used for the first set of experiments and the last set of experiments was a gamma cell 220 at Sandia National Laboratories. This cell has a cylindrical irradiation volume eight inches high with a six inch diameter. The exposure volume moves on an elevator into a lead shielded Cobalt-60 ring for exposure and up out of the cell for test device installation. The geometry of the cell allows devices to be tested on the end of approximately five feet of cable. For the second and third experiments a contoured lead dose leveler was installed in the gamma cell. The dose lever reduces the dose rate to 56% of the unattenuated dose rate but reduces the dispersion in dose across the radiation volume from 20% to 5%. The cell delivers a 10^6 rad (Si) dose in approximately 98 minutes when unattenuated and in 175 minutes with the dose leveler installed.

The other radiation source used in these experiments was the Gamma Irradiation Facility (GIF) at Sandia National Laboratories.

This facility can irradiate much larger volumes than the gamma cell 220 and was therefore used for the experiments where thirty MOSFET pairs were irradiated simultaneously in a controlled temperature environment. This facility uses water to shield the experimenter during experiment set up. After the experiment was set up and shielding doors were in place, the Co^{60} source was raised out of the water to expose the samples.

All experiments were to total doses of approximately 1 Mrad(Si) as determined by knowing the dose rate of the source. The doses were the same within each experiment but doses between experiments performed using the two different sources could differ by thirty percent. Also since transistors and measurement techniques differ from the two sets of experiments, data comparisons are strictly valid only within an experiment set.

Effect Demonstration Experiments

The first set of three experiments was performed in the low dose rate gamma cell 220 at Sandia National Laboratories. The objective of the first experiment was to see if the observation of Dressendorfer [2] could be reproduced. For this experiment, SA3000 die bonded by Mulitus Associates were used. The dose leveler was not installed in the gamma cell for the first experiment. For the second experiment, the test transistors were bonded by Sandia National Laboratories and the dose lever was installed in the gamma cell. For each of these first three experiments, seven packages were irradiated simultaneously. Each package contained an n-channel and a p-channel MOSFET. During the irradiations, one pair of MOSFETs was biased "on,"

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one pair was biased "off" and five other pairs were alternately biased "on" and "off" at frequencies between 5 Hz and 10 Mhz. The alternating bias was supplied from a series of MC14017 CMOS decade dividers and MC14049 buffers using a 10 volt power supply. After doses of 3×10^4, 1×10^5, 3×10^5, and 1×10^6, the I-V characteristics of the devices were measured using an HP 4145 transistor analyzer. The measurements were made within 30 minutes of reaching the dose level and the circuits were returned to the bias fixture in the gamma cell after characterization until a Mrad(si) dose was accumulated.

The test devices from the third experiment were placed under post irradiation continuous bias at 100 °C to see if the ultimate interface state density after rebound was greater for MOSFETs irradiated under alternating bias. The frequencies used for the first two experiments were 5Mhz, 500khz, 50khz, 5khz, 500hz, on, and off. For the third experiment, the frequencies were 10Mhz, 5khz, 500hz, 50hz, 5hz, on, and off. For all experiments, the source, drain, and substrate (or p-well) were tied together and the bias was applied to the gate. For the n-channel MOSFETs, the "on" bias was +10 volts while the p-channel "on" bias was -10 volts. The 5Mhz and 10Mhz biases were supplied directly by a 50 ohm waveform generator driven through a short length of 50 ohm coaxial cable terminated in a 50 ohm carbon resistor in the gamma cell. The voltage amplitude and offset voltage were carefully set to insure that the peak voltage of the alternating bias matched the power supply. The CMOS MC14049 buffers that supplied the switching biases used the same 10 volt power supply so that no voltage offset between the fixed and alternating biases was possible. The

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bias was supplied through unterminated coaxial cable from the CMOS buffers. The rise time of the pulse was approximately 200ns.

Temperature, Bias, Process Experiments

The second set of experiments was intended to provide information on the functional dependence of the switching frequency, the temperature, bias voltage, and hydrogen in the oxide, on the alternating bias effect. For these experiments, the MOSFETs were irradiated to approximately a one Mrad dose with no intermediate measurements. The dose was achieved in a 91 minute irradiation. Temperature control was maintained by immersing the test transistors (enclosed in several layers of plastic bags to maintain dryness) in temperature controlled water in a ten gallon aquarium. For 0 °C irradiations, an ice-water bath was maintained in the aquarium. For 60 °C irradiations, the preheated water was maintained at the required temperature by two 60 watt bimetal thermostatically controlled aquarium heaters.

To obtain data on a finer frequency mesh, MC140XX CMOS binary dividers were used to obtain measurements at over three points per decade in frequency. Also, the range of frequencies was expanded to include frequencies from 0.015 hz to 1 Mhz. The biases for these experiments were supplied over approximately 10 feet of 40 conductor ribbon cable. Ground lines were used between the pulse bias lines at the frequencies over 100khz to minimize cross talk.

Switching Experiments

An additional experiment set was performed to look at the limiting low frequency, switching the bias half way through the

radiation. These experiments were also performed in the Sandia National Laboratory gamma cell 220. The test transistors were radiated to a half Mrad dose, characterized, the bias switched, and the radiation continued. These experiments also included devices radiated in the "on" and "off" bias conditions as well as switching between "on" and "off" at a 50 Hz rate. The devices were annealed at 100 °C to measure the interface state density following complete annealing of the trapped holes.

CHAPTER IV

EXPERIMENTAL RESULTS

Alternating Bias Effect

The results of these experiments verified the basic observation
of Dressendorfer [2] and showed that the primary source of the
observed effect is due to enhanced interface state buildup and reduced
hole trapping. The observation of his paper that at frequencies below
10 khz the threshold voltage shift in the alternating bias parts falls
between "off" and "on" was not seen even at frequencies as low as
0.015hz.

Table I presents the data on the radiation induced threshold
voltage shift as well as the shift due to interface states and trapped
holes for the n-channel devices in the first set of experiments.
Similar data for p-channel devices is given in table II. The shift
observed during the 67 hour 100 °C 8.3 volt biased anneal is also
given in these tables. Figure 4.1 is a plot of this data for
n-channel MOSFETS biased "on," "off," and switched at 50hz between
"on" and "off." Figure 4.2 shows similar plots for P-channel devices.
All of the alternating bias parts had a more positive shift than the
static bias devices for all frequencies in the range of 5 hz to 10
Mhz. The alternating bias MOSFETs tend to buildup interface states
like they are "on" all of the time while the hole trapping is like
they are "off" all the time. The result is a positive shift in the
threshold voltage of the alternating biased MOSFETs.

The devices maintained at constant 8.3 volt DC bias at elevated

TABLE I
EFFECT DEMONSTRATION EXPERIMENTS - N-CHANNEL DATA

BIAS		3E4	1E5	3E5	1E6	67HRS
ON	(Vth)	-0.14+0	-0.35+.01	-0.62+.05	-0.72+.03	2.17
	(Vot)	-0.28+.01	-0.70+0	-1.39+.01	-2.54+.04	-0.45
	(Vit)	0.14+.01	0.36+.01	0.78+.04	1.84+.01	2.62
OFF		-0.27+.01	-0.48+.01	-0.40+.03	0.12+0	2.80
		-0.36+.01	-0.74+.03	-1.02+.01	-1.30+.03	0.47
		0.09+.03	0.26+.01	0.61+.01	1.42+.03	2.34
10MHZ		-0.13	-0.29	-0.28	0.22	2.82
		-0.28	-0.66	-1.15	-1.73	0.30
		0.15	0.36	0.87	1.96	2.52
5MHZ		-0.11	-0.28	-0.28	0.27	
		-0.23	-0.62	-1.03	-1.47	
		0.12	0.34	0.76	1.74	
500KHZ		-0.11	-0.23	-0.16	0.48	
		-0.21	-0.51	-0.82	-1.08	
		0.10	0.27	0.66	1.57	
50KHZ		-0.10	-0.18	-0.04	0.83	
		-0.22	-0.52	-0.90	-1.23	
		0.13	0.34	0.86	2.06	
5KHZ		-0.12+.01	-0.24+.01	-0.12+.01	0.68+.03	2.84
		-0.26+.01	-0.58+.01	-0.94+0	-1.29+.01	0.25
		0.14+.01	0.34+.01	0.82+0	1.97+.01	2.59
500HZ		-0.14+.01	-0.26+0	-0.15+.03	0.81+.04	3.20
		-0.28+0	-0.64+0	-1.25+.28	-1.50+.07	0.28
		0.14+.01	0.38+0	1.10+.24	2.31+.11	2.92
50HZ		-0.14	-0.24	-0.03	0.94	3.32
		-0.31	-0.70	-1.14	-1.58	0.43
		0.17	0.45	1.10	2.53	2.89
5HZ		-0.15	-0.27	-0.13	0.72	3.00
		-0.30	-0.69	-1.11	-1.55	0.27
		0.16	0.42	0.98	2.26	2.72

TABLE II
EFFECT DEMONSTRATION EXPERIMENTS - P-CHANNEL DATA

BIAS		3E4	1E5	3E5	1E6	67HRS
	(Vth)	-0.05+.00	-0.15+.00	-0.37+.01	-0.75+.01	-0.71
ON	(Vot)	-0.05+.00	-0.14+.01	-0.36+.01	-0.71+.01	-0.46
	(Vit)	-0.00+.00	-0.01+.00	-0.01+.00	-0.04+.00	-0.25
		-0.29+.01	-0.59+.02	-1.06+.03	-2.09+.09	-1.58
OFF		-0.27+.01	-0.50+.01	-0.84+.02	-1.46+.06	-0.63
		-0.02+.01	-0.08+.01	-0.23+.01	-0.63+.02	-0.95
		-0.24	-0.19	-0.24	-0.38	-0.49
10MHZ		-0.21	-0.16	-0.18	-0.28	-0.16
		-0.02	-0.03	-0.06	-0.10	-0.33
		-0.04	-0.10	-0.16	-0.28	
5MHZ		-0.04	-0.09	-0.14	-0.23	
		-0.00	-0.01	-0.02	-0.05	
		-0.05	-0.11	-0.17	-0.28	
500KHZ		-0.04	-0.10	-0.15	-0.22	
		-0.00	-0.01	-0.02	-0.06	
		-0.05	-0.13	-0.22	-0.41	
50KHZ		-0.05	-0.11	-0.20	-0.32	
		-0.00	-0.02	-0.02	-0.09	
		-0.08+.01	-0.20+.02	-0.30+.02	-0.60+.06	-0.76
5KHZ		-0.08+.00	-0.19+.02	-0.26+.02	-0.48+.04	-0.30
		-0.01+.00	-0.02+.01	-0.05+.01	-0.12+.01	-0.46
		-0.12+.00	-0.27+.01	-0.45+.02	-0.76+.03	-0.89
500HZ		-0.12+.01	-0.25+.01	-0.39+.02	-0.60+.04	-0.36
		-0.00+.00	-0.03+.01	-0.06+.01	-0.16+.01	-0.53
		-0.16	-0.35	-0.57	-0.95	-1.04
50HZ		-0.15	-0.32	-0.50	-0.75	-0.42
		-0.01	-0.03	-0.07	-0.19	-0.62
		-0.17	-0.37	-0.59	-0.94	-1.00
5HZ		-0.16	-0.34	-0.51	-0.74	-0.41
		-0.01	-0.03	-0.08	-0.20	-0.59

27
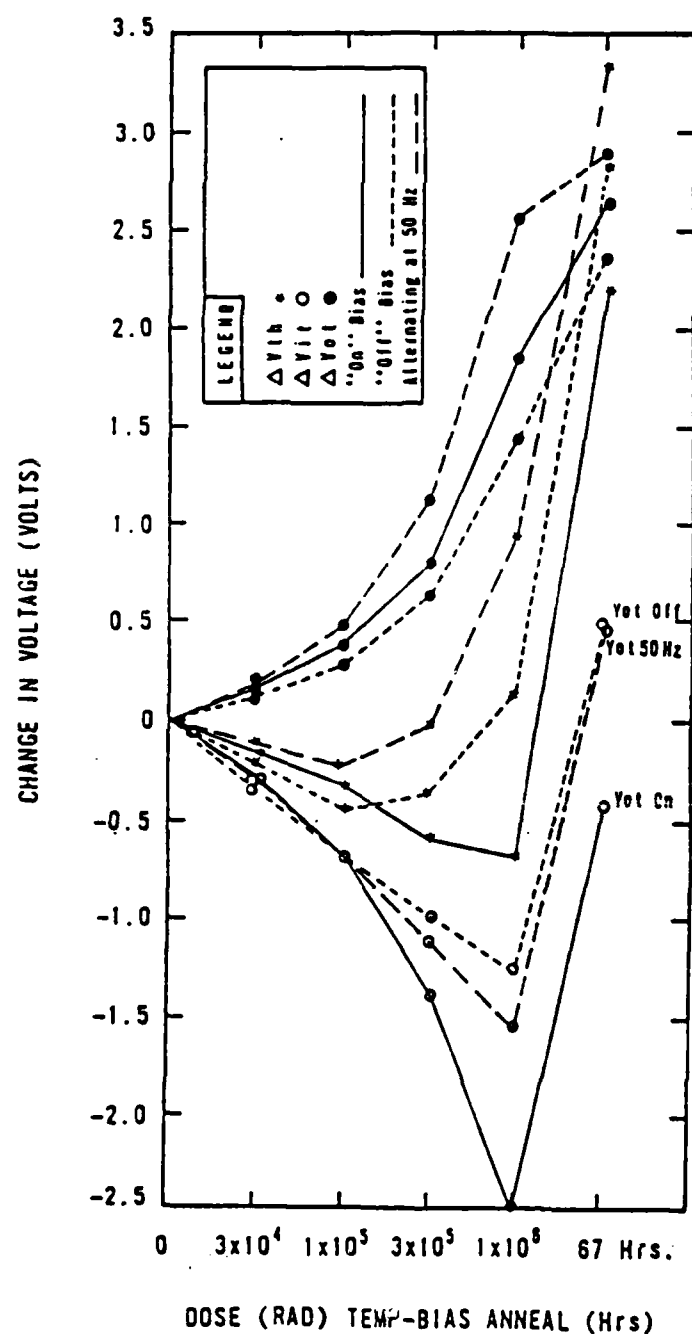
Figure 4.1 Threshold voltage shift with components due to trapped holes and interface states for N-channel MOSFETs biased "on," "off," and switched between "on" and "off" at a 50 Hz rate followed by an 8.3 volt, 100 °C anneal.

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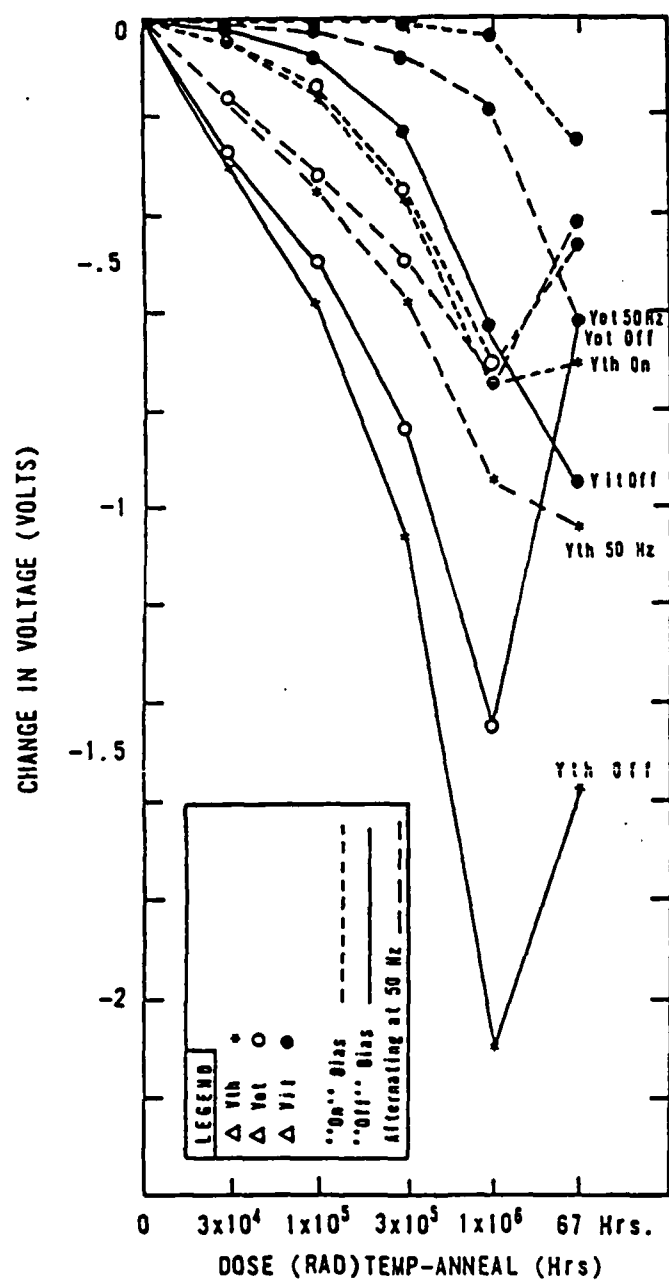
Figure 4.2 Threshold voltage shift with components due to trapped holes and interface states for P-channel MOSFETs biased "on," "off," and switched between "on" and "off" at a 50 Hz rate followed by an 8.3 volt, 100 °C anneal.

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temperature (100 °C) for three days exhibited classic rebound. The rebound results are also shown in figures 4.1 and 4.2. As can be seen in these figures, the MOSFET irradiated under alternating bias has a half volt more interface state voltage shift at the end of the irradiation and maintain that half volt more interface states through the anneal. Therefore, parts irradiated under alternating bias could fail sooner due to rebound than parts irradiated under static bias.

Figures 4.3 and 4.4 show the threshold voltage shift after 1 Mrad as a function of the applied bias frequency. Also shown in these figures are the components of the threshold voltage shift due to interface state build up and hole trapping. Figure 4.3 clearly shows that the alternating bias causes hole trapping to be like "off" hole trapping while interface state buildup is like "on" interface state buildup. These two effects combine to cause the threshold voltage shift for the alternating biased parts to be more positive than either static biased case. Figure 4.3 also shows that alternating bias causes a substantial increase in interface state buildup at lower frequencies. These figures also show the alternating bias effect to be more pronounced at lower frequency for both n and p channel MOSFETs. The two peaks in the n-channel threshold voltage and interface state voltage curves of figure 4.3 suggested the possibility of a resonance effect in the alternating bias frequency. The possibility was suggested by Dr Patrick Lenahan of Sandia National Laboratories that the peak at 50 hz could be due to a hydrogen transport resonance and the peak at 50 khz could be due to a hole transport resonance.

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3

Vit Pulsed
Vit_On − − − − − − − − − −
Vit_Off − − − − − − − − − −

2

1

Vth_Off − − − − − − − − −

0

Vth_On − − − − − − − − −

−1

Vot_Off − − − − − − − − −
Vot Pulsed

−2

Vot_On − − − − − − − − − −

−3

VOTAGE CHANGE (VOLTS)

10^0 10^1 10^2 10^3 10^4 10^5 10^6 10^7

PULSED BIAS FREQUENCY (Hz)
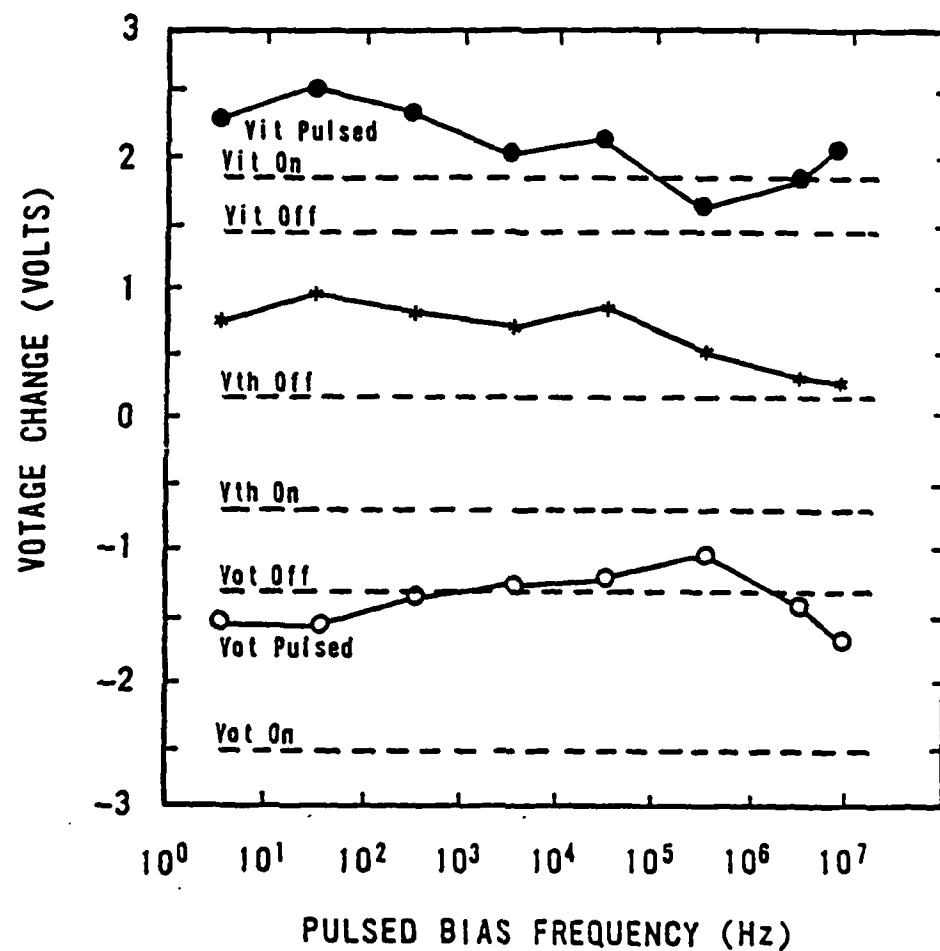
Figure 4.3   Threshold voltage shift with components due to trapped holes and interface states vs alternating bias frequency for N-channel MOSFETs after a 1 Mrad radiation dose.
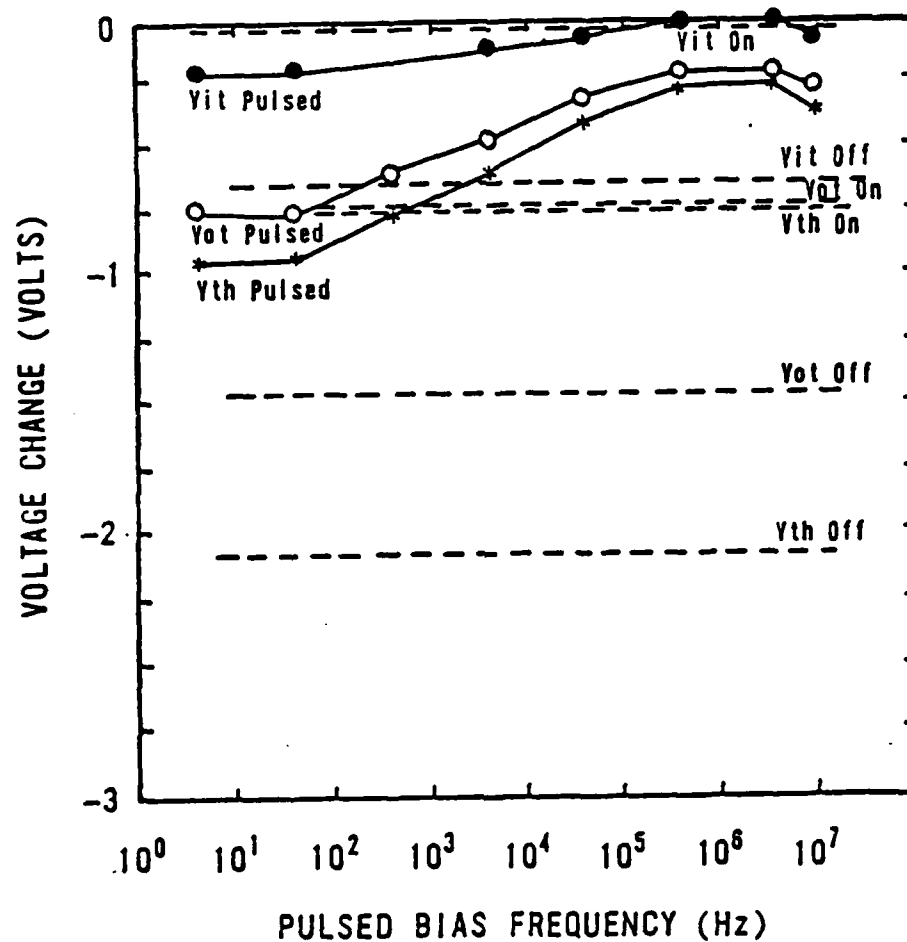
Figure 4.4   Threshold voltage shift with components due to trapped holes and interface states vs alternating bias frequency for P-channel MOSFETs after a 1 Mrad radiation dose.

Figure 4.5 compares the two subthreshold conductance techniques for obtaining the contributions to the threshold voltage shift due to trapped holes and interface states. The subthreshold swing technique seems to under estimate the trapped hole and interface state density. This under estimation is due to the decrease in the slope of the subthreshold curves at the lowest current levels. The subthreshold swing technique gives slighly more reproducible results with a 3% deviation among measurements while the extrapolation to midgap technique gives a 5% deviation. Figure 4.6 gives the subthreshold curves for the n-channel device alternatingly biased on and off at 50 Hz. Notice the change in the subthreshold conductance curves at low currents.

Temperature, Process, Bias Effects

The design of the second set of experiments was largely motivated by a test of the temperature and alternating bias voltage effects on the location of the peaks. If they were transport time resonances, then changing the temperature should change the transport time constants and move the location of the peaks. The amount of shift would then provide a more direct measurement of the transport time constants in silicon dioxide.

Table III gives the n-channel data from the second set of experiments while Table IV gives the data for the p-channel devices. For these experiments, the devices were irradiated to a dose of approximately one Mrad(si) with no intermediate measurements. The data from these experiments is plotted in Figures 4.7 through 4.14. The relative effects of temperature, hydrogen in the process, and

33
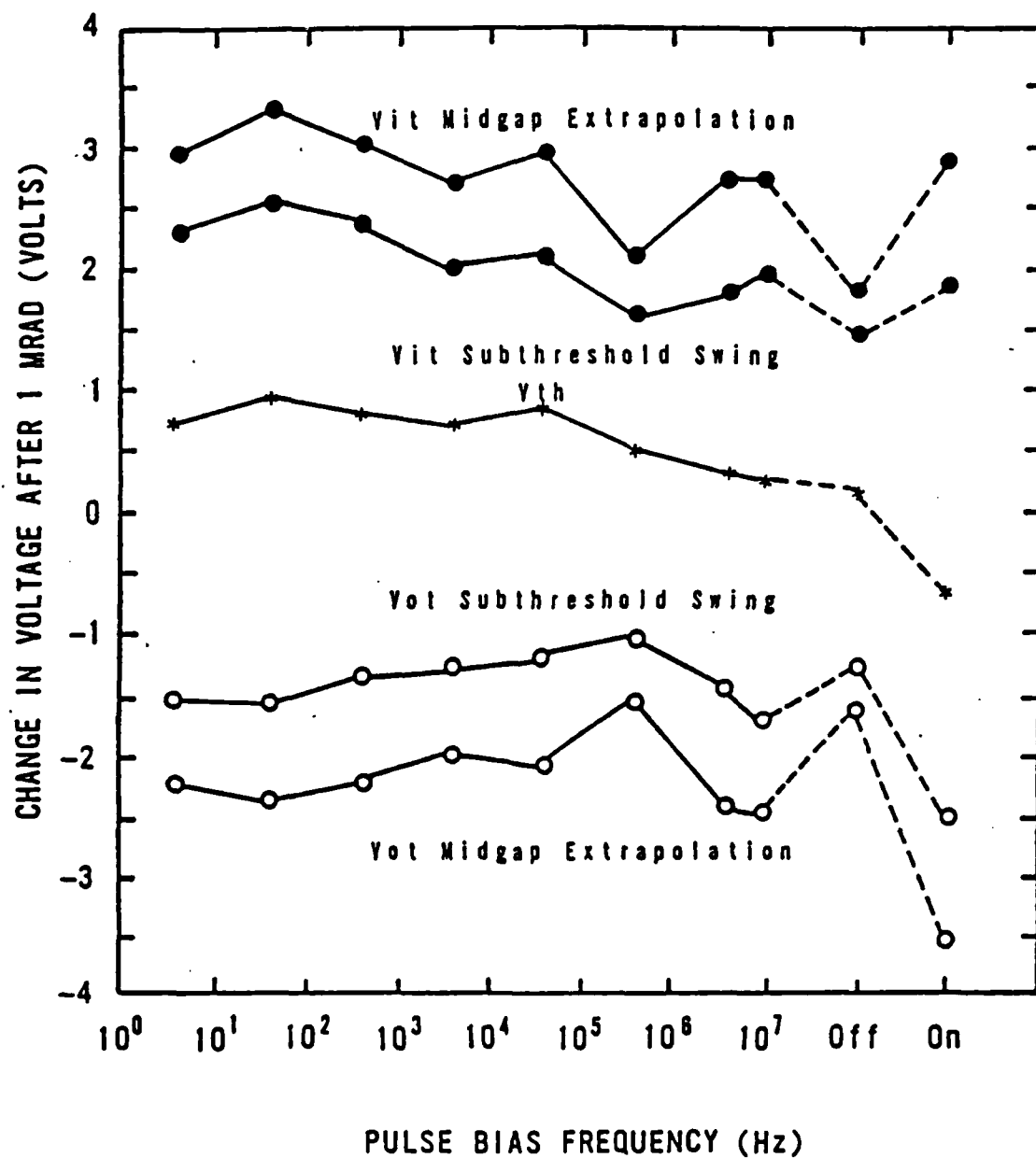
Figure 4.5 Comparison of the two subthreshold conductance techniques for determining the trapped hole and interface state components of the threshold voltage shift.

34
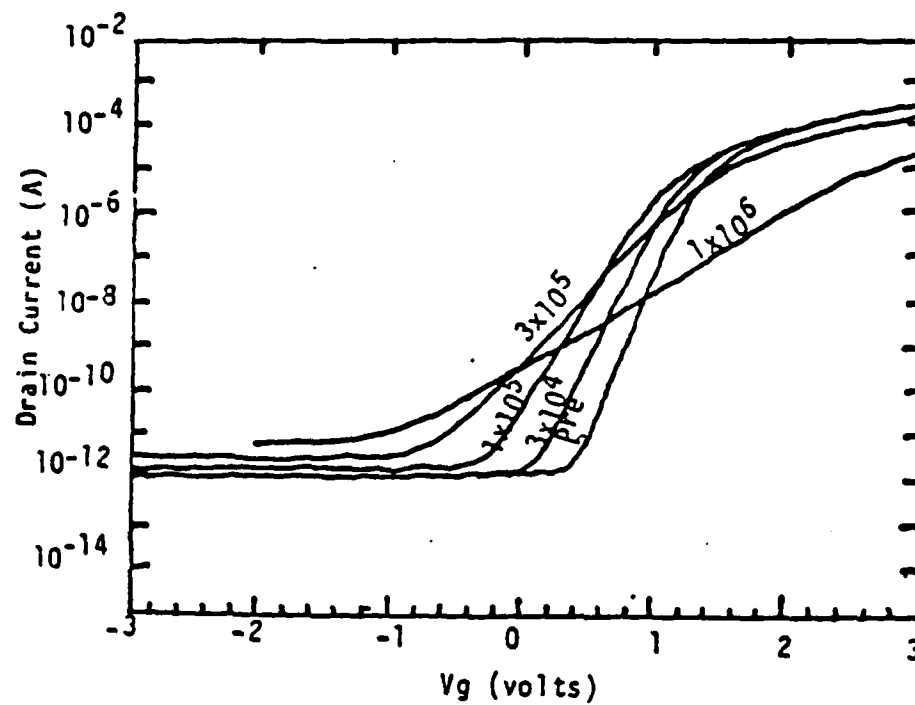
Figure 4.6   Subthreshold I-V curves for an N-channel MOSFET
alternatinly biased "on" and "off" at 50 Hz after several
radiation doses.

TABLE III
TEMPERATURE, HYDROGEN, BIAS EFFECT EXPERIMENTS
N-CHANNEL DATA

Temp	64 °C	4 °C	4 °C	4 °C
Process	Standard	Standard	Reduced H	Reduced H
Bias	10	10	3	10
on (Vth)	1.09	−0.44	−0.66	−0.79
(Vot Vit)	−1.92 3.01	−2.93 2.48	−1.58 0.92	−1.62 0.83
off	1.13	0.61	0.07	0.04
	−0.80 1.93	−0.84 1.45	−0.70 0.77	−0.86 0.90
reverse	0.17	−0.10	0.29	−0.09
	−0.03 0.19	−0.19 0.09	0.08 0.21	−0.17 0.08
1.0E6	1.58	0.61	−0.49	0.03
	−0.67 2.25	−0.67 1.28	−1.42 0.93	−0.82 0.84
5.0E5	1.64	0.58	----	−0.08
	−0.90 2.54	−0.69 1.27	---- ----	−0.94 0.86
2.5E5	1.46	0.84	−0.32	----
	−0.89 2.35	−0.58 1.42	−1.19 0.87	---- ----
1.2E5	1.54	0.61	----	0.07
	−0.87 2.41	−0.63 1.24	---- ----	−0.76 0.83
6.3E4	1.52	0.61	−0.10	−0.32
	−0.78 2.30	−0.91 1.52	−1.14 1.04	−1.04 0.72
3.1E4	1.41	0.60	----	−0.13
	−1.05 2.46	−0.80 1.40	---- ----	−1.16 1.02
1.6E4	1.79	0.62	−0.20	0.07
	−0.96 2.74	−0.86 1.48	−1.14 0.94	−0.75 0.82
7.8E3	1.66	0.59	0.00	−0.01
	−1.04 2.70	−0.84 1.43	−1.01 1.00	−0.98 0.97
3.9E3	1.69	0.67	0.05	0.08
	−1.02 2.71	−0.87 1.55	−1.14 1.19	−0.85 0.93
2.0E3	2.12	0.72	0.11	0.05
	−1.38 3.50	−0.85 1.57	−0.97 1.08	−0.78 0.83
9.8E2	1.90	0.98	0.10	−0.05
	−1.22 3.12	−1.13 2.10	−0.89 0.99	−0.91 0.87
4.9E2	----	0.44	----	0.02
	---- ----	−1.12 1.56	---- ----	−1.22 1.24
2.4E2	1.85	0.58	0.08	−0.38
	−1.12 2.97	−1.07 1.65	−1.04 1.13	−1.45 1.08
1.2E2	1.88	1.75	0.00	0.07
	−1.18 3.05	−0.46 2.21	−1.05 1.05	−0.86 0.92
6.1E1	1.75	0.636	−0.01	0.07
	−1.27 3.02	−1.15 1.78	−1.09 1.07	−1.08 1.15
3.0E1	1.86	0.65	−0.11	0.14
	−1.27 3.13	−1.45 2.10	−1.01 0.90	−0.96 1.09
1.5E1	1.85	0.41	0.05	0.07
	−1.28 3.13	−1.52 1.94	−1.09 1.14	−1.00 1.06
7.6E0	1.75	0.80	−0.06	−0.02
	−1.33 3.08	−1.49 2.29	−1.03 0.97	−1.06 1.04
3.8E0	1.75	0.68	−0.20	0.11
	−1.33 3.09	−1.22 1.90	−1.16 0.96	−1.16 1.27
1.9E0	1.63	1.02	−0.09	0.08
	−1.19 2.82	−1.35 2.37	−1.09 1.01	−1.40 1.48

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TABLE III (cont.)
TEMPERATURE, HYDROGEN, BIAS EFFECT EXPERIMENTS
N-CHANNEL DATA

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Temp	64 °C	4 °C	4 °C	4 °C
Process	Standard	Standard	Reduced H	Reduced H
Bias	10	10	3	10
9.5E-1	1.78	0.79	0.02	0.18
	-1.33 3.11	-1.28 2.06	-1.01 1.03	-0.99 1.16
4.8E-1	1.99	1.03	0.08	0.08
	-1.25 3.23	-1.10 2.13	-1.01 1.09	-1.22 1.30
2.4E-1	1.68	1.49	0.09	0.20
	-1.32 3.00	-0.84 2.33	-0.91 1.00	-1.12 1.32
1.2E-1	1.66	0.71	0.16	0.12
	-1.26 2.92	-1.58 2.30	-0.96 1.12	-1.36 1.48
6.0E-2	1.86	0.84	0.08	----
	-1.24 3.10	-1.39 2.23	-0.93 1.01	---- ----
3.0E-2	1.97	0.69	-0.04	-0.24
	-1.50 3.48	-1.34 2.03	-0.91 0.88	-1.46 1.22
1.5E-2	1.51	1.08	-0.06	0.10
	-1.54 3.04	-1.12 2.21	-1.06 1.00	-1.35 1.46

<div align="center">

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TABLE IV
TEMPERATURE, HYDROGEN, BIAS EFFECT EXPERIMENTS
P-CHANNEL DATA

Temp Process Bias	64 °C Standard 10	4 °C Standard 10	4 °C Reduced H 3	4 °C Reduced H 10
on (Vth)	−0.87	−0.92	−0.28	----
(Vot Vit)	−0.63 −0.25	−0.70 −0.22	−0.24 −0.03	---- ----
off	−2.15	−1.54	−0.86	−0.88
	−0.56 −1.58	−0.76 −0.78	−0.63 −0.23	−0.63 −0.25
reverse	−3.10	−3.09	−2.40	----
	−1.56 −1.08	−2.33 −0.76	−1.97 −0.42	---- ----
1.0E6	−0.36	−0.29	−0.29	−0.15
	−0.14 −0.22	−0.13 −0.16	−0.19 −0.10	−0.12 −0.03
5.0E5	−0.42	−0.33	----	−0.16
	−0.16 −0.26	−0.17 −0.16	---- ----	−0.12 −0.04
2.5E5	−0.40	−0.37	−0.24	----
	−0.16 −0.25	−0.13 −0.24	−0.16 −0.08	---- ----
1.2E5	−0.51	----	----	−0.18
	−0.21 −0.30	---- ----	---- ----	−0.14 −0.03
6.3E4	−0.43	−0.39	−0.13	−0.18
	−0.21 −0.23	−0.18 −0.21	−0.04 −0.09	−0.14 −0.04
3.1E4	----	−0.38	----	−0.22
	---- ----	−0.19 −0.19	---- ----	−0.16 −0.06
1.6E4	−0.54	−0.44	−0.28	----
	−0.26 −0.28	−0.22 −0.21	−0.19 −0.09	---- ----
7.8E3	−0.67	−0.44	----	−0.26
	−0.33 −0.34	−0.24 −0.21	---- ----	−0.20 −0.07
3.9E3	−0.65	----	−0.37	−0.29
	−0.33 −0.32	---- ----	−0.24 −0.13	−0.22 −0.07
2.0E3	−1.04	−0.57	−0.43	−0.31
	−0.48 −0.56	−0.33 −0.24	−0.67 −1.10	−0.25 −0.06
9.8E2	−0.84	−0.70	−0.36	−0.30
	−0.38 −0.46	−0.36 −0.34	−0.25 −0.11	−0.23 −0.07
4.9E2	----	----	----	−0.49
	---- ----	---- ----	---- ----	−0.34 −0.15
2.4E2	−0.89	----	----	0.10
	−0.44 −0.45	---- ----	---- ----	0.37 −0.28
1.2E2	−0.85	−0.99	----	----
	−0.38 −0.46	−0.53 −0.46	---- ----	---- ----
6.1E1	----	−0.82	----	−0.50
	---- ----	−0.50 −0.33	---- ----	−0.38 −0.12
3.0E1	−0.89	−1.03	----	----
	−0.42 −0.47	−0.54 −0.49	---- ----	---- ----
1.5E1	----	−0.93	----	----
	---- ----	−0.59 −0.34	---- ----	---- ----
7.6E0	−0.91	−1.01	−0.49	−0.42
	−0.47 −0.44	−0.60 −0.42	−0.35 −0.14	−0.32 −0.10
3.8E0	----	−0.92	----	−0.63
	---- ----	−0.59 −0.33	---- ----	−0.48 −0.14
1.9E0	−1.56	−0.96	−0.49	−0.67
	−1.25 −0.31	−0.61 −0.34	−0.34 −0.15	−0.48 −0.19

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TABLE IV (cont.)
TEMPERATURE, HYDROGEN, BIAS EFFECT EXPERIMENTS
P-CHANNEL DATA

Temp Process Bias	64 °C Standard 10		4 °C Standard 10		4 °C Reduced H 3		4 °C Reduced H 10	
9.5E-1	----		-1.05		----		-0.59	
	----	----	-0.61	-0.44	----	----	-0.47	-0.12
4.8E-1	-1.07		-0.92		-0.53		----	
	-0.48	-0.58	-0.59	-0.33	-0.36	-0.17	----	----
2.4E-1	-1.11		-0.93		-0.50		----	
	-0.51	-0.60	-0.53	-0.41	-0.36	-0.14	----	----
1.2E-1	----		-0.90		----		-0.69	
	----	----	-0.58	-0.33	----	----	-0.50	-0.19
6.0E-2	-0.95		-1.20		-0.51		----	
	-0.56	-0.39	-0.63	-0.57	-0.37	-0.15	----	----
3.0E-2	-1.22		----		-0.48		-0.66	
	-0.41	-0.81	----	----	-0.35	-0.13	-0.48	-0.17
1.5E-2	-1.32		-1.05		-0.53		----	
	-0.59	-0.72	-0.56	-0.49	-0.38	-0.15	----	----

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CHANGE IN VOLTAGE (VOLTS)

4

3 — △ Vit On
— △ Vit Pulsed
— △ Vit Off

2 — △ Vth Pulsed
— △ Vth Off

1 — △ Vth On

0

-1 — △ Vot Off
— △ Vot Pulsed

-2 — △ Vot On

-3

-4

10^{-2} 10^{-1} 10^{0} 10^{1} 10^{2} 10^{3} 10^{4} 10^{5} 10^{6}

PULSE BIAS FREQUENCY (Hz)

Figure 4.7   Threshold voltage shift with components due to trapped holes and interface states vs alternating bias frequency for N-channel MOSFETs at 64° C, standard process and 10 volt bias after a 1 Mrad dose.

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Figure 4.8 Threshold voltage shift with components due to trapped holes and interface states vs. alternating bias frequency for N-channel MOSFETs at 0° C, standard process and 10 volt bias after a 1 Mrad dose.

41

Figure 4.9 Threshold voltage shift with components due to trapped holes and interface states vs alternating bias frequency for N-channel MOSFETs at 0° C, reduced hydrogen process and 10 volt bias after a 1 Mrad dose.

42

Figure 4.10 Threshold voltage shift with components due to trapped holes and interface states vs alternating bias frequency for N-channel MOSFETs at 0° C, reduced hydrogen process and 3 volt bias after a 1 Mrad dose.

43
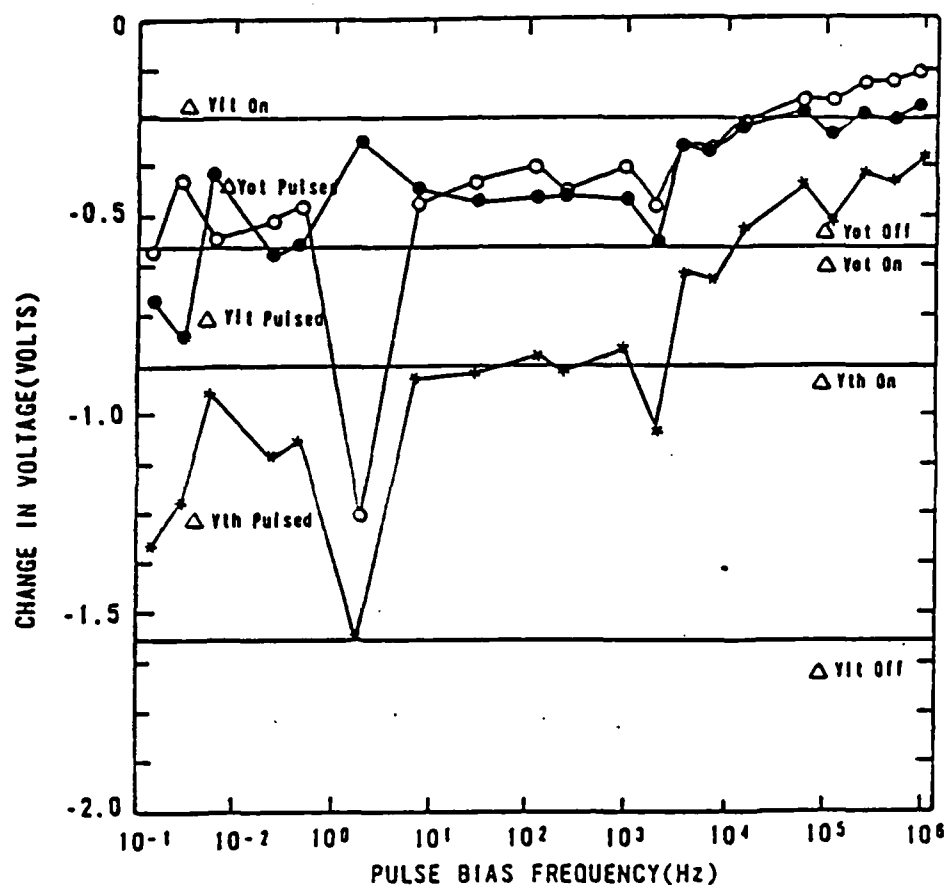
Figure 4.11 Threshold voltage shift with components due to trapped holes and interface states vs alternating bias frequency for P-channel MOSFETs at 64° C, standard process and 10 volt bias after a 1 Mrad dose.

44
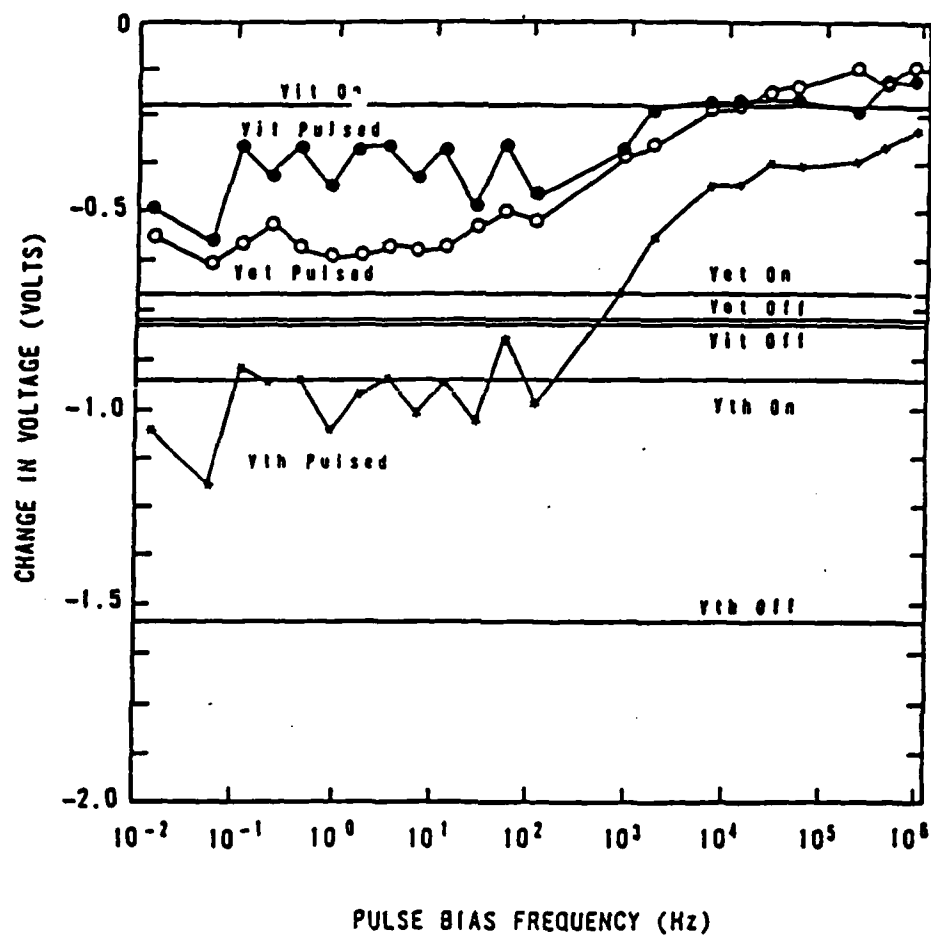
Figure 4.12 Threshold voltage shift with components due to trapped holes and interface states vs alternating bias frequency for P-channel MOSFETs at 0°C, standard process and 10 volt bias after a 1 Mrad dose.

45
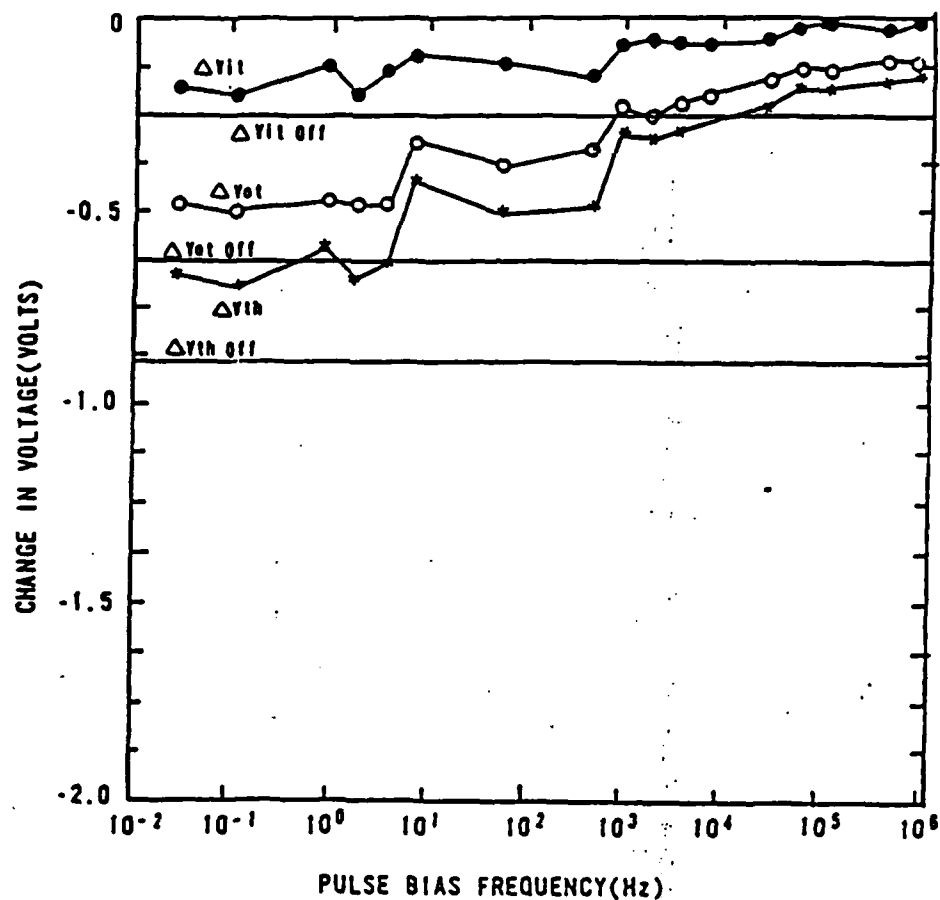
Figure 4.13 Threshold voltage shift with components due to trapped holes and interface states vs alternating bias frequency for P-channel MOSFETs at 0° C, reduced hydrogen process and 10 volt bias after a 1 Mrad dose.
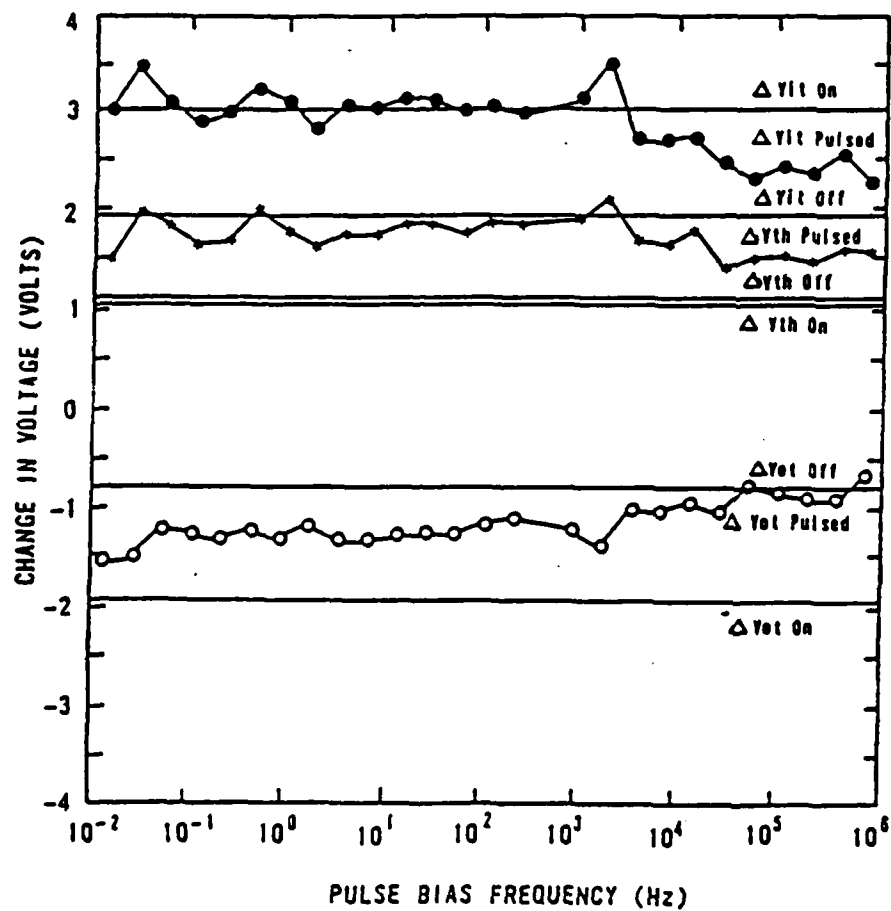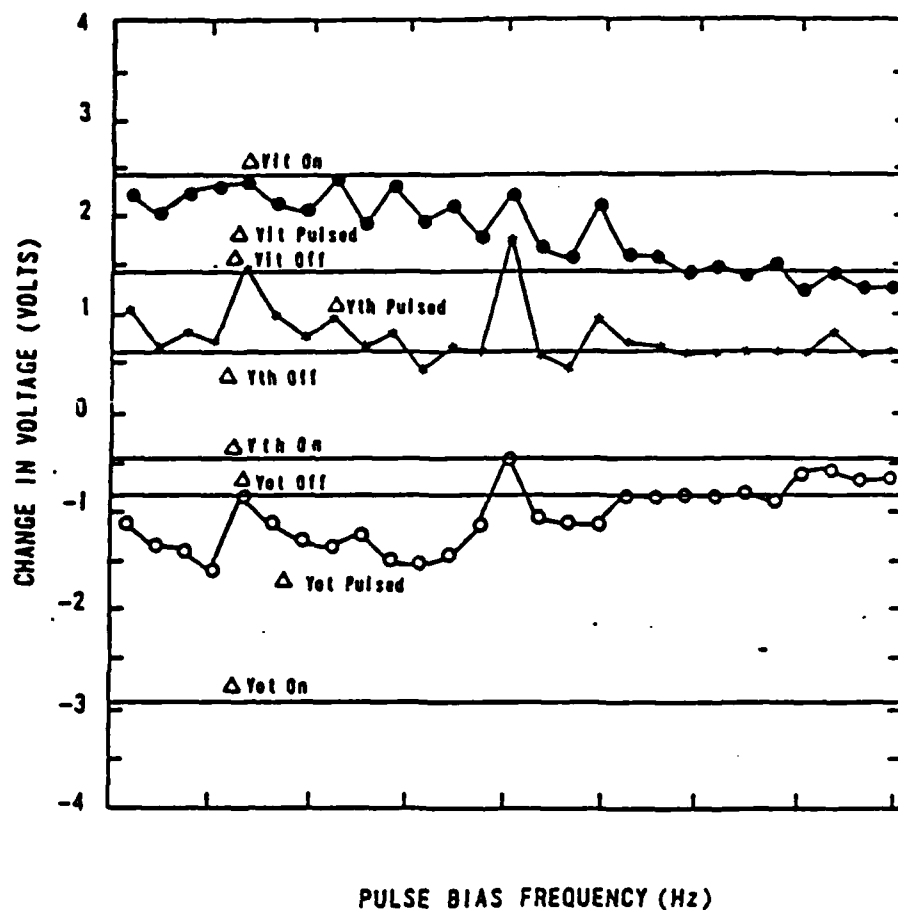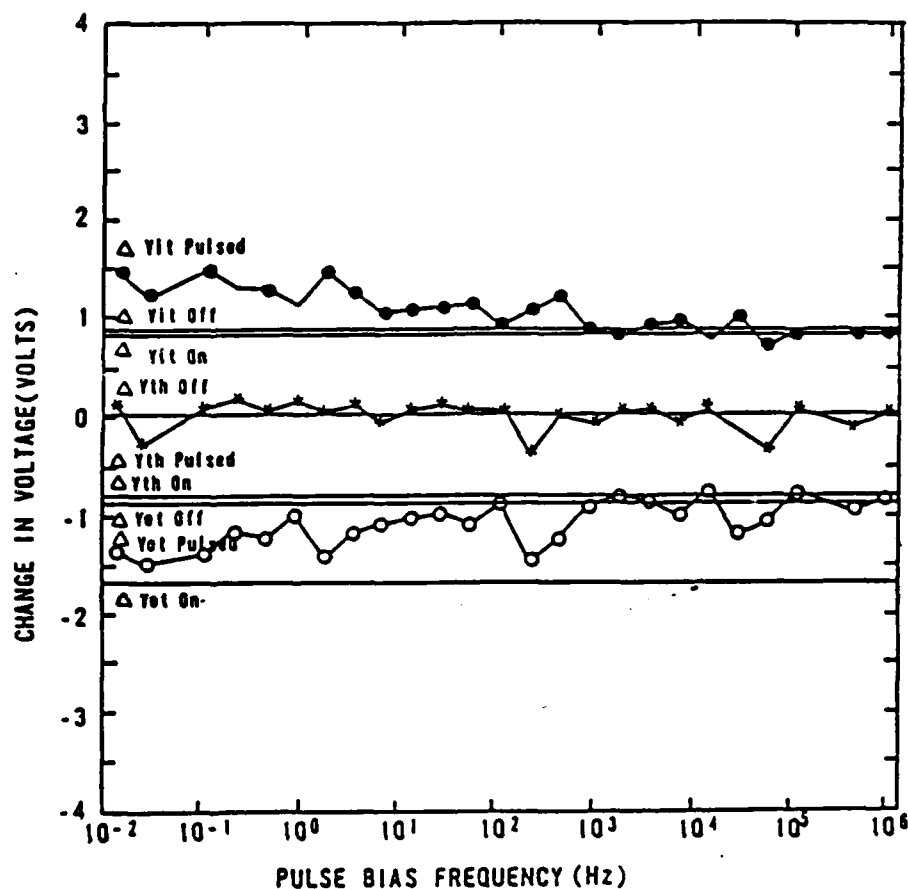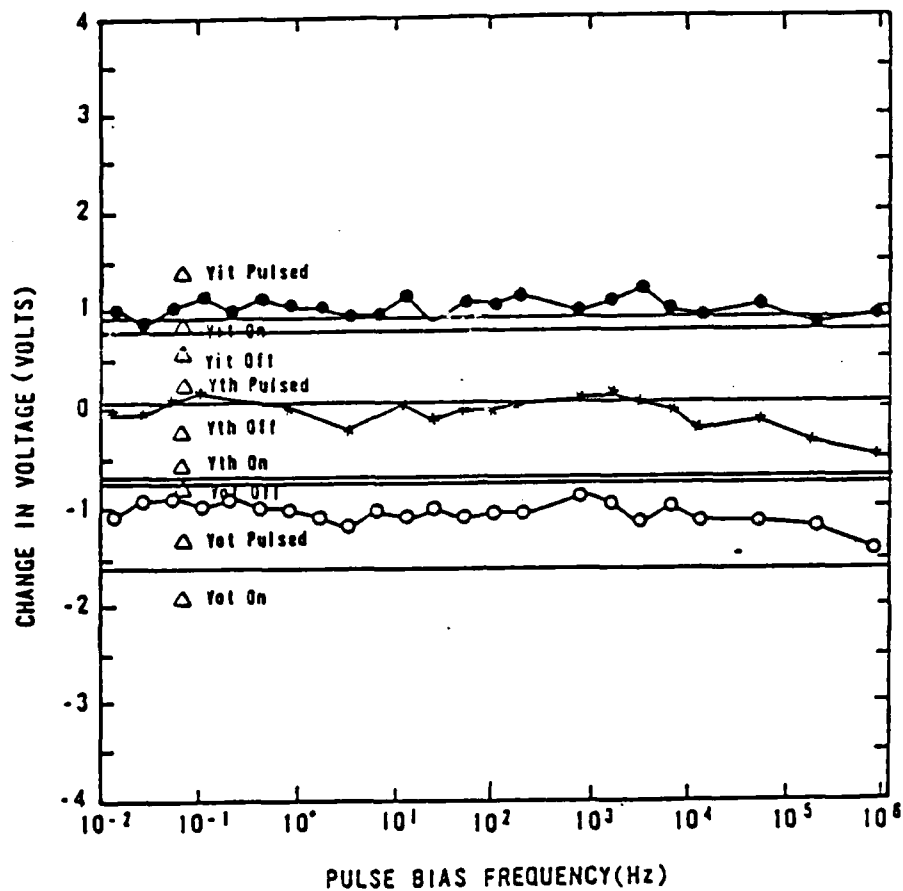
46
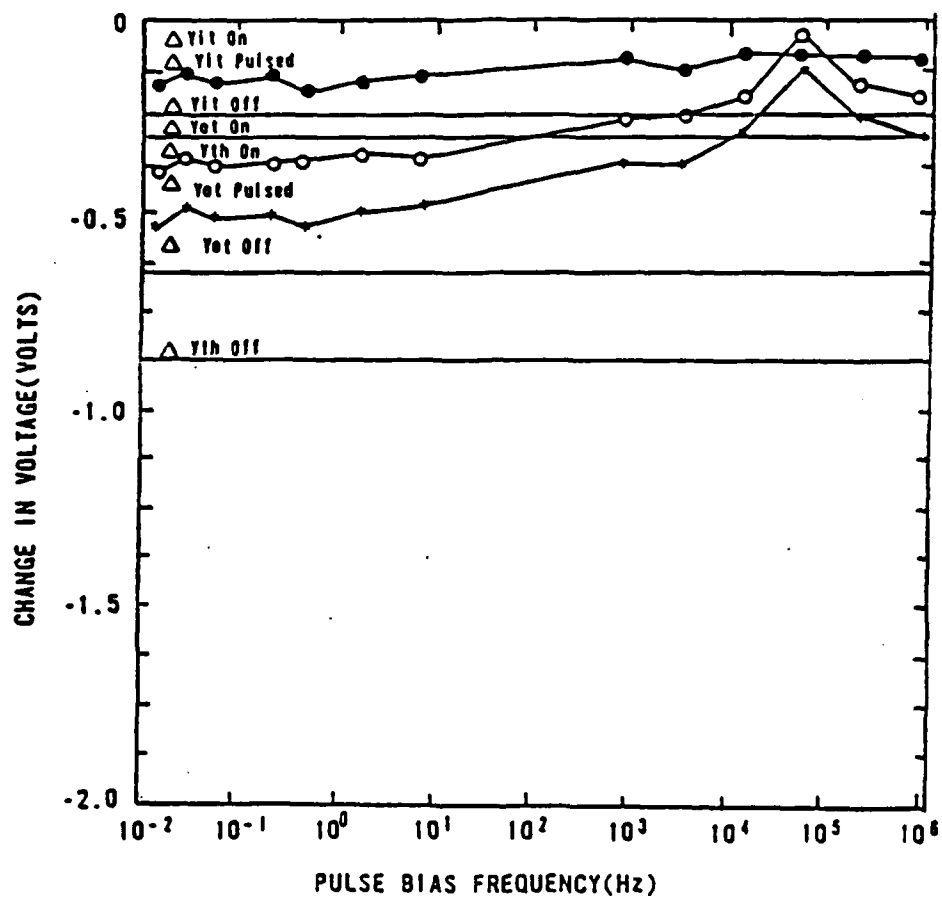
Figure 4.14 Threshold voltage shift with components due to trapped holes and interface states vs alternating bias frequency for P-channel MOSFETs at $0°C$, reduced hydrogen process and 3 Volt bias after a 1 Mrad dose.

47

reducing the bias are most easily understood by overlaying the figures. Comparison of low and high temperature effects on the n-channel devices revealed 50% more "on" hole trapping at the lower temperature with no change in the "off" and alternating bias hole trapping. The interface state buildup was a volt less for the alternating bias parts and a half volt less for "on" and "off" biases. The reduced-hydrogen parts had less hole trapping for the "on" case, with little difference in hole trapping for the "off" and alternating biased cases. "On" interface states were 1.5 volts less for the reduced hydrogen process, while the off and alternating bias cases had approximately 0.5 volt less interface states for the reduced-hydrogen parts. Reducing the applied bias to three volts made very little difference in the response except to reduce the frequency dependence on the alternating bias response. A summary of these results is given in Table V.

Switching Results

The last set of experiments clearly showed that switching the bias from "on" to "off" halfway through the irradiation caused a radiation enhanced annealing of the trapped holes and additional interface state buildup. For the n-channel MOS devices switched from "off" to "on" the interface state buildup and hole trapping increased. The part switched between "on" and "off" at 50 Hz showed the expected increase in interface state buildup and decrease in hole trapping. Annealing of these devices at 100 $^\circ$C showed that the n-channel MOS FETs alternately biased "on" and "off" had greater interface state buildup after all the holes had annealed than the devices maintained

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TABLE V

RESULTS SUMMARY FOR TEMPERATURE, HYDROGEN, BIAS
EFFECTS EXPERIMENTS

	N-Channel	P-Channel

Temperature
Reduced from
64 °C to 4 °C
	Hole Trapping
	Off Pulsed-NC
	On-increased 50 %
	  Interface State
	On Off-1/2 V less
	Pulsed-1V less
		Hole Trapping
		On Pulsed-NC
		 Off-increased
		  Interface States
		On Pulsed-NC
		 Off-1/2

Hydrogen Reduced	Hole Trapping Off Pulsed-NC On-reduced Interface States On-reduced 1 1/2 V Off Pulsed -reduced 1/2 V	Hole Trapping Pulsed-Reduced 20% Off-reduced Interface States Off-reduced to 1/3 Pulsed-reduced 50%
Bias Reduced 10 V to 3 V	Frequency Dependence – Reduced	Frequency Dependence – Reduced

"on" continuously through the radiation and anneal. The annealing of trapped holes is much more complete for the alternating bias and switched MOSFETs. Another observation in these curves is that interface states tend to anneal at 100 °C when no bias is applied. The results of these experiments is given in figures 4.15 through 4.25.

Figure 4.15 Threshold voltage shifts with components due to trapped holes and interface states, from switching experiments - continuously "on" for radiation and anneal using N-channel MOSFET.

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Figure 4.16   Threshold voltage shifts with components due to trapped holes and interface states, from switching experiments – continuously "off" for radiation and anneal using N-Channel MOSFET.

Figure 4.17 Threshold voltage shifts with components due to trapped holes and interface states, from swiching experiments - "on" switched to "off" durring radiation followed by 10 volt, 100° C Anneal using N-channel MOSFET.

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Figure 4.18 Threshold voltage shifts with components due to trapped holes and interface states, from switching experiments - "off" switched to "on" durring radiation followed by 0 volt, 100°C anneal using N-channel MOSFET.
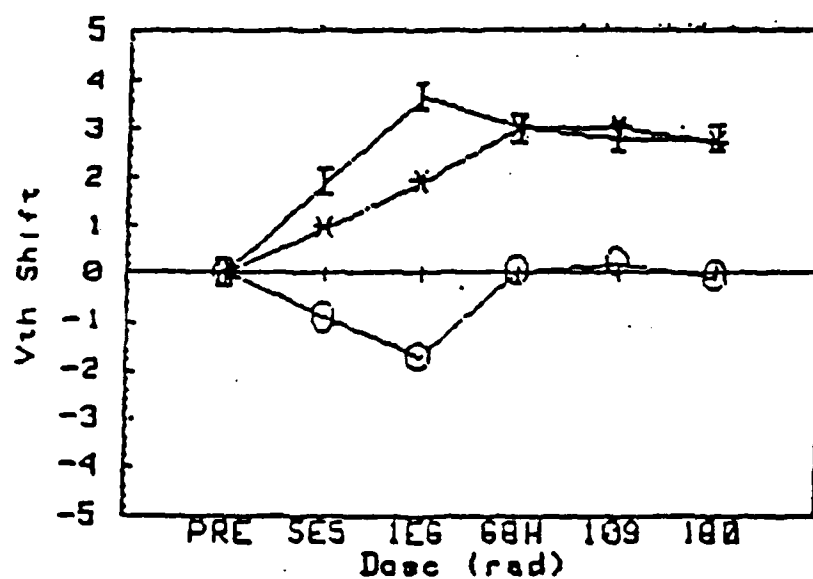
Figure 4.19 Threshold voltage shifts with components due to trapped holes and interface states, from switching experiments - alternating between "on" and "off" at 50 Hz followed by 10 Volt, 100°C anneal using N-channel MOSFET.
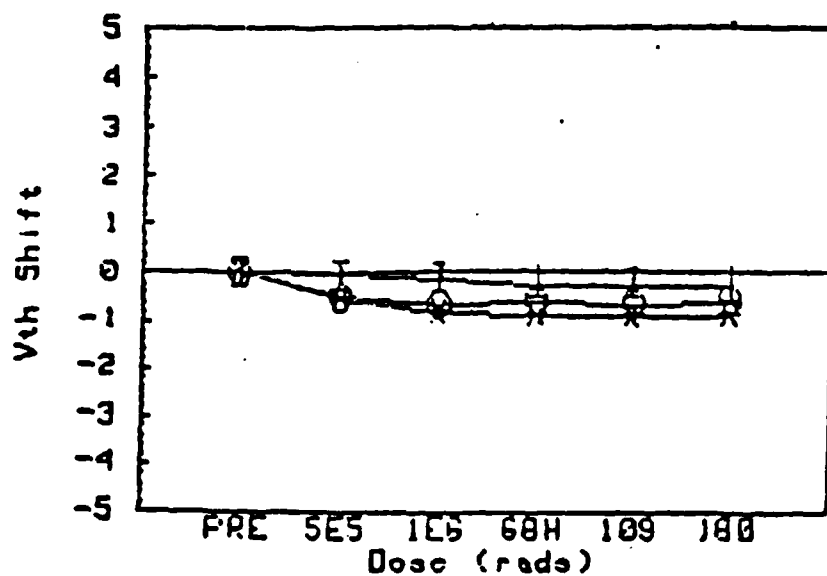
Figure 4.20   Threshold voltage shifts with components due to trapped holes and interface states, from switching experiments - continuously "on" for radiation and anneal using P-channel MOSFET.
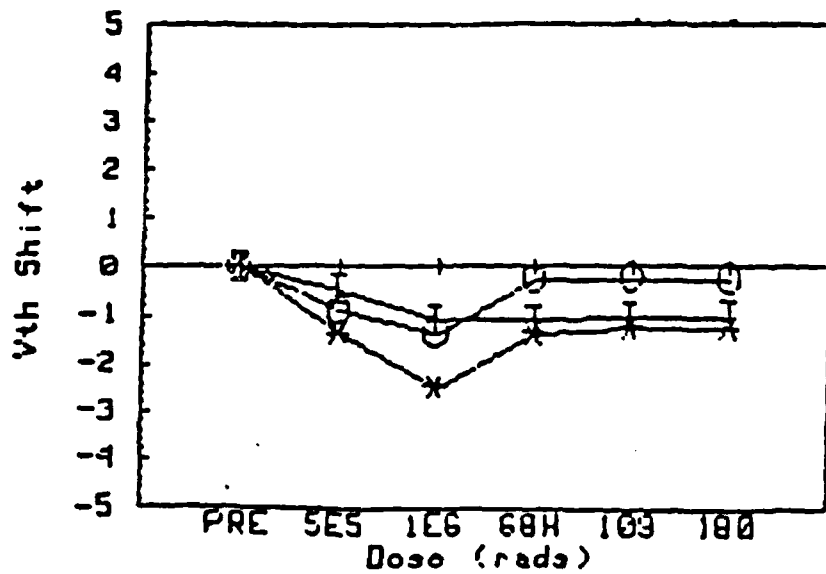
Figure 4.21 Threshold voltage shifts with components due to trapped holes and interface states, from switching experiments – continuously "off" for radiation and anneal using P-channel MOSFET.
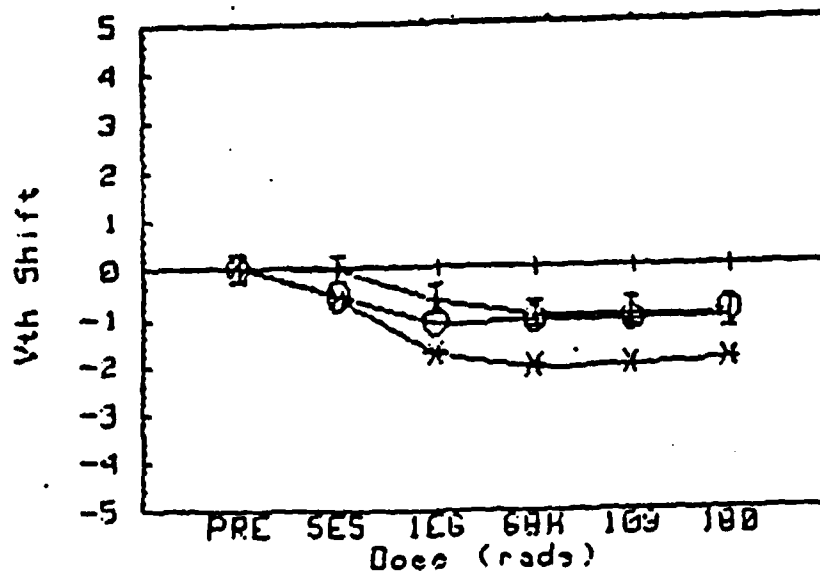
Figure 4.22 Threshold voltage shifts with components due to trapped holes and interface states, from swiching experiments - "on" switched to "off" durring radiation followed by 10 volt, 100° C anneal using P-channel MOSFET.
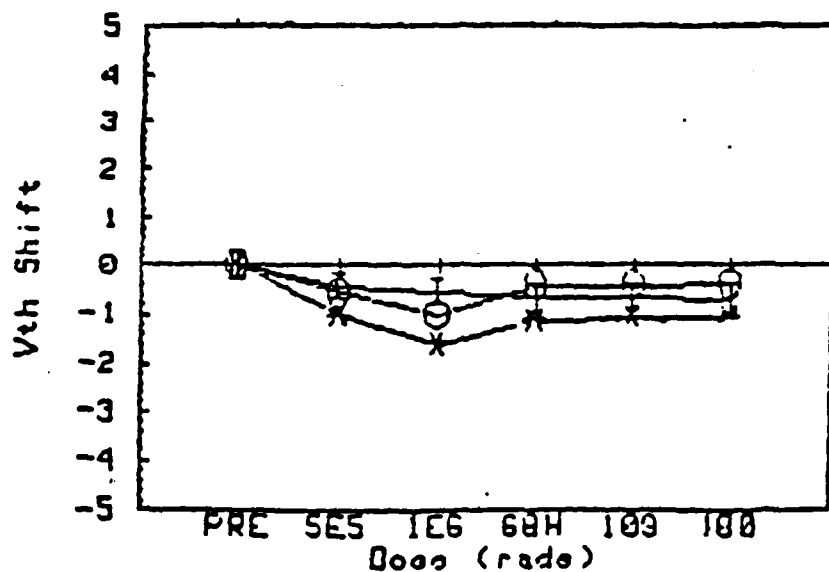
Figure 4.23 Threshold voltage shifts with components due to trapped holes and interface states, from switching experiments - "off" switched to "on" durring radiation followed by 0 volt, 100° C anneal using P-channel MOSFET.
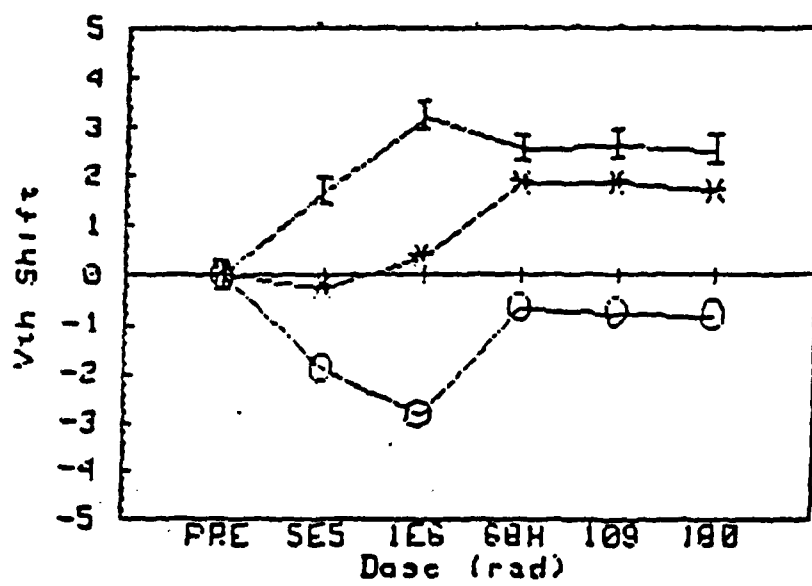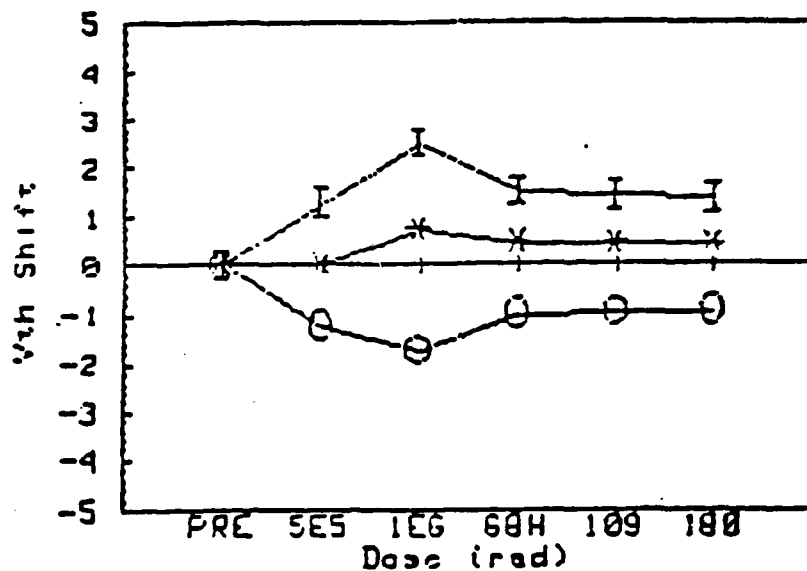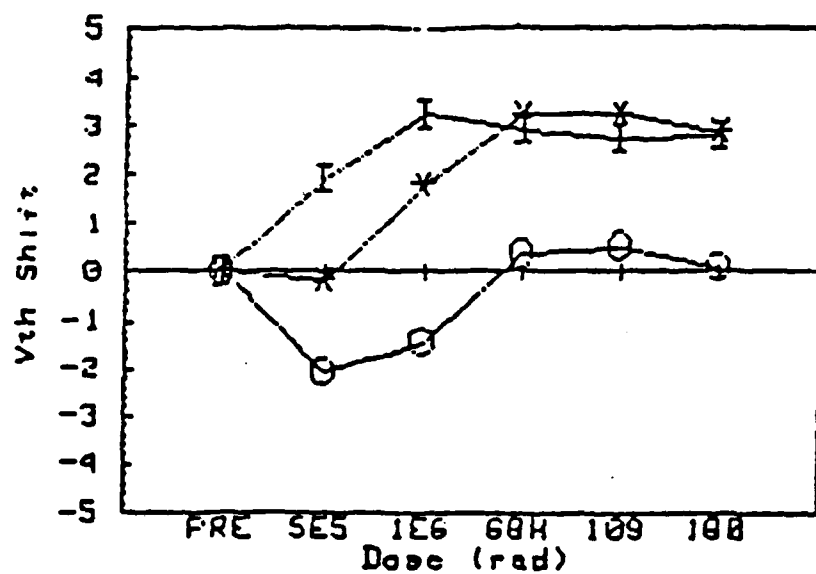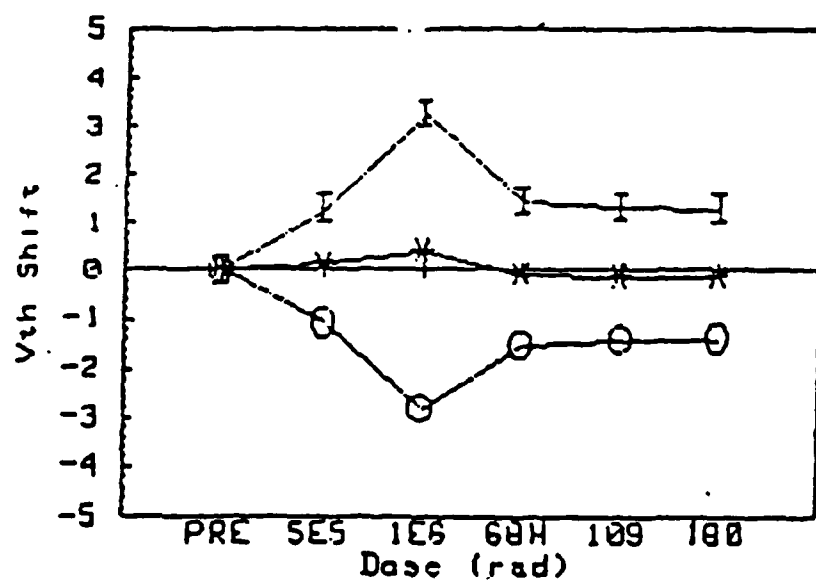
59
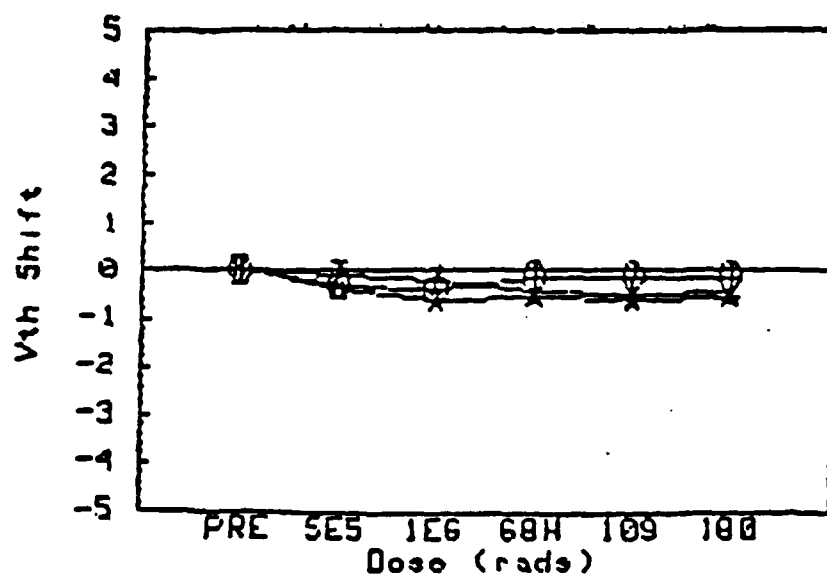
Figure 4.24 Threshold voltage shifts with components due to trapped holes and interface states, from switching experiments - alternating between "on" and "off" at 50 Hz followed by 10 Volt, 100°C anneal using P-channel MOSFET.

CHAPTER V

A MODEL FOR ALTERNATING BIAS EFFECTS

Qualitative Model

This model is based on the following observations from the radiation effects literature cited in the background section of this dissertation. The charge yield in an irradiated MOS insulator is a strong function of applied bias since an applied bias separates the electron-hole pairs reducing the initial recombination. The efficiency of trapping of holes is increased if the drift field influencing the hole is smaller since the cross section for hole trapping falls off as the reciprocal of the square root of the field. Electrons are very mobile and exit the oxide quickly (pico seconds) under the influence of an electric field. Holes are much less mobile than electrons but respond to an electric field. The presence of charge near the oxide-semiconductor interface has a much stronger effect on the threshold voltage than charge near the gate interface. Holes are trapped near (less than 50 Å) of the interfaces. An appreciable internal space charge can be developed by the trapped holes that can influence the transport of holes, and electrons. Trapped holes near the interface when annihilated by electrons become interface states. Electrons from the semiconductor can tunnel into trapped holes near the oxide-semiconductor interface under a positive gate bias. Figure 5.1 gives the bias cases considered by this model.

The basic model for the observed alternating bias effect is that holes are trapped at the oxide semiconductor interface during the positive bias portion of the irradiation, and during the zero bias

BIAS CASES

	N-Channel		P-Channel	

Starting Radiation

Vg=10 Vbi=1.1	Vg=0 Vbi=1.1	Vg=-10 Vbi=0.4	Vg=0 Vbi=0.4
Gate	Gate	Gate	Gate

Ending Radiation

Vg=10 Vbi=1.1	Vg=0 Vbi=1.1	Vg=-10 Vbi=0.4	Vg=0 Vbi=0.4
Gate	Gate	Gate	Gate

Alternating Biase

Vg=10 Vbi=1.1	Vg=0 Vbi=1.1	Vg=-10 Vbi=0.4	Vg=0 Vbi=0.4
Gate	Gate	Gate	Gate
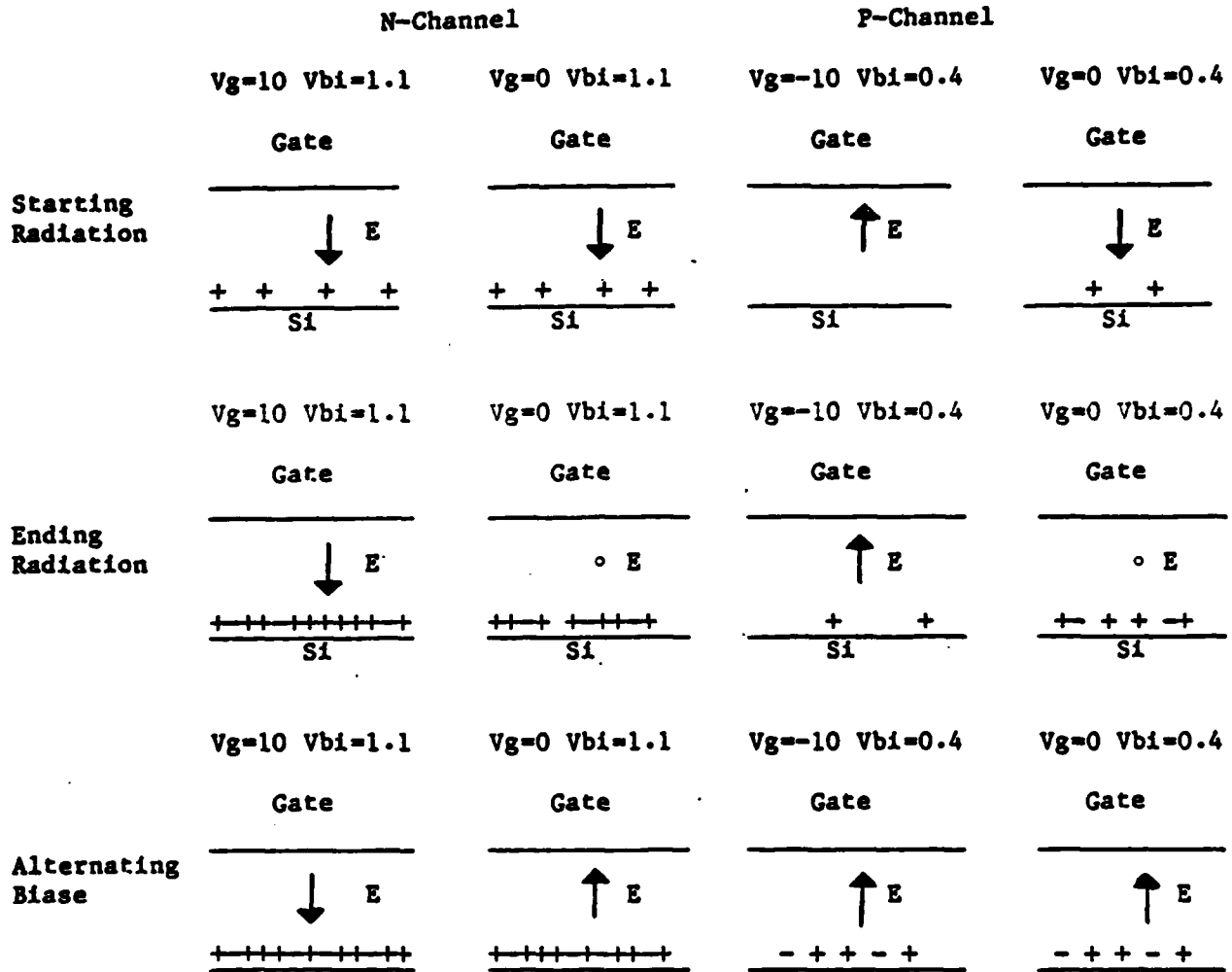
Figure 5.1 Bias cases for the alternating bias effect model

portion of the irradiation the trapped holes are annihilated by radiation produced electrons pulled to the interface by the trapped hole space charge. The annihilated holes become interface states. Thus, the alternating biased n-channel parts have more interface state buildup and less hole trapping. The swiched bias experiments strongly support this model. They show rapid annihilation of the holes trapped during the "on" portion of the irradiation when the irradiation continues with the bias removed and an increase in the interface state buildup.

Since the MOSFETs used in these experiments have n-type poly-silicon gates, the n-channel MOSFEts have a built in field of 1.1 volts with no bias applied. This field is strong enough to produce sizable hole yield but not strong enough to reduce the hole trapping at the interface. Thus, initially, the "off" bias produces more threshold shift due to hole trapping than the "on" bias. As the radiation produced space charge builds up, it compensates the built-in field decreasing the hole yield through increased initial recombination. At the same time, the space charge is reducing the effective field across the "on" biased oxide increasing the hole capture cross section. The result is that the "on" bias starts to have a more negative threshold voltage shift than the "off" bias. The electrons produced by the radiation are pulled by the trapped hole space charge to the interface where they annihilate the trapped holes producing interface states.

For n-channel MOSFETs continuously biased "on" during the radiation, the positive bias traps the holes near the interface.

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Radiation produced electrons created on the Si-SiO$_2$ interface side of the traps annihilate trapped holes and produce interface states. A secondary effect at the dose-rate of these experiments is tunneling of electrons from the silicon surface into the close traps causing annihilation of the trapped hole and producing interface states. The slight decrease in the alternating bias effect as the frequency of the alternating bias increases, results from the dispersive transport of the holes and the time required to trap some fraction of the radiation produced holes. The change in hole mobility with temperature would then just cause a shift in the frequency responce of the interface state buildup so that the effect could begin at higher frequencies at higher temperatures.

The observation of more complete annealing of the trapped holes for alternating bias and switched bias suggests a shift in the location of the trapped hole distribution under alternating bias. Under a static bias the trapped holes would go out to perhaps 50 Å from the interface. The trapped holes over 30 Å from the interface may not be accessable to tunneling electrons from the substrate. Under an alternating bias trapped holes nearest the gate would be annihilated first since the radiation produced electrons would be moving toward the substrate. Thus only the trapped holes close to the interface which are accessable to tunneling electrons would remain and rebound would be more complete following a temperature - bias anneal.

The greater post-radiation annealing of interface states with no bias applied supports the Lai model of interface state generation since the negatively charged non-bridging oxygen atom in the model

would be less likely to move toward a negatively charged interface state under positive gate bias. Under zero bias, the interface states would be neutral and would not prevent restoration of the broken strained bonds under thermal agitation.

For p-channel devices that are on continuously, the holes are pulled to the gate electrode and thus have little effect on the threshold voltage shift. Only the few holes produced very near the semiconductor interface have the possibility of being trapped there and then annihilated to produce interface states. Thus, very little interface state buildup occurs in p-channel devices biased on. For p-channel devices biased off, the 0.4 volt metal-semicondutor work function provides a slight positive bias at the gate pulling holes to the interface. Diffusion and holes created in the trapping region also contribute to the trapped hole space charge. Electrons from the irradiation get pulled into this space charge distribution, causing annihilation of trapped holes and the build up of interface states. In the alternating bias case, the holes can only drift toward the interface during the off portion of the cycle by the space charge buildup at the gate poly silicon. The alternating bias case can thus buildup trapped holes and interface states during the off portion of the cycle. At high frequencies, holes cannot get near the interface before the bias changes and the holes are pulled toward the gate. Thus, the increased alternating bias effect at lower frequencies.

Computer Simulation

A simple computer model was developed to test the qualitative model described above. This model is based on a paper by Freeman and

Holes-Siedle entitled "A Simple Model For Predicting Radiation Effects In MOS Devices[37]." This model simplifies the radiation effects modeling by assuming the holes are all trapped in a plane at a distance X1 from the silicon interface. Since experiments have shown the hole traps to be within 50 $\overset{\circ}{A}$ of the silicon interface, this simplifying assumption is not a bad one. In fact, since trapped holes are annihilated by electron tunneling, the trapped hole space charge must reside within a reasonable tunneling distance of the silicon surface or about 30 $\overset{\circ}{A}$.

In this model, the distance from the trapping plane to the gate contact is called X2, and the total thickness of the oxide is called Xox. Then, from simple electrostatics, a charge of Qox on the trapping plane would induce an image charge of Qs in the silicon surface where:

$$Qs = -X2*Qox/Xox \qquad (5.1)$$

To compensate for the image charge, a charge of -Qs must be applied to the gate. From the relationship between charge and voltage in a parallel plate capacitor, the change in voltage that must be supplied to restore the semiconductor surface to its preradiation condition is:

$$del \ Vot = Qs*Xox/(Eox*Eo) = q*Nox*X2/(Eox*Eo) \qquad (5.2)$$

where Eox is the dielectric constant of silicon dioxide, Eo is the permittivity of free space, Nox is the number of trapped holes per unit area and q is the charge on an electron. The generation rate (G) for electron-hole pair generation in SiO2 is taken to be 7.9×10^{12} $cm^{-3}rad^{-1}$. The yield of electron-hole pairs in SiO2 is known to be a

function of the applied field across the oxide separating the electron-hole pairs from initial recombination. Also, Dozier and Brown have shown that the probability of hole trapping at the interface is a function of the field across the oxide with the trapping probability falling off as $E^{-1/2}$ at fields over approximately 0.5 Mv/cm. This result is used to provide a function $Yt(E)$ that gives the fraction of the holes trapped at a given field, taking into account the $E^{1/2}$ dependence of initial hole yield and the trapping fall off at high field. Also, the collection length is a function of field since a positive gate bias will allow hole collection from the gate to the charge trapping sheet while a negative bias would result in collection over the shorter distance from the charge trapping sheet to the silicon surface. Using these relationships the holes trapped per unit area per unit dose would be:

Nox=G*Xch*Yt(E)   (5.3)

where Xch is the hole collection distance. Substituting Nox in the above relationship yields:

del Vot=-q*G*X2*Xch*Yt(E)*D/(Eox*Eo)   (5.4)

In their model Freeman and Holmes-Siedle do not allow hole annihilation or interface state formation. Since hole annihilation coupled with interface state creation is a crucial component of the qualitative model of the alternating bias effect, the model was expanded to account for these possibilities. The electrons produced by the radiation are collected over a field dependent distance called Xce. Also, electrons can tunnel into the trapped hole space charge if a positive bias is applied to the gate. These electrons annihilate a

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number of the trapped holes Anox where:

$$Anox=Nox*Z*(G*Xce*Yt*D+T)/(G*Xox*Mxi*1.E+6) \qquad (5.5)$$

In this equation, Z is the normalization factor and contains the probability of an electron annihilating a trapped hole. Mxi is the maximum trapped hole yield used in the Dozier and Brown function for hole yield vs applied electrical field. The expression in the denominator normalizes the value of Z from a number like 10^{-12} to a reasonable number. The value of Z for roughly equal probability of electron and hole trapping would be approximately 50. The sample runs of the code typically used a value of 40 for Z. T is the electron density from tunneling and is a function of the applied bias. Some fraction of the annihilated holes are assumed to become interface states. Thus, the interface state density is just:

$$Nit= Anox*Frac \qquad (5.6)$$

The threshold voltage shift from interface states would be:

$$del\ Vit=Nit*Xox*Q/(Eox*Eo) \qquad (5.7)$$

The threshold voltage would then just be the sum of the components due to trapped holes and interface states.

$$del\ Vth=del\ Vot+del\ Vit \qquad (5.8)$$

This computer model accurately predicts the effects observed in the previously described experiments of this research. For example, the results given in Figure 4.1 are qualitatively reproduced in Figure 5.2. Note that the early time "off" hole trapping is greater than the early time "on" hole trapping as was observed in the experiments. Also observe that the computer model predicts the reduced hole trapping and increased interface state buildup in the alternating bias

68
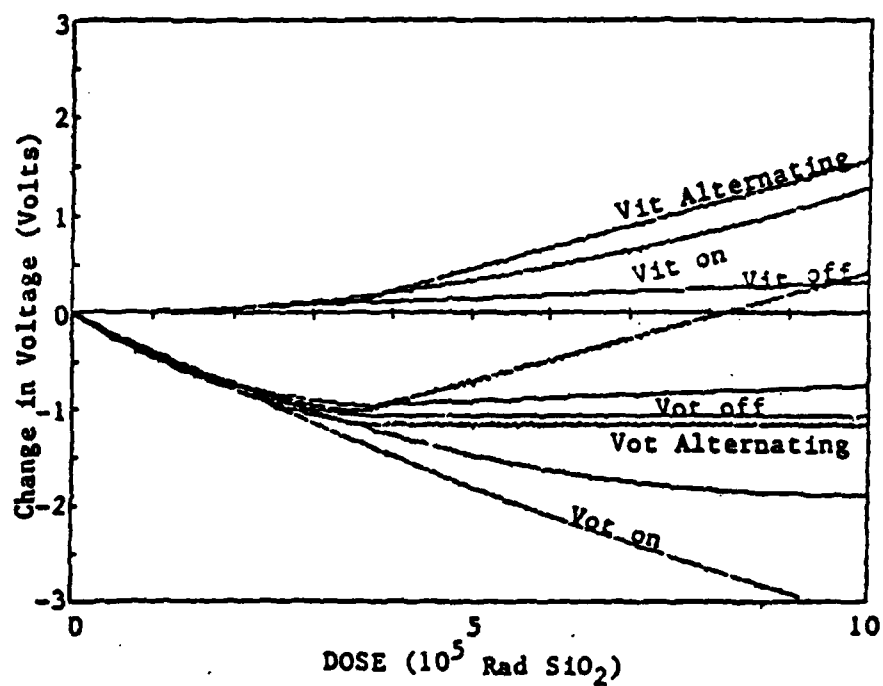
Figure 5.2   Computer simulation of N-channel MOSFETs biased "off", "on", and alternating between "on" and "off" 100 times durring the simulation to 1 Mrad.

case. The computer model predicts, with reasonable accuracy, the results of the switching experiments as is illustrated in Figure 5.3. Adjusting the possition of the hole trapping sheet shows that the alternating bias effect is stronger when the charge sheet is closer to the semiconductor interface. The best qualitative agreement between the model and the experiments results when the centroid of hole traps is located approximately 15 Å from the Si surface.

The very rapid annihilation of trapped holes predicted by the computer model when the bias is switched from "on" to "off" sugests that a larger percentage of "on" time would result in increased interface state buildup. Figure 5.4 gives the modeled response of MOSFETs irradiated with 80%, 50%, and 20% duty cycle alternating biases. The larger duty cycle produces greater interface state buildup. Also in this model, substantial interface state build up under an alternating bias is delayed until the trapped hole space charge can invert the built-in field due to the metal-semiconductor work function. By applying a bias that alternates between +10 volts and -10 volts, interface state build up could start imediately. This condition is illustrated in figure 5.5.

A detailed listing of the computer code in BASIC, based on this model, is given in Appendix A with sample runs of the program given in Appendix B.

70
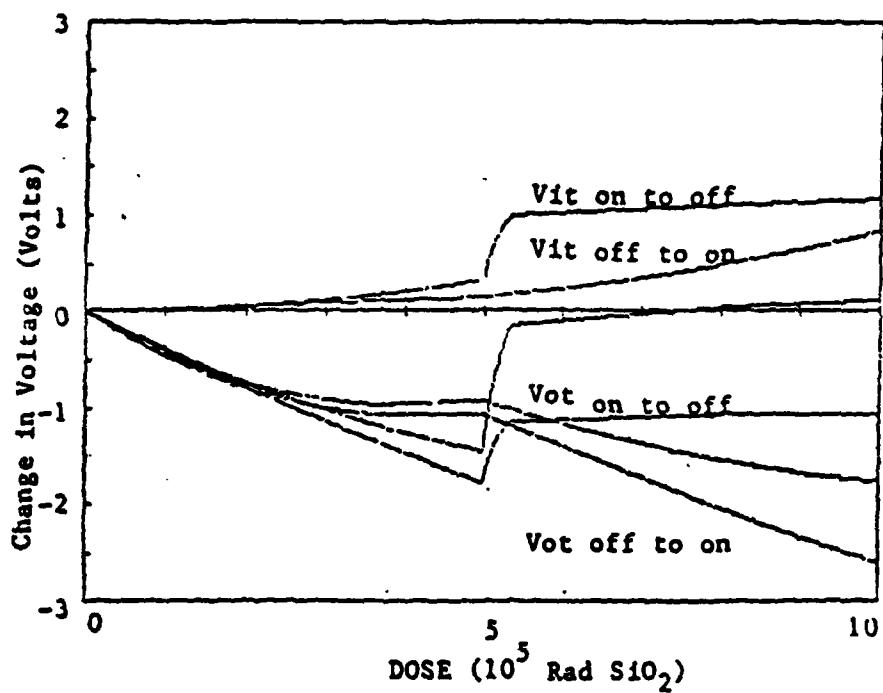
Figure 5.3 Computer simulation of N-channel MOSFETs switched from "on" to "off" and switched from "off" to "on.
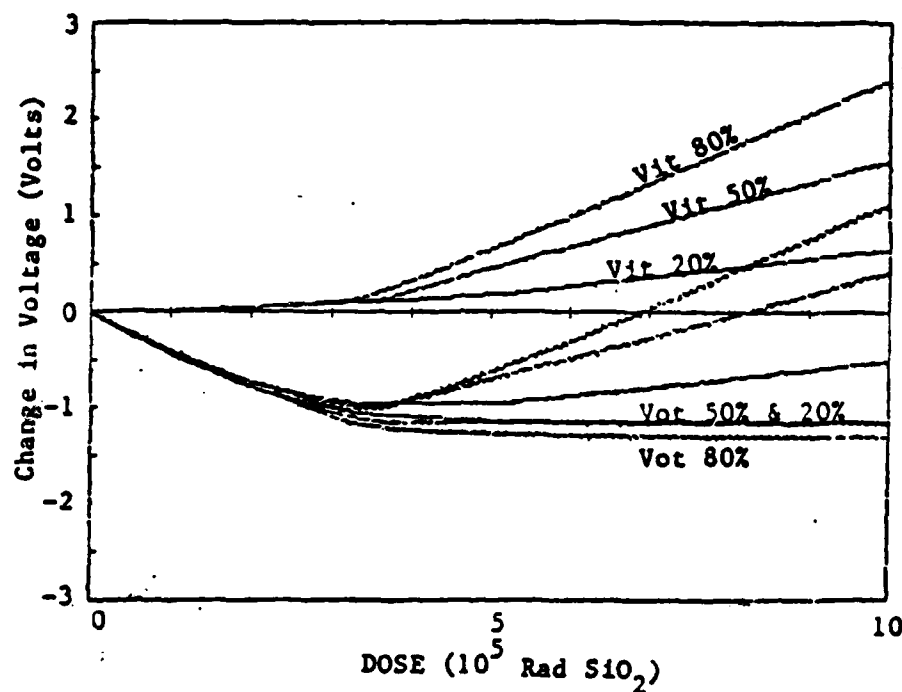
Figure 5.4   Computer simulation of duty cycle effects on the interface state buildup for N-channel MOSFETs showing the possibility of increased interface state buildup with short of times.
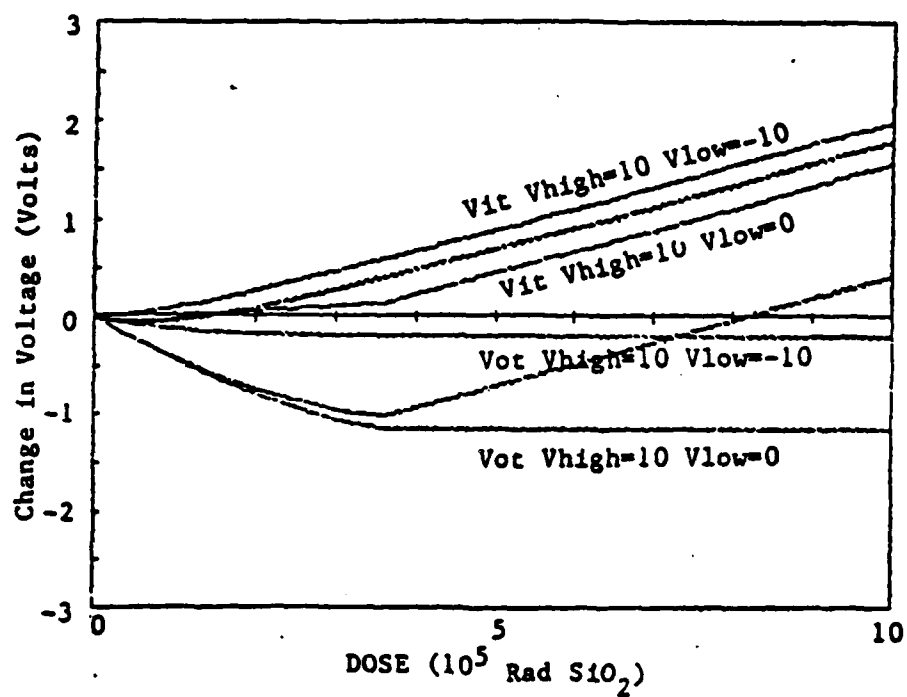
Figure 5.5   Computer simulation of symmetrical alternating
bias compared with bias alternating between "on" and "off"
showing the possibility of increased interface state buildup.

CHAPTER VI

CONCLUSIONS

These experiments have shown the source of the alternating bias effect reported by Dressendorfer to be due to radiation enhanced annealing of trapped holes with a concurrent creation of interface states. Because of the different rates for hole annihilation from radiation produced electrons and electrons tunneled from the substrate, the effect would be dose rate dependent, as well as dependent on temperature. Also, the effect would be masked if large numbers of holes were trapped throughout the oxide since the contribution to the threshold voltage shift from interface states could then be relatively small.

These results support a two stage model of interface state formation that has hole trapping as the first stage, followed by hole annihilation by electrons either supplied by the ionizing radiation or tunneled in from the substrate. The anneal of the trapped holes appears to correlate with interface state buildup. But the interface state buildup is not always obvious since under some conditions interface states can anneal.

A follow-on experiment is suggested to more thoroughly characterize the role of radiation produced electrons in the observed effect. The experiment would be to pulse irradiate devices at a LINAC facility synchronizing the alternating bias to the radiation pulse so that some devices are always irradiated with a positive bias applied to the gate of the device and some devices are always irradiated with

zero bias on the gate. Then, assuming a rapid repetition rate of pulse radiation and bias switching (100khz to 1Mhz), holes would be transported during both bias conditions, but electrons would be transported before the bias switched. Comparing the radiation induced shifts in the two sets of parts should more clearly identify the role of electrons in the radiation-enhanced anneal effect, since the MOSFETs always irradiated with the positive bias on the gate should not have much radiation produced electron annealing. Also, the experiments suggested by the computer model, namely using different duty cycles and also using a true possitive to negative alternating bias should be performed.

This research has shown that MOS devices irradiated while being switched between "on" and "off" can have more interface state build up and less hole trapping than MOS devices irradiated while maintained continuously "on." Also the annealing of trapped holes would be more complete when the MOS device is irradiated with an alternating bias applied. Therefore, MOS devices being tested for long term, low dose applications should be tested in as close to the actual operating environment as possible. Since testing at the low dose rate of space is not practical, testing for rebound failure should be done on operating circuits followed by bias-temperature annealing.

APPENDIX A

COMPUTER SIMULATION CODE

```
10    !  THE EFFECT OF PULSED BIAS ON HOLE TRAPPING AND INTERFACE STATE BUILDUP
20    !  IN RADIATED MOS DEVICES
30    !  BY TIMOTHY D. STANLEY
40    !  25 APRIL 1985
50    !  A MODEL BASED ON "A SIMPLE MODEL FOR PREDICTING RADIATION EFFECTS IN
60    !  MOS DEVICES"  BY RODGER FREEMAN AND ANDREW HOLMES-SIEDLE, IEEE TRANS
70    !  ON NUC SCIENCE, VOL N5-25, NO.6, DEC 1978
80    !
90    !  THIS CODE WAS DESIGNED TO OPERATE ON AN HP 98XX COMPUTER USING BASIC
100   !  VERSION 2.1
110   !
120   GINIT
130    REAL Delvit(1000),Delvot(1000),Delvth(1000)
140    !
150    !  DELVIT- CHANGE IN THRESHOLD VOLTAGE DUE TO INTERFACE STATE BUILDUP
160    !  DELVOT- CHANGE IN THE THRESHOLD VOLTAGE DUE TO TRAPPED HOLES
170    !  DELVTH- CHANGE IN THE THRESHOLD VOLTAGE
180    !  THESE ARE VALUES FOR EACH TIME STEP
190    Steps=1000   !  THE TOTAL NUMBER OF TIME STEPS IS 1000
200    INPUT "FRAC,VAPP,Z,SWITCH(Y OR N)",Frac,Vapp,Z,Sw$
210    !
220    !  FRAC IS THE FRACTION OF ANNIHILATED HOLES THAT BECOME INTERFACE STATES
230    !  VAPP IS THE APPLIED VOLTAGE IN VOLTS
240    !  Z IS A NORMALIZATION CONSTANT BETWEEN ELECTRON AND HOLE TRAPPING
250    !  FOR EQUAL HOLE TRAPPING BETWEEN ELECTRONS AND HOLES FOR MOST CASES
260    !  Z WOULD EQUAL APPROXIMATELY 50
270    !  RECOMMEND USING Z=40
280    !  SW$ EQUALS "Y" IF THE SIMULATION IS TO USE ALTERNATING BIAS
290    !
300    IF Sw$="Y" THEN
310    INPUT "VHIGH,VLOW,COUNTS HIGH, COUNTS LOW",Vhigh,Vlow,Mhigh,Mlow
320    !
330    !  VHIGH IS THE HIGH VOLTAGE FOR ALTERNATING BIAS
340    !  VLOW IS THE LOW VOLTAGE FOR ALTERNATING BIAS
350    !  COUNTS HIGH IS THE NUMBER OF TIME STEPS BEFORE THE BIAS SWITCHES
360    !  COUNTS LOW IS THE NUMBER OF TIME STEPS THE VOLTAGE STAYS LOW BEFORE
370    !  SWITCHING BACK.  BY ADJUSTING COUNTS HIGH AND LOW THE DUTY CYCLE
380    !  AND FREQUENCY CAN BE ADJUSTED
390    !
400    END IF
410    WINDOW 0,1.E+6,-3,3
420    FRAME
430    AXES 1.E+5,.5
440    PLOT 5.E+5,0,-2
450    !
460    Vbi=1.1          !  BUILT-IN VOLTAGE (PHI MS) N-POLY OVER P SI
470    Xox=.0000045   !  TOTAL OXIDE THICKNESS IN CM
480    G=7.9E+12       !  ELECTRON-HOLE PAIRS PER CUBIC CM PER RAD SIO2
490    Q=1.6E-19       !  ELECTRON CHARGE IN COULOMBS
500    Eps=3.9*8.854E-14   !  PERMITIVITY OF SIO2 IN FARADS/CM
```

```basic
510    ! Xch - COLLECTION LENGTH FOR HOLES IN CM
520    ! Xce - COLLECTION LENGTH FOR ELECTRONS IN CM
530    Mxi=.12 ! MAXIMUM TRAPPING FRACTION
540    Edif=10000    ! THE MINIMUM E-FIELD DUE TO DIFFUSION
550    !
560    !  THE HOLE-ELECTRON PAIR YIELD FROM INITIAL RECOMBINATION IS
570    !  PROPORTIONAL TO THE SQUARE ROOT OF THE FIELD ACROSS THE OXIDE
580    !  BASED ON DOSIER AND BROWN IEEE TRANS ON NUC SCIENCE DEC 1980
590    !  THE HOLE TRAPPING PROBABILITY IS PROPORTIONAL TO 1/SQR(E-FIELD)
600    !  SAME REFERENCE
610    !
620    A=Mxi/580000^.5  ! NORMALIZATION COEFFICIENT  FOR ELECTRON HOLE YIELD
630    B=Mxi*580000^.5  ! NORMILIZATION COEFFICIENT  FOR HOLE TRAPPING
640    D=1.E+6/Steps     ! DOSE PER STEP
650    X1=.00000015 ! DISTANCE FROM SI TO HOLE TRAPPING SHEET
660    X2=.00000435 ! DISTANCE FROM HOLE TRAPPING SHEET TO GATE
670    X3=.00000030 ! COLLECTION LENGTH LIMIT DUE TO DIFFUSION
680    PRINT "    FRAC=";Frac;"   V APP=";Vapp;"      Z=";Z;"     SWITCH=";Sw$
690    PRINT "   EDIF=";Edif;"    MAX TRAP=";Mxi
700    IF Sw$="Y" THEN
710    PRINT "DUTY CYCLE=";Mhigh/(Mhigh+Mlow)*100;"% CYCLES=";Steps/(Mhigh+Mlow):
"    VHIGH=";Vhigh;"     VLOW=";Vlow
720    END IF
730    PRINT
740    PRINT "  DOSE      DEL VTH    DEL VOT    DEL VIT     NOT         NIT
    V"
750    Chigh=0
760    Clow=0
770    !
780    !  START OF SIMULATION LOOP
790    !
800    FOR I=1 TO Steps
810    !
820    !  BIAS SWITCHING ROUTINE
830    !
840      IF Sw$<>"Y" THEN 980
850      IF Vapp=Vhigh THEN
860       Chigh=Chigh+1
870        IF Chigh=Mhigh THEN
880        Vapp=Vlow
890        Chigh=0
900        END IF
910      ELSE
920      Clow=Clow+1
930       IF Clow=Mlow THEN
940        Vapp=Vhigh
950        Clow=0
960        END IF
970      END IF
980      V=Vapp+Delvot(I-1)+Vbi
990      E=V/Xox
1000      IF E<-Edif THEN
```

```
1010        Xch=X1
1020        Xce=X2
1030        GOTO 1120
1040     END IF
1050     IF E>Edif THEN
1060        Xch=X2
1070        Xce=X1
1080        GOTO 1120
1090     END IF
1100     Xch=X3
1110     Xce=X3
1120     E=ABS(E)
1130     IF E<Edif THEN E=Edif
1140     IF E<590000 THEN
1150        Yt=A*E^.5
1160     ELSE
1170        Yt=B/E^.5
1180     END IF
1190     !
1200     Nox=Nox+G*Xch*Yt*D       !   TRAP HOLES
1210     Anot=Nox*Z*(G*Xce*Yt*D+T)/(G*Xox*Mxi*1.E+6)    ! ANNIHILATE TRAPPED HOLES
1220     Nox=Nox-Anot
1230     Nit=Nit+Anot*Frac        !    ANNIHILATED HOLES BECOME INTERFACE STATES
1240     !
1250     Delvot(I)=-Q*X2*Nox/Eps
1260     Delvit(I)=Q*Xox*Nit/Eps
1270     Delvth(I)=Delvit(I)+Delvot(I)
1280     IF 0=I MOD (Steps/10) THEN    !    ONLY PRINT OUT TEN ENTRIES
1290     PRINT USING "MD.DDE,XX";D*I,Delvth(I),Delvot(I),Delvit(I),Nox,Nit,V
1300     END IF
1310  NEXT I
1320  !
1330  !   END OF SIMULATION LOOP -   START PLOTTING THE RESULTS
1340  !
1350  FOR I=0 TO Steps
1360  PLOT D*I,Delvth(I),1
1370  NEXT I
1380  PLOT 5.E+5,0,-2
1390  FOR I=0 TO Steps
1400  PLOT D*I,Delvot(I),1
1410  NEXT I
1420  PLOT 5.E+5,0,-2
1430  FOR I=0 TO Steps
1440  PLOT D*I,Delvit(I),1
1450  NEXT I
1460  PLOT 5.E+5,0,-2
1470  PRINT
1480  Nox=0
1490  Anot=0
1500  Nit=0
1510  GOTO 130
1520  END
```

APPENDIX B

SAMPLE RUNS OF SIMULATION CODE

FRAC= 1   V APP= 10   Z= 40   SWITCH=N
EDIF= 10000   MAX TRAP= .12

DOSE	DEL VTH	DEL VOT	DEL VIT	NOT	NIT	V
1.00E+05	-3.80E-01	-3.94E-01	1.36E-02	1.95E+11	6.51E+09	1.07E+01
2.00E+05	-7.15E-01	-7.69E-01	5.38E-02	3.81E+11	2.58E+10	1.03E+01
3.00E+05	-1.01E+00	-1.13E+00	1.20E-01	5.59E+11	5.77E+10	9.98E+00
4.00E+05	-1.25E+00	-1.47E+00	2.13E-01	7.27E+11	1.02E+11	9.64E+00
5.00E+05	-1.46E+00	-1.79E+00	3.31E-01	8.87E+11	1.59E+11	9.32E+00
6.00E+05	-1.62E+00	-2.09E+00	4.74E-01	1.04E+12	2.27E+11	9.01E+00
7.00E+05	-1.74E+00	-2.38E+00	6.42E-01	1.18E+12	3.08E+11	8.72E+00
8.00E+05	-1.82E+00	-2.65E+00	8.34E-01	1.32E+12	4.00E+11	8.45E+00
9.00E+05	-1.86E+00	-2.91E+00	1.05E+00	1.44E+12	5.03E+11	8.19E+00
1.00E+06	-1.87E+00	-3.15E+00	1.29E+00	1.56E+12	6.18E+11	7.95E+00
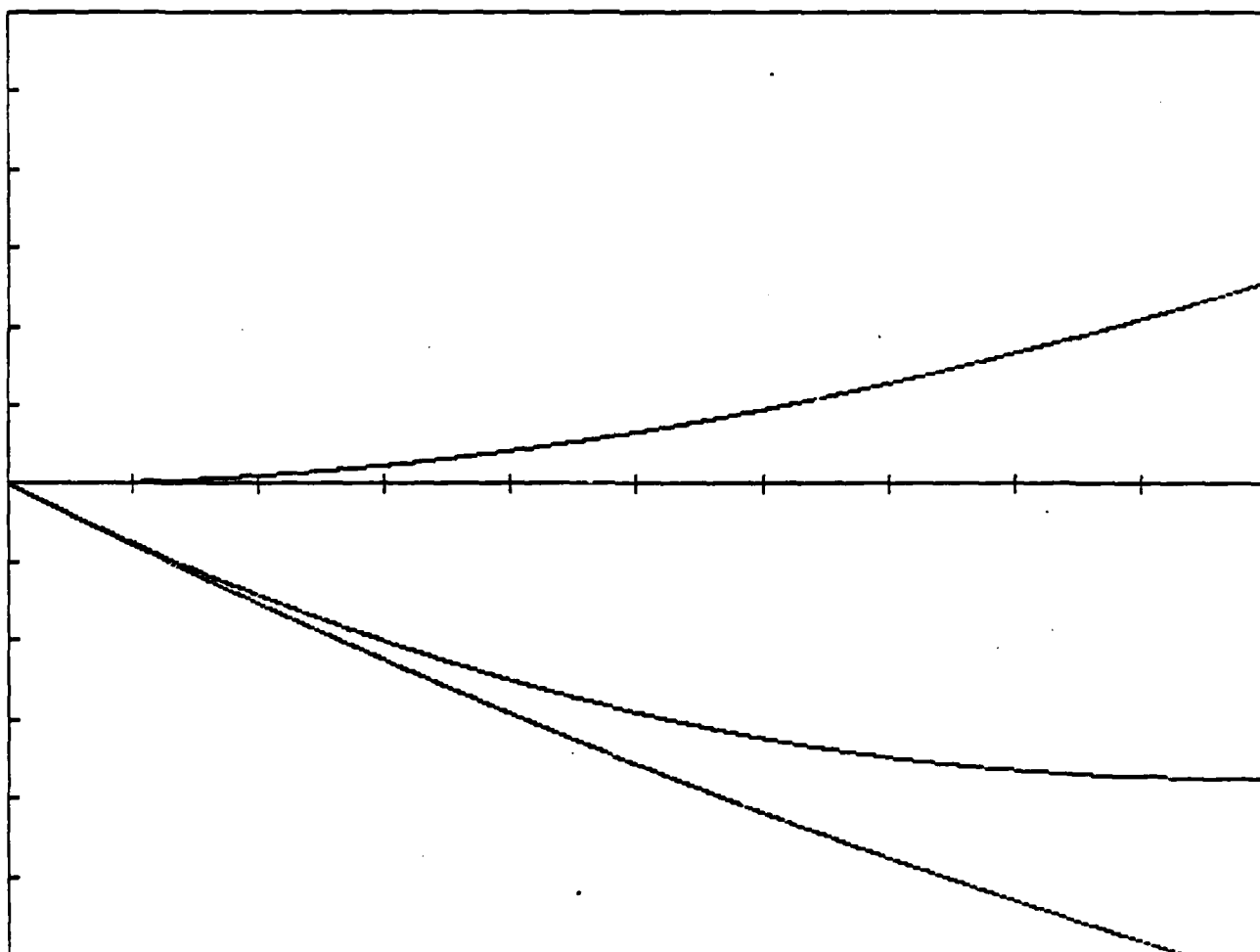
FRAC= 1   V APP= 0   Z= 40   SWITCH=N
EDIF= 10000   MAX TRAP= .12

DOSE	DEL VTH	DEL VOT	DEL VIT	NOT	NIT	V
1.00E+05	-4.39E-01	-4.58E-01	1.85E-02	2.27E+11	8.87E+09	6.46E-01
2.00E+05	-7.21E-01	-7.76E-01	5.48E-02	3.85E+11	2.63E+10	3.27E-01
3.00E+05	-8.89E-01	-9.79E-01	8.93E-02	4.86E+11	4.28E+10	1.23E-01
4.00E+05	-9.38E-01	-1.05E+00	1.17E-01	5.23E+11	5.62E+10	4.49E-02
5.00E+05	-9.05E-01	-1.06E+00	1.51E-01	5.24E+11	7.22E+10	4.43E-02
6.00E+05	-8.71E-01	-1.05E+00	1.84E-01	5.23E+11	8.84E+10	4.48E-02
7.00E+05	-8.38E-01	-1.06E+00	2.18E-01	5.24E+11	1.04E+11	4.42E-02
8.00E+05	-8.04E-01	-1.05E+00	2.51E-01	5.23E+11	1.21E+11	4.48E-02
9.00E+05	-7.71E-01	-1.06E+00	2.85E-01	5.24E+11	1.37E+11	4.42E-02
1.00E+06	-7.36E-01	-1.05E+00	3.18E-01	5.23E+11	1.53E+11	4.47E-02

FRAC= 1   V APP= 10   Z= 40   SWITCH=Y
    EDIF= 10000   MAX TRAP= .12
DUTY CYCLE= 50 % CYCLES= 100   VHIGH= 10   VLOW= 0

DOSE	DEL VTH	DEL VOT	DEL VIT	NOT	NIT	V
1.00E+05	-4.12E-01	-4.28E-01	1.61E-02	2.12E+11	7.73E+09	1.07E+01
2.00E+05	-7.21E-01	-7.76E-01	5.49E-02	3.85E+11	2.63E+10	1.03E+01
3.00E+05	-9.43E-01	-1.05E+00	1.03E-01	5.19E+11	4.93E+10	1.01E+01
4.00E+05	-9.20E-01	-1.14E+00	2.24E-01	5.68E+11	1.08E+11	9.96E+00
5.00E+05	-7.00E-01	-1.15E+00	4.46E-01	5.69E+11	2.14E+11	9.96E+00
6.00E+05	-4.80E-01	-1.15E+00	6.68E-01	5.69E+11	3.20E+11	9.96E+00
7.00E+05	-2.47E-01	-1.14E+00	8.95E-01	5.67E+11	4.29E+11	9.96E+00
8.00E+05	-2.70E-02	-1.14E+00	1.12E+00	5.68E+11	5.36E+11	9.96E+00
9.00E+05	1.92E-01	-1.15E+00	1.34E+00	5.69E+11	6.42E+11	9.96E+00
1.00E+06	4.13E-01	-1.15E+00	1.56E+00	5.69E+11	7.48E+11	9.96E+00

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```
FRAC= 1     V APP= 10      Z= 40      SWITCH=Y
   EDIF= 10000    MAX TRAP= .12
DUTY CYCLE= 80 % CYCLES= 100      VHIGH= 10      VLOW= 0

  DOSE        DEL VTH     DEL VOT     DEL VIT       NOT          NIT          V
1.00E+05    -3.93E-01   -4.08E-01    1.46E-02    2.02E+11     7.00E+09     1.07E+01
2.00E+05    -7.18E-01   -7.73E-01    5.44E-02    3.83E+11     2.61E+10     1.03E+01
3.00E+05    -9.74E-01   -1.09E+00    1.14E-01    5.40E+11     5.45E+10     1.00E+01
4.00E+05    -8.86E-01   -1.22E+00    3.32E-01    6.04E+11     1.59E+11     9.89E+00
5.00E+05    -6.07E-01   -1.26E+00    6.49E-01    6.23E+11     3.11E+11     9.85E+00
6.00E+05    -2.79E-01   -1.27E+00    9.91E-01    6.30E+11     4.75E+11     9.83E+00
7.00E+05     6.68E-02   -1.27E+00    1.34E+00    6.32E+11     6.43E+11     9.83E+00
8.00E+05     4.19E-01   -1.28E+00    1.70E+00    6.33E+11     8.13E+11     9.83E+00
9.00E+05     7.74E-01   -1.28E+00    2.05E+00    6.34E+11     9.84E+11     9.83E+00
1.00E+06     1.13E+00   -1.28E+00    2.41E+00    6.34E+11     1.15E+12     9.83E+00
```


84

```
FRAC= 1     V APP= 10      Z= 40      SWITCH=Y
   EDIF= 10000    MAX TRAP= .12
DUTY CYCLE= 20 % CYCLES= 100      VHIGH= 10      VLOW= 0

   DOSE      DEL VTH     DEL VOT     DEL VIT      NOT         NIT         V
 1.00E+05   -4.29E-01   -4.47E-01   1.76E-02    2.22E+11    8.44E+09   1.07E+01
 2.00E+05   -7.22E-01   -7.78E-01   5.51E-02    3.86E+11    2.64E+10   1.03E+01
 3.00E+05   -9.11E-01   -1.01E+00   9.46E-02    4.99E+11    4.54E+10   1.01E+01
 4.00E+05   -9.49E-01   -1.09E+00   1.37E-01    5.39E+11    6.56E+10   1.00E+01
 5.00E+05   -9.46E-01   -1.13E+00   1.85E-01    5.61E+11    8.85E+10   9.97E+00
 6.00E+05   -8.73E-01   -1.14E+00   2.68E-01    5.66E+11    1.29E+11   9.96E+00
 7.00E+05   -7.88E-01   -1.15E+00   3.58E-01    5.68E+11    1.71E+11   9.96E+00
 8.00E+05   -6.91E-01   -1.14E+00   4.53E-01    5.68E+11    2.17E+11   9.96E+00
 9.00E+05   -5.95E-01   -1.14E+00   5.48E-01    5.67E+11    2.63E+11   9.96E+00
 1.00E+06   -4.98E-01   -1.14E+00   6.43E-01    5.66E+11    3.09E+11   9.96E+00
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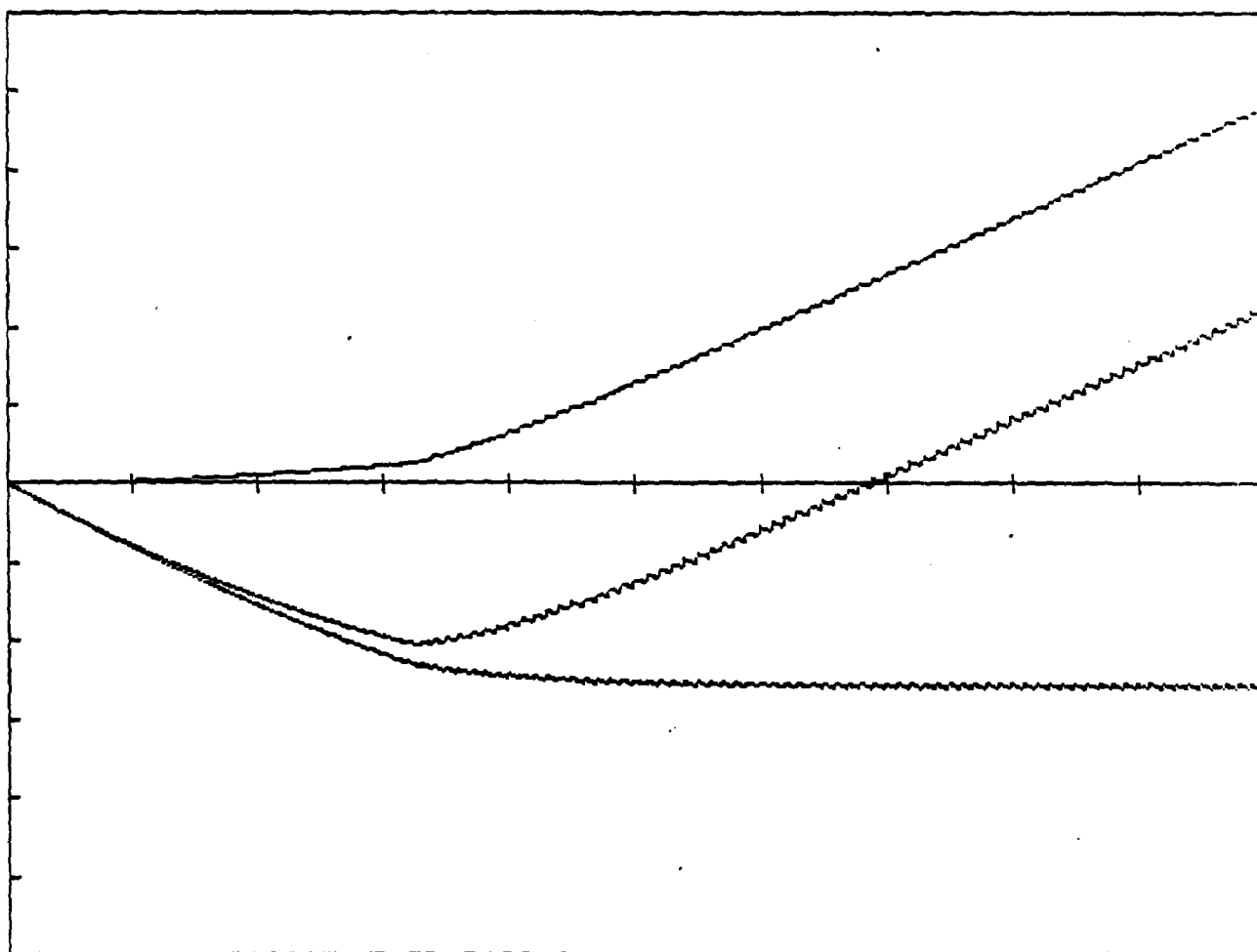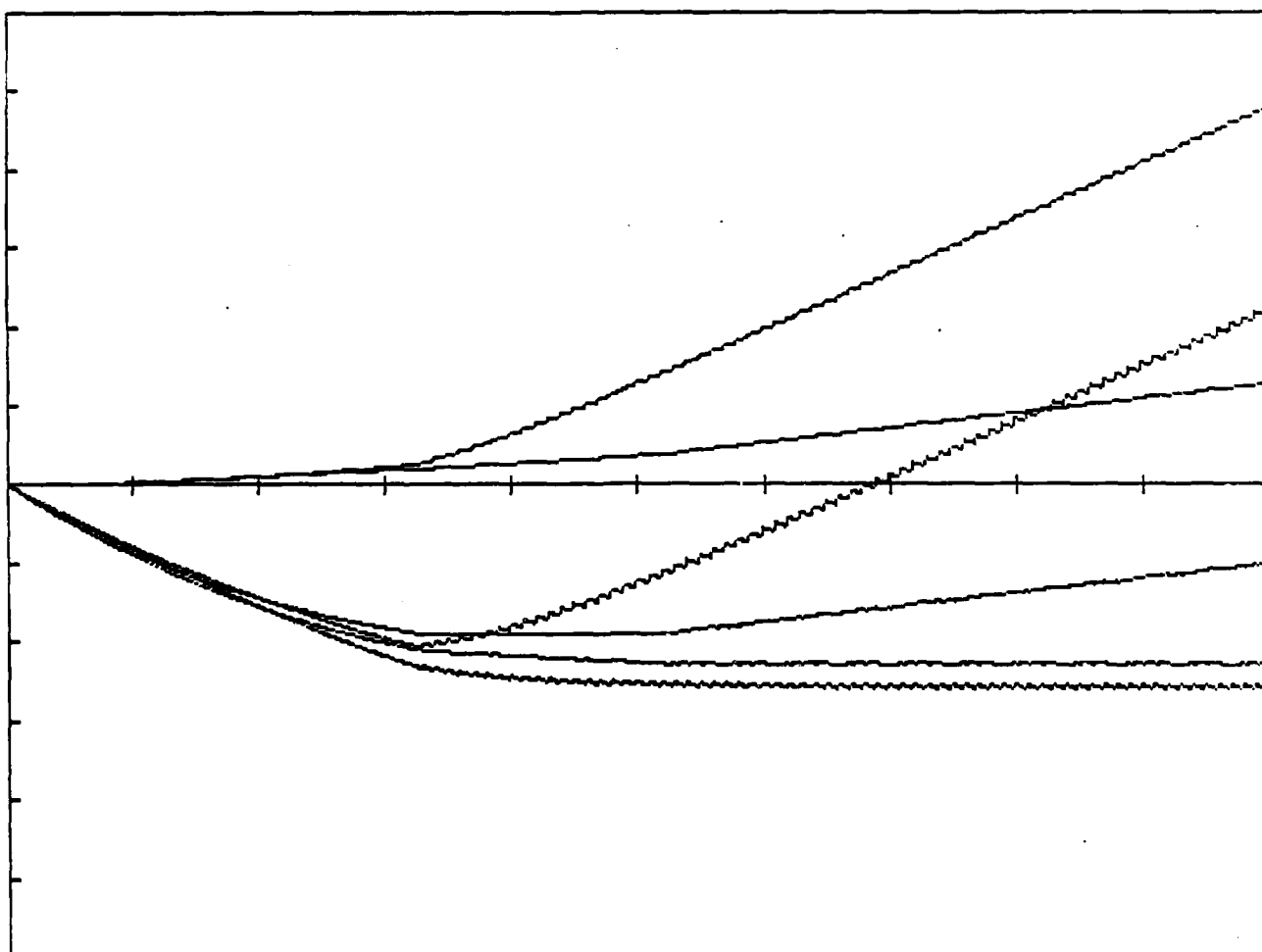

85

FRAC= 1   V APP= 10   Z= 40   SWITCH=Y
EDIF= 10000   MAX TRAP= .12
DUTY CYCLE= 50 % CYCLES= 100   VHIGH= 10   VLOW= 0

DOSE	DEL VTH	DEL VOT	DEL VIT	NOT	NIT	V
1.00E+05	-4.12E-01	-4.28E-01	1.61E-02	2.12E+11	7.73E+09	1.07E+01
2.00E+05	-7.21E-01	-7.76E-01	5.49E-02	3.85E+11	2.63E+10	1.03E+01
3.00E+05	-9.43E-01	-1.05E+00	1.03E-01	5.19E+11	4.93E+10	1.01E+01
4.00E+05	-9.20E-01	-1.14E+00	2.24E-01	5.68E+11	1.08E+11	9.96E+00
5.00E+05	-7.00E-01	-1.15E+00	4.46E-01	5.69E+11	2.14E+11	9.96E+00
6.00E+05	-4.80E-01	-1.15E+00	6.68E-01	5.69E+11	3.20E+11	9.96E+00
7.00E+05	-2.47E-01	-1.14E+00	8.95E-01	5.67E+11	4.29E+11	9.96E+00
8.00E+05	-2.70E-02	-1.14E+00	1.12E+00	5.68E+11	5.36E+11	9.96E+00
9.00E+05	1.92E-01	-1.15E+00	1.34E+00	5.69E+11	6.42E+11	9.96E+00
1.00E+06	4.13E-01	-1.15E+00	1.56E+00	5.69E+11	7.48E+11	9.96E+00

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FRAC= 1   V APP= 10   Z= 40   SWITCH=Y
EDIF= 10000   MAX TRAP= .12
DUTY CYCLE= 20 % CYCLES= 100   VHIGH= 10   VLOW= 0

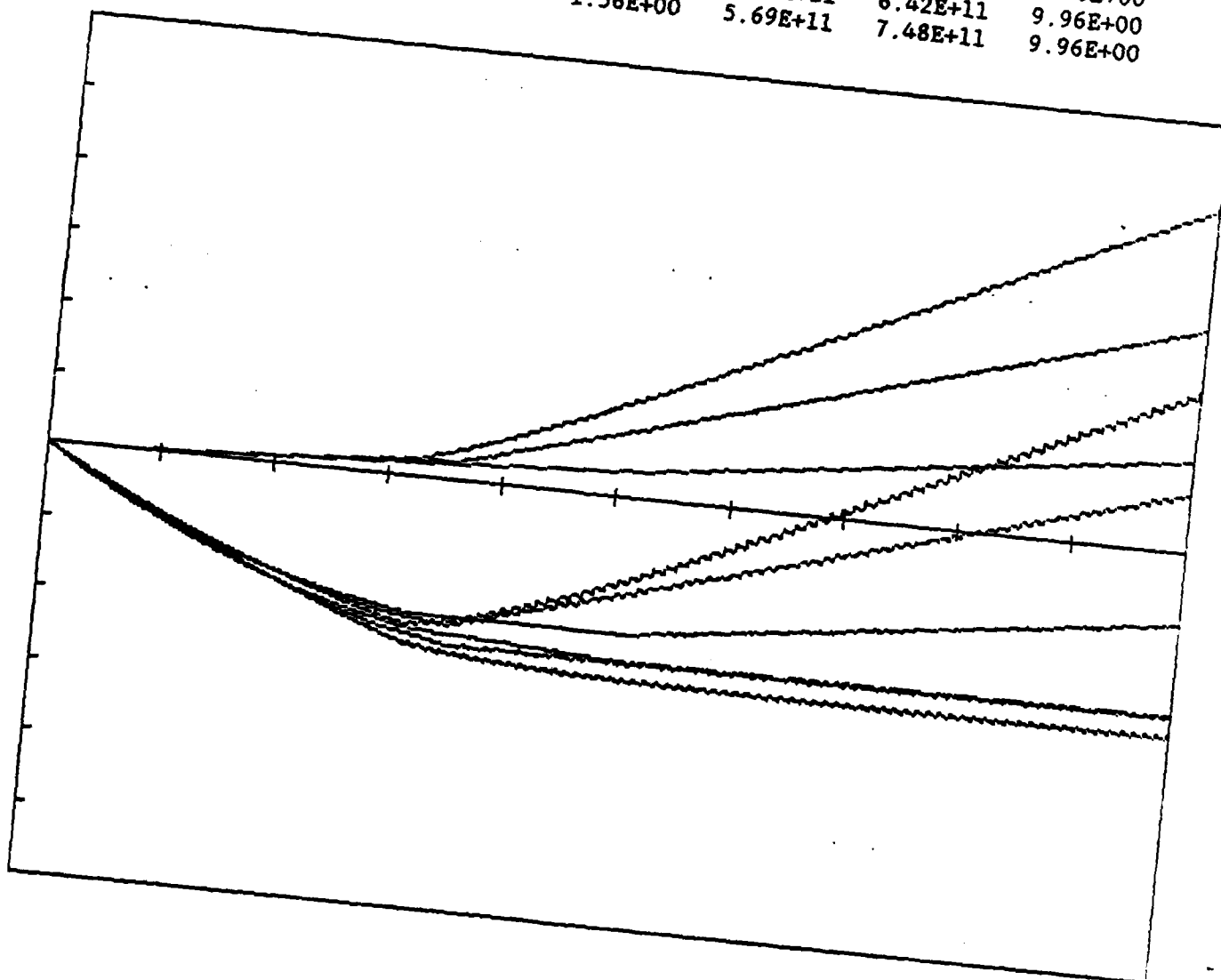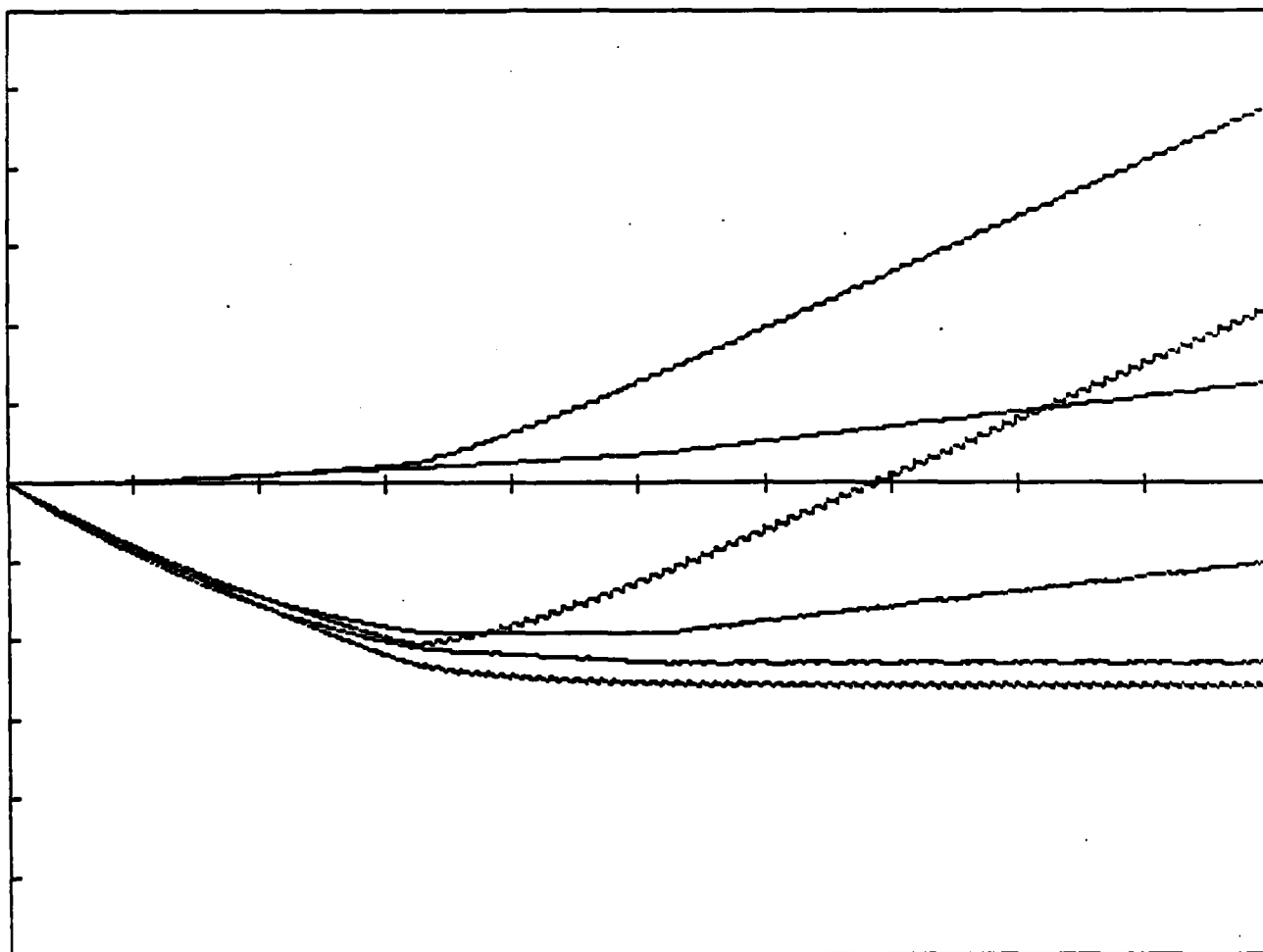| DOSE	DEL VTH	DEL VOT	DEL VIT	NOT	NIT	V
1.00E+05	-4.29E-01	-4.47E-01	1.76E-02	2.22E+11	8.44E+09	1.07E+01
2.00E+05	-7.22E-01	-7.78E-01	5.51E-02	3.86E+11	2.64E+10	1.03E+01
3.00E+05	-9.11E-01	-1.01E+00	9.46E-02	4.99E+11	4.54E+10	1.01E+01
4.00E+05	-9.49E-01	-1.09E+00	1.37E-01	5.39E+11	6.56E+10	1.00E+01
5.00E+05	-9.46E-01	-1.13E+00	1.85E-01	5.61E+11	8.85E+10	9.97E+00
6.00E+05	-8.73E-01	-1.14E+00	2.68E-01	5.66E+11	1.29E+11	9.96E+00
7.00E+05	-7.88E-01	-1.15E+00	3.58E-01	5.68E+11	1.71E+11	9.96E+00
8.00E+05	-6.91E-01	-1.14E+00	4.53E-01	5.68E+11	2.17E+11	9.96E+00
9.00E+05	-5.95E-01	-1.14E+00	5.48E-01	5.67E+11	2.63E+11	9.96E+00
1.00E+06	-4.98E-01	-1.14E+00	6.43E-01	5.66E+11	3.09E+11	9.96E+00

FRAC= 1   V APP= 10   Z= 40   SWITCH=Y
  EDIF= 10000   MAX TRAP= .12
DUTY CYCLE= 50 % CYCLES= 100   VHIGH= 10   VLOW=-10

DOSE	DEL VTH	DEL VOT	DEL VIT	NOT	NIT	V
1.00E+05	-3.58E-02	-1.24E-01	8.86E-02	6.17E+10	4.25E+10	1.10E+01
2.00E+05	9.52E-02	-1.67E-01	2.62E-01	8.29E+10	1.26E+11	1.09E+01
3.00E+05	2.83E-01	-1.82E-01	4.65E-01	9.02E+10	2.23E+11	1.09E+01
4.00E+05	4.91E-01	-1.87E-01	6.78E-01	9.27E+10	3.25E+11	1.09E+01
5.00E+05	7.06E-01	-1.89E-01	8.94E-01	9.36E+10	4.29E+11	1.09E+01
6.00E+05	9.23E-01	-1.89E-01	1.11E+00	9.39E+10	5.33E+11	1.09E+01
7.00E+05	1.14E+00	-1.90E-01	1.33E+00	9.40E+10	6.38E+11	1.09E+01
8.00E+05	1.36E+00	-1.90E-01	1.55E+00	9.41E+10	7.43E+11	1.09E+01
9.00E+05	1.58E+00	-1.90E-01	1.77E+00	9.41E+10	8.47E+11	1.09E+01
1.00E+06	1.80E+00	-1.90E-01	1.98E+00	9.41E+10	9.52E+11	1.09E+01

```
FRAC= 1     V APP= 10      Z= 40      SWITCH=Y
   EDIF= 10000    MAX TRAP= .12
DUTY CYCLE= 50 % CYCLES= 100      VHIGH= 10      VLOW= 0

   DOSE       DEL VTH     DEL VOT      DEL VIT       NOT          NIT         V
 1.00E+05    -4.12E-01   -4.28E-01    1.61E-02     2.12E+11     7.73E+09   1.07E+01
 2.00E+05    -7.21E-01   -7.76E-01    5.49E-02     3.85E+11     2.63E+10   1.03E+01
 3.00E+05    -9.43E-01   -1.05E+00    1.03E-01     5.19E+11     4.93E+10   1.01E+01
 4.00E+05    -9.20E-01   -1.14E+00    2.24E-01     5.68E+11     1.08E+11   9.96E+00
 5.00E+05    -7.00E-01   -1.15E+00    4.46E-01     5.69E+11     2.14E+11   9.96E+00
 6.00E+05    -4.80E-01   -1.15E+00    6.68E-01     5.69E+11     3.20E+11   9.96E+00
 7.00E+05    -2.47E-01   -1.14E+00    8.95E-01     5.67E+11     4.29E+11   9.96E+00
 8.00E+05    -2.70E-02   -1.14E+00    1.12E+00     5.68E+11     5.36E+11   9.96E+00
 9.00E+05     1.92E-01   -1.15E+00    1.34E+00     5.69E+11     6.42E+11   9.96E+00
 1.00E+06     4.13E-01   -1.15E+00    1.56E+00     5.69E+11     7.48E+11   9.96E+00
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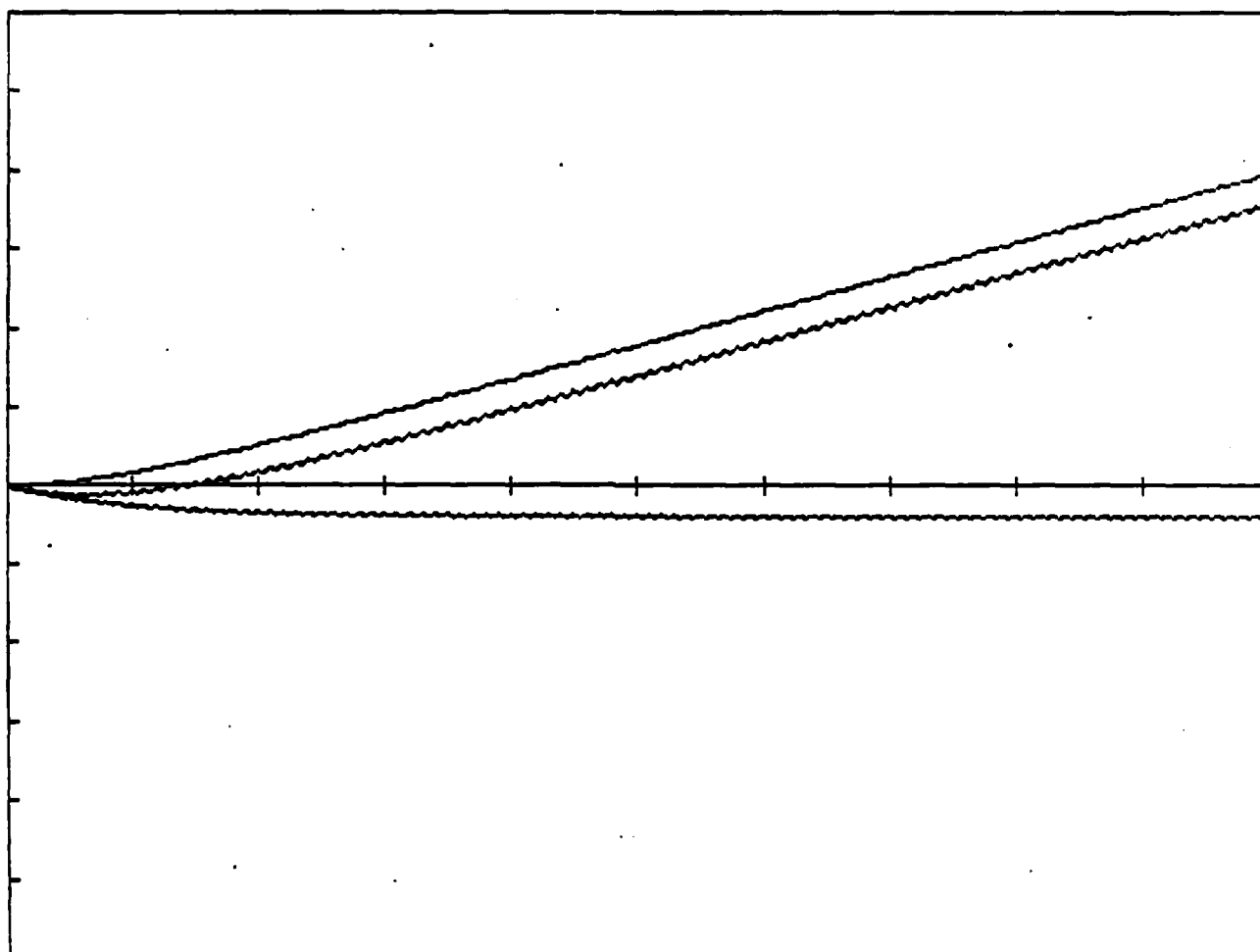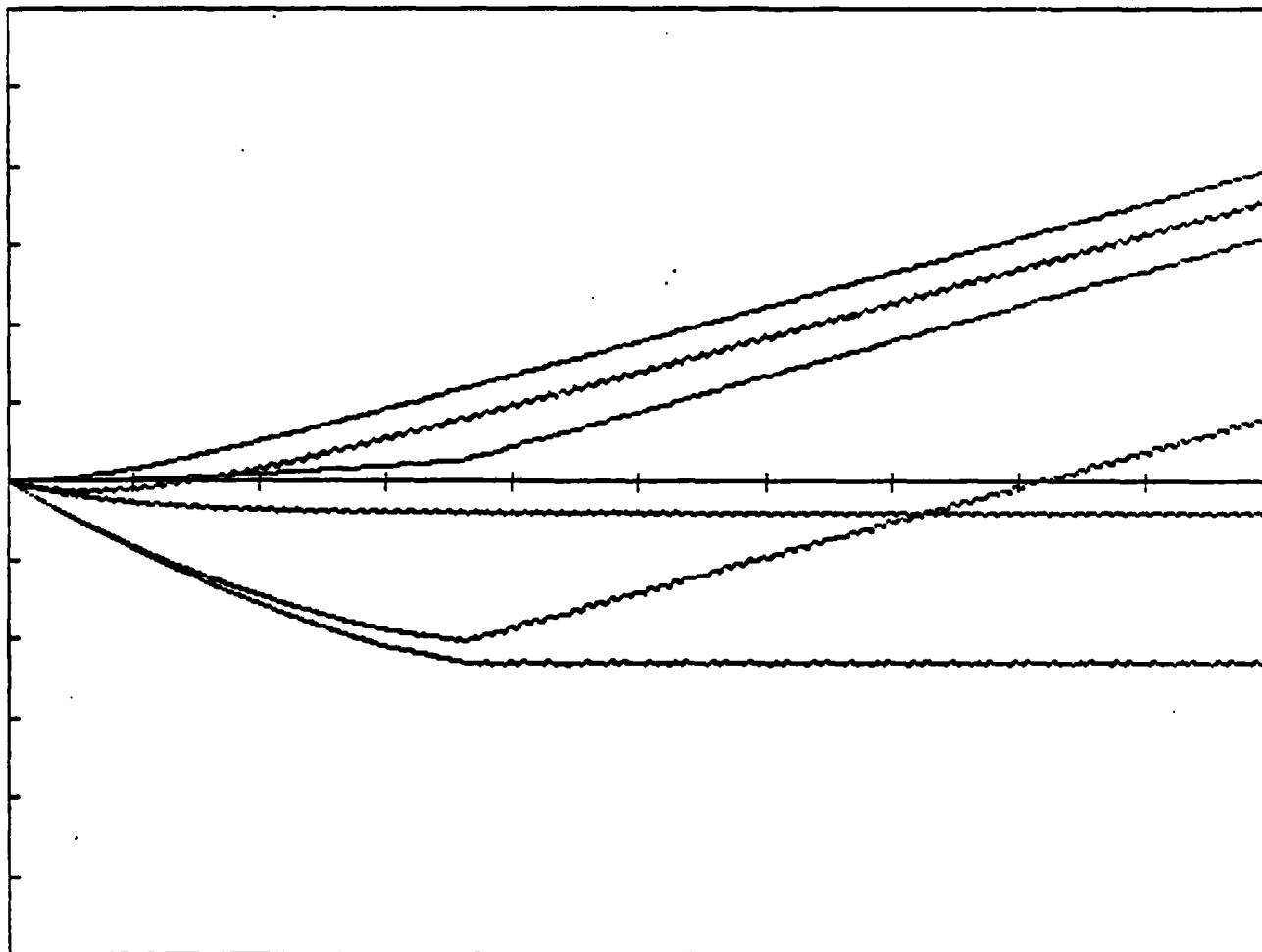
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2.00E+05	1.12E-01	-2.16E-01	3.28E-01	1.07E+11	1.57E+11	-9.12E+00
3.00E+05	3.42E-01	-2.30E-01	5.72E-01	1.14E+11	2.74E+11	-9.13E+00
4.00E+05	5.91E-01	-2.34E-01	8.25E-01	1.16E+11	3.95E+11	-9.14E+00
5.00E+05	8.45E-01	-2.35E-01	1.08E+00	1.17E+11	5.18E+11	-9.14E+00
6.00E+05	1.10E+00	-2.36E-01	1.34E+00	1.17E+11	6.41E+11	-9.14E+00
7.00E+05	1.36E+00	-2.36E-01	1.59E+00	1.17E+11	7.64E+11	-9.14E+00
8.00E+05	1.61E+00	-2.36E-01	1.85E+00	1.17E+11	8.87E+11	-9.14E+00
9.00E+05	1.87E+00	-2.36E-01	2.11E+00	1.17E+11	1.01E+12	-9.14E+00
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2.00E+05   -7.15E-01   -7.69E-01    5.38E-02    3.81E+11    2.58E+10    1.03E+01
3.00E+05   -1.01E+00   -1.13E+00    1.20E-01    5.59E+11    5.77E+10    9.98E+00
4.00E+05   -1.25E+00   -1.47E+00    2.13E-01    7.27E+11    1.02E+11    9.64E+00
5.00E+05   -1.38E+00   -1.75E+00    3.66E-01    8.68E+11    1.76E+11   -6.84E-01
6.00E+05   -9.90E-02   -1.12E+00    1.02E+00    5.57E+11    4.91E+11   -2.24E-02
7.00E+05   -2.77E-02   -1.09E+00    1.06E+00    5.41E+11    5.10E+11    8.83E-03
8.00E+05    4.14E-02   -1.06E+00    1.10E+00    5.26E+11    5.29E+11    3.90E-02
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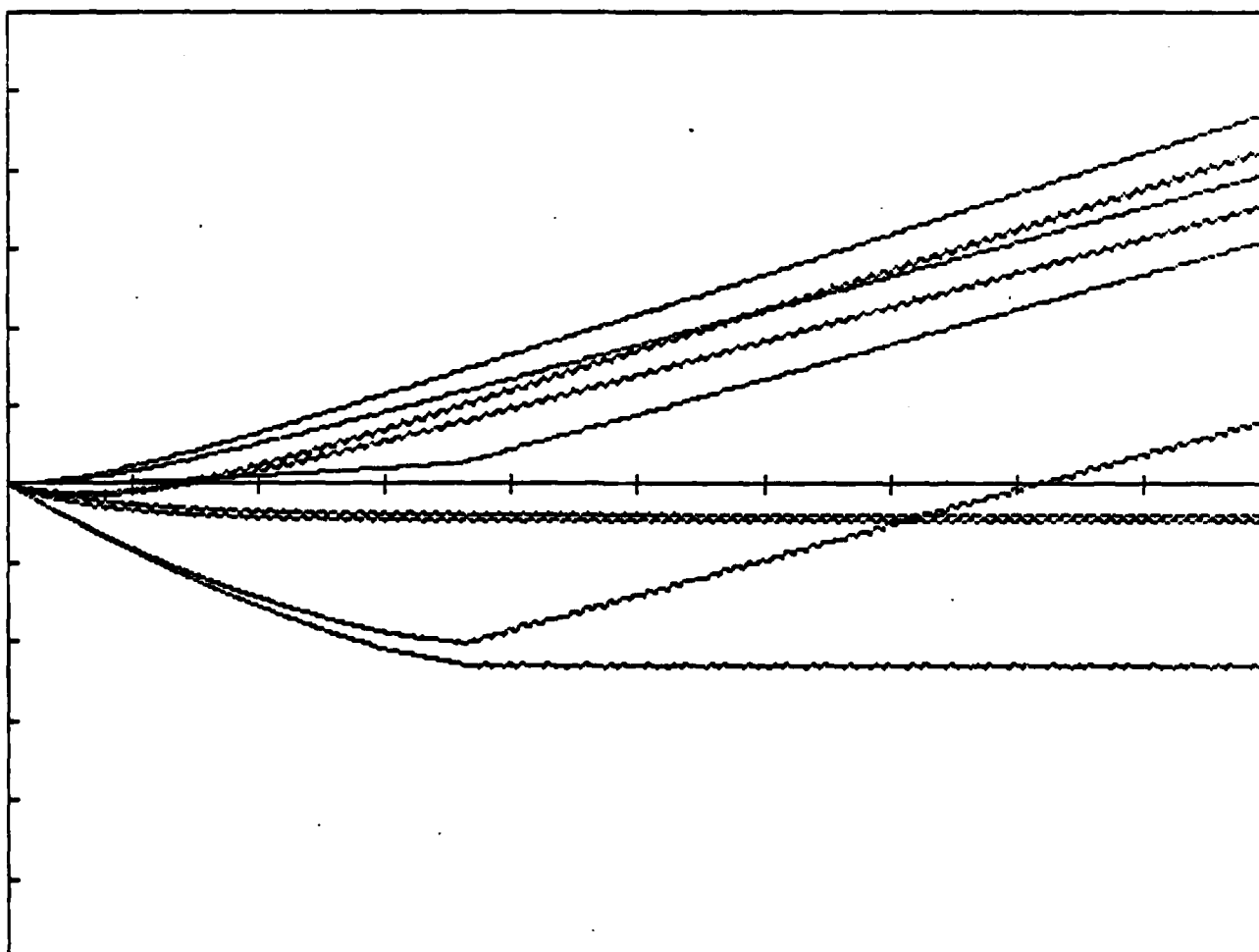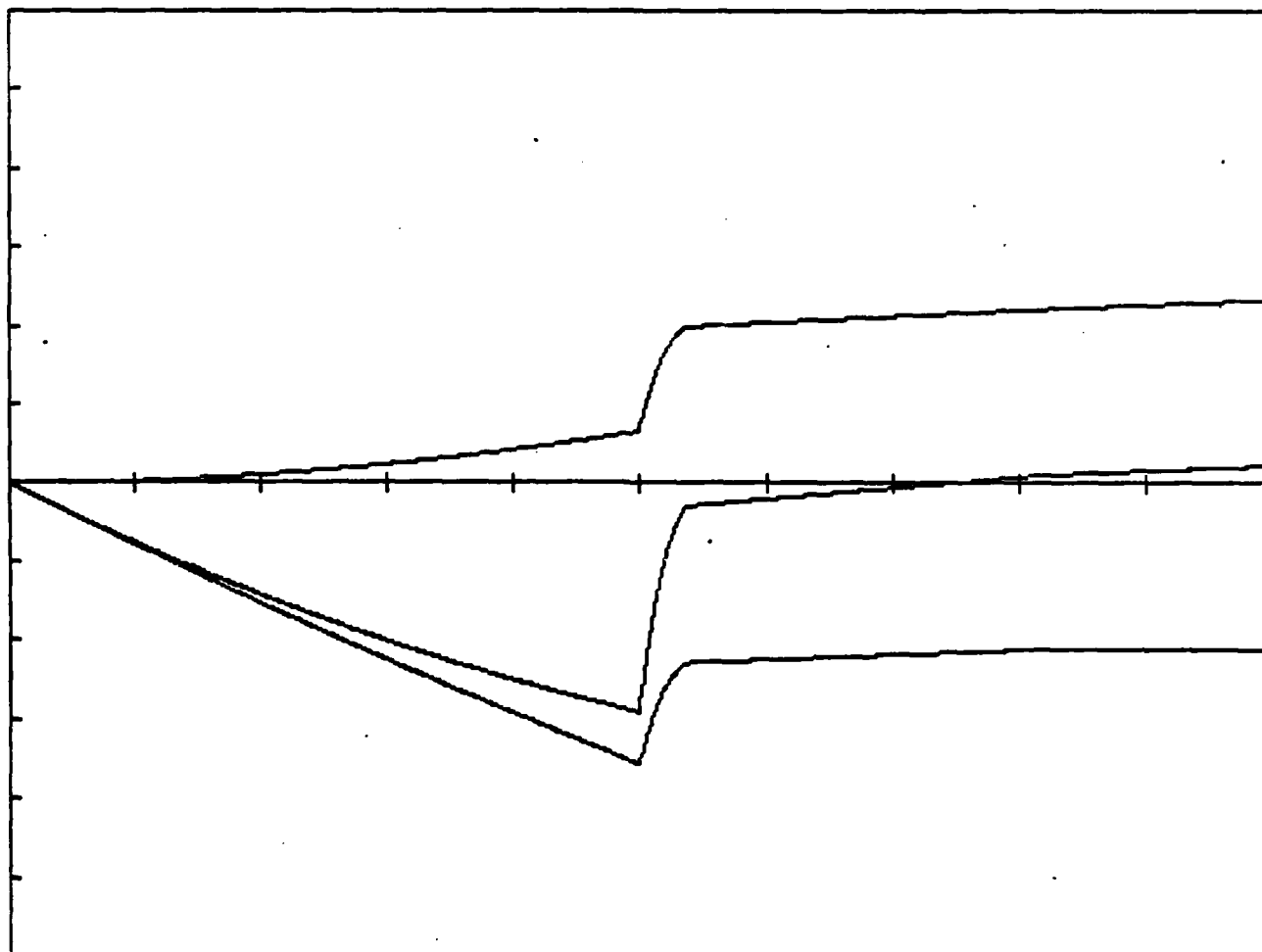
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DOSE	DEL VTH	DEL VOT	DEL VIT	NOT	NIT	V
1.00E+05	-4.39E-01	-4.58E-01	1.85E-02	2.27E+11	8.87E+09	6.46E-01
2.00E+05	-7.21E-01	-7.76E-01	5.48E-02	3.85E+11	2.63E+10	3.27E-01
3.00E+05	-8.89E-01	-9.79E-01	8.93E-02	4.86E+11	4.28E+10	1.23E-01
4.00E+05	-9.38E-01	-1.05E+00	1.17E-01	5.23E+11	5.62E+10	4.49E-02
5.00E+05	-9.08E-01	-1.06E+00	1.51E-01	5.26E+11	7.24E+10	1.00E+01
6.00E+05	-1.16E+00	-1.40E+00	2.39E-01	6.96E+11	1.14E+11	9.70E+00
7.00E+05	-1.38E+00	-1.73E+00	3.52E-01	8.57E+11	1.69E+11	9.38E+00
8.00E+05	-1.55E+00	-2.04E+00	4.90E-01	1.01E+12	2.35E+11	9.07E+00
9.00E+05	-1.67E+00	-2.33E+00	6.53E-01	1.15E+12	3.13E+11	8.78E+00
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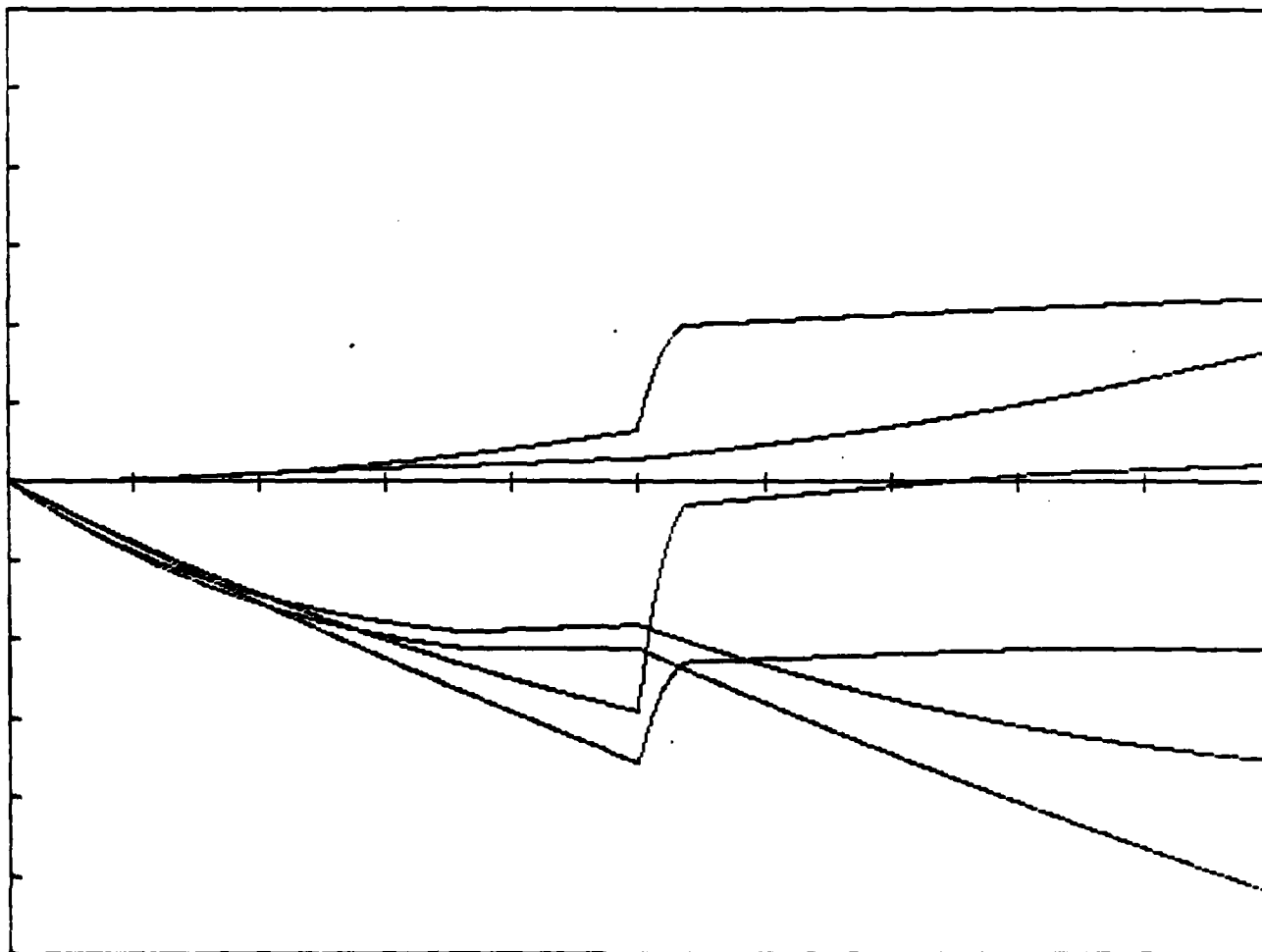
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Curriculum Vitae

TIMOTHY D. STANLEY

Timothy Daryl Stanley was born on June 2, 1947 in Logan, Utah to Daryl H. and Olive F. Stanley. He graduated from Orem High School, Orem, Utah in May 1965. He attended one year of a physics program at Brigham Young University before two years of missionary service on the Navajo Indian Reservation. He graduated from Brigham Young University in May 1971 and received a commission in the United States Air Force through the Air Force Reserve Officer Training Program (ROTC). His first assignment was as a Minute Man Missile Operations Officer at Ellsworth Air Force Base in South Dakota. There, he attended South Dakota State University part-time and earned a Masters of Science degree in Economics in May of 1975. His research topic was titled "The Social Cost of Alcohol Related Motor Vehicle Accidents in South Dakota in 1973." His next assignment was to full-time graduate training at the Air Force Institute of Technology (AFIT) in Nuclear Engineering. His thesis at AFIT, which was titled "Thermal Neutron Damage in Bipolar PNP Transistors," was republished by the Air Force Weapons Laboratory and an extract was published in the 1977 issue of the IEEE Transactions on Nuclear Science. He graduated from AFIT in December 1976. His next Air Force assignment was to the Air Force Technical Applications Center in Florida where he performed nuclear weapon related research and published two classified technical reports titled "Debris Sampling" and "PONY EXPRESS Analytical Results." His next assignment was to Sandia National Laboratories (SNL) as a laboratory research associate. He started this assignment in the Diagnostic Division of the Particle Beam Fusion Department. His major contributions in that department were the characterization of the negative ion leakage currents in magnetically insulated transmission lines and the development of passive voltage monitoring techniques using nuclear track film. His publications while assigned to this department included "Measurement of Magnetically-Insulated Line Voltage Using A Thomson Parabola Charged Particle Analyser." in NBS Special Publication 628 and "Negative Ion Formation In Magnetically-Insulated Transmission Lines" in the Journal of Applied Physics, May 1982 (Co-author: R. W. Stinnett). His second year at SNL was spent in their Center for Radiation-hardened Microelectronics (CRM). There, he studied the rapid annealing phenomenon in MOS devices following pulsed radiation exposure. Publications while working in the CRM include: "Rapid Anneal of Pulsed Radiation Damage in MOSFETs," Government Microcircuit Applications Conference (GOMAC), 1982 Digest of Papers - classified edition and "Transient Annealing in MOS Devices," Proceedings of the first Hardened Electronics And Radiation Technology (HEART) Conference. Following his assignment to SNL, he was assigned to the Air Force Weapons Laboratory (AFWL) as the Chief of the Radiation Effects on Electronics Section.

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