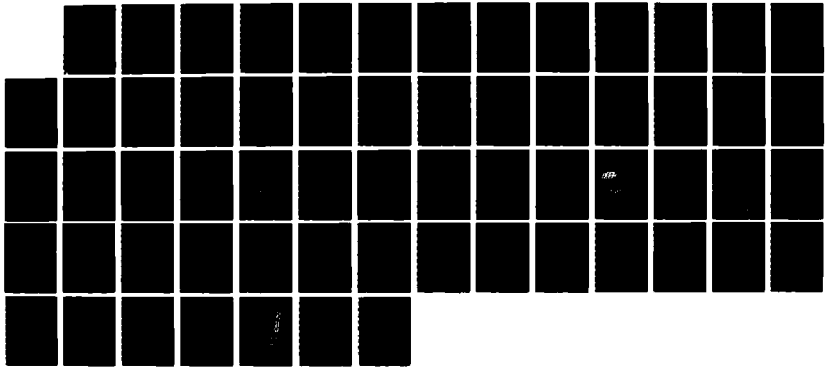
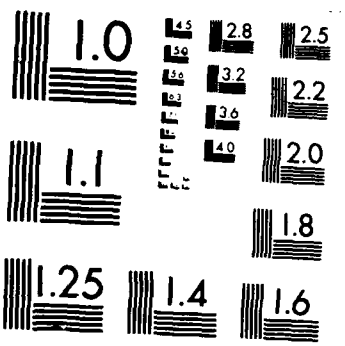
AD-A174 853 PARALLEL OPTICAL DATA PROCESSING(U) CALIFORNIA UNIV SAN 1/1
DIEGO LA JOLLA DEPT OF ELECTRICAL ENGINEERING AND
COMPUTER SCIENCES S H LEE 01 AUG 86 AFOSR-TR-86-2020
UNCLASSIFIED AFOSR-84-0336 F/G 20/6 NL





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16. SUPPLEMENTARY NOTATION: ☐ SUMMARY AND CONCLUSIONS - OPTICAL COMPUTING

17. COSATI CODES		
FIELD	GROUP	SUB.

19. ABSTRACT (Continue on reverse if)

OTIC FILE COPY

- OPTICAL COMPUTING HAS BEEN EFFECTIVE AT SOLVING COMPUTATIONALLY DIFFICULT PROBLEMS,
- OPTICAL COMPUTING RESEARCH HAS HIGH RISKS, BUT HIGH POTENTIAL BENEFITS,
- AFOSR HAS HAD THE LEAD ROLE IN BASIC OPTICAL COMPUTING RESEARCH AND MUST CONTINUE THIS ROLE IN COORDINATION WITH OTHER GOVERNMENT AND INDUSTRIAL FUNDING,
- CURRENT AND FUTURE OPTICAL COMPUTING SYSTEMS CAN BE ORGANIZED INTO A UNIFIED STRUCTURE WITH FIVE MAJOR COMPONENTS: INPUT, PROCESSOR ARRAY, INTERCONNECTIONS, MEMORY, OUTPUT,
- OPTICS HAS GREAT POTENTIAL ADVANTAGES IN SPEED, BANDWIDTH AND PARALLELISM, BUT ELECTRONICS HAS THE ADVANTAGES OF A WELL-DEVELOPED TECHNOLOGY,
- BASIC RESEARCH NEEDS,
  - MATERIALS - NONLINEAR, SYNTHETIC STRUCTURES
  - PROCESSING ELEMENT ARRAYS - SLMs
  - INTERCONNECTIONS/MEMORIES - MATERIALS, DEVICES, ARRAYS
  - ARCHITECTURES/ALGORITHMS - UTILIZE PARALLELISM,

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AFOSR-TR- 86-2020

FINAL REPORT

(AFOSR-84-0336)

During the seventeen months of the granting period, six researchers from four institutions (A. Sawchuk and K. Jenkins from the University of Southern California, J. Caulfield of the University of Alabama at Huntsville, S. Collins at the Ohio State University, C. Guest and S. Lee of the University of California at San Diego) met several occasions to discuss the current status of "Parallel Optical 2-D data processing architectures and algorithms," to assess most promising trends of development and to project future research needs. For example, they met on October 30, 1984 (in conjunction with the OSA annual meeting) at San Diego, in January, 1985 (in conjunction with the SPIE-LA meeting) at Los Angeles and in March, 1985 (in conjunction with the topical meeting of OSA on Optical Computing) at Incline Village, CA. Later the study group was expanded to include A. Tanguay of the University of Southern California and D. Psaltis of the California Institute of Technology and met a couple more times a the end of May, 1985 at the Office of Naval Research and on August 27, 1985 at USC. The finding from these meetings was summarized in a two-hour report, and presented by A. Sawchuk on behalf of the study group at AFOSR on October 15, 1985. A copy of the viewgraphs used in the presentation is attached to this final report. The same presentation was given at the SPIE-LA meeting in January 1986, in a panel discussion titled "Optical Information Processing: The Development and Future Optical Computing." Positive responses on the report were received.

Sing H. Lee
Principal Investigator

SHL:pwn

OPTICAL INFORMATION PROCESSING:

THE DEVELOPMENT AND FUTURE

OF OPTICAL COMPUTING

□ AUTHORS -- A GROUP EFFORT FROM SEPTEMBER 1984 THROUGH PRESENT

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• H. JOHN CAULFIELD	UNIV. OF ALABAMA - HUNTSVILLE
• STUART COLLINS, JR.	OHIO STATE UNIVERSITY
• C. LEE GILES	AFOSR
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• DEMETRI PSALTIS	CALIFORNIA INST. OF TECHNOLOGY
• ALEXANDER A. SAWCHUK	USC
• ARMAND R. TANGUAY, JR.	USC

□ OUTLINE

- OPTICAL COMPUTING - WHAT IS IT, HOW DID IT DEVELOP
  - COMPUTATIONALLY DIFFICULT PROBLEMS
  - CURRENT PERSPECTIVE

    AFOSR ROLE
    ADVANCED DEVELOPMENT AND OPERATIONAL SYSTEMS

- GENERIC OPTICAL PROCESSING/COMPUTING ARCHITECTURE
  - COMPONENTS OF THE GENERIC ARCHITECTURE: STATE-OF-THE-ART
  - SPECIFIC EXAMPLES AND APPLICATIONS
  - COMPARISON OF OPTICS AND ELECTRONICS

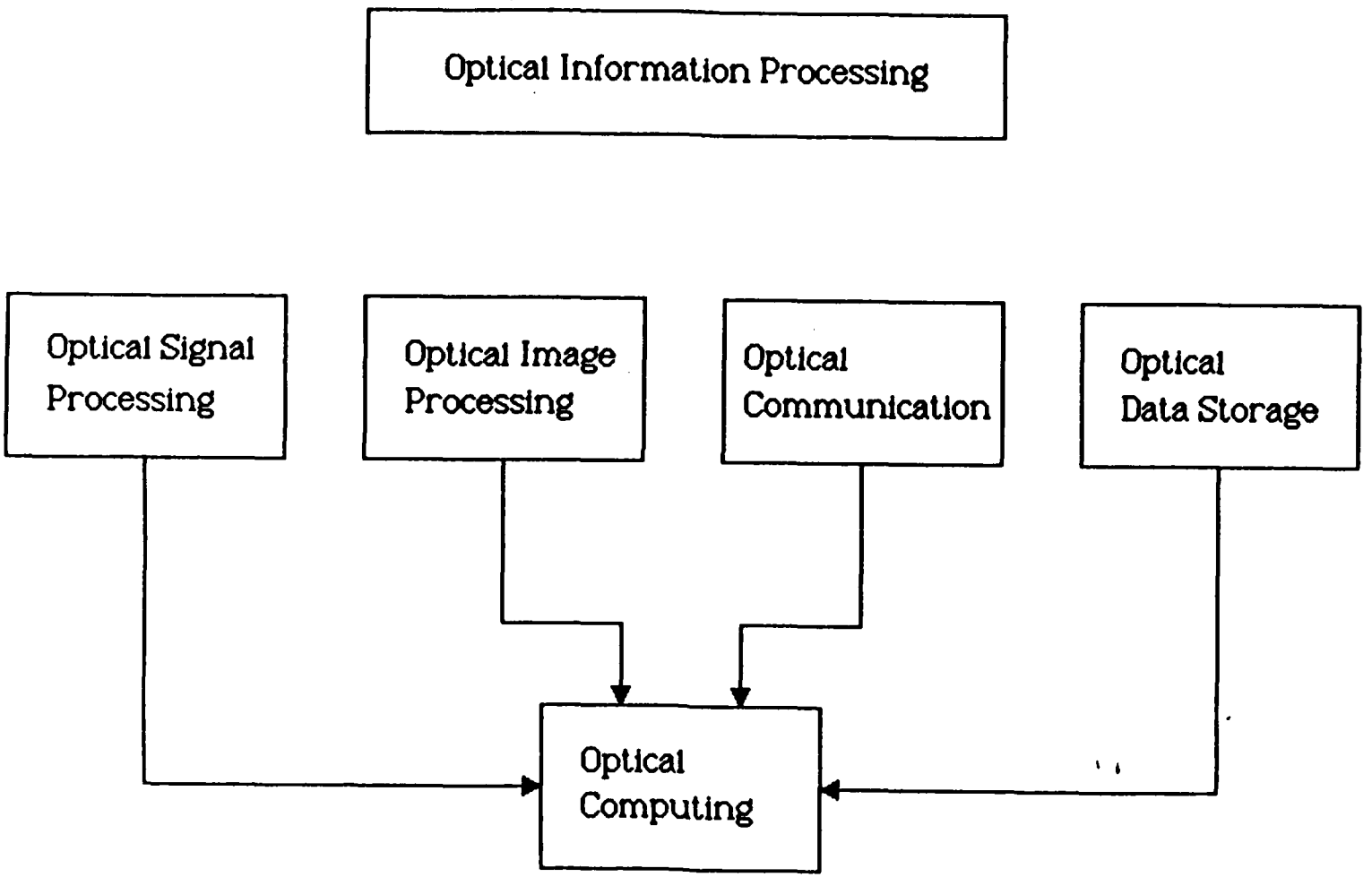
- FUTURE
  - GOALS
  - ISSUES AND NEEDS FOR ACHIEVING THESE GOALS

    MATERIALS
    DEVICES
    ARCHITECTURES
    ALGORITHMS
  - THINGS THAT ARE WORTH FUNDING
- SUMMARY AND CONCLUSIONS

□ OPTICAL COMPUTING

- IS THE PROCESSING OR MANIPULATION OF INFORMATION
- BY OPTICAL MEANS
- TO PERFORM ARITHMETIC OR SYMBOLIC OPERATIONS

- AREAS LEADING TO OPTICAL COMPUTING



- COMPUTATIONALLY DIFFICULT PROBLEMS: EXAMPLES

  - SIGNAL PROCESSING/RADAR, SONAR, SPREAD SPECTRUM, SENSOR FUSION
  - MACHINE VISION/IMAGE UNDERSTANDING/PATTERN RECOGNITION
  - AI/INTELLIGENT SYSTEMS/EXPERT SYSTEMS
  - LARGE DATA BASE MANAGEMENT
  - SOLUTION OF LARGE DIMENSIONAL PDE'S
  - NUMERICAL ANALYSIS

- COMPUTATIONALLY DIFFICULT PROBLEMS

  - FUNDAMENTALLY LIMITED
    - INHERENTLY DIFFICULT FOR ANY COMPUTING ARCHITECTURE AND ALGORITHM

  - TECHNOLOGY LIMITED
    - PRESENT STATE OF TECHNOLOGY IS ILL-SUITED TO SOLVING THE PROBLEM
    - IMPROVED ARCHITECTURES AND ALGORITHMS COULD IMPROVE COMPUTATION

  - OPTICAL PROCESSING AND COMPUTING ADVANCES HAVE BEEN DRIVEN BY COMPUTATIONALLY DIFFICULT PROBLEMS

- WHY ARE SUCH PROBLEMS COMPUTATIONALLY DIFFICULT?

  - SIZE OF THE PROBLEM (E.G. DATA-BASE MANAGEMENT, IMAGE PROCESSING)
  - MANY "OPERATIONS" PER DATA POINT
  - LACK OF UNDERSTANDING ON THE USE OF PARALLEL ARCHITECTURES
  - NEED FOR COMPLEX FIXED AND PROGRAMMABLE INTERCONNECTIONS (INTERCONNECTED PARALLEL ARRAYS)
  - INPUT/OUTPUT BOTTLENECKS
  - EXISTING METHODS OF COMPUTING ARE LIMITED MORE BY PRACTICAL CURRENT TECHNOLOGY THAN BY FUNDAMENTAL PRINCIPLES

- CURRENT PERSPECTIVE - OPTICAL INFORMATION PROCESSING

  - ACCOMPLISHMENTS
    - SYNTHETIC APERTURE RADAR (SAR) PROCESSORS
    - CORRELATION SYSTEMS (SIGNALS, IMAGES, PATTERNS)
    - SPECTRUM ANALYZERS
    - FIBER OPTIC COMMUNICATIONS
    - OPTICAL DISCS
  - DEVICE DEVELOPMENT
    - ACOUSTO-OPTIC (AO) DEVICES
    - SPATIAL LIGHT MODULATORS (SLMs)
    - SOURCES AND DETECTORS
    - FIBER OPTICS
    - HOLOGRAMS: ANALOG AND COMPUTER-GENERATED
  - ARCHITECTURE AND ALGORITHM DEVELOPMENT
    - OPTICAL SYSTOLIC ARRAYS
    - MATRIX-VECTOR PROCESSORS
    - ADVANCED 2-D AO PROCESSORS
    - OPTICAL COMPUTERS

□ CURRENT PERSPECTIVE - OPTICAL INFORMATION PROCESSING

- INDUSTRIAL ADVANCED DEVELOPMENT AND OPERATIONAL SYSTEMS (6.2., 6.3 AND BEYOND)
  - ESL - P. KELLMAN - AO ANALOG SIGNAL PROCESSING/SPECTRUM ANALYSIS/CORRELATORS
  - AT&T BELL LABS - A. HUANG - OPTICAL COMPUTING/OPTICAL DEVICES
  - HARRIS - A. VANDERLUGT - AO SYSTEMS
  - HONEYWELL - L. HUTCHESON - INTEGRATED OPTICS, OPTICAL INTERCONNECTIONS, COMPUTING
  - LOCKHEED - A. TARASEVICH - AO SYSTEMS
  - AEROSPACE CORP. - J. BREEDLOVE - AO/ELECTRO-OPTIC SIGNAL PROCESSING/IMAGING
  - WESTINGHOUSE - P. TAMURA - AO SYSTEMS

    .
    .
    .

□ CURRENT PERSPECTIVE - OPTICAL INFORMATION PROCESSING

- GOVERNMENT ADVANCED DEVELOPMENT AND OPERATIONAL SYSTEMS (6.2., 6.3 AND BEYOND)
  - AF SPACE DIVISION - D. TOMCZAK - AO/ELECTRO-OPTIC SIGNAL PROCESSING/ IMAGING
  - NSA - D. BROWN - SPECTRUM ANALYZERS/CORRELATORS
  - RADC - J. GRANIERO - (HANSCOM / GRIFFISS) ANTENNA ARRAY PROCESSING
  - AFWAL - R. PAULSON - (DAYTON) ANTENNA ARRAY PROCESSING
  - NRL - A. SPEZIO - AO SYSTEMS / SPECTRUM ANALYSIS
  - EGLIN - J. RIGGINS, R. WEHLING - TERMINAL GUIDANCE
  - NASA/SHUTTLE - M. SOKOLOWSKY - AO SAR PROCESSOR - MARCH 1986
  - NASA/SETI - SEARCH FOR EXTRA TERRESTRIAL INTELLIGENCE - CALTECH - SPECTRUM ANALYSIS
  - MICOM - J. JOHNSON - TERMINAL GUIDANCE

  :

□ CURRENT PERSPECTIVE - AFOSR FUNDING OF OPTICAL COMPUTING

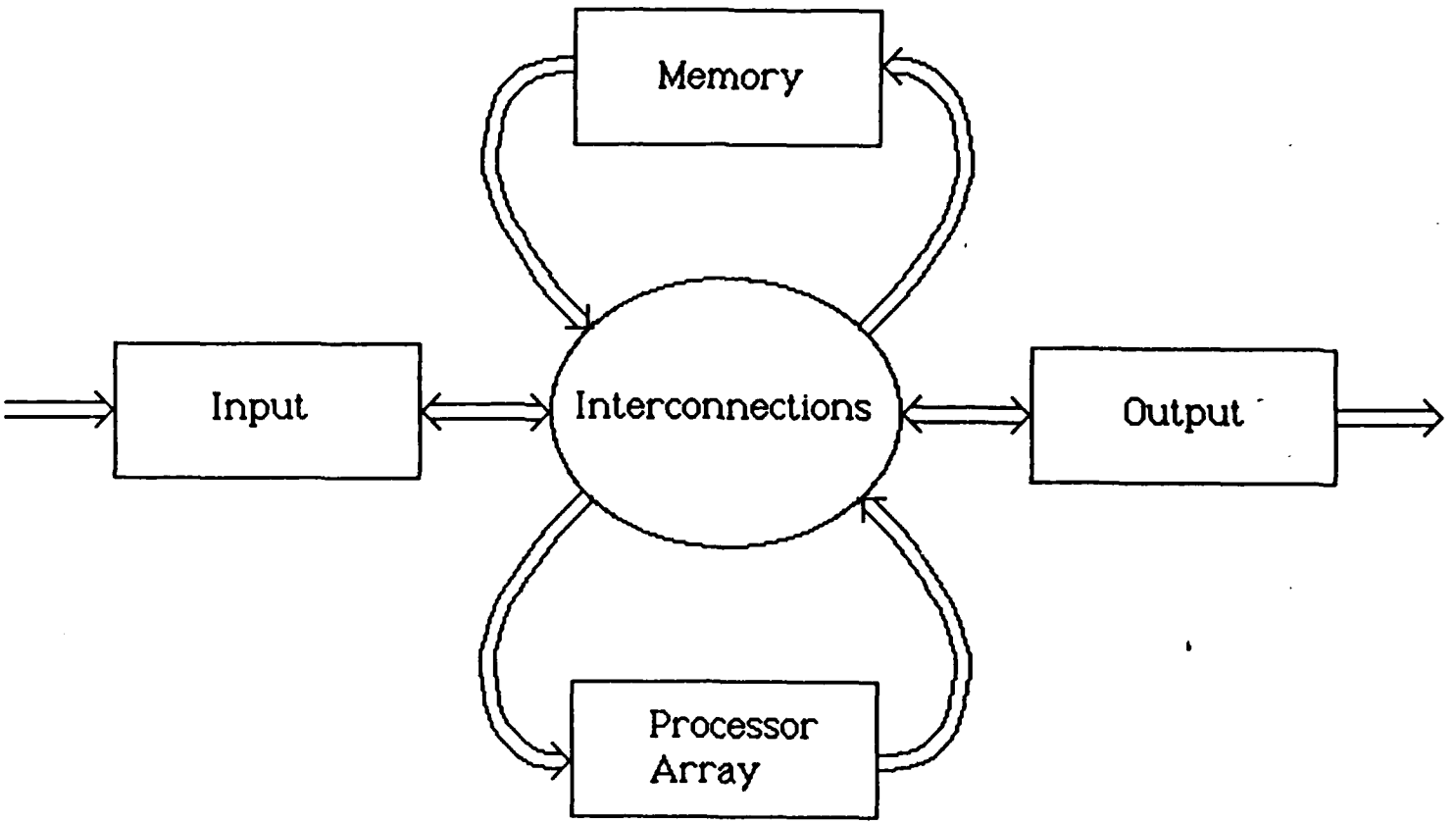
- AFOSR HAS THE LEADING ROLE IN BASIC RESEARCH (6.1) FUNDING IN OPTICAL COMPUTING
- ACCOMPLISHMENTS FUNDED BY AFOSR ARE THE DRIVING FORCE FOR 6.2, 6.3 FUNDING FROM OTHER SOURCES: DARPA, SDI
- AFOSR HAS LEVERAGED ITS FUNDING BY COMPLEMENTARY SUPPORT FROM OTHER 6.1 FUNDING AGENCIES (ARO, ONR, NSF) AND INDUSTRY (ITT, GTE, IBM, AT&T)
- THE OTHER SOURCES LISTED MIGHT NOT EXIST WITHOUT AFOSR 6.1 FUNDING

- GENERIC OPTICAL PROCESSING/COMPUTING ARCHITECTURE

  - PURPOSES

    - PERSPECTIVE ON PAST AND EXISTING SYSTEMS
    - FRAMEWORK FOR NEW RESEARCH IDEAS
    - A GENERIC ARCHITECTURE FOR COMPARISON OF SYSTEMS
    - IDENTIFICATION OF CRITICAL BOTTLENECKS IN MATERIALS, DEVICES, SYSTEMS

Generic Optical Processing/Computing Architecture



- INPUT/FORMAT DEVICE
  - FUNCTION/DESCRIPTION
    - ELECTRONIC => OPTICAL TRANSDUCER
    - OPTICAL => OPTICAL TRANSDUCER
    - INPUT BUFFER
    - FORMATTER (E.G. RASTER => VECTOR)
    - PREPROCESSING (E.G. THRESHOLDING, A/D)
  - COMPONENTS/TECHNOLOGY
    - SPATIAL LIGHT MODULATOR (SLM) TECHNOLOGY (OPTICALLY OR ELECTRONICALLY ADDRESSED)

- PROCESSOR ARRAY
  - FUNCTION/DESCRIPTION
    - LARGE 2-DIMENSIONAL ARRAY OF OPTICALLY CONNECTED PROCESSING ELEMENTS
    - INTERNAL REPRESENTATION CAN BE ANALOG, DIGITAL, NUMBER THEORETIC, SYMBOLIC
    - ELEMENTS CAN BE LOGIC GATES, ANALOG MULTIPLIERS, THRESHOLD DEVICES, BISTABLE DEVICES, ELECTRONIC PROCESSING ELEMENTS
  - COMPONENTS/TECHNOLOGY
    - SPATIAL LIGHT MODULATORS (SLMs)
    - NON-LINEAR OPTICAL MATERIALS AND DEVICES
    - ELECTRONIC CIRCUITS WITH OPTICAL I/O

- INTERCONNECTIONS
  - FUNCTION/DESCRIPTION
    - CENTRAL ELEMENT OF PARALLEL COMPUTING
    - PROVIDES GLOBAL COMMUNICATIONS AMONG PROCESSING ELEMENTS
    - ALLOWS SEQUENCING AND FEEDBACK
    - PROVIDES PARALLEL COMMUNICATION: PROCESSOR, MEMORY AND I/O
    - DYNAMIC/RECONFIGURABLE INTERCONNECTIONS DESIRABLE
    - 3-D TECHNOLOGY DESIRABLE
  - COMPONENTS/TECHNOLOGY
    - SPATIAL LIGHT MODULATORS (SLMs)
    - CLASSICAL OPTICAL COMPONENTS
    - HOLOGRAMS
      - THIN/VOLUME
      - FIXED/DYNAMIC (NONLINEAR OPTICAL MATERIALS)
      - COMPUTER/OPTICALLY GENERATED
    - FIBER OPTICS

- INTERCONNECTIONS

	Spatial Scale
• Gate	10^{-6}-10^{-3}m
• Chip	10^{-3}-10^{-2}m
• Wafer	10^{-2}-10^{-1}m
• Board	10^{-1}-10^{0}m
• Processor	10^{0}m-10^{3}m

- MEMORY

  - FUNCTION/DESCRIPTION

    ORGANIZATION

    - LOCATION ADDRESSED - LOCATION IN => DATA OUT
    - CONTENT ADDRESSED - DATA IN => LOCATION OUT
    - ASSOCIATIVE ADDRESSED - DATA IN => DATA OUT

    ACCESS

    - SERIAL
    - PARALLEL

    STORAGE

    - DISTRIBUTED
    - LOCAL
    - HIERARCHICAL

  - COMPONENTS/TECHNOLOGY

    - OPTICAL, MAGNETIC, ELECTRONIC, CHEMICAL

- MEMORY
  - COMPARISON (FOR VON NEUMANN MACHINES)

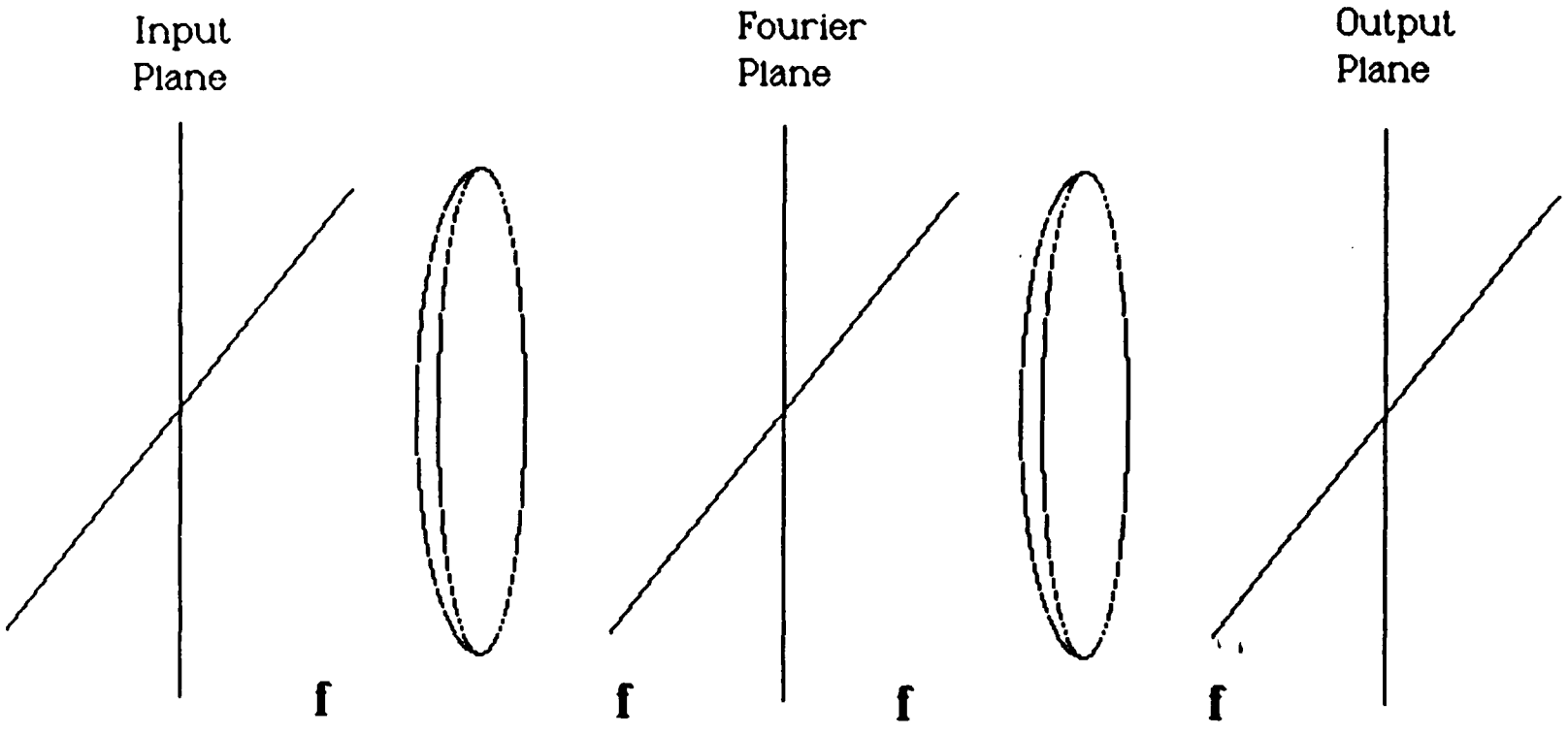
		ACCESS TIME (S)	CAPACITY (BITS)	EXAMPLES
	TAPE	10^{2}	$>10^{11}$	OPTICAL ELECTRONIC
	DISC	10^{-5}-10^{-1}	10^{9}-10^{10}	OPTICAL MAGNETIC
POSSIBLY PART OF PROCESSOR	RAM	10^{-8}	10^{8}	ELECTRONIC
	CACHE	10^{-9}	10^{4}	ELECTRONIC
	REGISTER	10^{-10}	10^{2}	ELECTRONIC

- OUTPUT DEVICES
  - FUNCTION/DESCRIPTION
    - OPTICAL => ELECTRONIC TRANSDUCER
    - OPTICAL => OPTICAL TRANSDUCER
    - FORMATTING RASTER => VECTOR
    - OUTPUT BUFFER
    - POST PROCESSING
  - COMPONENTS/TECHNOLOGY
    - SEMICONDUCTOR DETECTOR ARRAY
    - HUMAN OBSERVER DISPLAY
    - SPATIAL LIGHT MODULATORS (SLMs)
    - FIBERS

- SPECIFIC EXAMPLES OF OPTICAL PROCESSING/COMPUTING ARCHITECTURES

  1. Analog information processor (open or closed loop)
  2. Neural network processor
  3. Parallel sequential processor
  4. Cellular logic processor
  5. Electronic chip with optical interconnections
  6. Numerical linear algebra processor (residue, DMAC)
  7. Parallel access optical mass data base
  8. Data flow

- 1. ANALOG INFORMATION PROCESSOR



- 1. ANALOG INFORMATION PROCESSOR

  LINEAR SHIFT-INVARIANT FOURIER OPTICS PROCESSOR

  SPECTRUM ANALYZER

  ACOUSTOOPTIC (AO) PROCESSOR

  VECTOR MATRIX PROCESSOR

  SPACE-VARIANT PROCESSOR

  SYNTHETIC APERTURE RADAR (SAR) PROCESSOR

  IMAGE CORRELATOR

  INPUT - SLM

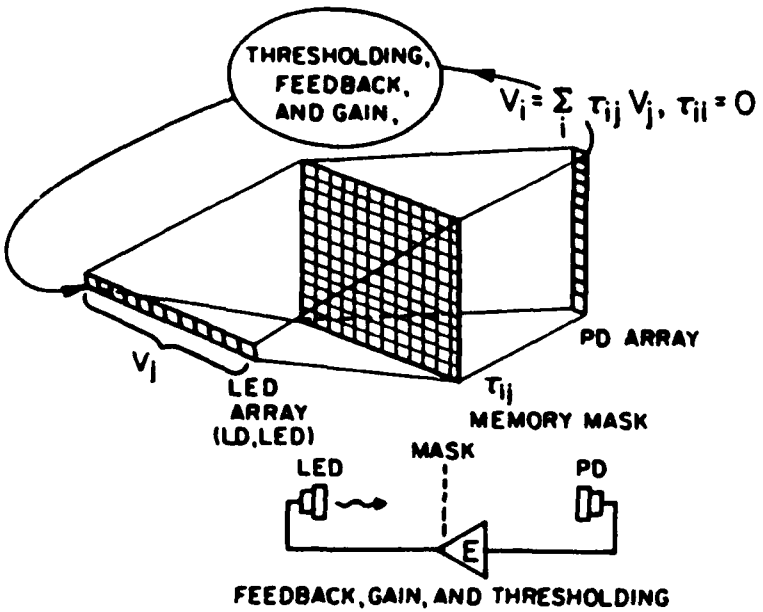
  PROCESSOR ARRAY - SPATIAL FILTER COMPLEX ANALOG MULTIPLIERS

  INTERCONNECTIONS - IMAGING SYSTEM OR TRANSFORMING SYSTEM

  MEMORY - FIXED: HOLOGRAM
  VARIABLE: SLM

  OUTPUT - DETECTOR ARRAY

- 2. NEURAL NETWORK PROCESSOR



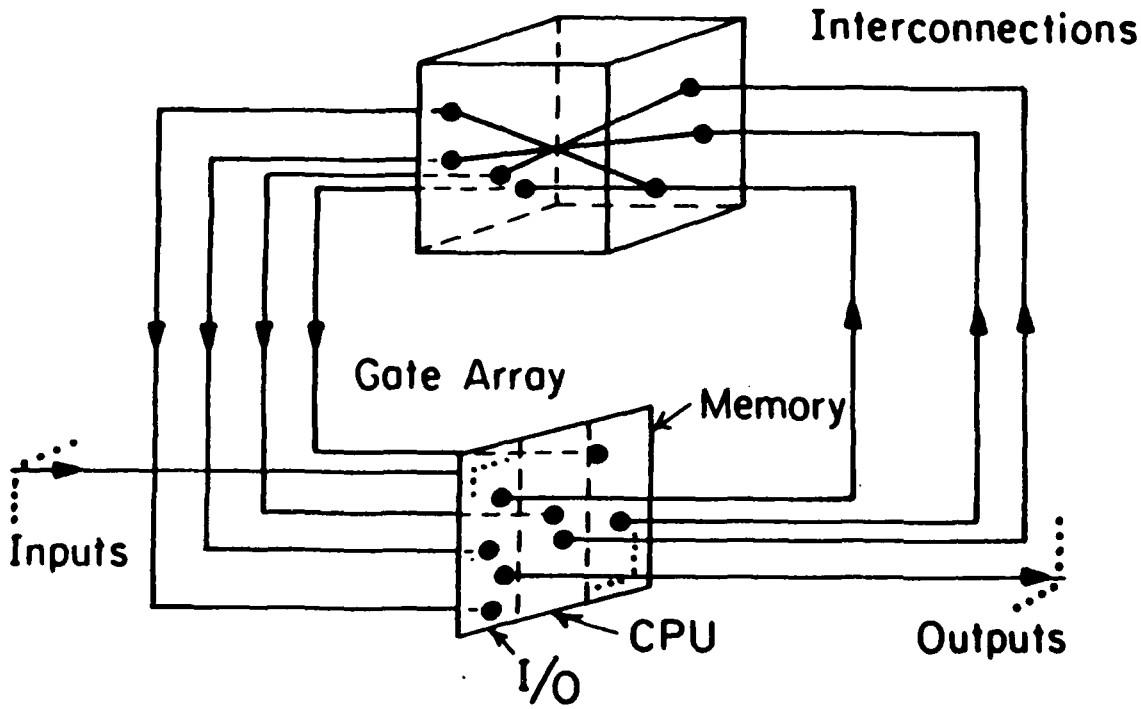
ASSOCIATIVE MEMORY - FEEDBACK IS OPTICAL OR ELECTRONIC

2. NEURAL NETWORK PROCESSOR

- HOPFIELD PROCESSOR - FULLY INTERCONNECTED ARRAY OF THRESHOLD ELEMENTS - FIXED THRESHOLD
- BOLTZMANN/ISING MODELS - PROBABILISTIC THRESHOLD TRANSITIONS AMONG ELEMENTS
- RELAXATION/OPTIMIZATION - SATISFY CONSTRAINTS
- ASSOCIATIVE MEMORY
- ADAPTIVE MODELS - STOCHASTIC LEARNING AUTOMATA

- INPUT - SLM
- PROCESSOR ARRAY - ARRAY OF OPTICAL THRESHOLD ELEMENTS
- INTERCONNECTIONS - OPTICAL SYSTEM AND MASK
- MEMORY - MASK (FIXED OR VARIABLE)
- OUTPUT - DETECTOR ARRAY

□ 3. PARALLEL SEQUENTIAL PROCESSOR



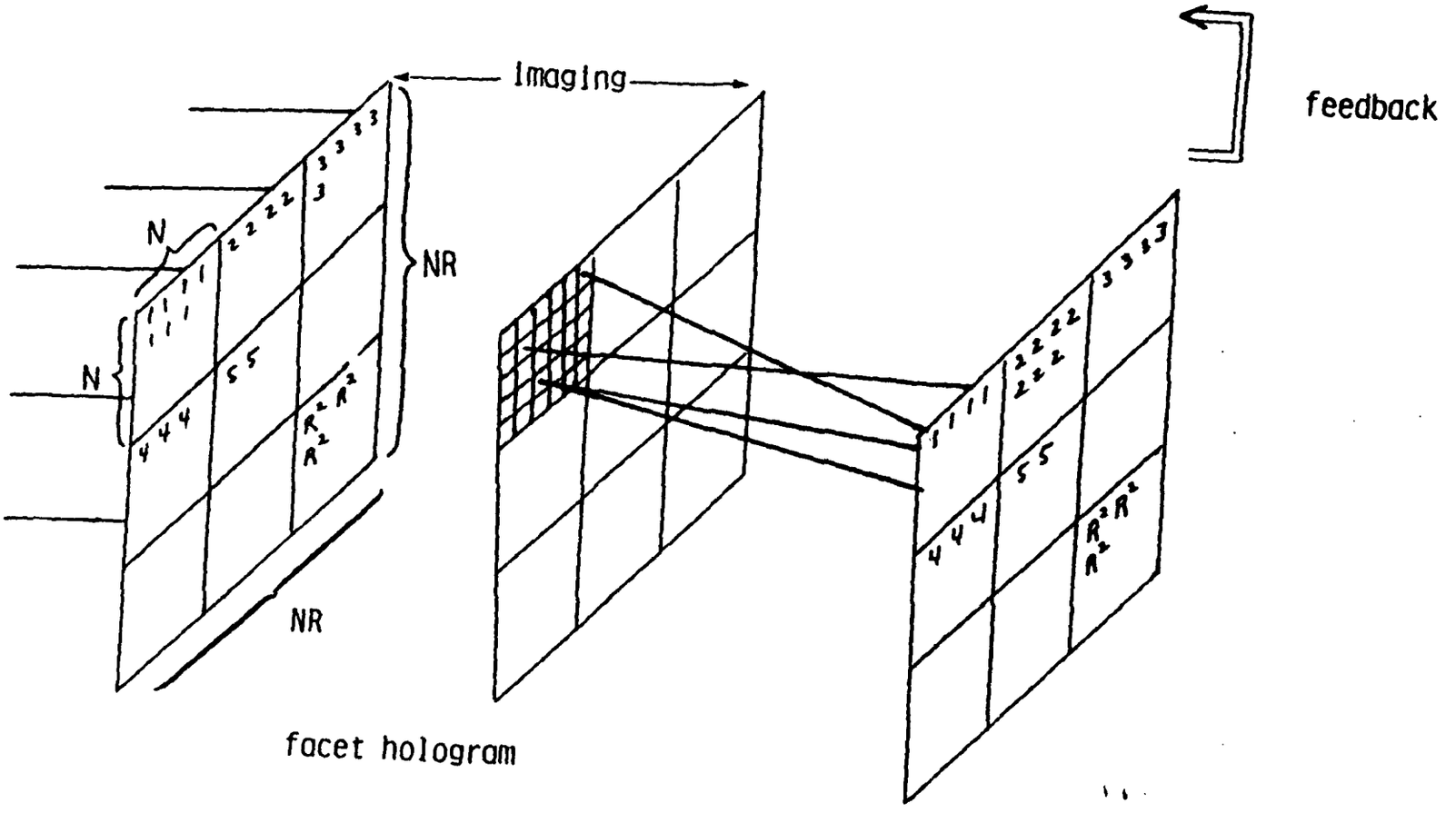
- BINARY COMPUTER - NOT VON NEUMANN ARCHITECTURE
- PARALLEL I/O POSSIBLE - NO PIN-IN/PIN-OUT CONSTRAINTS
- ARBITRARY INTERCONNECTIONS - GLOBAL/LOCAL

3. PARALLEL SEQUENTIAL PROCESSOR

- COMBINATORIAL AND SEQUENTIAL BINARY OPTICAL COMPUTER
- GLOBAL INTERCONNECTIONS AND PARALLEL I/O VS. LOCAL INTERCONNECTIONS, PIN-IN/PIN-OUT PROBLEMS, BUS LIMITATIONS, CLOCK-SKEW PROBLEMS OF VLSI
- HAS BINARY DIGITAL ACCURACY AND DYNAMIC RANGE
- NON VON NEUMANN BINARY ARCHITECTURE:
  - SINGLE INSTRUCTION MULTIPLE DATA (SIMD)
  - MULTIPLE INSTRUCTION MULTIPLE DATA (MIMD)
  - OTHER ARCHITECTURES
- ARBITRARY INTERCONNECTIONS - GLOBAL/LOCAL
- 3D INTERCONNECTIONS

- INPUT - SLM
- PROCESSOR ARRAY - SLM
- INTERCONNECTIONS - FIXED ANALOG OR COMPUTER-GENERATED HOLOGRAMS
  - DYNAMIC WITH SLM OR VOLUME MATERIAL
- MEMORY - FLIP/FLOP ARRAY; CLOSELY COUPLED TO PROCESSOR
  - FORMED BY GATES AND INTERCONNECTIONS
- OUTPUT - SLM TO DETECTOR ARRAY

□ 4. CELLULAR LOGIC PROCESSOR



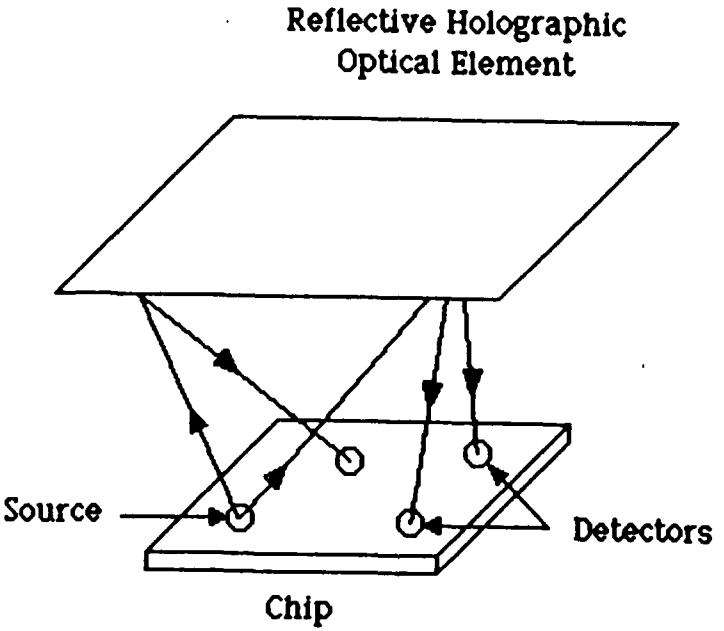
- FOR PARALLEL BINARY OR GRAY-LEVEL IMAGE PROCESSING
- AN ARRAY OF PARALLEL PROCESSORS FOR EACH INPUT PIXEL WITH LOCAL INTERCONNECTIONS

□ 4. CELLULAR LOGIC PROCESSOR

- A PROCESSOR BEHIND EVERY DATA POINT
- BINARY OR ARITHMETIC
- ORGANIZATION - LOCAL NEIGHBORHOOD (3 x 3 WINDOW) MESH
  - GLOBAL NEIGHBORHOOD (2^N DISTANCES) CELLULAR HYPERCUBE
  - PYRAMID
- WELL SUITED TO 2-D, RECTANGULAR GRID AND REPETITIVE PREPROCESSING NATURAL TO IMAGES
- APPLICATIONS - PARALLEL IMAGE PROCESSING
  - SINGLE INSTRUCTION, MULTIPLE DATA MACHINES (SIMD)
  - MULTIPLE INSTRUCTION, MULTIPLE DATA MACHINES (MIMD)

- INPUT - SLM
- PROCESSOR ARRAY - SLM
- INTERCONNECTIONS - FIXED ANALOG, COMPUTER - GENERATED HOLOGRAM
  ANALOG REPLICATION OF COMPUTER-GENERATED HOLOGRAM
- MEMORY - FLIP/FLOP ARRAY FORMED BY GATES AND INTERCONNECTIONS
- OUTPUT - SLM TO DETECTOR ARRAY

5. ELECTRONIC CHIP WITH OPTICAL INTERCONNECTIONS



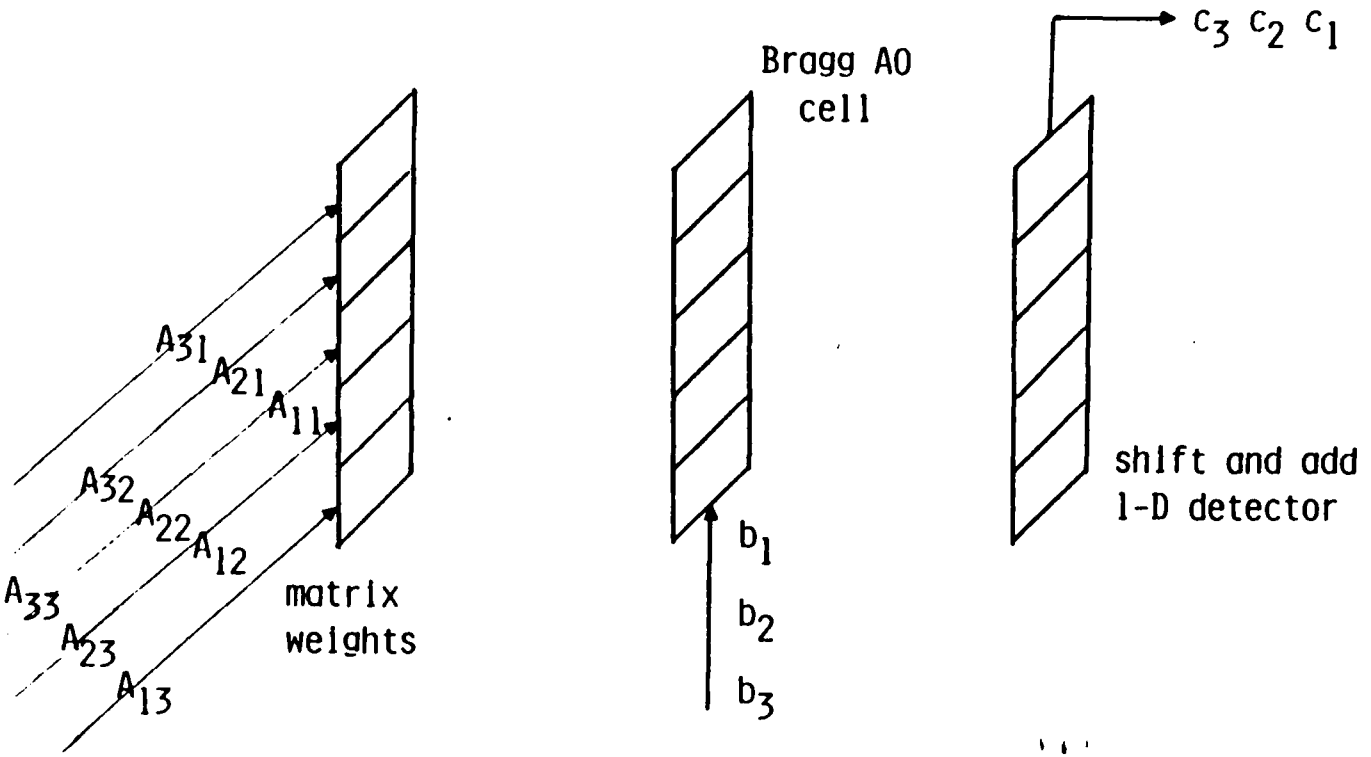
5. ELECTRONIC CHIP WITH OPTICAL INTERCONNECTIONS

- INTERCONNECTION DELAYS DOMINATE GATE DELAYS IN VLSI
- IMAGING OPTICAL INTERCONNECTIONS REDUCE INTERCONNECTION DELAYS
- MUTUAL INTERFERENCE IMMUNITY
- FREEDOM FROM CAPACITIVE LOADING
- FREEDOM FROM PLANAR OR QUASI-PLANAR CONSTRAINTS
- REPROGRAMMABLE OR DYNAMIC INTERCONNECTION POSSIBILITIES

- INPUT - SOURCES ON CHIP
- PROCESSOR ARRAY - ELECTRONIC CHIP
- INTERCONNECTIONS - HOLOGRAPHIC ELEMENT AND FREE-SPACE PROPAGATION
- MEMORY - ELECTRONIC CHIP AND HOLOGRAPHIC ELEMENT
- OUTPUT - DETECTOR ARRAY ON CHIP

□ 6. NUMERICAL LINEAR ALGEBRA PROCESSOR

• Matrix-vector systolic processor



☐ 6. NUMERICAL LINEAR ALGEBRA PROCESSOR

- NUMBER REPRESENTATION
  - RESIDUE - UNCOMMON, NO DIVISION, BUT NO CARRY
  - DIGITAL POSITION ENCODED - TWOS COMPLEMENT, OR OTHER (EVEN NEGATIVE) RADICES WITH

    PARALLEL (OUTER PRODUCT)
    SYSTOLIC (INNER PRODUCT, DIGITAL MULTIPLICATION BY ANALOG CONVOLUTION (DMAC))

- APPLICATIONS
  - FUNDAMENTAL OPERATIONS

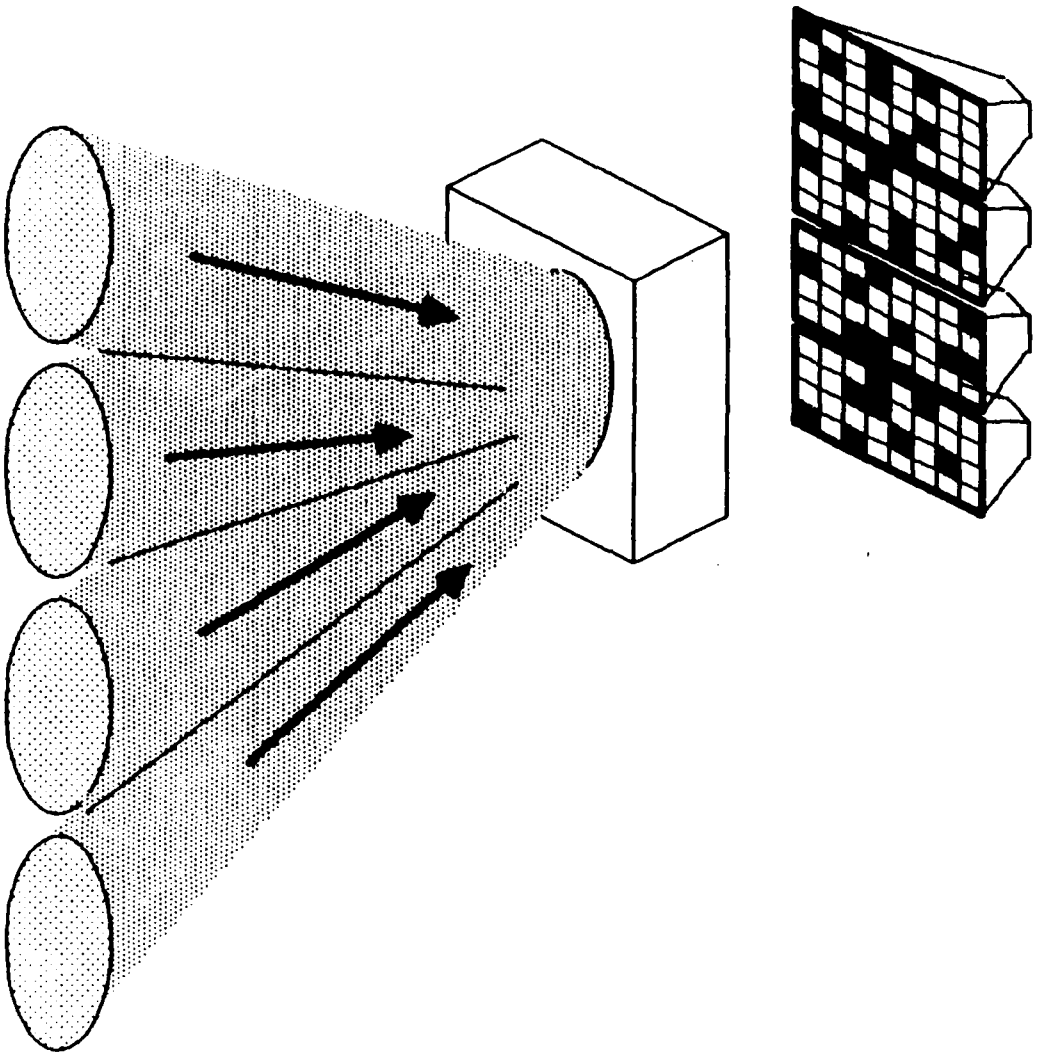
    MATRIX - VECTOR MULTIPLICATION
    MATRIX - MATRIX MULTIPLICATION

  - CHAINS OF OPERATIONS

    SOLUTION OF LINEAR SYSTEMS
    EIGENSYSTEMS
    SINGULAR VALUE DECOMPOSITION (SVD)
    KALMAN FILTERING
    SWITCHING/INTERCONNECTION SYSTEMS

- INPUT - MULTI-CHANNEL AO DEVICES
- PROCESSOR ARRAY - AO ANALOG MULTIPLIERS
- INTERCONNECTIONS - MOSTLY IMAGING OPTICS
- MEMORY - ELECTRONIC OR OPTICAL MATRIX STORAGE
- OUTPUT - DETECTOR ARRAYS

- 7. PARALLEL ACCESS OPTICAL MASS DATA BASE



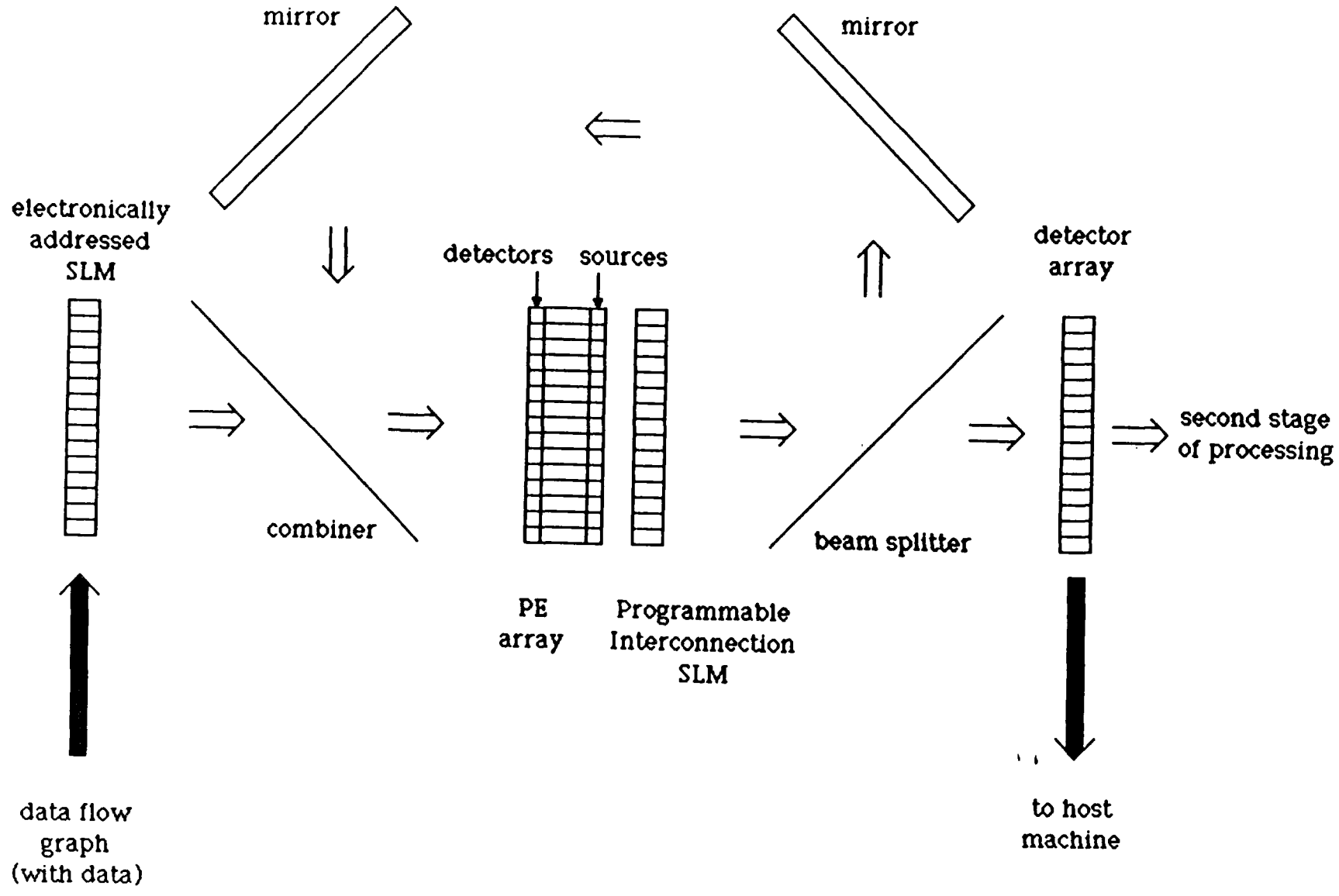
MULTIPORT OPTICAL MEMORY

□ 7. PARALLEL ACCESS OPTICAL MASS DATA BASE

- DATA STORED IN VOLUME REAL TIME HOLOGRAPHIC MATERIAL
- PARALLEL ACCESS TO PLANAR ARRAYS OF DATA
- ASSOCIATIVE PROCESSING POSSIBLE

- INPUT - BEAM DEFLECTOR AND LIGHT SOURCE
- INTERCONNECTIONS AND PROCESSOR ARRAY - BRAGG SELECTIVE IMAGING
- MEMORY - VOLUME HOLOGRAPHIC STORAGE
- OUTPUT - DETECTOR ARRAY

□ 8. DATA FLOW



OPTICAL DYNAMIC DATA FLOW MULTIPROCESSOR

□ 8. DATA FLOW

- System uses programmable interconnections to route data to processing elements
- Data/demand driven architecture - asynchronous

- Input - SLM
- Processor array - electronic or optical processing elements
- Interconnections - programmable interconnection system / SLM
- Memory - in processor array and interconnections
- Output - detector array

- STATE-OF-THE-ART: OPTICAL => OPTICAL SLM
  - 500 X 500 RESOLUTION ELEMENTS IN 2.5 CM X 2.5 CM PLANAR ARRAY
  - 30 MS SWITCHING TIME
  - ROOM TEMPERATURE OPERATION
  - INPUT AND OUTPUT AT SAME WAVELENGTH
  - LINEAR ANALOG OPERATION 200:1 DYNAMIC RANGE
  - THRESHOLD (BINARY SWITCHING) CHARACTERISTICS POOR
  - SENSITIVITY

- STATE-OF-THE-ART: ELECTRONIC => OPTICAL SLM
  - > 128 x 128 RESOLUTION ELEMENTS IN 2.5 CM x 2.5 CM PLANAR ARRAY
  - 1 MICROSECOND SWITCHING TIME
  - ROOM TEMPERATURE OPERATION
  - LINEAR ANALOG OPERATION: LOW DYNAMIC RANGE (20:1)
  - THRESHOLD (BINARY SWITCHING) DYNAMIC RANGE > 500:1

□ COMPARISON OF OPTICS AND ELECTRONICS - 1

- ELECTRONICS
  - SERIAL I/O BOTTLENECKS; PIN-IN/PIN-OUT PROBLEMS
  - HIGH SPEED BINARY PROCESSING ELEMENTS EXIST (500 MHz, 2NS)
  - INTEGRATION OF BINARY PROCESSING ELEMENT ARRAYS WELL-DEVELOPED ($>10^5$ GATES/CHIP)
  - LEVEL RESTORE, FAULT TOLERANCE HAS BEEN DEVELOPED
  - DECISION COST PER BIT IS INEXPENSIVE
- OPTICS
  - PARALLEL I/O NATURAL DUE TO 2D, 3D CHARACTERISTICS
  - HIGH SPEED BINARY PROCESSING ELEMENTS EXIST (1000 GHz, 1 PS)
  - INTEGRATION OF BINARY PROCESSING ELEMENT ARRAYS IMMATURE (10^3 GATES/CHIP)
    INTEGRATION OF ANALOG PROCESSING ELEMENT ARRAYS WELL-DEVELOPED ($> 10^6$ GATES/CHIP)
  - LEVEL RESTORE, FAULT TOLERANCE IS IMMATURE
  - DECISION COST PER BIT IS EXPENSIVE

□ COMPARISON OF OPTICS AND ELECTRONICS - 2

- ELECTRONICS
  - INTERCONNECTIONS ARE PLANAR (2D); ON-CHIP
  - PROBLEMS WITH INTERFERENCE, CROSSTALK, INTERCONNECTION DELAY, SYNCHRONIZATION; LOCAL INTERCONNECTIONS ONLY
  - LOW COMMUNICATIONS BANDWIDTH (10 - 100 MHz)
  - MATURE THEORY AND DEVELOPMENT FOR VON NEUMANN (SISD) MACHINES
  - NEW PARALLEL COMPUTING PARADIGMS NEEDED

- OPTICS
  - INTERCONNECTIONS OCCUPY A VOLUME (3D); OFF-CHIP
  - REDUCED INTERFERENCE, CROSSTALK, INTERCONNECTION DELAY, SYNCHRONIZATION DIFFICULTY; GLOBAL INTERCONNECTIONS FEASIBLE
  - HIGH COMMUNICATIONS BANDWIDTH (> 1 GHz)
  - MATURE THEORY AND DEVELOPMENT FOR CERTAIN PARALLEL, LARGE-DIMENSIONAL COMPUTATIONS
  - UNEXPLORED POTENTIAL OF EXISTING AND NEW PARALLEL COMPUTING PARADIGMS

□ COMPARISON OF OPTICS AND ELECTRONICS - 3

- ELECTRONICS
  - MATURE TECHNOLOGY

    GENERIC MATERIALS TECHNOLOGY WELL ESTABLISHED AND WELL CHARACTERIZED (SILICON)

    GENERIC, COMPATIBLE DEVICES DEVELOPED

    MANUFACTURABLE, INTEGRATABLE

    HEAVILY LEVERAGED (CONSUMER AND INDUSTRIAL ELECTRONICS)

- OPTICS
  - IMMATURE TECHNOLOGY

    GENERIC MATERIAL TECHNOLOGY NOT YET IDENTIFIED, BUT POTENTIALLY REVOLUTIONARY

    NON-GENERIC, INCOMPATIBLE DEVICES DEVELOPED

    MANUFACTURABILITY, INTEGRATION IS BEING DEVELOPED

    UNEXPLOITED LEVERAGE (E.G. OPTICAL COMMUNICATIONS)

- FUTURE
  - GOALS
  - ISSUES AND NEEDS FOR ACHIEVING THESE GOALS
    - MATERIALS
    - DEVICES
    - ARCHITECTURES
    - ALGORITHMS
  - THINGS THAT ARE WORTH FUNDING

- ACHIEVABLE OPTICAL PROCESSING/COMPUTING GOALS: 2 - 5 YEARS

1. REAL TIME, LOW POWER, COMPACT RADAR PROCESSORS
2. IMAGE ANALYSIS AND PATTERN RECOGNITION SYSTEMS FOR TERMINAL GUIDANCE, TARGET IDENTIFICATION
3. 100 x 100 ARRAYS OF THRESHOLD (GATE) ELEMENTS: (OPTICAL INPUT, OPTICAL OUTPUT)
4. VLSI ENHANCEMENT THROUGH PROGRAMMABLE OPTICAL INTERCONNECTIONS
5. SYMBOLIC PROCESSING ARRAYS FOR AI SOFTWARE IMPLEMENTATION
6. RECONSTRUCTIVE ASSOCIATIVE MEMORIES FOR AI DATABASE SYSTEMS
7. INTERCONNECTION BACKPLANE FOR SUPERCOMPUTERS
8. OPTICAL SWITCHING MACHINES

ACHIEVABLE OPTICAL PROCESSING/COMPUTING GOALS: 5-10 YEARS

1. 1000 x 1000 ARRAYS OF THRESHOLD (GATE) ELEMENTS: (OPTICAL INPUT, OPTICAL OUTPUT)

2. HIGH PERFORMANCE OPTICAL SWITCHING NETWORKS FOR COMMUNICATIONS, PARALLEL COMPUTERS

3. VERY HIGH RESOLUTION ANALOG COPIES OF COMPUTER-GENERATED HOLOGRAMS WITH SPACE-BANDWIDTH PRODUCT > 10^{10}.

□ DIGITAL OPTICAL LOGIC - Wish List

- Arrays of devices - easy fabrication
  - high packing density - gates in 3 cm x 3 cm area
  - 500 x 500 x 20 gates/pixel $\Rightarrow$ cellular logic processor
    $\Rightarrow 5 \cdot 10^6$ gates/array
- Easy interconnections/communications
  - on chip; off chip
  - exploit non-planar interconnections
- Room temperature operation
- Switching time < 1 μs
- Input and output at same wavelength $\Rightarrow$ cascading
- Avoid photon-electron-photon conversions
- Complete logical set: NOT-OR, NOT-AND, NOR, NAND
  - all 16 binary logic functions <u>not</u> needed or wanted
- Good threshold switching characteristics - future
- Bistability <u>not</u> needed

□ MATERIALS

- Issues
  1. Active materials (electrooptic, acoustooptic, magnetooptic, photorefractive, etc.)
  2. Passive materials (dielectric blocking layers, transparent conductors, fixed holographic optical elements)
  3. Thin film, layered, bulk structures
  4. Single crystal, polymer, amorphous nonlinear materials
  5. Inorganic vs. organic
  6. Generic vs. single function (Is there an optical silicon?)

- Needs
  1. New material development - synthetic structures
     - superlattice
     - multiple quantum well
     - organic materials
  2. Materials characterization
  3. Leverage from III-V materials work

□ DEVICES

- ISSUES
  1. LOW COST VS. HIGH PERFORMANCE
  2. AVAILABILITY VS. HIGH PERFORMANCE
  3. FLEXIBLE DEVICE WITH BROAD APPLICATIONS

- NEEDS
  1. BETTER SPATIAL LIGHT MODULATORS (SLMS) (ANALOG AND BINARY)
  2. BETTER DETECTOR ARRAYS
  3. HOLOGRAPHIC OPTICAL ELEMENTS
  4. MANUFACTURABILITY (IMMEDIATE; LONG TERM)
  5. ADVANCED DEVICE ANALYSIS (FUNDAMENTAL VS. TECHNOLOGICAL LIMITATIONS)
  6. EXPLORE CAD/CAM TECHNIQUES FOR DEVICE FABRICATION
  7. DEVELOP INDUSTRIAL/COMMERCIAL LEVERAGE

□ ARCHITECTURES

- ISSUES

1. PARALLEL AND MASSIVELY PARALLEL COMPUTING

SISD, SIMD, MIMD, TIME
SYNCHRONOUS VS. ASYNCHRONOUS
DATA FLOW
NEURAL NET
CONTROL

2. DEVICES/SYSTEMS

INTERCONNECTIONS
- GLOBAL VS. LOCAL
- STATIC VS. DYNAMIC
- BANDWIDTH

MEMORY
- SHARED, LOCAL, GLOBAL
- DIMENSIONALITY
- ACCESS TIME

PROCESSING ELEMENTS
- GRAININESS
- BANDWIDTH
- CONTROL

I/O
- BANDWIDTH
- PREPROCESSING
- DIMENSIONALITY

- ARCHITECTURES
  - NEEDS
    1. PARALLEL COMPUTATION PARADIGMS AS EXTENSIONS OF VON NEUMANN SISD PARADIGMS
    2. MAPPING OF THESE PARADIGMS TO OPTICAL COMPUTERS IN ACCORDANCE WITH MATERIAL AND DEVICE CONSTRAINTS/PROPERTIES
    3. FAULT TOLERANCE/NUMBER REPRESENTATION

- ALGORITHMS
  - Issues
    1. Programmability
    2. Hybrid electronic/optical processor management
    3. Algorithms well-matched to optical computing architectures
    4. Device limitations on optical algorithms
  - Needs
    1. Parallel computation paradigms
    2. Parallel operating systems

- OPTICAL COMPUTING: COMPETITION AND CHALLENGES

  - JAPAN
    - III-V MATERIALS AND DEVICES FOR OPTOELECTRONICS
    - MITI OPTICAL COMPUTING/OPTICAL COMMUNICATIONS RESEARCH AND DEVELOPMENT

  - SOVIET UNION
    - LARGE MATERIALS AND DEVICE EFFORT
    - ADVANCES IN OPTICAL COMPUTING DEVELOPMENT/DEPLOYMENT

  - ELECTRONICS
    - BROAD BASED, HIGH INERTIA TECHNOLOGY

- OPTICAL COMPUTING: GREAT DEVELOPMENTS ON THE HORIZON

1. HIGH SPEED, BISTABLE OPTICAL SWITCHING DEVICES (PICOSECOND RESPONSE)
2. INTEGRATED SEMICONDUCTOR SOURCES AND DETECTORS
3. VOLUME HOLOGRAMS IN NONLINEAR MATERIALS
4. HIGH RESOLUTION COMPUTER GENERATED HOLOGRAMS

- OPTICAL COMPUTING: WHAT KIND OF EFFORT IS NEEDED OVERALL?

1. A PARALLEL, SYSTEMATIC, COORDINATED EFFORT BETWEEN FUNDING AGENCIES AND RESEARCH SCIENTISTS/ENGINEERS

2. AFOSR - HAS BEEN THE LEADER AND MUST CONTINUE AS LEADER IN BASIC MATERIALS, DEVICES, ARCHITECTURE AND ALGORITHM 6.1 RESEARCH

DARPA - 6.1, 6.2, 6.3 FUNDING
- EXPLORATORY MATERIALS DEVELOPMENT
- OPTICAL INTERCONNECTIONS DEVELOPMENT
- OPTICAL SYMBOLIC COMPUTING
- OPTICAL DETECTORS

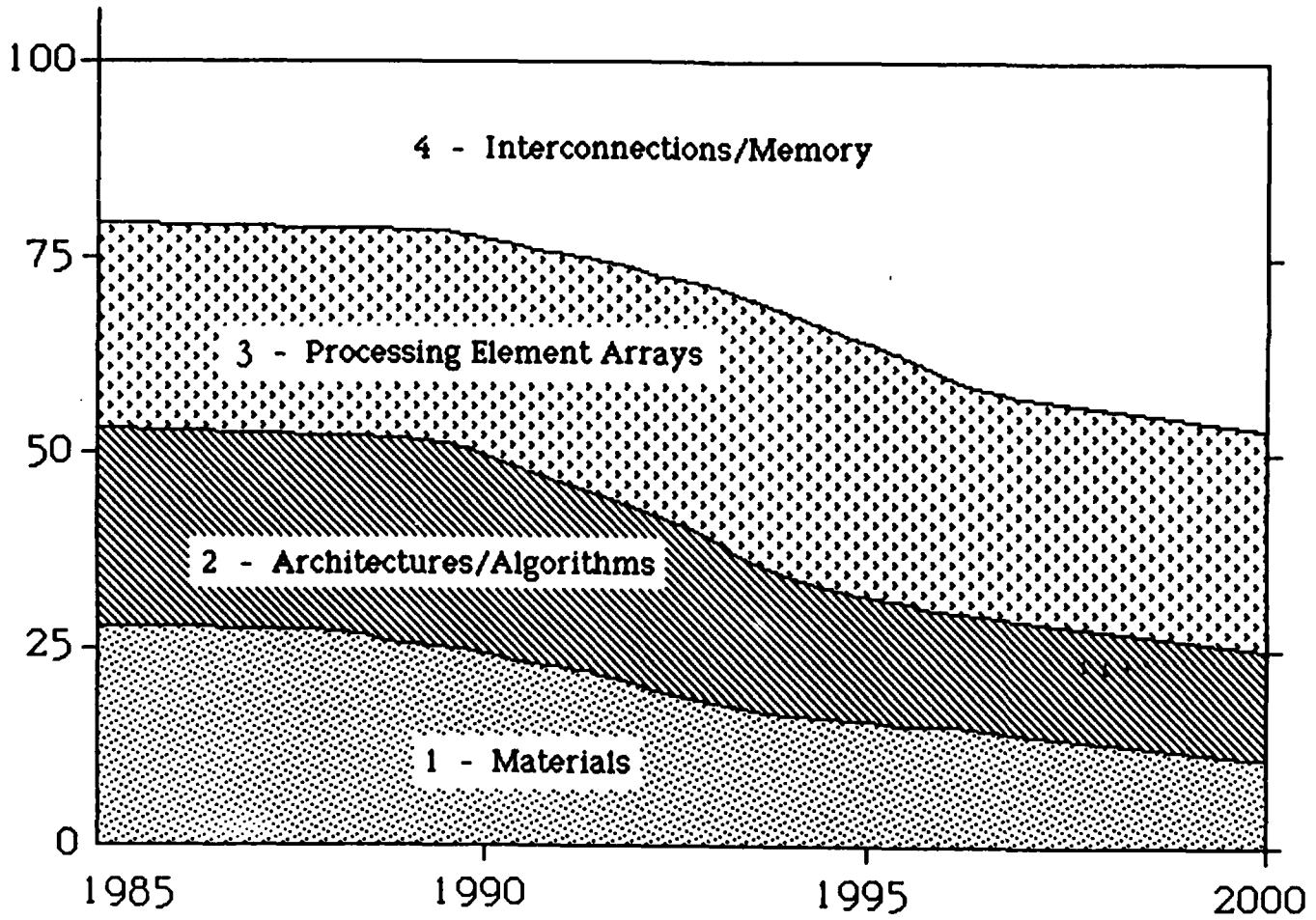
SDI - 6.1, 6.2, 6.3 EXPLORATORY FUNDING
- LINEAR ALGEBRA
- NUMBER REPRESENTATION
- ASSOCIATIVE MEMORY

INDUSTRY - 6.1, 6.2, 6.3
- OPTICAL COMMUNICATIONS
- OPTICAL SWITCHING

- THINGS THAT ARE WORTH FUNDING - WHAT IS NEEDED NOW?

1. INEXPENSIVE, LARGE, LOW LOSS, LOW POWER DISSIPATION, ROOM TEMPERATURE, MANUFACTURABLE, TRANSPARENT MATERIALS OR STRUCTURES WITH LARGE INTERACTION COEFFICIENTS
2. ORGANIZATIONAL PRINCIPLES AND ALGORITHMS FOR OPTICAL COMPUTING ARCHITECTURES AND SYSTEMS
3. ACTIVE PROCESSING AND I/O ELEMENT ARRAYS
4. OPTICAL INTERCONNECTIONS AND MEMORIES

Relative Importance of 6.1 Basic Research Areas to Optical Computing



▫ SUMMARY AND CONCLUSIONS - OPTICAL COMPUTING

- OPTICAL COMPUTING HAS BEEN EFFECTIVE AT SOLVING COMPUTATIONALLY DIFFICULT PROBLEMS

- OPTICAL COMPUTING RESEARCH HAS HIGH RISKS, BUT HIGH POTENTIAL BENEFITS

- AFOSR HAS HAD THE LEAD ROLE IN BASIC OPTICAL COMPUTING RESEARCH AND MUST CONTINUE THIS ROLE IN COORDINATION WITH OTHER GOVERNMENT AND INDUSTRIAL FUNDING

- CURRENT AND FUTURE OPTICAL COMPUTING SYSTEMS CAN BE ORGANIZED INTO A UNIFIED STRUCTURE WITH FIVE MAJOR COMPONENTS: INPUT, PROCESSOR ARRAY, INTERCONNECTIONS, MEMORY, OUTPUT

- OPTICS HAS GREAT POTENTIAL ADVANTAGES IN SPEED, BANDWIDTH AND PARALLELISM, BUT ELECTRONICS HAS THE ADVANTAGES OF A WELL-DEVELOPED TECHNOLOGY

- BASIC RESEARCH NEEDS

  - MATERIALS - NONLINEAR, SYNTHETIC STRUCTURES
  - PROCESSING ELEMENT ARRAYS - SLMs
  - INTERCONNECTIONS/MEMORIES - MATERIALS, DEVICES, ARRAYS
  - ARCHITECTURES/ALGORITHMS - UTILIZE PARALLELISM

END

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