AD-A175 636 FAULT-TOLERANT SIGNAL PROCESSING ARCHITECTURES WITH DISTRIBUTED ERROR CONTROL(U) CALIFORNIA UNIV DAVIS DEPT OF ELECTRICAL AND COMPUTER ENGINEE.. R REDINBO 1/1

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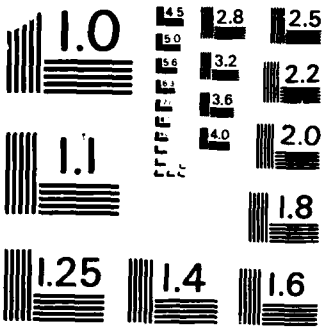

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# FAULT-TOLERANT SIGNAL PROCESSING ARCHITECTURES WITH DISTRIBUTED ERROR CONTROL

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## PROGRESS SUMMARY

New fault-tolerant architectures are investigated to protect modern VLSI implementations against soft errors, internal momentary errors, random in both time and space, characterized by their short and infrequent nature. Work has progressed on both recursive and nonrecursive digital filters. One approach in the recursive case uses many parallel sections, each employing distinct finite field arithmetic and protected by powerful cyclic codes distributed throughout the realization.[1,2] These results are easily extended to the signal processing aspects of other important systems such as protecting and speeding the operations in cyclic error-correcting code decoders.[3,4] In another direction, convolutions between data arrays can be protected with cyclic codes defined over the real rings and fields commonly used in arithmetic units. On the other hand, recursive realizations can be made fault-tolerant by embedding convolutional error-correcting codes, defined over either real or complex fields or finite integer rings, directly with the filter weighting. This is a natural integration since both the filtering operations and those generating the convolutional codes are essentially the same once the time-varying nature of the code structure is properly located. The impact of fault tolerance on system overhead is being analyzed, and the advantages of interacting with existing test subsystems, such as scan designs and built-in self-test, are being evaluated.

The results concerning convolutional codes in recursive realizations for digital filters seems most promising. In general, convolutional codes involve time-varying filtering which may be cascaded with the desired IIR filter weighting. However, systematic convolutional codes produce the filter outputs directly and permit checking parity values to be computed in separate adjacent parallel sections. High-rate codes offer multiple-error detection capabilities with relatively few additional computed samples. A rate k/n code provides (n-k) filtered parity samples , per k filter samples, for checking the hardware operations. Furthermore, the filter states are encoded indirectly and more efficiently since the additional complexity overhead is much less than other methods which employ block code structures, necessitating parity-checking at each filter sample cycle.

The filtered parity samples are generated by (n-k) individual filters each including a decimator operating at rate k. The respective parity channels are defined by the cascade of the desired filter response with the time-invariant weighting from the convolutional code. However, the code's transfer function corresponds to an FIR structure whose tap weights are only 0 or 1. Therefore it is possible to interchange the zero portion of the original filter's transfer function with the one from the convolutional code, permitting the former to be implemented at a rate decimated by k. This interchange of transfer zero portions shifts many nontrivial arithmetic operations to the slower rate realization, significantly reducing the overall number of operations needed in the parity channels.

## Publications

1. "Fault-Tolerant Digital Filtering Structures For Wafer Scale VLSI" , *Proceedings of IEEE International Conference on Acoustics, Speech, and Signal Processing*, 1986.

2. " Signal Processing Architectures Containing Distributed Fault Tolerance", *IEEE Asilomar Conference on Signals, Systems and Computers*, 1986.

3. "Fault-Tolerant Decoders For Cyclic Error-Correcting Codes", *IEEE Transactions on Computers*, vol. C-36, 1987.

4. "Faster Decoding Methods For Cyclic Codes," *IEEE Phoenix Conference on Computers and Communications*, 1987.

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