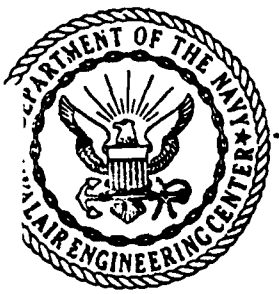

LAKEHURST, N.J.
08733

NAVAL AIR ENGINEERING CENTER

REPORT NAEC-ENG-91-7999

CAPACITY SELECTOR VALVE
ELECTRONICS ENCLOSURE ASSEMBLY
CONTROLLER CARD ASSEMBLY
TEST SPECIFICATIONS

REVISED - SEE BACK COVER

Ship and Shore Installations Engineering Department (SSIED)
Naval Air Engineering Center
Lakehurst, New Jersey 08733

28 December 1982

Prepared for

Commanding Officer
Naval Air Engineering Center
Lakehurst, New Jersey 08733

NAEC-ENG-91-7999

CAPACITY SELECTOR VALVE ELECTRONICS ENCLOSURE ASSEMBLY CONTROLLER CARD ASSEMBLY TEST SPECIFICATIONS

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Approved by: for J. L. MOSS
Engineering Officer

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20 ABSTRACT *(Continue on reverse side if necessary and identify by block number)*

This document is a test procedures for the printed circuit board in the electronic enclosure assembly of the capacity selector valve system. The tests are intended to be only functional screening tests for the assembled boards.

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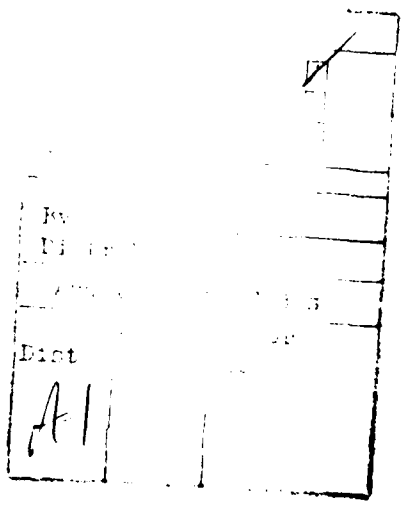
I. PREFACE

This is a test procedure for the printed circuit board in the electronic enclosure assembly. The tests are intended to be only functional screening tests for the assembled boards. The tests do not provide accelerated life tests for individual components.

If any section of the board fails, the board testing should stop and that section of the board should be repaired. Upon completion of repairs, the board should be retested.



II. TABLE OF CONTENTS

III. LIST OF FIGURES AND TABLES

III. LIST OF FIGURES AND TABLES (CONT.)

IV. INTRODUCTION AND DESCRIPTION

A. INTRODUCTION

1. The purpose of this report is to provide test specifications and procedures to insure proper operation of the electronic circuit card assembly used in the electronic enclosure assembly.

2. The information contained herein details the requirements for the tests and the procedures to be followed for the various sections of the card.

3. Equipment necessary to perform these tests and apparatus needed to generate the specified power requirements shall be the responsibility of the manufacturer. This does not preclude the procuring agency from providing any equipment or apparatus that may prove advantageous in expediting the testing of the circuit cards.

4. The test specification for each circuit card section consists of five parts with the final part being the actual test procedure. For ease of testing each procedure follows exactly the same format. An outline of a typical test procedure is included below.

a. Card Section Title

(1) Circuit Description

(2) Test Requirements

(3) Test Equipment and Power Requirements

(4) Preliminary Test Procedure (Test Setup)

(5) Final Test Procedure

B. GENERAL TEST REQUIREMENTS

1. This section provides general information in the following test area:

a. Percent of units to be tested.

b. Instructions for filling out Test Data Sheets.

c. Standard test conditions.

d. Quality Assurance Provisions.

e. Lists of test instruments and miscellaneous equipment.

f. Necessary information to assemble circuit card test fixture.

2. Testing shall be performed on 100% of the units supplied.

3. Test data resulting from each card test shall be recorded and retained in the testing department file. Test data sheets shall include the unit serial number of each corresponding assembly, shall reference the Test Procedure performed, the Test Specification used and include appropriate approval or disapproval signature. The technician performing the test shall sign and date each data sheet.

4. TEST CONDITIONS, STANDARD

a. Standard test conditions are defined as follows:

(1)	Temperature	Room Ambient 65°F to 75°F
(2)	Pressure	28 to 32 inches of Mercury
(3)	Relative Humidity	not greater than 95%

5. QUALITY ASSURANCE PROVISIONS

a. Assemblies, including all their parts, shall be constructed and finished in manner to assure compliance with all the requirements of this specification. Attention shall be paid to neatness and thoroughness of soldering, marking of parts and assemblies, hardware assemblage and overall final coating.

b. The provisions of this specification are applicable in all respects and departures from this specification shall be cause for rejection.

C. TEST EQUIPMENT

1. Table 1 lists test equipment required to test the circuit card assembly. This equipment is intended as a guide. Many equivalent pieces of test gear are available. It will be up to the testing agency to select alternate equipment where desired.

2. Figures 1 thru 18 and Table 2 describe equipment that can be manufactured to simplify testing.

D. TEST PROCEDURES

1. Prior to the functional tests described herein, each printed circuit board should be given a visual inspection to ensure that the assembly has been made in accordance with the specifications of the Board Assembly drawing (621244-1).

2. All circuit board test results shall be recorded on the associated test data sheets.

TABLE I. LIST OF TEST EQUIPMENT

1.	DC POWER SUPPLY;	Input power:	115VAC 60Hz
		Output:	15VDC ± 5% at 500 mA
		Regulation:	.05% line .05% load
2.	DC POWER SUPPLY;	Input power:	115 VAC 60Hz
		Output:	5VDC ± 5% at 5 Amp
		Regulation:	.05% line .05% load
3.	DIGITAL MULTIMETER;	Fluke 8000A/8010 or equivalent	

E. MISCELLANEOUS TEST EQUIPMENT

Included in the following list of equipment is a card test fixture which is to be assembled to Figures 1 through 18.

Table 2 is a list of materials needed to assemble the test fixture.

1. Circuit Card Test Fixture
2. POS-CMD Patch Cable

TABLE II. MATERIAL LIST FOR CIRCUIT CARD TEST FIXTURE

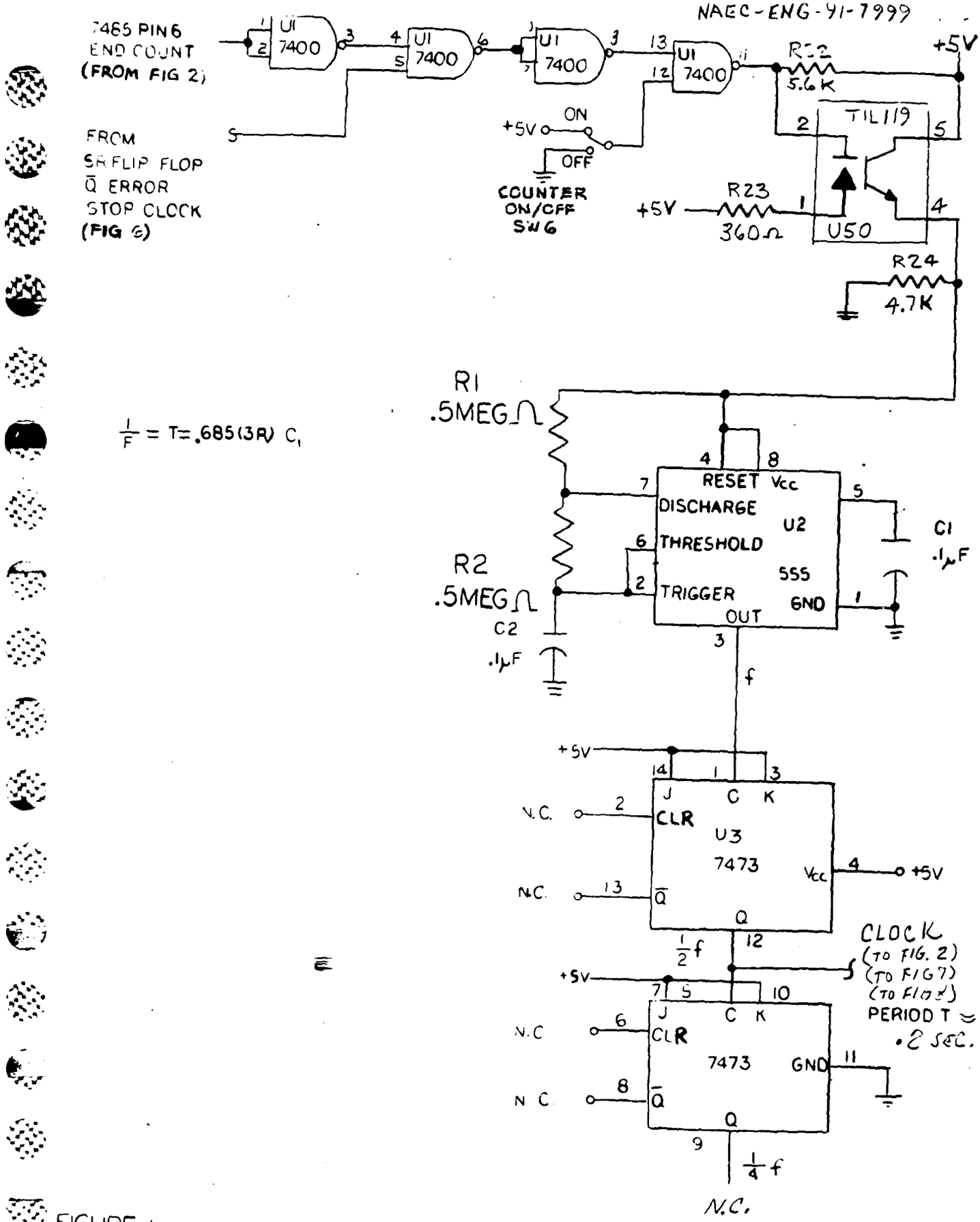
Item	Description	Qty
U1, U4	(7400) Quad 2 input NAND Gate	2
U5, U43	(7402) QUAD 2 input NOR Gate	2
U45	(7425) Dual 4 input NOR Gate	1
U42, U47	(7432) Quad 2 input OR Gate	2
U3	(7473) JK Flip Flop	1
U8, U9, U10 U39, U40, U41	(7485) 4 bit Magnitude Comparitor	6
U26, U27, U28 U44	(7486) Quad EX-OR Gate	4
U11, U12, U16 through U19, U48, U64	(74157) Quad Multiplexer	8
U20 thru U25	(74184) BCD to Binary Converter	6
U6, U7, U13, U14, U15, U63	(74192) Decade Up/Down Counter	6
U2	(555) Timer	1
U32, U35	(4071) Quad 2 input OR Gate	2
U33, U34	(4072) Dual 4 input OR Gate	2
U29, U30, U31, U36, U37, U38, U49	(40109B) Level Shifter	7
U50	(TIL119) OPTO-Coupler	1
U54(2), U55(2)	9x4.7K OHM Resistor Network (1 end common)	4
U56(2), U60, U61, U62	9x10K OHM Resistor Network (1 end common)	5
U58, U59	9x680 OHM Resistor Network (1 end common)	2
DS10, DS11, DS12	(HP7300) Numeric Indicator (Hewlett Packard)	3
DS1 thru DS6 DS8, DS9	(HP P/N 5082-4403) Light Emitting Diode	8

TABLE II. MATERIAL LIST FOR CIRCUIT CARD TEST FIXTURE (CONT.)

Item	Description	Qty
R1, R2	.5 MEGOHM 1/8 Watt ± 5% Resistor	2
R4, R5, R12, R13	2.2K OHM 1/8 Watt ± 5% Resistor	4
R6, R7, R11, R25	330 OHM 1/8 Watt ± 5% Resistor	4
R20, R21, R24	4.7K OHM 1/8 Watt ± 5% Resistor	3
R22	5.6K OHM 1/8 Watt ± 5% Resistor	1
R23	360 OHM 1/8 Watt ± 5% Resistor	1
R26 thru R31	2.7K OHM 1/8 Watt ± 5% Resistor	6
R32, R33	1.3K OHM 1/8 Watt ± 5% Resistor	2
R17	1K OHM 2W Potentiometer with Plastic knob on shaft	1
C1, C5, and 22 For Power Supply Filtering	.1 mf 50V±20% Capacitor (CK05BX104K)	24
Power Supply Filtering	47 mf 35V Capacitor	2
SW2, 6, 8 thru 17	SPDT Toggle Switch	12
SW3	DPDT Toggle Switch	1
SW7	4PDT Toggle Switch	1
SW1, 4, 5	SPST Momentary Pushbutton with Red Cap	3
SW18 thru 26	BCD Switches	9

TABLE II. MATERIAL LIST FOR CIRCUIT CARD TEST FIXTURE (CONT.)

Item	Description	Qty
TP1, TP3	Test Point Red Pomona P/N 3542-2	2
TP2, TP4	Test Point Black Pomona P/N 3542-0	2
	Enclosure Aluminum	1
P.C.B.	Wire Wrap Board (Electronic Solutions, Inc. - 8000D0364W)	1
P1, P2	P. C. Connector (Viking Industries - 3VH25/1JN5)	2
J1, J2	P. C. Connector (M21097/4-34) (Elco)	2
J3	P. C. Connector (Viking Industries - 3VH30/1JN5)	1
J4	P. C. Connector (Amphenol - 225-24 321-101)	1



$\frac{1}{F} = T = .685(3R)\,C_1$

FIGURE 1

TEST SET ON OFF SWITCH AND CLOCK

(REV C)

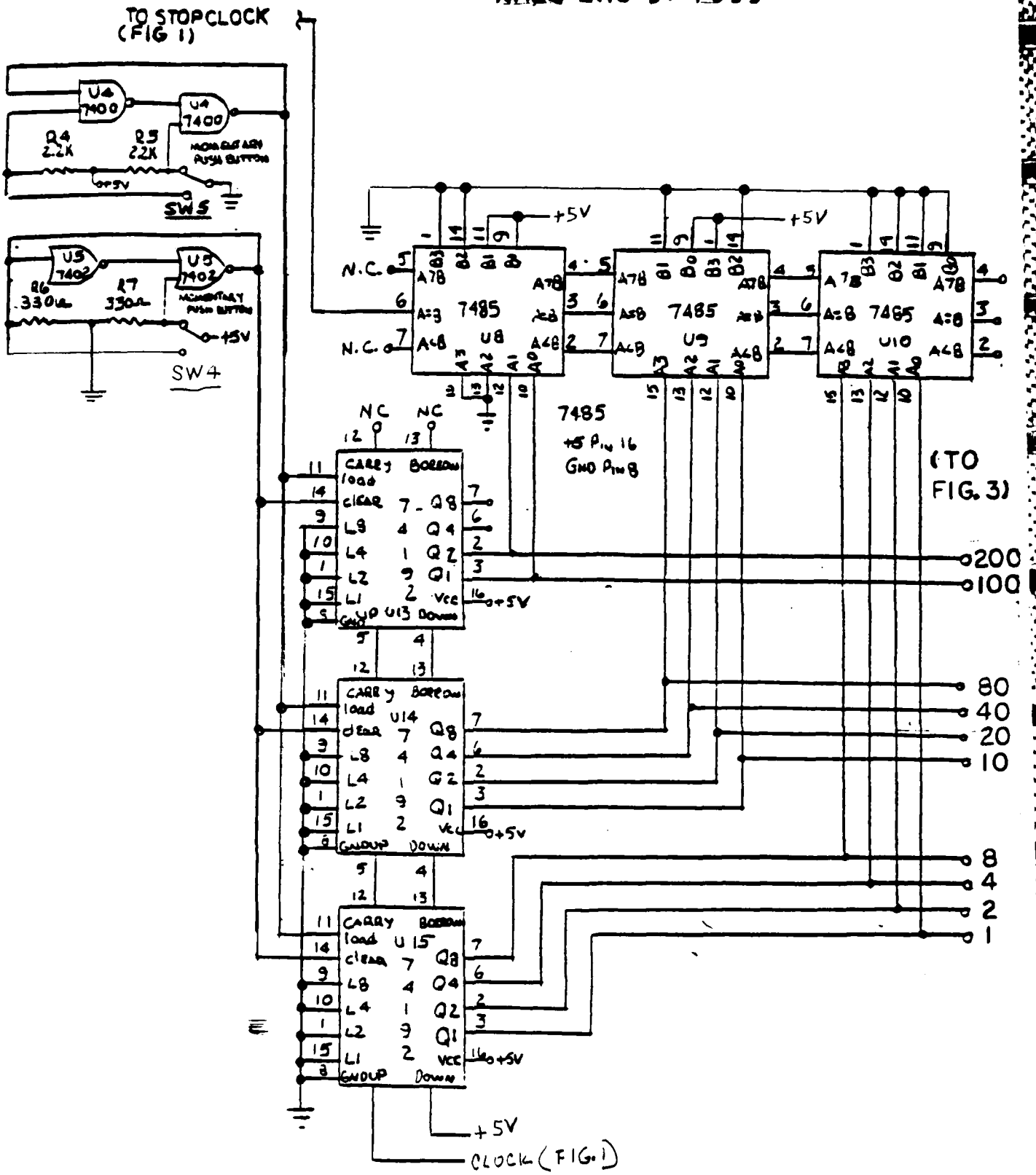
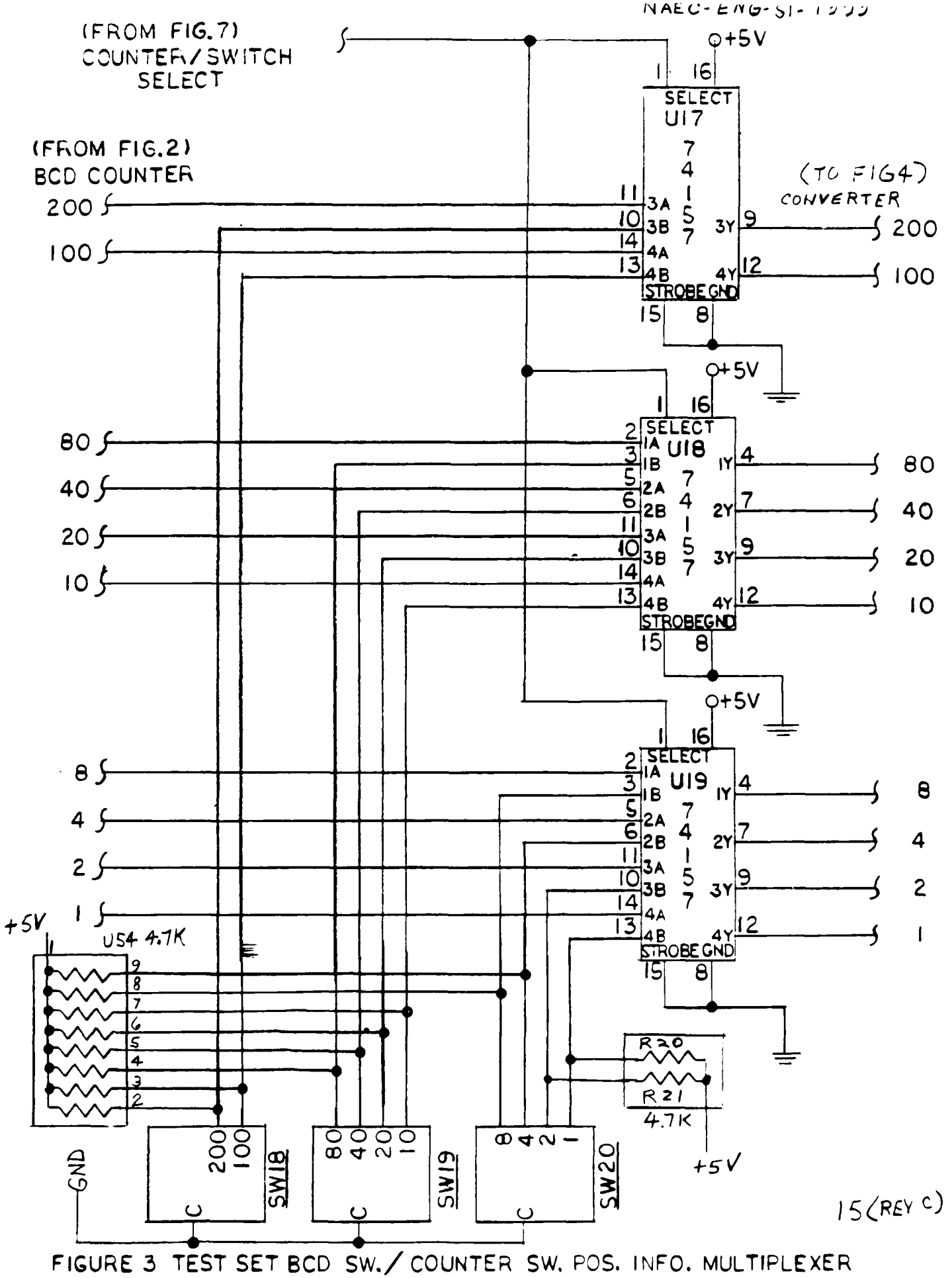


FIGURE 2 TEST SET
BCD COUNTER 0 TO 360

(REV C)



15 (REV C)

FIGURE 3 TEST SET BCD SW./ COUNTER SW. POS. INFO. MULTIPLEXER

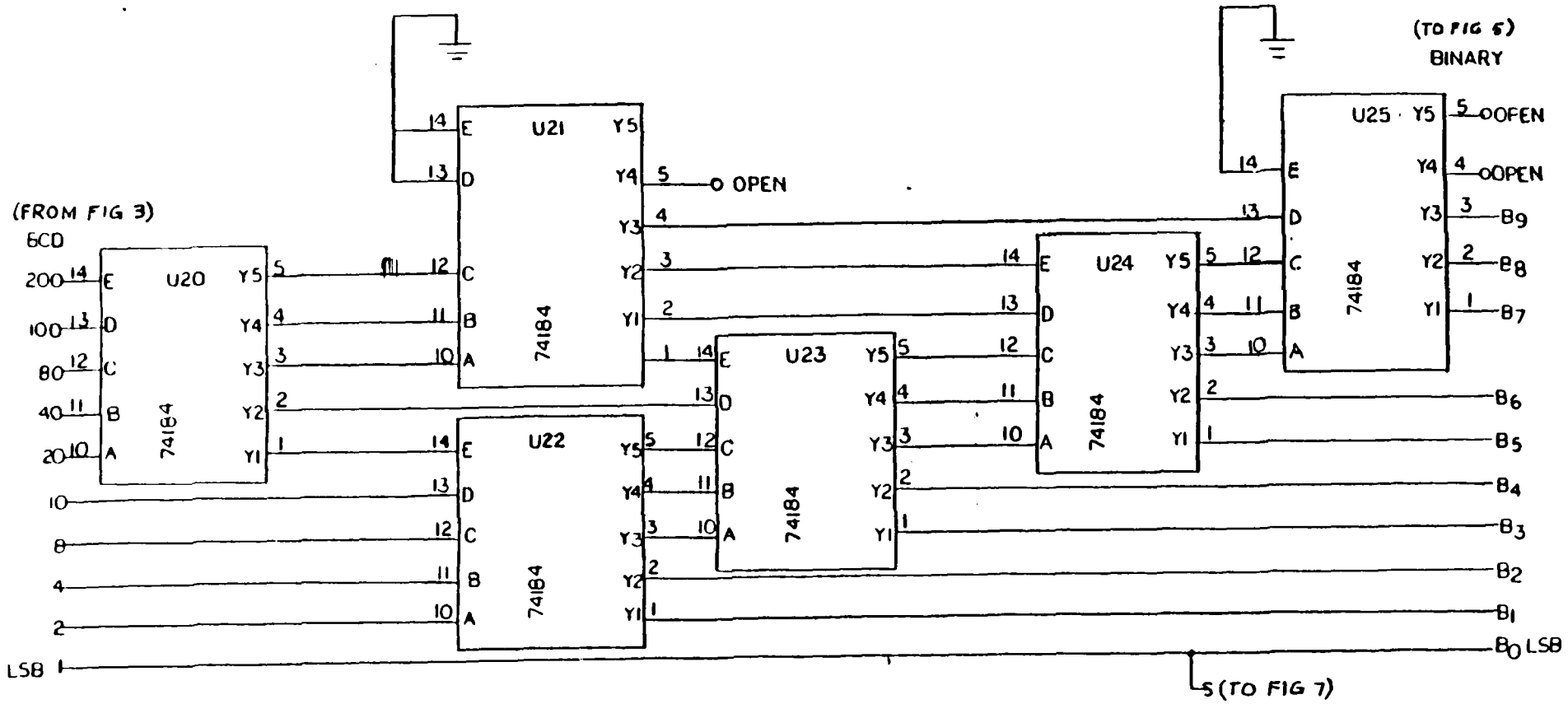


FIGURE 4 TEST SET
BCD TO BINARY CONVERTER

ALL CHIPS 74184

POWER: VCC - PIN 16 +5V
GND - PIN 8 GND ov
Y6 - PIN 6
Y7 - PIN 7
Y8 - PIN 9
ENABLE G - PIN 15 GND ov

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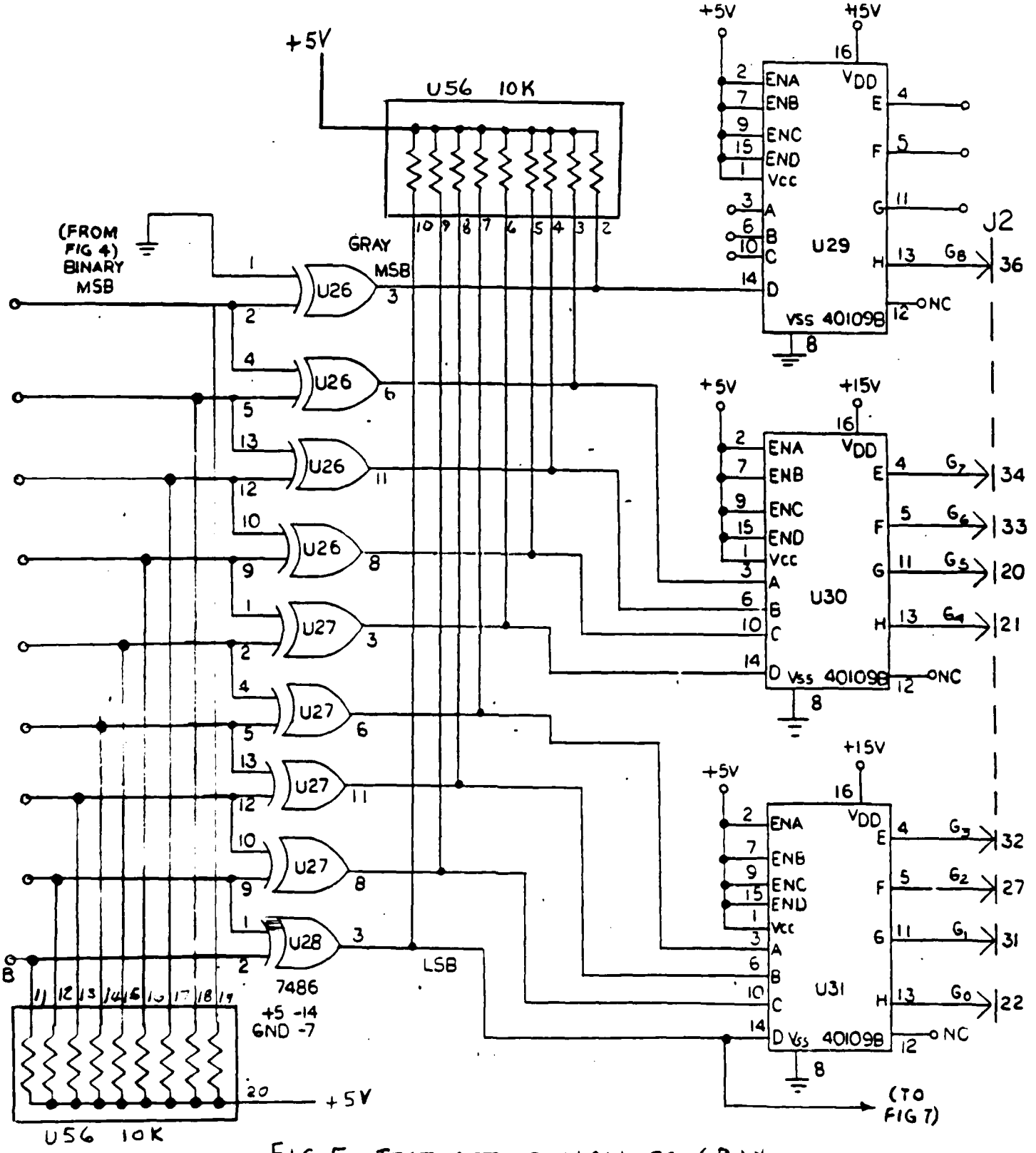

FIG 5 TEST SET BINARY TO GRAY CONVERTER WITH 5V TO 15V LEVEL SHIFTER

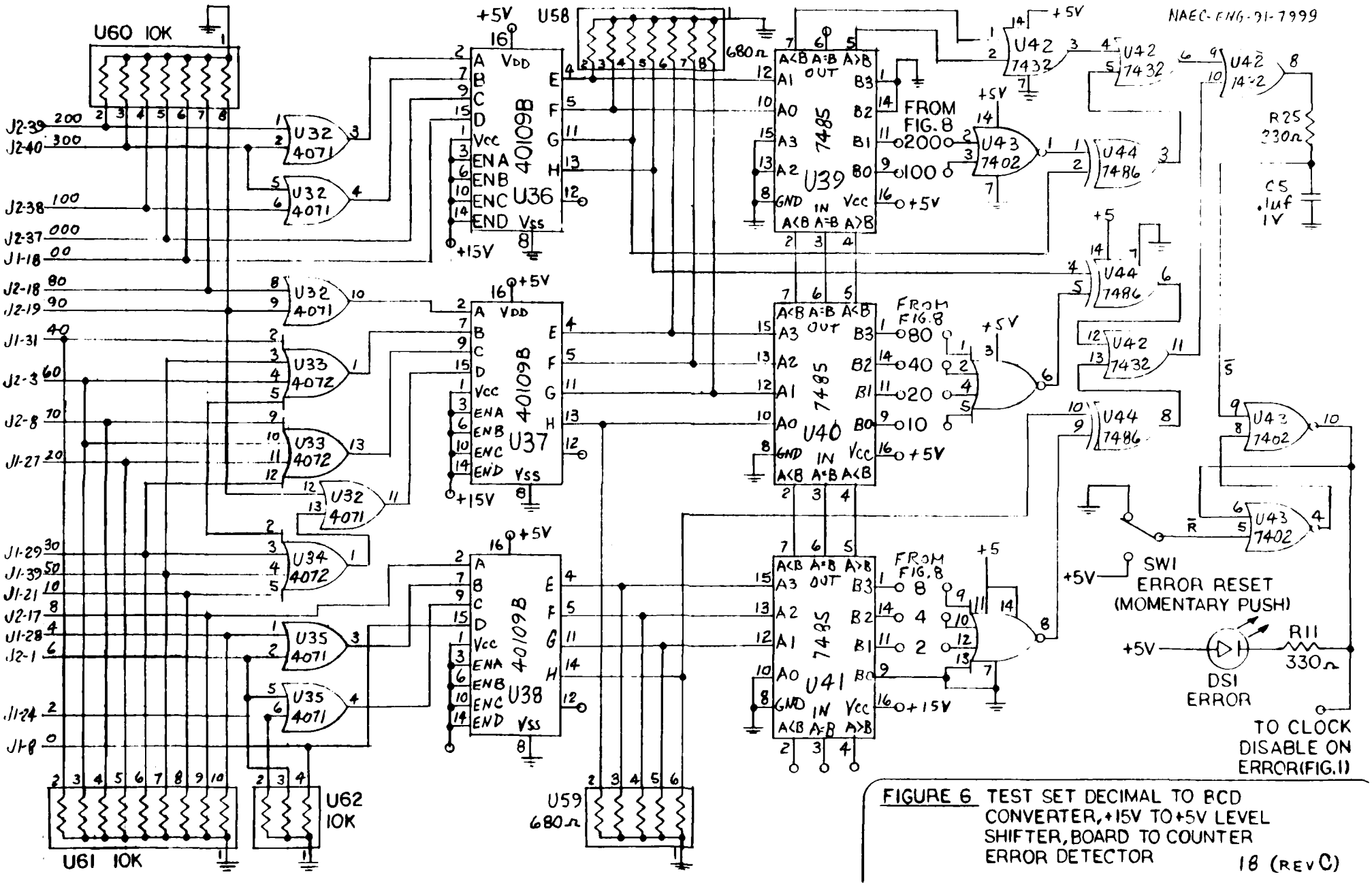

FIGURE 6 TEST SET DECIMAL TO BCD CONVERTER, +15V TO +5V LEVEL SHIFTER, BOARD TO COUNTER ERROR DETECTOR

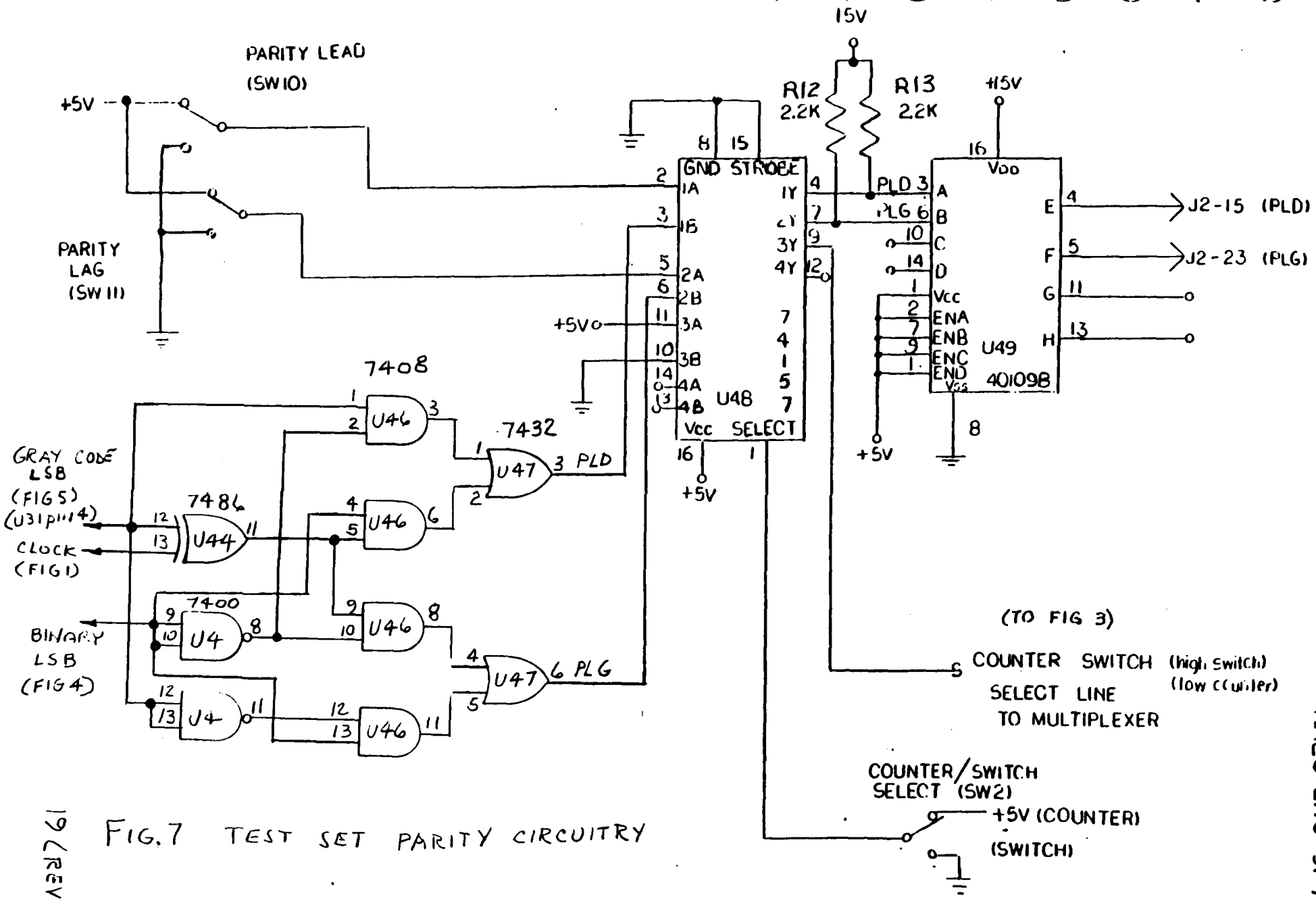

FIG. 7 TEST SET PARITY CIRCUITRY

(REV C) 19

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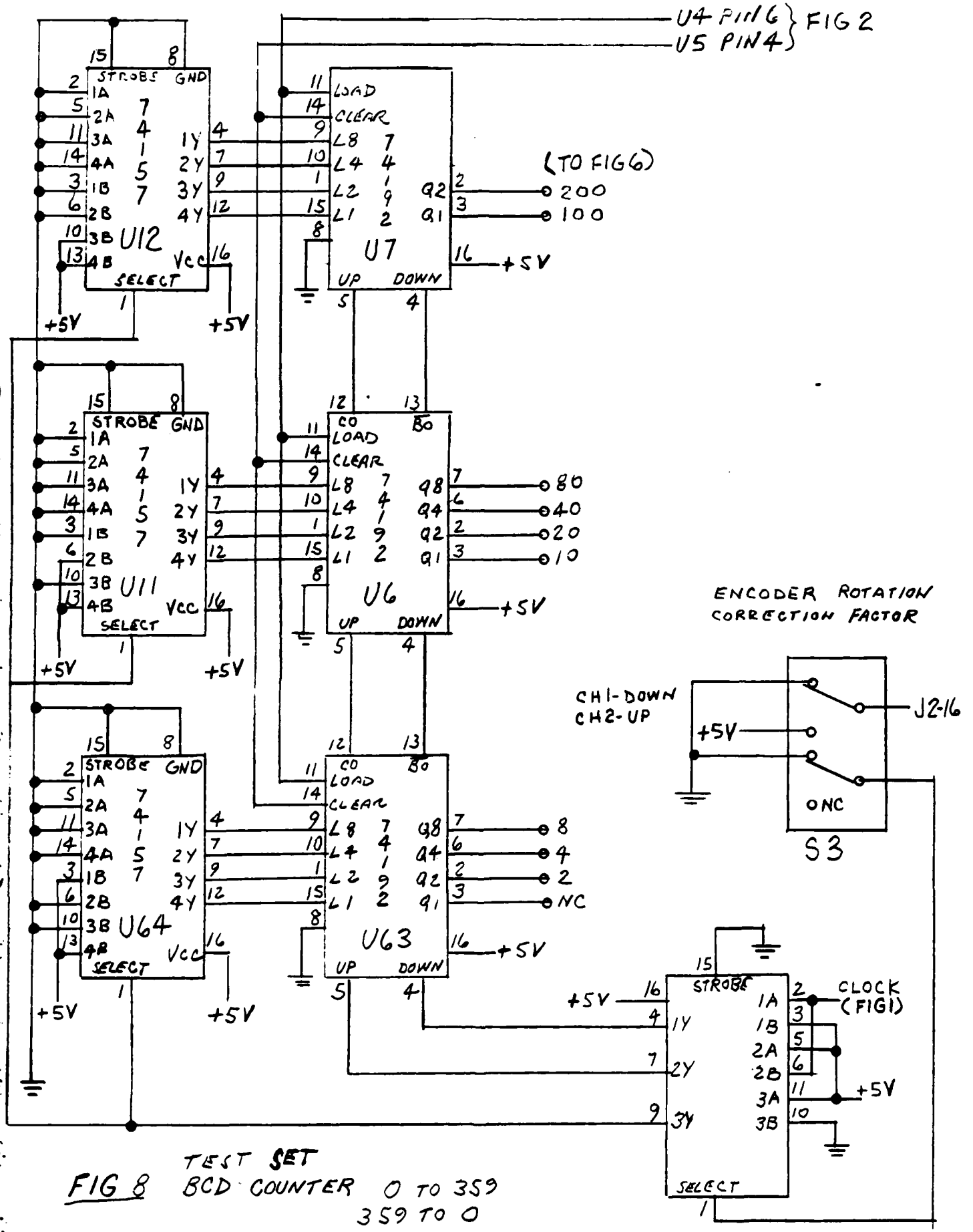


TEST SET

FIG 8 BCD COUNTER 0 TO 359
359 TO 0

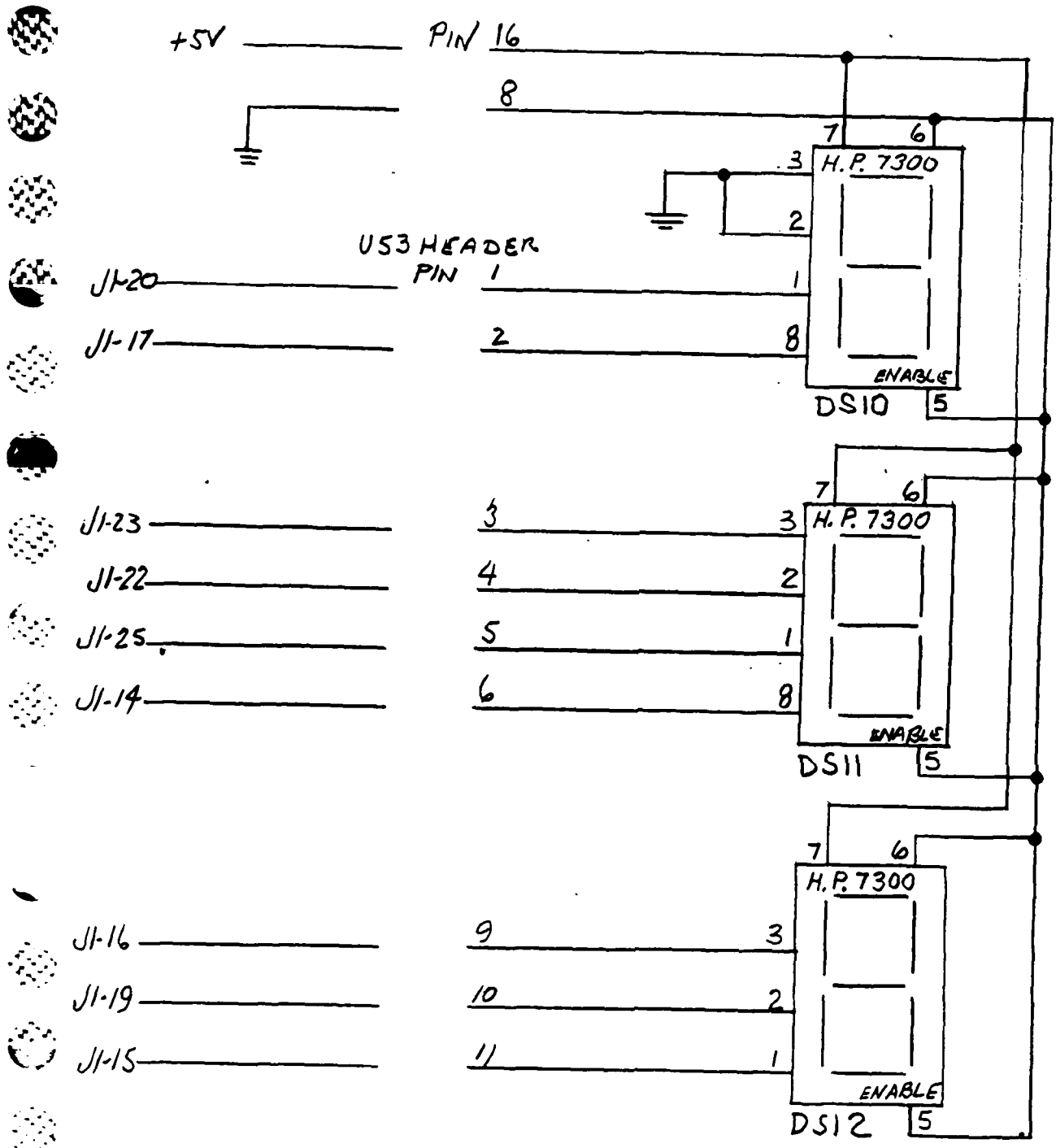


FIG. 8A TEST SET
POS-CMD ERROR READOUT CIRCUITS

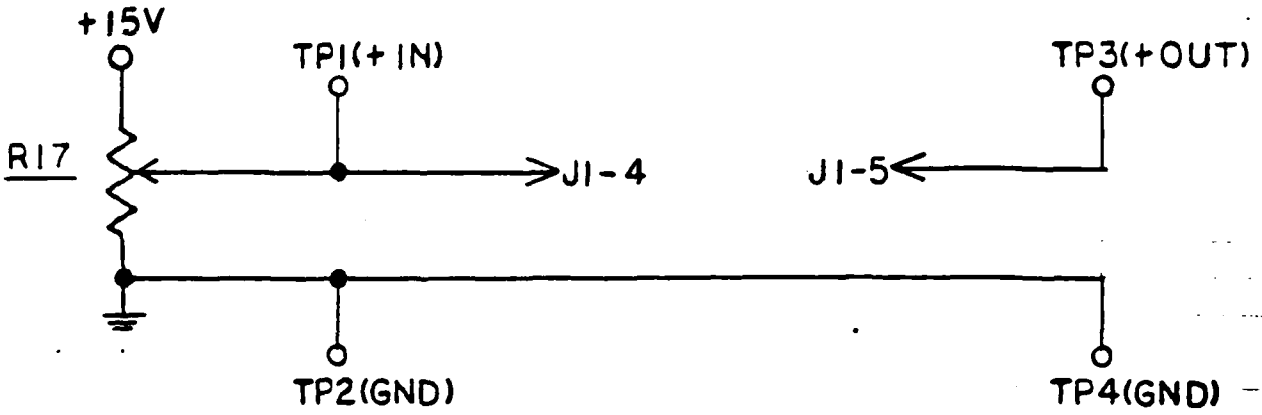


FIGURE 9 TEST SET INTENSITY CIRCUIT

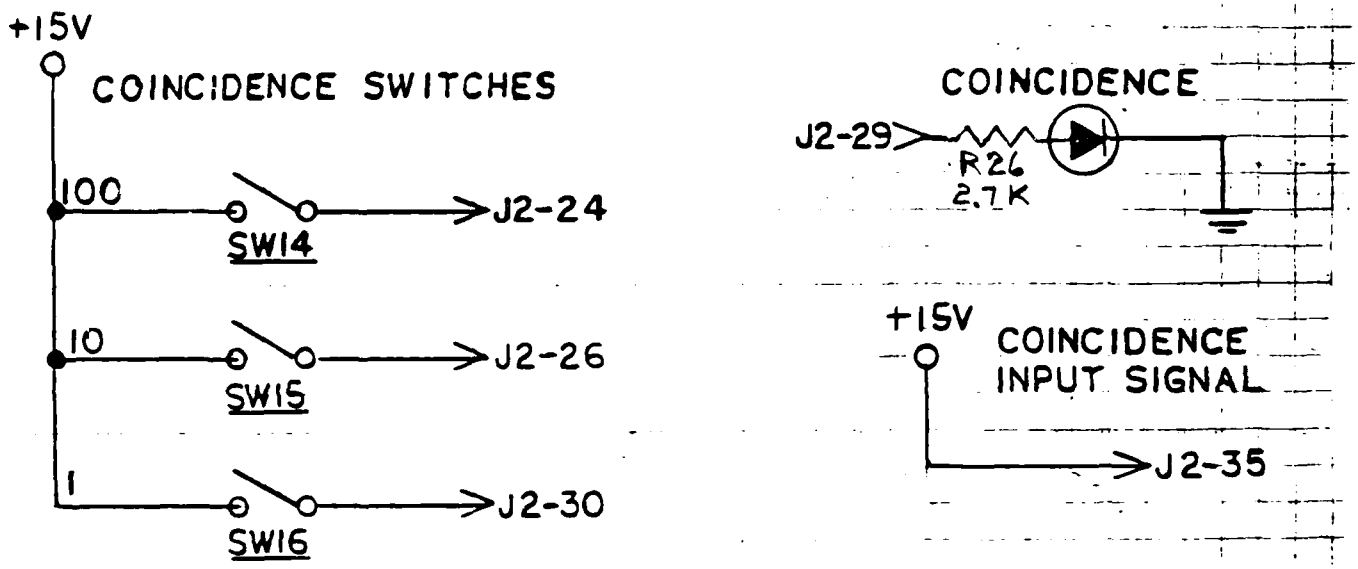


FIGURE 10 TEST SET COINCIDENCE CIRCUIT

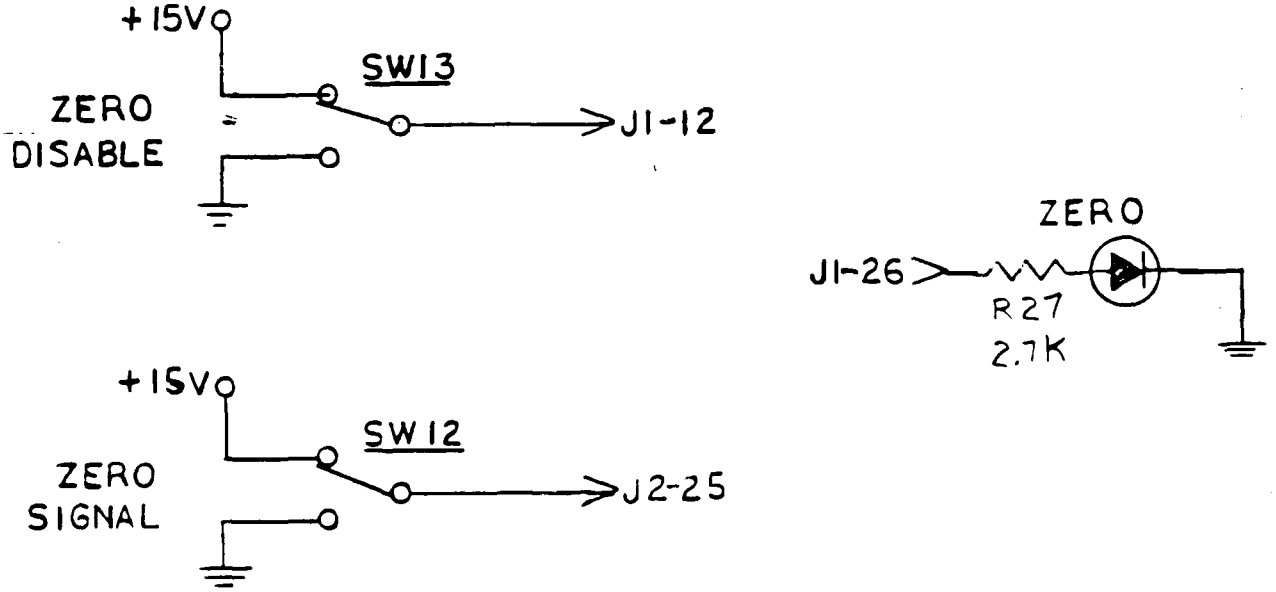


FIGURE 11 TEST SET ZEROING CIRCUIT

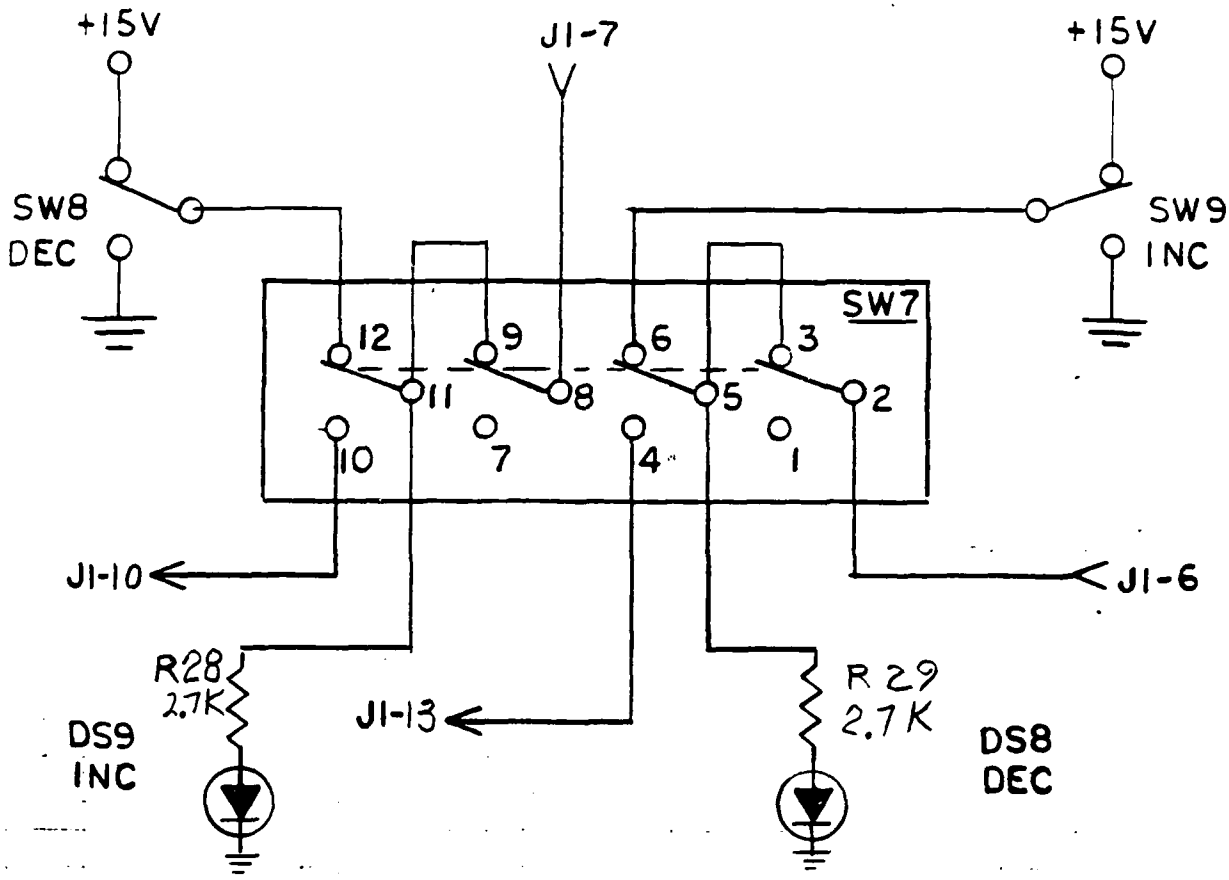
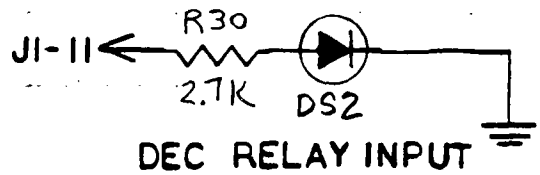
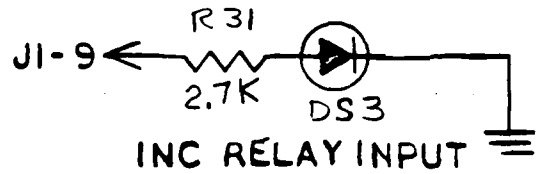


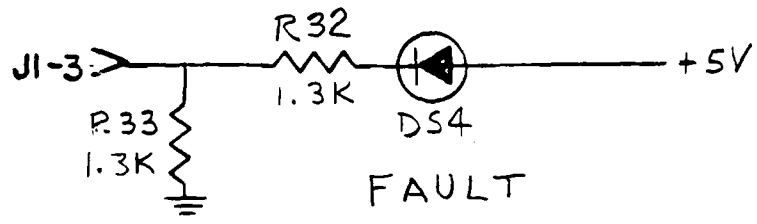
FIG. 12A
DECREASE / INCREASE INPUT/OUTPUT SELECT SWITCH



DEC RELAY INPUT



INC RELAY INPUT



FAULT

FIGURE 12. TEST SET DECREASE / INCREASE CIRCUIT

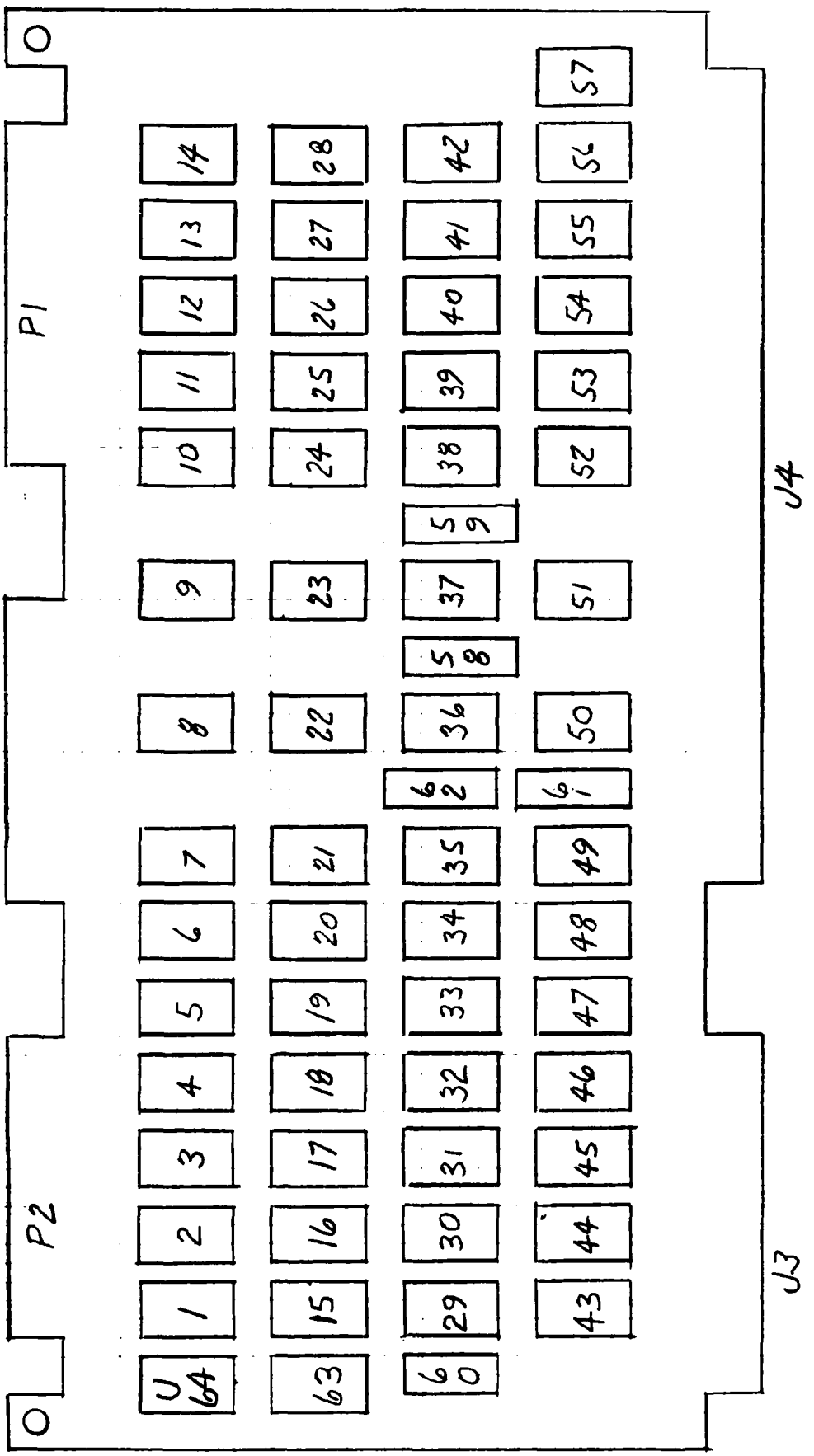


FIG 13
PCB LAYOUT

23 A (REV C)

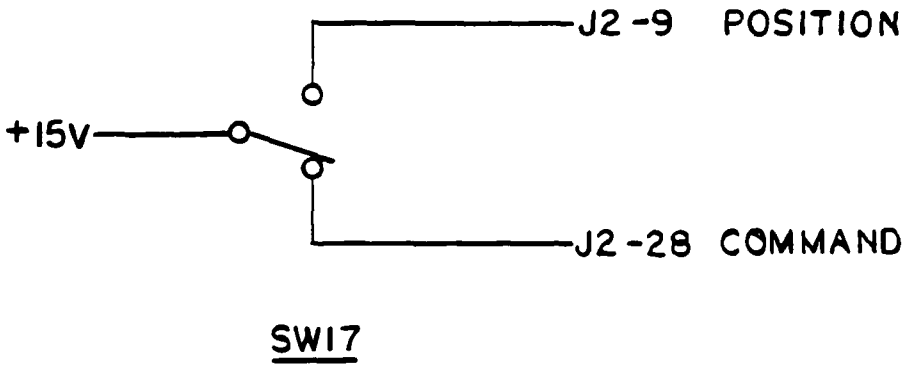


FIGURE 14 TEST SET POS/CMD SELECT SWITCH

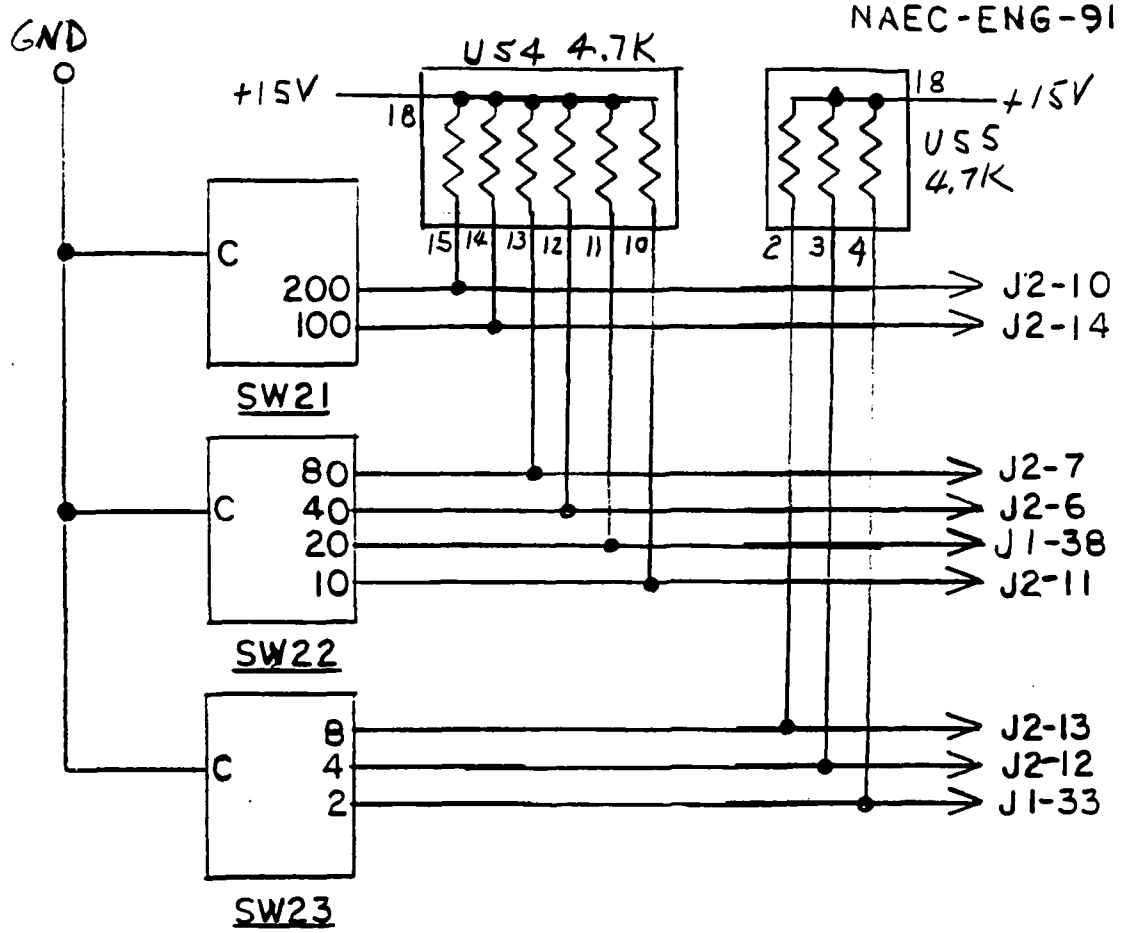


FIGURE 16 TEST SET COMMAND SWITCH INPUTS

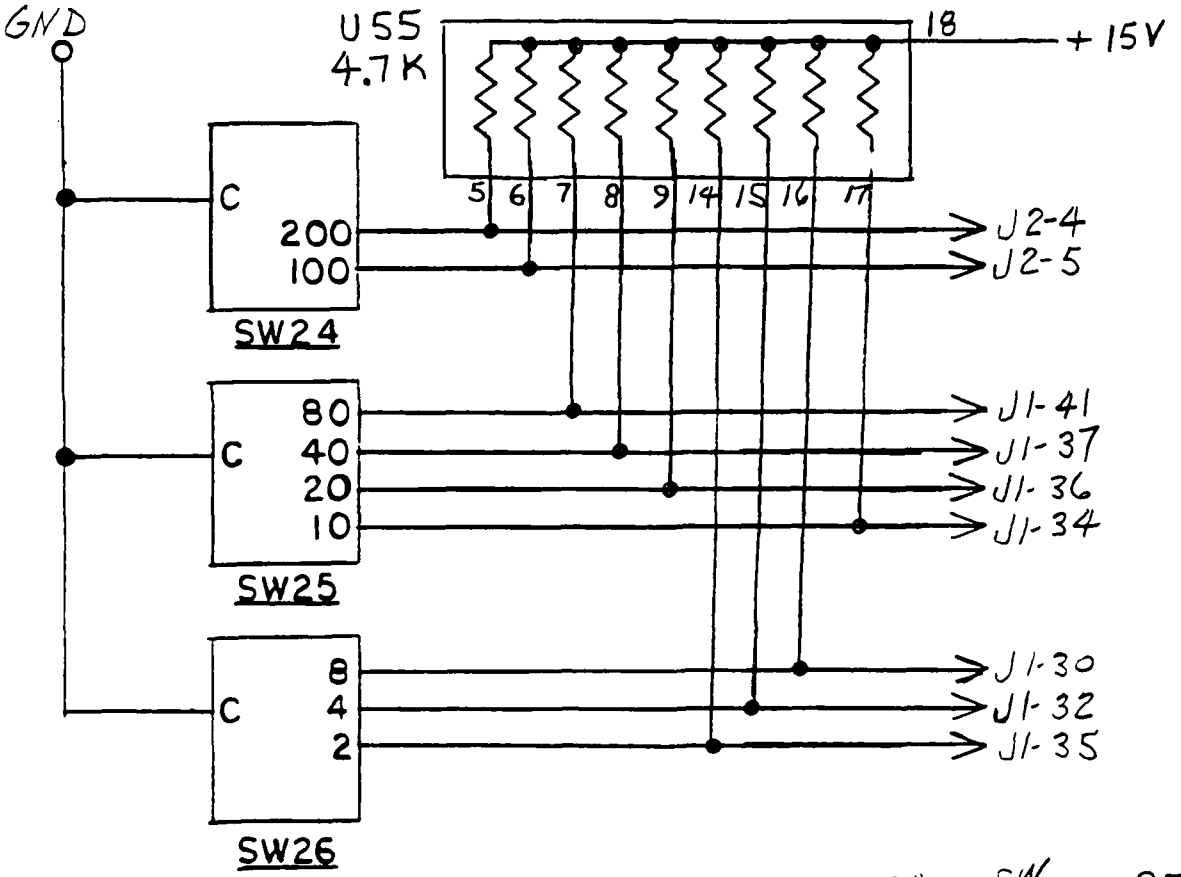


FIG. 17 TEST SET REDUNDAINT BOARD POS CMD ERROR SW. 25 (REV C)

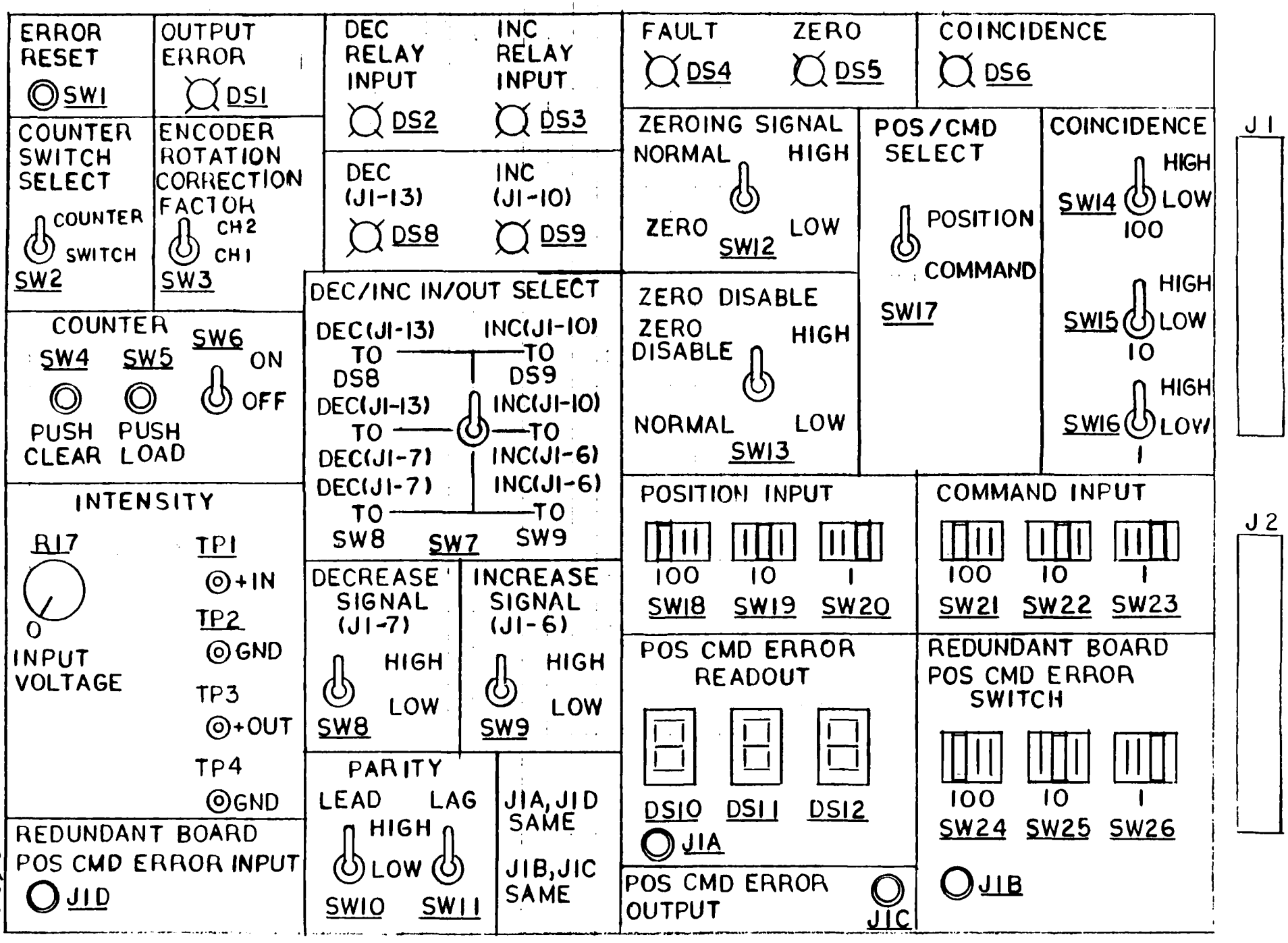


FIGURE 18 TEST SET SWITCHES & INDICATORS (PROPOSED)

V. DETAILED CIRCUIT CARD TEST PROCEDURES

A. Encoder Inputs to Readouts and Readout Zeroing

B. BCD Subtractor Circuit

C. Direction Logic Circuit

D. Increase/Decrease Circuit

E. Crosscheck Subtractor Circuit

F. Sign Error Circuit

G. Parity Error Circuit

H. Zeroing Circuit

I. Coincidence Circuit

J. Intensity Lighting Control Circuit

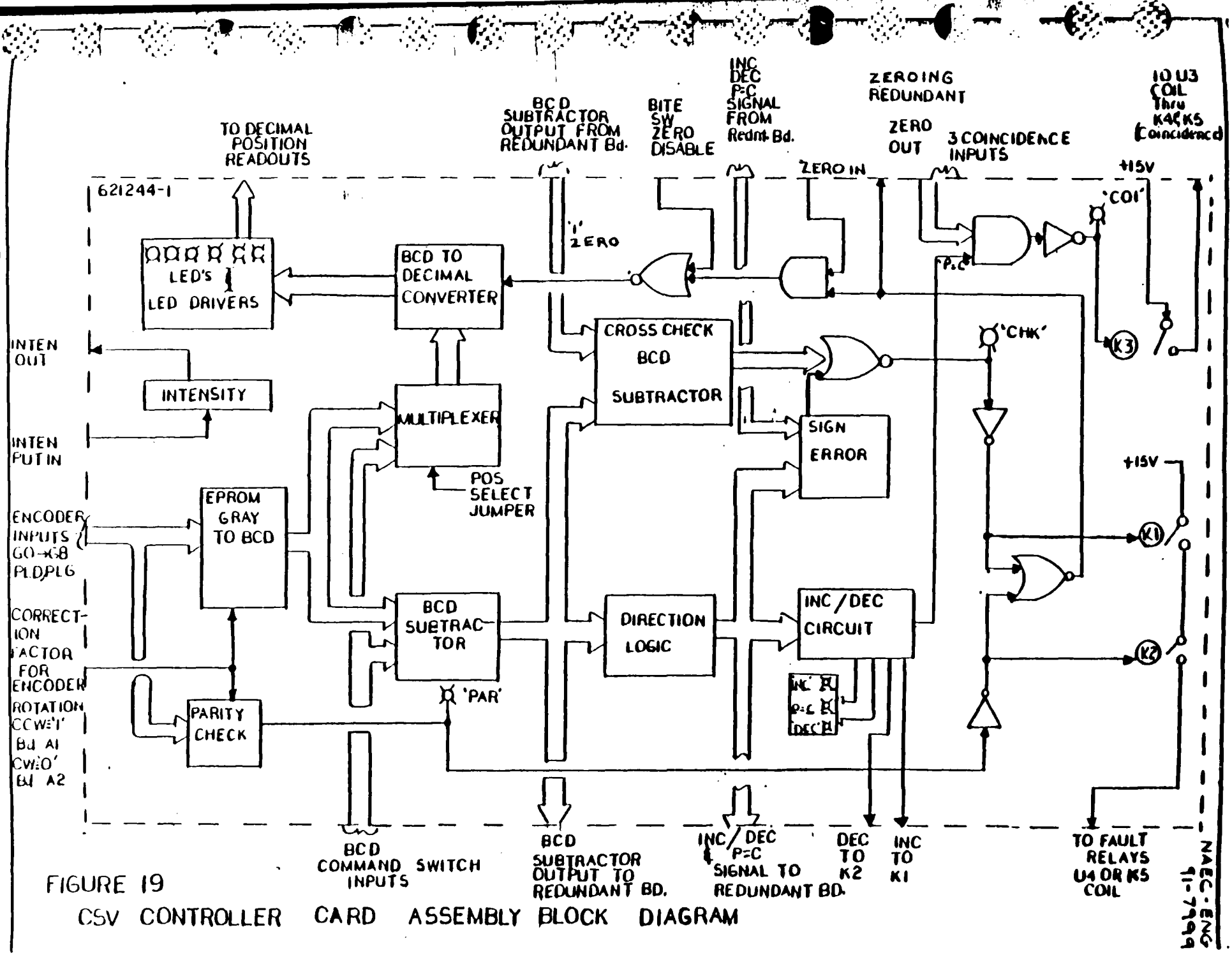


FIGURE 19

CSV CONTROLLER CARD ASSEMBLY BLOCK DIAGRAM

A. ENCODER INPUTS TO READOUTS AND READOUT ZEROING

1. CIRCUIT DESCRIPTION

a. This section of the card inputs the gray code information thru the gray to BCD converters, into the multiplexer, thru to the BCD to decimal converters and out to the LED drivers and the readouts.

b. In the system each encoder provides a gray code output which is switched thru a six position six deck switch.

The output of the BITE switch is received by a gray to BCD converter consisting of two erasable programmed read only memories (EPROM's) located on the circuit boards.

The BCD output of the EPROM's is inputed to a multiplexer along with the BCD command switch information. The multiplexer's output is hard wired for a BCD signal output.

The output of the multiplexer is then processed by a BCD to Decimal converter which also includes an output zeroing circuit that is activated when a parity or crosscheck/sign error is detected. The decimal output is then fed to the LED transistor driver's which are connected to the LED indicators on each circuit board. This position signal is also routed to the remote valve position readouts.

c. The schematic for the Encoder position input protection circuit is shown in Figure 20.

The schematic for the EPROM Gray to BCD converter is shown in Figure 21.

The schematic for the multiplexer is shown in Figure 22.

The schematic for the BCD to Decimal converter is shown in Figure 23.

The schematic for the LED driver's, LED's and Remote Readout Outputs is shown in Figure 24.

The encoder and BITE switch inputs are in the form of a 9 bit gray code. The inputed data is transferred thru series resistors (R81 thru R89) and resistors (U40) to limit current surges. Then it is subjected to the protection diodes (CR55 thru CR64 and CR88 and CR95) to drain off excess voltage. The gray code inputs then pass thru inverters (U27 and U28). The signal is then sent to Parity Check Chip (U13) and to inverters (U14 and U15). The signal from inverters (U14 and U15) is then inputed to two Erasable Programmed Read Only Memories (EPROM's) (U1 and U2) for decoding the signal from gray code to BCD.

U1 performs the hundreds decoding

U2 performs the units and tens decoding

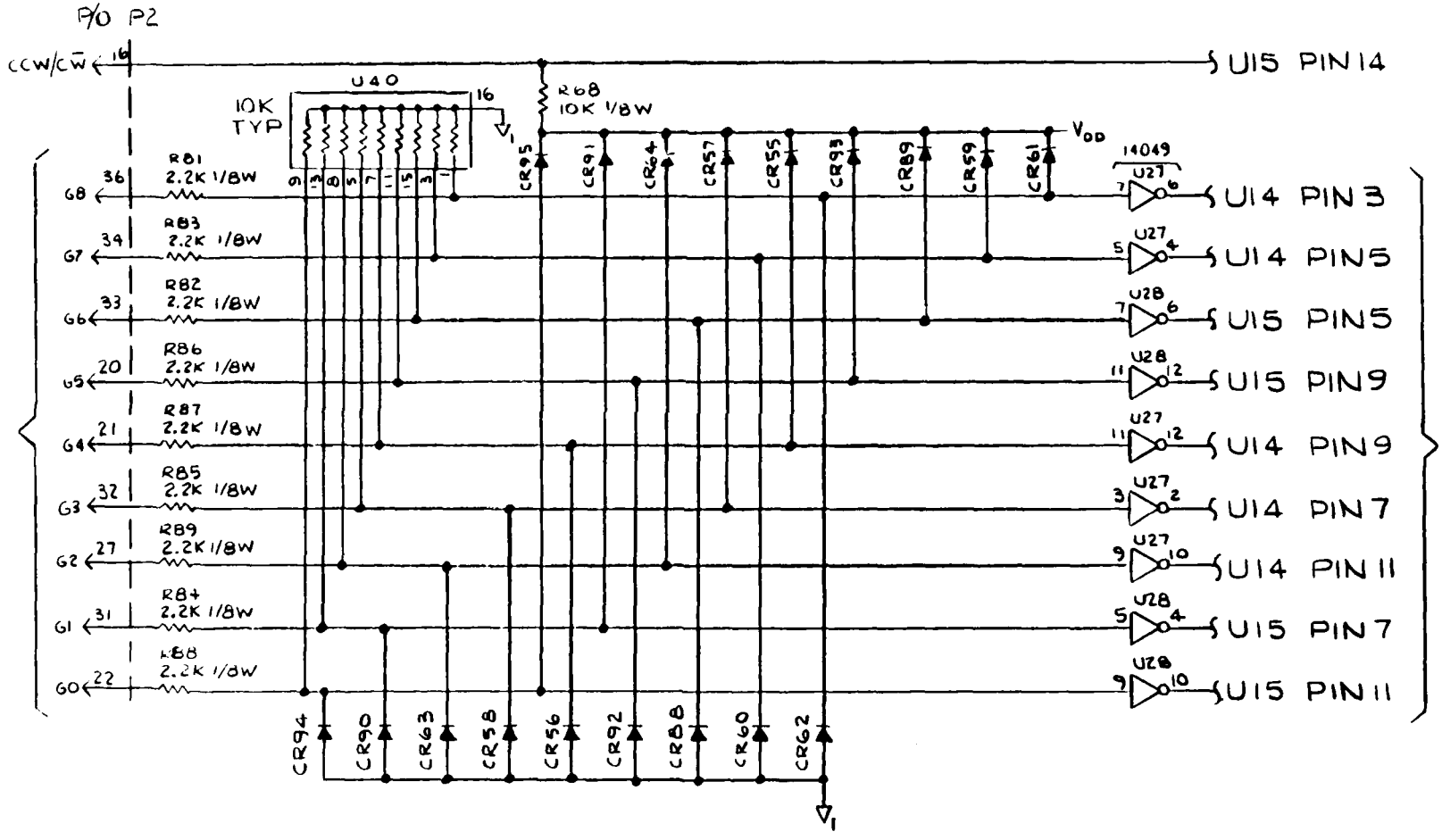
The EPROM's also accept a correction factor routed from (J2 PIN 16) which is necessary to locate the proper decoding address in the EPROM's due to the opposite shaft rotation of the two encoders. The correction factor is high '1' for channel A1 which is inverted when passed thru inverter (U15) and then inputed to (U1 and U2). The correction factor is low '0' for channel A2 which is inverted when passed thru inverter (U15) and then inputed to (U1 and U2). The multiplexer circuit on 621244-1 is hardwired for both position and command output. The command BCD Output is fed into Multiplexers (U5, U7, and U10). The actual BCD position signal is also fed into Multiplexers (U5, U7, and U10). The Multiplexers outputs are controlled by external wiring from the P/C Connector via P2-9 (for position) and P2-28 (for command). The output is then fed into the BCD to Decimal Converter and zeroing circuit. The output of the multiplexer is fed to

a BCD to decimal converter which has a display zero enable when there is a crosscheck/sign error or parity error. The circuitry used in the BCD to decimal converter is BCD to decimal decoder (U4, U8 and U11) and strobed Hex inverter/buffer with output disable (U6, U9, and U12). The output of the multiplexer is fed into BCD to decimal decoders (U4, U8 and U11). The decimal output is then fed into Inverter/Buffer IC's (U6, U9, and U12) with output disable pins. When there is a parity error or crosscheck/ sign error a high '1' signal is inputed to (U6, U9, and U12 Pin 4) OD (output disable). This causes the Inverter/Buffers chips to output a low '0'.

When the outputs are disabled transistor (Q22) is saturated energizing the '0' lines for the units, tens, and hundreds by putting a low '0' to the base of the driver transistor.

The signal from the BCD to decimal converter circuit is fed into the LED display drivers into the position LED's and also out to the position/ command readouts.

If there are no errors the output of inverter buffers chips (U6, U9, and U12) is fed into display driver transistor (Q1 thru Q19). A zero to the driver transistor will turn on the LED and also feed a high '1' signal thru the lines to the position/ command readouts. The position/command readouts are fed thru (P1 PINS 8, 18, 21, 24, 27, 28, 29, 31, and 39 and P2 PINS 1, 3, 8, 17, 18, 19, 37, 38, 39 and 40).



ENCODER POSITION INPUT PROTECTION CIRCUIT

FIGURE 20.

NAEC-ENG-91-7999

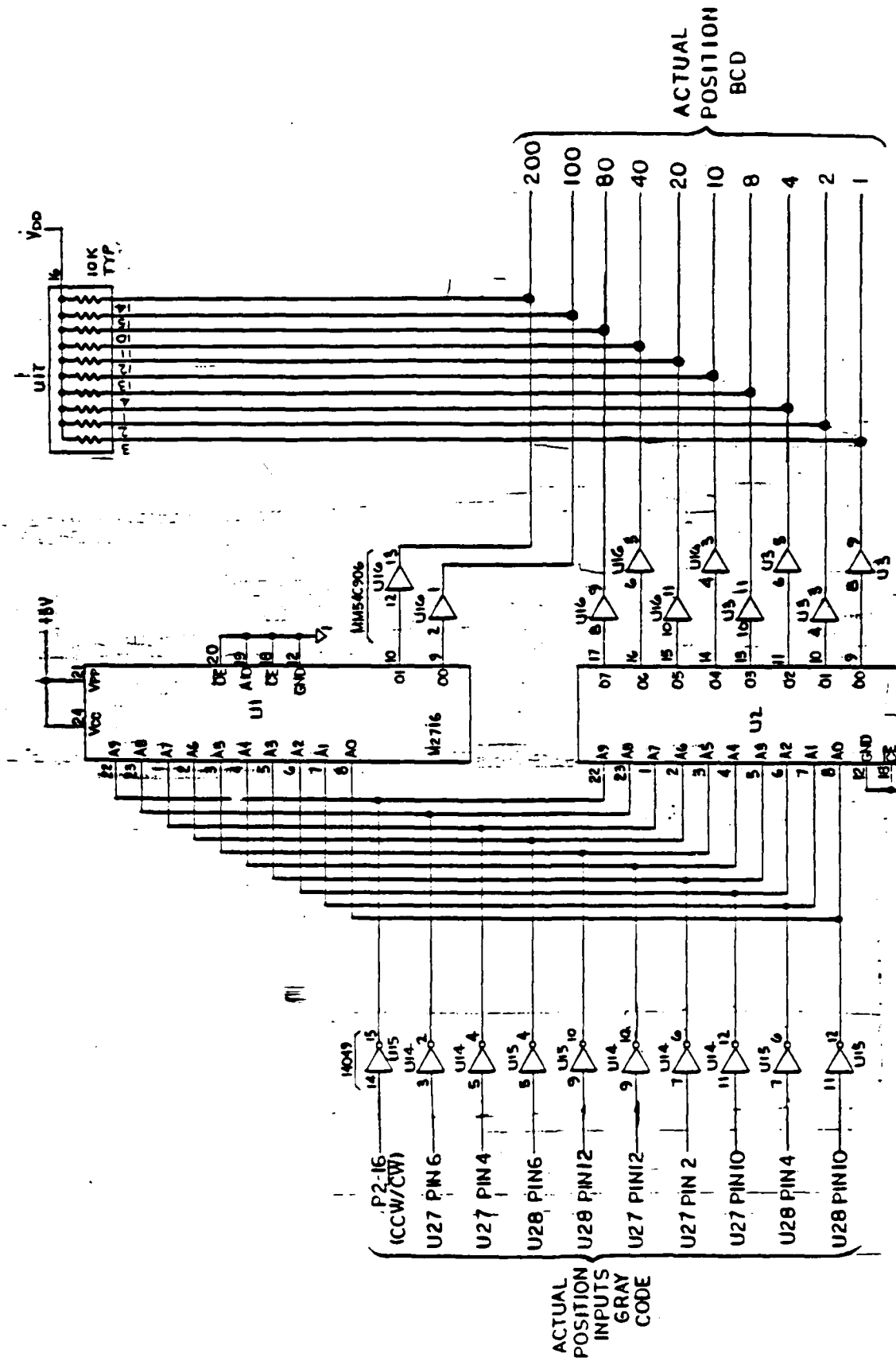


FIGURE 21 EPROM GRAY TO BCD CONVERTER

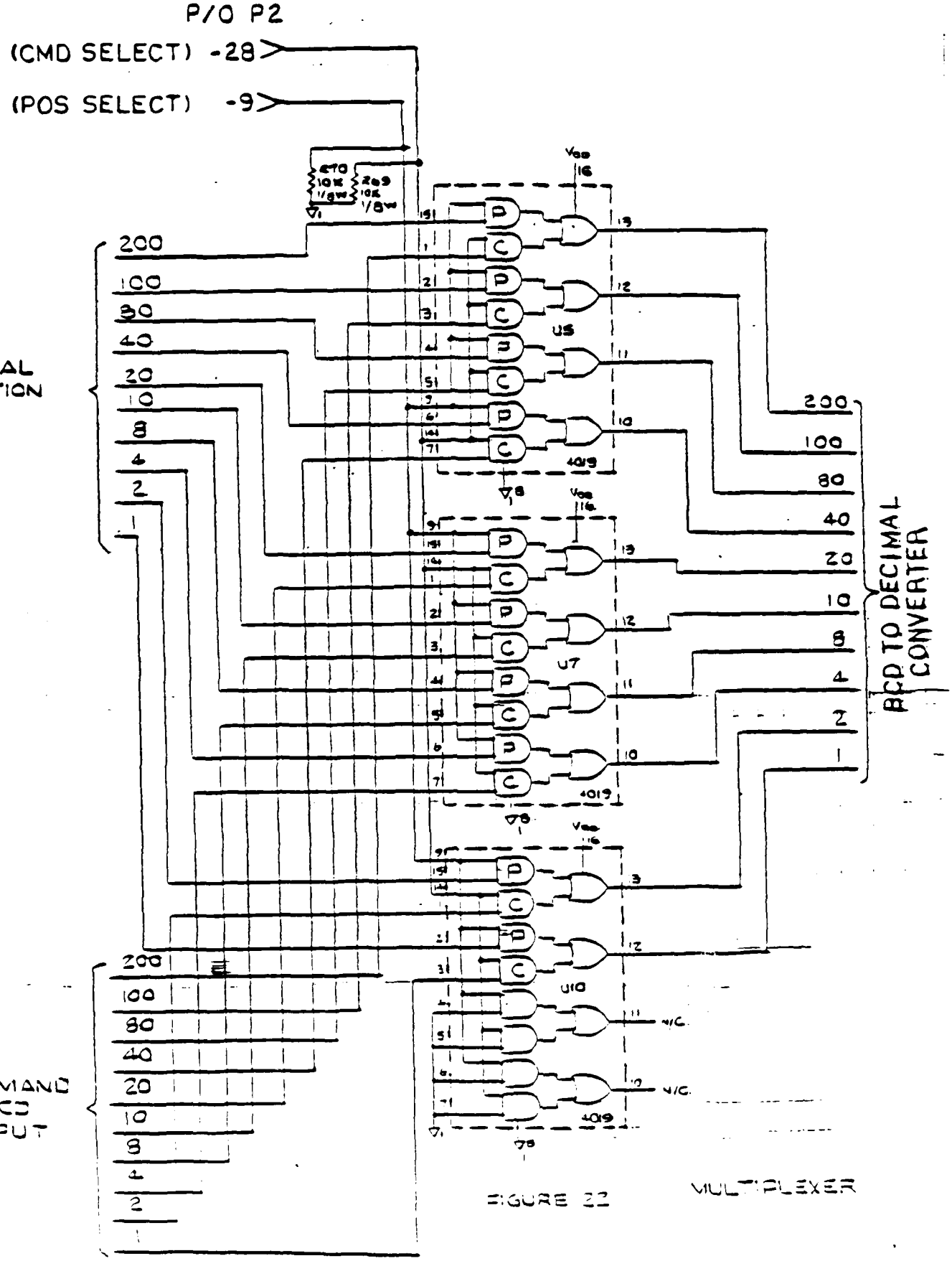


FIGURE 22 MULTIPLEXER

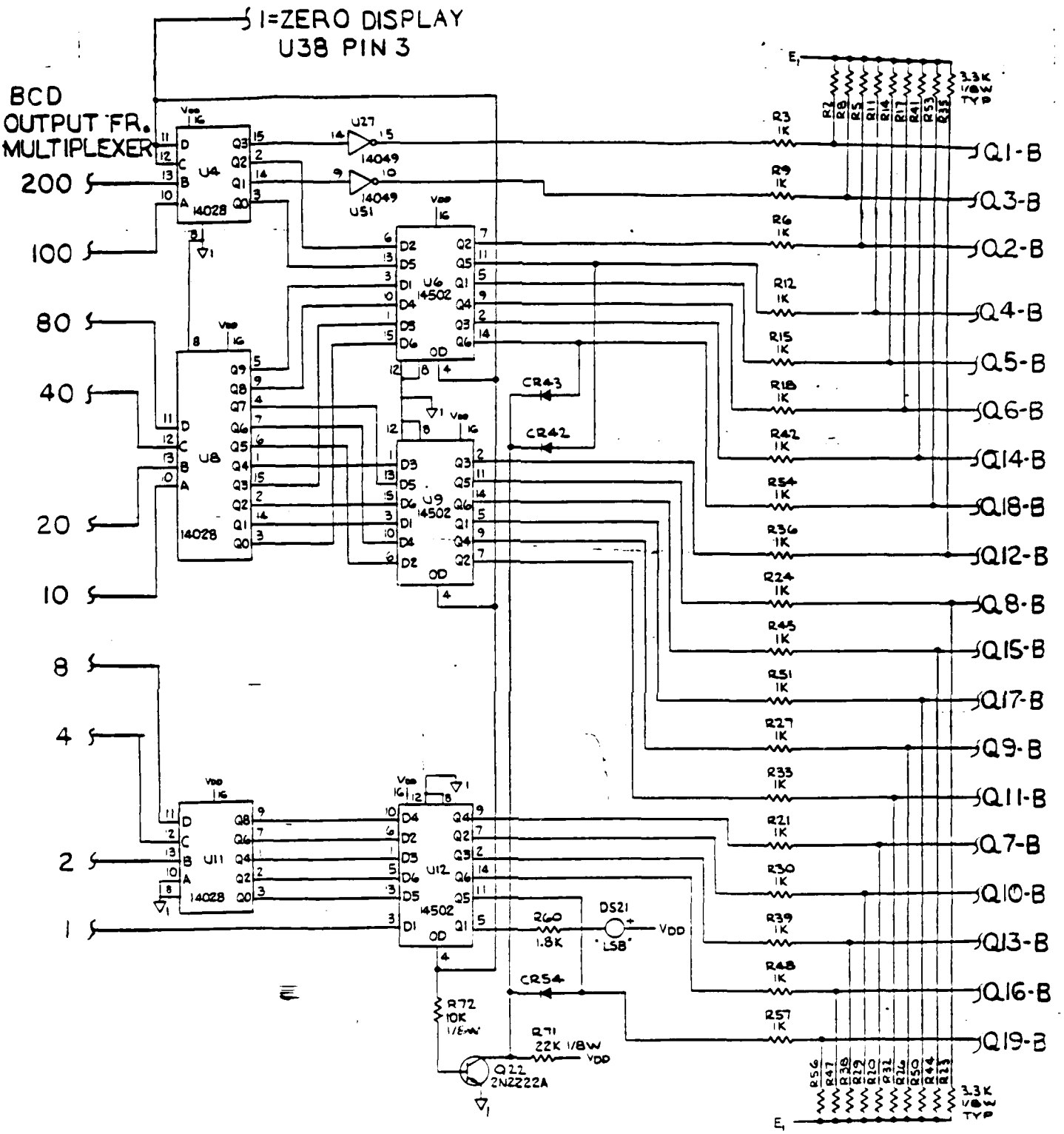
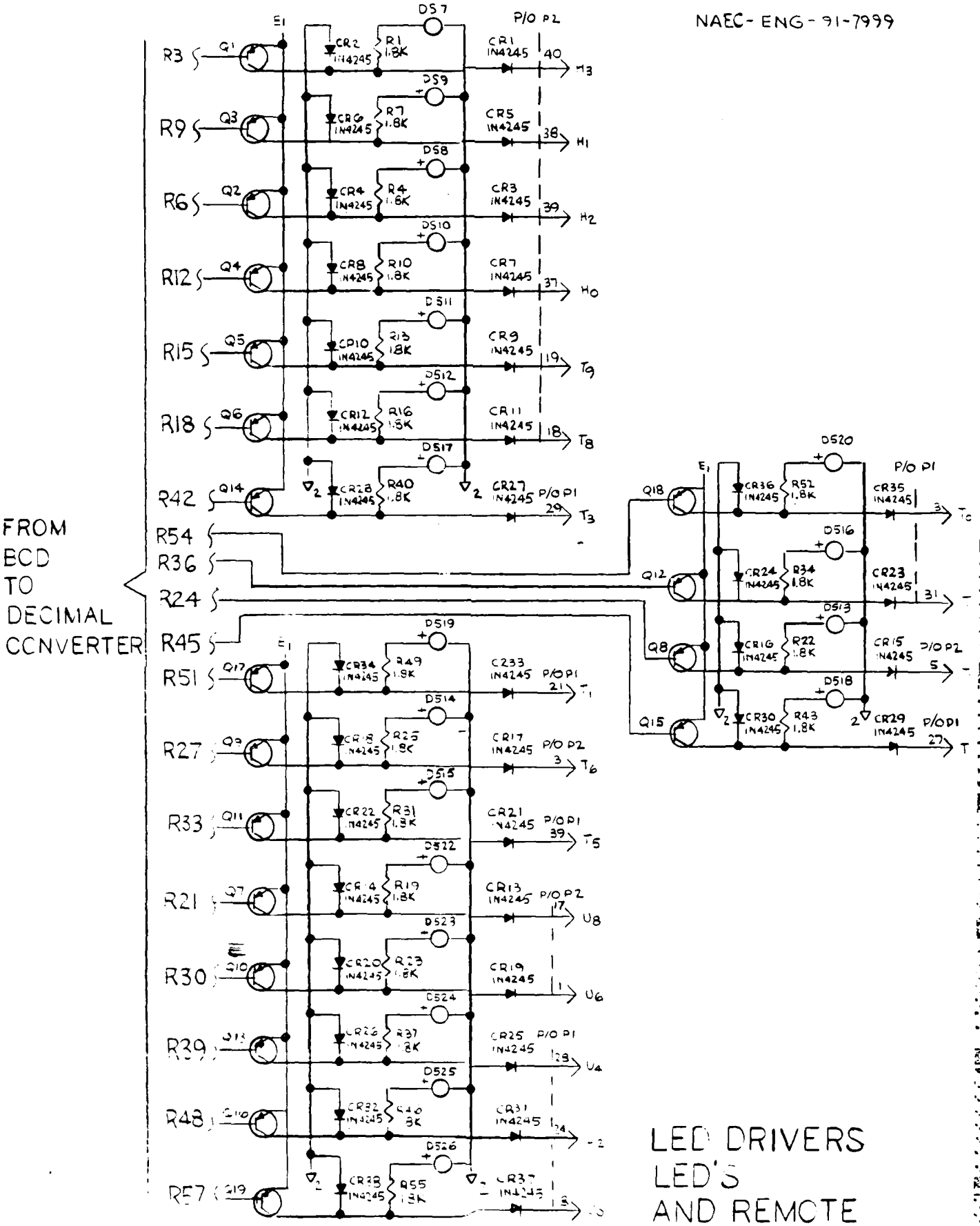


FIGURE 23 BCD TO DECIMAL CONVERTER



LED DRIVERS
LED'S
AND REMOTE
READOUT OUTPUTS

FIGURE 24

2. TEST REQUIREMENTS

a. There are four distinct circuits tested in this section. These tests are designed to go no-go tests. If any unusual indications are observed or the test criteria is not met then the card is considered defective.

The four sections tested are:

(1) EPROM gray to BCD converter

(2) Multiplexer

(3) BCD to decimal converter with zeroing

(4) LED drivers and LED's

b. (1) A count sequence of 000 to 359 in gray code for Channel A1 and 359 to 000 for channel A2 will be inputed to the circuit board along with the proper lead and lag parity signals.

(2) The output of the BCD subtractor circuit to the redundant board should be connected to the BCD subtractor output from the redundant board to remove the cross check subtractor circuit.

(3) The increase/decrease lines to the redundant board should be connected to the increase/decrease line outputs from the redundant boards.

(4) The zero signal line from the redundant board should have a high input to represent a no error situation.

(5) The zero disable line should have a low input so the output is able to be zero in case of an error.

(6) The command switch should be set to 000.

(7) The count sequence should be inputed for an encoder rotation correction factor of '1' (15VDC for Channel A1) and '0' (0VDC for Channel A2).

c. The actual position encoder inputs gray code bits G_0 thru G_8 are fed thru the gray to BCD converters, to the multiplexer, into the BCD to decimal converter, and out to the LED driver's which light the proper LED's.

The output LED's should be checked for the proper count sequence and the remote readout outputs will be compared to the input count.

In this test the parity bits for each count are checked.

The crosscheck subtractor circuit is also checked.

If there are any parity or crosscheck errors the displays will go to all zeros and the proper error ('PAR' or 'CHK') will light.

The test will stop if an error is detected and the display is zero or if the output count does not equal the input count.

The parity circuit and crosscheck/sign error circuits will be tested later. The tests in this section are included because of ease of testing these circuits along with testing the encoder inputs to readout sections.

3. TEST EQUIPMENT AND POWER REQUIREMENTS

a. 15VDC power supply

b. 5VDC power supply

c. Digital Multimeter, Fluke 800A or equivalent

d. Circuit card test fixture

e. Assorted test leads

4. PRELIMINARY TEST PROCEDURE

a. Connect the power plugs of the test equipment to a source of single phase, 60 Hz, 115 volt AC power.

b. Connect the DVM, +15 volt DC power supply, and +5 volt DC power supply to 110 to 125 volt AC power and turn on.

c. Adjust +15 volt and +5 volt power supplies to within + or -0.1 volt using DVM.

d. Place +15 volt and +5 volt power supply switches off.

e. Place counter/switch select switch (SW2) up to counter position.

f. Place counter on/off switch (SW6) down to off position.

g. Place encoder rotation correction factor switch (SW3) down to Channel A1 position.

h. Place decrease/increase input/output switch (SW7) to the down position for the decrease/increase signal from the main board output to the redundant board.

i. Place the zero disable switch (SW13) up to zero disable position.

j. Place the zeroing signal switch (SW12) up to normal position.

k. Set command input switch (SW21, 22 and 23) to 000.

m. Place POS/CMD select switch (SW17) up to 'Position' position. This selects 'position' output of multiplexers.

n. Insert the card to be tested in the test fixture.

5. FINAL TEST PROCEDURES

NOTE: Record test results on Data Sheet 1 (Appendix A).

a. Turn on +15 volt, and +5 volt power supplies.

b. Push counter clear switch (SW4).

c. Push count load switch (SW5). LED readouts on circuit board should read 000.

d. If output error light (DS1) is lit, push error reset switch (SW1).

e. Place counter on/off switch (SW6) up to the on position.

Observe the LED's on the board for a proper count sequence, that is, starts of 000 and counts to 359 (358 and LSB).

f. If an error occurs, the error light (DS1) will light and the count will stop. Record the count that the board stopped on the data sheet. Remove card and repair board.

g. Count sequence will stop after 359; place counter on/off switch (SW6) down to the off position.

i. Place encoder rotation correction factor switch (SW3) up to the Channel A2 position.

j. Push counter clear switch (SW4).

k. Push count load switch (SW5). LED readouts on a circuit board should read 359 (358 + LSB).

l. If output error light (DS1) is lit, push error reset switch (SW1).

m. Place counter on/off switch (SW6) up to the on position.

n. Observe the LED's on the board for a proper count sequence, that is, starts at 359 and counts to 000.

o. If an error occurs, the error light (DS1) will light and the count will stop. Record the count that the board stopped on the data sheet.

p. Turn off +115 volt and +5 volt power supplies.

q. End of test. Proceed to Section B.

B. BCD SUBTRACTOR CIRCUIT

1. CIRCUIT DESCRIPTION

a. The BCD subtractor checks the output of the command BCD input from the command switches against the actual position BCD input from the EPROM's on the board.

b. The BCD position signal (POS) from the EPROM's is fed to the BCD subtractor along with the command signal from the center deck command readout station (CMD). The BCD position is subtracted from the BCD command signal.

If the CMD input is greater than the POS input, the information from the subtractor is fed into the direction logic circuit which will activate a decrease signal that will be sent to relay K2.

If the POS input is greater than the CMD input, the information from the subtractor is fed into the direction logic circuit which will activate a increase signal that will be sent to relay K1.

c. The BCD subtractor circuit is shown in Figure 25.

The CMD signal is received thru current limit resistors (R101 thru R105) and (R107 thru 110). The CMD signal also passes thru excess voltage protection diodes (CR50 thru CR53), (CR71 thru CR79) and (CR80 thru CR86). The POS signal from the EPROM's is fed into buffers (U3 and U16). The BCD subtractor circuit consists of BCD adders (U19, U21 and U23) and nine's complementors (U18, U20, U22, U24, U31 and U34). The BCD subtractor circuit takes the POS signal into the BCD nines complementors (U18, U20, and U22) and performs a nines complement on the input data. The outputs of (U18, U20, and U22) are fed into BCD adders (U19, U21, and U23) along with the CMD signal. The BCD adders perform a subtraction of the two signals by adding the nines complement of the POS signal to the uncomplemented CMD signal.

A Low '0' carry 'Co' on (U19) indicates the difference is a negative number in 9's complement form.

A high '1' carry 'Co' on (U19) indicates the difference is a positive number.

The carry out 'Co' on (U19) is tied to the carry in 'C_N' on (U23). This end around carry is required because the subtraction is done in 9's complement arithmetic. The carry out 'Co' of (U19) is also tied to the complement pin c (pin 6) of (U24, U31, and U34).

If CMD is greater than POS the carry out 'Co' of (U19) is high '1'. The nines complementors (U24, U31, and U34) are disabled. The uncomplemented number is passed straight thru (U24, U31, and U34). The CMD-POS error output from (U24, U31, and U34) is a positive uncomplemented number.

If CMD is less than POS the carry out 'Co' of (U19) is low '0'. The nines complementors (U24, U31 and U34) are enabled. The output from (U19, U21, and U23) is nines complemented again returning the error difference to a positive uncomplemented state.

The carry out 'Co' is also used in the direction logic circuit. The output of the BCD subtractor circuit goes to the crosscheck subtractor and is fed to the redundant channel error output (P1 Pins 14 thru 17, 19, 20, 22, 23, 25).

2. TEST REQUIREMENTS

a. The BCD subtractor is tested in this section. This test is go no-go test. If any unusual indications are observed or the test criteria are not met then the card is considered defective.

b. A set of input counts will be inputed to the actual position inputs G_0 thru G_8 and the command BCD inputs.

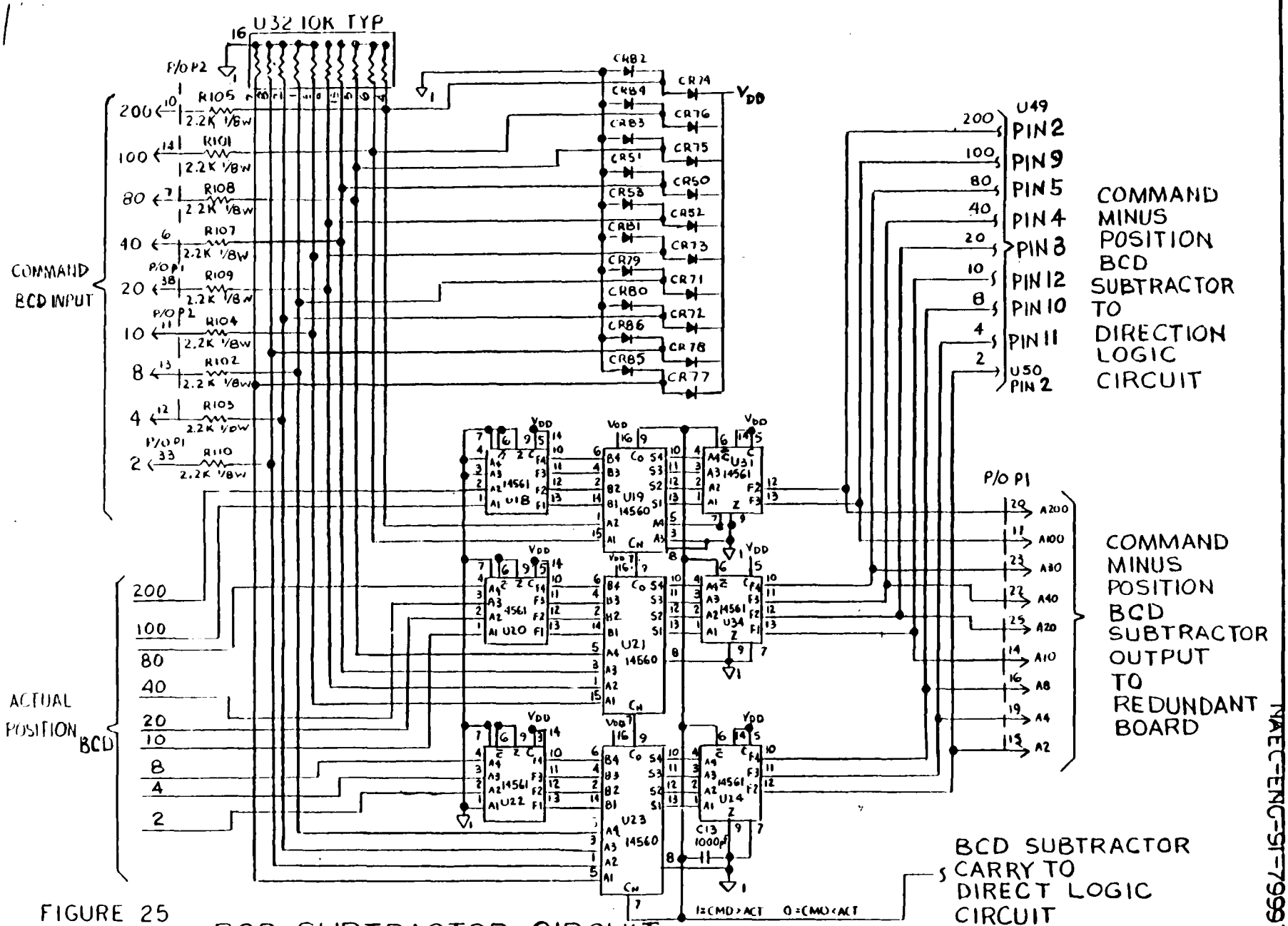


FIGURE 25

BCD SUBTRACTOR CIRCUIT

43 (REV A)

MAEC-ENG-SI-7999

c. The output of the command minus position BCD subtractor output will be compared to the proper count output. Any discrepancy will be considered an error.

3. TEST EQUIPMENT AND POWER REQUIREMENTS

a. 15VDC power supply

b. 5VDC power supply

c. Digital Multimeter, Fluke 800A or equivalent

d. Circuit card

e. Assorted test leads.

4. PRELIMINARY TEST PROCEDURE

a. Connect the power plugs of the test equipment to a source of single phase, 60 Hz, 115 volt AC power.

b. Connect the DVM, +15 volt DC power supply, and +5 volt. DC power supply to 110 to 125 volt AC power and turn on.

c. Adjust +15 volt and +5 volt power supplies to within + or -0.1 volt using DVM.

d. Place +15 volt and +5 volt power supply switches off.

e. Place encoder rotation correction factor switch (SW3) down to Channel A1.

f. Place counter/switch select switch (SW2) down to switch mode.

g. Set position input switch (SW18, 19, and 20) to 000.

h. Set command input switch (SW21, 22, and 23) to 000.

5. FINAL TEST PROCEDURES

NOTE: Record test results on Data Sheet 2 (Appendix A).

a. Turn on +15 volt and +5 volt power supplies.

b. Set position input switch (SW18, 19 and 20) and command input switch (SW21, 22, and 23) to values listed on data sheet.

Compare value on position minus command error readout (DS10, 11, and 12) to output listed on data sheet. Counts should be within $\pm$ 2 counts.

c. Turn off +15 volt and +5 volt power supplies.

d. End of test. Proceed to Section C.

C. DIRECTION LOGIC CIRCUIT

1. CIRCUIT DESCRIPTION

a. The direction logic circuit uses the output of the BCD subtractor to determine the direction (increase or decrease) the CSV must travel.

b. The Direction Logic Circuit schematic is shown in Figure 26.

The direction logic circuit uses the output of the CMD-POS subtractor, and the carry out 'Co' of the BCD subtractor (U19) to determine the direction the CSV must travel.

The circuitry used in the direction logic circuit consists of NOR gates (U49, and U50), inverters (U51) and LED (DS5).

The output of the CMD-POS subtractor is fed to a NOR gate circuit consisting of 8 input NOR gate (U49), inverter (U51), and NOR gate (U50). The NOR gate circuit will output a high '1' at (U50 Pin 3) if all input lines are low '0's' signifying position equals Command 'P=C'.

This 'P=C' output is fed to (U29 PIN 8) on each board for use in the coincidence circuitry and is also fed thru inverter (U51) to light LED (DS5) 'P=C' when position equals command. The 'P=C' line is fed into NOR gates (U50) along with the carry out 'Co' from (U19).

When CMD is greater than POS than 'Co' is high '1' which is fed thru inverter (U51) and inputed to (U50 Pin 8) as a low '0'. When the 'P=C' line is low '0' at the same time the output of NOR gate (U50 Pin 10) will be a '1' indicating an increase direction.

When CMD is less than POS then 'Co' is low '0' which when fed into (U50 Pin 13) along with the low '0' from the 'P=C' line causes the output of NOR gate (U50 Pin 11) to be a '1' indicating a decreasing direction.

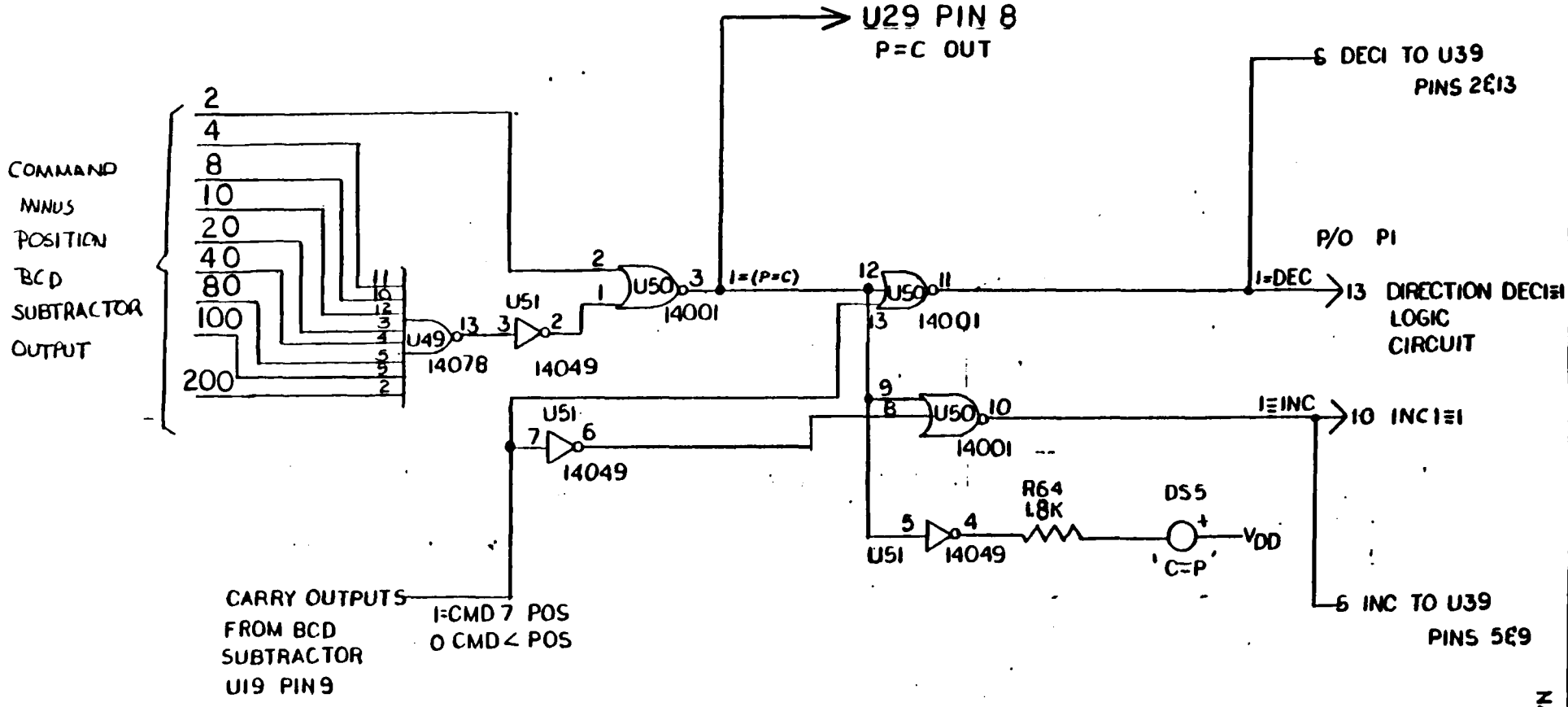


FIGURE 26 DIRECTION LOGIC CIRCUIT

2. TEST REQUIREMENTS

a. The direction logic circuit is tested in this section. This test is a go no-go test. If any unusual indications are observed or the test criteria are not met then the card is considered defective.

b. A set of input counts will be inputed to the Actual Position inputs G_0 thru G_8 and the command BCD inputs.

c. The increase and decrease signals will be checked for the proper output. Any discrepancy will be considered an error.

3. TEST EQUIPMENT AND POWER REQUIREMENTS

a. 15VDC power supply

b. 5VDC power supply

c. Digital Multimeter, Fluke 800A or equivalent

d. Circuit card test fixture

e. Assorted test leads.

4. PRELIMINARY TEST PROCEDURE

a. Connect the power plugs of the test equipment to a source of single phase, 60 Hz, 115 volt AC power.

b. Connect the DVM, +15 volt DC power supply, and +5 volt DC power supply to 110 to 125 volt AC power and turn on.

c. Adjust +15 volt and +5 volt power supplies to within + or -0.1 volt using DVM.

d. Place +15 volt and +5 volt power supply switches off.

e. Place counter/switch select switch (SW2) down to switch position.

f. Place encoder rotation correction factor switch (SW3) down to Channel A1 position.

g. Place decrease/increase/input/output select switch (SW7) to the up position for Dec/Inc signal to lights.

5. FINAL TEST PROCEDURES

NOTE: Record test results on Data Sheet 3 (Appendix A).

a. Turn on +15 volt and +5 volt power supplies.

b. Set position input switch (SW18, 19, and 20) and command input switch (SW21, 22 and 23) to values listed on Data Sheet. Check for proper output on board position LED's and 'INC' (DS9) and 'DEC' (DS8) lights on test set-up.

c. Place encoder rotation correction factor switch (SW3) up to Channel A2 position. Set position input switch (SW18, 19 and 20) and command input switch (SW21, 22 and 23) to values listed on Data Sheet. Check for proper output on board LED's and lights on test set-up.

d. Turn off +15 volt and +5 power supplies.

e. End of Test. Proceed to Section D.

D. INCREASE/DECREASE CIRCUIT

1. CIRCUIT DESCRIPTION

a. The increase/decrease circuit takes the signal from the direction logic circuits and conditions it to drive external relays K1 and K2.

b. The schematic for the increase/decrease circuit is shown in Figure 27.

The circuitry used consists of inverters (U26 and U51), and gates (U39) transistors (Q20 and Q21), Diodes (CR44 thru CR49) and LED indicators (DS4 and DS6).

When CMD is greater than the pos signal the output of (U50 Pin 10) is high '1'. This '1' is fed into AND gate (U39 Pin 9). The output of the decrease circuit from the redundant board (DEC 2) is fed thru inverter (U51) into (U39 Pin 8).

When both of these inputs are high '1' the output of (U39 Pin 10) is high '1'. This signal is fed into inverter (U26) and the switch to ground '0' turns on transistor (Q21) which lights 'INC' LED (DS4) and feeds a '1' to the increase relay (K1) thru (P1 Pin 9).

When CMD is less than the pos signal the output of (U50 Pin 11) is high '1'. This '1' is fed into AND gate (U39 Pin 13). The output of the increase circuit from the redundant board (INC 2) is fed thru inverter (U51) into (U39 Pin 1).

When both of these inputs are high '1' the output of (U39 Pin 3) is high '1'. This signal is fed into inverter (U26) and the switch to ground '0' turns on transistor (Q20) which lights 'DEC' LED (DS6) and feeds a '1' to the decrease relay (K2) thru (P1 Pin 11).

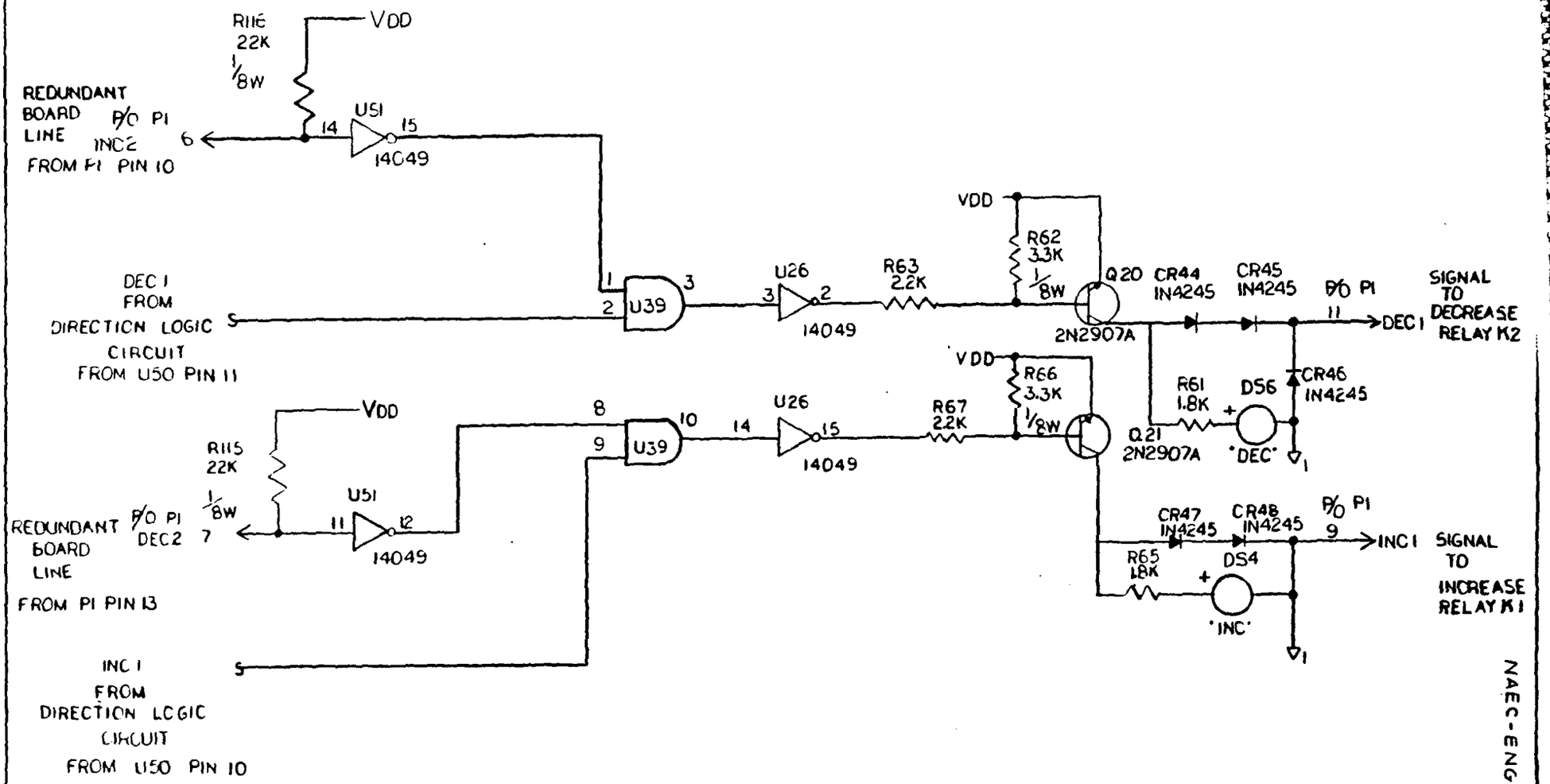


FIGURE 27 INCREASE / DECREASE CIRCUIT

2. TEST REQUIREMENTS

a. The increase/decrease circuit is tested in this section. This test is a go no-go test. If any unusual indications are observed or the test criteria are not met then the card is considered defective.

b. A set of input counts will be inputed to the actual position inputs G_0 thru G_8 and the command BCD inputs.

c. The increase and decrease lines to the external relays will be checked for proper output along with the 'INC' or 'DEC' LED's on the boards.

3. TEST EQUIPMENT AND POWER REQUIREMENTS

a. 15VDC power supply

b. 5VDC power supply

c. Digital Multimeter, Fluke 800A or equivalent

d. Circuit card test fixture

e. Assorted test leads.

4. PRELIMINARY TEST PROCEDURE

a. Connect the power plugs of the test equipment to a source of single phase, 60 Hz, 115 volt AC power.

b. Connect the DVM, +15 volt DC power supply, and +5 volt DC power supply to 110 to 125 volt AC power and turn on.

c. Adjust +15 volt and +5 volt power supplies to within + or -0.1 volt using DVM.

d. Place +15 volt and +5 volt power supply switches off.

e. Place counter/switch select switch (SW2) down to switch position.

f. Place encoder rotation correction factor switch (SW3) down to Channel 1 position.

2. TEST REQUIREMENTS

a. The increase/decrease circuit is tested in this section. This test is a go no-go test. If any unusual indications are observed or the test criteria are not met then the card is considered defective.

b. A set of input counts will be inputed to the actual position inputs G_0 thru G_8 and the command BCD inputs.

c. The increase and decrease lines to the external relays will be checked for proper output along with the 'INC' or 'DEC' LED's on the boards.

3. TEST EQUIPMENT AND POWER REQUIREMENTS

a. 15VDC power supply

b. 5VDC power supply

c. Digital Multimeter, Fluke 800A or equivalent

d. Circuit card test fixture

e. Assorted test leads.

4. PRELIMINARY TEST PROCEDURE

a. Connect the power plugs of the test equipment to a source of single phase, 60 Hz, 115 volt AC power.

b. Connect the DVM, +15 volt DC power supply, and =5 volt DC powers supply to 110 to 125 volt AC power and turn on.

c. Adjust +15 volt and +5 volt power supplies to within + or -0.1 volt using DVM.

d. Place +15 volt and +5 volt power supply switches off.

e. Place counter/switch select switch (SW2) down to switch position.

f. Place encoder rotation correction factor switch (SW3) down to Channel 1 position.

g. Place decrease/increase input/output select switch (SW7) down to Dec/Inc signal to redundant board input.

h. Place decrease signal switch (SW8) up to high position.

i. Place increase signal switch (SW9) up to high position.

j. Set position input switch (SW18, 19, and 20) to 000.

k. Set command input switch (SW21, 22, and 23) to 000.

5. FINAL TEST PROCEDURES

NOTE: Record test results on Data Sheet 4 (Appendix A)

a. Turn on +15 volt, and +5 volt power supplies.

b. Set position input switch (SW18, 19, and 20) to 166.

c. Set command input switch (SW21, 22, and 23) to 310.

d. Set decrease signal switch (SW9) down to 'low' position.

e. Check that circuit board LED (DS4) 'inc' is lit.

f. Check that 'inc' relay input light on test set-up (DS3) is lit.

g. Set decrease signal switch (SW9) up to high position.

h. Set position input switch (SW18, 19, and 20) to 310.

i. Set command input switch (SW21, 22, and 23) to 166.

j. Set increase signal switch (SW8) down to 'low' position.

k. Check that circuit board LED (DS6) 'dec' is lit.

l. Check that 'dec' relay input light on test set-up (DS2) is lit.

m. Turn off +15 volt, and +5 power supplies.

n. End of test. Proceed to Section E.

E. CROSSCHECK SUBTRACTOR CIRCUIT

1. CIRCUIT DESCRIPTION

a. The crosscheck subtractor checks the output of the BCD subtractor on the main board against the output of the BCD subtractor on the redundant board. If an error is detected in the crosscheck subtractor or the sign error circuit the 'CHK' LED lights and the relay K1 deenergizes opening the circuit to external relays K4 and K5 which would disengage the K3 conincidence relay.

b. The crosscheck subtractor circuit is shown in Figure 28. The crosscheck subtractor works similarly to the BCD CMD-POS subtractor. The crosscheck subtractor takes the output of the BCD CMD-POS subtractor and subtracts it from the error input of the redundant channel.

The crosscheck subtractor circuit consists of BCD adders (U43, U46, and U48) and nine's complementors (U33, U35, U37, U42, U45, and U47).

The error input from the redundant channel (ER2) is fed into BCD nines complementors (U42, U45, and U47) and performs a nines complement on this data. The outputs of (U42, U45, and U47) are fed into BCD adders (U43, U46 and U48) along with the output of the BCD CMD-POS subtractor (ER1). The BCD adders perform a subtraction of the two signals by adding the nines complement of the ER2 signal to the uncomplemented ER1 signal.

A Low '0' carry 'C_O' on (U43) indicates the difference is a negative number in 9's compliment form.

A high '1' carry 'C_O' on (U43) indicates the difference is a positive number.

The carry out 'C_O' on (U43) is tied to the carry in C_N on (U48).

This end around carry is required because the subtraction is done in 9's complement arithmetic. The carry out 'Co' of (U43) is also tied to the complement Pin c (Pin 6) of (U33, U35, and U37).

If ER1 is greater than ER2 the carry out 'Co' of (U43) is high '1'. The nine's complementors (U33, U35 and U37) are disabled. The uncomplemented number is passed straight thru (U33, U35, and U37). The ER1-ER2 crosscheck output from (U33, U35, and U37) is a positive uncomplemented number.

If ER1 is less than ER2 the carry out 'Co' of (U43) is low '0'. The nine's complementors (U33, U35, and U37) are enabled. The output from (U33, U35, and U37) is nine's complimented again returning the error difference to a positive uncomplemented state.

The crosscheck/sign error circuit consists of NOR gate (U36), inverters (U26), LED indicator (DS1) and relay (K1).

The output of the sign error circuit from (U25 PIN 6) is inputed into NOR gate (U36 Pin 12). The output of the BCD crosscheck error circuit without the two least significant bits are also fed into (U36) also. The crosscheck error circuit is set to trigger when there is a 4 count or greater discrepancy between boards.

If any input line to (U36) is high '1' the output (U36 Pin 13) will be low '0'. This signal is fed into inverter (U26) which disable the crosscheck/sign error board relay (K1) which will break the circuit to external relays (K4 or K5) thereby disabling the external conincidence relay (K3). The signal is also fed into inverter (U26 Pin 7) which will output a low '0' which will light 'CHK' LED (DS1).

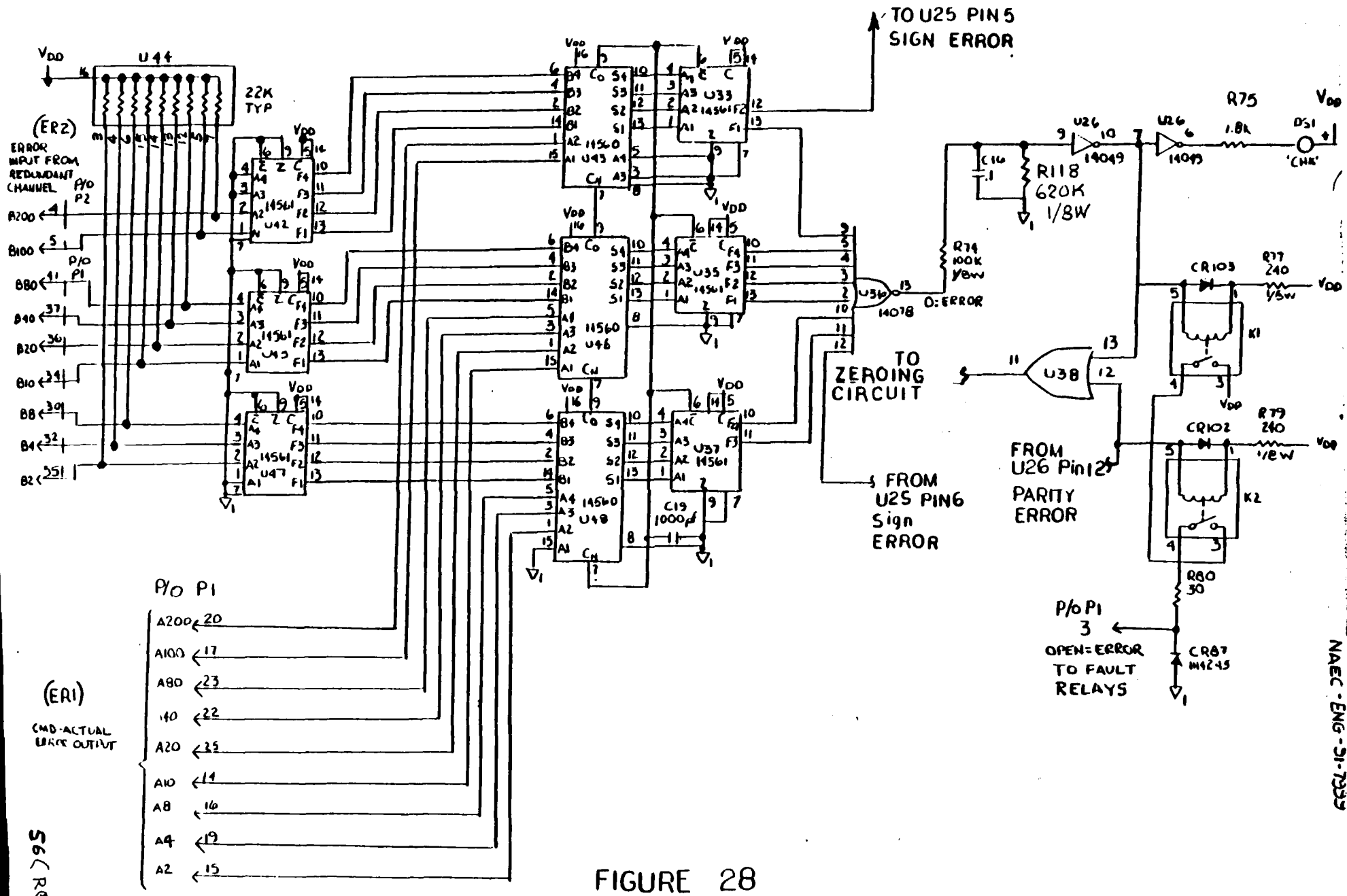


FIGURE 28
CROSSCHECK SUBTRACTOR CIRCUIT

2. TEST REQUIREMENTS

a. The crosscheck subtractor circuit is tested in this section. This test is a go no-go test. If any unusual indications are observed or the test criteria are not met then the card is considered defective.

b. A set of input counts will be inputed to the actual position inputs G_0 thru G_8, the command BCD inputs and the error input from the redundant channel.

c. The output of the crosscheck subtractor is checked by observing the output of the 'CHK' LED on the board and monitoring the output to the fault relays.

3. TEST EQUIPMENT AND POWER REQUIREMENT

a. 15VDC power supply

b. 5VDC power supply

c. Digital Multimeter, Fluke 800A or equivalent

d. Circuit card test fixture

e. Assorted test leads.

4. PRELIMINARY TEST PROCEDURE

a. Connect the power plugs of the test equipment to a source of single phase, 60 Hz, 115 volt AC power.

b. Connect the DVM, +15 volt 1DC power supply, and +5 volt DC power supply to 110 to 125 volt LAC power and turn on.

c. Adjust +155 volt and +5 volt power supplies to within + or -0.1 volt using DVM.

d. Place +15 vvolt and +5 volt power supply switches off.

e. Place counter/switch select switch (SW2) down to switch position.

f. Place encoder rotation correction factor switch (SW3) down to Channel A1 position.

g. Set position input switch (SW18 , 19, and 20) to 100.

h. Set command input switch (SW21, 22, and 23) to 100.

i. Set redundant board POS-CMD error switch (crosscheck) (SW24, 25, and 26) to 000.

j. Place Dec/inc in/out select switch (SW7) down.

k. Place decrease signal switch (SW8) and increase signal switch (SW9) down.

5. FINAL TEST PROCEDURES

NOTE: Record test results on Data Sheet 5 (Appendix A).

a. Turn on +15 volt and +5 volt power supplies.

b. Place redundant board POS-CMD error switch (crosscheck) (SW24, 25, and 26) to 002. Observe circuit board 'CHK' LED (DS1) and test set-up 'FAULT' lights (DS4) are not lit.

c. Place redundant board POS-CMD error switch (crosscheck) (SW24, 25, and 26) to 004 observe circuit board 'CHK'and test set-up 'FAULT' lights (DS4) are lit.

d. Place redundant board POS-CMD error switch (crosscheck) (SW24, 25, and 26) to 000.

e. Place command input switch (SW21, 22, and 23) to the values listed on the data sheet. Check to see circuit board 'CHK' (DS1) and the test set-up 'FAULT' light DS40 match data sheet.

f. Place the redundant board POS-CMD error switch (crosscheck) (SW24, 25, and 26) to 100.

g. Place the redundant board POS-CMD error switch (crosscheck) (SW24, 25, and 26) to the values listed on the data sheet. Check to see that the circuit board 'CHK' (DS1) and test set-up 'FAULT' light (DS4) are lit.

h. Turn off +15 volt and +5 volt power supplies

i. End of Test. Proceed to Section F.

F. SIGN ERROR CIRCUIT

1. CIRCUIT DESCRIPTION

a. The sign error circuit determines if there is an error in the increase or decrease circuits such as a failure of one input bit.

b. The sign error inputs are the increase and decrease lines from the direction logic circuit and the increase and decrease lines from the redundant board. Also included in this circuit is the 200's output from the crosscheck BCD subtractor due to a lack of inputs in the 8 input NOR gate (U36).

c. The coincidence circuit schematic is shown in Figure 29.

The sign error circuitry uses AND gates (U39) and 3 input OR gate (U25). The outputs of the Direction Logic Circuit (U50 Pin 11) for decrease (DEC) and (U50 Pin 10) for increase (INC) are fed in AND gates (U39). The Increase and Decrease outputs from the redundant check board is also fed into AND gates (U39).

If there is an error between the direction indicated by channel A1 or A2. The output of (U39 Pin 11) will be high '1' for an INC error. The output of (U39 Pin 4) will be high '1' for a DEC error.

The output of (U39 Pins 4 and 11) are fed into an OR gate (U25) along with the hundreds output of the crosscheck subtractor.

If any of the inputs to (U25) are high '1's there will be a high '1' at the output (U25 Pin 6). This output is fed into the 'CHK' error circuitry.

2. TEST REQUIRMENT

a. The sign error circuit is tested in this section. This test is a go no-go test. If any unusual indications are observed or the test criteria are not met then the card is considered defective.

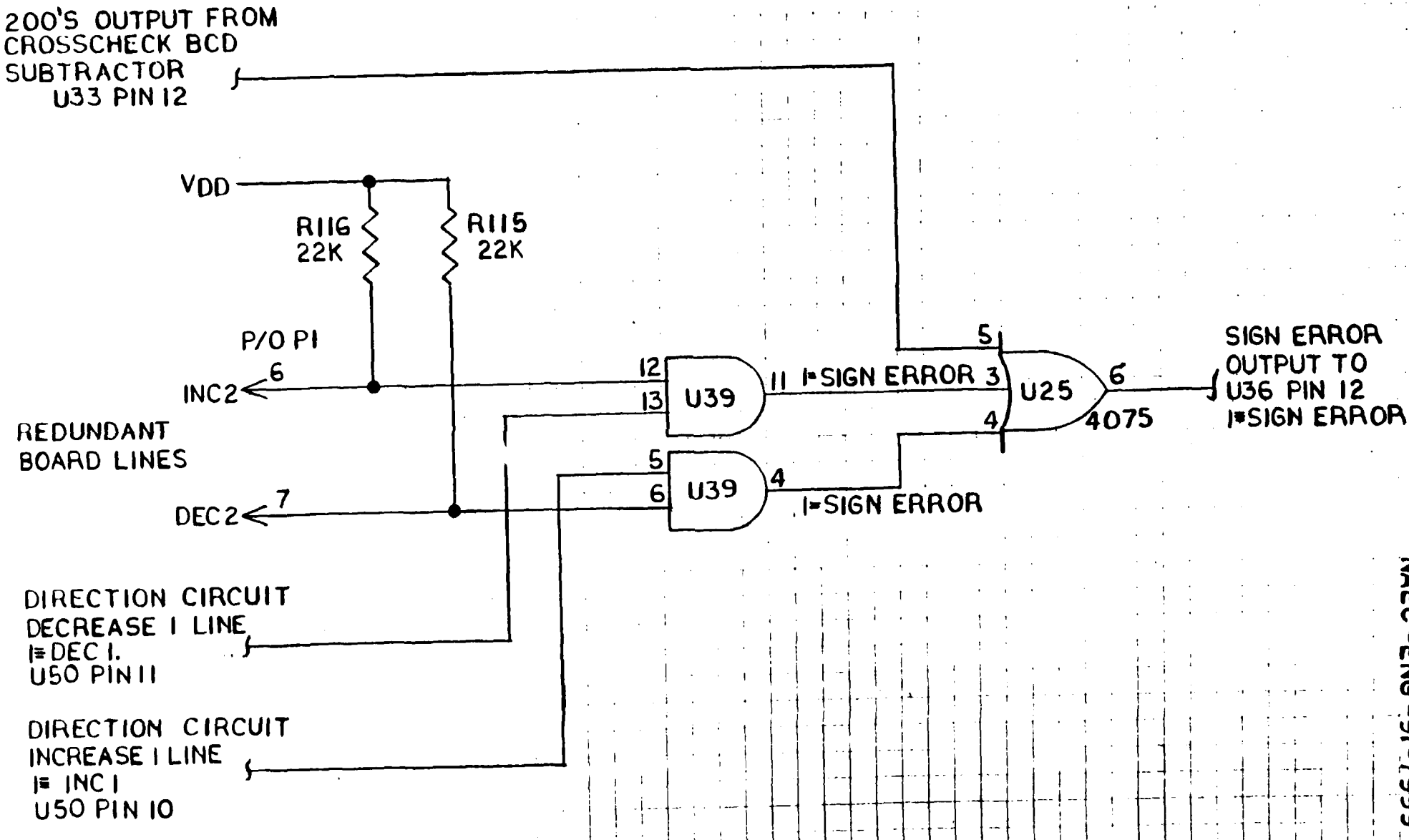


FIGURE 29 SIGN ERROR CIRCUIT

b. A set of input counts will be inputed to the actual position inputs G_0 thru G_8, the command BCD inputs and increase and decrease lines from the redundant board.

c. The output of the sign error circuit is checked by observing the output of the 'CHK' LED on the board and monitoring the output to the fault relays.

3. TEST EQUIPMENT AND POWER REQUIREMENTS

a. 15VDC power supply

b. 5VDC power supply

c. Digital Multimeter, Fluke 800A or equivalent

d. Circuit card test fixture

e. Assorted test leads.

4. PRELIMINARY TEST PROCEDURE

a. Connect the power plugs of the test equipment to a source of single phase, 60 Hz, 115 volt AC power.

b. Connect the DVM, +15 volt DC power supply, and +5 volt DC power supply to 110 to 125 volt AC power and turn on.

c. Adjust +15 volt and -5 volt power supplies to within + or -0.1 volt using DVM.

d. Place +15 volt and -5 volt power supply switches off.

e. Place counter/switch select switch (SW2) down to switch position.

f. Place encoder rotation correction factor switch (SW3) down to Channel A1 position.

g. Set decrease/increase input/output select switch (SW7) down to DEC/INC signal to redundant board input.

h. Set decrease signal input (SW8) down to low.

i. Set increase signal input (SW9) down to low.

5. FINAL TEST PROCEDURES

NOTE: Record test results on Data Sheet 6 (Appendix A).

a. Turn on +15 volt and +5 volt power supplies.

b. Place decrease signal switch (SW8) up to high position.

c. Set position input switch (SW18, 19, and 20) to 128.

d. Set command input switch (SW21, 22, and 23) to 246.

e. Check that circuit board 'CHK' LED (DS1) is lit and test set-up fault light (DS4) is lit.

f. Place decrease signal switch (SW8) down to low position.

g. Place increase signal switch (SW9) up to high position.

h. Set position input switch (SW18, 19 and 20) to 248.

i. Set command input switch (SW21, 22, and 23) to 120.

j. Check that circuit board 'CHK' LED (DS1) is lit and test set-up 'FAULT' light (DS4) is lit.

k. Turn off +15 volt and +5 volt power supplies.

l. End of test. Proceed to Section G.

G. PARITY ERROR CIRCUIT

1. CIRCUIT DESCRIPTION

a. A parity or bit check is applied to the inputed gray code data to determine if the data has been transmitted correctly. When a parity error is detected board relay K2 will open and LED DS2 will light.

b. The encoder pattern for the parity bits are read by a "lead" brush (J2 Pin 15) and a "lag" brush (J2 Pin 23). The gray code pattern (bits G_8 thru G_0) will have only one bit change state for each count of the encoder. The time interval between one gray code bit transition and the next transition (cell interval) will have a parity bit change state while the other parity signal will be maintained at a constant logic level. The parity check logic will only "look at" the parity bit signal that is held at a constant logic level during the cell interval. The pattern of the generated parity signal (when looking at the PLD or PLG brush) is to alternate between a "constant level" and a transition.

c. A schematic for the parity error circuit is shown in Figure 30.

The nine bit gray code with the exception of the least significant bit (LSB) G_0 is inputed to Parity Check I.C. (U13). This data is compared to the output of the Parity bit changing bit mask circuit consisting of exclusive OR gate (U41) and AND gate (U30).

The parity changing bit mask circuit has as its inputs LEAD and LAG signals from the encoders, Binary Coded Decimal Least Significant Bit (BCD LSB) from the EPROM output and the encoder direction correction factor.

The BCD LSB is fed into (U41 Pin 2). The Encoder Direction correction factor is fed into (U41 Pin 1).

For channel A1 this signal is high '1'.

For channel A2 this signal is ground '0'.

The output of (U41 Pin 3) is fed into NAND gate (U30 Pin 1) which acts as an inverter and into NAND gate (U30 Pin 9). The lead signal is fed into NAND gate (U30 Pin 13) along with the inverted output of (U41 Pin 3). The Lag signal is fed into NAND gate (U30 Pin 8) along with the output of (U41 Pin 3). The output of these two AND gates are fed into NAND gate (U30 Pins 5 and 6). The output of NAND gate (U30 Pin 4) is the masked Parity signal (that is the signal that is not changing) this data is inputed to (U13 Pin 10) and is compared to the parity of the sum of bits G_1 thru G_8.

Any error between the two will cause the parity check line (U13 Pin 9) to go 'low'. The parity check signal from (U13 Pin 9) is used to light 'PAR' LED (DS2), disable board parity relay (K2), and is fed to zeroing circuit thru U38 Pin 12.

The parity check indicator circuitry consist of inverters (U26), indicator (DS2) and relay (K2). The parity check signal is fed into inverter (U26). When a parity error occurs the output (U26 Pin 12) will be high '1'. This will disable (K2) which will break the circuit to external relays (K4 or K5) thereby dis-abling the external conincidence relay (K3). The output of inverter (U26 Pin 12) is also inputed to inverter (U26 Pin 5) which when there is a parity error lights 'PAR' LED (DS2).

2. TEST REQUIREMENTS

a. The parity error circuit is tested in this section. This test is a go no-go test. If any unusual indications are observed or the test criteria are not met then the card is considered defective.

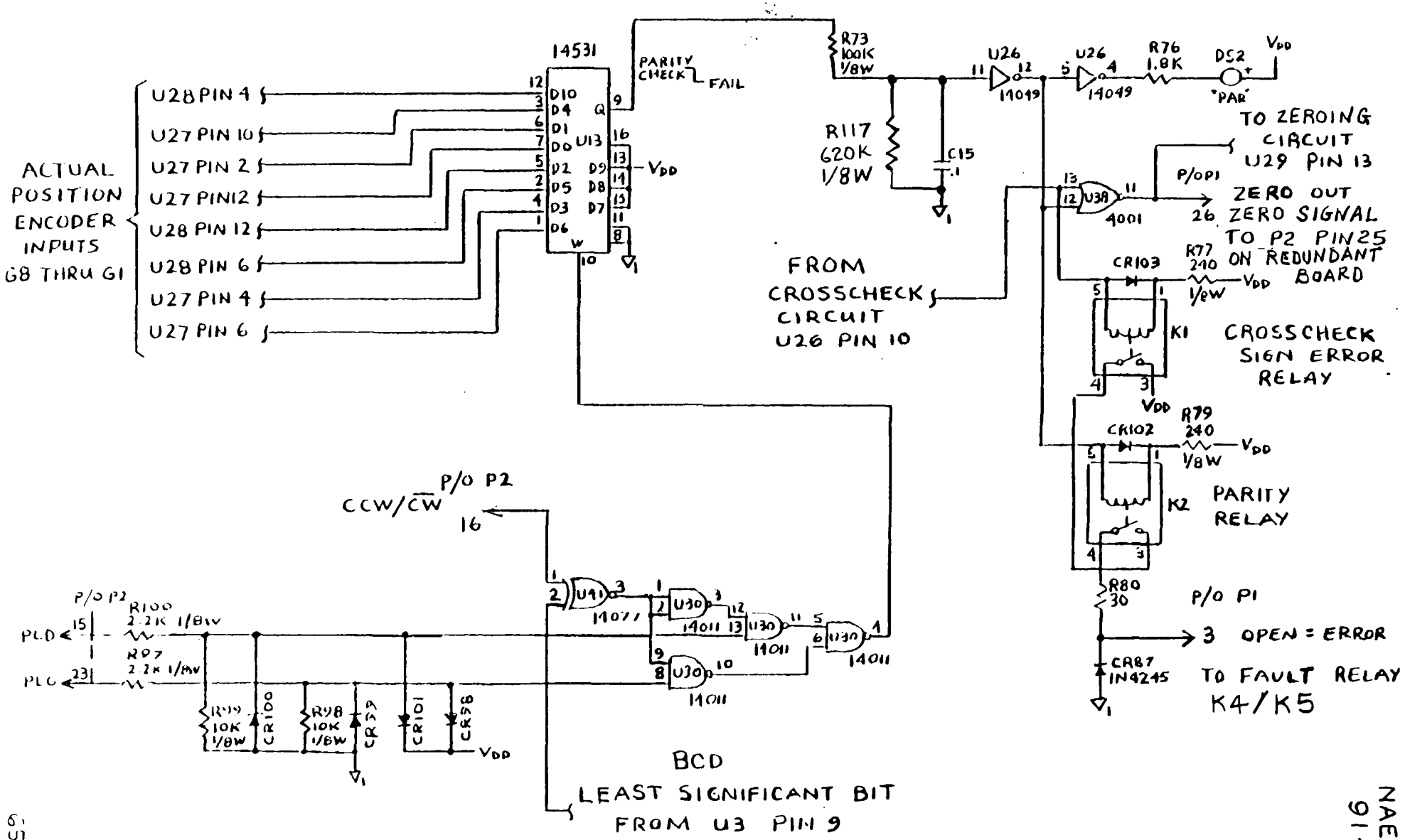


FIGURE 30 PARITY CIRCUIT

b. A set of parity signals; lead and lag, will be inputed into the parity circuit.

c. The output of the parity circuit is checked by observing the output of the "PAR' LED on the board and monitoring the output to the fault relays.

3. TEST EQUIPMENT AND POWER REQUIREMENTS

a. 15VDC power supply

b. 5VDC power supply

c. Digital Multimeter, Fluke 800A or equivalent

d. Circuit card test fixture

e. Assorted test leads.

4. PRELIMINARY TEST PROCEDURES

a. Connect the power plugs of the test equipment to a source of single phase, 60 Hz, 115 volt AC power.

b. Connect the DVM, +15 volt DC power supply, and +5 volt DC power supply to 110 to 125 volt AC power and turn on.

c. Adjust +15 volt and +5 volt power supplies to within + or -0.1 volt using DVM.

d. Place +15 volt and +5 volt power supply switches off.

e. Place counter/switch select switch (SW2) down to switch position.

f. Place encoder rotation correction factor switch (SW3) down to Channel A1 position.

g. Place decrease/increase input/output switch (SW7) to down position for the decrease/increase signal from the main board output to the redundant board.

h. Place parity lead switch (SW10) down to low position.

i. Place parity lag switch (SW11) down to low position.

j. Set position input switch (SW18, 19, and 20) to 102.

5. FINAL TEST PROCEDURES

NOTE: Record test results on Data Sheet 7 (Appendix A).

a. Turn on +15 volt and +5 volt power supplies.

b. Place the PARITY LEAD switch (SW10) and the PARITY LAG switch (SW11) to the positions listed on the data sheet and check for the proper response from the test set-up 'FAULT' (DS4) and 'ZERO' (DS5) lights and the circuit board 'PAR' LED (DS2).

c. Turn off + 15 volt and +5 volt power supply.

d. End of test. Proceed to section H.

H. ZEROING CIRCUIT

1. CIRCUIT DESCRIPTION

a. When a parity, crosscheck or sign error is detected the outputs will be zero. This brings an error to the attention of the operator. A zero disable line from the built in test equipment (BITE) switch is fed into the circuit to disable the output zeroing when the error input test signals are inputed, and to help troubleshoot the system when there are errors.

b. The zeroing circuit is shown in Figure 31.

The zero disable lines are enabled by a parity error crosscheck/ sign error, or zero input from the redundant board. The circuity used in the zero disable circuit are NOR gates (U38) and AND gate (U29). When there is a parity or crosscheck/sign error. A high '1' is fed into (U38). If either or both signals are high '1's the output of (U38 Pin 11) is low '0'. The output of (U38 Pin 11) is fed to the redundant circuit board thru zero out (P1 pin 26).

The zero signal from the redundant channel A2 is fed into channel A1 thru (P2 Pin 25) and is fed into AND gate (U29) along with the error signal from (U38 Pin 11). If any inputs to (U29) (Pins 11, 12, and 13) are low '0's'. The output of (U29 Pin 10) will be low '0'. The output of (U29 Pin 10) is fed into NOR gate (U38 Pin 2) along with a zero disable signal from the BITE switch from (P1 Pin 12). When both inputs to (U38) (pins 1 and 2) are low '0's' the output (U38 Pin 3) will be high '1' which will be fed into the output disable (OD) of Inverter/Buffer IC's (U6, U9, and U12).

When the output of (U38 Pin 3) is low '0' the Acutal Position BCD signal is fed thru the Inverter/Buffer IC's to the LED drivers.

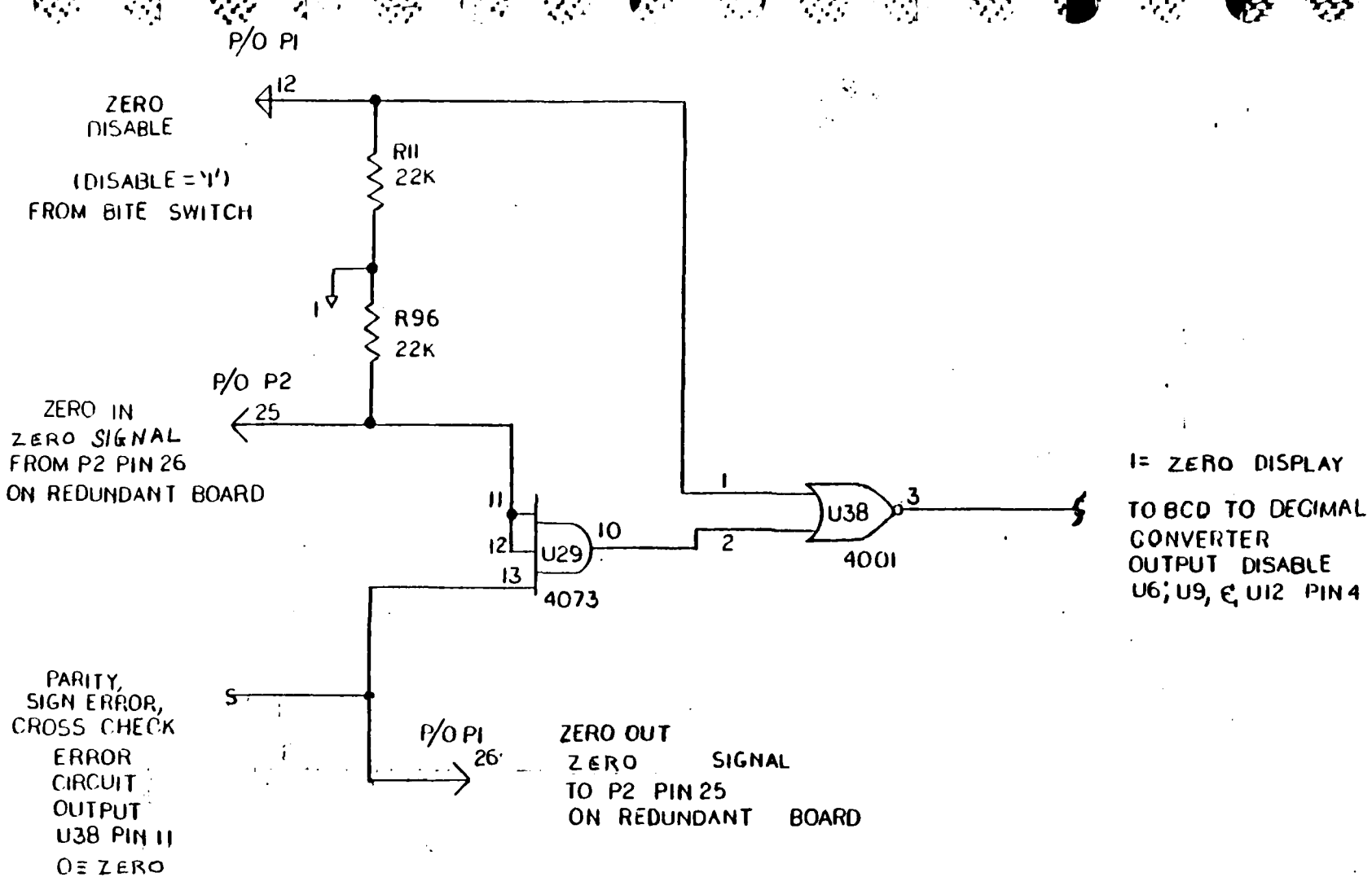


FIGURE 3 ZEROING CIRCUIT

69 (REV A)

NAEC-ENG-91-7999

2. TEST REQUIREMENTS

a. The zeroing circuit is tested in this section. This test is a go no-go test. If any unusual indications are observed or the test criteria are not met then the card is considered defective.

b. Each of the inputs to the zeroing circuit will be activated to check the circuit. These inputs are:

(1) Parity error

(2) Sign error

(3) Crosscheck subtractor error

(4) Zero input

(5) Zero disable input

c. This section of the board is tested by observing the output LED's on the board and monitoring if they zero when the proper error is inputed and if the zero is disabled when the zero display line is actuated.

3. TEST EQUIPMENT AND POWER REQUIREMENTS

a. 15VDC power supply

b. 5VDC power supply

c. Digital Multimeter, Fluke 800A or equivalent

d. Circuit card test fixture

e. Assorted test leads.

4. PRELIMINARY TEST PROCEDURE

a. Connect the power plugs of the test equipment to a source of single phase, 60 Hz, 115 volt AC power.

b. Connect the DVM, +15 volt DC power supply, and +5 volt DC power supply to 110 to 125 volt AC power and turn on.

c. Adjust +15 volt and +5 volt power supplies to within + or 0.1 volt using DVM.

d. Place +15 volt and +5 volt power supply switches off.

e. Place counter/switch select switch (SW2) down to switch position.

f. Place encoder rotation correction factor switch (SW3) down to Channel A1 position.

g. Place decrease/increase/input/output switch (SW7) to down position for the decrease/increase signal from the main board output to the redundant board.

h. Place the PARITY LEAD switch (SW10) down to the low position.

i. Place the PARITY LAG switch (SW11) down to the low position.

j. Place the decrease signal input (SW8) down to low.

k. Place the increase signal input (SW9) down to low.

l. Place the zero signal switch (SW12) up to high for normal operation.

m. Place the zero DISABLE switch (SW13) down to low for normal zeroing operation.

5. FINAL TEST PROCEDURES

NOTE: Record test results on Data Sheet 8 (Appendix A).

a. Turn on +15 volt and +5 volt power supplies.

PARITY ERROR

b. Place the position input signal switch (SW18, 19, and 20) to 187.

c. Place the command input signal switch (SW21, 22, and 23) to 187.

d. Place the redundant board POS-CMD error (crosscheck) (SW24, 25, and 26) to 000.

e. Place the PARITY LEAD switch (SW10) up for high signal input.

f. Check that the test set-up zero light (DS5) is not lit.

g. Check that the LED readouts on the circuit board read 000.

h. Place the ZERO DISABLE switch (SW13) down to the low position for normal zeroing operation.

i. Check that the LED readouts on the circuit boardd readd 187.

j. Check that the test set-up ZERO light (DS5) is not lit.

k. Place the PARITY LEAD switch (SW10) down for low signal input.

l. Place the ZERO DISABLE switch (SW13) down to the low position for normal zeroing operation.

INPUT SIGN ERROR

m. Place the position input signal switch (SW18, 19, and 20) to 068.

n. Place the command input signal switch (SW21, 22, and 23) to 148.

o. Place the redundant board POS-CMD error switch (crosscheck) (SW24, 25, and 26) to 080.

p. Place the increase signal switch (SW9) to the up position for high input.

q. Check that the circuit board LED's read 068 and the test set-up ZERO light (DS5) is lit.

r. Place the increase signal switch (SW9) to the down position for low input.

s. Place the decrease signal switch (SW8) to the up position for high inpu..

t. Check that the test set-up ZERO light (DS5) is not lit.

u. Check that the LED readouts on the circuit board read 000.

v. Place ZERO DISABLE switch (SW13) up the zero disable position.

w. Check that the circuit board LED's read 068.

x. Check the test set-up ZERO light (DS5) is not lit.

y. Place the decrease signal switch (SW8) down to the low position.

z. Place the ZERO DISABLE switch (SW13) down to the normal position.

INPUT CROSSCHECK ERROR

aa. Place the position input signal switch (SW18, 19, and 20) to 128.

bb. Place the command input signal switch (SW21, 22, and 23) to 128.

cc. Place the redundant board POS-CMD error switch (crosscheck) (SW24, 25, and 26) to 000.

dd. Check that the circuit board LED's read 128 and the test set-up ZERO light (DS5) is not lit.

ee. Place the redundant board POS-CMD error switch (crosscheck) (SW24, 25, and 26) to 111.

ff. Check that the test set-up ZERO light (DS5) is not lit.

gg. Check that the LED readouts on the circuit board read 000.

hh. Place ZERO DISABLE switch (SW13) up to the ZERO disable position.

ii. Check that the circuit board LED's read 128.

jj. Check the test set-up. Zero light (DS5) is not lit.

kk. Place the redundant board POS-CMD error switch (crosscheck) (SW24, 25, and 26) to 000.

ll. Place ZERO DISABLE switch (SW13) down to the normal position.

ZERO SIGNAL FROM REDUNDANT BOARD

mm. Place the ZEROING signal switch (SW12) down to low for ZEROING condition.

nn. Check that the test set-up ZERO light (DS5) is lit.

oo. Check that the LED readouts on the circuit board read 000.

pp. Place the ZERO DISABLE switch (SW13) up to the ZERO DISABLE position.

qq. Check that the LED readouts on the circuit board read 128.

rr. Check that the test set-up ZERO light (DS5) is lit.

ss. Turn off +15 volt and +5 volt power supply.

tt. End of test. Proceed to Section I.

I. COINCIDENCE CIRCUIT

1. CIRCUIT DESCRIPTION

a. The coincidence circuit checks that the position setting is equal to the command setting so the system will not launch an aircraft while incorrectly set.

b. The three coincidence lines are the actual position inputs fed thru one section of the BCD Command Switch in the BCD Command Readout Station. If the command digit is the same as the position digit the 'high' line corresponding to that position is fed thru the coincidence section of the switch to the board. The three lines correspond to the units, tens, and hundreds of the position/command BCD data.

c. The coincidence circuit schematic is shown in Figure 32.

The command switch coincidence inputs (P2 Pins 24, 26, 28) and the 'P=C' input at (U50 PIN 3) determines when there is coincidence.

The three coincidence lines are transfered thru series resistors (R90, R92, and R94) and resistors (R91, R93, and R95) to limit current surges. Then it is subjected to protection diodes (CR66, CR 68 and CR70) and (CR65, CR67, and CR69) to limit current surges. The three inputs are then fed into AND gate (U29). When all three are high '1's' (coincidence) a high '1' signal is outputed at (U29 Pin 6). This high '1' signal is inputed into another AND gate (U29) along with the 'P=C' input. When both are high '1's the output at (U29 Pin 9) is high '1'. This output is inverted by (U28) to turn on 'COI' LED (DS3). This output is also inverted by another inverter (U28) to energize the board coincidence relay (K3).

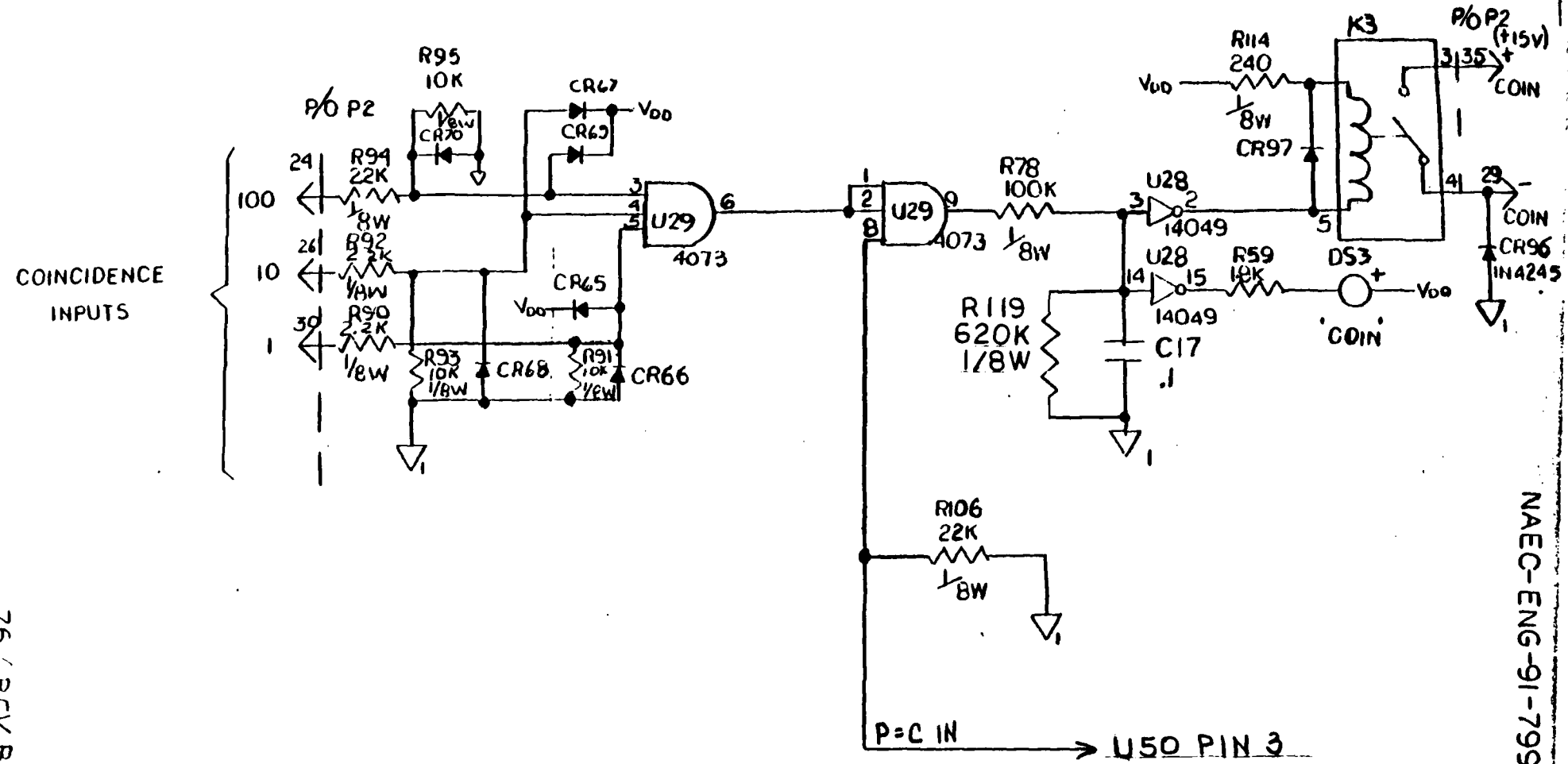


FIGURE 32 COINCIDENCE CIRCUITS

2. TEST REQUIRMENTS

a. The coincidence circuit is tested in this section. This test is a go no-go test. If any unusual indications are observed or the test criteria are not met then the card is considered defective.

b. The three conincidence line signals and the position equals command signal from the increase/decrease circuit are inputed to the section for this test.

c. The output of the conincidence circuit is checked by observing if the 'COI' LED is lit. The +15 volt signal is passed thru the board coincidence relay K3 when all input lines are energized. If any input line is deenergized the LED and the +15 volt signal go off.

3. TEST EQUIPMENT AND POWER REQUIREMENTS

a. 15VDC power supply

b. 5VDC power supply

c. Digital Multimeter, Fluke 800A or equivalent

d. Circuit card test fixture

e. Assorted test leads

4. PRELIMINARY TEST PROCEDURE

a. Connect the power plugs of the test equipment to a source of single phase, 60 Hz, 115 volt AC power.

b. Connect the DVM, +15 volt DC power supply, and +5 volt DC power supply to 110 to 125 volt AC power and turn on.

c. Adjust +15 volt and +5 volt power supplies to within + or - 0.1 volt using DVM.

d. Place +15 volt and +5 volt power supply switches off.

e. Place the 100 coincidence switch (SW14) up to the high position.

f. Place the 10 coincidence switch (SW15) up to the high position.

g. Place the 1 coincidence switch (SW16) up to the high position.

5. FINAL TEST PROCEDURES

NOTE: Record test results on Data Sheet 9 (Figure 23).

a. Turn on +15 volt and +5 volt power supply.

b. Check that the circuit board 'COI' LED (DS3) and the test set-up 'COINCIDENCE' light (DS6) are lit.

c. Place the PARITY LEAD switch (SW10) and PARITY LAG switch (SW11) to low positions and check the circuit board 'COI' LED (DS3) and the test set-up 'COINCIDENCE' light (DS6) for the proper response, as each coincidence switch is switched up and down.

d. Turn off +15 volt and +5 volt power supplies.

e. End of test. Proceed to Section J.

J. INTENSITY LIGHTING CIRCUIT

1. CIRCUIT DESCRIPTION

a. The intensity lighting circuit is used to help control the intensity of the lights in the command switch readouts of the BCD command readout station.

b. The schematic for the intensity lighting control circuit is shown in Figure 33.

The wiper of the intensity control pot on the BCD command readout station is fed into (P1 Pin 4). The output at (P1-5) tracks the input and is fed to the base of power transistor (Q1) 2N3712 inside the Electronics Enclosure Assy. The emitter output of (Q1) is fed to lamps L1, L2, and L3 of the command switch readout.

2. TEST REQUIREMENTS

a. The intensity lighting circuit is tested in this section. If any unusual indications are observed or the test criteria are not met then the card is considered defective.

b. A 0 to +14 volt DC signal is inputed for this test.

c. The output of the intensity lighting circuit should be the same as the input.

3. TEST EQUIPMENT AND POWER REQUIREMENTS

a. 15VDC power supply

b. 5VDC power supply

c. Digital Multimeter, Fluke 300A or equivalent

d. Circuit card test fixture

e. Assorted test leads

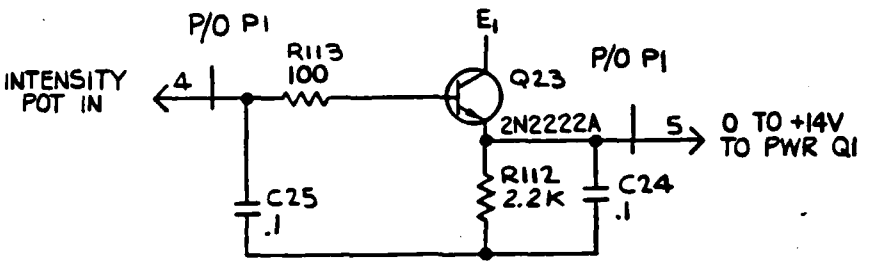


FIGURE 33 INTENSITY LIGHTING CONTROL CIRCUIT

4. PRELIMINARY TEST PROCEDURE

a. Connect the power plugs of the test equipment to a source of single phase, 60 Hz, 115 volt AC power.

b. Connect the DVM, and +15 volt DC power supply to 110 to 125 volt AC power and turn on.

c. Adjust +15 volt power supply to within + or -0.1 volt using DVM.

d. Place +15 volt and power supply switch off.

e. Preset INTENSITY potentiometer (R17) to full counterclockwise position.

f. Connect a DVM between + input (TP1) and ground (TP2) and another DVM between + output (TP3) and ground (TP4).

5. FINAL TEST PROCEDURES

NOTE: Record test results on Data Sheet 10 (Appendix A).

a. Turn on DVMs and +15 volt power supply.

b. Adjust INTENSITY potentiometer (R17) to obtain output voltages listed on data sheet to within $\pm$ 0.1 volt. Compare input voltage at (TP1) and (TP2) ground to output voltage at (TP3) and (TP4) ground. The difference should be no more than 1 volt DC.

c. Turn off + 15 volt power supply and DVM's.

d. Remove card from test fixture.

e. End of card test.

VI BURN-IN TEST

A. INTRODUCTION

B. TEST EQUIPMENT

C. TEST PROCEDURE

VI BURN-IN TEST

A. INTRODUCTION

After acceptance tests have been successfully completed and conformal coating has been applied, the circuit board must undergo burn-in tests as described in Section C.

VI BURN-IN TEST

B. TEST EQUIPMENT

1. Circuit board test fixture and remote cable for board receptacle.

2. Temperature chamber, range 0° F to 90° F.

3. Sequential timer

VI BURN-IN

C. TEST PROCEDURE

1. Place the circuit board into the temperature chamber and connect the circuit board to the test fixture cable.

2. Apply power and conduct normal circuit board tests as described in this report.

3. Set the Sequential timer for 60 minutes power on and 60 minutes power off cycles.

4. Set the temperature chamber to cycle for 2 hour periods, one hour at 0° F and the other at 90°F.

5. During the power on cycles, conduct a functional test at 4 points of the burn-in test at 6 hour intervals. If a failure occurs while testing, follow procedures described in paragraph 6 and 7.

6. At the conclusion of the test, perform a complete acceptance test procedure at room temperature. If a failure(s) occurs, troubleshoot and replace failed component(s).

7. Failed unit shall be subjected to burn-in test for a total of 24 hours failure free. Repeat paragraph 6.

8. See Figure 34 on page 86 for paragraph 1 through 7.

9. Use test data sheet number 1 page 99.

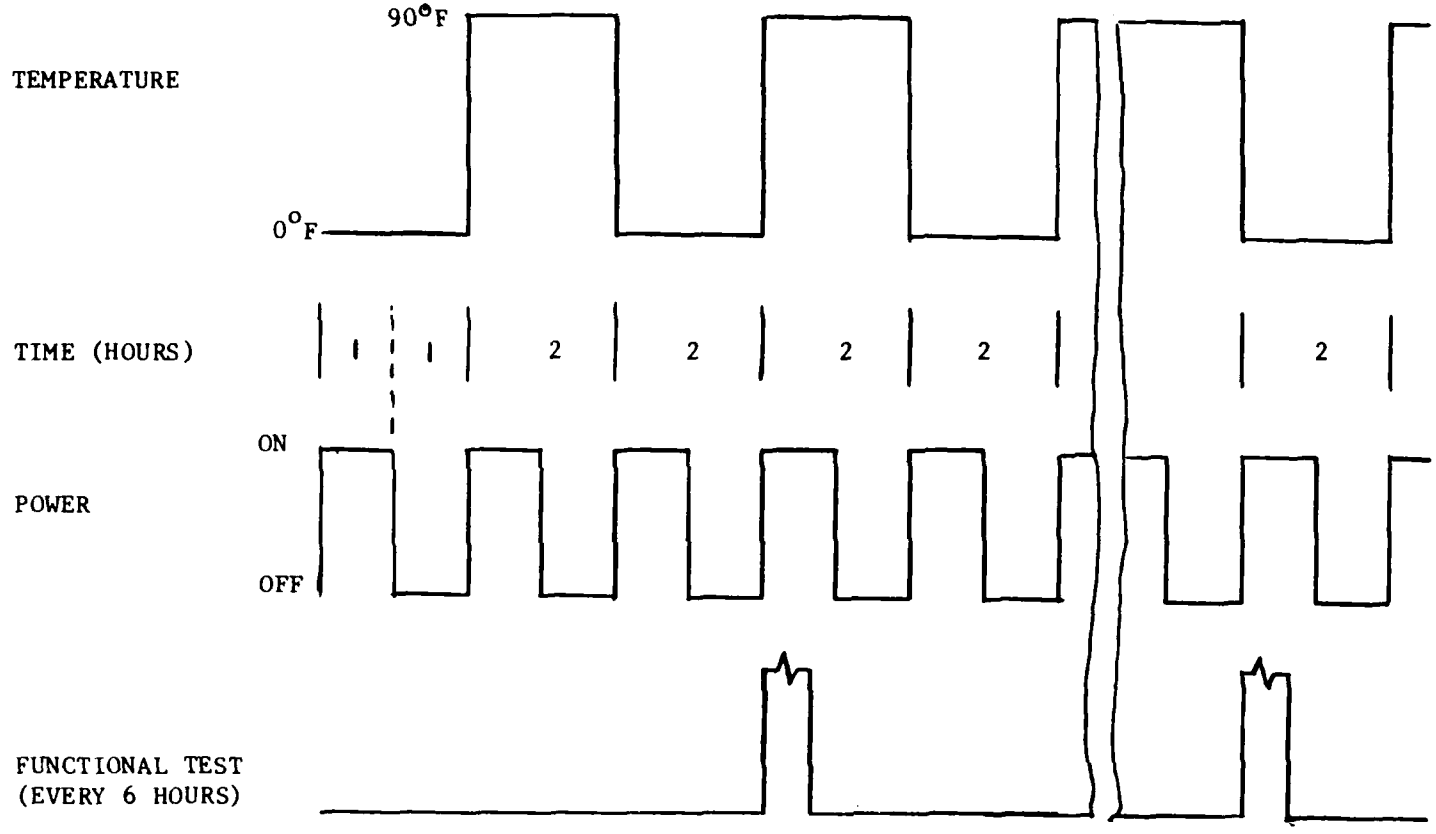


FIG. 34
BURN-IN CHART

Appendix A

Capacity Selector Valve
Electronics Enclosure Assembly
Controller Card Assembly
Test Data Sheets

TEST DATA SHEET #1	SECTION: VA
TITLE: ENCODER INPUTS TO READOUTS AND READOUT ZEROING	PAR. 5
SERIAL NO.	DATE

REFERENCE: Test Procedure and Test Specification

STEP	FUNCTION	STATUS	ACCEPT	REJ
C	Led Readouts on Circuit Board	000		
D	Output Error Light on Test Fixture	OFF		
E	Led Readouts on Circuit Board	Count from 000 to 359		
K	Led Readouts on Circuit Board	359		
L	Output Error Light on Test Fixture	OFF		
N	Led Readouts on Circuit Board	Count from 359 to 000		

NOTES:

TEST ENGINEER	TEST TECHNICIAN	INSPECTOR

TEST DATA SHEET #2	SECTION: VB
TITLE: BCD SUBTRACTOR CIRCUIT	PAR. 5
SERIAL NO.	DATE

REFERENCE: Test Procedure and Test Specification

STEP	POS INPUT	CMD INPUT	POS-CMD READOUT W/± 2 COUNTS	ACCEPT	REJ
D	000	000	000		
	000	100	100		
	000	102	102		
	000	104	104		
	000	108	108		
	000	200	200		
	000	210	210		
	000	220	220		
	000	240	240		
	000	280	280		
	000	300	300		
	100	000	100		
	101	000	100		
	102	000	102		
	104	000	104		
	108	000	108		
	200	000	200		
	210	000	210		
	220	000	220		
	240	000	240		
	280	000	280		
	300	000	300		

NOTES:

TEST ENGINEER	TEST TECHNICIAN	INSPECTOR

TEST DATA SHEET #3	SECTION: VC
TITLE: DIRECTION LOGIC CIRCUIT	PAR. 5
SERIAL NO.	DATE

REFERENCE: Test Procedure and Test Specification

STEP	POS INPUT	CMD INPUT	POS-CMD READOUT	TEST FIXTURE		ACCEPT	REJ
				INC	DEC		
B	024	200	176	ON	OFF		
B	312	024	288	OFF	ON		
C	335	200	176	ON	OFF		
C	047	024	288	OFF	ON		

NOTES:

TEST ENGINEER	TEST TECHNICIAN	INSPECTOR

TEST DATA SHEET #4	SECTION: VD
TITLE: INCREASE/DECREASE CIRCUIT	PAR. 5
SERIAL NO.	DATE
REFERENCE: Test Procedure and Test Specifications	

STEP	FUNCTION	STATUS	ACCEPT	REJ
E	Circuit Board "INC" Led (DS4)	LIT		
F	Test Fixture "INC" Relay Input Light	LIT		
K	Circuit Board "DEC" Led (DS6)	LIT		
L	Test Fixture "DEC" Relay Input Light	LIT		

NOTES:

TEST
ENGINEER

TEST DATA SHEET #5	SECTION: VE
TITLE: CROSS CHECK SUBTRACTOR CIRCUIT	PAR. 5
SERIAL NO.	DATE

REFERENCE: Test Procedure and Test Specification

STEP	POS INPUT	CMD INPUT	CROSS CHECK INPUT	CKT BD LED "CHK"	TEST FIXTURE "FAULT"	ACCEPT	REJ
B	100	100	002	OFF	OFF		
C	100	100	004	ON	ON		
D	100	100	000	OFF	OFF		
EFG	100	102	002	OFF	OFF		
	100	104	004	OFF	OFF		
	100	108	008	OFF	OFF		
	100	110	010	OFF	OFF		
	100	120	020	OFF	OFF		
	100	130	030	OFF	OFF		
	100	140	040	OFF	OFF		
	100	150	050	OFF	OFF		
	100	160	060	OFF	OFF		
	100	170	070	OFF	OFF		
	100	180	080	OFF	OFF		
	100	190	090	OFF	OFF		
	100	200	100	OFF	OFF		
	000	200	200	OFF	OFF		
	000	300	300	OFF	OFF		
	000	300	302	OFF	OFF		
	000	300	304	ON	ON		

NOTES:

TEST ENGINEER	TEST TECHNICIAN	INSPECTOR

TEST DATA SHEET #6	SECTION: VF
TITLE: SIGN ERROR CIRCUIT	PAR. 5
SERIAL NO.	DATE

REFERENCE: Test Procedure and Test Specification

STEP	POS INPUT	CMD INPUT	TEST SWITCHES DEC SIG	TEST SWITCHES INC SIG	CKT BD "CHK" LED	TEST FIX "FAULT"	ACCEPT	REJ
E	128	246	HIGH	LOW	ON	ON		
J	248	120	LOW	HIGH	ON	ON		

NOTES:

TEST ENGINEER	TEST TECHNICIAN	INSPECTOR

TEST DATA SHEET #7	SECTION: VG
TITLE: PARITY ERROR CIRCUIT	PAR. 5
SERIAL NO.	DATE

REFERENCE: Test Procedure and Test Specification

STEP	POS	TEST FIXTURE		CKT BD	TEST FIXTURE		ACCEPT	REJ
	INPUT	PAR LEAD	PAR LAG	LED "PAR"	"FAULT"	"ZERO"		
B	102	HIGH	LOW	OFF	ON	OFF		
	102	LOW	LOW	ON	ON	OFF		
	102	HIGH	HIGH	OFF	ON	OFF		
	102	LOW	HIGH	ON	ON	OFF		
	000	HIGH	LOW	ON	ON	OFF		
	000	LOW	LOW	OFF	OFF	ON		

NOTES:

TEST ENGINEER	TEST TECHNICIAN	INSPECTOR

TEST DATA SHEET #8	SECTION: VH
TITLE: ZEROING CIRCUIT	PAR. 5
SERIAL NO.	DATE

REFERENCE: Test Procedure and Test Specification

STEP	FUNCTION	STATUS	ACCEPT	REJ
F	POS INPUT	187		
F	CMD INPUT	187		
F	CROSS CHECK	000		
F	PARITY LEAD	HIGH		
F	PARITY LAG	LOW		
F	ZERO DISABLE	LOW		
F	ZERO SIGNAL	HIGH		
F	DECREASE SIGNAL SWITCH	LOW		
F	INCREASE SINGAL SWITCH	LOW		
G	TEST FIXTURE "ZERO" LIGHT	ON		
G	CKT BD LED READOUTS	000		
I	ZERO DISABLE	HIGH		
J	CKT BD LED READOUTS	187		
J	TEST FIXTURE " ZERO" LIGHT	OFF		
Q	POS INPUT	068		
Q	CMD INPUT	148		
Q	CROSS CHECK	080		
Q	PARITY LEAD	LOW		
Q	ZERO DISABLE	LOW		
Q	INCREASE SIGNAL SWITCH	HIGH		
Q	CKT BD LED READOUTS	068		
Q	TEST FIXTURE "ZERO" LIGHT	OFF		
T	DECREASE SIGNAL SWITCH	HIGH		
T	INCREASE SIGNAL SWITCH	LOW		
T	TEST FIXTURE "ZERO" LIGHT	OFF		
U	CKT BD LED READOUTS	000		
W	ZERO DISABLE	HIGH		
W	CKT BD LED READOUTS	068		
X	TEST FIXTURE "ZERO" LIGHT	OFF		
DD	POS INPUT	128		
DD	CMD INPUT	128		
DD	CROSS CHECK	000		
DD	ZERO DISABLE	LOW		
DD	DECREASE SIGNAL SWITCH	LOW		
DD	CKT BD LED READOUTS	128		
DD	TEST FIXTURE "ZERO" LIGHT	ON		
FF	CROSS CHECK	111		

NOTES:

TEST ENGINEER	TEST TECHNICIAN	INSPECTOR

TEST DATA SHEET #8	SECTION: VH
TITLE: ZEROING CIRCUIT	PAR. 5
SERIAL NO.	DATE

REFERENCE: Test Procedure and Test Specification

STEP	FUNCTION	STATUS	ACCEPT	REJ
FF	TEST FIXTURE "ZERO" LIGHT	OFF		
GG	CKT BD LED READOUTS	000		
II	ZERO DISABLE	HIGH		
II	CKT BD LED READOUTS	128		
JJ	TEST FIXTURE "ZERO" LIGHT	OFF		
NN	CROSS CHECK	000		
NN	ZERO DISABLE	LOW		
NN	ZERO SIGNAL	LOW		
NN	TEST FIXTURE "ZERO" LIGHT	ON		
OO	CKT BD LED READOUTS	000		
QQ	ZERO DISABLE	HIGH		
QQ	CKT BD LED READOUTS	128		
RR	TEST FIXTURE "ZERO" LIGHTS	ON		

NOTES:

TEST ENGINEER	TEST TECHNICIAN	INSPECTOR

TEST DATA SHEET #9	SECTION: VI
TITLE: COINCIDENCE CIRCUIT	PAR. 5
SERIAL NO.	DATE

REFERENCE: Test Procedure and Test Specification

STEP	COINCIDENCE SWITCHES			CKT BD	TEST FIXTURE	ACCEPT	REJ
	100	10	1	"COI"	"COINCIDENCE"		
B	HIGH	HIGH	HIGH	ON	ON		
C	LOW	HIGH	HIGH	OFF	OFF		
C	HIGH	LOW	HIGH	OFF	OFF		
C	HIGH	HIGH	LOW	OFF	OFF		

NOTES:

TEST ENGINEER	TEST TECHNICIAN	INSPECTOR

TEST DATA SHEET #10	SECTION: VJ
TITLE: INTENSITY LIGHTING CIRCUIT	PAR. 5
SERIAL NO.	DATE

REFERENCE: Test Procedure and Test Specification

STEP	SPECIFICATION	MEASUREMENT	TEST INPUT	ACCEPT	REJ
B	TP3 & TP4 (GND) 0 VOLT + 1 VOLT	VOLTS	TP1 & TP2 (GND) POT IN 0 VOLTS		
B	1 VOLT ± 1 VOLT	VOLTS	POT IN 1 VOLT		
B	2 VOLTS ± 1 VOLT	VOLTS	POT IN 2 VOLTS		
B	4 VOLTS ± 1 VOLT	VOLTS	POT IN 4 VOLTS		
B	6 VOLTS ± 1 VOLT	VOLTS	POT IN 6 VOLTS		
B	8 VOLTS ± 1 VOLT	VOLTS	POT IN 8 VOLTS		
B	10 VOLTS ± 1 VOLT	VOLTS	POT IN 10 VOLTS		
B	11 VOLTS ± 1 VOLT	VOLTS	POT IN 11 VOLTS		
B	12 VOLTS ± 1 VOLT	VOLTS	POT IN 12 VOLTS		
B	13 VOLTS ± 1 VOLT	VOLTS	POT IN 13 VOLTS		
B	14 VOLTS ± 1 VOLT	VOLTS	POT IN 14 VOLTS		
D	END OF TEST				

NOTES:

TEST ENGINEER	TEST TECHNICIAN	INSPECTOR

TEST DATA SHEET #11	SECTION: VI
TITLE: BURN-IN	PAR.
SERIAL NO.	DATE

REFERENCE: Burn-In Test Procedure

STEP	FUNCTION TEST	REASON FOR REJ	ACCEPT	REJ
5.	1			
	2			
	3			
	4			

NOTES:

TEST ENGINEER	TEST TECHNICIAN	INSPECTOR

DISTRIBUTION LIST

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91233 (3)
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9113 (1)
9122 (1)
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REVISION LIST

REVISION	PAGES AFFECTED	DATE OF REVISION
A	Front Cover, 2, 3, 4, 7, 10, 11, 12, 15, 20, 21, 22, 24, 25, 25A, 26 to 31, 33, 34, 35, 37 to 40, 42 to 49, 52 to 58, 60 to 76, 78, 80, 81, 83, 84, 87, 88, 89, and 91 to 95.	6 March 1984
B	56, 65, 76	12 July 1984
C	1, 2, 3, 4, 10, 11, 12, 13, 14, 15, 17, 18, 19, 20, 20A, 21, 22, 23A, 24, 25, 38, 39, 40, 44, 48, 52, 53, 57, 58, 61, 66, 67, 71, 72, 73, 78, 82, 83, 84, 85, 86, 87, 88, 89, 90, 91, 92, 93, 94, 95, 96, 97, 98, 99	17 December 1986