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LEXINGTON, MASSACHUSETTS

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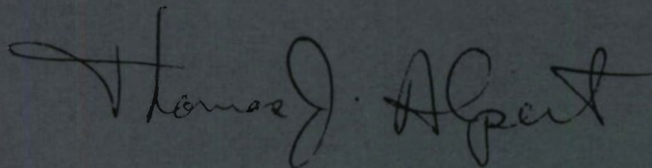

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SOLID STATE RESEARCH

QUARTERLY TECHNICAL REPORT

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ABSTRACT

This report covers in detail the solid state research work of the Solid State Division at Lincoln Laboratory for the period 1 November 1985 through 31 January 1986. The topics covered are Solid State Device Research, Quantum Electronics, Materials Research, Microelectronics, and Analog Device Technology. Funding is primarily provided by the Air Force, with additional support provided by the Army, DARPA, Navy, SDIO, NASA, and DOE.

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INTRODUCTION

1. SOLID STATE DEVICE RESEARCH

Two-dimensional arrays of 16 laser elements have been fabricated using the mass-transport process. Good uniformity, low threshold current (typically 11 to 14 mA) and high CW power (up to 0.27 W at 22°C) were obtained.

To assess the applicability of semiconductor diode lasers as components in analog, amplitude-modulated optical transmission systems, the levels of second- and third-order intermodulation products were measured. Initial results at about 500 MHz on a commercial AlGaAs device indicate approximately 45-dB suppression at an optical modulation depth (OMD) of 1.0, with the suppression increasing to approximately 70 dB for an OMD less than 0.1.

2. QUANTUM ELECTRONICS

Room-temperature CW operation of a $TiAl_2O_3$ laser has been demonstrated for the first time. The laser was excited using a multiline Ar-ion laser pump and emitted at 770 μm with a maximum output power of 1.6 W, and internal quantum efficiency of 64 $\pm$ 10 percent, and a round trip cavity loss of 2.4 $\pm$ 0.5 percent.

Laser action at 1.62 μm using a 1.475-μm laser pump has been observed for the first time in Er:YAG. Further experiments are being conducted to determine the laser parameters, including threshold energy, and to improve laser operation.

3. MATERIALS RESEARCH

A new capping technique employing high-temperature NH_3 annealing has been developed to insure uniform wetting by the molten Si zone during zone-melting recrystallization of Si-on-insulator (SOI) films. By using this technique, recrystallized 1-μm-thick films have been obtained with large areas that are free of subboundaries, containing only threading dislocations at densities of less than 2×10^6 cm^{-2}.

Both n- and p-channel junction field-effect transistors (JFETs) have been fabricated in SOI films prepared by zone-melting recrystallization. These devices exhibit excellent resistance to total-dose radiation at levels up to 10^8 rad (Si), making complementary SOI/JFET technology a very promising candidate for ultra-hard integrated circuit applications.

Semi-insulating crystals of InP with resistivities of 1-3 $\times$ 10^6 Ωcm have been grown by the liquid-encapsulated Czochralski method from melts co-doped with Ti, a deep donor located 0.62 $\pm$ 0.02 eV below the conduction band, and shallow acceptors. This technique should make it possible to obtain crystals with resistivities of 10^7 to 10^8 Ωcm, which would be of interest for integrated circuit applications if their thermal stability is found to exceed that of Fe-doped semi-insulating InP.

4. MICROELECTRONICS

A CCD analog vector-matrix product device capable of performing 2.5 billion multiplications per second at a clock frequency of 10 MHz has been designed, fabricated, and tested. This circuit has been mask programmed to perform a 16-point discrete cosine transform, with the precision of the fixed-weight multipliers being within approximately one percent of their design values.

A GaAs monolithic Ku-band analog phase shifter with integrated planar varactor diodes has been fabricated. This device has achieved comparable phase shift, but with lower insertion loss at higher frequency than a previously reported analog phase shifter. Furthermore, this approach is extendable to millimeter-wave frequencies.

A focused beam of electrons can be used to alter logic function of fully fabricated CMOS digital systems by selectively charging floating-gate FET devices. An overlapping metal electrode structure has been found to be useful in reducing the parasitic effects in the floating-gate devices.

The microwave noise power of several double-barrier quantum well structures has been measured and found to be about a factor of two less than predicted by a full shot noise model. This is strong evidence for a built-in negative feedback mechanism due to the accumulation of charge in the well.

A low-threshold laser for use with optical interconnects has been fabricated and driven directly by a GaAs logic circuit at a clock rate of 1.3 GHz. A packaging technique is being developed for integrating these individual logic and laser chips into a single package by imbedding them in a potting material to form a large multichip.

The first demonstration of the imaging of a distributed millimeter-wave source using heterodyning techniques has been carried out with a two-dimensional array of planar detectors at 135 GHz. The array, consisting of five printed dipole antenna pairs integrated with Schottky diodes on top of a crystal quartz substrate, was placed in the focal plane of an f/0.8 offset paraboloid.

5. ANALOG DEVICE TECHNOLOGY

A revised design of the SAW/FET programmable transversal filter has been built and preliminary testing has been completed. The new design has a programmable bandwidth of 100 MHz and a demonstrated on/off ratio of 20 dB.

The use of associative-memory-based pattern-recognition techniques for detecting lines in an optical image has been studied by computer simulation, with the ultimate goal of implementing these techniques in silicon charge-coupled devices. At present, the associative memory has a somewhat higher probability of false detection than a conventional two-dimensional matched filter, but this problem can be reduced by optimizing the choice of the association matrix.

An 80-MHz-bandwidth chirp-transform adaptive-filter system has been developed that is capable of providing both spectral monitoring and the excision of multiple narrowband signals. In an arrangement using two identical subsystems to handle alternate 10-μs segments, spectral analysis is achieved with a multiply-convolve-(multiply) configuration in the forward section of each subsystem, spectral components are excised by subsequent time gating of the transformed signals, and, finally, inverse-transform sections recreate 12.5-μs-long segments of the filtered time-domain signal and combine them into a continuous signal by overlap summation of the two channels.

REPORTS ON SOLID STATE RESEARCH

1 November 1985 through 31 January 1986

PUBLISHED REPORTS

Journal Articles

JA No.			
5720	Enhanced Quantum Efficiency Internal Photoemission Detectors by Grating Coupling to Surface Plasma Waves	S.R.J. Brueck V. Diadiuk T. Jones W. Lenth	Appl. Phys. Lett. **46**, 915 (1985)
5736	Laser Remote Sensing of Atmospheric Ammonia Using a CO_2 LIDAR System	A.P. Force* D.K. Killinger W.E. DeFeo N. Menyuk	Appl. Opt. **24**, 2837 (1985)
5741	Laser Linewidth	A. Mooradian	Phys. Today **38**, 42 (1985), DTIC AD-A157970
5766	Room-Temperature Operation of GaAs/AlGaAs Diode Lasers Fabricated on a Monolithic GaAs/Si Substrate	T.H. Windhorn G.M. Metze	Appl. Phys. Lett. **47**, 1031 (1985), DTIC AD-A164116
5771	Superconductive Analog Signal Processing Devices	R.S. Withers	Superconductive Technology in Review, No. 85-2, 1 (1985)
5786	Photorefractive Effects in $LiNbO_3$ Channel Waveguides: Model and Experimental Verification	R.A. Becker R.C. Williamson	Appl. Phys. Lett. **47**, 1024 (1985)
5795	Linewidth Reduction of Semiconductor Diode Lasers	J. Harrison A. Mooradian	*Laser Spectroscopy VII*, T.W. Hansch and Y.R. Shen, Eds. (Springer-Verlag, New York, 1985), p. 354
5802	Spectroscopic and Laser Characteristics of $Ti:Al_2O_3$	P.F. Moulton	J. Opt. Soc. Am. B **3**, 125 (1986)

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Meeting Speeches

MS No.			
6647A	14-GHz Operation of Q-Switched Diode Lasers	D.Z. Tsang J.N. Walpole S.H. Groves Z.L. Liau	*Optical Technology for Microwave Applications II,* S-K. Yao, Ed., Proc. SPIE **545**, 14-17 (1985)
6776	Technique for Measuring Surface Diffusion by Laser-Beam-Localized Surface Photochemistry	H.J. Zeiger J.Y. Tsao D.J. Ehrlich	J. Vac. Sci. Technol. B **3**, 1436 (1985)
6800	Electronic Structure of Deep-Lying Sulfur Centers in Si	H.J. Zeiger W.H. Kleiner*	Materials Research Society Symposium Proc., Vol. 46T, San Francisco, California, 15-18 April 1985, pp. 519-524
6803	Integrated Optics Wavefront Measurement Sensor	R.H. Rediker T.A. Lind	*Adaptive Optics*, Proc. SPIE **551**, 113 (1985)
6818	High-Speed Lateral Photodetectors on Semi-insulating InGaAs and InP	V. Diadiuk S.H. Groves	*Optical Technology for Microwave Applications II,* S-K. Yao, Ed., Proc. SPIE **545**, 18-22 (1985)
6890	Integrated-Optical Components for Fiber Gyroscopes	L.M. Johnson	*Fiber Optic and Laser Sensors III,* Proc. SPIE **566**, 96 (1985)
6901	Wideband Analog Programmable Transversal Filter	J.B. Green D.E. Oates D.L. Smythe	Digest of Papers, Government Microcircuit Applications Conference, Orlando, Florida, 5-7 November 1985, pp. 387-390
6902	Superconductive Dispersive Delay Lines for Wide-Bandwidth Analog Signal Processing	J.B. Green R.S. Withers A.C. Anderson	Digest of Papers, Government Microcircuit Applications Conference, Orlando, Florida, 5-7 November 1985, pp. 287-290

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MS No.			
6905	Chaotic Pulsation of Semiconductor Lasers with a Proton-Bombarded Segment	M. Kuznetsov* D.Z. Tsang J.N. Walpole Z.L. Liau	Proc. International Meeting on Instabilities and Dynamic of Lasers and Nonlinear Optical Systems, Rochester, New York, 18-21 June 1985
6921	Methods of Characterizing Photorefractive Susceptibility of $LiNbO_3$ Waveguides	R.A. Becker	*Integrated Optical Circuit Engineering II*, S. Sriram, Ed., Proc. SPIE **578**, 12-18 (1985), DTIC AD-A164077
6928	Integrated-Optical Components for Fiber Sensors	L.M. Johnson	*Integrated Optical Circuit Engineering II*, S. Sriram, Ed., Proc. SPIE **578**, 233-235 (1985)
7008	Picosecond Photodetectors Fabricated in GaAs Layers Grown on Silicon and Silicon-on-Sapphire Substrates	G.W. Turner G.M. Metze V. Diadiuk B-Y. Tsaur H.Q. Le	1985 International Electron Devices Meeting, Technical Digest, Washington, D.C., 1-4 December 1985, pp. 468-470
7047	Monolithic Integration of Si MOSFETs and GaAs MESFETs	H.K. Choi G.W. Turner B-Y. Tsaur	1985 International Electron Devices Meeting, Technical Digest, Washington, D.C., 1-4 December 1985, pp. 766-767

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UNPUBLISHED REPORTS

Journal Articles

JA No.			
5505A	Limitations on Power Transfer Efficiency of Three-Guide Optical Couplers	J.P. Donnelly	Accepted by IEEE J. Quantum Electron.
5739	An Investigation of the Co:MgF_2 Laser System	P.F. Moulton	Accepted by IEEE J. Quantum Electron.

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JA No.			
5827	Monolithic Integration of Si MOSFETs and GaAs MESFETs	H.K. Choi G.W. Turner B-Y. Tsaur	Accepted by Electron Device Lett.
5830	Electron-Pumped High Efficiency Semiconductor Laser	V. Daneu D. DeGloria A. Sanchez F. F-K. Tong R. Osgood	Accepted by Appl. Phys. Lett.
5841	Thoughts on the Junction Laser: The Past and the Future	R.H. Rediker	Accepted by MITA Press (Japan)

Meeting Speeches*

MS No.			
6683A	Mass-Transported GaInAsP/InP Buried-Heterostructure Lasers	Z.L. Liau D.C. Flanders J.N. Walpole D.Z. Tsang N.L. DeMeo	1985 N.E. Assoc. Chinese Professionals Tech. and Science Conference, Newton, Massachusetts, 29 November-1 December 1985
7004	Millimeter-Wave Monolithic Circuits for Receiver and Transmitter Applications	C.L. Chen A. Chu W.E. Courtney L.J. Mahoney	1985 N.E. Assoc. Chinese Professionals Tech. and Science Conference, Newton, Massachusetts, 29 November-1 December 1985
6911A	Electron Beam Pumping of Semiconductor Lasers	A. Sanchez V. Daneu D. DeGloria J.H. Peers F. F-K. Tong R.M. Osgood†	International Conference on Lasers '85, Las Vegas, Nevada, 27 November-6 December 1985
7005A	Novel GaInAsP/InP Laser Devices by Mass Transport	Z.L. Liau J.N. Walpole D.C. Flanders D.Z. Tsang	International Conference on Lasers '85, Las Vegas, Nevada, 27 November-6 December 1985

* Titles of Meeting Speeches are listed for information only. No copies are available for distribution.

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MS No.			
6935	AlGaAs Optoelectronic Devices on Monolithic GaAs/Si Substrates	T.H. Windhorn G.M. Metze	Conference on Fiber Optic Sources and Detectors, Part of Second Intern. Tech. Symp. on Optical and Electro-optical Applied Science and Engineering, Cannes, France, 25-29 November 1985
6971	Transient Transport Studies on Ion Implanted Polymers	B. Wasserman* M.S. Dresselhaus* M. Wolf* J.D. Woodhouse G.E. Wnek	1985 Fall Meeting of the Materials Research Society, Boston, Massachusetts, 1-6 December 1985
6978	Laser-Induced Submicrometer Etching of II-VI Compounds	C. Arnone M. Rothschild D.J. Ehrlich	
6979	New Reactions for the Laser Deposition of W/Si Discretionary Interconnects	J.G. Black D.J. Ehrlich J.H.C. Sedlacek	
7015	Capping Techniques for Zone-Melting-Recrystallized Si-on-Insulator Films	C.K. Chen L. Pfeiffer* K.W. West* M.W. Geis S. Darack* G. Achaibar* R.W. Mountain B-Y. Tsaur	
7019	Assessment of Si-on-Insulator Technologies for VLSI	B-Y. Tsaur	
7086	Characterization and Reduction of Defects in Zone-Melted Recrystallized Si Films	M.W. Geis C.K. Chen H.I. Smith* P.M. Nitishin B-Y. Tsaur R.W. Mountain	

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MS No.			
6984	Balanced Monolithic Mixer for Use at 44 GHz	B.J. Clifton R.W. Chick	Tenth International Conference on Infrared and Millimeter Waves, Orlando, Florida, 9-13 December 1985
6995	Diode-Laser Infrared Heterodyne Radiometer at 28 μm	D.L. Spears R.E. Reeder	
7001	Planar Dipole-Fed Mixer Arrays for Imaging at Millimeter and Submillimeter Wavelengths	J.A. Taylor T.C.L.G. Sollner C.D. Parker J.A. Calviello*	
7021	Linewidth Reduction of Semiconductor Diode Lasers	J. Harrison A. Mooradian	First International Laser Science Conference, Dallas, Texas, 18-22 November 1985
7022	Laser Remote Sensing of the Atmosphere	D.K. Killinger N. Menyuk	
7076	Picosecond Carrier Density and Light Output Dynamics of Modulated Diode Lasers	B.C. Johnson A. Mooradian	EECS/RLE Seminar Series on Optics and Quantum Electronics, Massachusetts Institute of Technology, Cambridge, Massachusetts, 20 November 1985
7079	New Tricks with Optical Waveguides	L.M. Johnson	Modern Optics and Spectroscopy Seminar, Massachusetts Institute of Technology, Cambridge, Massachusetts, 19 November 1985
7120	Associative Memories, Neural Networks, and the Hopfield Model	J.P. Sage	Seminar, Raytheon Research Divison, Lexington, Massachusetts, 29 January 1986
7122	Optical Waveguide Devices	L.M. Johnson	Seminar, Department of Electrical and Computer Engineering, University of Massachusetts, Amherst, Massachusetts, 21 January 1986

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MICROELECTRONICS

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1. SOLID STATE DEVICE RESEARCH

1.1 MONOLITHIC TWO-DIMENSIONAL ARRAYS OF HIGH-POWER GaInAsP/InP SURFACE-EMITTING DIODE LASERS

Diode lasers fabricated in a surface-emitting geometry[1-4] allow construction of two-dimensional laser arrays. However, until now the only two-dimensional array reported[5] consisted of three operating elements fabricated with vertical cavities, which produced a total of 1 mW at 77 K. Here we report good uniformity and high performance in a 16-element (4 $\times$ 4), horizontal-cavity InGaAsP diode laser array operating at room temperature with a total CW output power of 270 mW at 1.3 μm.

Selective chemical etching and mass transport were used to form the buried heterostructure (BH) cavities, as well as the cavity mirrors and integrated 45° beam deflectors which deflect the laser outputs perpendicular to the wafer surface. This fabrication was essentially the same as that previously described for individual surface-emitting lasers[4], except that p-type substrates were used for the LPE growth of the double heterostructure wafer rather than n-type substrates. The BH lasers were 150 μm in length with active regions approximately 2-μm wide by 0.2-μm thick. Oxide insulation and metallization, as previously described, were used. The mirrors at one of the ends of the laser cavities were metallized so that all the light was emitted from the beam-deflector ends of the cavities. The metallization was patterned so that each element of the array could be individually electrically contacted by wires bonded to pads at the periphery of the array.

A double-exposure photograph of an array taken with an infrared image converter is shown in Figure 1-1. The laser emission patterns at the beam deflectors are superimposed on another exposure of the illuminated surface of the array. The wire bonds mentioned above can be seen at the edges. The spacing between each emitting element is 254 μm in both directions. All 16 elements shown in Figure 1-1 were electrically connected in parallel with a total current of 500 mA and were operating above threshold.

Fourteen of the elements had threshold currents between 11 and 14 mA; the remaining two threshold currents were 22.5 and 26.5 mA. The individual CW output power vs current characteristics of the 16 devices are shown superimposed in Figure 1-2. These data were taken before the array was die bonded to a heat sink. After heat sinking, the lasers showed slightly better efficiencies at high bias currents. Threshold currents were slightly reduced as well, but by less than 0.5 mA. Figure 1-3 shows the output power vs current for the best single element of the array after heat sinking. The maximum quantum efficiency of this device is about 36 percent and occurs at about 60 mA of bias current. The maximum differential quantum efficiency is 50 percent for bias levels just above threshold.

Figure 1-4 shows the output power vs current of the entire array at room temperature with all elements connected in parallel. The 270 mW of power measured at 1 A corresponds to an average power density of 26 W/cm^2 and an overall quantum efficiency of 29 percent. The power efficiency is only 11 percent, however, due to poor ohmic contact to the p-substrate. Recent

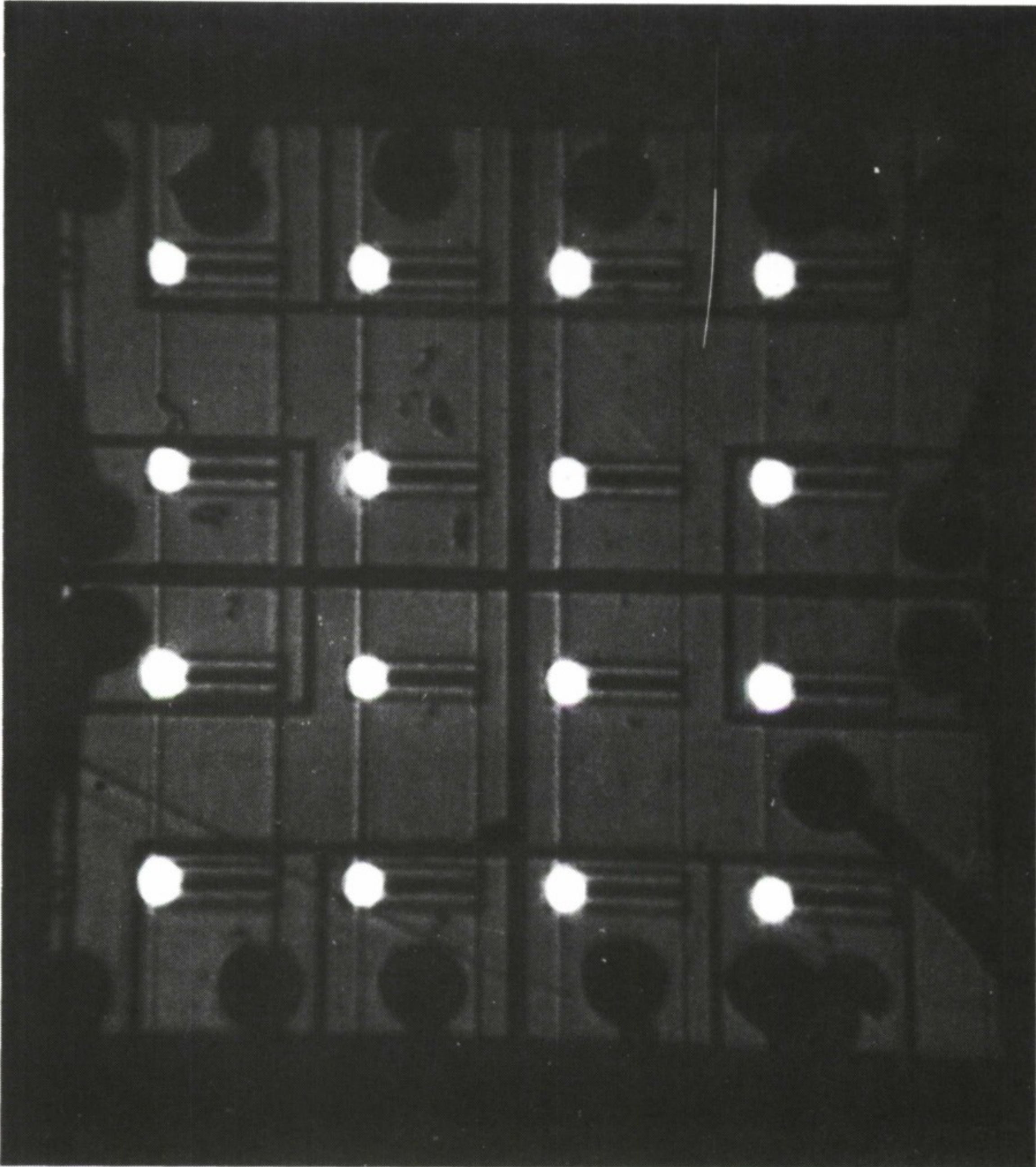

Figure 1-1. Infrared micrograph of 4×4 array of surface-emitting diode lasers during operation. Emitting elements are 254 μm apart in each direction.

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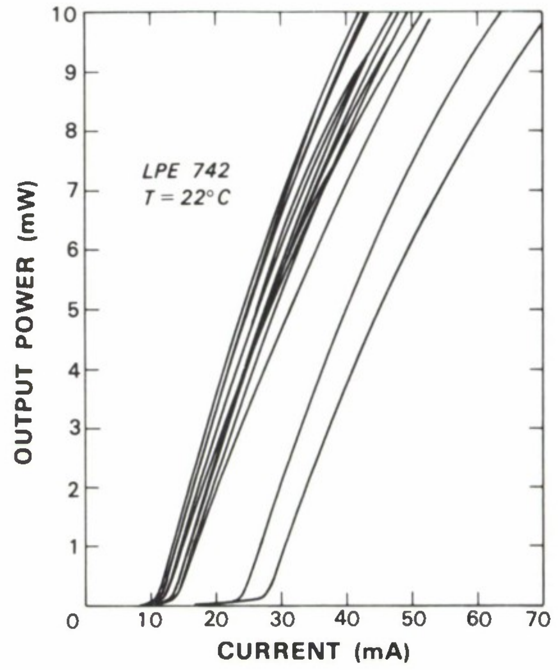

Figure 1-2. Room-temperature CW output power vs current for individual lasers of the 4 × 4 array before bonding to the heat sink.

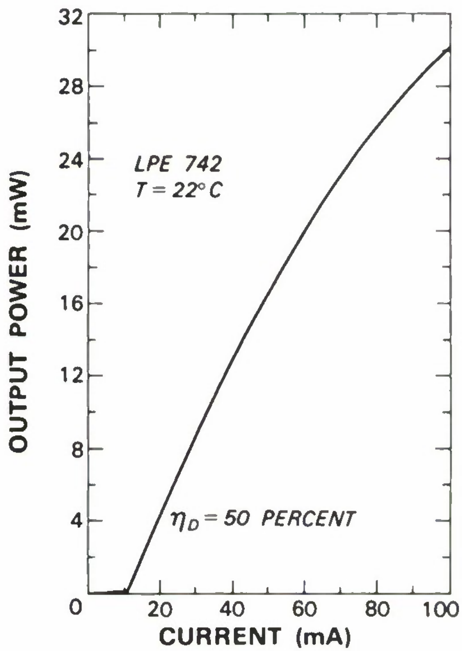

Figure 1-3. Room-temperature CW output power vs current for the best single element of the 4 × 4 array after bonding to the heat sink. The maximum differential quantum efficiency η_D is 50 percent.

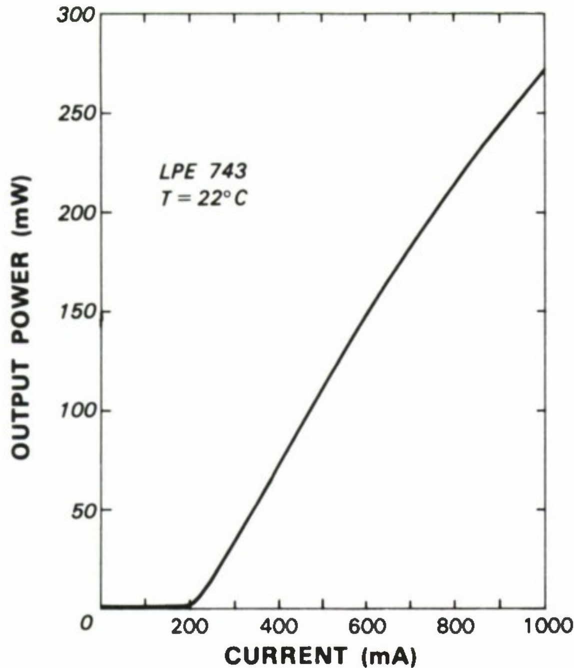

Figure 1-4. Room-temperature CW output power vs current for the 4 × 4 array with parallel electrical connections of the elements.

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improvements in contacting procedures should increase this power efficiency to about 22 percent. Even higher efficiencies are expected with further improvements in quantum efficiency and electrical contacts. The total power and the power density of the arrays will increase with larger arrays and with closer spacing of elements. Our calculations indicate that three to five times the present density of elements can be used without significant sacrifice in power efficiency.

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1.2 INTERMODULATION MEASUREMENTS OF SEMICONDUCTOR DIODE LASERS

Dynamic range is an important design parameter in many amplitude-modulated transmission systems. Typically the lower limit of the dynamic range is determined by the noise level; the upper limit is ultimately set by the power-handling capabilities of the system components, e.g., an amplifier's 1-dB compression level. However, nonlinearities in the input-to-output transfer functions of many system components usually establish a tighter upper limit for high-level signals. The linearity in the optical power output vs signal current of semiconductor diode lasers has improved considerably over the last several years. To assess the applicability of semiconductor diode lasers as a component in analog amplitude-modulated optical transmission systems, initial measurements of the linearity of a commercial AlGaAs diode laser have been made.

Since the tolerable degree of nonlinearity is usually too small to be measured directly, standard RF techniques[6] were employed. These techniques involve applying two equal amplitude RF

signals to the system under test at closely spaced frequencies f_1 and f_2 and measuring certain of the nonlinear mixing frequencies given by $nf_1 \pm mf_2$; m,n = 1,2,3.... Second-order intermodulation (IM) terms are given by n + m = 2, and the third-order terms by n + m = 3. In systems with more than an octave bandwidth, the second-order IM outputs, $f_1 \pm f_2$, although widely separated from the input frequency, can limit the maximum tolerable signal level. In systems with less than an octave bandwidth, these second-order outputs are usually filtered out, as are two of the third-order IM outputs, $2f_1 + f_2$ and $2f_2 + f_1$. The other two third-order IM outputs, $2f_1 - f_2$ and $2f_2 - f_1$, are close to the input frequencies and consequently are not amenable to filtering. Hence these terms will limit the maximum signal level and the dynamic range.

The diagram in Figure 1-5 outlines the experimental setup used to measure the second-order IM outputs at $f_1 \pm f_2$ and the third-order IM outputs at $2f_1 - f_2$ and $2f_2 - f_1$ produced by semiconductor diode lasers. In order to minimize the generation of IM products within the test set, it was necessary to operate with signal levels well within the linear range of test set components. Linearity was checked by breaking the circuit and substituting a 20-dB attenuator for the laser and photodetector. With careful choice of components, the system nonlinearities could be made negligible, even at an input diode laser drive power of –4 dBm. To achieve this, it was necessary to keep reflected signals at a minimum in order to avoid amplitude modulation and mixing associated with reflected power. All components in the IM test set were estimated to have a

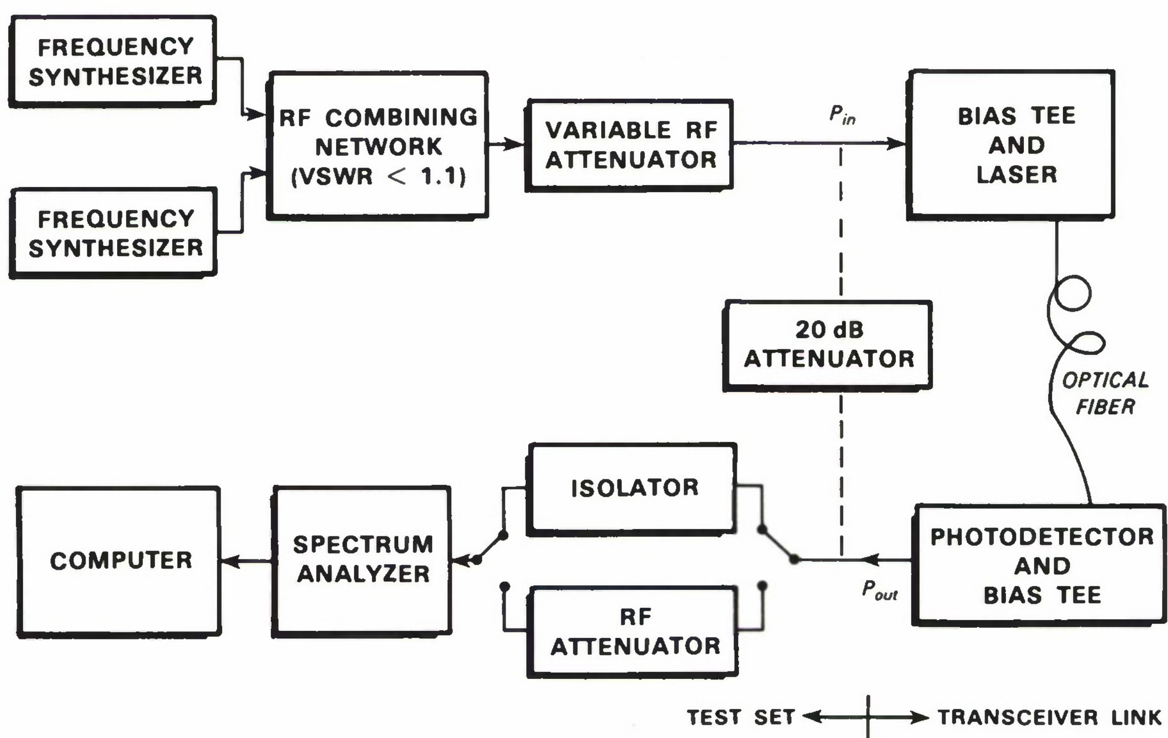

Figure 1-5. Simplified block diagram of experimental setup used to measure the intermodulation distortion of semiconductor lasers.

VSWR < 1.1, except the PIN photodiode used for the measurements described below, which had an impedance of about 500 Ω (VSWR = 10). However, placing an RF isolator between the photodiode and spectrum analyzer eliminated reflections due to this impedance mismatch.

Because of the strong dependence of the IM signal on the input signal, good instrument amplitude stability was also required, particularly in the signal sources. Any variation in the input signal is magnified by three for the case of the third-order IM signal. Accurate determination of the slope of the IM-power-vs-input-power curve gives rise to a stability requirement that is related to the RF input power range used for the particular IM measurement run. For a 10-dB range, an amplitude stability of ±0.5 dB is required to obtain a third-order IM slope accuracy of ±10 percent, whereas for a 40-dB range, a ±2 dB stability is needed.

The test set was used to evaluate a single-mode fiber-pigtailed AlGaAs diode laser (Ortel Model SL 620) with the optical power output vs current characteristic shown in Figure 1-6. The output of the laser was coupled via a graded-index, multimode fiber (50-μm core; 125-μm cladding) to a fiber-pigtailed AlGaAs PIN photodiode (Ortel Model PD050-PM). The IM measurements were carried out using modulation frequencies of 493 and 515 MHz, well below the laser's relaxation frequency of approximately 5 GHz. The results of two typical IM runs with the laser biased at an optical power P_0 of 1 mW are shown in Figure 1-7. The second-order IM data were taken without an RF isolator between the photodiode and the spectrum analyzer, whereas the isolator was used for the third-order data. The plots depict the average of the two fundamental, second-order and third-order output powers from the photodetector vs the average of the two fundamental RF powers at the laser input. The abscissa in Figure 1-7 is also labeled in terms of the optical modulation depth (OMD), which is defined[7] as the ratio of 1/2 of the peak-to-peak

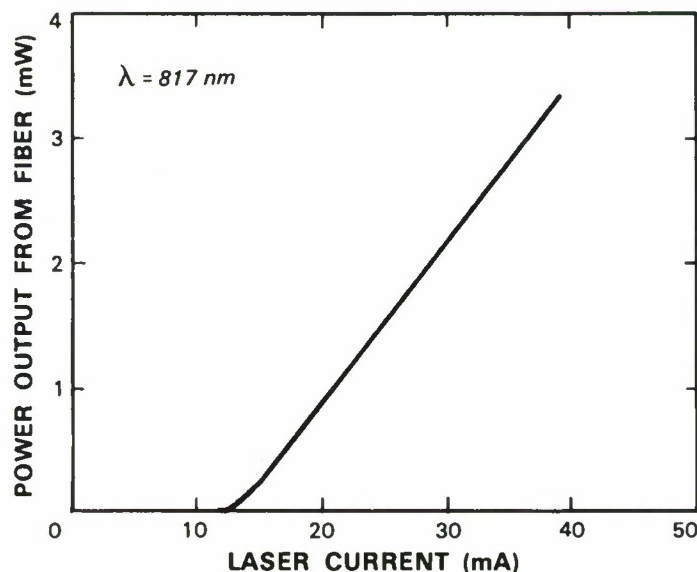

Figure 1-6. Optical power output vs AlGaAs diode laser current.

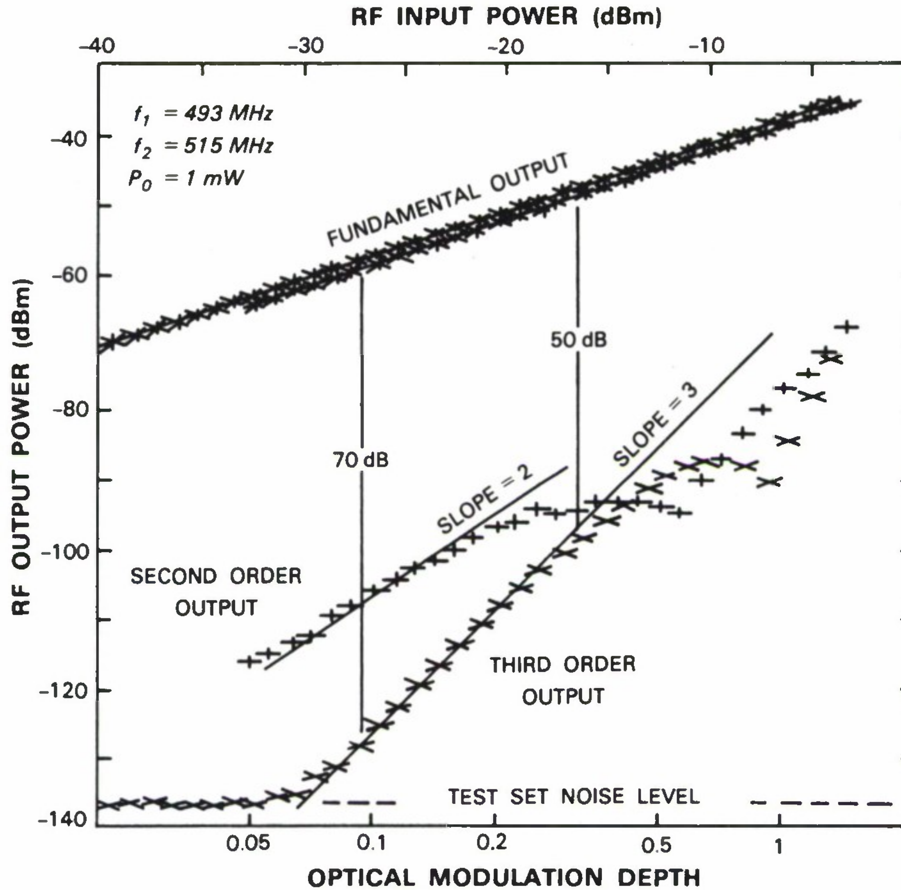

Figure 1-7. Pairwise average of the fundamental, second-order and third-order intermodulation RF output powers vs average RF input power and optical modulation depth for a AlGaAs laser biased at an optical output of 1 mW.

variation in the laser optical power to the DC optical power of the laser. For a diode laser with a linear optical power-current characteristic above threshold (Figure 1-6 shows that this is a reasonable approximation for the diode being evaluated), OMD is proportional to the square root of RF input power. For such diode lasers, unity OMD occurs when the RF input power is just sufficient to shut off the laser power during part of the waveform. Ideally, the slopes of the IM data vs average RF input power should be 1, 2, and 3 for the fundamental, second- and third-order IM signals, respectively.

The slope of the fundamental frequency data is unity to within ±0.3 percent up to an OMD of 100 percent. The insertion loss between the input to the laser and the detector output is about 32 dB. The majority of this loss can be accounted for by the 8.6 percent differential quantum efficiency of the laser (21-dB loss) and the specified ⩾40 percent quantum efficiency of the detector (⩽8-dB loss).

The second- and third-order data show the expected slopes of 2 and 3, respectively, for moderate RF modulation power. At higher RF input power the slopes decrease. The third-order

data show a strong dip when the fundamental RF output power is about –40 dBm and the optical modulation depth is very close to unity, whereas the second-order data show a dip at slightly lower OMD. These effects occurring at OMDs approaching unity are probably related to the curvature in the power-current characteristic of the laser near threshold (Figure 1-6). For OMDs greater than unity, a region where the laser is very nonlinear, both IM outputs rise rapidly with input power, particularly the third-order output.

Evidence that the anomalous behavior at high powers is probably not due to a photodiode nonlinearity is given in Figure 1-8, which shows the fundamental and third-order IM signals for an optical bias power of 2 mW. Here no strong dip is present at a fundamental output power level of –40 dBm. However, these data also show the falloff of the third-order signal from the ideal power slope of three as the OMD approaches unity. Insufficient RF input power from the test set precluded obtaining OMDs greater than unity at this higher optical bias level. Data at an

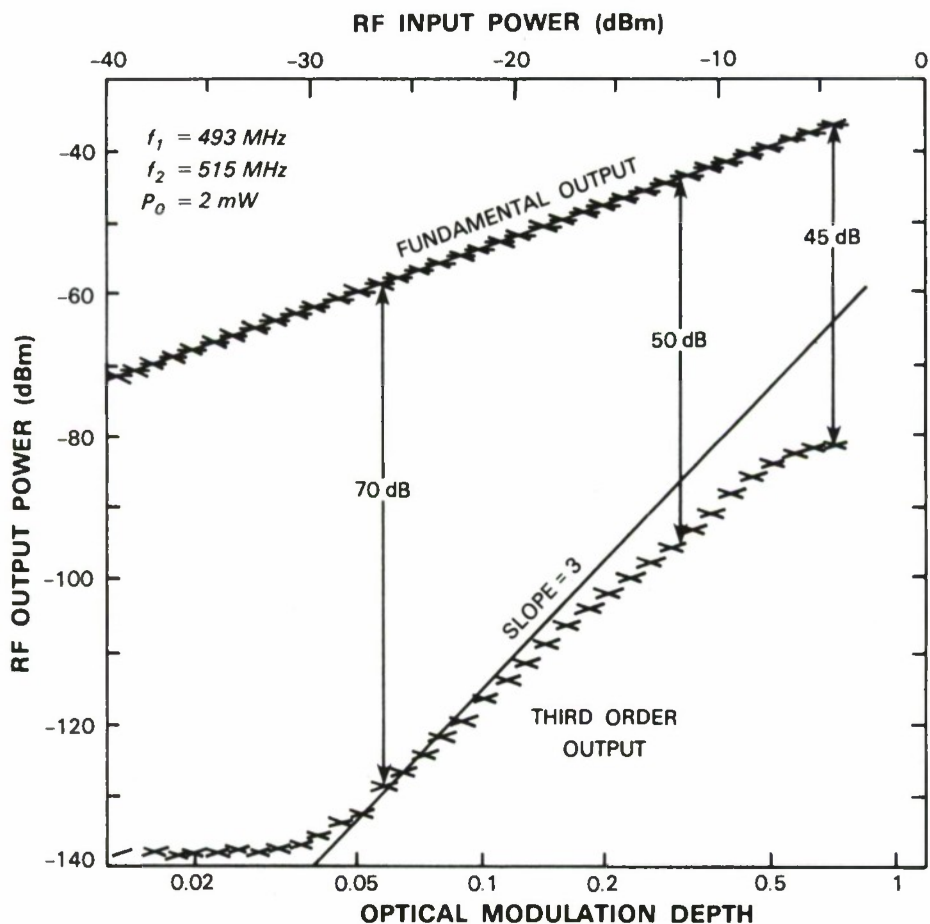

Figure 1-8. Pairwise average of the fundamental and third-order intermodulation RF output powers vs average RF input power and optical modulation depth for a AlGaAs laser biased at an optical output of 2 mW.

optical bias of 3 mW exhibited similar behavior: well-behaved (slope = 3) at low OMDs and a depression of the third-order IM signal as high OMDs were approached. At all three optical bias levels there appeared to be a 20-dB depression of the IM signal at an OMD = 1 from the extrapolated low-power slope value. Experiments are planned to further investigate these effects.

Reasonably high third-order IM suppression (ratio of fundamental power to IM power) was obtained for this transceiver link. As can be seen in Figures 1-7 and 1-8, at OMDs less than about 0.3, the third-order IM suppression was over 50 dB and increased with decreasing power in a well-behaved manner. At high OMDs (0.5 - 1.0) the suppression varied from 45 to 50 dB. These IM performance values are somewhat worse than previously reported[7] data (limited to OMDs > 0.4) for a similar laser. To put these IM suppression values in a system perspective, consider the noise level of a typical wideband transceiver system (which at 1 GHz is -75 dBm for a 3-dB noise figure) and note in Figures 1-7 and 1-8 that the IM powers would exceed this noise only for OMDs greater than unity.

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2. QUANTUM ELECTRONICS

2.1 ROOM-TEMPERATURE CW OPERATION OF A $Ti:Al_2O_3$ LASER

We report the first CW operation of a $Ti:Al_2O_3$ laser at room temperature. CW operation at liquid-nitrogen temperature has previously been reported.[1] However, at room temperature only quasi-CW operation was possible, using a low-duty-cycle chopper in the pump beam.[1,2] High-quality $Ti:Al_2O_3$ crystals with low parasitic absorption and scattering are required for CW laser operation at room temperature.

Crystals used in this work were grown by the vertical gradient-freeze technique.[3] The concentration of Ti^{3+} ions, which are responsible for laser action, was obtained from magnetization measurements. As shown in Figure 2-1, there is a linear relationship between the concentration of Ti^{3+} ions and the optical absorption coefficient for $\vec{E} \| \hat{c}$ at 490 nm, the peak of the laser pump band. This relationship yields an absolute value of the peak absorption cross section $\sigma = (9.3 \pm 1.0) \times 10^{-20}$ cm^2 at room temperature.

A laser rod of 1.8 cm length (ℓ) and 6 mm square cross section was fabricated. The ends of the rod were cut at the Brewster angle (60°) and polished optically flat. The crystallographic c

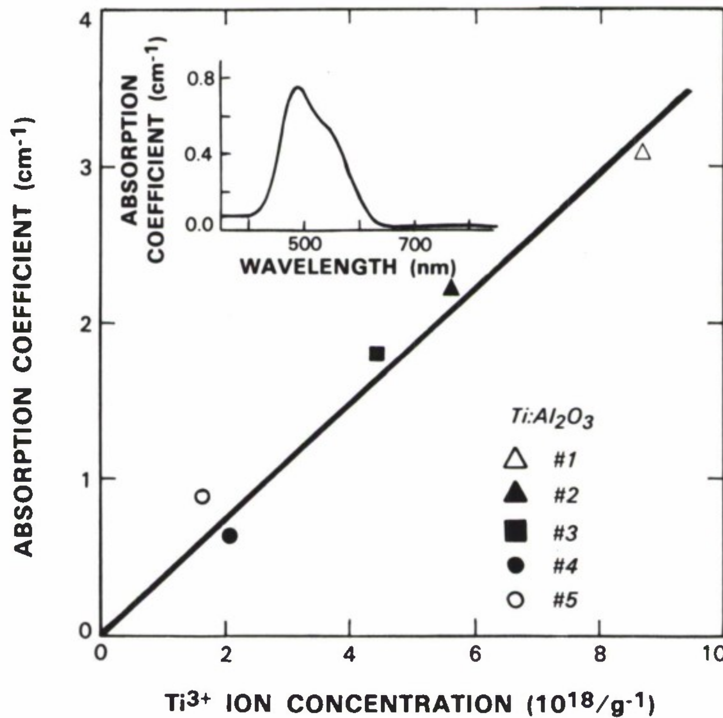

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Figure 2-1. Optical Absorption coefficient α (cm^{-1}) measured at room temperature in the $\vec{E} \| \hat{c}$ polarization at λ = 490 nm vs Ti^{3+} concentration for four as-grown samples and for a sample (#5) annealed at 1600° C in Ar gas containing ~ 100 ppm O_2. The inset shows a typical absorption spectrum for the 490-nm band.

axis was perpendicular to the axis of the rod and in the plane of incidence defined by the Brewster faces. The laser rod, supported by a water-cooled heat sink, was placed at the minimum waist of an astigmatically compensated three-mirror folded cavity.[4] The pump radiation from a multiline argon-ion laser was injected into the cavity through the folding mirror and focused into the laser rod by a lens placed outside the cavity. Figure 2-2 shows the laser output power at

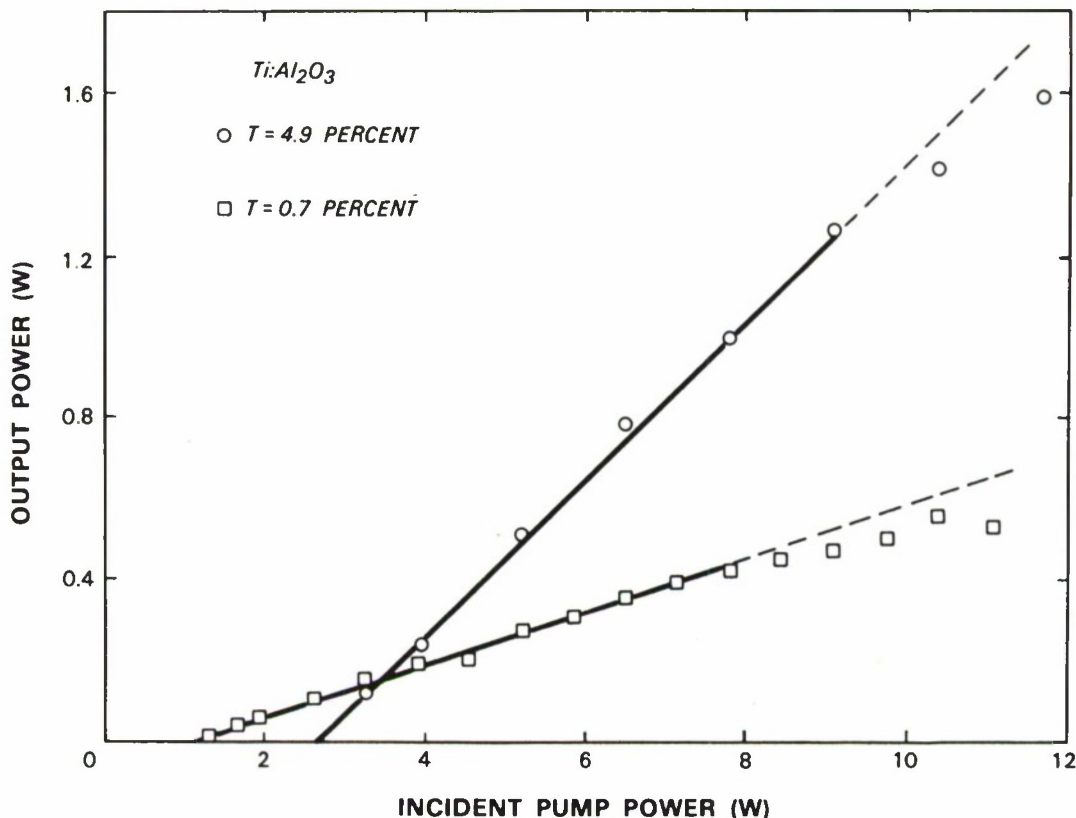

Figure 2-2. $Ti:Al_2O_3$ laser output vs incident pump power for two output couplers with transmittance of 0.7 percent and T = 4.9 percent and at the lasing wavelength of 770 nm.

770 nm vs the incident pump power, for two coupling mirrors with 0.7 percent and 4.9 percent transmittance. The maximum output power was 1.6 W. The slope efficiencies obtained with the two couplers were η = 6.5 percent and 19 percent, respectively. Using these values of η and the fraction of incident power absorbed (0.7), we obtain values for the internal quantum efficiency, η^i_Q = (64 ± 10) percent, and the round trip cavity loss, L = (2.4 ± 0.5 percent). This value of L implies an upper bound of $\alpha = L/(2\ell) = 0.007\ cm^{-1}$ on the absorption coefficient of $Ti:Al_2O_3$ at the laser wavelength using π polarization ($\vec{E}\|\hat{c}$). This value of α is 100 times smaller than the absorption coefficient for the pump radiation at 490 nm.

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2.2 Er:YAG LASER DEVELOPMENT

Lasing action at 1.62 μm in Er:YAG has been observed using a 1.475-μm optical pump. The laser was constructed using a 15-mm-long, 1 percent Er:YAG laser rod which was placed in a liquid nitrogen dewar. The dewar was centered in a vacuum-tight, concentric, 29-cm-long laser cavity. The input and output cavity mirrors were 25-cm radius of curvature dichroics with 85 percent transmission at 1.475 μm and 99.5 percent reflectivity at 1.62 μm. The Er:YAG crystal was collinearly pumped by the focused output from a 1.475-μm F-center laser, which in turn was pumped by 25 percent-duty-cycle chopped output of a 3-W, unpolarized, CW Nd:YAG laser; the peak output power of the F-center laser was approximately 100 mW. The beam waist size of the laser cavity was calculated to be 250 μm in radius, which is close to the measured 225-μm pump laser focal radius. Spectrometers and Ge detectors were used to monitor the absorption and fluorescence spectra from the Er:YAG laser crystal, both in the collinear direction and at 90 degrees.

The tunable F-center laser was scanned across a number of Er:YAG absorption lines near 1.475 μm and laser action near 1.62 μm was observed using several pump wavelengths. The threshold for laser action was approximately 60 mW, which is a factor of ten higher than predicted, indicating that unexpected loss mechanisms may be present. Work is underway to lower the threshold by using a much shorter cavity and tighter focusing, to use a Brewster angle cavity to reduce internal optical losses, and to increase the pump laser power. Spectroscopic measurements are being made to investigate energy transfer processes under high pump intensities and a careful determination is being made of other parameters related to laser operation.

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3. MATERIALS RESEARCH

3.1 NEW CAPPING TECHNIQUE FOR ZONE-MELTING RECRYSTALLIZATION OF Si-ON-INSULATOR FILMS

In the zone-melting recrystallization (ZMR) process for preparing silicon-on-insulator (SOI) films, a polycrystalline Si film on a SiO_2-coated Si substrate is recrystallized by the passage of a molten Si zone.[1] To obtain a device-quality SOI film, the poly-Si film must be encapsulated to insure that the molten Si zone will exhibit uniform wetting as it traverses the film. We have developed a new capping technique that has made it possible to achieve a major improvement in the effectiveness and reproductibility of ZMR performed by the graphite-strip-heater technique.

The basic structure of a wafer for ZMR processing is shown schematically in Figure 3-1. The SiO_2 capping layer by itself does not insure wetting by the molten Si. In previous studies we

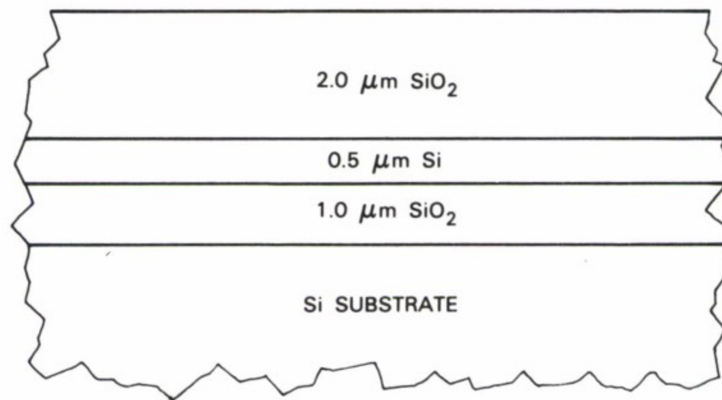

Figure 3-1. Schematic cross section of a typical SOI wafer.

have achieved considerable success by coating this layer with a Si-rich SiN_x film ~ 300 Å thick deposited by RF sputtering of a Si_3N_4 target.[1] Because of the difficulty in controlling the sputtering process, however, wetting is not reproducible, so that such effects as film agglomeration, void formation, and thickness variation occur too frequently for practical applications.

In a recent study[2] we obtained substantial evidence that SiN_x encapsulation promotes wetting because a trace amount of N diffuses through the capping SiO_2 layer and is incorporated at the CVD-SiO_2/poly-Si interface. In earlier work[3] on samples prepared by growing a film of thermal SiO_2 ~ 400 Å thick on a Si wafer, it had been shown that high-temperature annealing in NH_3 caused the introduction of N into the SiO_2/Si film, and that the N concentrations were higher at the upper and lower boundaries of the film than in the interior. These findings suggested that NH_3 annealing of SOI samples encapsulated with SiO_2 might cause incorporation of sufficient N at the upper SiO_2/Si interface to promote wetting by the molten Si during ZMR. We have found this to be the case. For samples with the geometry shown in Figure 3-1, high-temperature annealing at 1100°C for three hours in NH_3, oxidizing for ~ 20 minutes in O_2, and

annealing in NH_3 for an additional three hours consistently results in excellent wetting and <100> texture of the SOI film. Before each annealing step the system is purged with N_2 to prevent reaction between NH_3 and O_2. Annealing in NH_3 for the same total time without an intermediate oxidation step is less effective. Exposure to NH_3 produces a thin oxynitride film on the SiO_2 surface that apparently impedes incorporation of N into the SiO_2. Removal of this layer by oxidation permits incorporation to proceed more rapidly. With the NH_3-O_2-NH_3 procedure, ZMR reproducibly yields SOI films 0.3 to 0.5-μm thick that are extremely smooth, nearly free of voids, and uniform in thickness.

We have used Auger electron spectroscopy to investigate the N concentrations that are introduced by NH_3 annealing. From measurements on a control sample prepared by the deposition of Si_3N_4, we estimate that our detection limit for N at the SiO_2/Si interface is approximately half a monolayer. For a sample with the structure shown in Figure 3-1, after NH_3-O_2-NH_3 annealing sufficient to produce excellent wetting during ZMR, no N was detected by Auger analysis at the SiO_2/Si interface. Consistent with this result, from our earlier study[2] we believe that the amount of N present at the interface is approximately one-third of a monolayer.

The SOI films prepared in earlier ZMR experiments using SiN_x capping generally contain a high density of branched subgrain boundaries (subboundaries). In recent experiments using such capping, however, 1-μm SOI films scanned at 0.5 mm/s were found to contain large areas with unbranched subboundaries as well as some regions with only trails of dislocation clusters and diffuse bands of dislocations.[4] We have obtained still better results in similar experiments using a single eight-hour NH_3 anneal of the SOI wafer before ZMR, which introduces less N than the NH_3-O_2-NH_3 treatment described above. Figure 3-2 shows optical micrographs, taken after Secco etching for defect delineation, of a portion of a recrystallized 1-μm SOI film with a 2-μm underlying SiO_2 layer, scanned at 0.5 mm/s.[5] Very few subboundaries are observed, although small ridges or slight thickness variations occur in locations where subboundaries might be expected. The only defects observed over ~ 80 percent of a three-inch-diameter wafer (other than those associated with grain boundaries like the one seen at the left side of Figure 3-2) are trails of isolated dislocations, which have been shown by transmission electron microscopy to be threading dislocations running nearly normal to the surface. The density of these defects averaged over an area of several square centimeters is typically less than 2×10^6 cm^{-2}.

The critical influence of the experimental conditions on the quality of SOI films is illustrated by Figures 3-3 and 3-4. Figure 3-3(a) is an optical micrograph of a larger region of the recrystallized film shown in Figure 3-2. Except for several grain boundaries, which can be prevented by seeding to the underlying substrate,[6] isolated threading dislocations are the only defects present in the upper portion of the sample. The lower portion shown in Figure 3-3(a), which was recrystallized after an increase of ~ 5 percent in the power to the upper strip heater, contains a high density of subboundaries. Figures 3-3(b) and 3-3(c) are scanning electron micrographs of the two portions of the sample taken in the backscattering mode. A very distinct channeling pattern, indicating a high degree of crystalline perfection is observed in (b), while the pattern for (c) clearly shows discontinuities associated with the subboundaries.

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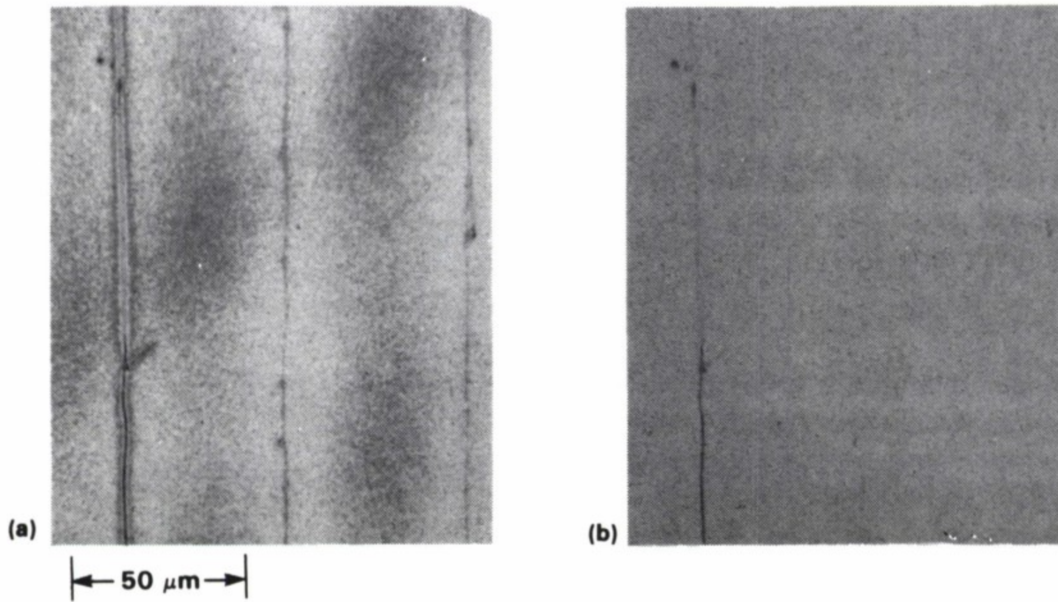

Figure 3-2. Two optical micrographs of the same area of a recrystallized SOI film after defect etching, illuminated by (a) monochromatic radiation and (b) white light. A grain boundary is seen on the left side, showing that the defect etch was effective.

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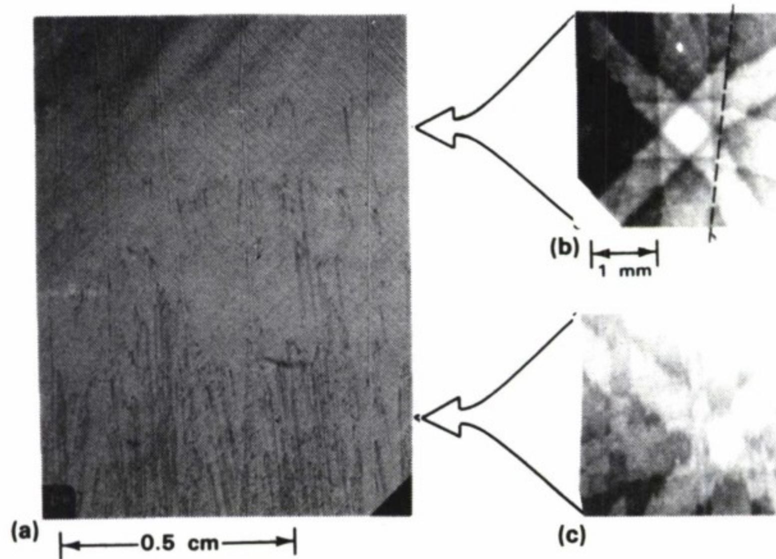

Figure 3-3. (a) Optical micrograph of the SOI film of Figure 3-2. The scan direction was from top to bottom. (b), (c) Electron channeling patterns obtained by operating a scanning electron microscope in the backscattering mode. The dashed line in (b) shows the location of a grain boundary.

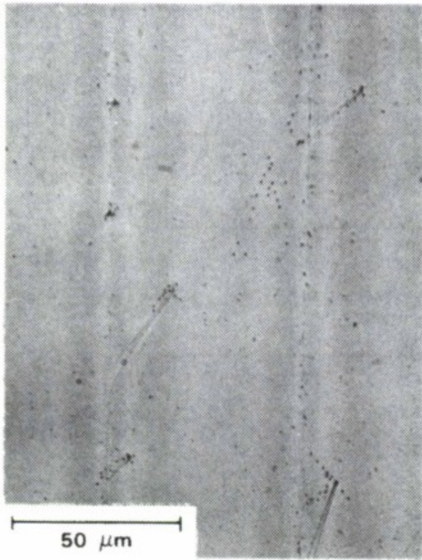

Figure 3-4. Optical micrograph showing the low defect density region of Figure 3-3(a) at higher magnification. The dislocation density is ~ 10^6 cm^{-2}.

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3.2 RADIATION-HARDENED Si-ON-INSULATOR JFETs

Devices fabricated in Si-on-insulator films are of great interest as potential elements for radiation-hardened integrated circuits. Because the active semiconductor volume is small, such SOI devices are less susceptible than bulk Si devices, both to logic upset and latchup induced by transient radiation and to single-event upset. However, SOI/CMOS devices can be sensitive to total-dose radiation, which tends to produce a shift in threshold voltage and an increase in leakage current because of charge trapping in the gate oxide and in the buried oxide underneath the device channel, respectively.[7]

In the JFET structure, the gate is formed by a p-n junction. Since there is no gate oxide, this structure should be inherently less sensitive to total-dose radiation than the MOS structure. Therefore excellent radiation resistance is expected for JFETs fabricated in the SOI films, provided that a negative substrate bias[7] is used to minimize the effects of charge trapping in the buried oxide layer. In addition, n- and p-channel JFETs can be combined to form complementary structures that offer the advantages of low-power operation, good noise immunity, and simple circuit design that have made CMOS circuits so useful. As the first step in developing a radiation-hardened complementary SOI/JFET technology, we have fabricated n- and p-channel JFETs in SOI films prepared by zone-melting recrystallization using the graphite-strip-heater technique.[8] These devices, the first reported SOI/JFETs, exhibit excellent resistance to total-dose radiation at levels up to 10^8 rad(Si).

The JFETs were fabricated in 0.5-μm-thick SOI films on 1-μm-thick SiO_2 layers on Si substrates. Figure 3-5 is a schematic diagram of the device structure. The channel depth was made small enough so that both n- and p-channel transistors operate as enhancement mode devices. The nominal gate width is 50 μm, the gate length is 4 μm, and the source-drain spacing is 8 μm.

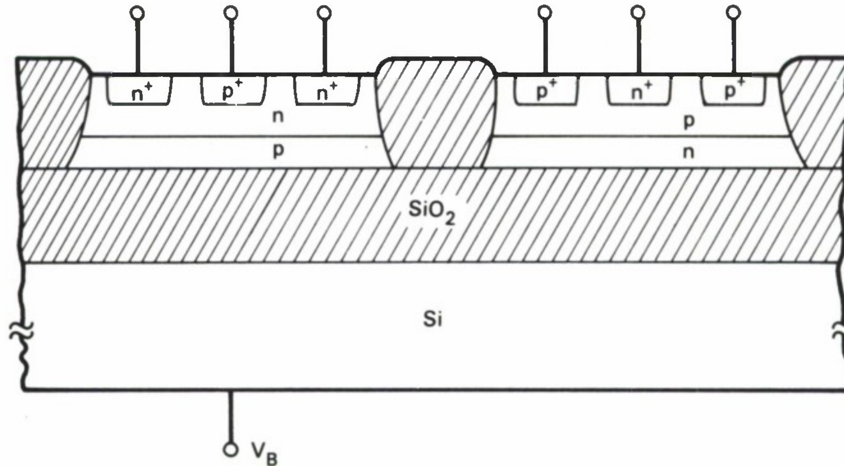

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Figure 3-5. Schematic device structure of SOI complementary JFETs.

The junction characteristics of the p^+/n and n^+/p gate diodes in the n- and p-channel JFETs have been determined by I-V measurements. In both cases the plots of log I vs V are linear, with slopes corresponding to diode ideality factors of 1.5 to 1.7. The threshold voltages for n- and p-channel devices are ~ + 0.6 and -0.6 V, respectively.

The JFETs were mounted in ceramic packages without covers and irradiated with doses of 1.5-MeV electrons corresponding to ionizing doses from 5×10^4 to 10^8 rad(Si). When no bias was applied to the substrate, a large shift in threshold voltage ($\Delta V_T > -0.2$ V) was observed for n-channel JFETs after irradiation to a dose of only 10^6 rad. This shift was greatly reduced by applying a substrate bias of -5 V. Figure 3-6 shows the subthreshold characteristics of n- and p-channel devices before irradiation and after exposures of 10^7 and 10^8 rad. The threshold voltage shift (ΔV_T) and drain leakage current (I_ℓ) remained small for both types of devices. In Figures 3-7 and 3-8, respectively, ΔV_T and I_ℓ are plotted as a function of ionizing dose for $V_B = -5$ V and three different pairs of V_D and V_G values during irradiation.

The qualitative features of Figures 3-7 and 3-8 can be explained as follows. The threshold voltage of a JFET is given by $V_T = V_b - V_p$, where V_b is the built-in voltage of the gate junction and V_p is the pinch-off voltage. Ionizing radiation causes a shift in V_T because it changes V_p. For n-channel devices, since exposure to such radiation results in the trapping of positive charge in the buried oxide layer, there is initially an increase in V_p and therefore a decrease in V_T. However, very high ionizing doses also produce defect states at the Si-oxide interface. In p-type Si, the interface states may be negatively charged,[9] in which case they compensate the positive charge trapped in the oxide. For very high doses, the concentration of these states becomes high enough to reverse the initial decrease in V_T and in some cases to increase V_T above its original value, thereby changing ΔV_T from negative to positive, as shown in Figure 3-7.

In the case of p-channel devices, trapping of radiation-induced positive charge in the buried oxide layer produces a decrease in the magnitude of V_p and a corresponding increase in the magnitude of V_T, so that the sign of ΔV_T due to charge trapping is negative. Any threshold shift due

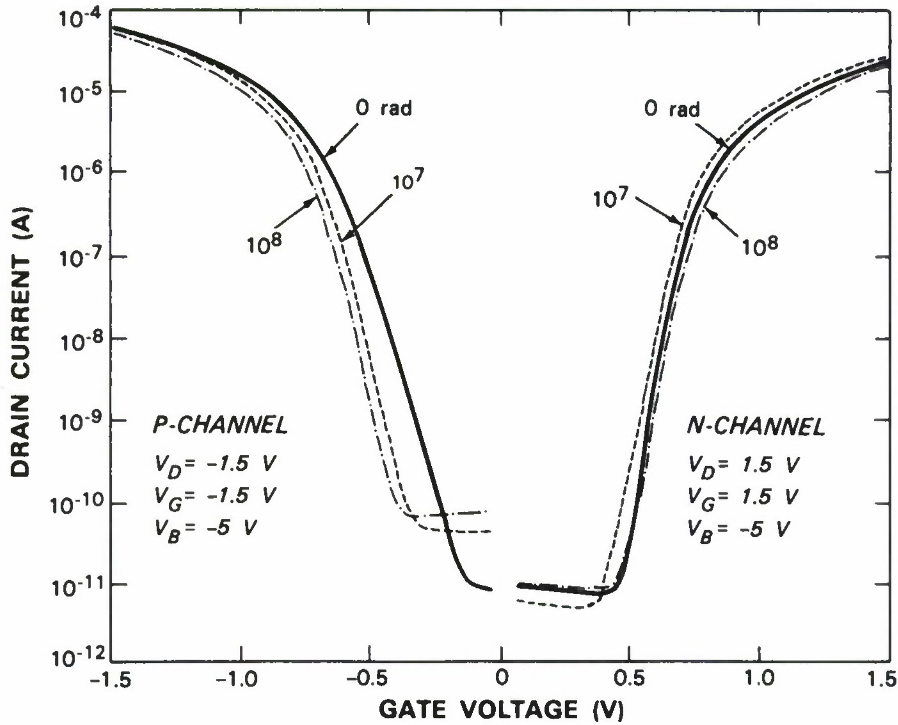

Figure 3-6. Subthreshold characteristics of n- and p-channel JFETs before and after irradiation. The bias voltages during irradiation are shown in the figure.

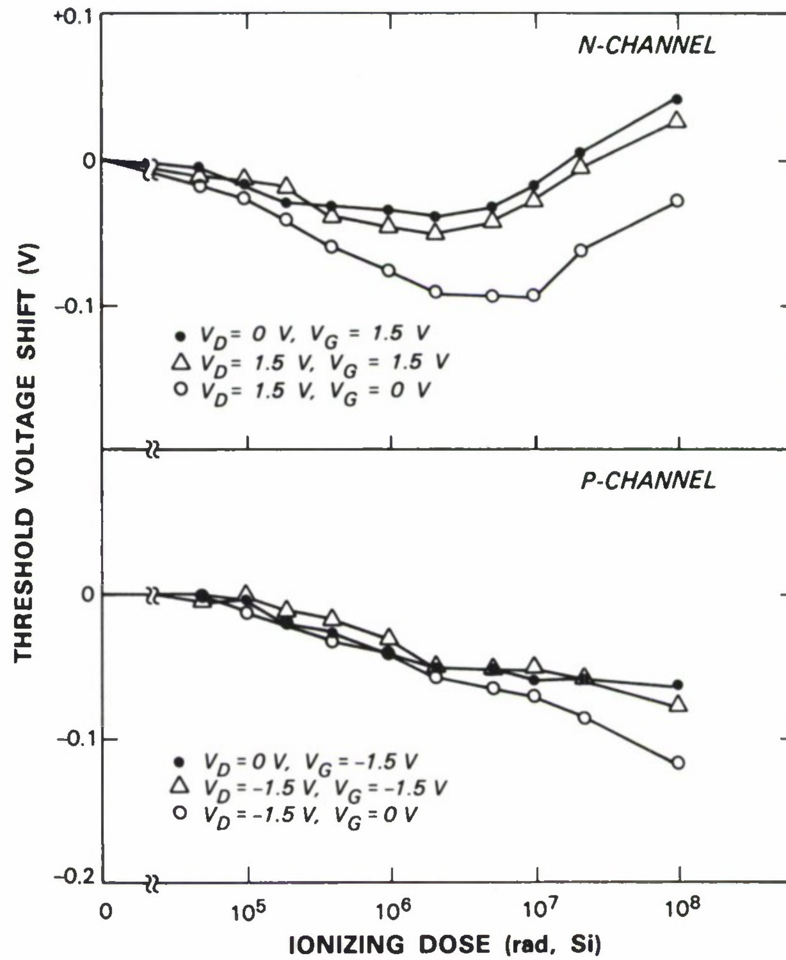

Figure 3-7. Threshold-voltage shifts of n- and p-channel JFETs as a junction of ionizing dose.

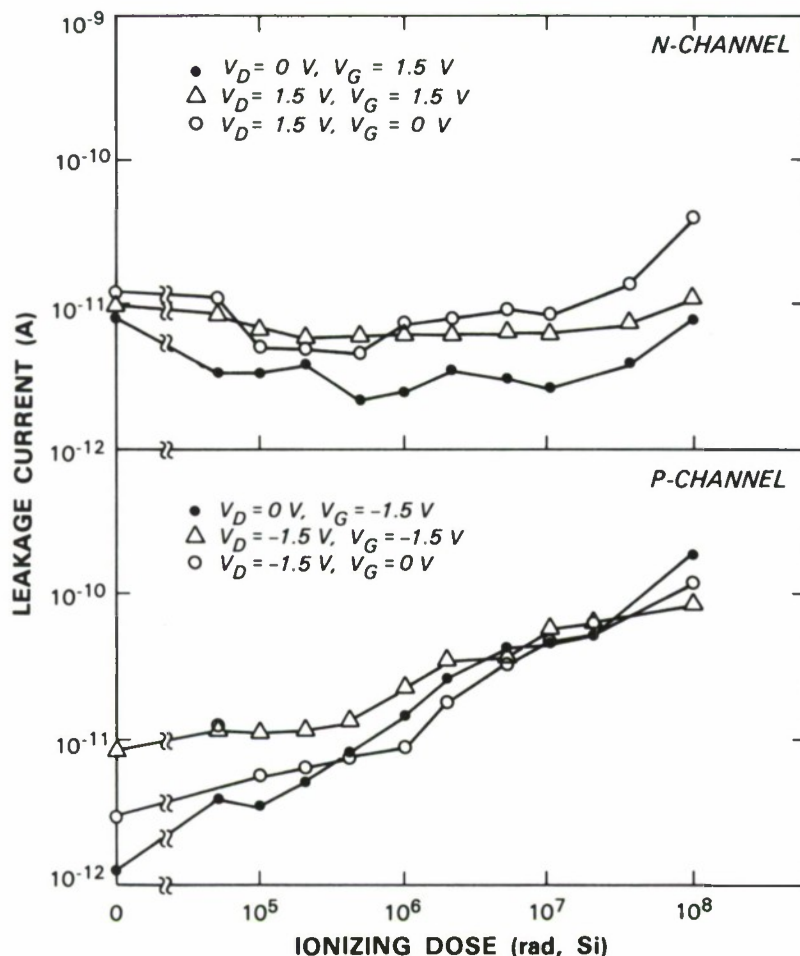

Figure 3-8. Leakage currents of n- and p-channel JFETs as a junction of ionizing dose.

to formation of interface states at high radiation doses is also negative, since in n-type Si such states are either neutral or positively charged.[9] Therefore the magnitude of ΔV_T increases monotonically with dose, as shown in Figure 3-7.

For JFETs incorporating an n/p or p/n junction below the channel, the drain leakage current is predominantly due to carrier generation in the space-charge region between the channel and the junction. Therefore I_ℓ varies with the width of this region. For n-channel devices, with increasing dose, this width initially decreases due to charge trapping in the buried oxide, but eventually increases due to interface-state generation. Consequently, I_ℓ ·st decreases and then increases, as shown in Figure 3-8. For p-channel devices, I_ℓ increases monotonically with dose, since both trapped charge and interface states increase the width of the space-charge region.

The generation of interface states by ionizing radiation frequently causes the degradation of surface carrier mobility and therefore leads to a reduction in the transconductance of MOS

devices. For the present JFET devices, in which the n/p or p/n junction confines carrier transport to the central region of the SOI film, interface-state generation does not have a strong effect on transconductance. After a total dose of 10^8 rad, the transconductance is at least 85 percent of its original value for both n- and p-channel devices.

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3.3 Ti-DOPED SEMI-INSULATING InP

Nominally updoped InP crystals are n-type, with electron concentrations typically in the mid-10^{15} cm^{-3} range, since the majority of electrically active impurities and defects are donors. Semi-insulating InP has been obtained reproducibly only by doping with Fe, an acceptor located 0.65 eV below the conduction band.[10] Pinning the Fermi level close to this level yields room-temperature resistivities of 10^7 to 10^8 Ω cm. However, the thermal stability of Fe-doped semi-insulating InP is inadequate for many device fabrication procedures.[11]

On the basis of DLTS data for n-type InP doped with Ti, Brandt *et al.*[12] have recently reported that Ti is a deep donor located 0.63 ± 0.03 eV below the conduction band. As these authors have suggested,[12] it should be possible to obtain semi-insulating InP by co-doping with Ti and a shallow acceptor impurity whose concentration is greater than the residual donor concentration but less than the total of the residual donor and Ti concentrations. For such an acceptor concentration the Ti centers will be partially occupied, fixing the Fermi level in the vicinity of the Ti level. We have used this technique to grow three semi-insulating crystals, each doped with a different acceptor impurity, having resistivities of 1.0 to 3.3×10^6 Ω cm.

The liquid-encapsulated Czochralski (LEC) method was used to grow (111)B-oriented InP crystals from melts contained in pyrolytic boron nitride crucibles. For each growth run, the starting charge of polycrystalline InP was doped with the selected acceptor impurity. After a portion of the crystal was grown, metallic Ti was dropped into the melt, and growth was completed. Semi-insulating crystals doped with Zn or Cd were grown at Lincoln Laboratory, and one doped with Be was grown at Rome Air Development Center. A fourth crystal was doped with sufficient Cd to remain low-resistivity p-type after Ti incorporation. Rectangular bars for measuring the resistivity (ρ) and Hall coefficient (R_H) were cut from the crystal portions grown just before and after Ti was added.

The results of room-temperature electrical measurements on two samples from each of the four InP crystals are given in Table 3-1, which lists the acceptor concentration added to the charge, the hole concentration ($p = e/R_H$) and hole mobility ($\mu = R_H/\rho$) before Ti doping, the Ti concentration added to the melt, and the resistivity, carrier concentration, and carrier mobility after Ti doping. For crystals 1, 2, and 3, which were doped with Zn, Cd and Be, respectively, the Ti-doped samples are semi-insulating, with electron concentrations (n) ranging from 7.3×10^8 to 2.5×10^9 cm^{-3}. These samples have mobilities of 2500 or 2600 $cm^2V^{-1}s^{-1}$, which are similar to the values generally obtained for Fe-doped semi-insulating InP.

TABLE 3-1 Room-Temperature Properties of Ti-doped InP				
Crystal	1	2	3	4
Acceptor	Zn	Cd	Be	Cd
Acceptor concentration added to charge (cm^{-3})	7.0×10^{15}	5.0×10^{16}	2.0×10^{19}	3.0×10^{17}
Before Ti doping				
p (cm^{-3})	1.9×10^{15}	4.5×10^{15}	2.9×10^{14}	2.8×10^{16}
μ ($cm^{-2}V^{-1}s^{-1}$)	140	150	140	145
Ti concentration added to melt (cm^{-3})	4.8×10^{19}	5.0×10^{19}	5.0×10^{19}	2.3×10^{19}
After Ti doping				
ρ (Ω cm)	3.3×10^{6}	1.1×10^{6}	1.0×10^{6}	2.04
n (cm^{-3})	7.3×10^{8}	2.2×10^{9}	2.5×10^{9}	
p (cm^{-3})				2.3×10^{16}
μ ($cm^{2}V^{-1}s^{-1}$)	2600	2600	2500	130

Optical absorption measurements were made at ~ 15 K on semi-insulating samples from crystals 1 and 2 over the wavelength range from 0.9 μm, the absorption edge of InP, to 10 μm. Only two absorption bands, located at 546.5 and 550 meV, were observed. These bands were also observed by Brandt *et al.*[12] in n-type conducting samples. They are due to intra-atomic transitions from the ground state of the occupied (un-ionized) Ti^{3+} center, which has a ($3d^1$) configuration.

For crystals 1 and 2, the values of p measured before Ti addition, as listed in Table 3-1, are qualitatively consistent with the Zn and Cd concentrations added to the charge, together with the values reported[13] for the distribution coefficients of these elements in InP. For crystal 3, the Be charge was 2.0×10^{19} cm^{-3}, but p measured before Ti addition was only 2.9×10^{14} cm^{-3}. The distribution coefficient of 1.5×10^{-5} corresponding to these values is far below the reported[13] lower limit of 0.16. Apparently most of the added Be did not dissolve in the melt.

For crystal 4, the difference between the values of p before and after Ti doping is 5×10^{15} cm^{-3}, which should equal the concentration of Ti donors incorporated into the crystal. The ratio of this difference to the concentration of Ti added to the melt is the effective distribution coefficient of Ti. The value obtained is ~ 2×10^{-4}, in reasonable agreement with the value of ~ 5×10^{-4} estimated by Brandt *et al.*[12] from their DLTS data.

In order to determine the thermal activation energy of the Ti donors, R_H was measured as a function of temperature between 20 and 100°C for the Ti-doped samples from crystals 1 and 2. The results are shown in Figure 3-9, where $R_H T^{3/2}$ is plotted against $1/T$. The activation energies found are 0.64 and 0.61 eV, respectively, placing the Ti level at 0.62 ± 0.02 eV, in good agreement with the value of 0.63 ± 0.03 eV reported by Brandt.[12]

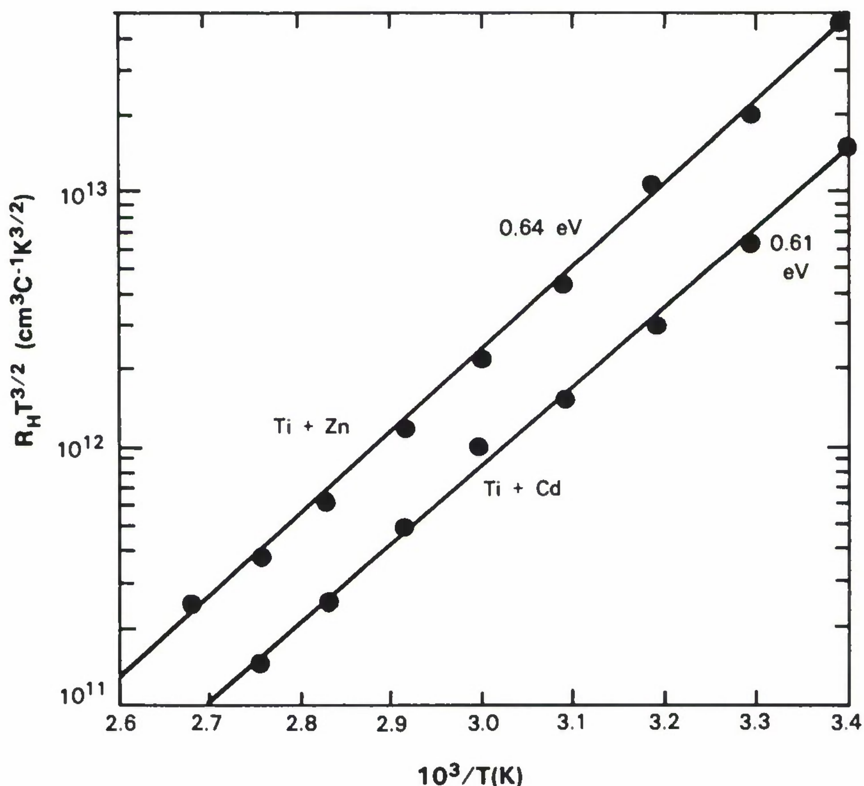

Figure 3-9. Temperature dependence of Hall coefficient for semi-insulating samples of InP co-doped with Ti and either Zn or Cd.

For the semi-insulating samples, the Fermi level calculated from the measured value of n is 0.4 to 0.5 eV below the conduction band. Since the Ti donor level is about 0.1 to 0.2 eV lower, most of the Ti centers are occupied. Crystals with lower carrier concentration and higher resistivity would be obtained by decreasing the ratio of the Ti concentration to the difference between the acceptor concentration and the residual donor concentration. It should be possible to control the doping levels well enough for the reproducible preparation of crystals with resistivities of 10^7 to 10^8 Ω cm. Such crystals will be of great interest for integrated circuit applications if the thermal stability is found to be significantly greater for Ti-doped InP than for Fe-doped material.

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4. MICROELECTRONICS

4.1 CCD VECTOR-MATRIX PRODUCT DEVICE

A CCD vector-matrix product device has been designed and evaluated to perform a sixteen-point discrete cosine transform (DTC).[1] The architecture of this device is implemented by a bank of fixed weight multipliers that represent the matrix by which the input vector will be multiplied. The first wafer run has been fabricated, and preliminary evaluation indicates that the precision of the fixed weight multipliers is within approximately one percent of their design values. At a 10-MHz clock rate the DCT device will be capable of performing 2.5 billion multiplications per second.

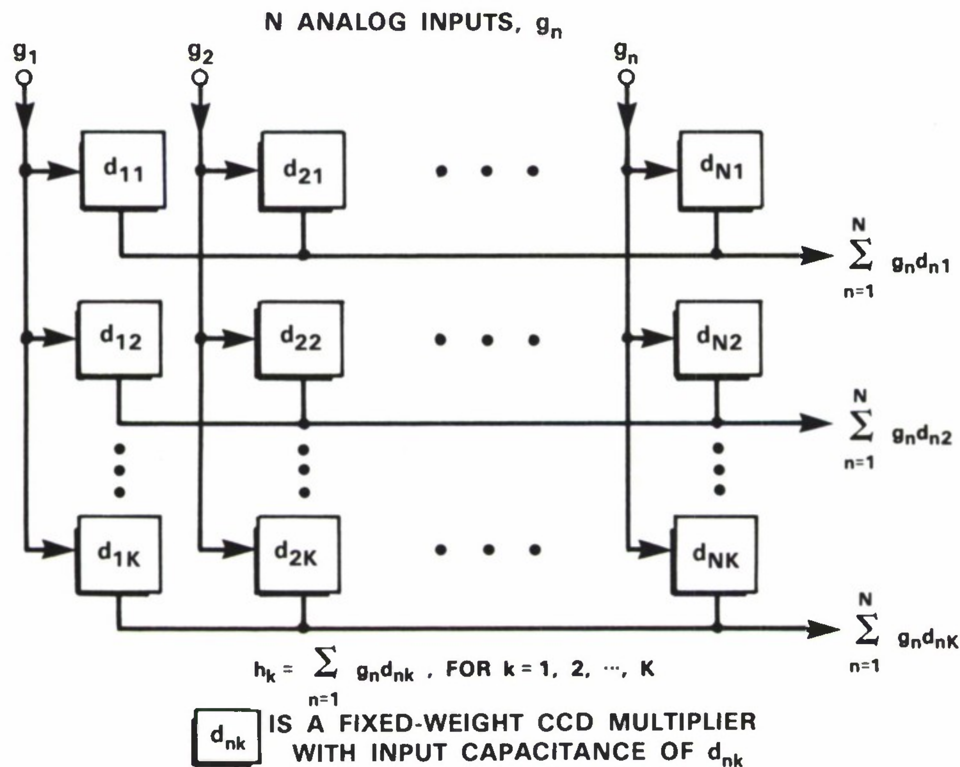

Figure 4-1. Schematic of a CCD vector-matrix product device.

A schematic of the vector-matrix product device is shown in Figure 4-1. Voltages which represent the input vector components, g_n, are placed on columns n = 1 to N. There, the elements of the input vector are multiplied by the appropriate column vectors of the matrix. The products of these multiplications are summed together over each row to produce the elements of the output vector

$$h_k = \sum_{n=1}^{N} g_n d_{nk} \quad . \tag{1}$$

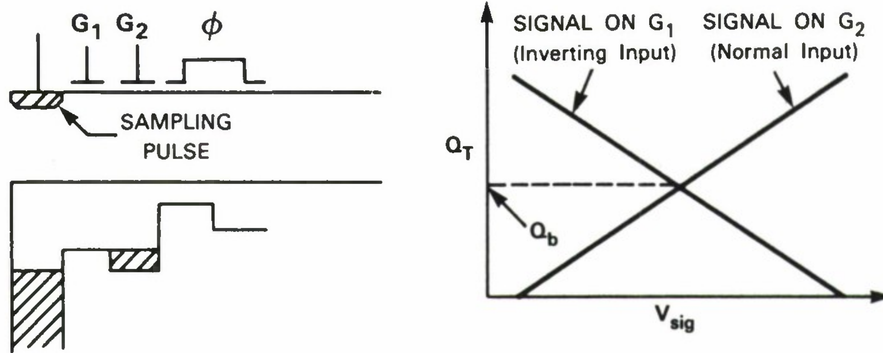

Figure 4-2. A four quadrant CCD fixed-weight multiplier. Q_b is the bias charge (one half full well).

Each element of the matrix, d_{nk}, is represented by a fixed-weight multiplier. The multipliers are implemented as a one-stage surface channel charge-coupled device (see Figure 4-2). The amount of charge injected into the channel of the CCD device during the potential equilibriation, or "fill and spill", method is given by Equation 2.[2]

$$Q_{in} = A_{nk} C_{ox} (V_{g2} - V_{gl}) \tag{2}$$

where C_{ox} is the capacitance of the gate oxide, A_{nk} is the area associated with each multiplier weight d_{nk}, V_{g2} is the voltage placed on gate G2, and V_{Gl} is the voltage placed on gate G1. As shown in Figure 4-2, for a positive weight multiplier, the signal voltage is applied to G2 and a reference voltage to G1; this is reversed for a negative weight multiplier. With a half-full-well bias charge, Q_b, one can see that the device has the capability for four-quadrant multiplication. In order to perform a sixteen-point discrete cosine transform, the multiplier weights are chosen so that they are proportional to the discrete cosine kernels, for example,

$$A_{nk} \approx d_{nk} = \cos\left(\frac{2\pi nk}{16}\right) . \tag{3}$$

Then, if the input vector corresponds to real time samples, the output vector will correspond to the real part of the sixteen spectral points.

A photomicrograph of the DCT device is shown in Figure 4-3. A double poly, double metal CCD process was used to fabricate the device, which measures 4.5 × 4.5 mm.

The precision of the DCT device is dependent on three factors. The first is the linearity of the CCD multipliers themselves. The next is the gain and linearity of the source-follower amplifier. The final factor is the precision with which the ratios of the multiplier weights can be controlled. The linearity of the CCD multipliers can be assured by using a surface channel input structure. The source follower was designed so that with a 3-V peak to peak, 10-MHz sine wave input, the total harmonic distortion at the output is less than 0.3 percent. Table 4-1 presents a summary of the overall DCT multiplier performance, which shows that the actual multiplier

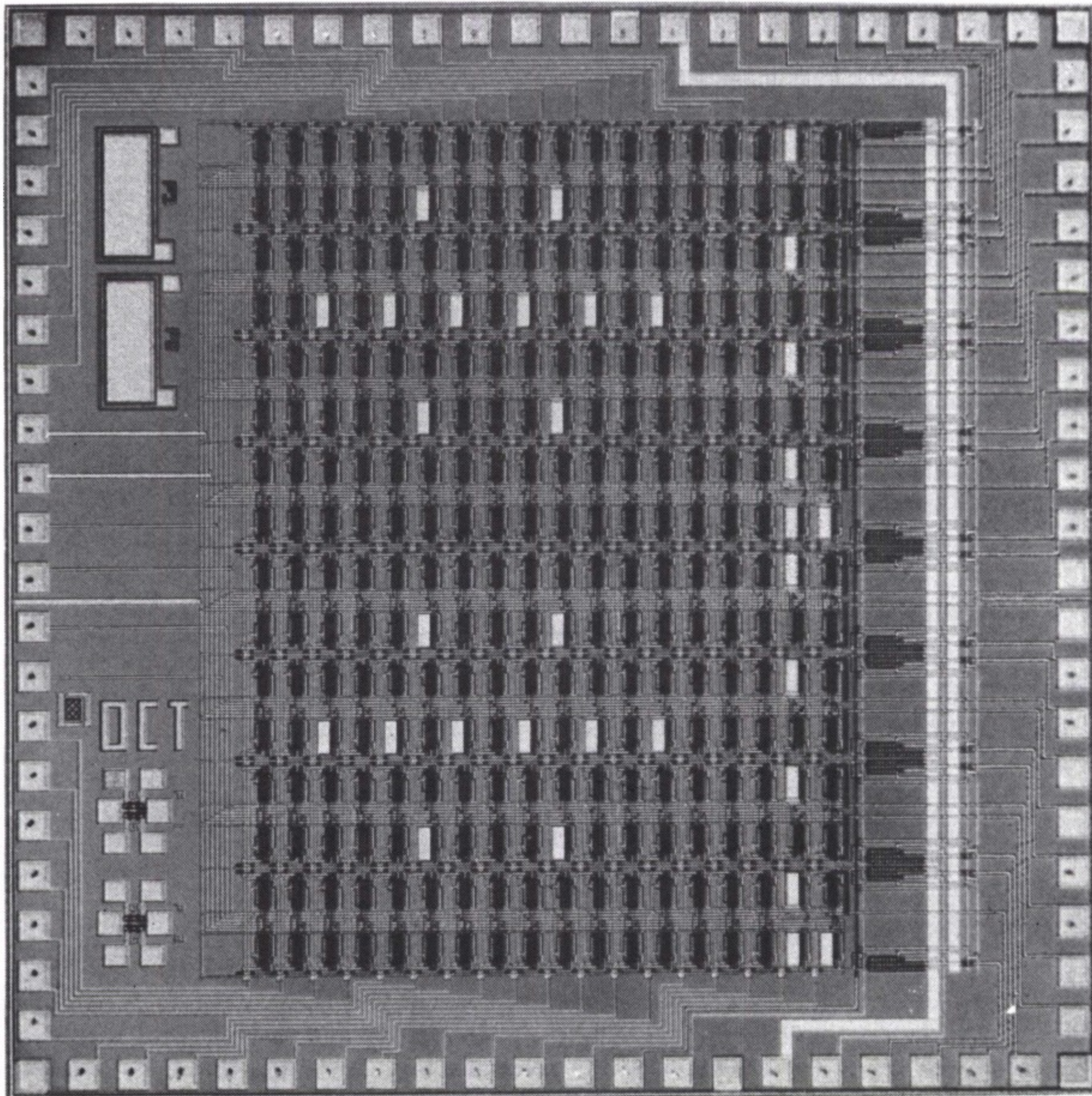

Figure 4-3. Photomicrograph of DCT chip.

TABLE 4-1		
Measure Performance of a CCD Vector-Matrix Product Device		
Designed Multiplier Weights	**Measure Multiplier Weights (Normalized)**	**Error (Percent)**
1.0000	1.0000 ± 0.0106	0.00
0.9250	0.9301 ± 0.0131	0.55
0.7071	0.7135 ± 0.0138	0.60
0.3825	0.3883 ± 0.0137	0.58
-1.0000	-1.0023 ± 0.0099	0.23
-0.9250	-0.9400 ± 0.0073	1.50
-0.7075	-0.7249 ± 0.0126	1.74
-0.3825	-0.3959 ± 0.0096	1.34

weight accuracies are within about 1 percent of their design values. These data were taken at a clock rate of one 100 kHz. Further testing of the device at higher speeds is planned.

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4.2 A LOW-LOSS Ku-BAND MONOLITHIC ANALOG PHASE SHIFTER

We have fabricated a GaAs monolithic Ku-band analog phase shifter with integrated planar varactor diodes. This device has achieved a phase shift comparable to that obtained with a previously reported analog phase shifter,[3] but with lower insertion loss at higher frequency. Furthermore, this approach is extendable to millimeter-wave frequencies. We have also demonstrated a full 360° phase shifter with low insertion loss by cascading three monolithic phase shifter chips.

GaAs epitaxial layers grown by molecular beam epitaxy (MBE) were used for circuit fabrication. A 2-μm n^+ layer doped to 1×10^{18} cm^{-3} was first grown on a semi-insulating substrate, followed by a 5000-Å n-type layer with 8×10^{16} cm^{-3} doping concentration. The n layers in the ohmic contact regions were chemically etched off, and Ni/Ge/Au metallizations were then defined in these regions by lift-off. After alloying at 450°C for 30 s, the diodes were isolated by a

deep mesa etch. The Schottky barrier contacts and the microwave circuit were defined simultaneously using a PMMA-AZ 1470 photoresist double-layer structure to lift off a 2-μm Ti/Au metallization.

The phase shifter circuit is shown in Figure 4-4. It consists of a branch line 90° hybrid coupler with a Schottky diode at each of the output arms. Both diodes are grounded through high impedance inductive lines; this increases the total phase shift. The chip size is 3.1 × 2.4 mm. Due to the simplicity of the circuit and the small component count, high yield can be expected. Greater than 80 percent yield has been achieved in the several wafers fabricated thus far.

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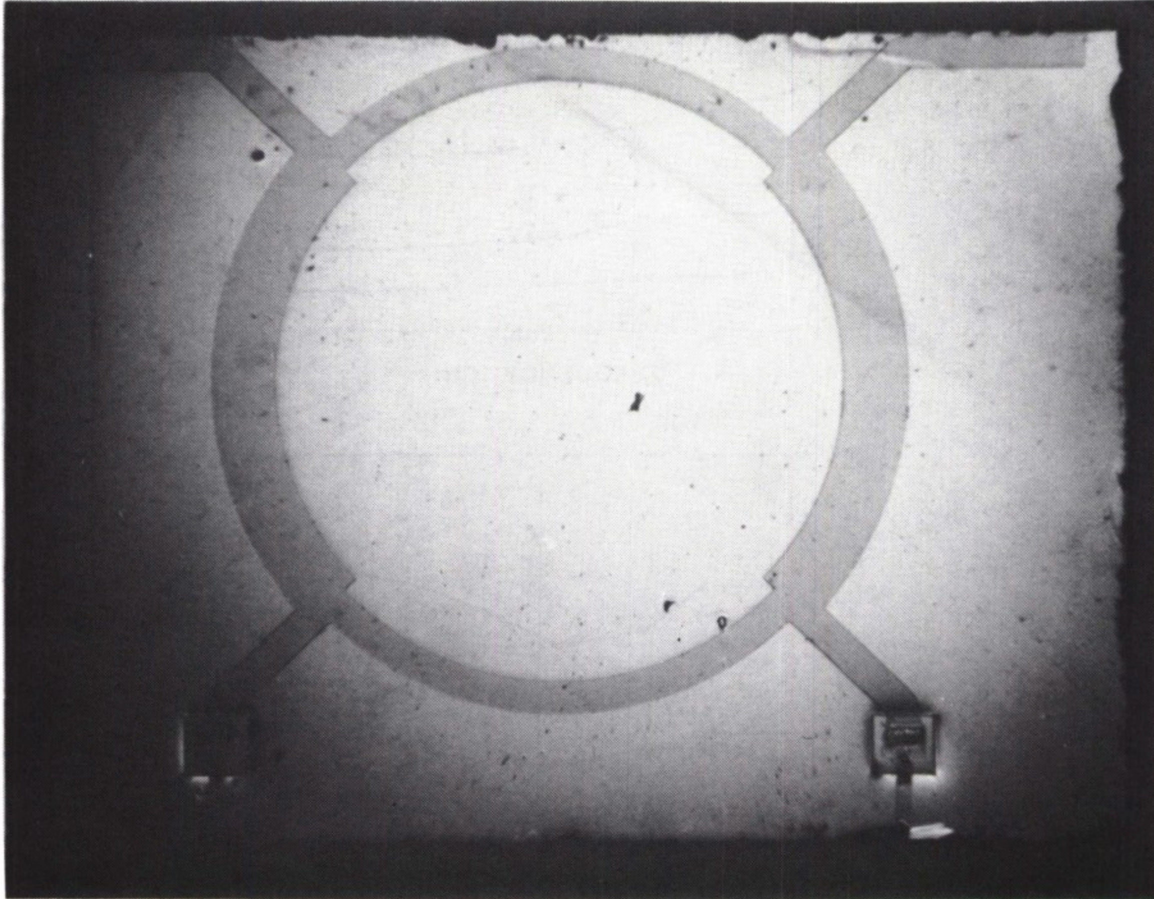
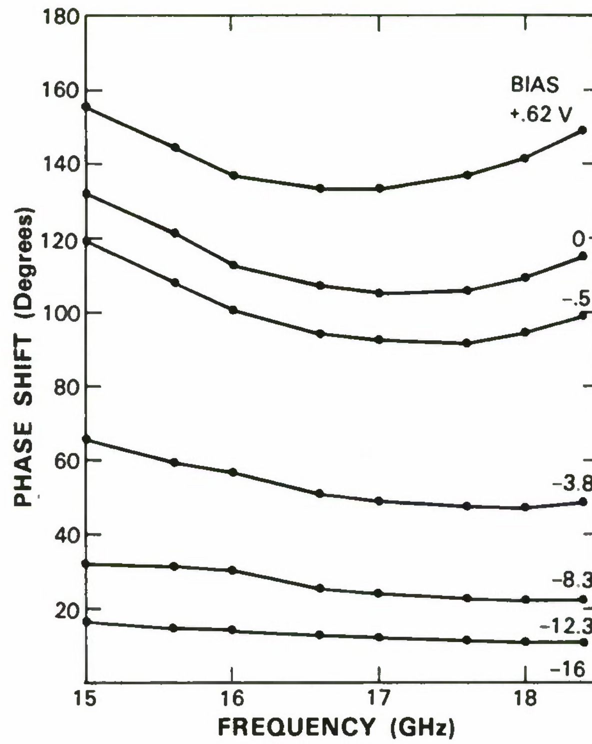


Figure 4-4. Photograph of the analog phase shifter. The chip size is 3.1 × 2.4 mm.

The Schottky barrier diodes integrated in the circuit had a reverse breakdown voltage of 16 V and a series resistance of 4 Ω. The zero-bias capacitance was 0.33 pF and the capacitance ratio between a reverse bias of 0 V and 16 V was approximately 3:1. The measured phase shift and insertion loss are shown in Figure 4-5. From 0 V to 16 V reverse bias, a phase shift of 109° ± 3° was obtained between 16 and 18 GHz. The measured insertion loss was 1.8 ± 0.3 dB.



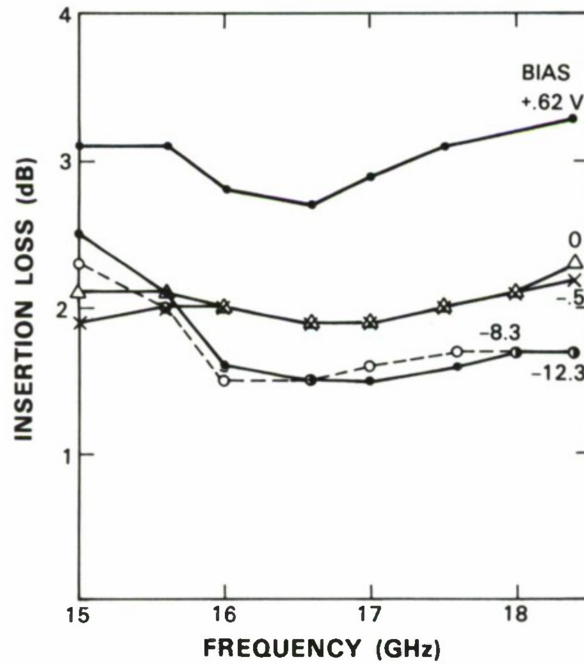


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Figure 4-5. Phase shift and insertion loss of the phase shifter. The insertion loss includes approximately 0.5 dB of test-fixture loss.

All the insertion loss results reported here include approximately 0.5 dB of test fixture loss. Both phase and insertion loss variations increase with bandwidth. For example, from 15.5 to 18.5 GHz a phase shift of 114° ± 8° with an insertion loss of 1.9 ± 0.6 dB was measured. In this same frequency range, when the diodes were forward biased to +0.62 V, the phase shift increased to 140° but the insertion loss also increased to approximately 3 dB. Increasing the input power to 20 dBm resulted in no measurable phase change.

A 180° phase shifter was realized by connecting two phase shifter chips in series. Between 16 and 18 GHz the measured phase shift was 183° ± 7° and the insertion loss was 3.2 ± 0.6 dB. A full 360° phase shifter was constructed in the same manner by cascading three phase shifter chips. As shown in Figure 4-6, the measured phase shift was 359° ± 17° between 16 and 18 GHz and the insertion loss was 4.2 ± 0.9 dB. For a smaller bandwidth, 16 to 17.5 GHz, the insertion loss was reduced to 3.9 ± 0.6 dB and the phase variation decreased to ± 8°. To the best of our knowledge, this is the lowest insertion loss reported for a Ku-band 360° phase shifter. Both the device technology and design approach can be applied to phase shifters at millimeter wave frequencies.

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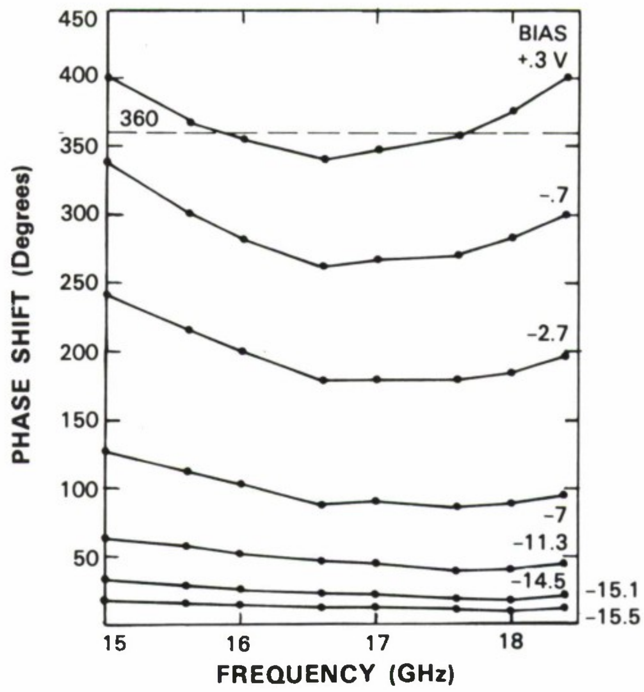
4.3 ELECTRON-BEAM PROGRAMMING OF CMOS DIGITAL SYSTEMS

An electron beam is particularly interesting in high-density circuit restructuring applications since commercially available systems provide submicrometer beam size, accurate positioning, and high speed deflection. An electron beam can be used to selectively charge floating gate FET devices and thereby affect the logic function. In a previous report[4] the fabrication of an nMOS, wafer scale, electron beam programmable, read only memory system was described. We are currently working to extend these techniques to the programming and testing of CMOS systems.

In CMOS technology, p-channel floating gate FET devices, which are similar to the transistors used in commercial EPROM circuits, provide the basic element for circuit restructuring. In the unprogrammed state, the floating gate transistors demonstrate a high impedance between source and drain, but they can be programmed into the conducting state by selective electron beam irradiation. Nonvolatile programming is assured, since the charge deposited on the gates has been shown to be stable for many years of room temperature operation. The floating gates can be discharged by exposing the devices to flood illumination with ultraviolet light. The floating-gate FET can thus be used as a nonvolatile, programmable digital switch.

A number of test devices have been fabricated in a 3-μm, p-well, CMOS technology using the MOSIS silicon foundry. In the off state, these devices demonstrated very low leakage currents, of the order of 1 pA, but the leakage was observed to increase with increasing drain voltage. Typically, CMOS logic is operated with a drain voltage of 5 V and a substrate bias of 5 V.

* Present address: M/A-Com.



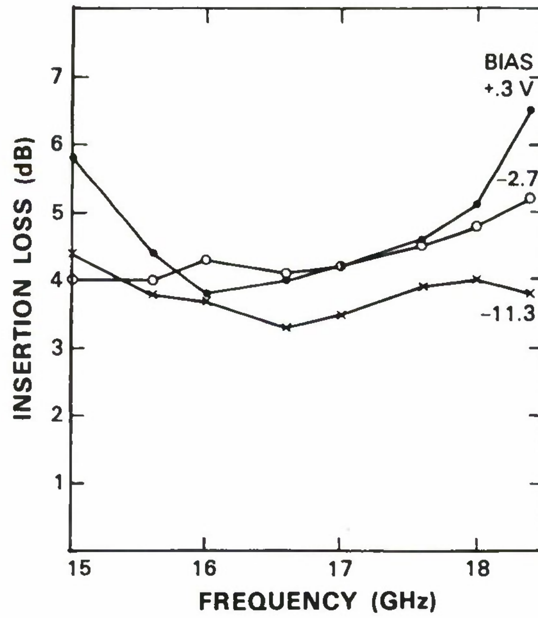


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Figure 4-6. Phase shift and insertion loss of a 360° phase shifter constructed by cascading three phase shifter chips. The insertion loss is not corrected for test fixture loss.

Under these conditions, the drain leakage current, for a minimum feature size floating gate device, approaches 15 μA, as illustrated in Figure 4-7. The observed leakage is due to capacitive coupling between the floating gate and the drain, which has the effect of biasing the gate toward conduction as the drain voltage is increased. As illustrated in Figure 4-7 the problem can be solved by increasing the substrate bias, thereby shifting the thresholds of the p-channel devices and reducing the leakage. While this technique solves the leakage problem and also improves the switching speed of the circuits, it is not compatible with many existing designs and cell libraries which tie the substrate to the drain power supply bus throughout the circuit. For this reason, we are interested in other solutions to the leakage current problem.

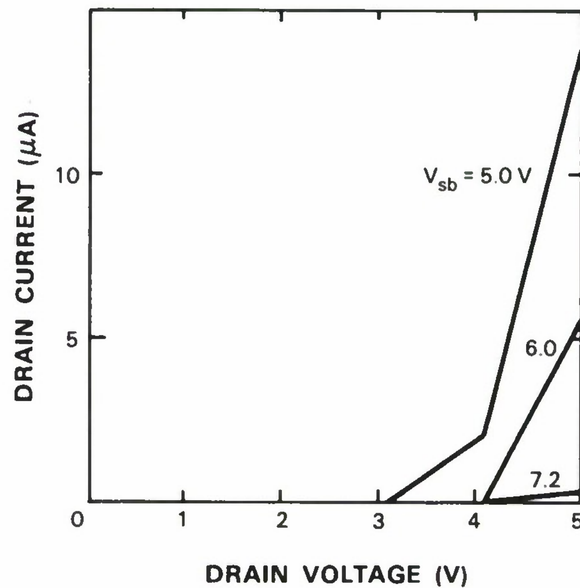

Figure 4-7. Drain leakage current vs drain voltage for various values of the substrate bias voltage (V_{sb}).

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In the circuit structure shown in Figure 4-8 a metal conductor has been routed over the floating gate, insulated from the gate by a dielectric layer. This floating gate FET can be programmed in the conventional manner by targeting the electron beam on the small stub of polysilicon that extends beyond the metal structure. Potentials applied to the metal electrode will be coupled capacitively to the gate and thereby affect the channel conduction of the FET. For the p-channel devices, negative potentials will enhance channel conduction and positive potentials will diminish conduction, as illustrated in Figure 4-9. A potential of about 10 V is required to reduce the drain leakage current to below 1 nA. In a digital system, one metal bus would be routed over all the floating gate FETs and connected to an input pin or to an on-chip bias generator.

Additional applications of the overlapping metal electrode circuit structure are currently under investigation. The insulating dielectric layer, which separates the metal electrode and floating gate, can be rendered conductive by exposure to ultraviolet light. Preliminary experiments indicate that biasing the metal electrode during UV exposure can be used to induce trapped charge on the floating gate. The conduction of the device may be enhanced or diminished depending upon the polarity of the metal electrode during UV exposure. This experiment suggests

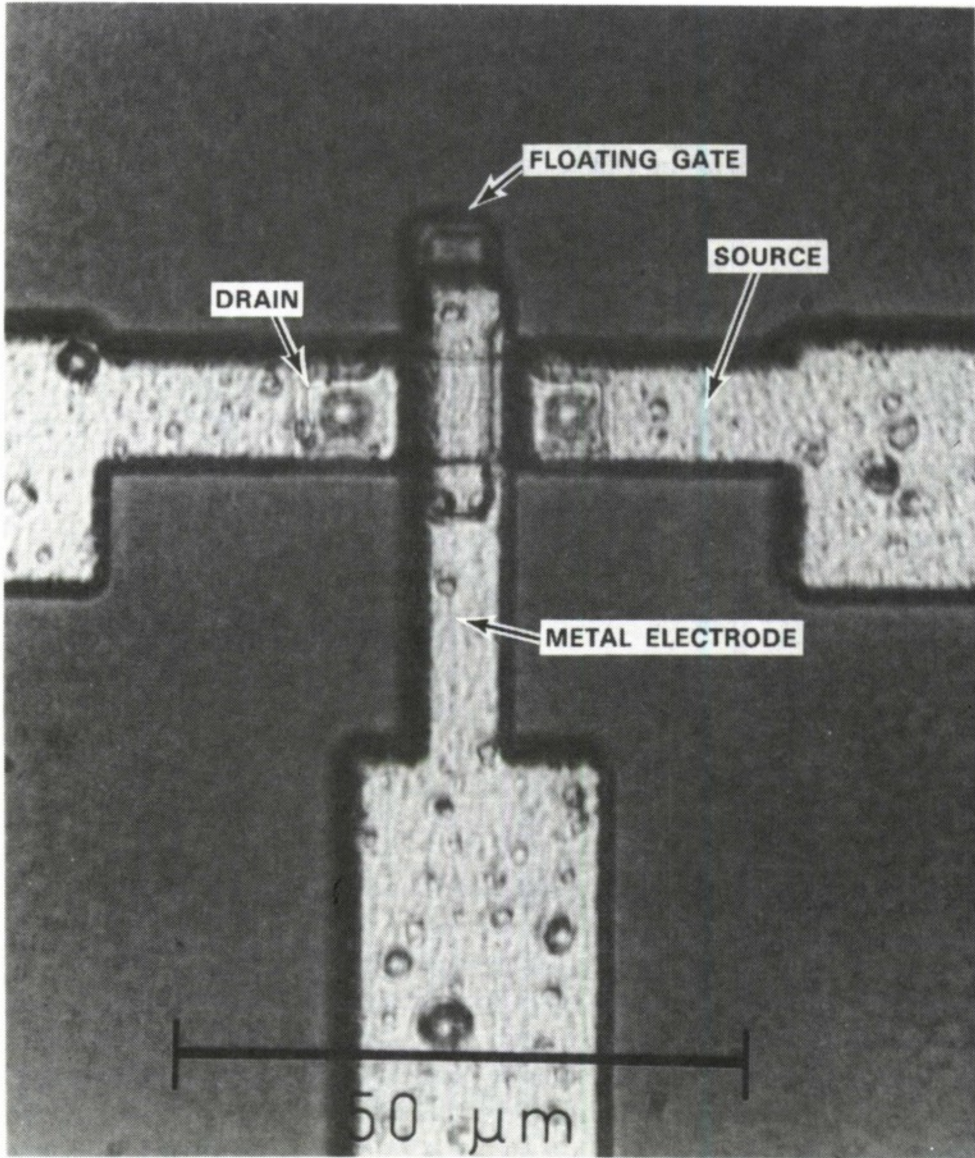

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Figure 4-8. Floating-gate FET with overlapping metal electrode.

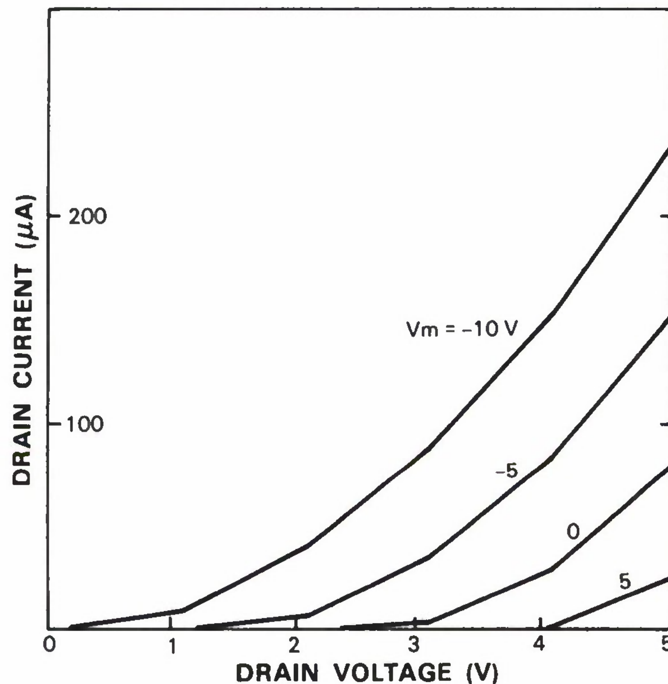

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Figure 4-9. Drain leakage current vs drain voltage for various values of the metal electrode voltage (V_m).

that a focused beam of electrons of the appropriate energy could be used to induce the conductivity in the same manner, which would offer the possibility of selectively erasing the devices in the electron beam system.

T.M. Lyszczarz

4.4 NOISE PROPERTIES OF QUANTUM WELL STRUCTURES

Double barrier, quantum well structures continue to attract interest in their application as ultrafast two-terminal and possibly three-terminal devices. Several two-terminal devices have been demonstrated to date. These include the negative resistance oscillator[5] at microwave frequencies and the direct detector in the submillimeter region.[6]

Recently we have studied the feasibility of using the quantum well structure as a two-terminal negative resistance amplifier. In the course of these studies, the microwave power spectrum was measured to determine the limitations on amplifier noise figure. Surprisingly, the noise was significantly less than expected. Specifically, it was at least a factor of two less than would have been generated by a high-quality tunnel diode having identical I-V characteristics. This has important implications on the performance of the two-terminal amplifier and on any three-terminal counterpart. It may also be an important clue in understanding the dynamical behavior of the quantum well structure.

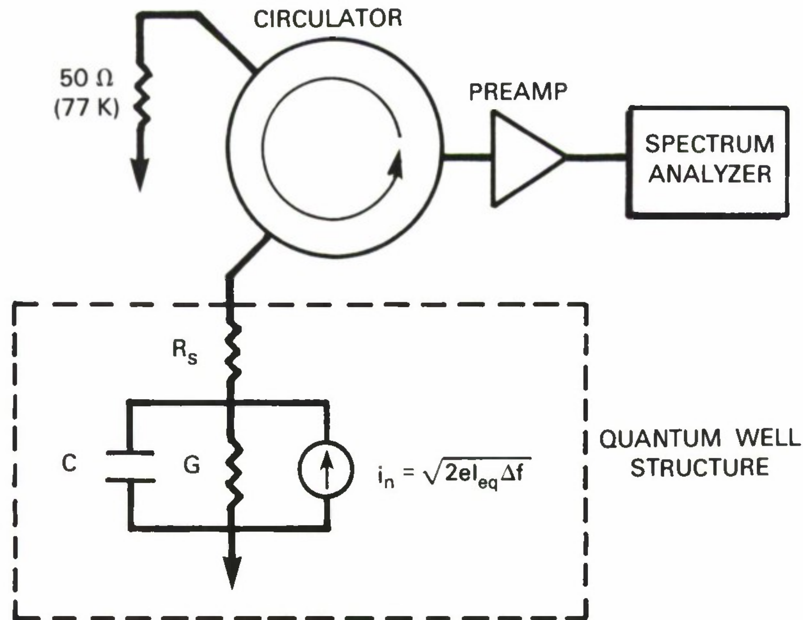

Figure 4-10. Small signal model of quantum well structure and apparatus used to measure noise power.

The small signal and noise circuit model tentatively adopted for the quantum well structure is shown within the dashed box of Figure 4-10. It is simply the well-known junction diode model, wherein G represents the dynamic conductance of the sample, C is the capacitance, and R_s is the series resistance. For the quantum well samples, R_s has both contact and substrate contributions. Because all evidence indicates that R_s should be at least an order of magnitude less than the dynamic resistance, it was neglected in the present work. All of the noise generated by the sample is lumped into the shot noise current generator, i_n. For full shot noise we expect I_{eq} to be equal to the DC bias current, I_0. Historically, tunnel diodes have always been found to display values of I_{eq} somewhat greater than the bias current.[7]

Also shown in Figure 4-10 is a schematic diagram of the apparatus used to measure the noise power. The quantum well structure is coupled to a standard preamplifier through a low-loss circulator. This allowed for accurate measurements at all points of the I-V curve without complication due to device-preamplifier impedance mismatch. The noise power was measured in a narrow bandwidth centered near 1.0 GHz. This frequency is well above the 1/f knee of these devices but well below the cutoff frequency,

$$f_c = \frac{1}{2\pi C[R_s/G]^{1/2}}.$$

Separate network measurements performed on all the samples confirmed that the impedance was predominantly real and that there were no resonances in the 1.0 GHz region. From the known dynamic resistance of the device, the noise temperature and gain of the preamplifier, the bandwidth of the spectrum analyzer and the characteristics of the circulator, the equivalent shot noise current was determined directly from the noise power.

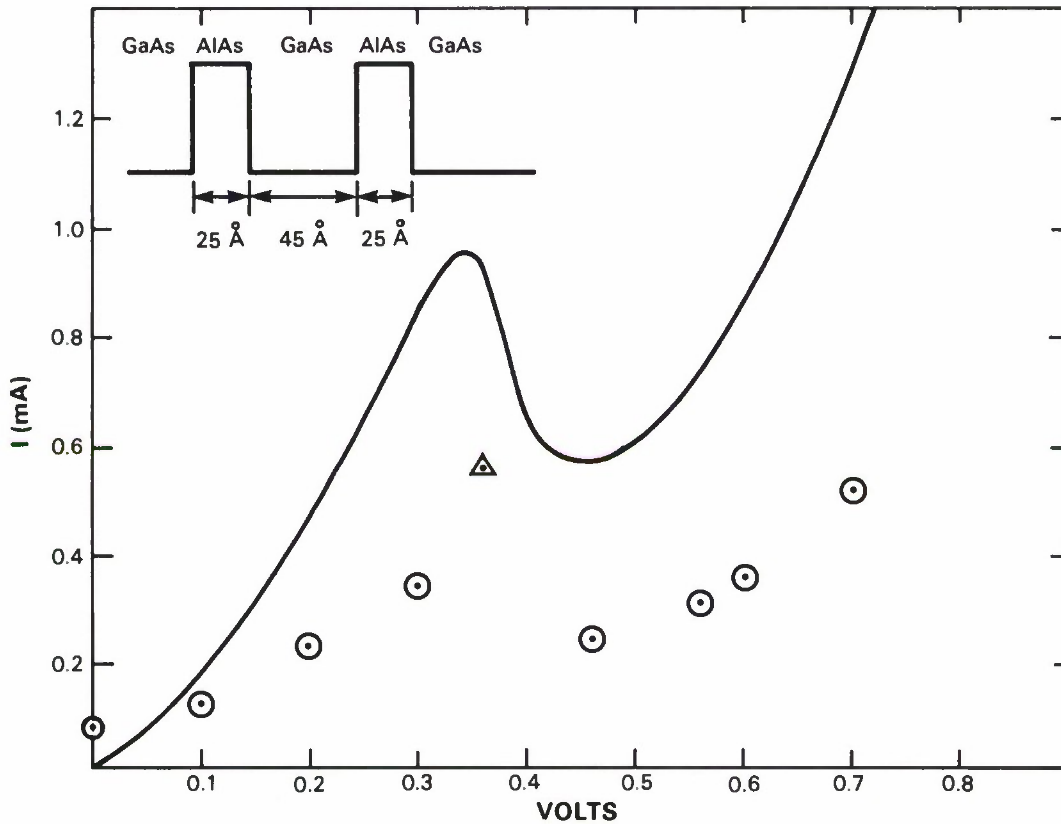

Figure 4-11. Current-voltage characteristic of quantum well structure and calculated values of equivalent shot noise current. (⊙ = I_{eq} at 299 K; ◬ = I_{eq} in negative resistance region.)

Shown in Figure 4-11 is the I-V curve and the calculated value of equivalent shot noise current for a representative quantum well sample at room temperature. This particular sample has pure AlAs barriers, both approximately 25-□ thick. At most points of the I-V curve the equivalent shot noise current is significantly less than the bias current. Above 0.2 V, the ratio I_{eq}/I_0 is about 0.4. The data point in the negative resistance region was obtained by shunting the device with a stabilizing resistor of 50 Ω. The noise measurement was repeated on different samples and at different temperatures. For example, another AlAs-barrier sample was tested at 22 K and an AlGaAs-barrier sample was tested at room temperature. In both cases, the results were qualitatively very similar to those shown in Figure 4-11. At the reduced temperature, the ratio I_{eq}/I_0 was close to 0.5.

A convenient check on the data and measurement technique is provided by the zero-bias noise. Under zero bias, the quantum well is in thermodynamic equilibrium. Therefore, one expects the equivalent shot noise current to approach the value $I_{eq} = 2kTG/e$. For the sample in Figure 4-11 and all others tested, the zero bias equivalent shot noise current did approach this value within 5 percent.

We are presently considering two models to explain the observed noise of the quantum well structures. One model assumes that the shot noise is generated primarily by the current that tunnels through the first barrier. The noise is smoothed because the charge stored in the well increases the first barrier height and thereby suppresses further current flow. This is a built-in negative feedback mechanism analogous to the effect of the space charge on the shot noise in vacuum tubes.[8] Feedback mechanisms in the quantum well structure have been proposed,[9] but the present results could represent the first experimental evidence for their existence. The other model assumes that the device noise is generated by shot noise currents in both barriers, and that these currents are fully uncorrelated. The equivalent circuit for this model would be different than that shown in Figure 4-10. Specifically, there would be a dynamic resistance for each barrier and two independent shot noise current generators. Although this model yields good agreement with experiment at low temperatures, we believe it is less plausible than the feedback model because it requires that the second barrier have a tunneling conductance comparable to the first. In order for this to be true, an electron would have to scatter inelastically in the well before tunneling out. The lifetime of electrons in the well is thought to be far too short for such relaxation to occur.

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4.5 TECHNOLOGIES FOR OPTICAL INTERCONNECTS

We are developing a hybrid approach called multichip integration which integrates logic and driver electronics with optoelectronic devices. Laser and logic chips are imbedded in a potting material to form a large multichip, which then can be processed photolithographically as one large chip to form thin film interconnections between the imbedded component chips. With this approach, the individual components can be optimized and selected without regard to the process compatibility required for monolithic integration.

One of the first steps in this development effort was selection of a potting material compatible with the photolithographic processing required to interconnect the chips. A room-temperature curable epoxy has been found and used with success. It joins continuously to the device without gaps, as required for thin film metallization, and has satisfactory adherence. When fully cured, this epoxy resists all solvents and acids used during photolithographic processing and does not outgas during vacuum deposition of conductor metallization. Preliminary testing has shown this epoxy to be transparent to optical radiation, possibly eliminating the need to protect the output facet of the laser from the epoxy.

Chips have been embedded successfully in this epoxy by attaching the devices directly to a heat sink and injecting a metered amount of epoxy to flow around the chips and fill the cavity in the mold. The natural surface tension of the liquid epoxy prevents the overflow of the epoxy onto the active areas and provides a smooth planar surface up to the edges of the chips with no gaps at the interface. Circuit metallization has been deposited and photolithographically defined over these edges with no discontinuities.

The first multichip under investigation is the transmitter part of an optical interconnect between high speed digital circuits. We plan to integrate a GaAs integrated circuit with a laser to function as a 4:1 parallel-to-serial converter with a clock rate of 1.3 GHz. We have tested a discrete coaxial breadboard of this circuit which consists of a GaAs 4-bit universal shift register connected to a laser. This breadboard has been operated successfully with the GaAs logic circuit driving the laser directly at a clock rate of 1.3 GHz.

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4.6 HETERODYNE IMAGING OF A 135-GHz SOURCE USING MICROSTRIP ANTENNAS INTEGRATED WITH PLANAR MIXERS

Images in the millimeter band have been formed traditionally by the mechanical or electronic scanning of a single beam, after which the image is assembled pixel by pixel. Among the limitations of this approach are its inability to produce real time images as well as the cost and complexities introduced by the scanning apparatus. Recently there has been progress in the application of planar antenna and detector array technology to imaging, but until now the only planar imaging systems demonstrated have used video detection.[10-12] Obstacles to the development of planar arrays of heterodyne detectors have been the difficulty of properly illuminating all elements of the array simultaneously with both signal and local oscillator and the difficulty of building sensitive high-frequency planar mixers.

Here we describe an approach to the illumination problem and report the first use of an array of planar heterodyne detectors to obtain the image of a distributed millimeter wave source. Our two-dimensional array consisted of five pairs of printed dipole antennas integrated with Schottky diodes on top of a crystal quartz substrate, as shown in Figure 4-12. The design and sensitivity of the elements of the array have been described earlier.[13]

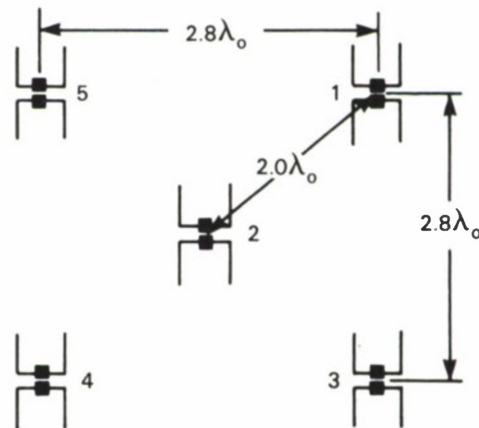

Figure 4-12. Arrangement of antenna pairs on substrate. Not shown are the five diodes and the transmission lines from the diodes to the edges of the substrate.

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The quartz substrate was placed in the focal plane of a 10-cm, f/0.8 offset paraboloid for the imaging test. An offset paraboloid was chosen because there is no aperture blockage of the signal by the array and because the local oscillator can be coupled onto the array without the use of a beam splitter or diplexer, as described below.

The carcinotron local oscillator signal was optically coupled onto the array from an f/3 scalar feed located at the side of the offset paraboloid, as shown in Figure 4-13. The beam from the LO feed was focused to a diameter of 10 λ at the array plane, thus providing nearly uniform excitation of the five elements with ~ 1.5 mW each of LO power.

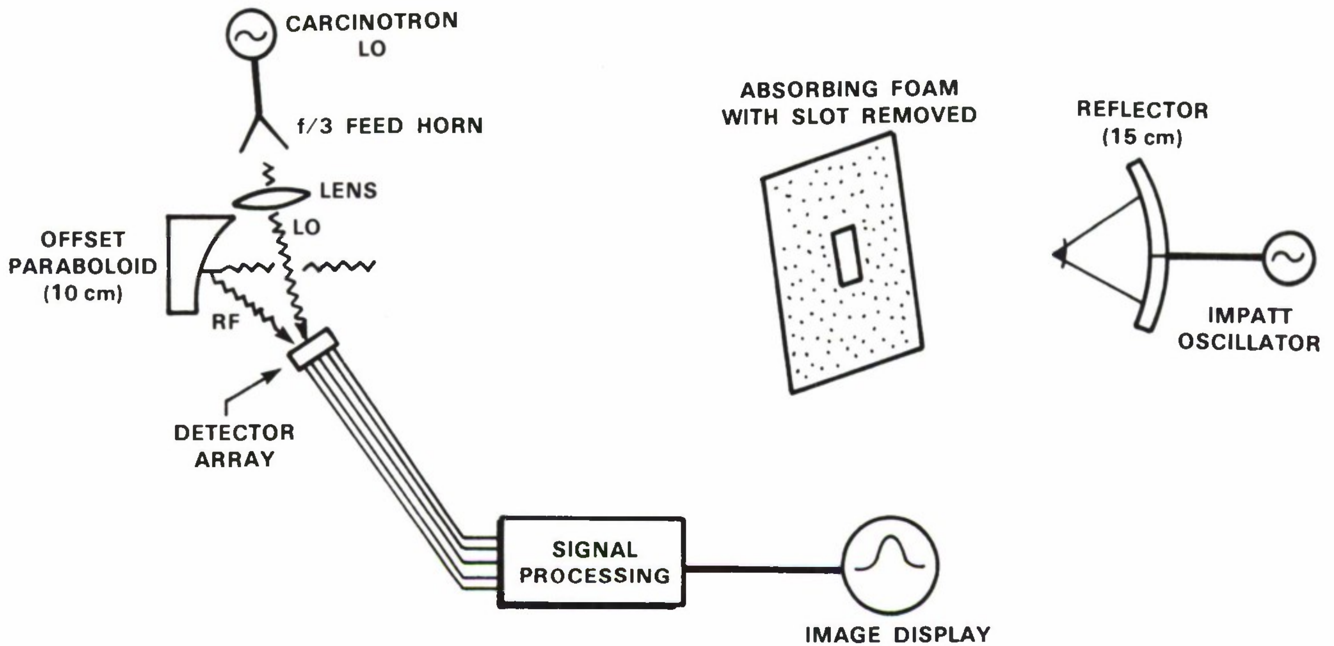

Figure 4-13. Diagram of the imaging experiment.

The distributed source was a 7.7 × 23 λ aperture of radiation at ~ 2 × 10^7 K against a background at 300 K. This source was created by removing a 1.7 × 5.0 cm slot of material from the center of a large sheet of absorbing foam, and by illuminating the back side of the foam with the radiation from a 15-cm reflector antenna, as shown in Figure 4-12. The reflector was driven by a 3-mW, 135-GHz IMPATT oscillator, which was coupled to a variable attenuator. The distributed source was positioned 40 cm from the 10-cm offset paraboloid.

The first image was obtained using video detection (no LO signal) of an amplitude-modulated signal from the IMPATT. A theoretical estimate of the image size of the slot at the focal plane is 1.8 × 5.4 λ. Figure 4-14(a) was recorded when the slot was positioned so that elements 1, 2 and 4 were illuminated, and Figure 4-14(b) was recorded when the slot was rotated by 90° and elements 2, 3 and 5 were then illuminated. This figure illustrates the uniform response and high on-off contrast which was achieved.

Figure 4-15 shows an image of the slot obtained when the power from the IMPATT was decreased by 50 dB and heterodyne detection was used. The LO frequency was 133.5 GHz and the intermediate frequency was 1.5 GHz with an IF bandwidth of 75 MHz. The principal advantage that heterodyne detection offers over video detection is significantly greater sensitivity, which is demonstrated in this experiment.

A resolution test of the system was performed by placing a point source at different locations in the far field of the offset paraboloid, which yielded a resolution of 3.0° ± 0.3°. This value can be compared with a calculated value of 3.25°. The calculated value is approximately 2.5 times the diffraction limit available with the 10-cm paraboloid. For the given reflector, the resolution could be improved by approximately a factor of two by decreasing the separation of the detectors on the focal plane. Further improvement beyond a factor of two comes at the expense of increased interaction among the elements as they are brought closer together.

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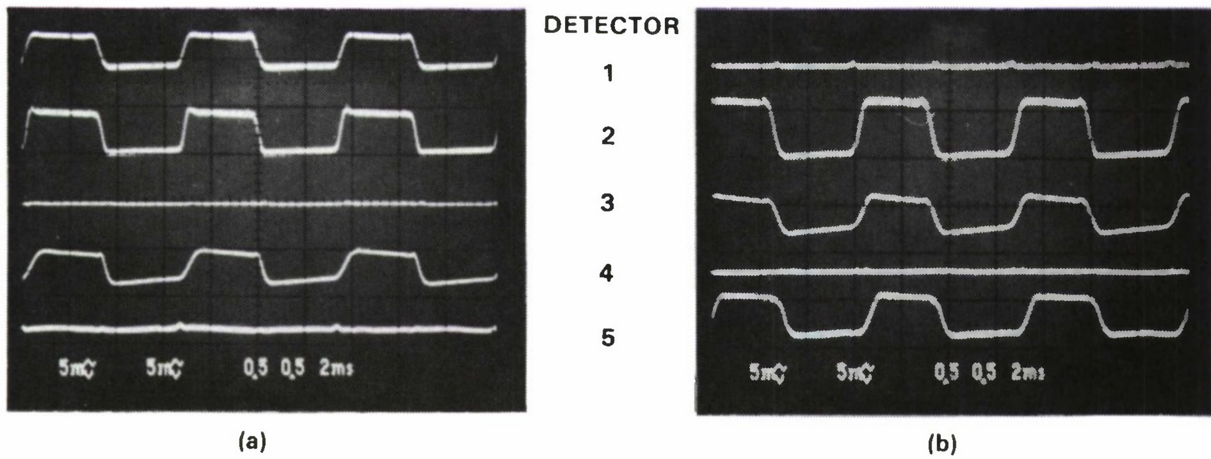

Figure 4-14. Representation of video image of the slot when (a) elements 1, 2 and 4 were illuminated, and when (b) elements 2, 3 and 5 were illuminated.

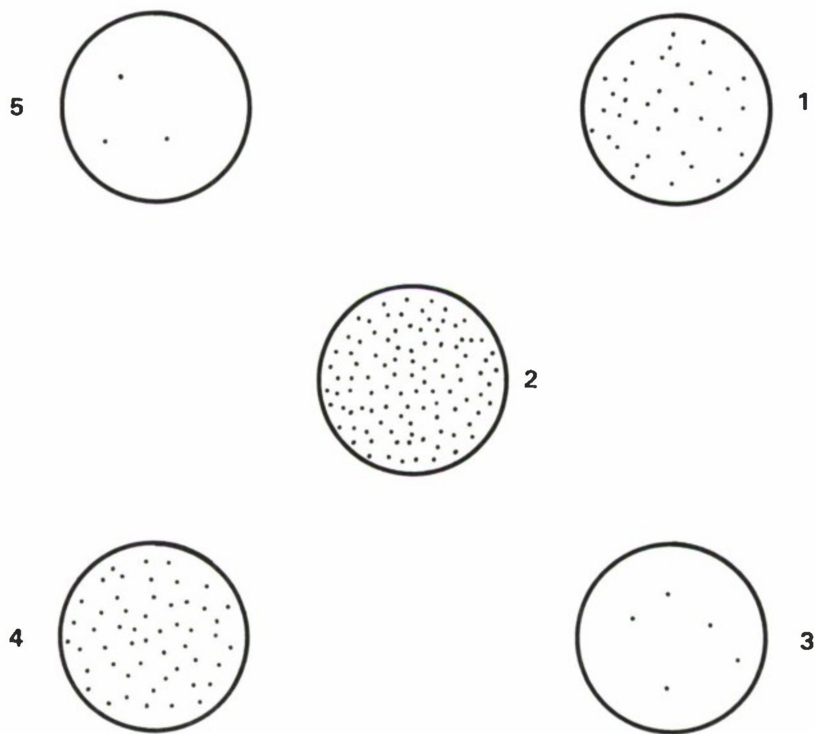

Figure 4-15. Representation of heterodyne image of the slot when elements 1, 2 and 4 were illuminated. The density of the dots is proportional to the power received by each detector.

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5. ANALOG DEVICE TECHNOLOGY

5.1 SAW/FET PROGRAMMABLE TRANSVERSAL FILTER WITH 100-MHz BANDWIDTH AND ENHANCED PROGRAMMABILITY

The surface acoustic wave/field effect transistor (SAW/FET)[1-3] is a wideband programmable transversal filter with a large tap-weight programmability. Substantial design and fabrication improvements have yielded a 100-MHz programmable bandwidth and 20-dB programmable on/off ratio, the latter being defined as the ratio of the output with all taps on to the response with all taps off.

The SAW/FET was described in detail previously.[2-3] Briefly, as shown in Figure 5-1, a $LiNbO_3$ SAW delay line is coupled to a Si integrated circuit that contains the programmable analog taps which sample the signal propagating along the SAW delay line. The taps are metal fingers weighted by the variable capacitance of their inherent MOS varactor. The varactor weights are programmed by bias voltages introduced through an array of programming FETs which are switched by an on-chip digital shift register. The tap outputs are capacitively coupled to an on-chip summing bus. A dual-track structure is used to increase the programmable on/off ratio and to provide bipolar programming weights.

The extension to 100 MHz of programmable bandwidth has been accomplished by halving the finger pitch to 15 μm and doubling the number of taps to 350 with minimal increase in the density of programming circuitry in the silicon. The pitch of the shift register remains at 30 μm, but each stage of the shift register now controls access to a pair of taps. The actual tap which is connected to the programming line is determined by a pair of additional pass transistors switched by an additional pair of input clocks, ϕ_e and ϕ_o, as shown in Figure 5-1.

Calculations[3] indicate that 30 dB of programmable on/off ratio is possible if the varactor taps can be biased over the full range of capacitance expected for a planar MOS structure. In the previous device the full range of capacitance was not available because each tap was connected to the source diffusion of a MOSFET, which formed a junction diode to the substrate and prevented full accumulation of the MOS varactor. The present SAW/FET, however, makes possible the full range of bias voltages and corresponding capacitance variation by placing the n-channel logic and programming circuits in a junction-isolated p-doped region on an n-type silicon substrate, as shown in Figure 5-1.

Figure 5-2 shows the SAW/FET impulse response when programmed with a square wave such that groups of ten adjacent taps are turned fully on and the next ten adjacent taps are turned off. The top trace shows the input RF impulse and the second trace from the top shows the RF output. The programming waveform and shift register input are shown at the bottom of the picture on a much slower time scale than the top two traces. The on/off ratio is about 20 dB in dual-track operation and about 6 dB in single-track operation. The difference in amplitude between the front and rear portions of the impulse response results from the use of two output summing busses per acoustic track with different output impedances. These can easily be made equal by using different matching circuits.

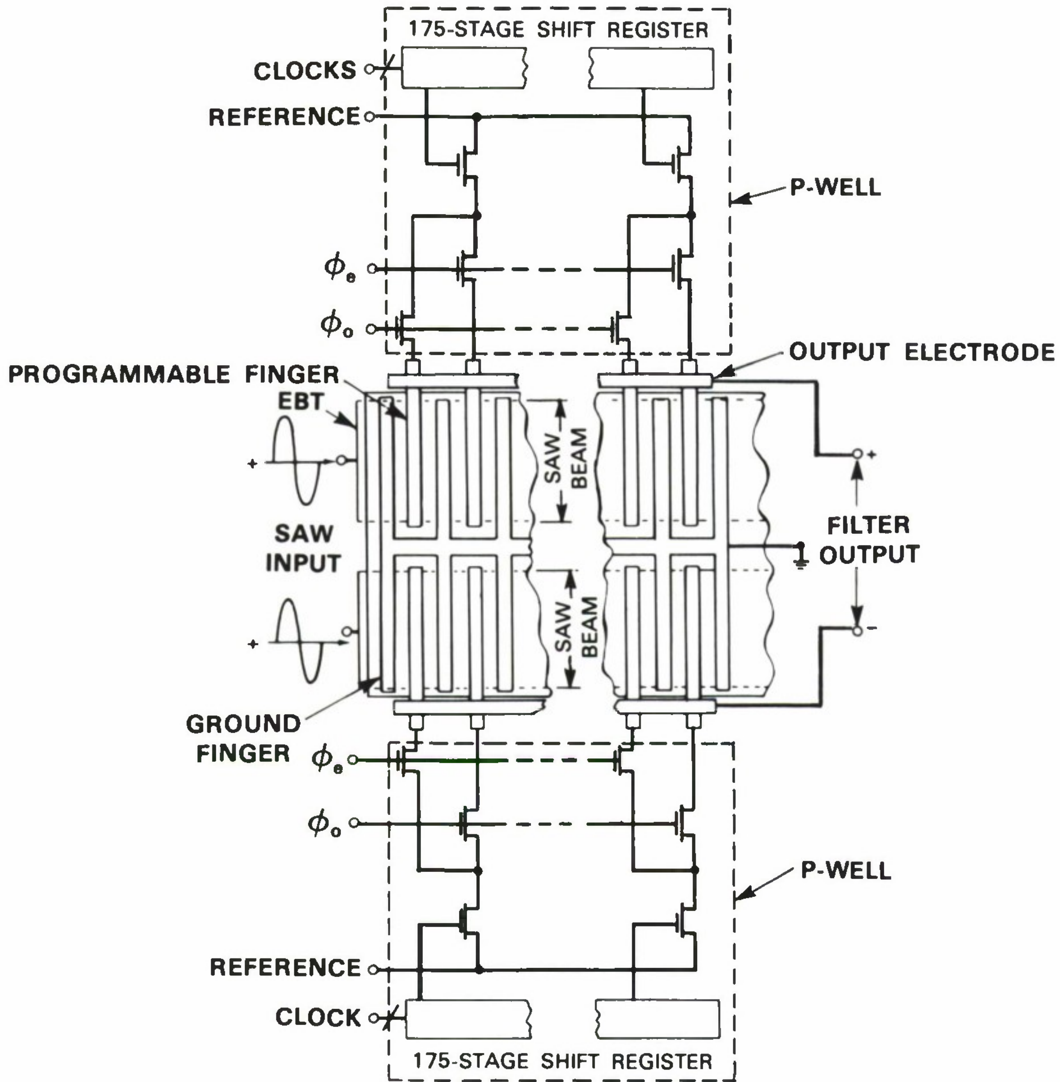

Figure 5-1. Schematic of 350-tap, 100-MHz-bandwidth SAW/FET, including the extra programming circuitry for 100-MHz-bandwidth operation. The p-well structure provides diode isolation from the substrate, allowing positive and negative programming voltages and serving to increase the programmable on/off ratio.

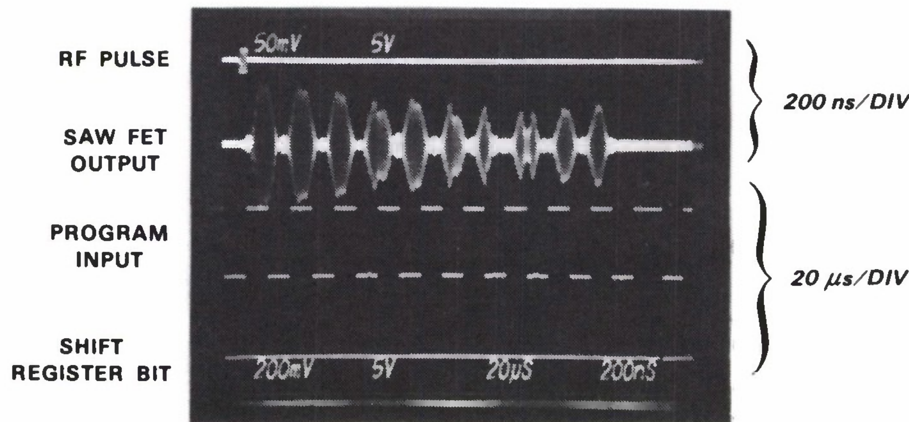

Figure 5-2. Response of 350-tap SAW/FET to a short burst of RF. The program input is a square wave which turns on and off alternating sets of 10 adjacent taps. Note different time scales for SAW/FET output and for program input.

Figure 5-3 shows the frequency response of the SAW/FET when programmed as a narrow-band filter. The sequence of four pictures shows results with four different programming inputs varying between 880 and 170 kHz from top to bottom, producing the expected passband, which varies from 130 to 212 MHz. The device clearly shows the 100 MHz of programmable bandwidth. The out-of-band rejection is seen to be approximately 25 dB except for a few isolated frequencies, at which higher spatial harmonics generated by the nonlinear relationship between programming voltage and tap weight are aliased about the 232-MHz sampling frequency and appear in band. The dynamic range over thermal noise is greater than 55 dB with a 27-dBm input signal.

The measured on/off ratio of 20 dB is lower than expected. Based on the resistivity of the Si substrate and assuming a planar capacitor, we expected a 10:1 variation in capacitance with a programming-voltage variation of six volts.[4] Our measurements, however, found a variation of only 4:1. This difference is a result of edge effects along the long and narrow (1.2-mm long by 3.5-μm wide) sampling fingers, giving a substantially larger than expected capacitance at a given bias voltage. Recent test results indicate that with higher resistivity substrate material we can obtain a 10:1 capacitance variation and thus reach 30-dB on/off ratio. Wafer fabrication with higher-resistivity silicon substrates is underway.

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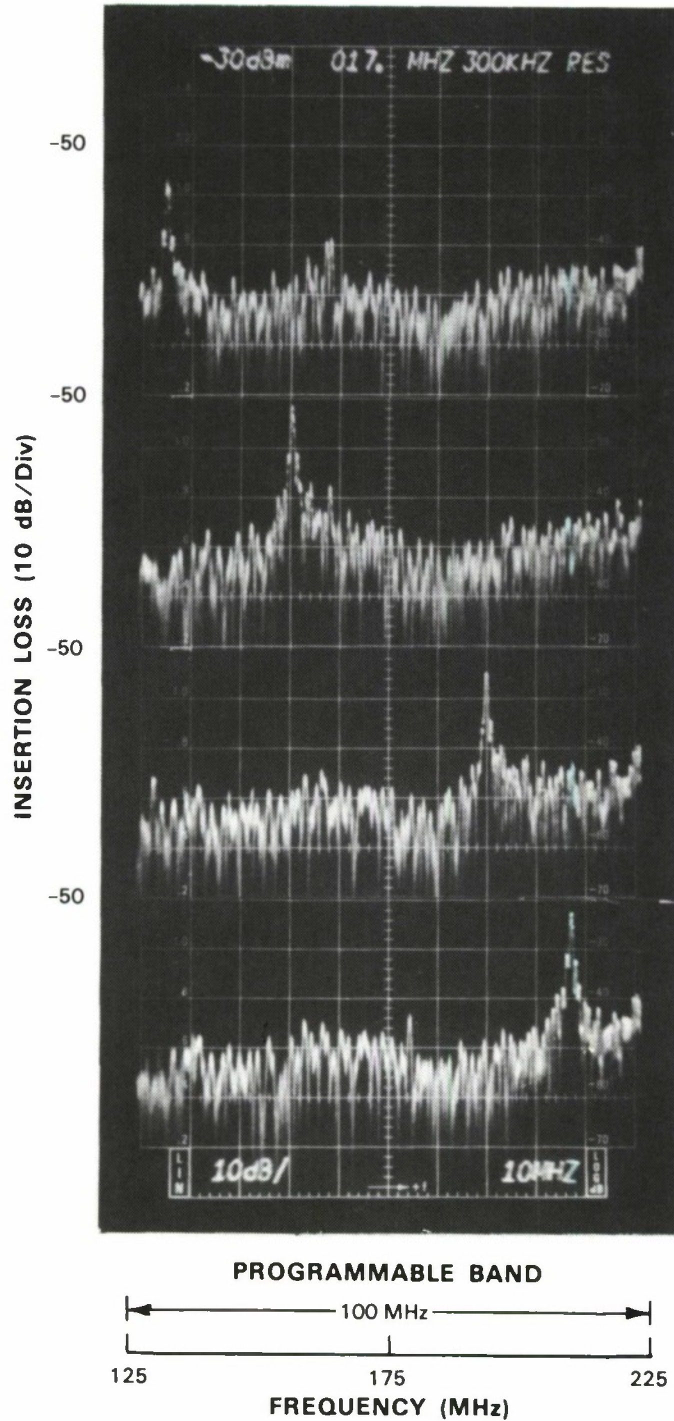

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Figure 5-3. Amplitude-vs-frequency response of 350-tap SAW/FET programmed as narrowband filter. Four different program inputs were used.

5.2 A COMPARISON OF NONLINEAR ASSOCIATIVE MEMORY AND MATCHED-FILTER PROCESSING FOR DETECTING LINES IN OPTICAL IMAGES

We have been studying the applicability of associative-memory-based pattern recognition techniques[5] to the problem of detecting lines in an optical image. We have carried out computer simulations to determine the probabilities of false alarm and missed detection using conventional two-dimensional matched filtering techniques as well as several versions of nonlinear associative memory (neural network) processing.[6] For our analysis we assumed that the object giving rise to the observed image is known to be one of a limited set of ideal patterns, which in this example are line segments oriented at specific angles or a uniform field. The image of the object, however, is corrupted by the addition of Gaussian noise. The processor attempts to determine which of the ideal objects gave rise to the observed image.

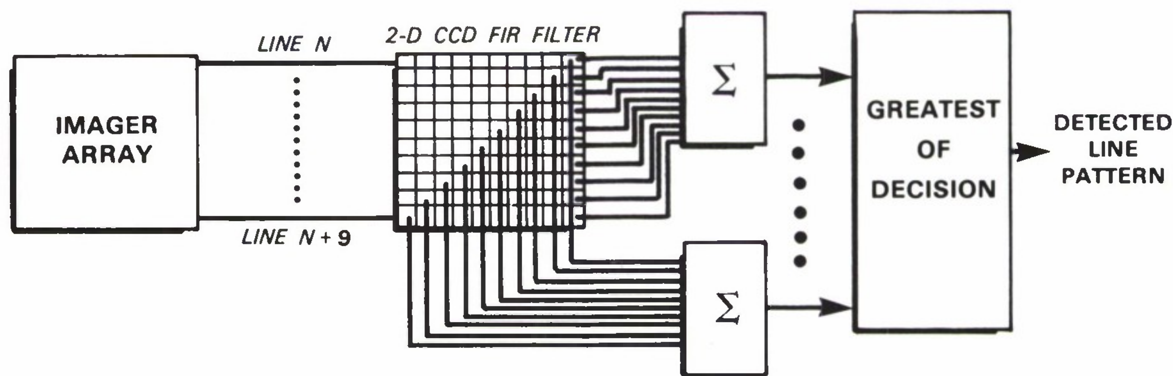

Figure 5-4. Near-focal-plane CCD-based two-dimensional matched filter.

Figure 5-4 shows an example of a near-focal-plane integrated circuit, based on charge-coupled device (CCD) storage and tapping, that can simultaneously carry out all of the two-dimensional matched filters needed to make the detection decision. For simplicity, the figure shows the tapping points to implement only two of the filters, one for lines oriented vertically and one for lines oriented at 45° to the vertical. As the image is clocked through the array, the matched filtering is performed for each possible position of the image relative to the filter templates.

For associative-memory processing, the two-dimensional image is mapped (using a raster scan format, for example) into a one-dimensional vector of pixel intensity values. In the linear associative (or correlation matrix) memory[7] the analog input state vector is multiplied by a stored matrix that is built from information related to the patterns which are to be recognized. After a single operation, the resulting output is a more accurate version of the true input pattern, i.e., one in which the noise has been reduced. The nonlinear associative memory[6] differs in several respects. First, the input vector has binary quantized components; second, the output vector from the linear multiplication by the memory matrix is binary quantized; and third, the output vector after each step is treated as an input vector and processed by the memory matrix again until a

stable state is reached. Ideally, this stable output pattern would correspond exactly to the true input pattern with noise removed. An analog integrated circuit based on MNOS/CCD techniques[8] has been designed to perform this processing.

The associative memory matrix was initially constructed, as described by Hopfield, directly from the actual vectors to be recognized:

$$\vec{M}_{ij} = \sum_k \vec{P}_i(k)\, \vec{P}_j(k) \tag{1}$$

where the vectors of the patterns are given by $\vec{P}^{(k)}$. Examples of two such vectors, drawn as 5×5 arrays, are shown in Table 5-1, row (a). The error rates with this approach were very much higher than those obtained with the corresponding two-dimensional matched-filter-bank processor using a maximum likelihood criterion (which selects the state corresponding to the filter with the largest output).

Since the Hopfield associative memory matrix made false identifications even when presented with perfect input patterns, we next investigated a memory matrix built using a technique that

TABLE 5-1

5-by 5 Input State and Orthogonal Basis Vectors for the Case of a Line Oriented at 45° to the Vertical and a Field Without an Object

	No Line Present					Line Present				
(a) Input State Vectors	-1	-1	-1	-1	-1	+1	-1	-1	-1	-1
	-1	-1	-1	-1	-1	-1	+1	-1	-1	-1
	-1	-1	-1	-1	-1	-1	-1	+1	-1	-1
	-1	-1	-1	-1	-1	-1	-1	-1	+1	-1
	-1	-1	-1	-1	-1	-1	-1	-1	-1	+1
(b) Mutually Orthogonal Basis Vectors [AM 1]	0	-1	0	-1	-1	+4	-1	-1	-1	-1
	-1	0	0	-1	-1	-1	+4	-1	-1	-1
	-1	-1	-16	-1	-1	-1	-1	+4	-1	-1
	-1	-1	0	0	-1	-1	-1	-1	+4	-1
	-1	-1	0	-1	0	-1	-1	-1	-1	+4
(c) Optimum Orthogonal Basis Vectors [AM 2]	-3.4	-0.4	-3.4	-0.4	-0.4	+4	-1	-1	-1	-1
	-0.4	-3.4	-3.4	-0.4	-0.4	-1	+4	-1	-1	-1
	-0.4	-0.4	-6.4	-0.4	-0.4	-1	-1	+4	-1	-1
	-0.4	-0.4	-3.4	-3.4	-0.4	-1	-1	-1	+4	-1
	-0.4	-0.4	-3.4	-0.4	-3.4	-1	-1	-1	-1	+4

guarantees perfect recognition of perfect patterns. Instead of building the association matrix from the actual state vectors $\vec{P}$, we used a set of basis vectors $\vec{B}^{(k)}$ that obeyed a special mutual orthonormality relationship to the $\vec{P}^{(k)}$ state vectors:

$$\vec{B}^{(k)} \cdot \vec{P}^{(j)} = \delta_{kj} \qquad (2)$$

where the dot indicates the inner product of the vectors and δ is the Kronecker delta function. If the $\vec{P}$ vectors are linearly independent, such a set of $\vec{B}$ vectors can always be found and (if the number of $\vec{P}$ vectors is less than their dimensionality) are not unique. Row (b) of Table 5-1 shows the set of basis vectors (the component values in the table are multiplied by 40 to make all values integers) chosen by inspection for a set of three patterns: a uniform field and a 45° line seen in the first row, and also a vertical line whose vector is not shown in Table 5-1. The association matrix was then taken as:

$$\vec{\vec{M}}_{ij} = \sum_k \vec{P}_i^{(k)} \vec{B}_j^{(k)} \quad . \qquad (3)$$

One can easily show that when a trial vector is presented that is precisely one of the $\vec{P}$ vectors, the result after multiplying by $\vec{M}$ is exactly the input vector. With this choice of association matrix, significantly better results were obtained.

Having achieved better results using one set of mutually orthogonal basis vectors, we proceeded to study how best to choose the vectors from the infinity of possible choices consistent with Equation 2. Specifically, we considered the amount of error in the output vector when the input vector was not precisely one of the state vectors $\vec{P}$. For a deviation $\overrightarrow{\Delta P}$ in the input vector, the deviation $\overrightarrow{\Delta S}$ in the output vector is given by

$$\overrightarrow{\Delta S} = \vec{M}\overrightarrow{\Delta P} \quad . \qquad (4)$$

Basis vectors were chosen to minimize the rms deviation $\overrightarrow{\Delta S}$ over a statistical distribution of input deviations. These optimal basis vectors are shown in row (c) of Table 5-1. The association matrix that was built to use these basis vectors turns out to be the optimal linear association matrix.[5] With this matrix, still better results were obtained.

Table 5-2 summarizes some of the results for 5 × 5 pixel fields of data based on three ideal input states: a line oriented vertically, a line oriented at 45°, and a field with no object. The input state vectors (ideal patterns) were represented using values of -1 and +1. The table shows the percentage of noisy patterns that were correctly and incorrectly identified when the per-pixel input signal-to-noise ratio was 6 dB. The column labeled AM1 shows results for a memory matrix built from a set of *ad hoc* mutually orthogonal basis vectors. The column labeled AM2 shows the results obtained using the optimum linear association matrix. The columns labeled MF are the results of the two-dimensional matched filter maximum-likelihood computation. In comparison, storing of the Hopfield association matrix, Equation 1, resulted in a 50 percent error rate.

With the matched filter analysis, only one type of error can occur: identifying the wrong pattern. The probability of this happening is a monotonically decreasing function of the distance between the states. When a line is present, the only likely error with the signal-to-noise ratio used

TABLE 5-2

Detection Probabilities (Percent) for Recognition of Angled Lines in Associative Memory (AM) and Matched Filter (MF) Processors

Input State Identified	Line Present			Line Not Present		
	AM 1	AM 2	MF	AM 1	AM 2	MF
Correct State	88.6	97.3	98.6	81.0	97.0	97.5
Wrong State	1.2	1.4	1.4	6.2	3.0	2.5
Spurious State	10.2	1.3	0.0	12.8	0.0	0.0

is misidentification of the uniform field, since the distance to the wrong line pattern is much farther. When no line is present, the matched filter error rate is approximately twice that what it would be if the line were present, as there is an equal probability of falsely detecting either of the two possible lines.

The associative memory calculation was found to exhibit a second type of error. Besides settling into wrong states, it can also settle into a spurious state, one that is not any of the ideal states but is a superposition of two of them. In the matched filter receiver, such ambiguities are resolved by comparing the relative amplitudes of the individual filter outputs. This kind of error becomes increasingly significant when one applies the analysis to a larger set of ideal patterns.

In summary, the simulations indicate that the matched filter approach provides both superior performance and a reduced computational cost. However, the matched filter structure requires maximum-likelihood detection to select the best match, while the associative memory simply iterates until a solution is reached. The associative memory is also expected to be more fault tolerant as a result of distributing its information storage over more memory cells.

We are presently extending this work to cover larger fields of data (9×9), larger numbers of stored patterns, and input data that represent an ideal object but with lateral shifts. In addition, we are investigating more sophisticated processing algorithms, such as non-binary nonlinearities (i.e., a "soft" limiter), variable thresholds, and noise injection into the association matrix.

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5.3 WIDEBAND CHIRP-TRANSFORM ADAPTIVE FILTER

Real-time adaptive filtering and spectral analysis are desirable functions for inclusion in the front end of a wideband receiver. Adaptive filtering improves reception by dynamically suppressing narrowband interferers. Spectral analysis provides information required to deploy other suppression resources. These functions can be provided by a chirp-transform system (CTS)[9,10] using surface-acoustic-wave (SAW) chirp filters.

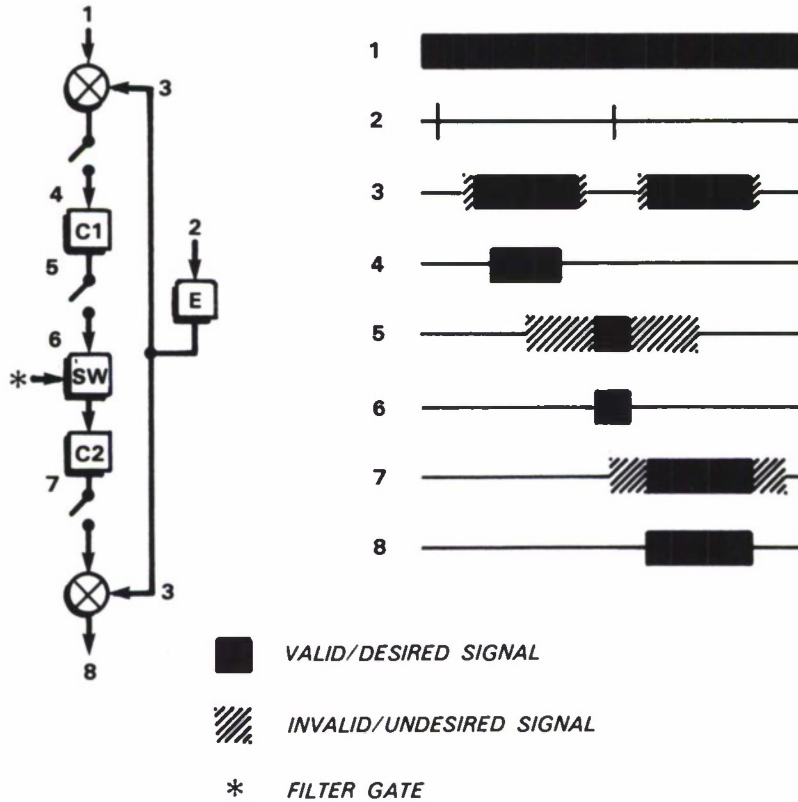

Figure 5-5. Chirp-transform adaptive filter and signal timing.

Figure 5-5 shows the basic elements and signal timing for a CTS structure sufficient for the adaptive filtering of an isolated segment of a continuous signal. When this segment is chirp modulated and passed through a chirp filter, its chirp-modulated Fourier transform is produced, which can be sampled for spectral analysis and time gated for narrowband excision. When this transform is passed through a second chirp filter, the chirp-modulated inverse transform of the segment is produced. Chirp demodulation then results in a filtered version of the input segment. Filtering, however, elongates the segment by approximately the inverse of the spectral notch width.

In the CTS structure of Figure 5-5 the chirps required for chirp modulation and demodulation are both generated by impulsing an 'expander' chirp filter denoted E. The impulse response

of the expander is long enough to demodulate the output segment, which is longer than the input segment due to filtering. Following chirp filter C1, the invalid signal preceding and succeeding the valid Fourier transform is gated away prior to chirp filter C2. Following C2 the invalid signal preceding and succeeding the inverse-transform output is gated away prior to chirp demodulation.

In continuous operation, contiguous signal segments are processed alternately between two channels and then reconstructed into a continuous signal. The segments, elongated by filtering, must be permitted to overlap on summation[11] or residual signal will remain around the segment boundaries.

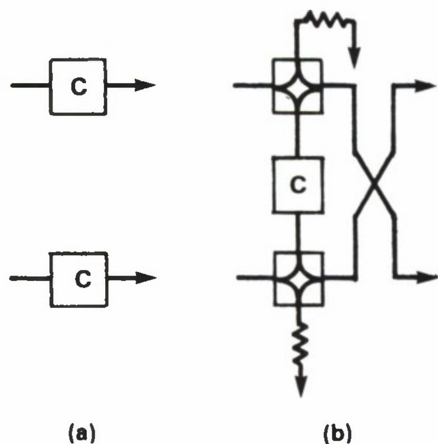

Figure 5-6. Chirp-filter channel pairs: (a) two filters; (b) bilateral operation with hybrid networks.

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A dual-channel adaptive filter requires one pair of devices for each chirp filter shown in the single-channel structure of Figure 5-5. Two separate devices or a single bilateral device[12] (Figure 5-6) can be used to realize each chirp-filter pair. For the bilateral structure [Figure 5-6(b)], each channel uses one of two possible signal-flow directions through a single device, with inputs and outputs timed and device delay chosen to prevent coincidence at each port. The bilateral structure is preferable to separate devices since fewer chirp filters are required and the channels are better matched, providing greater coherence for overlap summation and better tracking with time and temperature variations.

A system for the prefiltering of a 300-MHz-center-frequency minimum-shift-key (MSK) modulated 92.5 Mchip/s PN-coded signal prior to matched-filter detection and demodulation is currently under development. The goal is to provide greater than 30 dB narrowband suppression.

The system and device specifications are shown in Table 5-3. In the configuration of Figure 5-7, switches prior to the reflective-array-compressor (RAC) chirp filters C1 and C2 are used to minimize interference from coupler feedthrough to the low-level outputs, while switches following C1 and C2 prevent amplifier saturation by suppressing high-level coupler feedthrough. At the expander, class C amplifiers provide additional on/off isolation prior to the couplers, while high-level coupler feedthrough is suppressed using limiters. Each channel utilizes its own noncontiguous, nonoverlapping chirp stream. All switches are controlled by signals derived from a 430-MHz

TABLE 5-3

Adaptive-Filter Specifications

System		
Bandwidth	B	80 MHz
Minimum Notch Width	f_n	400 kHz
Output-Segment Overlap	$t_o = 1/f_n$	2.5 μs
Fractional Overlap	T_o/T	0.25
Input-Segment Duration	$T = 4T_o$	10 μs
Fourier Transform Duration	$T - T_o$	7.5 μs
Output-Segment Duration	$T + T_o$	12.5 μs
Fourier Transform Resolution	$1/T$	100 kHz
No. of Resolution Cells	TB	800
Transform Frequency/Time (Chirp Slope)	$B/(T - T_o)$	10.7 MHz/μs
System Delay	4T	40 μs

Device	**E**	**C1**	**C2**
Dispersion	12.5 μs	17.5 μs	20 μs
Bandwidth	133 MHz	187 MHz	213 MHz
Center Frequency	430 MHz	730 MHz	730 MHz
Ct. Freq. Group Delay	19 μs	20 μs	20 μs
Chirp Type	Down	Up	Down
Insertion Loss	40 dB	50 dB	50 dB
Weighting	x/sin(x)	Uniform	Uniform
Feedthru/Reflections	< -120 dB	< -90 dB	< -90 dB

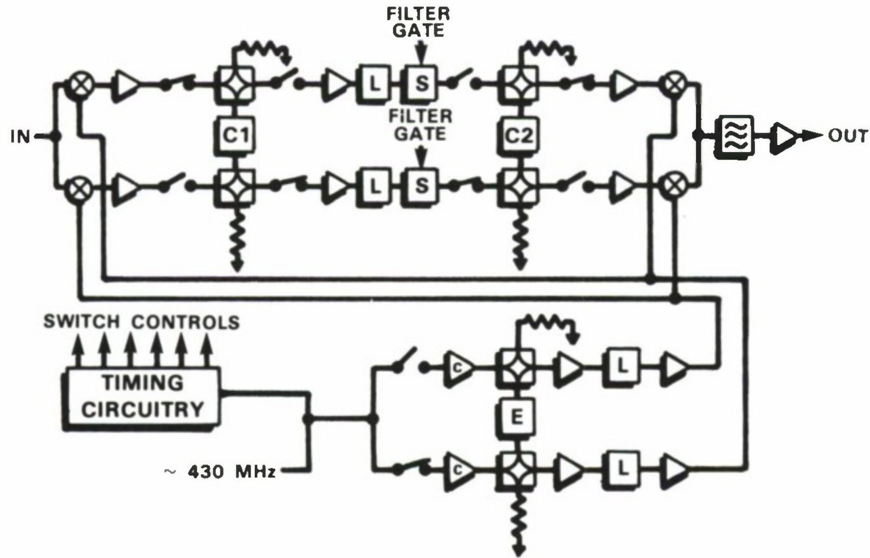

Figure 5-7. Chirp-transform adaptive filter.

(nominal) tunable oscillator, whose output is also gated for impulse generation. The system is calibrated by adjusting the frequency of the oscillator until chirp demodulation is properly aligned, which occurs simultaneously in the balanced channels.

Figure 5-8 shows the Fourier transform, in a single channel, for an MSK input in the top trace and the same MSK with a 295-MHz CW interferer, at a 20-dB interference-to-signal ratio, in the bottom trace. Both transforms possess 400-kHz-wide notches at 295 MHz and display the signal spectrum extending from 260 to 340 MHz, left to right. Residual of the spectral peak due to the CW interferer is shown in the bottom trace. This residual produces an output for each segment that is canceled by overlap summation of successive output segments. Figure 5-9 shows the continuous system output for an MSK input in the top trace and for an equal-level 295-MHz CW tone in the bottom trace. The MSK output is unaffected by filtering. However, the CW signal has been appreciably suppressed. Current narrowband suppression capability is in the 10 to 15 dB range. It is expected that improvements in device quality and system implementation will boost this performance to the 20 to 25 dB range and also improve the current 34 dB dynamic range.

An MSK signal was matched filtered with and without CW interference at an input interference-to-signal ratio of 20 dB. The matched-filter processing gain was about 20 dB. The results in Figure 5-10 were obtained without CTS adaptive filtering. In the bottom trace the CW interference overwhelms the correlation spike seen without interference in the top trace. The results of Figure 5-11 were obtained with CTS adaptive preprocessing of the matched-filter input (see the transforms in Figure 5-8). The interference exhibited in Figure 5-10 has been appreciably reduced in Figure 5-11.

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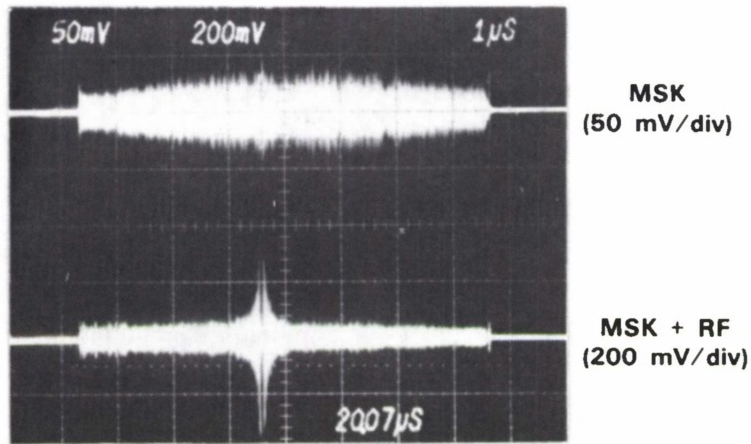

Figure 5-8. Notched Fourier transforms — single channel.

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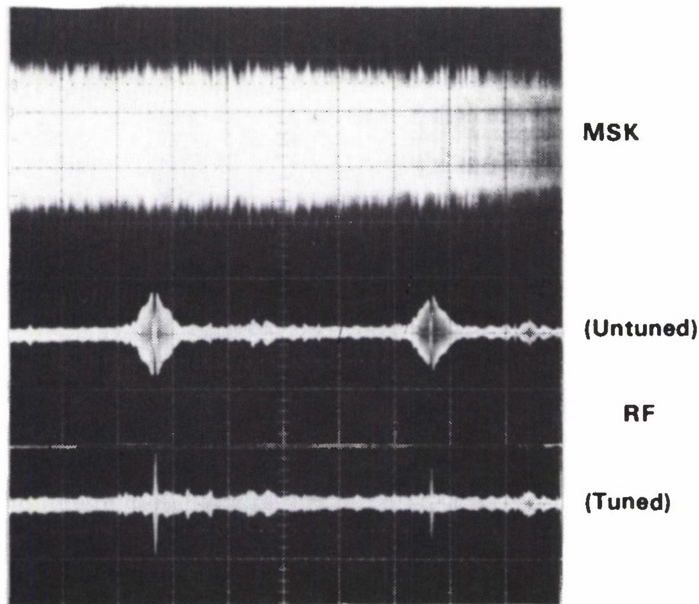

Figure 5-9. System outputs for MSK (top trace) and CW interference (bottom trace) at equal levels at system input.

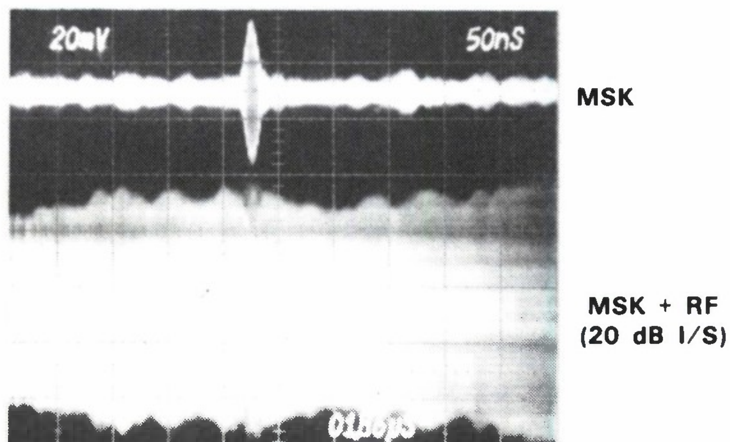

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Figure 5-10. Matched-filter outputs without adaptive preprocessing: top trace — MSK input only; bottom trace — MSK with added CW interference.

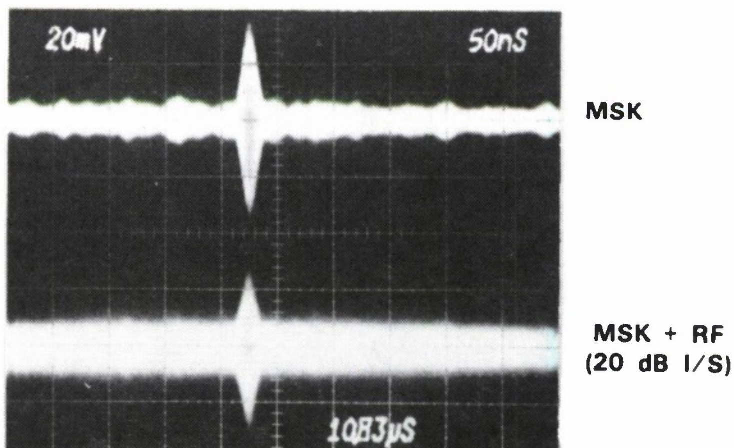

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Figure 5-11. Matched-filter outputs with adaptive preprocessing: top trace —MSK input only; bottom trace — MSK with added CW interference.

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20. ABSTRACT *(Continue on reverse side if necessary and identify by block number)*

This report covers in detail the solid state research work of the Solid State Division at Lincoln Laboratory for the period 1 November 1985 through 31 January 1986. The topics covered are Solid State Device Research, Quantum Electronics, Materials Research, Microelectronics, and Analog Device Technology. Funding is primarily provided by the Air Force, with additional support provided by the Army, DARPA, Navy, SDIO, NASA, and DOE.

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