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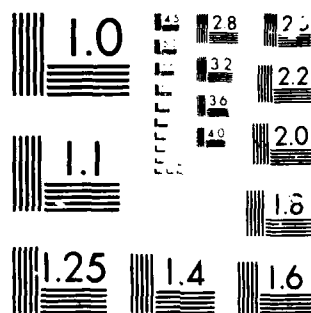
AUTOMATED TESTING AND FAULT ISOLATION OF A LOW
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AUTOMATED TESTING AND FAULT ISOLATION
OF A LOW FREQUENCY ANALOG CIRCUIT
CARD ASSEMBLY

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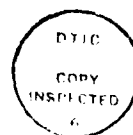
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ABSTRACT

This thesis describes the automated testing and fault isolation which is performed on a Circuit Card Assembly (CCA) used in a complex naval weapons system. The automated testing is performed using a Hewlett Packard 9826 computer and IEEE-488 bus compatible equipment which comprise the Test Set known as the TE304. A complete circuit analysis of the CCA being tested is included in this thesis as well as program descriptions of the Acceptance Test Program and the Fault Isolation Program. Also included in this thesis is background information on the TE304 Automated Test Set, the equipment which make it up, and the software which is used to control it. This thesis was made possible through a U. S. Navy contract between the University of Louisville Electrical Engineering Department and the Naval Ordnance Station in Louisville.

TABLE OF CONTENTS

Page

APPROVAL PAGE	ii
ACKNOWLEDGEMENTS	iii
ABSTRACT	iv
TABLE OF CONTENTS	v
LIST OF TABLES	ix
LIST OF ILLUSTRATIONS	x
I. INTRODUCTION.....	1
II. INSTRUMENTATION AND HARDWARE	4
A. TE304 Automated Test Set	4
B. Interface Adapter Hardware	6
III. CIRCUIT ANALYSIS	13
A. Continuity Tests	13
B. Current Demand	13
C. Voltage Regulator Circuit (TIM)	14
D. AC and DC Gain Tests	15
1. VBM DC Gain	15
2. VBM AC Ripple Gain (1 Hz)	16
3. VBM AC Ripple Gain (10 Hz)	18
4. VBM AC Ripple Gain (1 Hz)	19
5. IFKT DC Gain	21
6. IFKT AC Ripple Gain (1 Hz)	22
7. IFKT AC Ripple Gain (10 Hz)	24
8. IFKT AC Ripple Gain (1 Hz)	25
9. IFMT DC Gain	26
10. IFMT AC Ripple Gain (1 Hz)	27
11. IFMT AC Ripple Gain (10 Hz)	29
12. IFMT AC Ripple Gain (1 Hz)	30
E. DC Threshold Test	32
1. VBMH Threshold Input Voltage	32
2. IFKL Threshold Input Voltage	36
3. IFKH Threshold Input voltage	41
4. IFML Threshold Input Voltage	44

5.	IFMH Threshold Input voltage	49
F.	IFKL TTL Output Tests	52
1.	IFKL TTL Output (21260)	52
2.	IFKL TTL Output (21270)	53
G.	Full Power CDC(-) and FPD Logic	54
H.	5 Minute and 250 Msec Timers	56
1.	U1 Timer Circuit	56
2.	P2-11/35 Input Circuit	58
3.	Q7/Q8 Circuit	58
4.	U2 Timer Circuit	59
I.	20 Second Timer	63
1.	U3 Timer Circuit	63
2.	P2-12 Output Circuit	65
J.	1.5 Second Timer	66
1.	U25 Timer Circuit	69
K.	Power On Sequence Logic	72
1.	P2-1 Input Circuit	72
2.	Flip Flop Circuit	73
3.	P2-13 Output Circuit	76
4.	P2-37/38 Output Circuit	78
IV.	ACCEPTANCE TEST PROGRAM DESCRIPTION	81
A.	Program Header and Initial Conditions ...	81
B.	Patchbox Identification Check	82
C.	Continuity Tests	83
D.	Current Demand Tests	84
E.	Patchbox Circuit Check	85
F.	TIM Reference Voltage	85
G.	AC/DC Gain Tests	87
H.	DC Threshold Tests	88
I.	TTL Output Tests	89
J.	Full Power CDC/FPD Logic Test	89
K.	Power On Sequence Logic Test Part 1	90
L.	5 Minute and 250 msec Timers	92
M.	1.5 Second Timer Test	93

N.	Power On Sequence Logic Test Part 2	95
O.	20 Second Timer Test	95
V.	FAULT ISOLATION TEST PROGRAM DESCRIPTION	97
A.	Overview	97
B.	Voltage Regulator Circuit	99
C.	VBMT, IFKT, and IFMT Op Amp Circuits	100
D.	Comparator Circuits	102
E.	Full Power CDC/FPD Logic Circuits	104
F.	Power on Sequence Logic Tests	106
G.	U1 Timer Circuit	107
H.	U2 Timer Circuit	109
I.	U3 Timer Circuit	110
J.	U25 Timer Circuit	111
K.	P2-11/35 Input Circuit	112
L.	Q7-Q8 Transistor Circuit	113
M.	P2-12 Output Circuit	114
N.	P2-1 Input Circuit	115
O.	P2-13 Output Circuit	116
P.	P2-37/38 Output Circuit	118
Q.	Flip Flop Circuit	119
R.	Pulse Train Input Test	120
S.	Patchbox Adapter Circuit	121
	CONCLUSIONS	123
	BIBLIOGRAPHY	124
	APPENDIX A. ACCEPTANCE TEST REQUIREMENTS	126
	APPENDIX B. FAULT ISOLATION TEST REQUIREMENTS	137
	APPENDIX C. SCHEMATIC DIAGRAMS OF THE CCA	147

APPENDIX D. PATCHBOX WIRING LAYOUT AND ADAPTER CIRCUIT	173
APPENDIX E. FAULT ISOLATION FLOWCHARTS	178
APPENDIX F. ACCEPTANCE TEST PROGRAM	202
APPENDIX G. FAULT ISOLATION PROGRAM	214
VITA	262

	LIST OF TABLES	Page
TABLE I	TE304 EQUIPMENT LIST AND SPECIFICATIONS ..	9
TABLE II	FLIP FLOP CIRCUIT TRUTH TABLE	77
TABLE III	FLIP FLOP CIRCUIT, P2-13 OUTPUT CIRCUIT, AND CONTROLLING INPUTS TRUTH TABLE	77
TABLE IV	P2-37/38 OUTPUTS CIRCUIT TRUTH TABLE	79
TABLE V	PATCHBOX ADAPTER CIRCUIT TEST DESCRIPTIONS	86
TABLE VI	PATCHBOX JUMPER WIRE LIST	174

LIST OF ILLUSTRATIONS

FIGURE		Page
1	VBMH Comparator Triggering Window	34
2	IFKL Comparator Triggering Window	39
3	IFKH Comparator Triggering Window	43
4	IFML Comparator Triggering Window	47
5	IFMH Comparator Triggering Window	51
6	555 Timer Block Diagram	61
7	Test Series 31000 Timing Diagram	62
8	The Voltage At Node 2	68
9	A Portion of the Flip Flop Circuit	75
10	A Portion of the Flip Flop Circuit	75
11	CCA Schematic Part 1	148
12	CCA Schematic Part 2	149
13	CCA Parts Layout	150
14	Computer Generated Parts Layout (Quadrant 1) .	151
15	Computer Generated Parts Layout (Quadrant 2) .	152
16	Computer Generated Parts Layout (Quadrant 3) .	153
17	Computer Generated Parts Layout (Quadrant 4) .	154
18	Voltage Regulator Circuit	155
19	VBMT Op Amp Circuit	156
20	VBMH Comparator Circuit	157
21	IFKT Op Amp Circuit	158
22	IFKL Comparator Circuit	159
23	IFKH Comparator Circuit	160

FIGURE		Page
24	IFKL TTL Output Circuit	161
25	IFMT Op Amp Circuit	162
26	IFML Comparator Circuit	163
27	IFMH Comparator Circuit	164
28	Full Power CDC/FPD Logic Circuits	165
29	U1 Timer and P2-11/35 Input Circuits	166
30	U2 Timer and Q7/Q8 Transistor Circuits	167
31	U3 Timer and P2-12 Output Circuits	168
32	U25 Timer Circuit	169
33	Flip Flop and P2-1 Input Circuits	170
34	P2-13 Output Circuit	171
35	P2-37/38 Outputs Circuit	172
36	Patchbox Adapter Circuit	177
37	Voltage Regulator Circuit FI Flowchart	179
38	VBMT Op Amp Circuit FI Flowchart	180
39	VBMH Comparator Circuit FI Flowchart	181
40	IFKT Op Amp Circuit FI Flowchart	182
41	IFKL and IFKH Comparator Circuits FI Flowchart	183
42	IFMT Op Amp Circuit FI Flowchart	185
43	IFML and IFMH Comparator Circuits FI Flowchart	186
44	Full Power CDC/FPD Logic Circuits FI Flowchart	188
45	U1 Timer Circuit FI Flowchart	190
46	U2 Timer Circuit FI Flowchart	191
47	U3 Timer Circuit FI Flowchart	192
48	U25 Timer Circuit FI Flowchart	193

FIGURE		Page
49	P2-11/35 Inputs Circuit FI Flowchart	194
50	Q7/Q8 Transistor Circuit FI Flowchart	195
51	P2-12 Output Circuit FI Flowchart	196
52	P2-1 Input Circuit FI Flowchart	197
53	P2-13 Output Circuit FI Flowchart	198
54	P2-37/38 Outputs Circuit FI Flowchart	199
55	Flip Flop Circuit FI Flowchart	200
56	U24 Input Pulse FI Flowchart	201

I. INTRODUCTION

The purpose of this thesis is to develop software and hardware needed for automated testing and fault isolation of an analog circuit card assembly (CCA) which is used in a complex naval weapons system. The automated testing is accomplished using a Hewlett Packard 9826 desktop computer and various other electronic instrumentation which is controlled via the IEEE-488 interface bus. The U. S. Naval Ordnance Station in Louisville, Kentucky, (NOSL) has been involved with maintenance and overhaul of many types of weapons systems. The system from which this circuit card came contains some 80 analog circuit cards which are tested and repaired individually by the Production Engineering department at NOSL. The work for this thesis project has been made possible through a contract awarded to the University of Louisville Speed Scientific School by the NOSL.

Test Requirements (TR) for each CCA are set forth by the Naval Sea Systems Command (NAVSEA) and are known as the Acceptance Test for that CCA. The Acceptance Test TR for the circuit card used in this thesis is contained in APPENDIX A. These Acceptance Tests are performed on a number of Test Equipment Sets (TE) depending on what type of circuit card is being tested: low frequency analog, digital,

high power, or high frequency analog. Before any testing of the CCA's can be performed, a complete circuit analysis of the CCA must be accomplished. Schematic diagrams of the CCA to be tested are contained in APPENDIX C.

A hardware interface which is needed as a communication link between the CCA and the TE is designed next and built into a patchbox which is part of the TE. This interface hardware consists primarily of patchcords which are plugged into the patchbox and provide the necessary connections, by means of a switching matrix, between the instrumentation and the circuit card. Some adapter circuitry is also used in the patchbox which aids in performing certain types of tests that the instrumentation cannot perform directly. The schematic layout of the patchbox and adapter circuit can be found in APPENDIX D.

The writing of the software needed to perform the Acceptance Test and if any failures occur, the Fault Isolation Test, is the last task to be accomplished. This software uses subprograms, which have been developed as part of the TE operating system, to control the different instrumentation on the IEEE-488 interface bus. The language used for the HP 9826 computer is HP Basic 3.0 which is a high level operating system incorporating different aspects of BASIC, FORTRAN, and PASCAL. Because the TE used for this project is highly automated, very little operator intervention is needed during testing of the CCA. Fault

isolation procedures and tests must also be derived before developing the software for the Fault Isolation Test (FI). A complete listing of the Acceptance and Fault Isolation Test Programs is contained in APPENDIX F and G, respectively.

The completion of this project and the other Circuit Card Assemblies is a key part in the goals of the Production Engineering department at the NOSL. Prior work performed by University of Louisville students in this area follow basically the same procedures that were mentioned above. The TE's used in these projects were not totally automated and required much operator intervention which increased both productivity time and the possibility of mistakes. The software needed for the Acceptance and Fault Isolation Test of this project was developed on a new, almost totally automated TE, TE304, which was developed and built by NOSL Production Engineering in 1985. All future testing of analog CCA's will be done on this new system which will both speed up production and produce a higher-quality product.

II. INSTRUMENTATION AND HARDWARE

A. TE304 Automated Test Set

NOSL has been testing and repairing the analog circuit card assemblies (CCA) since 1982. Early Fault Isolation TE's were comprised of limited stimulus and measurement equipment and used a cumbersome patchcord jumper box which had to be operated manually. These systems were nicknamed the "Benchtops" because the operator actually sat at a bench while performing the tests on the CCA's. A Hewlett Packard 9826 desktop computer was the controlling device for these systems, but due to a primitive software system, was limited in setting up the equipment and taking readings. No switching matrix was available to interface the CCA to the equipment. The equipment and interfacing circuits had to be connected to the CCA through the patchcord jumper box using numerous banana-jack patchcords. The software written for the CCA acceptance and fault isolation tests would instruct the operator when and where to connect these patchcords. This type of system slowed down production rates and also increased the possibility of operator errors.

The TE8009 is an automated test set built by a major defense contractor which is also the main supplier of the CCA's. This test set is used for running the Acceptance

Test on low frequency analog CCA's as were the Benchtop TE's. However, the contractor does not provide any software for fault isolation tests on the CCA's; this was the main reason for developing the Benchtop program. The TE8009 was both extremely expensive and complicated due to a vast amount of custom hardware that was used in the test set. Very little of the equipment in the TE8009 was "off the shelf" equipment which made repair or replacement difficult.

The engineers who made up the Benchtop program have since designed and built a new almost totally automated test set which is now called the TE304 at a fraction of the cost it took to build the TE8009. This test set uses primarily Hewlett Packard equipment and equipment which is IEEE-488 bus compatible, all of which are "off the shelf". The controlling device is again the HP9826 desktop computer; however, a completely new array of software has been developed. It consists of an operating system, subprograms which make it easy to set up the equipment and take measurements, and various other programs and subprograms used by the TE304. The equipment which makes up the TE304 and the performance specifications for each are listed in TABLE I.

The software which was developed for the TE304 was a tremendous improvement over earlier systems. Subprograms were written which made it possible to set up the equipment and take measurements by using one subprogram call

statement. By changing the parameter list in the call statements, it is possible to configure the equipment in any number of operating modes. Because the programmer no longer has to use the long and complicated instrument command strings, writing and debugging CCA test software was made much easier. Software was also developed for system use by the Test Set operator. This software created a standardized method of running CCA tests, recording the data, and also helped perform TE maintenance and calibration checks.

B. Interface Adapter Hardware

As mentioned in the previous section, the TE304 uses a Patchbox and Switching Matrix to provide the proper connections between the CCA connector pins and the test equipment. However some circuitry is required to interface the signals between the CCA and the TE. This hardware is built onto a small wire-wrapped plug board and mounted in the Patchbox. Because the TE's are very versatile, little interface circuitry is needed. Only four load resistors are required for the CCA done in this thesis; the other required pullup resistors are supplied by the Digital Read Cards in the HP Multiprogrammer. The only other circuitry needed is a single 7408 quad AND gate which is used to protect the Digital Write Card from receiving any damaging voltages due to a bad CCA. One gate on this AND chip is used to control the triggering on one of the CCA's 555 timers. A noise

suppression capacitor is added across the IC power supply leads for protection. A complete schematic of the interface adapter circuit along with the physical layout of the Patchbox is contained in APPENDIX D.

The remaining interface hardware consists of many patchcords that are permanently plugged into the Patchbox. These jumpers connect the TE and CCA signals to the matrix points or directly to the CCA as in the case of the power supplies. The connections are fairly arbitrary as long as the equipment needed for a certain test can be connected to the CCA through the Switching Matrix. For a board of this size however, this requires careful planning of the wire layout and efficient use of equipment. Two additional resistors are added to the Patchbox between the Measurement Matrix points 98, 99, and 100 for use as a software patchbox identification check which is run at the beginning of each test.

The Stimulus Matrix (20 x 60 matrix points) is most useful for general connections of stimulus and measurement equipment to the CCA. Most of the TE is connected to the 20 lines of one side of the matrix while the many CCA pins and test points are connected to the 60 lines on the other side of the matrix. Additional measurements are made by using the Measurement Matrix (4 x 100). The four lines on one side of this matrix (A, B, C, and D) are connected to the Hi, Low, Sense Hi, and Sense Low inputs of the HP3497

Digital Multimeter. The Coaxial Matrix (16 x 20) is needed for CCA pins that are of coaxial output or input and for stimuli that is of higher frequency. A complete list of the patchbox jumpers is contained in APPENDIX D.

TABLE I

TE304 EQUIPMENT LIST AND DESCRIPTIONS

STIMULUS EQUIPMENT

- A. HP 3325A Function Generator
 - 1. sine wave : 0.000001 Hz to 20999999.9 Hz
 - 2. square wave : 0.000001 Hz to 10999999.9 Hz
 - 3. triangle wave : 0.000001 Hz to 10999.9 Hz
 - 4. pos./neg. ramp : 0.000001 Hz to 10999.9 Hz
 - 5. frequency resolution : 1 uHz for freq<100kHz
1 MHz for freq>100kHz
 - 6. frequency accuracy : $\pm 5 \times 10^{-6}$ of value
 - 7. amplitude range : 4 mVpp to 40 Vpp @ $\pm 2\%$
- B. HP 8116A Pulse/Function Generator
 - 1. frequency range : 1 MHz to 50 MHz
 - 2. frequency accuracy : 1 MHz-99.9 kHz $\pm 3\%$
100 kHz-50 MHz $\pm 5\%$
 - 3. duty cycle (sine, triangle, square)
range: 10% to 90% (1 MHz to 999 kHz)
20% to 80% (1 MHz to 9.99 MHz)
 - 4. pulse width : 10 ns to 999 ms $\pm 5\%$
 - 5. amplitude range : 7.95 Vdc @ $\pm 0.5\%$
- C. HP 8112A Pulse Generator
 - 1. frequency range : 1 Hz to 50 MHz
 - 2. pulse period : 20 ns to 950 ms @ $\pm 5\%$
 - 3. delay steps : 75 ns to 950 ms @ $\pm 5\%$
 - 4. double pulse : 20 ns to 950 ms @ $\pm 5\%$
 - 5. width : 10 ns to 950 ms @ $\pm 5\%$
 - 6. duty cycle : 1% to 99% @ $\pm 10\%$
 - 7. amplitude range : 0.2 to 32 Vdc @ $\pm 3\%$
- D. Elgenco 602A Gaussian Noise Generator
 - 1. ranges : 20 kHz, 500 kHz, 5 MHz
@ 1 dB, 2.5 dB, and 2.5 dB
 - 2. amplitude range : 0 to 5 Vrms
 - 3. output impedance : 900 ohms $\pm 10\%$
- E. ILC Data SR-460 Synchro/Resolver Simulator
 - 1. angular range : 0 - 353.9 deg resol. .01 deg
 - 2. accuracy : $\pm .01$ deg open, $\pm .03$ deg w/ load
 - 3. signal output : 11.8, 26, or 90 Vac
 - 4. reference : 26 or 115 Vac @ $\pm 3\%$

TABLE I (continued)

- F. Zi Tech 9811 Programmable Resistance Unit
 - 1. resistance range : 1 ohm to 1.5 Megohm
 - 2. accuracy : 0.1 %
 - 3. resolution : 1 ohm
 - 4. power rating : 1 Watt
- G. HP 69321B Digital to Analog Output Card
 - 1. used with HP 6940B Multiprogrammer
 - 2. amplitude range : -10.24 to 10.235 Vdc, +/-5 mv
 - 3. step range : 5 mVdc
- H. HP 69331B Digital Output Card
 - 1. used with HP 6940B Multiprogrammer
 - 2. TTL low output : 0 to 0.4 Vdc
 - 3. TTL high output : 4.75 to 5.25 Vdc
 - 4. max. current sink : 40 mA
 - 5. 12 separate outputs
- I. HP 69332A Open Collector Output Card
 - 1. used with HP 6940B Multiprogrammer
 - 2. low output : 0 to .7 Vdc
 - 3. high output : +30 Vdc max.
 - 4. max. current sink : 40 mA
 - 5. 12 separate outputs

Measurement Equipment

- A. HP 1980B Oscilloscope
 - 1. bandwidth : 100 MHz
 - 2. sweep delay : 0 to 9.9 sec., resol. 5 digits
 - 3. timebase : 5 ns/div to 1 sec/div, @ 3 digits
- B. HP 5335A Frequency Counter
 - 1. range : DC to 100 MHz
 - 2. additional functions : period, time AB, pulse width, duty cycle, slew rate, phase AB, tot. A
- C. HP 3457A Digital Multimeter
 - 1. DC voltage range : 30 mV to 300 V
 - 2. AC voltage range : 30 mV to 300 V
 - 3. resistance range : 3 ohm to 3 Gohm
 - 4. DC current : 300 mA to 1.5 A
 - 5. AC current : 30 mA to 1 A
- D. HP 69431A Digital Input Card
 - 1. used with HP 6940AB Multiprogrammer
 - 2. low input : 0 to .8 Vdc
 - 3. high input : 2 to 5 Vdc
 - 4. max. current sink : 6 mA
 - 5. 12 separate inputs

TABLE 1 (continued)

- E. HP 69422A Analog to Digital Input Card
 - 1. used with HP 6940B Multiprogrammer
 - 2. input ranges : ± 10 Vdc, ± 1 Vdc, ± 100 mVdc
 - 3. input resolution : 5 mV, 500 μ V, 50 μ V
 - 4. output resolution : 12 bits

Power Equipment

- A. HP 6034A DC Power Supply (6)
 - 1. voltage range : 0 to 60 Vdc
 - 2. current range : 0 to 10 A
 - 3. resolution : voltage-15 mV, current-2.5 mA
- B. Kepco PRM 28-7 28 Volt Power Supply
 - 1. voltage : 28 Vdc
 - 2. current : 7 A

Accessory Equipment

- A. Quantum Data CAT2000 Automatic Screwdriver
 - 1. backlash : none
 - 2. torque : 0 to 15 ounces inches
 - 3. step : 12,800 steps/revolution
 - 4. velocity : 2 to 1800 degrees/second

A.D. Data Inc. MC56-111583C Switching System

- A. Switching Control Unit
 - 1. ANSI/IEEE standard 488-1978 compatible
 - 2. one IEEE-488 address
 - 3. independent control of each sub matrix
- B. Measurement Matrix
 - 1. 4 x 100 configuration
 - 2. signals < 1 MHz
- C. Stimulus Matrix
 - 1. 20 x 60 configuration
 - 2. signals < 1 MHz
- D. Coaxial Matrix
 - 1. 20 x 16 configuration
 - 2. signals < 50 MHz
- E. Relay Specifications
 - 1. reed contacts
 - 2. initial contact resistance : < .11 ohms
 - 3. end life contact resistance : < .31 ohms
 - 4. life expectancy : > 10 million (rated load)
 - 5. DC breakdown : 200 Vdc

TABLE I (continued)

- 6. maximum current : 0.5 A
- 7. maximum voltage 200 Vdc

Control Hardware

- A. HP 9826 Computer
 - 1. 2 additional HP 98256A 256K RAM cards
 - 2. 1 additional HP 98624A IEEE-488 Bus card
 - 3. 7 inch CRT
 - 4. 5.25 inch flexible disc drive
 - 5. keyboard : ASCII character set, numeric keypad,
ten softkeys
 - 6. 68000 16 bit processor
- B. HP 9133L Winchester Disc Drive
 - 1. memory range : 40 Megabyte
 - 2. ANSI/IEEE-488 compatible
 - 3. 3.5 inch double density micro floppy disc drive
- C. HP 2934A/W Printer
 - 1. dot matrix printer
 - 2. ANSI/IEEE-488 compatible
 - 3. 200 characters per second (bi-directional)

III. CIRCUIT ANALYSIS

A. Continuity Tests

There are 16 continuity tests performed on the CCA during the Acceptance Test. All but two of these tests simply check continuity between two CCA connector pins which are tied together by wire lands on the circuit board. The other two tests measure 12 kohm identification resistors which are mounted between two connector pins on the CCA.

The only circuit analysis needed for this series of tests consists of analyzing the CCA wire lands and/or the two identification resistors for defects. During the Fault Isolation Program the TE operator is instructed to have the resistors replaced if they fail. The tolerances set forth by the TR allowed for these measurements are: 1 ohm maximum for the wire lands and plus or minus 1 kohm for the two resistors.

B. Current Demand

The CCA being tested here requires three DC power supplies: a 28-volt source, a 5-volt source, and a -5-volt source. The amount of current drawn from each of these power supplies varies according to what state of the many logic circuits on the CCA. Analysis needed to determine the total amounts of current drawn from each supply would

require a complete chapter in itself but is not required for this project. For the purposes of this CCA and the tolerances set forth by the Naval Sea Systems Command (NAVSEA) in the TR, the current drawn from each supply was determined from nominal readings taken from several good CCA's. The maximum allowable currents are approximately 10% higher than these nominal readings and are 230 mA for the 28 volt supply, 450 mA for the 5 volt supply, and 60 mA for the -5 volt supply.

C. Voltage Regulator Circuit (TIM)

Test number 20010 is the first test measurement to be made once the power has been applied to the CCA. This measurement is taken from a 5.1 volt zener diode, VR16, which is part of the voltage regulator circuit shown in FIGURE 18 of APPENDIX C. This circuit provides several reference voltages for other circuits on the CCA such as the comparator circuits.

A constant current of approximately 5 mA is maintained by the transistor Q41 which determines the reference voltages across the resistor branch of R150, R151, R153, and R154. The 5.1 volt zener diode VR16 maintains the voltage at CCA connector pin P2-27 which is where the measurement for test number 20010 is taken. The tolerances allowed for this reading by the TR are plus or minus 30% which is too high for this circuit. The normal tolerances

for a zener of this type, as shown in any standard data book, are plus or minus 20%. The actual voltage readings taken at the various reference points in the circuit are given on the schematic and are accurate for a 5 mA current flowing through the resistor branch mentioned above.

D. AC and DC Gain Tests

1. Test Number 21010 : VBMT DC Gain

The circuit for this test is shown in FIGURE 19 located in APPENDIX C. U21 is a 747 operational amplifier IC which is used as a Lossy Integrator and/or a Low Pass Filter. This test simply checks the DC gain of the amplifier using an input voltage of 12.5 volts DC. The voltage at the non-inverting input (pin 6) can be found using the formula for the voltage divider network consisting of R133, R134, the 5.1 vdc source, and the 12.5 vdc input voltage.

$$\begin{aligned} V(+) &= [12.5(R134)+5.1(R133)]/[R133+R134] \\ &= [(12.5*15000)+(5.1*150000)]/[15000+150000] \\ &= 5.77 \text{ vdc.} \end{aligned}$$

Because this test only involves DC analysis, the capacitors in the circuit can be ignored. The output voltage of U21 (pin 10) can be obtained directly from the standard op-amp equation used for a non-inverting amplifier.

$$\begin{aligned}
 V_o &= v(+)[1+(R131/R132)] \\
 &= 5.77*[1+(15/150)] \\
 &= 6.35 \text{ vdc.}
 \end{aligned}$$

If the output voltage at connector pin P2-26 is referenced to connector pin P2-27 which is at a potential of 5.1 vdc, the output voltage measured at connector pin P2-26 will be $6.35 - 5.10 = 1.25$ vdc. This is true because there is no voltage drop across R130 or R160. The DC Gain of the circuit can be obtained by simply dividing the output voltage by the input voltage.

$$\begin{aligned}
 \text{DC Gain} &= V_o/V_{in} = 1.25/12.5 \\
 &= 0.10.
 \end{aligned}$$

2. Test Number 21020 : VBMT AC Ripple Gain (1 Hz)

This test uses the same circuit as in test number 21010. The schematic is shown in FIGURE 19 of APPENDIX C. Here the circuit is tested for the AC ripple gain using an input of 1 Hz at 4 volts peak to peak. The input is applied to connector pin P2-2 referenced to P2-3. The voltage at the non-inverting input (pin 6) can be obtained using the voltage divider rule as follows.

$$\begin{aligned}
 v(+) &= (5.1 * R133) / (R133 + R134) \\
 &= (5.1 * 150) / (150 + 15) \\
 &= 4.64 \text{ vdc.}
 \end{aligned}$$

The DC output voltage can be calculated using the equation for a non-inverting op-amp.

$$\begin{aligned}
 V_o(\text{DC}) &= V_{in} (1 + R131/R132) \\
 &= 4.64 (1 + 15/150) \\
 &= 5.1 \text{ vdc.}
 \end{aligned}$$

The feedback impedance, Z2, of the op-amp consists of R131 in parallel with C14. The equivalent impedance at a frequency of 1 Hz is calculated next.

$$\begin{aligned}
 Z2 &= (R131 // C14) = [15000 // (1/10E-6s)] \\
 &= (15000/10E-6s) / (15000 + 1/10E-6s) \\
 &= 15000 / (0.15s + 1). \tag{1}
 \end{aligned}$$

$$\begin{aligned}
 \text{Let } s &= j\omega = j(2 * \pi * F) \\
 &= j(2 * 3.14 * 1) \\
 &= j6.28.
 \end{aligned}$$

$$\begin{aligned}
 \text{Then } Z2 &= 15000 / (0.15 * j6.28 + 1) \\
 &= 15000 / (1 + j0.942).
 \end{aligned}$$

$$\begin{aligned}
 |Z_2| &= 15000 / |(1 + j0.942)| \\
 &= 15000 / 1.374 \\
 &= 10920 \text{ ohms.}
 \end{aligned}$$

The output of the op-amp is obtained next by using the standard op-amp equation for an inverting amplifier.

$$\begin{aligned}
 V_o &= -V_{in}(Z_2/Z_1) \\
 &= -V_{in}(10.92/150) \\
 &= -V_{in}(0.0726).
 \end{aligned}$$

V_{in} is the input signal "A"

$$\begin{aligned}
 \text{AC Gain} &= V_o/V_{in} \\
 &= (-0.0726V_{in})/V_{in} \\
 &= -0.0726.
 \end{aligned}$$

3. Test Number 21030 : VBMT AC Ripple Gain (10 Hz)

This test is identical to the previous test (number 21020) with the input frequency changed to 10 Hz instead of 1 Hz. Using equation number 1, the new feedback impedance, Z_2 , can be calculated at a frequency of 10 Hz.

$$\begin{aligned}
 Z_2 &= 15000 / (0.15s + 1) \\
 &= j62.83.
 \end{aligned}$$

$$\text{where } s = j\omega = j(2\pi \cdot 10).$$

$$\begin{aligned} Z_2 &= 15000 / (0.15 * j62.83 + 1) \\ &= 15000 / (1 + j9.425), \end{aligned}$$

$$\begin{aligned} |Z_2| &= 15000 / |(1 + j9.425)| \\ &= 15000 / 9.478 \\ &= 1583 \text{ ohms.} \end{aligned}$$

The output voltage can now be recalculated using this impedance. The DC voltages are the same as in test number 21020.

$$\begin{aligned} V_o &= -V_{in}(Z_2/Z_1) \\ &= -V_{in}(1583/150000) \\ &= -V_{in}(0.0106), \end{aligned}$$

$$\text{AC Gain} = V_o/V_{in} = -0.0106,$$

4. Test Number 21040 : VBMT AC Ripple Gain (1 Hz)

Test number 21040 is a repeat of test number 21020 with the input signal reversed. The schematic is shown in FIGURE 19, located in Appendix C. The magnitude of the signal is still 4 volts peak-to-peak. The analysis for this test is somewhat different from that of the previous tests. Because the input signal (SIG. A) is applied to connector pin P2-3 and referenced to connector pin P2-2, the op-amp

acts as a non-inverting amplifier. The AC voltage at the non-inverting input of the op-amp (pin 6) must be found using the voltage divider rule. The 5.1 vdc source at node C on the schematic is assumed to be a ground for AC analysis.

$$\begin{aligned}
 \text{Let } Z3 &= R134 // C15 \\
 &= R131 // C14 = Z2 \text{ (feedback impedance)} \\
 &= 15k // 10\mu F = 10.92 \text{ kohms @ } 1 \text{ Hz.} \\
 &\text{(calculated in test \#21020 above)}
 \end{aligned}$$

$$\begin{aligned}
 V(+) &= V_{in}(Z3)/(R133+Z3) \\
 &= (V_{in} \cdot 10920)/(150000+10920) \\
 &= 0.0679 V_{in}.
 \end{aligned}$$

The AC output at pin 10 of the op-amp can now be found using the standard op-amp equation for the non-inverting mode. The AC gain can be obtained by then dividing the output voltage by the input voltage. The DC voltages are the same as in test number 21020.

$$\begin{aligned}
 V_o &= V(+)(1+Z2/Z1) \\
 &= V_{in}(0.0679)(1+10.92/150) \\
 &= 0.0726 V_{in}.
 \end{aligned}$$

$$\text{AC Gain} = V_o/V_{in} = 0.0726.$$

5. Test Number 21200 : 1FKI DC Gain

The circuit for this test is shown in FIGURE 21 located in APPENDIX C. U20 is a 747 operational amplifier which is used as a Lossy Integrator and/or a Low Pass Filter. This test simply checks the DC gain of the amplifier using an input voltage of 1.5 volts DC. The voltage at the non-inverting input (pin 6) can be found using the formula for the voltage divider network consisting of R122, R123, the 5.1 vdc source, and the 1.5 vdc input voltage.

$$\begin{aligned} V(+) &= [1.5(R123)+5.1(R122)]/[R122+R123] \\ &= [(1.5*118000)+(5.1*59000)]/[59000+118000] \\ &= 2.70 \text{ vdc.} \end{aligned}$$

Because this test only involves DC analysis, the capacitors in the circuit can be ignored. The output voltage of U20 (pin 10) can be obtained directly from the standard op-amp equation used for a non-inverting amplifier.

$$\begin{aligned} V_o &= V(+)[1+(R120/R121)] \\ &= 2.70*[1+(118/59)] \\ &= 8.10 \text{ vdc.} \end{aligned}$$

If the output voltage at connector pin P2-4 is referenced to connector pin P2-27 which is at a potential of 5.1 vdc, the output voltage measured at connector pin P2-4

will be $8.10 - 5.10 = 3.00$ vdc. This is true because there is no voltage drop across R119 or R160. The DC Gain of the circuit can be obtained by simply dividing the output voltage by the input voltage.

$$\begin{aligned}\text{DC Gain} &= V_o/V_{in} = 3.00/1.50 \\ &= 2.0.\end{aligned}$$

6. Test Number 21210 : IFKT AC Ripple Gain (1 Hz)

This test uses the same circuit as in test number 21200. The schematic is shown in FIGURE 21, located in APPENDIX C. Here, the circuit is tested for the AC ripple gain using an input of 1 Hz at 4 volts peak to peak. The input is applied to connector pin P2-28 referenced to P2-29. The voltage at the non-inverting input (pin 6) can be obtained using the voltage divider rule as follows.

$$\begin{aligned}V(+) &= (5.1 * R122) / (R122 + R123) \\ &= (5.1 * 59) / (118 + 59) \\ &= 1.70 \text{ vdc}.\end{aligned}$$

The DC output of the op-amp due to this voltage can be obtained using the equation for a non-inverting op-amp.

$$\begin{aligned}V_o(\text{DC}) &= V(+)[1 + R120/R121] \\ &= 1.7(1 + 118/59) = 5.1 \text{ vdc}.\end{aligned}$$

The feedback impedance, Z_2 , of the op-amp consists of R_{120} in parallel with C_{12} . The equivalent impedance at a frequency of 1 Hz is calculated below.

$$\begin{aligned} Z_2 &= (R_{120} // C_{12}) = [118000 // (1/10E-6s)] \\ &= (118000/10E-6s) / (118000 + 1/10E-6s) \\ &= 118000 / (1.18s + 1). \end{aligned} \quad (2)$$

$$\begin{aligned} \text{Let } s &= j\omega = j(2\pi \cdot \text{Hz}) \\ &= j(2 \cdot 3.14 \cdot 1) \\ &= j6.28. \end{aligned}$$

$$\begin{aligned} Z_2 &= 118000 / (1.18 \cdot j6.28 + 1) \\ &= 118000 / (1 + j7.410), \end{aligned}$$

$$\begin{aligned} |Z_2| &= 118000 / |(1 + j7.410)| \\ &= 118000 / 7.480 \\ &= 15770 \text{ ohms}. \end{aligned}$$

The output of the op-amp is obtained next by using the standard op-amp equation for an inverting amplifier.

$$\begin{aligned} V_o &= -V_{in}(Z_2/Z_1) \\ &= -V_{in}(15.77/59) \\ &= -V_{in}(0.267). \end{aligned}$$

V_{in} is the input signal "A".

$$\begin{aligned}
 \text{AC Gain} &= v_o/v_{in} \\
 &= (-0.267v_{in})/v_{in} \\
 &= -0.267.
 \end{aligned}$$

7. Test Number 21220 : IFKT AC Ripple Gain (10 Hz)

This test is identical to the previous test (number 21210) with the input frequency changed to 10 Hz instead of 1 Hz. This changes the equivalent resistance of the feedback circuit Z2.

$$\text{From equation 2: } Z2 = 118000/(1.18s+1)$$

$$\text{where } s = j\omega = j(2\pi * 10) = j62.83.$$

$$\begin{aligned}
 Z2 &= 118000/(1.18*j62.83+1) \\
 &= 118000/(1+j74.14).
 \end{aligned}$$

$$\begin{aligned}
 |Z2| &= 118000/|(1+j74.14)| \\
 &= 118000/74.15 \\
 &= 1590 \text{ ohms.}
 \end{aligned}$$

The output voltage can now be recalculated using this impedance as follows. The DC voltages are the same as in test number 21210.

$$\begin{aligned}
 v_o &= -v_{in}(Z_2/Z_1) \\
 &= -v_{in}(1590/59000) \\
 &= -v_{in}(0.0269) \\
 \text{AC Gain} &= v_o/v_{in} = -0.0269.
 \end{aligned}$$

8. Test Number 21230 : 1FKT AC Ripple Gain (1 Hz)

Test number 21230 is a repeat of test number 21210 with the input signal reversed. The schematic is shown in FIGURE 21 located in APPENDIX C. The magnitude of the signal is still 4 volts peak to peak. The analysis for this test is somewhat different from that of the previous tests. Because the input signal (SIG. A) is applied to connector pin P2-29 and referenced to connector pin P2-28, the op-amp acts as a non-inverting amplifier. The AC voltage at the non-inverting input of the op-amp (pin 6) must be found using the voltage divider rule. The 5.1 vdc source at node C is assumed to be ground for AC analysis.

$$\begin{aligned}
 \text{Let } Z_3 &= R_{123} // C_{13} \\
 &= R_{120} // C_{12} = Z_2 \text{ (feedback impedance)} \\
 &= 118k // 10\mu F = 15.77 \text{ kohms @ 1 Hz,} \\
 &\text{(calculated in test \#21210 above)}
 \end{aligned}$$

$$\begin{aligned}
 V(+) &= v_{in}(Z_3)/(R_{133}+Z_3) \\
 &= (v_{in} \cdot 15770)/(59000+15770) \\
 &= 0.2109 v_{in}.
 \end{aligned}$$

The AC output at pin 10 of the op-amp can now be found using the standard op-amp equation for the non-inverting mode. The AC gain can be obtained by then dividing the output voltage by the input voltage. The DC voltages are the same as in test number 21210.

$$\begin{aligned} V_o &= V(+)(1+Z_2/Z_1) \\ &= V_{in}(0.2109)(1+15.77/59) \\ &= 0.2670 V_{in}. \end{aligned}$$

$$AC \text{ Gain} = V_o / V_{in} = 0.2670.$$

9. Test Number 21400 : IFMT DC Gain

The circuit for this test is shown in FIGURE 25 located in APPENDIX C. U22 is a 747 operational amplifier which is used as a Lossy Integrator and/or a Low Pass Filter. This test simply checks the DC gain of the amplifier using an input voltage of 1.5 volts DC. The voltage at the non-inverting input (pin 6) can be found using the formula for the voltage divider network consisting of R107, R108, the 5.1 vdc source, and the 1.5 vdc input voltage.

$$\begin{aligned} V(+) &= [1.5(R108)+5.1(R107)]/[R108+R107] \\ &= [(1.5*105000)+(5.1*59000)]/[59000+105000] \\ &= 2.80 \text{ vdc}. \end{aligned}$$

Because this test only involves DC analysis, the capacitors in the circuit can be ignored. The output voltage of U22 (pin 10) can be obtained directly from the standard op-amp equation used for a non-inverting amplifier.

$$\begin{aligned} V_o &= V(+)[1+(R_{105}/R_{106})] \\ &= 2.80*[1+(105/59)] \\ &= 7.77 \text{ vdc.} \end{aligned}$$

If the output voltage at connector pin P2-31 is referenced to connector pin P2-27 which is at a potential of 5.1 vdc, the output voltage measured at connector pin P2-31 will be $7.77 - 5.10 = 2.67$ vdc. This is true because there is no voltage drop across R104 or R160. The DC Gain of the circuit can be obtained by simply dividing the output voltage by the input voltage.

$$\begin{aligned} \text{DC Gain} &= V_o/V_{in} \approx 2.67/1.50 \\ &= 1.78. \end{aligned}$$

10. Test Number 21410 : IFMT AC Ripple Gain (1 Hz)

This test uses the same circuit as in test number 21400. The schematic is shown in FIGURE 25, located in APPENDIX C. Here the circuit is tested for the AC ripple gain using an input of 1 Hz at 4 volts peak-to-peak. The

input is applied to connector pin P2-30 referenced to P2-5.
The voltage at the non-inverting input (pin 6) can be
obtained using the voltage divider rule as follows.

$$\begin{aligned} V(+) &= (5.1 \cdot R107) / (R107 + R108) \\ &= (5.1 \cdot 59) / (105 + 59) \\ &= 1.84 \text{ vdc.} \end{aligned}$$

The DC output of the op-amp due to this voltage can
be obtained using the equation for a non-inverting op-amp.

$$\begin{aligned} V_o(\text{DC}) &= V(+)[1 + R105/R106] \\ &= 1.84(1 + 105/59) \\ &= 5.1 \text{ vdc.} \end{aligned}$$

The feedback impedance, Z2, of the op-amp consists
of R105 in parallel with C10. The equivalent impedance at a
frequency of 1 Hz is calculated below.

$$\begin{aligned} Z2 &= (R105 // C10) = [105000 // (1/10E-6s)] \\ &= (105000/10E-6s) / (105000 + 1/10E-6s) \\ &= 105000 / (1.05s + !). \end{aligned} \tag{3}$$

$$\begin{aligned} \text{Let } s &= j\omega = j(2\pi \cdot F) \\ &= j(2 \cdot 3.14 \cdot 1) \\ &= j6.28. \end{aligned}$$

$$\begin{aligned} Z_2 &= 105000 / (1.05 * j6.28 + 1) \\ &= 105000 / (1 + j6.597), \end{aligned}$$

$$\begin{aligned} |Z_2| &= 105000 / |(1 + j6.957)| \\ &= 105000 / 6.673 \\ &= 15.7 \text{ kohms.} \end{aligned}$$

The output of the op-amp is obtained next by using the standard op-amp equation for an inverting amplifier.

$$\begin{aligned} V_o &= -V_{in}(Z_2/Z_1) \\ &= -V_{in}(15.70/59) \\ &= -V_{in}(0.266). \end{aligned}$$

V_{in} is the input signal "A"

$$\begin{aligned} \text{AC Gain} &= V_o/V_{in} \\ &= (-0.266 * V_{in})/V_{in} \\ &= -0.266. \end{aligned}$$

11. Test Number 21420 : IFMT AC Ripple Gain (10 Hz)

This test is identical to the previous test (number 21410) with the input frequency changed to 10 Hz instead of 1 Hz. This changes the equivalent resistance of the feedback circuit Z_2 .

From equation 3: $Z2 = 105000/(1.05s+1)$,

where $s = j\omega = j(2\pi \cdot 10) = j62.83$.

$$\begin{aligned} Z2 &= 105000/(1.05 \cdot j62.83 + 1) \\ &= 105000/(1 + j65.97), \end{aligned}$$

$$\begin{aligned} |Z2| &= 105000/|(1 + j65.97)| \\ &= 105000/65.98 \\ &= 1590 \text{ ohms.} \end{aligned}$$

The output voltage can now be recalculated using this impedance as follows. The DC voltages are the same as in test number 21410.

$$\begin{aligned} V_o &= -V_{in}(Z2/Z1) \\ &= -V_{in}(1590/59000) \\ &= -V_{in}(0.0269), \end{aligned}$$

$$\text{AC Gain} = V_o/V_{in} = -0.0269,$$

12. Test Number 21430 : IFMT AC Ripple Gain (1 Hz)

Test number 21430 is a repeat of test number 21410 with the input signal reversed. The schematic is shown in FIGURE 25, located in APPENDIX C. The magnitude of the signal is still 4 volts peak-to-peak. The analysis for this test is somewhat different from that of the previous tests.

Because the input signal (SIG. A) is applied to connector pin P2-5 and referenced to connector pin P2-30, the op-amp acts as a non-inverting amplifier. The AC voltage at the non-inverting input of the op-amp (pin 6) must be found using the voltage divider rule. The 5.1 vdc source at node C is assumed to be ground for AC analysis.

$$\begin{aligned}\text{Let } Z3 &= R108 // C11 \\ &= R105 // C10 = Z2 \text{ (feedback impedance)} \\ &= 105k // 10\mu F = 15.70 \text{ kohms @ } 1 \text{ Hz.} \\ &\text{(calculated in test \#21410 above)}\end{aligned}$$

$$\begin{aligned}V(+) &= V_{in}(Z3)/(R107+Z3) \\ &= (V_{in}*15.7)/(59+15.7) \\ &= 0.210 V_{in}.\end{aligned}$$

The AC output at pin 10 of the op-amp can now be found using the standard op-amp equation for the non-inverting mode. The AC gain can be obtained by then dividing the output voltage by the input voltage. The DC voltages are the same as in test number 21410.

$$\begin{aligned}V_o &= V(+)(1+Z2/Z1) \\ &= V_{in}(0.210)(1+15.7/59) \\ &= 0.266 V_{in}.\end{aligned}$$

$$\text{AC Gain} = V_o/V_{in} = 0.266.$$

E. DC Threshold Tests

1. Test Number 21050 : VBMH Threshold Input Voltage

The circuit for this test is shown in FIGURE 20, located in APPENDIX C. The output of op-amp U21 (pin 10), which was tested previously, is connected to the inverting input of U21 (pin 1). This half of U21 acts as a comparator. The input voltage is applied to connector pin P2-2 referenced to P2-3 and is decremented in 10 mvdc steps starting with -5.0 vdc until the output of the comparator switches logic states. The output of the comparator is connected to an opto-isolator Q39 which directly controls the TTL output at connector pin P1-48. The output voltage swing of the op-amp U21 can be calculated using the sum of the inverting and non-inverting gain equations for op-amps.

Output voltage due to inverting input (pin 7):

$$\begin{aligned} V_{o+} &= -V_{in} * (R_{131}/R_{132}) = -V_{in} * (15/150) \\ &= -0.1 V_{in} \quad \text{where} \quad -9.0 < V_{in} < -5.0. \end{aligned}$$

Output voltage due to non-inverting input (pin 6):

$$\begin{aligned} V_{o-} &= V(+)*(1+R_{131}/R_{132}) \\ &= [(5.1 * R_{133}) / (R_{133} + R_{134})] * [1 + R_{133}/R_{132}] \\ &= [(5.1 * 150) / (150 + 15)] * [1 + 15/150] \\ &= 5.1 \text{ vdc.} \end{aligned}$$

Total output voltage at pin 10:

$$V_o = (V_{o+}) + (V_{o-}) = 5.1 - 0.1 * V_{in}.$$

The comparator works like a Schmitt trigger. When the voltage at the inverting input is greater than the voltage at the non-inverting input, then the output is approximately equal to $-V_{cc}$ (0 vdc). Otherwise the output is approximately equal to $+V_{cc}$ (26 vdc, see schematic). The voltage at the non-inverting input is controlled by the 5.78 vdc source at node H and the output voltage at pin 12. The voltage divider rule can be used to obtain this voltage.

$$\begin{aligned} V(+) &= [(5.78 * R_{137}) + (V_o * R_{136})] / [R_{136} + R_{137}] \\ &= [(5.78 * 2200) + (V_o * 10)] / [2200 + 10] \\ &= 5.754 + (V_o / 221). \end{aligned}$$

For $V_o = 0$ vdc :	$V(+) = 5.754$ vdc	$V(-) > V(+)$.
$V_o = 26$ vdc :	$V(+) = 5.871$ vdc	$V(-) < V(+)$.

This difference in the $V(+)$ voltage levels creates a window for threshold voltages to fall into. In other words, if the output voltage of the comparator is 0 vdc then the trigger voltage needed at pin 1 will be 5.754 vdc. When the output voltage is 26 vdc, then the trigger level will be 5.871 vdc. FIGURE 1 illustrates these results using arrows

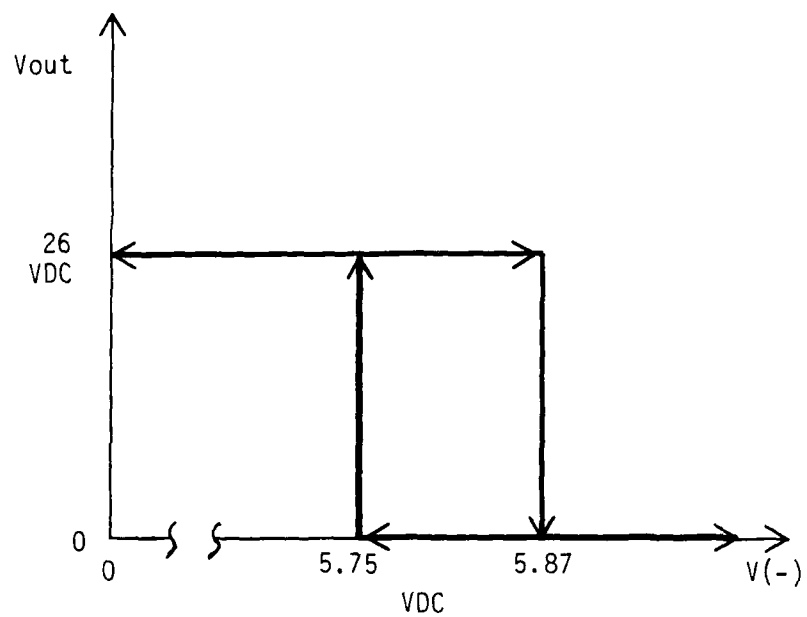


FIGURE - 1 VBMH Comparator Triggering Window

to indicate the direction in which the voltage $V(-)$ is either falling or rising.

When $V(-)$ is 0 vdc the output of the comparator is approximately 26 vdc. When $V(-)$ increases, the output will swing to 0 vdc at $V(-)$ equal to 5.871 vdc. When $V(-)$ starts to decrease from this point, it must reach 5.754 vdc for the output to swing high again.

The voltage at $V(-)$ (pin 1) is equal to the output voltage of the op-amp due to the fact that approximately no current flows into the input of an op-amp so no voltage drop occurs across R135. This voltage is obtained from the equation derived above for the output of the op-amp (pin 10). The input voltage at connector pin P2-2 ranges from -5.0 vdc to -9.0 vdc.

$$V(-) = V_o = 5.1 - 0.1 V_{in}.$$

$$\text{For } V_{in} = -5.0 : V_o = 5.6 \text{ vdc}$$

$$V_{in} = -9.0 : V_o = 6.0 \text{ vdc}$$

$$\text{Step size} = 0.1 \times 10 \text{ mv} = 1 \text{ mvdc}.$$

Therefore, $V(-)$ increments from 5.6 vdc to 6.0 vdc in 1 mvdc steps. Since the initial voltage of $V(-)$ is less than that of $V(+)$, the output voltage at pin 12 will be approximately 26 vdc and the trigger voltage will be 5.871 vdc. By working backwards with the above output equation

for V_o , the threshold voltage needed to cause the comparator to switch states can be obtained.

$$\begin{aligned} V_o &= 5.1 - 0.1 V_{in} \\ 5.871 &= 5.1 - 0.1 V_{in} \\ V_{in} &= (5.1 - 5.871) / 0.1 \\ &= -7.7 \text{ vdc.} \end{aligned}$$

The output of the comparator directly controls the TTL output at connector pin P1-48. The initial state of the comparator is high which causes Q39 to be turned on. This causes P1-48 to be shorted to ground and a TTL logic 0 will be measured. When the threshold voltage is reached and the comparator switches to a low state, Q39 will turn off. The pullup resistor R139 will then cause P1-48 to be at 5 vdc or TTL logic 1.

2. Test Number 21240 : IFKL Threshold Input Voltage

The circuit for this test is shown in FIGURE 22, located in APPENDIX C. The output of op-amp U20 (pin 10), which was tested previously, is connected to the inverting input of U20 (pin 1). This half of U20 acts as a comparator. The input voltage is applied to connector pin P2-29 referenced to P2-28 and is incremented in 10 mvdc steps, starting with 0.0 vdc until the output of the comparator switches logic states. The output of the comparator is connected to an opto-isolator Q38 which

directly controls the TTL output at connector pin P1-47.
The output voltage swing of the op-amp U20 can be calculated using the non-inverting gain equation for op-amps.

Output voltage due to non-inverting input (pin 6):

$$\begin{aligned}
 V_{o-} &= V(+)*(1+R_{120}/R_{121}) \\
 &= [(5.1*R_{122})+(V_{in}*R_{123})]/[R_{122}+R_{122}] \\
 &\quad *(1+R_{120}/R_{121}) \\
 &= [(5.1*59)+(V_{in}*118)]/[118+59]*(1+118/59) \\
 &= (0.667*V_{in}+1.7)*(3) \\
 &= 5.1+2*V_{in}.
 \end{aligned}$$

The comparator works like a Schmitt trigger. When the voltage at the inverting input is greater than the voltage at the non-inverting input, then the output is approximately equal to $-V_{cc}$ (0 vdc). Otherwise, the output is approximately equal to $+V_{cc}$ (26 vdc, see schematic). The voltage at the non-inverting input is controlled by the 6.67 vdc source at node G and the output voltage at pin 12. The voltage divider rule can be used to obtain this voltage.

$$\begin{aligned}
 V(+) &= [(6.67*R_{127})+(V_o*R_{126})]/[R_{126}+R_{127}] \\
 &= [(6.67*2200)+(V_o*10)]/[2200+10] \\
 &= 6.64+(V_o/221).
 \end{aligned}$$

For $v_o = 0$ vdc : $V(+)$ = 6.640 vdc $V(-) > V(+)$.
 $v_o = 26$ vdc : $V(+)$ = 6.758 vdc $V(-) < V(+)$.

This difference in the $V(+)$ voltage levels creates a window for threshold voltages to fall into. In other words, if the output voltage of the comparator is 0 vdc, then the trigger voltage needed at pin 1 will be 6.640 vdc. When the output voltage is 26 vdc, then the trigger level will be 6.758 vdc. FIGURE 2 illustrates these results using arrows to indicate the direction in which the voltage $V(-)$ is either falling or rising.

When $V(-)$ is 0 vdc, the output of the comparator is approximately 26 vdc. When $V(-)$ increases, the output will swing to 0 vdc at $V(-)$ equal to 6.758 vdc. When $V(-)$ starts to decrease from this point, it must reach 6.640 vdc for the output to swing high again.

The voltage at $V(-)$ (pin 1) is equal to the output voltage of the op-amp due to the fact that approximately no current flows into the input of an op-amp so no voltage drop occurs across R125. This voltage is obtained from the equation derived above for the output of the op-amp (pin 10). The input voltage at connector pin P2-29 ranges from 0.0 vdc to 1.0 vdc.

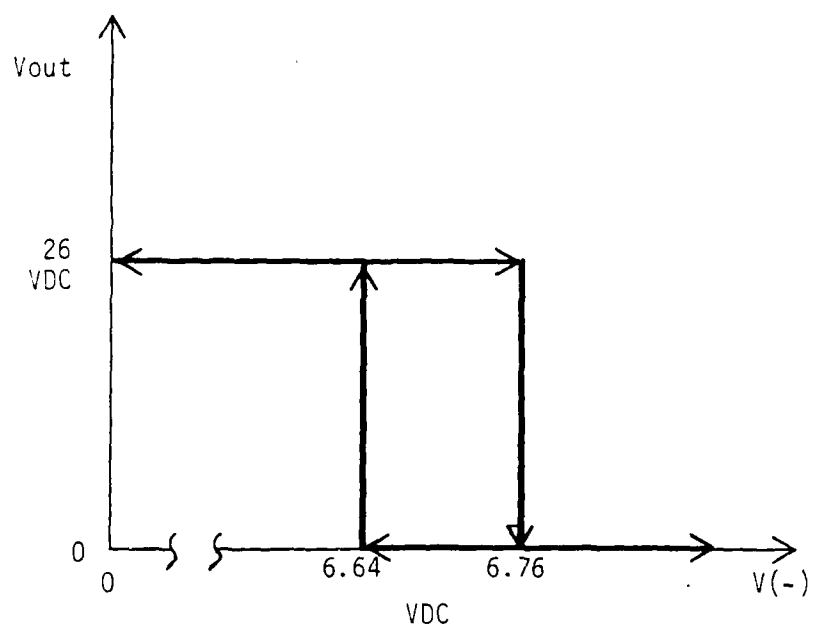


FIGURE 2 - IFKL Comparator Triggering Window

$$V(-) = V_o = 5.1 + 2.0 * V_{in}.$$

$$\text{For } V_{in} = 0.0 : V_o = 5.1 \text{ vdc}$$

$$V_{in} = 1.0 : V_o = 8.1 \text{ vdc}$$

$$\text{Step size} = 2.0 * 10 \text{ mv} = 20 \text{ mvdc}.$$

Therefore, $V(-)$ increments from 5.1 vdc to 8.1 vdc in 20 mvdc steps. Since the initial voltage of $V(-)$ is less than that of $V(+)$, the output voltage at pin 12 will be approximately 26 vdc and the trigger voltage will be 6.758 vdc. By working backwards with the above output equation for V_o , the threshold voltage needed to cause the comparator to switch states can be obtained.

$$V_o = 5.1 + 2.0 * V_{in}$$

$$6.758 = 5.1 + 2.0 * V_{in}.$$

$$V_{in} = (6.758 - 5.1) / 2.0 = 0.829 \text{ vdc}.$$

The output of the comparator directly controls the TTL output at connector pin P1-47. The initial state of the comparator is high which causes Q38 to be turned on. This causes P1-47 to be shorted to ground and a TTL logic 0 will be measured. When the threshold voltage is reached and the comparator switches to a low state Q38 will turn off. The pullup resistor R128 will then cause P1-47 to be at 5 vdc or TTL logic 1.

3. Test Number 21250 : IFKH Threshold Input Voltage

The circuit schematic for this test is shown in FIGURE 23, located in APPENDIX C. The op-amp U20 used in the previous test is used here also as the first stage of this test. The results from the above analysis are shown below.

$$V_o(\text{pin } 10) = 5.1 + 2 * V_{in}.$$

The second stage of the circuit consists of U22 which is used as a comparator or a Schmitt trigger. When the voltage at the inverting input is greater than the voltage at the non-inverting input, then the output is approximately equal to $-V_{cc}$ (0 vdc). Otherwise, the output is approximately equal to $+V_{cc}$ (26 vdc, see schematic). The voltage at the inverting input (pin 1) is controlled by zener diode VR17 which holds the voltage at 18 volts. The voltage at the non-inverting input is controlled by the output of the first stage op-amp and the output voltage at pin 12. The voltage divider rule can be used to obtain this voltage.

$$\begin{aligned} V(+) &= [(V_{in} * R_{117}) + (V_o * R_{116})] / [R_{116} + R_{117}] \\ &= [(V_{in} * 1800) + (V_o * 10)] / [1800 + 10] \\ &= 0.994 * V_{in} + V_o / 181. \end{aligned}$$

Note. $V(+)$ = pin 2; V_o = pin 12; V_{in} = pin 10.

The switching voltage for the comparator is at $V(+)$ equal to 18 vdc. By setting the above equation to this value, and by setting V_o to either 0 or 26 vdc, the window values for the input trigger voltages can be obtained.

$$V_o=0 : 18 = 0.994 \cdot V_{in} + 0/181 \quad V_{in} = 18.1 \text{ vdc.}$$

$$V_o=26 : 18 = 0.994 \cdot V_{in} + 26/181 \quad V_{in} = 17.96 \text{ vdc.}$$

This difference in the V_{in} voltage levels creates a window for threshold voltages to fall into. In other words, if the output voltage of the comparator is 0 vdc, then the trigger voltage needed at pin 10 will be 18.10 vdc. When the output voltage is 26 vdc, then the trigger level will be 17.96 vdc. FIGURE 3 illustrates these results using arrows to indicate the direction in which the voltage $V(-)$ is either falling or rising.

The initial voltage input is 3.0 volts which corresponds to an output voltage of 11.1 volts at pin 10 of U20 (see above equation). By looking at the equation obtained for $V(+)$ at pin 2 of the comparator, it can be seen that initially $V(-)$ will be greater than $V(+)$ which causes the output at pin 12 to be low or approximately 0 volts. The trigger voltage needed at pin 10 or U20 is therefore 18.1 vdc (see above). By working backwards with the output equation derived for U20, the threshold voltage needed at P2-29 can be calculated.

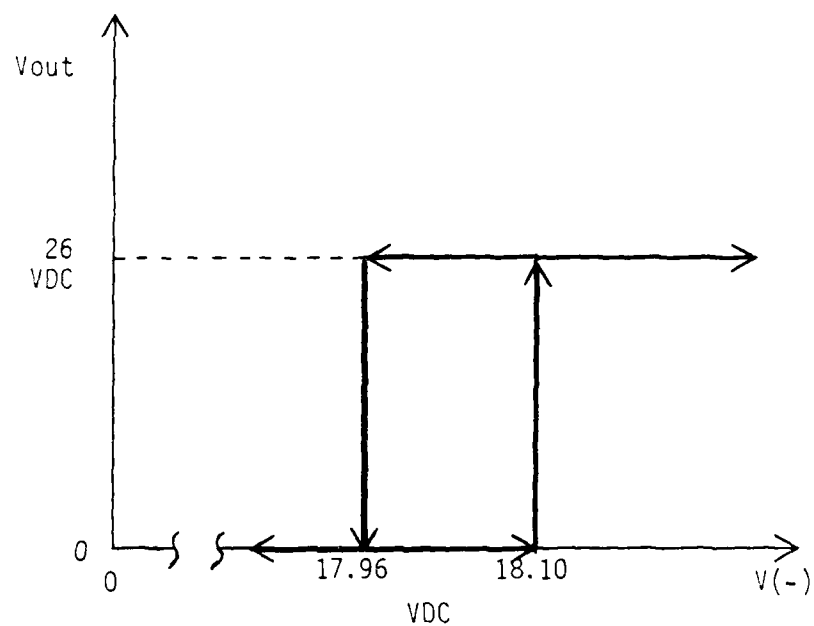


FIGURE - 3 IFKH Comparator Triggering Window

$$18.1 = 2.0 * V_{in} + 5.1$$

$$V_{in} = (18.1 - 5.1) / 2$$

$$= 6.5 \text{ vdc,}$$

The output of the comparator directly controls the TTL output at connector pin P1-22. The initial state of the comparator is low, which causes opto-isolator Q37 to be turned off. This causes P1-22 to be pulled up by R118 to +5 vdc or logic 1. When the threshold voltage at P2-29 reaches 6.5 vdc, the comparator switches states and Q37 turns on. This causes P1-22 to be shorted to ground and a logic 0 will be measured.

4. Test Number 21440 : IFML Threshold Input Voltage

The circuit for this test is shown in FIGURE 26, located in APPENDIX C. The output of op-amp U22 (pin 10), which was tested previously, is connected to the inverting input of U23 (pin 1). This half of U23 acts as a comparator. The input voltage is applied to connector pin P2-30 referenced to P2-5 and is decremented in 10 mvdc steps starting with 0.0 vdc until the output of the comparator switches logic states. The output of the comparator is connected to an opto-isolator Q36 which directly controls the TTL output at connector pin P1-45. The output voltage swing of the op-amp U22 can be calculated using the sum of the non-inverting and the inverting gain equations for

op-amps.

Voltage at non-inverting input (pin 6):

$$\begin{aligned} V(+) &= 5.1(R107)/(R107+R108) \\ &= 5.1(59)/(59+105) \\ &= 1.835 \text{ vdc.} \end{aligned}$$

Output voltage due to input voltage and $V(+)$:

$$\begin{aligned} V_o &= V(+)(1+R105/R106)-V_{in}(R105/R106) \\ &= 1.835(1+105/59)-V_{in}(105/59) \\ &= 5.1-1.78*V_{in} \end{aligned}$$

where $-1.3 < V_{in} < 0.0$ step size is 10 mv.

The comparator works like a Schmitt trigger. When the voltage at the inverting input is greater than the voltage at the non-inverting input, then the output is approximately equal to $-V_{cc}$ (0 vdc). Otherwise the output is approximately equal to $+V_{cc}$ (26 vdc, see schematic). The voltage at the non-inverting input is controlled by the 6.67 vdc source at node F and the output voltage at pin 12. The voltage divider rule can be used to obtain this voltage.

$$\begin{aligned} V(+) &= [(6.67*R111)+(V_o*R110)]/[R110+R111] \\ &= [(6.67*2200)+(V_o*10)]/[2200+10] \\ &= 6.64+(V_o/221). \end{aligned}$$

For $V_o = 0$ vdc : $V(+)$ = 6.640 vdc $V(-) > V(+)$.
 $V_o = 26$ vdc : $V(+)$ = 6.758 vdc $V(-) < V(+)$.

This difference in the $V(+)$ voltage levels creates a window for threshold voltages to fall into. In other words, if the output voltage of the comparator is 0 vdc, then the trigger voltage needed at pin 1 will be 6.640 vdc. When the output voltage is 26 vdc, then the trigger level will be 6.758 vdc. FIGURE 4 illustrates these results using arrows to indicate the direction in which the voltage $V(-)$ is either falling or rising.

When $V(-)$ is 0 vdc, the output of the comparator is approximately 26 vdc. When $V(-)$ increases, the output will swing to 0 vdc at $V(-)$ equal to 6.758 vdc. When $V(-)$ starts to decrease from this point, it must reach 6.640 vdc for the output to swing high again.

The voltage at $V(-)$ (pin 1) is equal to the output voltage of the op-amp due to the fact that approximately no current flows into the input of an op-amp so no voltage drop occurs across R109. This voltage is obtained from the equation derived above for the output of the op-amp (pin 10). The input voltage at connector pin P2-30 ranges from 0.0 vdc to -1.3 vdc.

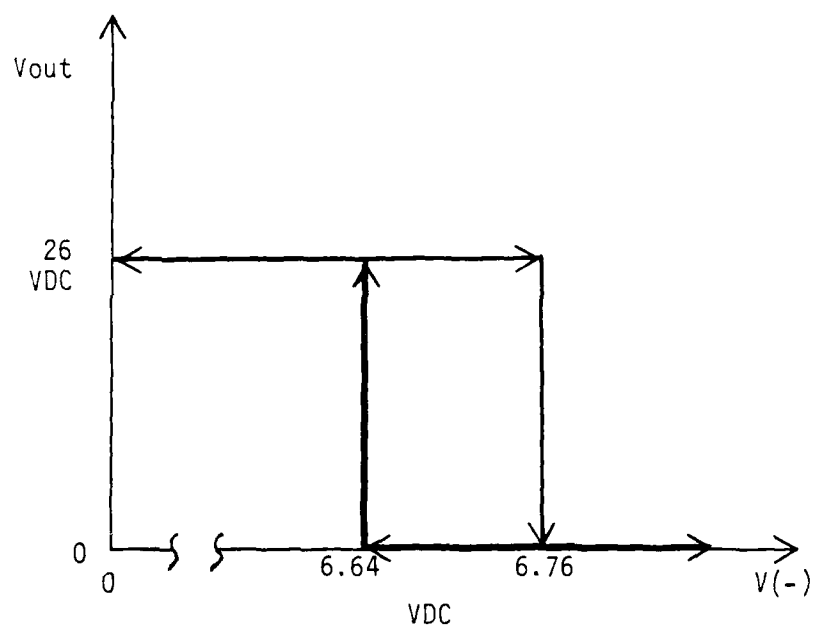


FIGURE - 4 IFML Comparator Triggering Window

$$V(-) = V_o = 5.1 - 1.78 \text{ vin.}$$

$$\text{For } V_{in} = 0.0 : V_o = 5.1 \text{ vdc}$$

$$V_{in} = -1.3 : V_o = 7.41 \text{ vdc.}$$

$$\text{Step size} = 1.78 * 10 \text{ mv} = 17.8 \text{ mvdc.}$$

Therefore, $V(-)$ increments from 5.1 vdc to 7.41 vdc in 17.8 mvdc steps. Since the initial voltage of $V(-)$ is less than that of $V(+)$, the output voltage at pin 12 will be approximately 26 vdc and the trigger voltage will be 6.758 vdc. By working backwards with the above output equation for V_o , the threshold voltage needed to cause the comparator to switch states can be obtained.

$$V_o = 5.1 - 1.78 * V_{in}$$

$$6.758 = 5.1 - 1.78 * V_{in}$$

$$\begin{aligned} V_{in} &= -(6.758 - 5.1) / 1.78 \\ &= -0.933 \text{ vdc} \end{aligned}$$

The output of the comparator directly controls the TTL output at connector pin P1-45. The initial state of the comparator is high which causes opto-isolator Q36 to be turned on. This causes P1-45 to be shorted to ground and a TTL logic 0 will be measured. When the threshold voltage is reached and the comparator switches to a low state, Q36 will

turn off. The pullup resistor R113 will then cause P1-45 to be at 5 vdc or TTL logic 1.

5. Test Number 21450 : IFMH Threshold Input Voltage

The circuit schematic for this test is shown in FIGURE 27, located in APPENDIX C. The op-amp U22 used in the previous test is used here also as the first stage of this test. The results from the above analysis are shown below.

$$V_o(\text{pin } 10) = 5.1 - 1.78 * V_{in}.$$

The second stage of the circuit consist of U23 which is used as a comparator or a Schmitt trigger. When the voltage at the inverting input is greater than the voltage at the non-inverting input, then the output is approximately equal to $-V_{cc}$ (0 vdc). Otherwise the output is approximately equal to $+V_{cc}$ (26 vdc, see schematic). The voltage at the inverting input is connected to 10.2 volts through the voltage regulator. The voltage at the non-inverting input (pin 6) is controlled by the output of the first stage op-amp and the output voltage at pin 10. The voltage divider rule can be used to obtain this voltage.

$$\begin{aligned} V(+) &= [(V_{in} * R101) + (V_o * R102)] / [R101 + R102] \\ &= [(V_{in} * 2000) + (V_o * 10)] / [2000 + 10] \\ &= 0.995 * V_{in} + V_o / 201. \end{aligned}$$

Note: $V(+) = \text{pin } 2$; $V_o = \text{pin } 12$; $V_{in} = \text{pin } 10$.

The switching voltage for the comparator is at $V(+)$ equal to 10.2 vdc. By setting the above equation to this value, and by setting V_o to either 0 or 26 vdc, the window values for the input trigger voltages can be obtained.

$$V_o=0 : 10.2 = 0.995 \cdot V_{in} + 0/201 \quad V_{in} = 10.25 \text{ vdc.}$$

$$V_o=26 : 10.2 = 0.995 \cdot V_{in} + 26/201 \quad V_{in} = 10.12 \text{ vdc.}$$

This difference in the V_{in} voltage levels creates a window for threshold voltages to fall into. In other words, if the output voltage of the comparator is 0 vdc, then the trigger voltage needed at pin 10 will be 10.25 vdc. When the output voltage is 26 vdc then the trigger level will be 10.12 vdc. FIGURE 5 illustrates these results using arrows to indicate the direction in which the voltage $V(-)$ is either falling or rising.

The initial voltage input is -1.0 volts which corresponds to an output voltage of 6.88 volts at pin 10 of U22 (see above equation). By looking at the equation obtained for $V(+)$ at pin 6 of the comparator, it can be seen that initially $V(-)$ will be greater than $V(+)$ which causes the output at pin 10 to be low or approximately 0 volts. The trigger voltage needed at pin 10 of U22 is therefore

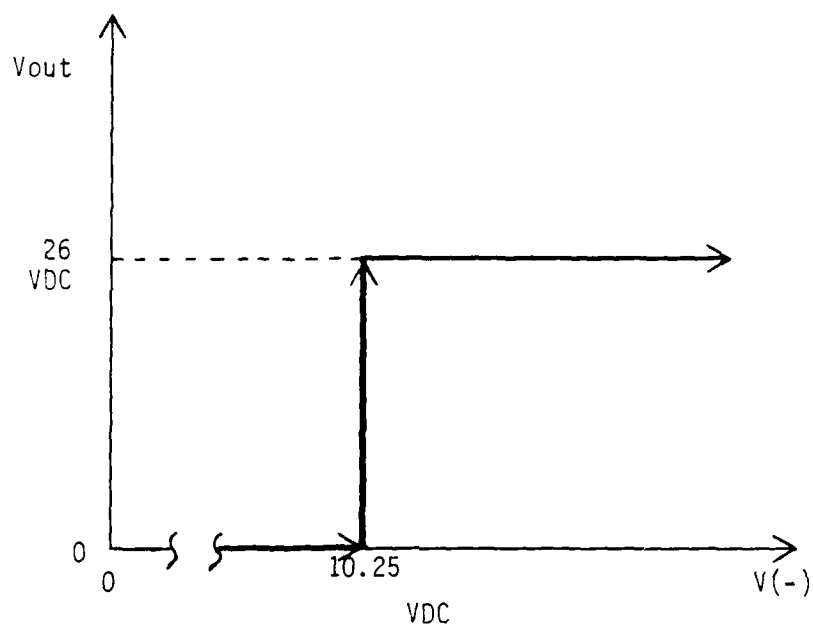


FIGURE - 5 IFMH Comparator Triggering Window

10.25 vdc (see above). By working backwards with the output equation derived for U22, the threshold voltage needed at P2-30 can be calculated.

$$10.25 = 5.1 - 1.78 * V_{in}$$

$$\begin{aligned} V_{in} &= -(10.25 - 5.1) / 1.78 \\ &= -2.89 \text{ vdc.} \end{aligned}$$

The output of the comparator directly controls the TTL output at connector pin P1-46. The initial state of the comparator is low which causes opto-isolator Q35 to be turned off. This causes P1-46 to be pulled up by R100 to +5 vdc or TTL logic 1. When the threshold voltage at P2-30 reaches -2.89 vdc, the comparator switches states and Q35 turns on. This causes P1-46 to be shorted to ground and a TTL logic 0 will be measured.

F. IFKL TTL Output Tests

1. Test Number 21260 : IFKL TTL Output

This test uses the same circuit used in test number 21240 and is reproduced in FIGURE 24, located in APPENDIX C. The circuit analysis is exactly identical to that of test number 21240 with the exception that the input voltage is not incremented. Because this is simply a TTL output test, the input voltage remains a constant which is 0 volts in

this case. The output equation derived for op-amp U20 is used below to obtain the output at pin 10.

$$\begin{aligned} V_o(\text{pin } 10) &= 5.1 + 2.0 * V_{in} && \text{where } V_{in} = 0 \text{ vdc} \\ &= 5.1 \text{ vdc.} \end{aligned}$$

The trigger voltages obtained for the comparator U20 where 6.64 and 6.76 volts which are both greater than 5.1 volts. This means that the voltage at the non-inverting input of the comparator will be greater than the voltage at the inverting input. The output of the comparator at pin 12 will then be approximately 26 volts causing the opto-isolator Q38 to be turned on. The connector pin P2-47 will be shorted to ground and measure a TTL logic 0.

2. Test Number 21270 : IFKL TTL Output

This test uses the same circuit used in test number 21240 and 21260 and is reproduced in Figure 21270, located in APPENDIX C. The circuit analysis is exactly identical to that of test number 21240, with the exception that the input voltage is not incremented and connector pin P2-6 is connected to a 28 vdc power source. In the previous tests, P2-6 had been left open. Because this is simply a TTL output test, the input voltage remains a constant which is 0 volts in this case. The output equation derived for op-amp U20 is used below to obtain the output at pin 10.

$$\begin{aligned} V_o(\text{pin } 10) &= 5.1 + 2.0 \cdot V_{in} \quad \text{where } V_{in} = 0 \text{ vdc} \\ &= 5.1 \text{ vdc.} \end{aligned}$$

The voltage seen at the non-inverting input (pin 1) of the comparator is not however 5.1 volts. Due to P2-6 being at a potential of 28 volts, the voltage divider rule must be used to obtain this voltage.

$$\begin{aligned} V(-) &= [28(R_{125}) + 5.1(R_{124})] / [R_{124} + R_{125}] \\ &= [28(33) + 5.1(120)] / [120 + 33] \\ &= 10.04 \text{ vdc.} \end{aligned}$$

The trigger voltages obtained for the comparator U20 where 6.64 and 6.76 volts which are both less than 5.1 volts. This means that the voltage at the non-inverting input of the comparator will be less than the voltage at the inverting input. The output of the comparator at pin 12 will then be approximately 0 volts causing the opto-isolator Q38 to be turned off. The connector pin P2-47 will be pulled up to +5 vdc by R128 and measure a TTL logic 1.

G. Full Power CDC(-) and FPD Logic Test (30010)

This series of tests has three parts as shown in the Test Requirement Document. The schematic diagram for this circuit is shown in FIGURE 28, contained in APPENDIX C. The input at connector pin P2-39 is an open collector input and

the outputs P2-41 and P2-15 are TTL logic level outputs. Each output has its own independent circuit. The output P2-41 is controlled by the 5-volt power supply and P2-15 is controlled by the 5-volt power supply and the open collector input P2-39. A separate 5-volt power supply is used for the pullup resistors which are needed for the P2-15 and P2-41 output pins. The two opto-isolators Q26 and Q23 act only as switches as do the 2N2222A transistors Q24 and Q25.

The analysis for the P2-41 output pin is as follows. As long as the 5-volt DC power supply is on, Q26 will be on which turns Q25 on also. This causes P2-41 to be shorted to ground and a TTL logic 0 to be measured. When the 5-volt DC power supply is turned off for test 3, Q26 and Q25 turn off and the 1-kohm pull-up resistor forces P2-41 to 5 volts DC or TTL logic 1.

The P2-15 output pin operates in much the same manner as the P2-41 output pin. This circuit is almost identical to the previous one, except that pin 7 of Q23 is connected to P2-39 instead of straight to ground. As long as the 5 volt DC power supply is on and P2-39 is grounded, Q23 will turn on turning Q24 on also. This causes the output P2-15 to be shorted to ground and a TTL logic 0 to be measured. If the 5 volt DC power supply is removed or the input P2-39 opened up, Q23 and Q24 will turn off. the output P2-15 will be forced to 5 volts by the 1-kohm pull-up resistor and a TTL logic 1 will be measured.

H. 5 Minute and 250 MSEC Timer Tests (31010-31020)

The next few tests deal with timer circuits which incorporate a military equivalent to the popular NE555 timer. Two timers, U1 and U2 are tested here simultaneously because the output of timer U1 triggers the timer U2. The schematics for these tests are shown in FIGURES 29 and 30, located in APPENDIX C. To begin, the timers must be initialized, or in other words, the timing capacitors completely discharged. This is accomplished by turning off the 28-volt power supply and grounding P2-36 for approximately one minute. This allows the timing capacitors C3 and C5 to discharge any voltage potential that may be present. Several inputs have various voltages applied to them in order to set up the correct state of certain logic circuits.

1. U1 Timer Circuit

The timer U1 is controlled by the open collector input P2-36 and operates as a one-shot. As long as this input is grounded, the timing capacitor C3 is held discharged through the series R5, CR1, R3, and CR2 to ground and the series R4 and CR2 to ground. Opto-isolator number Q5 is on as long as the 28-volt power supply is present. Because the trigger and threshold voltages of the timer are approximately 0 volts which are less than NE555 requirement of $1/3 V_{cc}$, the output at pin 3 is set high at approximately

15 volts DC. The normal configuration for a 555 one-shot would allow the timing capacitor to start charging at this time, but in this case it is still held discharged until P2-36 is opened up. When this happens, the voltage across the capacitor C3 starts to increase exponentially for a period of $1.1RC$ where R is the sum of $R3$ and $R4$ and C is equal to $C3$. This equation can be found in any linear data book which covers the 555 timer. At the end of this time period at which the voltage is equal to $2/3 V_{cc}$, the internal comparator resets the flip-flop and drives the output low. The time it takes the output to go low is calculated below.

$$\begin{aligned}
 T1 &= 1.1 * (R3 + R4) * C3 = 1.1 * (10E3 + 6.8E6) * 40E-6 \\
 &= 300 \text{ seconds for } R3 = 10 \text{ kohms} \\
 &= 324 \text{ seconds for } R3 = 560 \text{ kohms.}
 \end{aligned}$$

To sum up the above analysis, the voltage at label 1 on FIGURE 29 will initially be at approximately 15 volts minus the drop across the diode CR8. When the input P2-36 is opened up, the timer starts and drives the output at pin 3 low 300 to 324 seconds later (referred to as the nominal 315 seconds from here on). Label 1 is continued on FIGURE 30 where it is connected to the emitter of Q7. The voltage on the base of this transistor is set by the voltage divider network of R25 and R26. The straight voltage divider rule

yields a voltage of 10 volts DC which means that the voltage at the emitter must be greater than 10 plus 0.7 (the voltage drop across the base-emitter junction) for the transistor to turn on. During the 315 seconds that the U1 timer output is high, this transistor will be turned on since the output voltage of the timer is approximately 15 volts. This affects two circuits, the U2 Timer Circuit and the Q7/Q8 Transistor Circuit.

2. P2-11/35 Input Circuit

When the connector pin P2-11 has a TTL logic 0 applied to it, the opto-isolator Q6 is turned on. This grounds the anode side of diode CR9 forcing this input to node 1 (see schematic) to have no affect. If the P2-11 input pin is at a TTL logic 1 level, the opto-isolator Q6 is turned off which forces the anode side of CR9 to approximately 20 volts, ignoring the load at node 1. Connector pin P2-35 also has a TTL logic 0 applied to it in these two tests which forces the anode side of diode CR10 to approximately 0 volts. The voltage at label 1 is controlled only by the output of timer U1 for these two tests.

3. Q7/Q8 Transistor Circuit

The Q7/Q8 Transistor Circuit is controlled by the 3 wire-ORed sources discussed above: the U1 timer output, the P2-11 pin, and the P2-35 pin. The wire-ORed node is labeled node 1 on the schematic. The transistor Q7 is turned on whenever the voltage at node 1 exceeds approximately the

base voltage, which is determined by the voltage divider network of R25 and R26 or approximately 10 volts, plus the junction voltage of 0.7 volts. When the transistor Q7 is on, transistor Q8 turns on also and grounds the cathode side zener diode VR4. This causes the transistor Q3 to turn off and the output connector P2-10 will be forced to a TTL logic 1 by the 1 kohm pull-up resistor connected to 5 volts DC. After the nominal 315 seconds have elapsed and the voltage at node 1 drops below the above threshold, Q7 and Q8 turn off. The zener diode VR4 is rated at 4.7 volts so it becomes reversed biased due to the 28-volt power supply and the 2-kohm resistor R28. This reverse current through the zener turns Q3 on which shorts the output P2-10 to ground. A TTL logic 0 will then be measured.

4. U2 Timer Circuit

This output pin P2-9 is controlled by the second timer U2 which also acts as a one-shot but is configured slightly different than normal. During the initial 315 seconds when the transistor Q7 is on, the transistor Q4 will be on also due to current supplied from the Q7 collector. This causes the timing capacitor to be shorted out and the threshold voltage at pin 6 to be grounded. As mentioned above, when Q7 is on, Q8 will be on also and this results in the trigger level at pin 2 to be shorted to ground. The timer is in the initial state at this time and the output set high to Vcc which is 15 volts DC (see U1 timer analysis

for typical 555 timer operation). One important change in this configuration is the fact that a 10-kohm resistor, R14, is connected from the control voltage at pin 5 to ground. As seen in FIGURE 6 and the derivation below, this changes the control voltage level of the 555 to $1/2 V_{cc}$ instead of the normal $2/3 V_{cc}$ voltage level.

$$\begin{aligned}\text{Control Voltage} = CV &= [V_{cc}(10//10)]/[5+(10//10)] \\ &= V_{cc}(5)/(5+5) = 1/2 V_{cc}.\end{aligned}$$

One can see that if the 10 kohm resistor were not present, the control voltage would be $2/3 V_{cc}$. The timing equation for the 555 with a control voltage set at $1/2 V_{cc}$ must be derived. The standard equation used for finding the voltage-time relationship in an RC network is used below.

$$\begin{aligned}V_{out} &= V_{in}[1-e^{(-t/RC)}] \\ \text{or } t &= -(RC)\ln(1-V_{out}/V_{in}) \\ &= -(R11)(C5)\ln(1-1/2) \\ &= -(240E3)(1E-6)\ln(.5) \\ &= 166 \text{ msec.}\end{aligned}$$

To sum up the operation of timer U2, the output is initially high (about 15 vdc) and transistors Q4 and Q8 on. This high output is enough to turn on the transistor Q2 and ground the cathode side of zener diode VR3. Transistor Q1

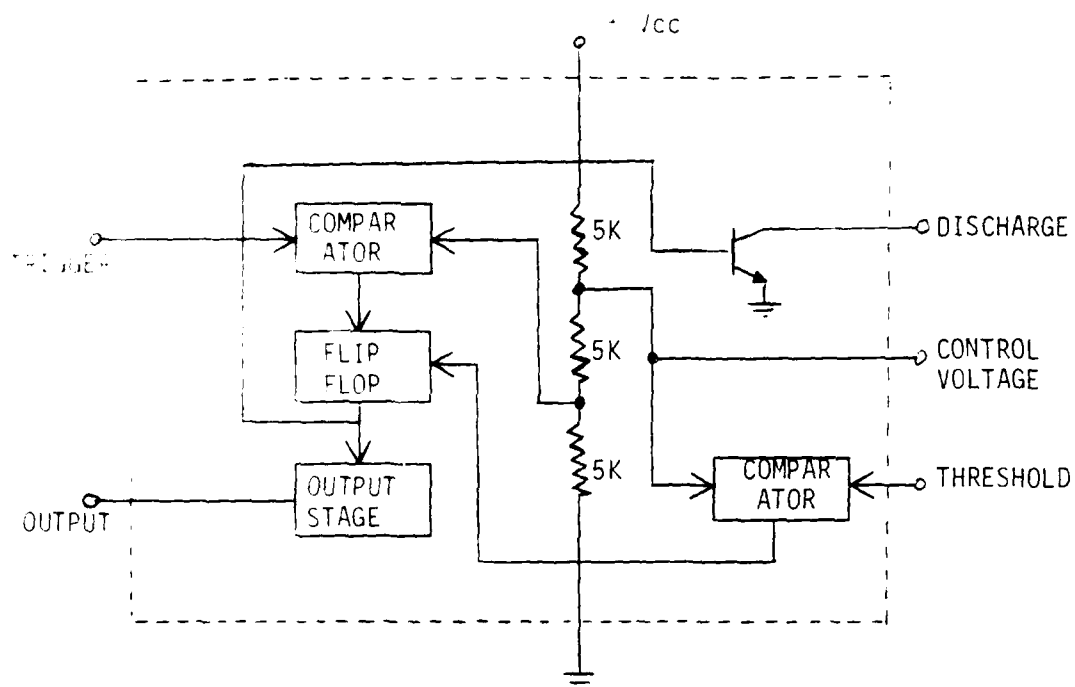


FIGURE 6 - 555 Timer Block Diagram

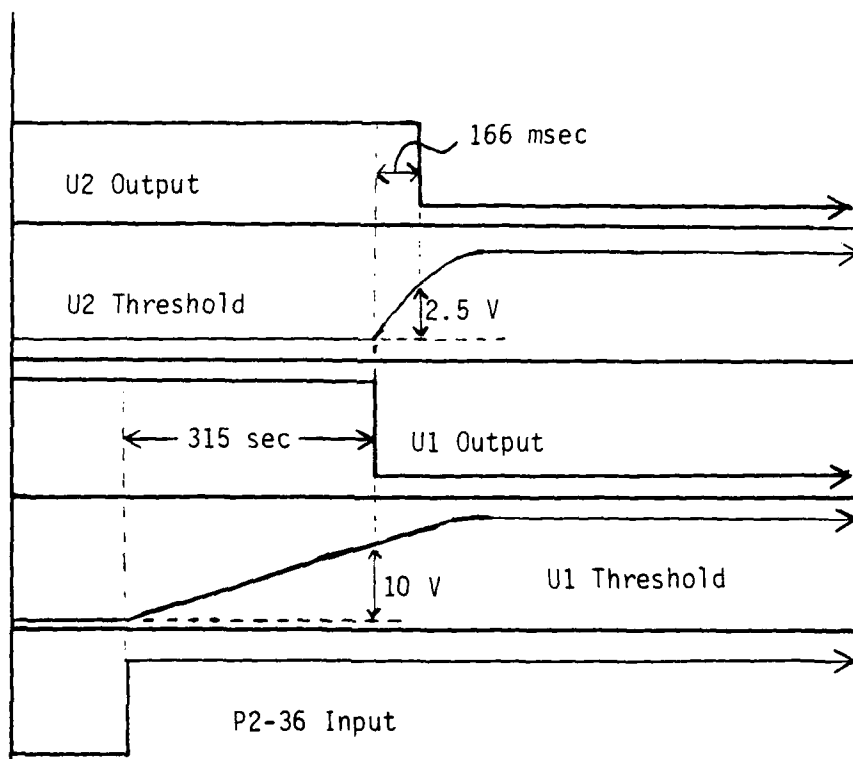


FIGURE 7 - Test Series 31000 Timing Diagram

remains off and the output at connector pin P2-9 is forced to a TTL logic 1 by the 1-kohm pull-up resistor tied to 5 volts. After the 315-second-U1-timer has expired and Q7 turns off, Q4 and Q8 turn off, triggering U2 and allowing C5 to begin charging. After the nominal 166 milliseconds has elapsed, the output of U2 at pin 3 is driven low, turning the transistor Q2 off. The reverse current flowing through the 4.7 volt zener diode VR3, which is supplied by the 28-volt power supply, then turns Q1 on, shorting the output P2-9 to ground. A TTL logic 0 will then be measured. A timing diagram of the input P2-36 and several other nodes including the outputs P2-9 and P2-10 is shown in FIGURE 7.

1. 20 SECOND TIMER (32010)

This test uses the same input signals as the previous timer test in order to discharge the timing capacitors and set up the proper logic. The schematic diagram for this test is shown in FIGURE 31, located in APPENDIX C. The output at CCA pin P2-12 is used to monitor the timer U3 and the open collector input P2-36 is used again to trigger the timer. The timer U3 is the military equivalent to the NE555 timer and once again used as a one-shot.

1. U3 Timer Circuit

There are two RC timing networks used in the U3 timer configuration, one for the threshold voltage and one

for the trigger voltage. The control voltage at pin 5 is set to $1/2 V_{cc}$ due to the 10 kohm resistor R45 tied to ground (see the analysis for the control voltage on the U2 Timer Circuit). The timing equation is therefore in the same form as that derived for the timer U2 above.

$$\begin{aligned} T1 &= -(RC)\ln(1-1/2) = (0.693)RC \\ &= 0.693*(R46+R47)*C9 = 0.693*2300*10E-6 \\ &= 15.25 \text{ seconds.} \end{aligned}$$

The second RC network is used to bring the trigger voltage up smoothly above the required $1/3 V_{cc}$. The trigger voltage is limited by the voltage divider network of R43 and R44. Using the voltage divider rule this limiting voltage is found to be 11.35 volts which is well above $1/3 V_{cc}$. The initial state of the timer is set by grounding P2-36 and turning the power off. This allows the two timing capacitors C7 and C9 to fully discharge. When the voltage is reapplied and the input P2-36 opened up, the capacitor C7 holds the trigger voltage down for a short time, T2, which causes the timer to be triggered. The trigger voltage must however rise above the 555 requirement of $1/3 V_{cc}$ before the 15.25 seconds have elapsed or the internal flip-flop will not switch states. It can be seen by using the time-voltage equation for an RC network that $1/3 V_{cc}$ or 5 volts will be reached in about 0.4 seconds which is very adequate.

$$\begin{aligned}
 T2 &= -(RC)\ln(1-V_{out}/V_{in}) \\
 &= -(150E3)(4.7E-6)\ln(1-5/11.35) \\
 &= 0.41 \text{ seconds.}
 \end{aligned}$$

R = R44, C = C7, V_{in} = 11.35 volts, V_{out} = 5volts.

Once the trigger voltage exceeds $1/3 V_{cc}$, the internal comparator waits for the threshold voltage to reach $2/3 V_{cc}$ at which time the output will flip states. The output at pin 3 is initially high or approximately 15 volts. After the timer is triggered by opening up P2-36, the capacitor C9 begins to charge up until $2/3 V_{cc}$ is reached. At this time, T1, which was calculated to be 15.25 seconds, the output at pin 3 drops to approximately 0 volts.

2. P2-12 Output Circuit

The P2-12 Output Circuit is directly controlled by the output of the U3 timer. The schematic is included in FIGURE 31 of APPENDIX C. When the output of the timer U3 is high, the transistor Q19 turns on shorting the cathode side of zener VR9 to ground. Transistor Q20 then turns off and the reverse current flowing through the 4.7 volt zener VR5 turns the transistor Q9 on. The output P2-12 is shorted to ground through Q9 and a TTL logic 0 will be measured.

After the 15.25 second timer has expired and the output at pin 3 drops low, Q19 will turn off. The reverse

current flowing through the 4.7 volt zener VR9 will turn transistor Q20 on causing the cathode side of zener VR5 to be grounded. Transistor Q9 then turns off and the output P2-12 is forced to a TTL logic 1 by the 1-kohm pull-up resistor. A summary of these states is shown below.

<u>U3-pin3</u>	<u>Q19</u>	<u>Q20</u>	<u>Q9</u>	<u>P2-12 state</u>
HIGH	ON	OFF	ON	LOGIC 0
LOW	OFF	ON	OFF	LOGIC 1

J. 1.5 Second Timer (33010-33020)

Test number 33010 and 33020 test the performance of the 555 timer U25. The schematics for these tests include FIGURES 29, 30, and 32 which are located in APPENDIX C. Several inputs have an effect on the output at connector pin P2-44. The timer U1 which was tested in test series 31000 is used again along with input connector pins P2-11 and P2-35. These three sources control the node labeled "1" in FIGURE 29. This node is continued on FIGURE 30 and controls the Q7/Q8 Transistor Circuit with output at node 2. FIGURE 32 shows the continuation of node 2 which feeds into an opto-isolator Q44. The output from this device feeds into a NAND gate, U24, along with the input from connector pin P1-34. The output from the NAND gate is what triggers the timer U25 and controls the state of the output at P2-44.

To begin, the input P2-36 is still left open from the previous tests so that the output at pin 3 of timer U1 is low or approximately 0 volts. A TTL logic 0 is also still present on the inputs P2-11 and P2-35. The combination of these three inputs cause the voltage at node 1 to be at approximately 0 volts. From FIGURE 30 and the Q7/Q8 Transistor Circuit analysis it is determined that a voltage level of this magnitude is not enough to turn on the transistor Q7. Because of this, the transistor Q8 cannot be turned on either and the voltage at node 2 will be approximately equal to 25.5 volts. This voltage level is obtained by isolating the components shown in FIGURE 8 and calculating the voltage at node 2.

Thevinize the right hand part:

$$\begin{aligned} V_{th} &= [(28 * R_{169}) + (27.3 * R_{28})] / [R_{169} + R_{28}] \\ &= [(28 * 1.5) + (27.3 * 2)] / [1.5 + 2] \\ &= 27.6 \text{ volts.} \end{aligned}$$

$$\begin{aligned} Z_{th} &= R_{169} // R_{28} = (2 * 1.5) / (2 + 1.5) \\ &= 857 \text{ ohms.} \end{aligned}$$

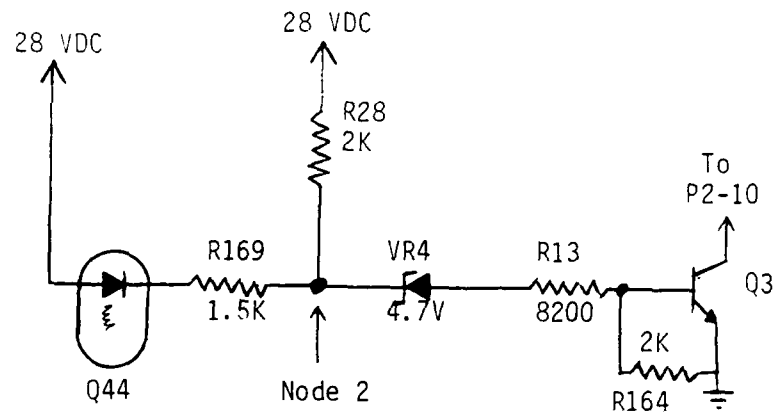


FIGURE 8 - The Voltage at Node 2

Now take the sum of currents:

$$[(27.6-V_2)/857] = [(V_2-4.7-.7)/(8200)]$$

$$8200(27.6-V_2) = 857(V_2-5.4)$$

$$V_2(8200+857) = 226320+4627.8$$

$$V_2 = 230947.8/9057$$

$$= 25.5 \text{ volts.}$$

By looking at the U25 Timer Circuit, it can be seen that 25.5 volts at node 2 does not provide enough current through the opto-isolator Q44 to turn it on. Therefore the TTL logic level at pin 5 of U24 NAND gate is a 1 and remains this way throughout the test. Pin 4 of the NAND gate is connected to the input pin P1-34 which is initially a TTL logic 1 and then dropped to a TTL logic 0 five seconds later. During this test the output of the NAND gate is simply the TTL inversion of P1-34.

1. U25 Timer Circuit

Timer U25 is used here as a one-shot as the others were but the configuration is somewhat more complicated. A PNP switching transistor, Q47, is used to ground the threshold input at pin 6 while the trigger input at pin 2 is connected directly to the output of the NAND gate. The initial state of the NAND gate output is TTL logic 0 which turns transistor Q47 on and forces the trigger input to a low voltage potential. The specifications for a 555 timer

reveal that the output at pin 3 will then remain in the high state. The timing equation for the U25 configuration is obtained using the time-voltage relationship for an RC network. In this case however, the emitter-collector voltage present in Q47 does not allow the timing capacitor to discharge fully. This voltage potential must be included in the equation as the initial voltage of the capacitor. The control voltage at pin 5 is again set to $1/2 V_{cc}$ by means of the 10-kohm resistor (R175) placed in parallel with C29 (see control voltage analysis for the U2 Timer Circuit).

$$\begin{aligned}
 T1 &= -(RC)\ln[1-(V_{out}-V_{ce})/V_{in}] \\
 &= -(R173)(C28)\ln[1-(V_{in}/2-V_{ce})/V_{in}] \\
 &= -(1.5)(1)\ln(.5+V_{ce}/5) \quad \text{where } V_{ce} = 0.3 \text{ vdc} \\
 &= 0.87 \text{ seconds.}
 \end{aligned}$$

To sum up the operation of the circuit for test number 33010, the timer output at pin 3 is initially high while the input P1-34 is held high. When P1-34 is grounded (TTL logic 0), the output of the timer is forced low approximately 0.87 seconds later. While the output of the timer is high, the transistor Q48 will be turned on providing a ground for the opto-isolator Q45. It then turns on along with the transistor Q46. The output P2-44 is then grounded and a TTL logic 0 is measured. After the 0.87 seconds have elapsed and the output of the timer drops low,

Q48, Q45, and Q46 turn off simultaneously and the output P2-44 is forced to a TTL logic 1 by the 1-kohm pull-up resistor.

The second part of this test, test number 33020, is identical to test number 33010 except for the input at P1-34. In this test the input used is a gated pulse train which is supposed to simulate the actual signal that would be present on the weapons system. This signal consists of a square TTL waveform with a pulse width of 18.5 milliseconds and a period of 684.5 milliseconds. A burst of pulses is superimposed on top of the 18.5 millisecond pulses and these burst pulses have a pulse width of 800 nanoseconds and a period of 20 microseconds. The test requirements call for this pulse to be applied to the input P1-34 for 5 seconds and then ground P1-34 measuring the time it takes the output at P2-44 to switch states.

From the above analysis it was seen that a TTL logic high at P1-34 would lock the timer U25 in the ready or high state and upon grounding of P1-34, the timer would switch states approximately 1 second later. The gated pulse train applied has a 800 nanosecond high time which is sufficient to keep the timer reset or in other words the time that the input at P1-34 is low is not enough to allow the threshold voltage across the timing capacitor to charge to $1/2 V_{cc}$ before being reset by the high pulse. As long as the circuit is working properly, this gated pulse input can be

considered a high input and the test works exactly as analyzed in the above test.

K. POWER ON SEQUENCE LOGIC TEST (34000)

The Power On Sequence Logic Test involves ten separate tests each of which includes a set of five inputs and 14 separate outputs. The test description is laid out in a logic table on page 14 of the TR document in APPENDIX C. This series of tests involves several of the CCA circuits discussed earlier plus four additional circuits which will be analyzed in this section.

1. P2-1 Input Circuit

The CCA input pin P2-1 is an open collector logic type which controls a transistor/opto-isolator switching circuit. The state of this circuit has an affect on several other circuits. The schematic for this circuit can be seen in FIGURE 33, located in APPENDIX C. The one output of this circuit is taken at the collector of Q34. It is assumed that all of the comparator circuits are off for this analysis. If any of these circuits were on, the transistor Q34 would remain on constantly.

The analysis of this circuit is straight forward using simply the logical states of the transistors. When P2-1 is grounded, the base of Q43 is essentially zero and the transistor is off. Current then flows from the 27 volt source through R143, CR24, and CR23 turning the transistor

Q34 on. The optical isolator Q40 is also on but its output does not affect this circuit. When Q34 is then turned on, the collector is essentially grounded and the circuit is considered to be in the low state.

When P2-1 is released from ground, the opposite states occur. The 27 volt source is enough to reverse bias the 4.7 volt zener diode VR15 and turn the transistor Q43 on. The voltage on the collector then falls too low to keep Q34 on so it turns off. The collector of Q34 is then pulled up by the resistor R98 which is tied to the 28-volt power supply. The circuit is then considered to be in the high state.

2. Flip Flop Circuit

The circuit which the author calls the Flip Flop Circuit is shown in FIGURE 33 of APPENDIX C. This circuit has two inputs labeled one and two and one output labeled node 4. Input number 1 turns on the transistor Q22 and input number 2 will turn on transistor Q21 but only one transistor at a time can be on.

The analysis starts by looking at the portion shown in FIGURE 9 and determining the voltages and currents assuming that the transistor Q21 is off.

$$I = (28 - 0.7) / (2400 + 18000 + 8200) = 0.955 \text{ mA}$$

$$\begin{aligned} V_x &= 28 - I \cdot 2400 = 28 - 0.955 \cdot 2400 \\ &= 25.7 \text{ volts.} \end{aligned}$$

The voltage V_x is the voltage at node 4 and with Q21 off and Q22 on, this voltage is approximately 25.7 volts. When Q21 is on and Q22 is off as shown in FIGURE 10, the analysis changes.

$$28 - 0.1 = I_1(330 + 2400) + I_2(2400)$$

$$27.9 = I_1(2730) + I_2(2400)$$

$$I_1 = 0.0102 - 0.8791 \cdot I_2 \quad (4)$$

$$28 - 0.7 = I_1(2400) + I_2(2400 + 18000 + 8200)$$

$$27.3 = I_1(2400) + I_2(28600) \quad (5)$$

Plug EQ. 4 into EQ. 5:

$$27.3 = 2400(0.0102 - 0.8791 \cdot I_2) + I_2(28600)$$

$$= I_2(26490) + 24.48$$

$$I_2 = 0.1065 \text{ mA.}$$

From EQ. 4:

$$I_1 = 0.0102 - 0.8791(0.1065 \text{E-}3) = 10.11 \text{ mA.}$$

$$V_x = 28 - (I_1 + I_2)2400 = 28 - (10.2165)2.4$$

$$= 3.5 \text{ volts.}$$

The voltage at node 4 when Q21 is on and Q22 is off is therefore approximately 3.5 volts and the circuit is considered to be in the low state. A truth table for the

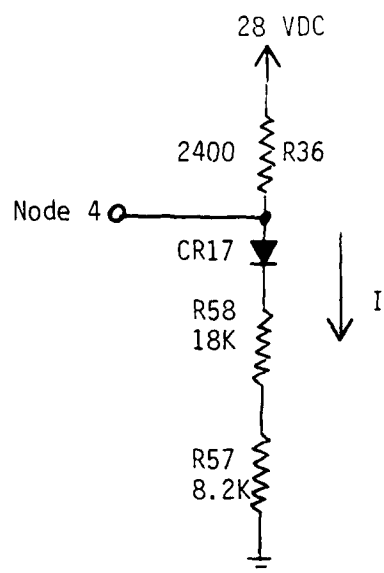


FIGURE 9 - A Portion of the Flip Flop Circuit

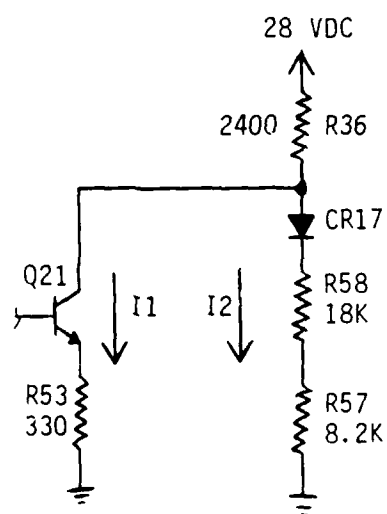


FIGURE 10 - A Portion of the Flip Flop Circuit

operation of the Flip Flop Circuit is shown in TABLE 2. A truth table showing the operation of the Flip Flop Circuit along with the conditions which control it and the P2-13 Output Circuit is shown in TABLE 3.

3. P2-13 Output Circuit

As seen on the schematic diagram shown in FIGURE 34 of APPENDIX C, the CCA output pin P2-13 is controlled by three sources: the P2-35 input pin, the P2-1 Input Circuit just discussed, and the output from the U3 Timer Circuit. These three sources are wire-ORed together by the diodes CR12, CR11, and CR14. When any of the three sources are in the high state, the transistors Q17 and Q16 turn on. The transistor Q17 turns on whenever the voltage at the emitter exceeds the base voltage, determined by R38 and R39 to be 10 volts, plus the base-emitter voltage of about 0.7 volts. The cathode side of the 4.7 volt zener diode VR6 is then grounded and Q15 turns off. The output at pin P2-13 is then pulled high by the 1-kohm pullup resistor and a TTL logic 1 would then be measured.

All three sources must be in the low state in order for Q16 and Q17 to be off. When this state occurs, the current supplied by the 28 volt power supply through R63 and the zener VR6, which is now reversed biased, is enough to turn on transistor Q15. The output pin P2-13 is then shorted to ground resulting in a TTL logic 0.

TABLE II

TRUTH TABLE FOR THE FLIP FLOP CIRCUIT

INPUT 1	INPUT 2	OUTPUT NODE 4
0	0	NO CHANGE
0	1	LOW
1	0	HIGH
1	1	DOES NOT EXIST

TABLE III

TRUTH TABLE FOR FLIP FLOP CIRCUIT, P2-13 OUTPUT
CIRCUIT, AND CONTROLLING INPUTS

P2-1	P2-36	P2 35	U3 OUTPUT	INPUT 1	INPUT 2	NODE 4	P2-13
0	0	0	HIGH	0	1	LOW	1
0	0	1	HIGH	0	1	LOW	1
0	1	0	LOW**	1	0	HIGH	1
0	1	1	LOW**	1	0	HIGH	1
1	0	0	HIGH	0	1	LOW	1
1	0	1	HIGH	0	1	LOW	1
1	1	0	LOW**	0	0	LOW*	0
1	1	1	LOW**	0	0	LOW*	1

* There is no change in this state. The output of the Flip Flop Circuit remains in the LOW state.

** The output of the U3 Timer, pin 3, will go low 15 seconds after P2-36 goes from low to high.

4. P2-37/38 Output Circuit

The two CCA output pins P2-37 and P2-38 are connected in series through two optical isolators Q11 and Q12. The schematic for this circuit is shown in FIGURE 35 of APPENDIX C. The state of the two opto-isolators are always the same and are controlled by the three sources: U1 Timer output, U3 Timer output, and the P2-1 Circuit output. The three sources are also wire-ORed together by the diodes CR6, CR25, and CR13 which feed into and control the emitter of the transistor Q14. When the output of the U1 or U3 Timer Circuits is high, this point will also be high forcing transistors Q13 and Q14 to be turned on. This also occurs whenever the output from the P2-1 circuit is low which causes transistor Q18 to be off. The pullup resistor R41 tied to the 28 volt supply then allows current to flow through CR13 and turn Q14 on. A truth table showing the state of the three inputs versus the level at the node labeled 4 is shown in TABLE 4.

Whenever the node labeled 4 is in the high state, transistors Q13 and Q14 are on which shorts out the opto-isolators Q11 and Q12. The two 1-kohm pullup resistors connected to the P2-37 and P2-38 output pins then force these outputs to a TTL logic 1 level. Transistors Q13 and Q14 turn off when node 4 is at the low state and the opto-isolators then both turn on. The output P2-37 is shorted to ground resulting in a TTL logic 0 and the output

TABLE IV
P2-37/38 OUTPUT CIRCUIT TRUTH TABLE

P2-1	P2-36	U1 OUT	U3 OUT	P2-1 OUT	P2-37	P2-38
0	0	1	1	0	1	1
1	0	1	1	1	1	1
0	1	0*	0*	0	1	1
1	1	0	0	1	0	0**

* The U1 output goes low 315 seconds after P2-36 is opened up. The U3 output goes low 15 seconds after P2-36 is opened.

** P2-36 is low if P2-14 is grounded, otherwise it remains high.

P2-38 also becomes grounded if the control pin P2-14 is tied to ground. If this is the case (normal operation), then P2-38 and P2-37 will always be in the same state. Otherwise the output P2-38 will remain in the TTL logic 1 condition.

IV. ACCEPTANCE TEST PROGRAM DESCRIPTION

A. Program Header and Initial Conditions

All programs written for use with the TE304 follow standardized testing procedures and format such as the header seen on the Acceptance Test program listing in APPENDIX F. These program format development procedures are required by the Navy and do not pertain to this thesis project and therefore will not be discussed. However descriptions of how each of the individual circuit tests are performed will be discussed. It is also assumed that the reader has a basic understanding of the HP Basic 3.0 programming language.

The header used on all the TE304 software is identical to that in the program listing which runs from the beginning to line number 470. This header contains the common variables used by the system software and also loads all of the subprograms from the hard disk drive. Program line 220 disables the keyboard, including the RESET key, which prevents the operator from interrupting the testing process except for the few times he or she is prompted by the computer. Program lines 240 through 340 contain the global or common variables found in the main program and in the subprograms and line number 350 dimensions the variables used only in the main program. The Subprograms, which are

stored in three directories, are loaded into the computer by lines 360 through 410. The remaining part of the header simply enables the interface interrupt lines and sets up the softkeys and keyboard handling routine.

The initial conditions for testing the CCA are described in the TR but will be repeated here briefly. The CCA requires three power supplies. The first power supply has an amplitude of +28 volts DC and is connected to pins P1-18, 19, and 43. The second power supply is set at +5 volts DC and is connected to pins P2-24 and 48. Power supply number three is set for -5 volts DC and is connected to pin P2-47. Pins P1-17, P1-27, P1-42, P2-14, P2-17, P2-25, and P2-49 are grounded. In addition to the power requirements, there are simulated resistive loads which must be connected to various CCA pins. These loads are listed on page 7 of the TR in APPENDIX A. The HP Digital Read Card in the Multiprogrammer provides the 1 kohm pullup resistors so only four resistors are needed in the patchbox adapter circuit.

B. Patchbox Identification Check

Before any CCA test can be performed on the TE304, a patchbox identification check must be performed to insure that the right patchbox is inserted for the test being run. This prevents mishaps such as damaging the patchbox circuitry or the CCA itself. A rather simple and

standardized method is used to accomplish this.

Each patchbox contains two resistors which are connected between Measurement Matrix points 98, 99, and 100 with no two patchboxes having the same values. The actual identification test, which is performed in program lines 520 through 650, simply checks the resistance of these two resistors by closing the above matrix points to the Digital Multimeter, which is set up for four wire ohm measurement. The measured values are then compared to assigned values written in the software. If the values do not match then the program will abort giving a patchbox identification error. The FIT subprogram is used for this purpose because these two tests are only a check and do not have any test numbers assigned to them.

C. Continuity Tests (10010-10160)

This series of 16 tests simply checks the wire lands between the CCA connector pins and the CCA test point connector. Two CCA resistors are also checked as a verification of the correct board. This is for the same reasons that the patchbox identification test described above was performed. Program lines 670 through 930 contain the software for this series of tests which is quite straight forward.

All the data including the matrix points and the test numbers are contained in DATA statements at the

beginning of the test series. Matrix points of the right coordinates are closed successively while the Digital Multimeter reads the resistance between the two points. This is accomplished in a FOR-NEXT loop which takes care of closing the correct matrix relays, taking the readings, and comparing the reading to the TR specifications. If any of these tests fail, the program will automatically abort to protect against damage that would occur if the wrong board was plugged into the Test Set. Because these are actual CCA tests, the FNTEST function is used to compare the results, print the results on the screen, and store the results in a large array for later use.

D. Current Demand Tests (11010-11030)

In the Current Demand test sequence, program lines 950 through 1250, the power to the CCA is turned on and the current drawn from each of the three power supplies is read back from the supply (the HP 6034A Power Supplies have this feature). If any of the power supplies exceed a current limit of 1 amp, the program will abort. Otherwise the readings are compared with the TR tolerances and the results printed on the screen and stored using the FNTEST function. Also as a double check the supply voltages are measured using the Digital Multimeter and the FIT subprogram.

E. Patchbox Circuit Test

Any circuitry used in the Patchbox Adapter Interface must be tested for proper operation. In this case only one integrated circuit is used and the testing made very simple. The schematic for the circuit is shown in Figure 1 of APPENDIX D.

The 5 volt supply is first connected to the circuit through one of the Multiprogrammer relays and then five tests are performed on the circuit. These tests are described on page 2 of the Fault Isolation TR which is contained in APPENDIX B and duplicated in Table 5. Again, because these are not CCA tests, the FIT subprogram is used and the program is aborted if any of the five tests fail.

F. TIM Reference Voltage (20010)

The TIM reference voltage test is a DC voltage measurement which roughly checks the regulator circuit on the CCA. The measurement is taken at the P2-27 connector pin with an expected value of 5.1 volts. The software for this test is contained in program lines 1550 through 1650 and uses the FNTEST function to perform this single test. Matrix points are closed and opened using the STIM subprogram and the measurement taken using the Digital Multimeter and the FNDVMR function.

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AUTOMATED TESTING AND FAULT ISOLATION OF A LOW
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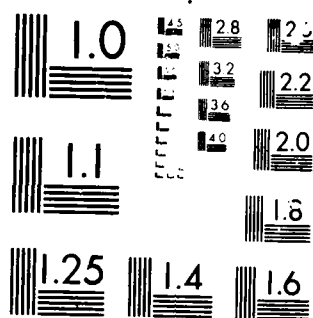


TABLE V
PATCHBOX ADAPTER CIRCUIT TEST DESCRIPTIONS

IO CODE	TEST DESCRIPTION	NOMINAL AND UNITS	LIMITS
	Apply Logic 1 to adapter pin A33 (DW#2). Apply pulse train to adapter B34 with a 10 msec period and a 1 msec pulse width.		
TESTX1	Measure pulse width at B32.	1 msec	0.5 1.5
TESTX2	Apply Logic 0 to A33 and measure pulse width at B32.	0	0
TESTX3	Measure TTL level of A33.	LOGIC 0	.8 vdc 0 vdc
TESTX4	Apply Logic 0 to A22 (DW#0). Measure pin A20.	LOGIC 0	.8 vdc 0 vdc
TESTX5	Apply Logic 1 to A22 and measure pin A20.	LOGIC 1	5.2 vdc 2.4 vdc

G. AC/DC Gain Tests (21010-21430)

As seen in the Acceptance Test TR contained in APPENDIX A, there are 9 AC gain tests and 3 DC gain tests. These are all performed on 741 operational amplifiers on the CCA and are all very similar in circuit configuration. It is for this reason that the testing is condensed into one software loop which includes program lines 1710 through 1960. The threshold and TTL output tests which do fall into this testing series are performed after the gain tests are completed. An individual gain test involves connecting a stimulus, either AC or DC, to the indicated connector pins, which are op-amp inputs, and then measuring the outputs at the specified pins. The input signal is also measured and the gain of the circuit calculated and compared to the tolerances in the TR.

All of the AC gain tests involve frequencies of 1 and 10 Hz which are too low for the HP1980A Oscilloscope to measure accurately. The Digital Multimeter is used to digitize the waveforms and then calculate the equivalent rms value in volts DC. This method is very accurate and provides excellent results. The program lines used to accomplish this are 1860 and 1870 for the input signal and 1890 and 1900 for the output signal. Program lines 1980 through 2090 contain the DATA statements for the test series and include the test numbers limits, input frequencies and

amplitudes, and the matrix point coordinates.

If the frequency read from the DATA statements is zero then a DC gain measurement will be performed. In this case the Multimeter reads the input and output voltages directly in DC volts. The gain is then calculated and the result compared to the tolerances using the FNTEST function.

H. DC Threshold Tests (21050-21450)

The five threshold tests are performed on the CCA comparators and are an extension of the op-amp tests described above. An initial DC voltage is applied to the specified CCA connector pin using the Digital Voltage Source and then incremented or decremented in 10 mV steps until a specified output pin, which is being continuously monitored by the Multimeter, switches from one state to another.

Again the software accomplishes these tests in a FOR-NEXT loop running from lines 2140 through 2390. This loop takes care of applying the initial voltage, incrementing or decrementing it, and monitoring the output voltage until it switches to the specified logic level. When this occurs, the input voltage at that time is compared to the limits in the TR using the FNTEST function. The DATA statements in lines 2400 through 2440 contain the test numbers, limits, initial voltage, matrix point coordinates, and the logic switch level to be monitored for each of the five threshold tests.

I. TTL Output Tests (21260 and 21270)

Program lines 2460 through 2630 contain the software for the two TTL output tests. Two additional outputs of the comparator circuits used in the threshold tests are tested for proper level, which make these tests simply an extension of the threshold circuit tests described above. A DC voltage is applied to the P2-29 and P2-28 CCA input pins and the TTL logic level of the P1-47 connector pin is measured. The only difference between the two tests is the voltage level applied to an additional input pin (P2-6). In the first test this pin is left open and in the second test 28 volts is applied to it.

Both tests are performed in the same FOR-NEXT loop in the software while only changing the test number, limits, and input voltages accordingly. The test number and limits are read from the DATA statement on line 2630 and the FNTEST function used to compare and store the results.

J. Full Power CDC/FPD Logic Test (30010)

There are six individual readings which are taken during this test series. Each of the readings represent a TTL logic output which corresponds to a specified set of inputs shown on page 12 of the Acceptance Test TR contained in APPENDIX A. The CCA connector pin P2-39 which is of open collector logic is one of the inputs and the +5 volt power

supply is the other input. The circuits tested here include two almost identical optically isolated switching networks with one of the outputs on pin P2-41 and the other on pin P2-15. The third part of the test is performed with the +5 volt power supply turned off.

The software which performs this test series includes program lines 2650 through 2810. Again a loop is used to simplify and shorten the measurement routines. The two TTL output pins P2-41 and P2-15 are monitored by the Digital Read Cards in the Multiprogrammer and the subprogram FNDR\$ used in line 2750. The comparison of the readings and the TR limits is done in lines 2760 through 2780 by the FNTEST function which actually stores and displays the data.

K. Power On Sequence Logic Test Part 1 (34010-34040)

This series of test performs the first four tests of a ten test TTL logic table seen on page 14 of the TR document contained in APPENDIX A. Each of the ten tests includes a specified set of five input conditions, some of which are TTL logic, and a set of 14 TTL logic outputs which must match those listed in the TR. Almost all of the outputs are measured using the Digital Read Cards in the Multiprogrammer and the FNDR\$ software function. The additional outputs are measured with the Digital Multimeter and converted to logic levels using the FIT subprogram.

Program lines 2830 through 3420 contain the software

needed to perform these four tests. Again a large loop is used to accomplish this easily. Initial CCA conditions are required for this series of test and these inputs or states are set up by the statements in lines 2860 through 2950. These statements connect the matrix points and turn on the power supplies required by the TR as initial conditions and also configure the Pulse Generator and the Pulse/Function Generator for the required pulse train needed as one of the five inputs.

It was necessary to add an additional test prior to beginning this series. The gated pulse train mentioned above is applied to a NAND gate which has been a common failure on this CCA. In order not to load down this pulse train, it was necessary to check the accuracy of this input with the stimulus applied. Because this is an actual test of the CCA it was given a test number of 90010 and will be added to the TR in future documents.

The four tests are performed inside of the FOR-NEXT loop which applies the specified inputs, takes all 14 of the readings, and compares them to the TR. The string of 14 logic levels is converted to an octal number in lines 3310 and 3320 and this number compared to the octal equivalent listed in the nominal column in the TR. The DATA statements in lines 3390 through 3420 contain the test number, input logic levels, and the octal equivalent of the expected output levels.

L. 5 Minute and 250 Msec Timers (31010 and 31020)

Two 555 timers which are connected in series (one timer triggers the other timer) are tested here for accuracy of time delay. The first timer, U1, has a nominal time delay of 315 seconds and the second timer, U2, has a time delay of 250 milliseconds. Again initial conditions are required to perform these tests and these are identical to those discussed in the Power On Sequence test discussed above. Additionally, the timing capacitors used by the two 555 timers have to be completely discharged. This is accomplished by grounding the trigger input pin P2-36 and turning off the power supply for 60 seconds. The power is then turned back on, the trigger pin opened up, and the delay times measured. The 250 millisecond timer delay is measured by the Frequency Counter while the 5 minute delay measured by the Computer.

Program lines 3450 through 3930 contain the software for these two test and is fairly straight forward. The initial conditions which were set up in the previous Power On Sequence test are left on so it is not necessary to repeat them in this section. As with all the tests performed on the TE304, provisions for a test repeat are available. However in this case, if the test is repeated, the timing capacitors must be completely discharged before taking a second reading. An IF-Then-Else format is used to

accomplish this and is seen in lines 3530 through 3650. If it is the first time through with the test then the capacitors are discharged as mentioned earlier for 60 seconds. Any repeat of the test forces the capacitors to be discharged for a full 330 seconds because the power supplies cannot be turned off as they were for the first test.

Once the capacitors have been discharged the trigger pin P2-36 is opened by the OC (open collector) subprogram and the Open Collector Card in the Multiprogrammer and the time measured for the outputs at pins P2-10 and P2-9 to switch states. The 315 second delay is measured using the clock in the computer and the REPEAT-UNTIL loop shown in lines 3750 through 3790. The 250 millisecond delay is measured by the Frequency Counter and the FNCNTR function shown in line 3810. These measurements are then compared to the limits in the TR and the results stored and displayed by the FNTEST function.

M. 1.5 Second Timer Test (33010 and 33020)

The 555 timer (U25) circuit is tested in this pair of tests. The same initial conditions for the CCA apply here and are still active from the 5 Minute Timer test. The trigger input for this timer is CCA connector pin P1-34, which is the same pin that the gated pulse train was applied to in the Power On Sequence Logic test. The first of the two test calls for a TTL logic 1 to be applied to this pin

and to wait 5 seconds causing the timing capacitor to be discharged. A TTL logic 0 is then applied to the P1-34 input and the time delay at the output pin P2-44 measured. The second test is identical to the first however the gated pulse train specified in the TR is applied in place of the 5 second TTL logic 1.

The Acceptance Test program lines number 3950 through 4240 perform these two tests and are fairly straight forward. The Frequency Counter is used to measure the time delay and is connected by the Stimulus Matrix and configured in lines 3970 and 4010. The Digital Voltage Source and the DVS subprogram are used to apply the TTL logic levels in lines 3990 and 4020. In the first test the measurement is taken in line 4040 using the FNCNTR (function Counter read) function and the results stored and displayed by the FNTEST function.

In the second test, test number 33020, the gated pulse train is applied using the Pulse Generator and the Pulse/Function Generator. These instruments are configured using their respective subprograms in lines 4110 and 4120. The Digital Write Card in the Multiprogrammer is used in conjunction with the Patchbox Adapter Circuit to turn this pulse train on and off while triggering the Counter to take a reading at the same time. This is accomplished in lines 4130 through 4160 and the reading entered into the computer using the FNCNTR function as before.

N. Power On Sequence Logic Test Part 2 (34050-34100)

This series of test includes six test numbers and is the second half of the previously discussed Power On Sequence Logic test. The initial conditions are all the same and the format of testing is identical having the same five inputs and 14 outputs. The logic table is listed on page 14 of the TR document contained in APPENDIX A and this series of test refers to tests 5 through 10 on that table.

The software for this series of test is similar to that of the first half of the Power On Sequence test with the readings being taken by the Digital Read Cards in the Multiprogrammer and the Digital Multimeter. This section includes program lines 4260 through 4900 and contains a large FOR-NEXT loop which applies the input logic levels, takes the readings, converts them to an equivalent octal number as before, and compares the results to those of the TR. The subprograms and functions are the same as those used and discussed above. The initial conditions described in part 1 of this series are removed upon completion of the last test in lines 4790 through 4840.

O. 20 Second Timer Test (32010)

The 20 Second Timer test is the last single test of the CCA Acceptance Test Program and measures the time delay of the 555 timer U3. The CCA connector pin P2-36 is the

trigger for this timer and this pin is grounded and the power supply turned off for ten seconds in order to discharge the timing capacitors. When the power is reapplied and the trigger released using the Open Collector Output Cards in the Multiprogrammer, the time delay is measured at the P2-12 output pin using the clock in the computer.

Program lines 4920 through 5180 contain the software for this last test and runs straight through with no loops. Two REPEAT-UNTIL loops, which run from lines 4970 through 5000 and lines 5060 through 5100, are used however to create the ten second delay and make the actual time delay measurement of the timer. The measurement is then compared to the tolerances given in the TR, stored, and displayed by the FNTEST function in line 5170. Upon completion of this last test, the END_TEST program is loaded and run by the statement in line 5250.

V. FAULT ISOLATION TEST PROGRAM DESCRIPTION

A. Overview

The Fault Isolation Program for the CCA is listed in APPENDIX G and follows the same standardized testing format as that of the Acceptance Test Program. However a few major changes in the way the program is run have been made. The Acceptance Test Program is run straight through with little or no operator intervention. In the case of the Fault Isolation Program, the operator runs different fault isolation tests for different circuits on the board from a menu on the screen. The operator is also required to connect various probes and integrated circuit clips to the components on the CCA so that additional measurements otherwise not available can be obtained. The Test Set operator is only required to run fault isolation on those circuits which fail the acceptance testing.

The header of the Fault Isolation Program, which ends at line number 640, is very similar to that of the Acceptance Program. It contains the same common or global variable declarations, a section which loads all the subprograms and functions from the hard disk drive, and an additional section which enters data from files used to display the CCA components layout on the screen. This graphical display of the CCA aids the operator in finding

parts that require a probe or chip clip to be connected. The softkeys and keyboard handling routines are also enabled in this header.

Before any power is applied to the CCA, the software must check that the correct Patchbox and CCA are inserted into the TE304 Test Set. This is accomplished in the same manner as that in the Acceptance Test Program. The program lines which perform these checks are 660 through 970. If any of these two checks fail, the program will abort giving an error message accordingly.

Once the correct Patchbox and CCA have been verified, power is applied to the CCA and the current demand tested. If one or more of the power supplies exceed the specified limit, the computer will prompt the operator if he or she wishes to continue. It is possible in this case to feel the components on the CCA for one that is too hot and probably defective. Program lines 980 through 1240 perform these steps and continue on if the currents are acceptable.

After power is applied to the CCA, a mandatory series of tests is performed on the voltage regulator circuit. This circuit provides reference voltages throughout the board and has been known to cause catastrophic failures. The subroutine which performs this test series will be discussed later. However, following completion of the voltage regulator test, a menu is displayed on the screen which allows the operator to run any

series of fault isolation tests on the various circuits that make up the CCA. Program lines 1290 through 1520 contain the menu and associated logic and upon completion of any of the fault isolation test series, the program will return to this menu. Item number 18 in the menu is provided for terminating the program.

B. Voltage Regulator Circuit (200110-200170)

As described in the Fault Isolation TR contained in APPENDIX B, there are 7 individual tests which make up this series. The subroutine T20010 which performs this series begins on line number 1740 and ends at line number 2360. This subroutine, as do all the fault isolation subroutines and subprograms, contains one section which performs the tests and a second section which determines which components on the CCA, if any, are bad. The FIND_IT subprograms used in lines 1800 through 1850 instruct the operator to connect the measurement probes to the various CCA components. The test numbers, limits, and matrix point coordinates are contained in the DATA statements on lines 1870 through 1890.

The seven tests are performed in a FOR-NEXT loop which runs from line 1910 to 2120. This loop sets up the testing conditions as specified in the TR, takes the reading using the Digital Multimeter, and compares the results to the limits using the FNTEST function.

These seven measurements are used in the fault isolation flow chart to determine any faulty components. The flow chart for this test series is shown in Figure 1 of APPENDIX E. The software equivalent of this flowchart begins at line 2140 and ends at line 2340 and uses the FOUND_BAD subprogram to display, print, and store the resulting bad parts.

C. VBMT, IFKT, and IFMT Op Amp Circuits (210010-214060)

There are three operational amplifier circuits on the CCA which are tested for proper gain at different frequencies. Each of the three independent fault isolation routines for these circuits are exactly identical except for the test numbers, part numbers, and a few voltage readings. These three series have six individual tests, plus one check called Test8, that fault isolate the VBMT, IFKT, and IFMT operational amplifier circuits respectively. The first five tests involve DC voltages and the sixth test an AC voltage. The additional calculation called Test8 is needed for one of the fault isolation flowchart branches. Descriptions of each individual test can be found in the Fault Isolation TR located in APPENDIX B under test numbers 210010 through 210060 for the VBMT circuit, 212010 through 212060 for the IFKT circuit, and 214010 through 214060 for the IFMT circuit.

The subroutine used for the VBMT op amp circuit

begins on line number 2400 with the subroutine name T21010 and ends on line number 3120. Because the AC signal and readings used in the fifth test are at 10 Hz, the Digital Multimeter must be used to digitize the waveforms and calculate the rms values. These digitized waveforms are stored in arrays which are allocated in line 2430. The 741 operational amplifier must have a chip clip attached to it and this is accomplished using the FIND_IT subprogram in line 2450. Test numbers, limits, and matrix point coordinates are contained in the DATA statements on lines 2470 and 2480.

Once again a FOR-NEXT loop is used to set up the individual testing conditions, close the appropriate matrix points, take the measurements, and compare the results to the limits. This loop begins on line 2530 and ends on line 2820. Inside this loop there is an IF-THEN-ELSE format which separates the DC tests from the AC test. The FNDVMR function is used to take the DC readings in line 2660 and the DVM_TIME and FNDVMRMS subprogram and function used to digitize the AC waveforms and convert them to an rms value in lines 2740, 2750, 2780, and 2790. After all six measurements have been completed, the Function Generator used for the DC and AC stimulus is turned off by the TOGGLE subprogram in line 2840 and the waveform storage arrays are deallocated or erased from memory in line 2860.

The second major section of the routine performs the

actual fault isolation in accordance with the fault isolation flowchart for this circuit which is shown in Figure 2 of APPENDIX E. Program lines 2870 through 3100 implement this flowchart using IF-THEN-ELSE statements and the FOUND_BAD subprogram to indicate the bad parts. Line number 3120 forces program flow back to the menu after completion of this test series.

The IFKT and IFMT operational amplifier routines are identical to the VBMT routine described above. The IFKT subroutine is labeled T21200 and begins on line 3730 and the IFMT subroutine is labeled T21400 and begins on line 5900. The fault isolation flowcharts are shown in Figures 4 and 7 of APPENDIX E.

D. Comparator Circuits (210510-214570)

There are a total of five comparator circuits on the CCA. The test numbers 210510 through 210570 pertain to the VBMH comparator which is an extension of the VBMT op amp circuit described above. The second and third comparator circuits are labeled IFKL and IFKH and include test numbers 212410 through 212570. These two circuits are extensions of the IFKT op amp circuit. The last two comparator circuits are extensions of the IFMT op amp circuit and are labeled IFML and IFMH using test numbers 214410 through 214570. All five fault isolation routines are very similar with differences only in test numbers, test values, and part

numbers. However, there are a few additional variations in circuit configuration and the appropriate software. Test descriptions can be found on pages 3 through 5 of the Fault Isolation TR document included in APPENDIX B.

The Subroutine for the VBMH comparator circuit is labeled T21050 and begins on line number 3130. The FIND_IT subprogram is used in lines 3190 and 3200 like before to instruct the operator to connect the chip clip and the red probe to the specified CCA components. The DATA statements in lines 3230 and 3240 contain the test numbers, limits, and matrix point coordinates for the various measurements. There are seven tests in this series and a FOR-NEXT loop running from line 3320 through 3510 handles the setup conditions, closing the proper matrix points, taking the readings, and comparing the results to the limits. All the readings are DC voltages and are obtained using the Digital Multimeter and the FNDVMR function in line number 3410. As in all the CCA tests, the FNTEST function is used in line 3480 to compare the results with the limits, store the results in the data array, and display the results on the screen.

The section of software beginning on line 3520 and ending on line 3600 performs the actual fault isolation of bad parts in accordance with the fault isolation flowchart shown in Figure 3 of APPENDIX V. This section of software uses the IF-THEN-ELSE format and the FOUND_BAD subprogram to

determine and display, if any, the bad parts.

The fault isolation routines for the IFKL and IFKH comparator circuits are run consecutively before returning to the menu. The subroutine which performs these two fault isolation routines is labeled T21240 and begins on line number 4490 and ends on line 5890. The IFKL routine is performed first followed by the IFKH routine which begins on line 5250. These two fault isolation routines are almost identical to that of the VBMH comparator routine described above. The fault isolation flowcharts for these circuits are shown in Figures 5 and 6 of APPENDIX E.

The fault isolation routines for the IFML and IFMH comparator circuits are also run consecutively before returning to the menu. This subroutine is labeled T21440 and includes program lines 6660 through 7840. The IFML fault isolation routine is performed first and the IFMH routine, which begins on line 7290 is performed second. The software and individual tests for these two circuits are also almost identical to that of the VBMH comparator circuit. The fault isolation flowcharts for these circuits can be seen in Figures 8 and 9 of APPENDIX E.

E. Full Power CDC/FPD Logic Circuits (300110-300180)

The CDC and FPD logic circuits are simple optically isolated switching networks and are almost identical. There are four individual tests performed on the two circuits

making a total of eight tests for this series. The two series of four tests are identical except for the fourth test in which the 5 volt power supply is turned off in the first series and the CCA connector pin P2-39 is opened for the second. The complete test descriptions are found on page 6 of the Fault Isolation TR located in APPENDIX B.

The subroutine which performs these eight tests is called T30010 and begins on line 7850 of the Fault Isolation Program. Again the FIND_IT subprograms are used to instruct the operator where to connect the measurement probes on the CCA. The DATA statements in lines 7970 through 8000 contain the part numbers for each network, test numbers, limits, and the coordinates for the matrix points to be closed. The OC("01B") statement in line 8020 grounds the P2-39 pin through the Open Collector Output Card in the Multiprogrammer prior to testing.

The actual measurements are taken within a nested FOR-NEXT loop beginning on line number 8060 and ending on line number 8200. The steps in the loop are repeated for all of the eight tests and include reading the data for a test, setting up the testing conditions, taking the measurement, and comparing the results to the limits. The first two measurements of each series are DC and are obtained using the Digital Multimeter and the the FNDVMR function in line 8120. The last two readings are TTL logic levels which are obtained through the Digital Read Card in

the Multiprogrammer and the FNDR\$ function in line 8150.

The fault isolation flowcharts for these two circuits are shown in Figures 10 and 11 of APPENDIX E. Except for the part numbers they are also identical and the software equivalent is performed in lines 8210 through 8390 following the loop described above. A larger FOR-NEXT loop which is run twice, once for each circuit, begins on line number 8040 and ends on line number 8400 includes the measurement taking loop and flowchart section described above. After the fault isolation routines for the CDC and FPD circuits have been completed, the program returns to the menu by the GOTO statement in line 8420.

F. Power On Sequence Logic Tests (34010-34100)

There are two sections of these tests which are called from the menu. The first part includes test numbers 1 through 4 and the second part includes test numbers 5 through 10 as seen on page 14 of the Acceptance Test TR contained in APPENDIX A. The subroutines in the program include lines 8710 through 10270 and are exactly identical to those described in the Acceptance Test Program. They are repeated here only to determine which of the fourteen outputs measured did fail. Once this has been determined, the appropriate fault isolation routines can be initiated.

Whenever a failure occurs in this section, the subroutine WHICH_ONE is called to determine which of the

outputs failed. This routine begins on line number 21840 and ends on line number 22210. The character string of outputs obtained from the test is compared with the correct character string formed from the test limits, which are of octal form, producing the pin number of the bad output. The appropriate fault isolation routine or routines are then initiated.

G. UI Timer Circuit (310110-310170)

Some of the CCA circuits involve several smaller circuits which can be broken apart and tested individually. In addition to this fact, several of these smaller circuits overlap to form other networks of the CCA. It is because of this that a separate section of subroutines for each of the smaller circuits was developed and included at the end of the main program. The section of software listed in lines 8430 through 8700 includes three subroutines called from the menu that in turn call the appropriate fault isolation routines for the smaller circuits that make up that network. The following is a description of the first of these subroutines.

The UI Timer Circuit consists of a 555 timer and associated components which create a nominal delay of 315 seconds upon triggering through the P2-36 CCA pin. The subroutine for this circuit includes program lines 10780 through 12430 which also contains a separate routine for

tailoring the time delay if necessary. A total of seven tests are performed in this series, all of which are accomplished inside the FOR-NEXT loop beginning on line 11030 and ending on line 11310. The descriptions of these tests can be found on page 6 of the Fault Isolation TR contained in APPENDIX B.

The FIND_IT subprogram and DATA statements in lines 10850 through 10990 are used as described in previous subroutine descriptions. The testing loop mentioned above also performs the same tasks as those of the previous subroutines. Inside this loop however is a REPEAT-UNTIL loop which uses the clock in the computer to measure the time delay of the circuit in the fifth test. The other six tests are DC voltage measurements and use the Digital Multimeter and FNDVMR function in line 11270.

Following the testing loop, the section of software which is equivalent to the fault isolation flowchart shown in figure 12 of APPENDIX E is performed. This section includes lines 11330 through 11750 and determines the bad components or initializes the tailoring routine if necessary.

The tailoring routine begins on line 11960 and is used to tailor the resistor R3 in an effort to produce a time delay within the TR tolerances. If in the fifth test when the time delay is measured, the circuit does switch but at a time just outside the limits, this routine will be

called. When this happens, the operator must clip the R3 resistor off allowing this resistance to be measured by the Digital Multimeter (program line 12120). A new value is then calculated from this value and the actual time delay measured in the fifth test. This new value is then inserted into the circuit using the Decade Resistor and the DECADE subroutine in line 12370 and the test series repeated. If a resistance value cannot be calculated, then all of the timing components are replaced and the program returns to the menu.

H. U2 Timer Circuit (310410-310480)

The U2 Timer Circuit also uses a 555 timer to create a time delay. This timer with its associated components produce a nominal time delay of 200 milliseconds upon a trigger from the Q7-Q8 Transistor Circuit which will be discussed later. There are eight individual tests in this series, all of which are DC voltage readings except for the sixth test which is the time delay measurement. The eight tests are described on page 7 of the Fault Isolation TR contained in APPENDIX B.

The subroutine for this test series is called U2_TIMER and begins on line number 12450. The format of this routine is the same as all the routines that have been discussed earlier. It begins with the FIND_IT and DATA statements followed by the FOR-NEXT loop beginning on line

12670 which performs the eight tests. The Frequency Counter and FNCNTR function in line 12830 are used to measure the time delay of the circuit while the Digital Multimeter and FNDVMR function in line 12720 used to make the DC readings. The CNTS subprogram is used in line 12810 to configure the Counter for a time A to B measurement.

The fault isolation flowchart for this circuit is shown in Figure 13 of APPENDIX E and reproduced in the software section running from lines 12910 through 13340. No tailoring is required for this circuit.

1. U3 Timer Circuit (320110-320160)

This circuit also has a 555 timer and with its associated components, produces a nominal time delay of 15 seconds. The trigger for this circuit is again the CCA connector pin P2-36 which is controlled by the Open Collector Output Card in the Multiprogrammer. A total of six tests are performed on this circuit and are described on page 7 of the Fault Isolation TR located in APPENDIX B. The fifth test in this series measures the time delay of the circuit while the other five tests measure DC voltages.

The U3_TIMER subroutine begins on line number 13390 and ends on line number 14130 and also follows the standard format described previously. The P2-36 pin is initially grounded by the Open Collector Output Card and the OC("0") statement in line 13570. The program then waits 10 seconds

For the timing capacitors to discharge and then begins the FOR-NEXT test loop at line 13590. During the fifth test, a REPEAT_UNTIL loop is used in lines 13690 through 13730 to measure the time delay of the circuit with the clock in the computer. All other measurements are obtained in line 13630 using the Digital Multimeter and FNDVMR function.

Program lines 13820 through 14100 perform the software equivalent of the fault isolation flowchart shown in Figure 14 of APPENDIX E. The FOUND_BAD subprogram is used to print and store any bad parts which are found.

J. U25 Timer Circuit (330110-330210)

The fault isolation routine for this circuit is a little more involved than that of the U2 or U3 Timer Circuits due to additional switching circuitry on the output stage of the 555 timer. This circuit provides a nominal time delay of 1 second and is triggered by the output of the U24 NAND gate. This gate is controlled by the P1-34 input pin and the output of the Q7-Q8 Transistor Circuit which will be discussed later. A description of the 11 individual tests which make up this series can be found on page 8 of the Fault Isolation TR contained in APPENDIX B.

The software for this fault isolation routine is called U25_TIMER and includes program lines 14150 through 15290. The format is again standard beginning with the FIND_IT subprogram calls and the DATA statements followed by

the test and measurement loop and the fault isolation logic. The FOR_NEXT loop which performs the 11 tests begins on line 14430 and ends on line 14650. After the initial testing conditions are established in lines 14450 through 14520, the measurements are obtained using the Digital Multimeter and the FNDVMR function in line 14610. During the eighth test however the time delay measurement is obtained using the Frequency Counter and the FNCNTR function in lines 14530 through 14600.

The fault isolation logic follows the flowchart developed for this circuit and is shown in Figure 15 of APPENDIX E. This section includes program lines 14680 through 15260 and uses the IF-THEN-ELSE statements and the FOUND_BAD subprograms to display, print, and store any bad parts which are found.

K. P2-11/35 Input Circuit (310210-310230)

The output of the UI Timer Circuit discussed earlier is wire-ORed with the output of the P2-11 and 35 Input Circuit. This circuit is very simple and only requires three tests for the fault isolation routine. These tests are described on page 6 of the Fault Isolation TR.

The P2_11_35 subroutine begins on line number 15300 with the standard FIND_IT subprogram calls and the DATA statements in lines 15370, 15380, 15500, and 15510. However in this test series a section of software before the DATA

statements is required to trigger the U1 Timer Circuit causing the output of this circuit to become low or almost zero volts. This section includes program lines 15400 through 15460 and makes it easier to test the P2-11/35 Circuit. The FOR-NEXT loop which includes lines 15530 through 15640 closes the proper matrix relays, applies the required stimulus, takes the DC voltage readings, and compares the results to the TR limits. The TOGGLE(-5) statement in line 15650 turns off the stimulus, power supply number 5, which was used in the third test.

Program lines 15680 through 15810 perform the fault isolation routines according to the fault isolation flowchart in Figure 16 of APPENDIX E.

L. Q7-Q8 Transistor Circuit (310310-310350)

The Q7-Q8 Transistor Circuit is controlled by the wire-ORed circuits described above. This circuit is also very simple and requires five tests which are described on page 7 of the Fault Isolation TR contained in APPENDIX B.

The subroutine for this test series, called Q7_Q8, begins on line number 15860 and is similar to that of the P2-11/35 Circuit discussed above. The section of software running from line 15990 to 16040 triggers the U1 Timer Circuit causing the output to become low in the same manner as the P2-11/35 subroutine. The DATA statements and FOR-NEXT loop, which includes lines 16080 through 16270,

then follow and perform the actual five tests. Program lines 16300 through 16530 accomplish the equivalent of the fault isolation flowchart for this circuit which is shown in Figure 17 of APPENDIX E.

M. P2-12 Output Circuit (320210-320250)

The P2-12 Output Circuit is a simple three stage transistor switching network which controls the CCA pin P2-12. The circuit is controlled directly by the U3 Timer Circuit and includes a total of five tests which are described on page 8 of the Fault Isolation TR. All the readings are in DC volts, however two of them are converted to TTL Logic levels by the Digital Read Card in the Multiprogrammer.

The fault isolation subroutine for this circuit includes program lines 16580 through 17230. After the probes have been connected to the specified parts in lines 16670 through 16690, the U3 Timer Circuit is triggered causing its output to become low or almost zero volts. This is accomplished in the REPEAT-UNTIL loop beginning on line 16740 by monitoring the output with the Digital Multimeter with the U3 Timer trigger input P2-36 open. Once this has occurred, the testing is performed as always during the FOR-NEXT loop running from line 16830 to 16950. Test numbers one and four use the Digital Read Card and FNDR\$ function in line 16910 to obtain the TTL logic levels while

the other tests simply use the Digital Multimeter and FNDVMR function in line 16880. Program lines 16970 through 17200 perform the fault isolation in accordance with the flowchart in Figure 18 of APPENDIX E.

N. P2-1 Input Circuit (340110-340150)

The P2-1 Input Circuit is a combination transistor and optical isolator switching circuit which uses the open collector logic CCA input pin P2-1 as the controller. The output of this circuit is wire-ORed with the outputs of the five comparator circuits discussed at the beginning of this chapter. The fault isolation routine for this circuit is comprised of five individual tests and one check, all of which are described on pages 8 and 9 of the Fault Isolation TR contained in APPENDIX B.

The portion of software in the Fault Isolation Program which performs this test series includes lines 17250 through 18000. This subroutine, which is called P2_1, begins with the required FIND_IT subprogram calls and then sets up the comparator power supply sequence which is described at the top of page 13 of the Acceptance Test TR. This stimulus sequence forces the outputs of all five comparator circuits to be in the low state so that there is no interference with the P2-1 Input Circuit test. Program lines 17370 through 17410 perform the necessary actions needed for this sequence. The OC("1") subprogram call in

line number 17460 grounds the P2-1 input pin through the Open Collector Output Card contained in the Multiprogrammer prior to beginning the FOR-NEXT testing loop.

The test loop, which includes lines 17470 through 17540 is short and simple. The required Measurement Matrix relay is closed, the measurement taken using the Digital Multimeter, the results compared to the TR limits using the FNTEST function, and Measurement Matrix relay is opened back up. On the third test however, the P2-1 input pin is released by the OC("9") subprogram call in line 17500. Upon completion of the five tests, the comparator power sequence is turned off by the statements in lines 17560 through 17580. The section of software running from line 17590 to 17970 performs the fault isolation with accordance to the flowchart shown in Figure 19 of APPENDIX E.

0. P2-13 Output Circuit (340210-340280)

This circuit is a transistor switching network controlled by three sources which are wire-ORed together. The first input is the CCA pin P2-35, the second is the output of the U3 Timer Circuit, and the third input is the output of the Flip Flop Circuit which will be discussed later. A total of eight tests make up this fault isolation series and involve both DC voltage measurements and TTL logic levels. The comparator power sequence described above is applied initially here also as well as controlling the

two open collector logic pins P2-1 and P2-36. The descriptions of the initial set up conditions and the eight tests can be found on page 9 of the Fault Isolation TR.

The subroutine for the fault isolation series begins on line 18020. Lines 18140 through 18180 apply the comparator power sequence in the identical manner as that in the P2-1 subroutine. The FUNGEN(0,"15V") call statement in line 18190 sets up the Function Generator for the 15 volt source needed in the third test. The two open collector logic pins mentioned above are configured in lines 18250 and 18260 according to the TR. Also, before testing can start, the U3 Timer Circuit must have switched to the low state. This is checked in the REPEAT-UNTIL loop and associated software logic which includes lines 18300 through 18410.

The testing is then ready to be performed by the standard FOR-NEXT loop running from line 18440 to 18780. In this loop, the DC voltage readings are obtained in line 18480 and the TTL logic levels in line 18740. The additional software inside the loop simply takes care of the testing conditions required by the TR. The REPEAT-UNTIL loop beginning on line 18660 waits for the U3 Timer to expire after it has been retrigged in the seventh test. After the eight tests have been completed, the comparator power sequence is turned off and the fault isolation routine running from line 18830 to 19210 is performed in accordance with the flowchart shown in Figure 20 of APPENDIX E.

P. P2-37/38 Output Circuit (340310-340420)

The CCA output pins P2-37 and P2-38 are both optically isolated TTL logic outputs wired in series. As long as the control pin P2-14 remains grounded, both inputs will always be in the same state. When the P2-14 pin is open the output pin P2-38 is forced to a high state. This circuit is controlled by the U1 Timer Circuit output, U3 Timer Circuit output, and the P2-1 Input Circuit output. The circuit is therefore difficult to test and requires a total of twelve individual tests which are described on pages 9 and 10 of the Fault Isolation TR. The comparator power sequence described in the previous fault isolation subroutines is applied here also.

The fault isolation subroutine for the P2-37/38 Output Circuit begins on line 19260 by executing five FIND_IT subprogram calls and the comparator power sequence in lines 19400 through 19440. The DATA statements which contain all the important test information are next followed by the FOR_NEXT test loop which runs from line 19510 to 19870. As one can see in this section, both the Digital Multimeter (FNDVMR function) and Digital Read Cards (FNDR\$ function) are used to obtain the DC voltages and TTL logic levels respectively. The open collector logic pins P2-36 and P2-1 are controlled by the OC subprogram in lines 19560,

19610, and 19720 while the P2-14 pin is controlled by the "T24" Stimulus Matrix relay in lines 19500 and 19540.

Following the FOR-NEXT loop, the comparator power sequence is turned off by the TOGGLE and STIM subprogram calls in lines 19880 through 19900. The fault isolation flowchart shown in Figure 21 of APPENDIX E is then implemented by program lines 19910 through 20610.

Q. Flip Flop Circuit (340510-340610)

The Flip Flop Circuit is a very interesting circuit to analyze and fault isolate. There are two inputs, one output, and an array of components which cause the circuit to act somewhat like a flip flop. Brute force is used to isolate the components in this fault isolation series which is made up of eleven individual tests. Page 10 of the Fault Isolation TR contained in APPENDIX B describes these eleven tests.

All eight of the measurement probes are used in the FLIP_FLOP subroutine which begins on line number 20660 along with the comparator power sequence. Program lines 20750 through 20930 include the FIND_IT subprogram calls, the application of the comparator power sequence, and the DATA statements.

The FOR-NEXT test loop runs from line 20940 to line 21180 and follows much the same format of previous loops. However, in line 21080, one of the measurement probes is

moved to a different component on the CCA. After the eleven tests have been performed, the comparator power sequence is turned off and the fault isolation flowchart shown in Figure 22 of APPENDIX E is implemented by the software which includes lines 21240 through 21790.

R. Pulse Train Input Test (90010)

The Pulse Train Input test is a single test which was added to the Acceptance Program to check the U24 NAND gate on the CCA which otherwise would not be caught if it was defective. The test is repeated as a fault isolation subroutine in order to complete the coverage of CCA components. The test description is found under IO CODE 90010 on page 2 of the Fault Isolation TR.

The T90010 subroutine includes lines 10280 through 10460 and is very straight forward with no loops. The gated pulse train which is described in the Acceptance Test TR is generated using the Pulse Generator (PULGEN subprogram) and the Pulse/Function Generator (PULFUN subprogram) in lines 10350 and 10360. The signal is then applied to the CCA pin P1-34 through the Patchbox Circuit logic which is enabled by the Digital Write Card in the Multiprogrammer and the DW("100B") subprogram call in line 10370.

The Frequency Counter is used to measure the pulse width at the input to check for any distortion or attenuation which might be caused by a defective U24 chip.

The measurement is returned by the FNCNTR function in line 10420 and then compared to the limits in line 10440 using the FNTEST function. If the test fails, the FOUND_BAD subprogram call in line 10450 instructs the operator to have U24 replaced.

5. Patchbox Adapter Circuit (TESTX1-TESTX5)

Because the Patchbox Adapter Circuit is not part of the CCA, actual tests using the standard data arrays and FNTEST software function cannot be used. The five tests which make up this fault isolation series are independent of the CCA tests and are therefore considered only "checks" of proper operation. Page 2 of the Fault Isolation TR describes the five "checks" under TESTX1 through TESTX5. The Patchbox Adapter Circuit itself consists only of one 7408 Quad 2-Input AND Gate which makes the testing quite simple.

The PATCHBX subroutine begins on line number 10470 and ends on line number 10730. There are no loops in this test series and all tests use the FIT subprogram instead of the FNTEST function which is used for CCA tests. The Pulse Generator and Digital Write Card are used to apply the signals to the circuit and the Frequency Counter and Digital Multimeter used to obtain the readings. The comparison of readings to the TR limits is performed by the FIT subprogram in lines 10580, 10600, 10620, 10660, and 10680. A pass/fail Boolean code is returned by these subprograms in the X1-X5

variables and if any of these are a "1", a failure, then the 7408 AND gate must be replaced.

CONCLUSIONS

The software developed for this thesis project performs automated testing of the CCA used in this project in accordance with the Naval Acceptance Test Requirements. This software also performs automated fault isolation procedures on the CCA whenever failures occur during the Acceptance Test. A complete circuit analysis must be derived in order to develop the fault isolation procedures for the various circuits on the CCA. Faulty or defective components can then be isolated quickly and easily by the automated test set, TE304.

The TE304 Automated Test Set provides faster and more reliable testing and fault isolation than previously used test sets. The amount of operator intervention is reduced to connecting only a few measurement probes to the components on the CCA and then pressing the CONTINUE key on the Hewlett Packard 9826 computer. Defective components are then isolated automatically and the part numbers displayed on the screen, printed on the printer, and also stored in an array for future use.

This thesis project provides the Naval Ordnance Station in Louisville, Kentucky with a set of concise and well formatted computer programs which test and fault isolate the CCA efficiently and reliably. Complete circuit analysis, the design and construction of interface circuitry, the development of fault isolation procedures, and the writing of the software all combine to make this project a success.

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APPENDIX A
ACCEPTANCE TEST REQUIREMENTS

3.0 TEST REQUIREMENTS.

3.1 TEST PARAMETERS. The input/output (I/O) test parameters for the unit are specified in Table I and apply when the assembly is operated in accordance with the conditions specified herein. The I/O code numbers of Table I identify related characteristics and specified toleranced I/O conditions applicable to test. I/O codes of the form XY000 (ending with 3 zeros) identify related characteristics and conditions applicable to toleranced I/O codes starting with the same XY. I/O codes not ending with three zeros are the specific test parameters applicable to test.

3.2 ENVIRONMENTAL CONDITIONS. The tolerances of Table I apply when the item is tested in standard ambient test conditions as defined in MIL-STD-810.

3.3 COMMON INPUT/OUTPUT TEST CONDITIONS.

a. DC Voltages

- (1) $+28.0 \pm 0.1$ Vdc P1 pins 18, 19, and 43 referenced to P2-17 and 42.
- (2) $+5.0 \pm 0.1$ Vdc to P2 pins 24 and 48 referenced to P2-49 and 25.
- (3) -5.0 ± 0.1 Vdc to P2-47 referenced to P2-49 and 25.
- (4) ± 5.0 Vdc Return to P2 pins 49 and 25.
- (5) $+28.0$ Vdc Return to P1 pins 17 and 42.
- (6) Connect 28 Vdc return to ± 5 Vdc return.

b. Gated TTL Pulse Input. 18.5 msec burst of pulses and 666 msec off time.

- (1) Pulse Characteristics
 - (a) Pulse width 800 nsec
 - (b) PRT 20 micro sec
- (2) Gate Pulse Characteristics
 - (a) Pulse width 18.5 msec
 - (b) PRT 584.5 msec

c. Standard TTL Logic

- (1) Logic 1; $+2.4$ to $+5.2$ Vdc
- (2) Logic 0; 0.0 to $+0.8$ Vdc

SIZE	CODE IDENT NO.	DRAWING NUMBER	
A			
SCALE: NONE	REV LTR	SHEET	5

d. Open Collector Logic

- (1) Logic 1†; open (> 10 meg ohm resistance)
- (2) Logic 0†; 0 to +0.8 Vdc

e. 28 Volt Logic

- (1) Logic 1*; $\geq +25.0$ Vdc
- (2) Logic 0*; $\leq +2.0$ Vdc

f. Special Logic

- (1) 1*; +1.0 to +10 Vdc (see Specific Use)
- (2) 0*; 0 to +0.8 Vdc

g. Line Receiver:

The differential input voltage of the line receivers, supplied from a matched source impedance, is nominally -12 mA times the total load resistance (Z_L). The corresponding logic of the (+) and (-) inputs is:

- (1) Logic 1; (+) input positive with respect to the (-) input.
- (2) Logic 0; (+) input negative with respect to the (-) input.

For test purposes the inputs shall be supplied by a line driver or equivalent circuit (See Figure 1). Line receiver inputs are P1-38(+) and P1-13(-), P1-39(+) and P1-15(-), P1-7(+) and P1-31(-), and P1-32(+) and P1-8(-).

h. Line Driver:

The differential output voltage of the line drivers, interfaced with a matched impedance load, is nominally -12 mA times the total load resistance (Z_L). The corresponding logic of the (+) and (-) outputs is:

- (1) Logic 1; (+) output = $0 + 50$ mVdc
(-) output = $(-12 \text{ mA} \times Z_L) \pm 20\%$
- (2) Logic 0; (+) output = $(-12 \text{ mA} \times Z_L) \pm 20\%$
(-) output = $0 + 50$ mVdc

For test purposes the output lines shall be interfaced with a line receiver or equivalent circuit (See Figure 2).

Line driver output is P1-35(+) and P1-33(-).

SIZE	CODE IDENT NO.	DRAWING NUMBER	
A			
SCALE: NONE	REV LTR	SHEET	6

i. Loads. The following loads are to be realized using components that meet or exceed the specification contained herein.

- (1) Interconnect a 5.6K ohm $\pm 5\%$ 1/4 watt resistor from +28 Vdc $\pm 5\%$ to P1-3.
- (2) Interconnect a 1.0K ohm $\pm 5\%$ 1/4 watt resistor from 5.0 Vdc $\pm 5\%$ to P2-9.
- (3) Interconnect a 1.0K ohm $\pm 5\%$ 1/4 watt resistor from 5.0 Vdc $\pm 5\%$ to P2-12.
- (4) Interconnect a 1.0K ohm $\pm 5\%$ 1/4 watt resistor from 5.0 Vdc $\pm 5\%$ to P2-13.
- (5) Interconnect a 1.0K ohm $\pm 5\%$ 1/4 watt resistor from 5.0 Vdc $\pm 5\%$ to P2-15.
- (6) Interconnect a 1.0K ohm $\pm 5\%$ 1/4 watt resistor from 5.0 Vdc $\pm 5\%$ to P2-37.
- (7) Interconnect a 250 ohm $\pm 5\%$ 1/4 watt resistor from 5.0 Vdc $\pm 5\%$ to P2-38.
- (8) Interconnect a 1.0K ohm $\pm 5\%$ 1/4 watt resistor from 5.0 Vdc $\pm 5\%$ to P2-41.
- (9) Interconnect a 5.6K ohm $\pm 5\%$ 1/4 watt resistor from ground to P1-1.
- (10) Interconnect a 5.6K ohm $\pm 5\%$ 1/4 watt resistor from ground to P1-26.
- (11) Interconnect a 1.0K ohm $\pm 5\%$ 1/4 watt resistor from 5 Vdc to P2-10.
- (12) Interconnect a 1.0K ohm $\pm 5\%$ 1/4 watt resistor from 5 Vdc to P2-44.

j. Terminations: Connect pins P1-17, P1-27, P1-42, P2-14 and P2-17 to ground.

4.0 ADJUSTMENTS/TAILORING. Tailor R3 for proper timing in I/O code 31010.

SIZE	CODE IDENT NO.	DRAWING NUMBER
A		
SCALE: NONE	REV LTR	A
	SHEET	7

TABLE I INPUT OUTPUT CHARACTERISTICS

I/O CODE	CHARACTERISTICS AND INPUT/OUTPUT CONDITIONS	NOMINAL AND UNITS	TOLERANCES
10000	RESISTANCE MEASUREMENTS Measure the resistance between the indicated points.		
10010	<u>Resistance from TP1-1 to P1-17</u>	1.0 ohm	max
10020	<u>Resistance from TP1-1 to P1-42</u>	1.0 ohm	max
10030	<u>Resistance from TP1-13 to P2-16</u>	1.0 ohm	max
10040	<u>Resistance from TP1-14 to P1-3</u>	1.0 ohm	max
10050	<u>Resistance from TP1-15 to P1-26</u>	1.0 ohm	max
10060	<u>Resistance from TP1-16 to P1-1</u>	1.0 ohm	max
10070	<u>Resistance from TP2-1 to P2-25</u>	1.0 ohm	max
10080	<u>Resistance from TP2-1 to P2-49</u>	1.0 ohm	max
10090	<u>Resistance from TP2-11 to P2-33</u>	1.0 ohm	max
10100	<u>Resistance from TP2-12 to P2-8</u>	1.0 ohm	max
10110	<u>Resistance from TP2-13 to P2-32</u>	1.0 ohm	max
10120	<u>Resistance from TP2-14 to P2-7</u>	1.0 ohm	max
10130	<u>Resistance from TP2-15 to P2-1</u>	1.0 ohm	max
10140	<u>Resistance from TP2-16 to P2-2</u>	1.0 ohm	max
10150	<u>Resistance from P2-11 to P2-19</u>	12 Kohm	13 11
10160	<u>Resistance from P1-10 to P1-11</u>	12 Kohm	13 11
11000	CURRENT DEMAND		
	Apply electrical power, as called out in paragraph 3.3.a. Measure indicated current demand.		
11010	<u>+28.0 VDC CURRENT DEMAND</u>	230 mA	max
11020	<u>+5.0 VDC CURRENT DEMAND</u>	450 mA	max
11030	<u>-5.0 VDC CURRENT DEMAND</u>	60 mA	max
	SIZE A	CODE IDENT. NO. DRAWING NUMBER	
	SCALE: NONE	REV LTR	SHEET 8

TABLE I INPUT OUTPUT CHARACTERISTICS

I/O CODE	CHARACTERISTICS AND INPUT/OUTPUT CONDITIONS	NOMINAL AND UNITS	TOLERANCES
20000	TIM REFERENCE VOLTAGE. Measure TREF Voltage at P2-27.		
20010	<u>TREF VOLTAGE (P2-27)</u>	+5.10 Vdc	+6.63 +3.57
21000	OA DC GAIN, AC GAIN AND THRESHOLD TEST. DC Gain: Apply the specified DC stimulus to the indicated (+) and (-) inputs. Measure the corresponding output. AC Gain: Apply an AC stimulus at the indicated frequency and amplitude to the specified pins. Measure the corresponding output gain. DC THRESHOLD: Apply a DC stimulus at the indicated initial voltage and increment in 10 mVdc steps until corresponding output changes to the specified logic level and record the input voltage.		
21010	<u>VBMT DC GAIN</u> Input: P2-3(+) = +12.5 $\pm$ 0.5 Vdc ref P2-2(-) Output: P2-26 ref P2-27	+0.10 v/v	+0.11 +0.09
21020	<u>VBMT AC RIPPLE GAIN</u> Input: P2-2(-), 1.00 $\pm$ 0.5 Hz, 4.0 $\pm$ 0.5 Vp-p ref P2-3(+) Output: P2-26 ref P2-27	0.0723 Vrms/Vrms	0.0871 0.0575
21030	<u>VBMT AC RIPPLE GAIN</u> Input: P2-2(-), 10.00 $\pm$ 0.05 Hz, 10.0 $\pm$ 0.5 Vp-p ref P2-3(+) Output: P2-26 ref P2-27	0.0100 Vrms/Vrms	0.0120 0.0080
SIZE A		CODE IDENT. NO.	
DRAWING NUMBER			
SCALE: NONE		REV LTR	B
SHEET		9	

TABLE I INPUT OUTPUT CHARACTERISTICS

I O CODE	CHARACTERISTICS AND INPUT OUTPUT CONDITIONS	NOMINAL AND UNITS	TOLERANCES												
21040	<u>VBMT AC RIPPLE GAIN</u> Input: P2-3(+), 1.00 ± 0.05 Hz, 4.0 ± 0.5 Vp-p ref P2-2(-) Output: P2-26 ref P2-27	0.0723 V _{rms} /V _{rms}	0.0871 0.0575												
21050	<u>VBMT THRESHOLD INPUT VOLTAGE</u> Input: P2-2(-) Initial Voltage = -5.0 ± 0.5 Vdc ref P2-3(+) Output: P1-48 = Logic 1	-7.00 Vdc	-5.50 -9.00												
21200	<u>IFKT DC GAIN</u> Input: P2-29(+) = 1.5 ± 0.5 Vdc ref P2-28(-) P2-6 = Open Output: P2-4, ref P2-27	+2.00 v/v	+2.40 +1.60												
21210	<u>IFKT AC RIPPLE GAIN</u> Input: P2-28(-) = 1.00 ± 0.05 Hz, 4.0 ± 0.5 Vp-p, ref P2-29(+) P2-6 = Open Output: P2-4, ref P2-27	0.266 V _{rms} /V _{rms}	0.320 0.211												
21220	<u>IFKT AC RIPPLE GAIN</u> Input: P2-28(-) = 10.00 ± 0.05 Hz, 10.0 ± 0.5 Vp-p, ref P2-29(+) P2-6 = Open Output: P2-4, ref P2-27	0.0250 V _{rms} /V _{rms}	0.0300 0.0200												
21230	<u>IFKT AC RIPPLE GAIN</u> Input: P2-29(+) = 1.00 ± 0.05 Hz, 4.0 ± 0.5 Vp-p, ref P2-28(-) P2-6 = Open Output: P2-4, ref P2-27	0.266 V _{rms} /V _{rms}	0.320 0.211												
<table border="1"> <tr> <td colspan="2">SIZE</td><td>CODE IDENT. NO.</td><td>DRAWING NUMBER</td></tr> <tr> <td colspan="2">A</td><td></td><td></td></tr> <tr> <td>SCALE: NONE</td><td>REV LTR</td><td>SHEET</td><td>10</td></tr> </table>				SIZE		CODE IDENT. NO.	DRAWING NUMBER	A				SCALE: NONE	REV LTR	SHEET	10
SIZE		CODE IDENT. NO.	DRAWING NUMBER												
A															
SCALE: NONE	REV LTR	SHEET	10												

TABLE I INPUT OUTPUT CHARACTERISTICS															
	CHARACTERISTICS AND INPUT OUTPUT CONDITIONS	NOMINAL AND UNITS	TOLERANCES												
21240	<u>IFKL THRESHOLD INPUT VOLTAGE</u> Input: P2-29(+) Initial Voltage = 0.0 ± 0.5 Vdc, ref P2-28(-) P2-6 = Open Output: P1-47 = Logic 1	+0.79 Vdc	+0.99 +0.59												
21250	<u>IFKH THRESHOLD INPUT VOLTAGE</u> Input: P2-29(+) Initial Voltage = 3.0 ± 0.5 Vdc, ref P2-28(-) P2-6 = Open Output: P1-22 = Logic 0	+4.20 Vdc	+7.00 +3.20												
21260	<u>IFKL TTL OUTPUT</u> Input: P2-29(+) = 0.0 ± 0.5 Vdc, ref P2-28(-) P2-6 = Open Output: P1-47	Logic 0													
21270	<u>IFKL TTL OUTPUT</u> Input: P2-29(+) = 0.0 ± 0.5 Vdc, ref P2-28(-) P2-6 = +28 Vdc Output: P1-47	Logic 1													
21400	<u>IFMT DC GAIN</u> Input: P2-5(+) = 1.5 Vdc, ref P2-30(-) Output: P2-31, ref P2-27	+1.78 v/v	+2.18 +1.38												
21410	<u>IFMT AC RIPPLE GAIN</u> Input: P2-30(-) = 1.00 ± 0.05 Hz, 4.0 ± 0.5 Vp-p, ref P2-5(+) Output: P2-31, ref P2-27	0.266 Vrms/Vrms	0.320 0.211												
21420	<u>IFMT AC RIPPLE GAIN</u> Input: P2-30(-) = 10.00 ± 0.05 Hz, 10.0 ± 0.5 Vp-p, ref P2-5(+) Output: P2-31, ref P2-27	0.025 Vrms/Vrms	0.030 0.020												
<table border="1"> <tr> <td colspan="2">SIZE</td><td>CODE IDENT. NO.</td><td>DRAWING NUMBER</td></tr> <tr> <td colspan="2">A</td><td></td><td></td></tr> <tr> <td>SCALE: NONE</td><td>REV LTR</td><td>D</td><td>SHEET 11</td></tr> </table>				SIZE		CODE IDENT. NO.	DRAWING NUMBER	A				SCALE: NONE	REV LTR	D	SHEET 11
SIZE		CODE IDENT. NO.	DRAWING NUMBER												
A															
SCALE: NONE	REV LTR	D	SHEET 11												

TABLE I INPUT OUTPUT CHARACTERISTICS																													
I/O CODE	CHARACTERISTICS AND INPUT OUTPUT CONDITIONS			NOMINAL AND UNITS	TOLERANCES																								
21430	<u>IFMT AC RIPPLE GAIN</u> Input: P2-5(+) = 1.00 $\pm$ 0.05 Hz, 4.0 $\pm$ 0.5 Vp-p, ref P2-30(-) Output: P2-31, ref P2-27			0.266 Vrms/Vrms	0.320 0.211																								
21440	<u>IFML THRESHOLD INPUT VOLTAGE</u> Input: P2-30(-) = Initial Voltage = 0.0 $\pm$ 0.5 Vdc, ref P2-5(+) Output: P1-45 = Logic 1			-1.00 Vdc	-0.80 -1.20																								
21450	<u>IFMH THRESHOLD INPUT VOLTAGE</u> Input: P2-30(-) = Initial Voltage = -1.0 $\pm$ 0.5 Vdc, ref P2-5(+) Output: P1-46 = Logic 0			-2.55 Vdc	-1.40 -3.70																								
30000	FULL POWER, CDC(-) AND FPD LOGIC TEST Apply $\pm$ 5.0 Vdc and +28 Vdc supplies as called out in paragraph 3.3.a. Verify the outputs as indicated in table. <table><tr><th>Test</th><th>Input</th><th colspan="2">Outputs</th></tr><tr><td></td><td>P2-39</td><td>P2-41</td><td>P2-15</td></tr><tr><td>1</td><td>0$\uparrow$</td><td>0</td><td>0</td></tr><tr><td>2</td><td>1$\uparrow$</td><td>0</td><td>1</td></tr><tr><td colspan="4">Remove +5 Vdc</td></tr><tr><td>3</td><td>1$\uparrow$</td><td>1</td><td>1</td></tr></table>			Test	Input	Outputs			P2-39	P2-41	P2-15	1	0 $\uparrow$	0	0	2	1 $\uparrow$	0	1	Remove +5 Vdc				3	1 $\uparrow$	1	1		
Test	Input	Outputs																											
	P2-39	P2-41	P2-15																										
1	0 $\uparrow$	0	0																										
2	1 $\uparrow$	0	1																										
Remove +5 Vdc																													
3	1 $\uparrow$	1	1																										
30010	<u>FULL POWER, CDC(-) AND FPD LOGIC</u>			Qual																									
		SIZE	CODE IDENT. NO.	DRAWING NUMBER																									
		A																											
		SCALE: NONE	REV LTR	SHEET	12																								

TABLE I INPUT OUTPUT CHARACTERISTICS

I/O CODE	CHARACTERISTICS AND INPUT OUTPUT CONDITIONS	NOMINAL AND UNITS	TOLERANCES												
31000	5 MINUTE TIMER AND 250 MSEC TIMER Turn on the +5 Vdc, turn off +28 Vdc supply and ground P2-36. Wait approximately 1 minute. Apply +28 Vdc stimulus to P2-1. Apply 9.0 ± 0.1 Vdc to P2-3 and Return to P2-2. Apply 2.0 ± 0.1 Vdc to P2-29 and Return to P2-28. Apply 1.3 ± 0.1 Vdc to P2-5 and Return to P2-30. Apply Logic 1 to P2-36. Apply TTL Logic 0 to P2-35 and P2-11. Apply +28 Vdc supply. Measure elapsed time from +28.0 Vdc turn on until P2-10 voltage switches to a Logic 0. Tailor R3 if required for specified timing. Measure elapsed time from P2-10 Logic 0 switch until P2-9 voltage switches to a Logic 0.														
31010	<u>P2-10 SWITCH TIME</u>	315 sec	330 300												
31020	<u>P2-9 SWITCH TIME</u>	200 msec	250 150												
32000	20 SECOND TIMER Apply the same input signals as in I/O code 31000. Turn off +28 Vdc supply for approximately 10 seconds. Measure elapsed time from +28 Vdc power reapplication for P2-12 to switch to a Logic 1.														
32010	<u>P2-12 SWITCH TIME</u>	15 sec	30 10												
33000	1.5 SECOND TIMER Apply the same input signals as in I/O code 31000. Apply Logic 1 to P1-34 and wait 5 seconds. Apply Logic 0 to P1-34 and measure time required for P2-44 to switch to Logic 0. Apply a gated pulse train as called out in paragraph 3.3.b to P1-34. Wait 5 seconds, apply Logic 0 to P1-34. Verify that P2-44 switches to a logic 1 before 2 seconds have elapsed.														
33010	<u>P2-44 SWITCH TIME</u>	1.0 sec	1.25 0.75												
33020	<u>P2-44 LOGIC OUTPUT</u>	Logic 1													
<table border="1"> <tr> <td colspan="2">SIZE</td><td>CODE IDENT. NO.</td><td>DRAWING NUMBER</td></tr> <tr> <td colspan="2">A</td><td></td><td></td></tr> <tr> <td>SCALE: NONE</td><td>REV LTR</td><td>A</td><td>SHEET 13</td></tr> </table>				SIZE		CODE IDENT. NO.	DRAWING NUMBER	A				SCALE: NONE	REV LTR	A	SHEET 13
SIZE		CODE IDENT. NO.	DRAWING NUMBER												
A															
SCALE: NONE	REV LTR	A	SHEET 13												

TABLE I INPUT OUTPUT CHARACTERISTICS																						
I/O CODE	CHARACTERISTICS AND INPUT OUTPUT CONDITIONS																		NOMINAL AND UNITS	TOLERANCES		
34000	POWER ON SEQUENCE LOGIC TEST																					
	Apply a gated pulse train as called out in paragraph 3.3.b to P1-34. Apply the same logic inputs as in I/O code 31000. Apply the indicated logic input signals and measure the specified logic output signals.																					
		Inputs					Outputs															
	T E S T	P1-34	P2-11	P2-1	P2-36	P2-35	P2-9	TP2-10	P2-10	TP2-9	P2-13	TP2-6	P2-12	TP2-8	P2-44	TP2-5	P2-37	TP2-7	P2-38	P2-19		
	1	2	0	1	0	0	1	1	1	1	1	0	0	1	1	1	1	1	1	0	37476g	
	2	2	1	1	0	0	1	1	1	1	1	0	0	1	1	1	1	1	1	1	37477g	
	3	2	0	0	0	0	1	1	1	1	1	0	0	1	1	1	1	1	0	37476g		
	4	2	0	1	0	1	1	1	1	1	1	0	0	1	1	1	1	1	0	37476g		
	5	2	0	1	1	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	00300g	
	6	2	1	1	1	0	1	1	1	1	0	0	1	1	1	1	0	0	0	1	36361g	
	7	2	0	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	37760g		
	8	2	0	0	1	0	0	0	0	1	1	1	1	0	0	1	1	1	0	01716g		
	9	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	00002g	
	10	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	00000g	

APPENDIX B
FAULT ISOLATION TEST REQUIREMENTS

COMPARATOR POWER SEQUENCE:

1. Apply 9.0 volts to P2-3 and return to P2-2.
2. Apply 2.0 volts to P2-29 and return to P2-28.
3. Apply 1.3 volts to P2-5 and return to P2-30.

GATED TTL PULSE TRAIN INPUT:

1. Pulse Characteristics
 - a. Pulse width 800 nsec.
 - b. Pulse period 20 usec.
2. Gate Pulse Characteristics
 - a. Pulse width 18.5 msec.
 - b. Pulse period 684.5 msec

IO CODE	TEST DESCRIPTION	NOMINAL & UNITS	LIMITS
	CURRENT DEMAND TEST		
11010	Measure +28 vdc supply current demand.	230 mA	max
11020	Measure +5 vdc supply current demand.	450 mA	max
11030	Measure -5 vdc supply current demand.	60 mA	max
	PATCHBOX TEST		
	Apply Logic 1 to adapter pin A33 (DW#2). Apply pulse train to adapter B34 with a 10 msec period and a 1 msec pulse width.		
TESTX1	Measure pulse width at Adapter B32.	1 msec	0.5 1.5
TESTX2	Apply Logic 0 to adapter A33 and measure pulse width at adapter B32.	0	0 0
TESTX3	Measure TTL level of adapter A33.	LOGIC 0	0.8 vdc 0 vdc
TESTX4	Apply Logic 0 to adapter pin A22 (DW#0). Measure adapter A20.	LOGIC 0	0.8 vdc 0 vdc
TESTX5	Apply Logic 1 to adapter pin A22 and measure adapter A20.	LOGIC 1	5.2 vdc 2.4 vdc
	TEST 90010 (U24 PULSE INPUT)		
90010	Apply Gated Pulse Train to P1-34 and measure pulse width with trigger level set at 2.4 volts.	20 usec	22 18

IO CODE	TEST DESCRIPTION	NOMINAL & UNITS	LIMITS
VOLTAGE REGULATOR TEST			
200110	Measure R147.	25.8 vdc	27.58 24.51
200120	Apply 25 vdc to R142, measure R147.	25.1 vdc	26.355 23.845
200130	Apply 13.6 vdc to R154, measure P2-27.	5.10 vdc	5.355 4.845
200140	Measure R153.	10.106 v	10.611 9.601
200150	Measure R151.	6.612 v	6.943 6.281
200160	Measure R150.	5.712 v	6.007 5.435
200170	Remove above stimulus, measure R154.	13.6 vdc	14.28 12.92
21000 VBMT SERIES TESTS			
210010	Apply 20vdc to P2-3, ground P2-2. Measure U21 pin 10.	7.10 vdc	7.81 6.39
210020	Measure U21 pin 6.	6.45 vdc	7.10 5.81
210030	Measure U21 pin 6, ref. U21 pin 7.	0 vdc	0.01 -0.01
210040	Measure voltage across R130.	0 vdc	0.05 -0.05
210050	Apply -20 vdc to P2-2. Measure U21 pin 10.	9.10 vdc	10.01 8.19
210060	Remove dc stimulus and apply 10Hz 5vpp to P2-2, ref. P2-3. Measure AC gain at U21 pin 10.	.01060 vrms/ vrms	.01166 .00954
Test 8	Calculate (IO codes 210010/210020).	1.10	1.21 0.99
210510	Apply voltage to U21 pin 1 equal to pin 2 - 0.5 vdc. Measure pin 12.	24.8 vdc	27.0 22.0
210520	Measure U21 pin 2=pin 12/221 +5.7538	Qual	+10 % -10 %
210530	Measure P1-48.	Logic 0	0.8 vdc 0 vdc
210540	Measure Q39 pin 7.	2.18 vdc	2.40 1.96
210550	Apply voltage at U21 pin1 equal to pin2 + 0.5 vdc. Measure pin 12.	2.14 vdc	2.35 1.93
210560	Measure P1-48.	Logic 1	5.2 vdc 2.4 vdc
210570	Remove stimulus and measure voltage across R135.	0 vdc	0.05 -0.05

IO CODE	TEST DESCRIPTION	NOMINAL & UNITS	LIMITS
	21200 IFKT SERIES TESTS		
212010	Apply 3vdc to P2-29, ground P2-28. Measure U20 pin 10.	9.10 vdc	10.01 8.19
212020	Measure U20 pin 6.	3.03 vdc	3.34 2.73
212030	Measure U20 pin 6, ref U20 pin 7.	0 vdc	0.01 -0.01
212040	Measure voltage across R119.	0 vdc	0.05 -0.05
212050	Apply -2 vdc to P2-28. Measure U20 pin 10.	13.1 vdc	14.41 11.79
212060	Remove dc stimulus and apply 10Hz 5vpp to P2-28, ref. P2-29. Measure AC gain at U20 pin 10.	.027 vrms/ vrms	.0297 .0243
Test 8	Calculate (IO codes 212010/212020).	3.00	3.30 2.70
212410	Apply voltage to U20 pin1 equal to U20 pin 2 - 0.5 vdc. Measure pin 12.	24.8 vdc	27.0 22.0
212420	Check voltage at pin2 equal to (pin12/221 + 5.7538).	Qual	+10% -10%
212430	Measure P1-47.	LOGIC 0	0.8 vdc 0.0 vdc
212440	Measure Q38 pin 7.	2.18 vdc	2.40 1.96
212450	Apply voltage to U20 pin1 equal to pin 2 + 0.5 vdc. Measure pin 12.	2.14 vdc	2.35 1.93
212460	Measure P1-47.	LOGIC 1	5.2 vdc 2.4 vdc
212470	Remove stimulus and measure voltage drop across R125.	0 vdc	0.05 -0.05
Test 8	Ground P2-6, check U20 pin1 equal to [(120*pin10 + 924)/153].	Qual	+10% -10%
212510	Measure voltage at U22 pin 1.	18 vdc	19 17
Test 1A	Measure voltage at VR17.	18 vdc	19 17
212520	Apply voltage to U22 pin2 equal to pin 1 + 0.5 vdc. Measure pin 12.	24.8 vdc	27 22
212530	Measure P1-22.	LOGIC 0	0.8 vdc 0.0 vdc
212540	Measure Q37 pin 7.	2.18 vdc	2.40 1.96
212550	Apply voltage at U22 pin2 equal to pin 1 - 0.5. Measure pin 12.	2.14 vdc	2.35 1.93
212560	Measure P1-22.	LOGIC 1	5.2 vdc 2.4 vdc
212570	Remove above stimulus and check U22 pin2=(pin12+180*U20 pin10)/181.	Qual	+10% -10%

IO CODE	TEST DESCRIPTION	NOMINAL & UNITS	LIMITS
21400 IFMT SERIES TESTS			
214010	Apply 2.5vdc to P2-5, ground P2-30. Measure U22 pin 10.	9.55 vdc	10.50 8.59
214020	Measure U22 pin 6.	3.44 vdc	3.78 3.09
214030	Measure U22 pin 6, ref U22 pin 7.	0vdc	0.01 -0.01
214040	Measure voltage across R104.	0 vdc	0.05 -0.05
214050	Apply -2 vdc to P2-30. Measure U22 pin 10.	13.1 vdc	14.42 11.80
214060	Remove dc stimulus and apply 10Hz 5vpp to P2-30, ref. P2-5. Measure AC gain at U22 pin 10.	.027 vrms/ vrms	.0297 .0243
Test 8: Calculate (IO codes 214010/214020).		2.78	3.058 2.502
214410	Apply voltage to U23 pin1 equal to U23 pin 2 - 0.5 vdc. Measure pin 12.	24.8 vdc	27.0 22.0
214420	Check voltage at pin2 equal to (pin12/221 + 6.6398).	Qual	+10% -10%
214430	Measure P1-45.	LOGIC 0	0.8 vdc 0.0 vdc
214440	Measure Q36 pin 7.	2.18 vdc	2.40 1.96
214450	Apply voltage to U23 pin1 equal to pin 2 + 0.5 vdc. Measure pin 12.	2.14 vdc	2.35 1.93
214460	Measure P1-45.	LOGIC 1	5.2 vdc 2.4 vdc
214470	Remove stimulus and measure voltage drop across R109.	0 vdc	0.05 -0.05
214510	Measure voltage at U23 pin 7.	10.2 vdc	10.7 9.70
214520	Apply voltage to U23 pin6 equal to pin 7 + 0.5 vdc. Measure pin 10.	24.8 vdc	27 22
214530	Measure P1-46.	LOGIC 0	0.8 vdc 0.0 vdc
214540	Measure Q35 pin 7.	2.18 vdc	2.40 1.96
214550	Apply voltage at U23 pin6 equal to pin 7 - 0.5. Measure pin 10.	2.14 vdc	2.35 1.93
214560	Measure P1-46.	LOGIC 1	5.2 vdc 2.4 vdc
214570	Remove above stimulus and check U23 pin6=(pin10+200*U22 pin10)/201.	Qual	+10% -10%

IO CODE	TEST DESCRIPTION	NOMINAL & UNITS	LIMITS
CDC AND FPD LOGIC TEST			
300110	Measure Q26 pin 5.	1.26 vdc	1.39 1.13
300120	Measure Q26 pin 3.	0.8 vdc	0.90 0.70
300130	Measure P2-41.	LOGIC 0	0.8 vdc 0 vdc
300140	Remove 5 volt supply, measure P2-41.	LOGIC 1	5.2 vdc 2.4 vdc
300150	Ground P2-39, measure Q23 pin 5.	1.26 vdc	1.39 1.13
300160	Measure Q23 pin 3.	0.8 vdc	0.90 0.70
300170	Measure P2-15.	LOGIC 0	0.8 vdc 0 vdc
300180	Open P2-39, measure P2-15.	LOGIC 1	5.2 vdc 2.4 vdc
UI TIMER TEST			
310110	Open P2_36 and measure Q5 pin 1 to 3.	0 vdc	0.05 0
310120	Ground P2-36 and short R4 for 1 second. Measure C3+.	0.7 vdc	0.8 0
310130	Measure R18.	0.37 vdc	0.5 0
310140	Measure CR8-.	10.5 vdc	12.1 9.9
310150	Open P2-36 and measure the time for the output at R17 to fall near zero.	315 sec	330 300
310160	Measure C3+.	10.5 vdc	11.5 9.41
310170	Measure R18.	14 vdc	16 10
INPUTS P2-11,35 TEST			
310210	Ground P2-11 and P2-35 and measure CR8-.	2.31 vdc	2.54 0
310220	Open P2-11 and measure CR8-.	10.5 vdc	11.55 9.45
310230	Ground P2-11 and apply 15 vdc to P2-35. Measure CR8-.	10.5 vdc	11.55 9.45

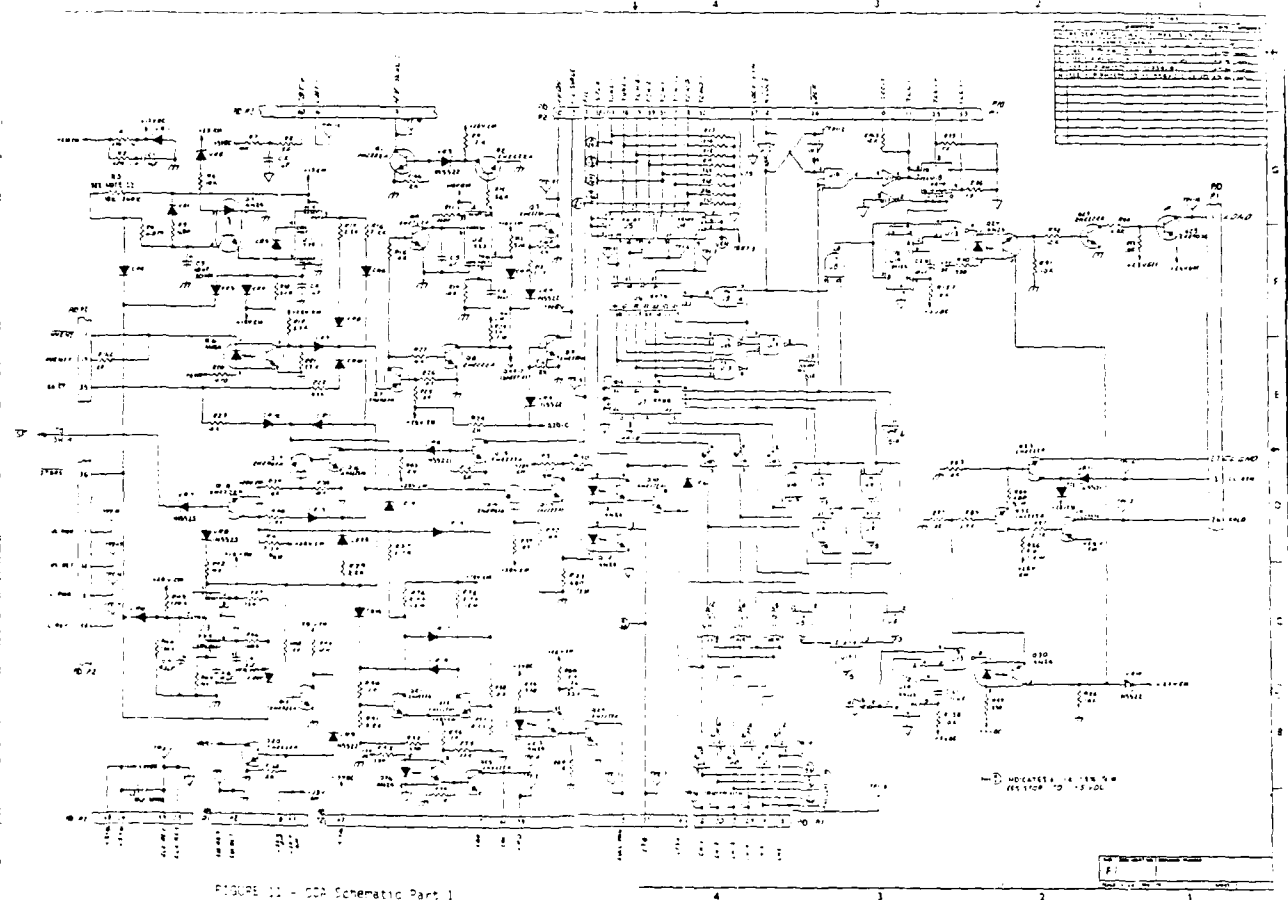
IO CODE	TEST DESCRIPTION	NOMINAL & UNITS	LIMITS
TRANSISTORS Q7/Q8 AND OUTPUT P2-10 TEST			
	Open P2-11 and P2-36 and apply 12 volts to C3+ for about 0.5 seconds.		
310310	Measure R26/R25 junction.	10 vdc	11 9
310320	Obtain a high level at Label 1 and measure P2-10.	LOGIC 1	5.2 vdc 2.4 vdc
310330	Measure R28.	0 vdc	0.5 0
310340	Ground P2-11 and measure P2-10.	LOGIC 0	0.8 vdc 0 vdc
310350	Measure R28.	25.4 vdc	27.94 22.86
U2 TIMER TEST			
310410	Open P2-11 and P2-36 and measure R14 at U2.	7.5 vdc	8.25 6.75
310420	Obtain a high input level at Label 1, wait 5 seconds and measure C5+.	.01 vdc	0.05 0
310430	Measure R12 at U2.	0.7 vdc	0.85 0.55
310440	Measure P2-9.	LOGIC 1	5.2 vdc 2.4 vdc
310450	Measure R9.	0 vdc	0.25 0
310460	Ground P2-11 and apply 12 volts to C3+ for about 0.5 seconds. Measure the time for P2-9 to switch to Logic 0.	166 msec	250 150
310470	Measure R10 at U2.	0 vdc	0.1 0
310480	Measure R12 at U2.	15 vdc	15.5 12.0
U3 TIMER TEST			
320110	Measure R45 at U3.	7.5 vdc	8.25 6.75
320120	Ground P2-36, wait 10 seconds, and measure C9+.	0.7 vdc	0.77 0.30
320130	Measure C7+.	0.7 vdc	0.77 0.30
320140	Measure R48 at U3.	12.7 vdc	15 11
320150	Open P2-36 and measure time for U3 output at R48 to go low.	15 sec	30 10
320160	Measure C7+.	>10 vdc	15 10

IO CODE	TEST DESCRIPTION	NOMINAL & UNITS	LIMITS
	P2-12 OUTPUT TEST		
320210	Open P2-36, wait for U3 timer to expire, and measure P2-12.	LOGIC 1	1 1
320220	Measure R49 at Q19.	5.3 vdc	5.83 4.77
320230	Measure R24 at Q20.	0 vdc	0.1 0
320240	Ground P2-36 and measure P2-12.	LOGIC 0	0 0
320250	Measure R49 at Q19.	0 vdc	0.1 0
	U25 TIMER TEST		
	Ground P2-11 and P2-35. Open P2-36 and apply 12 volts to C3+ for about 0.5 seconds.		
330110	Apply a Logic 1 to P1-34 and measure U24 pin 6.	LOGIC 0	0.8 vdc 0 vdc
330120	Apply Logic 0 to P1-34 and measure U24 pin 6.	LOGIC 1	5.2 vdc 2.4 vdc
330130	Apply Logic 1 to P1-34, open P2-11, and measure U24 pin 6.	LOGIC 1	5.2 vdc 2.4 vdc
330140	Measure R175 at U25.	2.5 vdc	2.75 2.25
330150	Ground P2-11, wait 5 seconds and measure C28+.	0.7 vdc	0.77 0.60
330160	Measure P2-44.	LOGIC 0	0.8 vdc 0 vdc
330170	Measure R174 at Q45.	1.37 vdc	1.57 1.29
330180	Apply Logic 0 to P1-34 and measure the time for P2-44 to switch to Logic 1.	1 sec	1.25 0.75
330190	Measure R177 at U25.	0 vdc	0.25 0
330200	Measure C28+ at U25.	>3.3 vdc	5.0 3.3
330210	Measure R174 at Q45.	5 vdc	5.0 4.8
	P2-1 INPUT CIRCUIT		
	Apply the comparator power sequence.		
340110	Ground P2-1 and measure R98 at Q34.	0 vdc	0.25 0
340120	Measure R143 at Q40.	3.2 vdc	3.45 2.83

IO CODE	TEST DESCRIPTION	NOMINAL & UNITS	LIMITS
TEST2A	Check if IO code 340120 is below or above the tolerances.		
340130	Open P2-1 and measure R98 at Q34.	5.8 vdc	6.40 5.20
340140	Measure R143 at Q40.	0 vdc	0.25 0
340150	Measure CR24 anode.	1.15 vdc	1.25 1.00
P2-13 OUTPUT TEST			
Apply the comparator power sequence. Open P2-1 and ground P2-36 and then open P2-36 and wait for U3 timer to expire.			
340210	Measure R38 R39 junction.	10 vdc	11 9
340220	Ground P2-35, open P2-36, and measure P2-13.	LOGIC 0	0 0
340230	Apply 15 volts to P2-35 and measure P2-13.	LOGIC 1	1 1
340240	Measure R63 at Q16.	0 vdc	0.25 0
340250	Ground P2-35 and P2-36 and measure P2-13	LOGIC 1	1 1
340260	Measure R63 at Q16.	0 vdc	0.25 0
340270	Open P2-36, ground P2-1, and measure P2-13.	LOGIC 1	1 1
340280	Measure R63 at Q16.	0 vdc	0.25 0
P2-37 AND P2-38 OUTPUT CIRCUIT TEST			
Apply the comparator power sequence.			
340310	Ground CR25- and P2-14 and measure P2-38	LOGIC 0	0 0
340320	Measure P2-37.	LOGIC 0	0 0
340330	Open P2-14 and measure P2-38	LOGIC 1	1 1
340340	Measure voltage from R30/R31 junction to Q12 pin 7.	8.9 vdc	9.80 8.00
340350	Ground P2-36, disconnect CR25 ground, and measure CR25 cathode.	11 vdc	11.77 9.63
340360	Measure P2-38.	LOGIC 1	1 1
340370	Measure P2-37.	LOGIC 1	1 1

IO CODE	TEST DESCRIPTION	NOMINAL & UNITS	LIMITS
340380	Measure voltage from R30/R31 junction to Q12 pin 7.	0 vdc	0.1 0
340390	Ground P2-36 and open P2-1. Measure R40 at Q18.	0 vdc	0.1 0
340400	Measure CR25 cathode.	11 vdc	11.77 9.63
340410	Open P2-36, wait for U1 timer to expire, and measure CR25 cathode.	11.8 vdc	12.78 10.46
340420	Open P2-1 and measure CR25 cathode.	1.2 vdc	3.75 0
FLIP FLOP CIRCUIT TEST			
340510	Apply the comparator power sequence, ground P2-36, open P2-1, and measure R41.	0 vdc	0.1 0
340520	Measure R50 at CR18.	23.5 vdc	25.85 21.15
340530	Open P2-36, ground P2-1, wait for U1 timer to expire and measure R41.	20 vdc	22 18
340540	Apply 28 volts to R50 at CR18 and R58 at CR17. Measure Q21 Vbe.	0.7 vdc	0.77 0.63
340550	Measure Q22 Vbe.	0.7 vdc	0.77 0.63
340560	Measure Q21 Vce	0.1 vdc	0.2 0
340570	Measure Q22 Vce	0.1 vdc	0.2 0
340580	Ground Q21 and Q22 bases and R37 at CR14. Measure R36 at CR17.	14.8 vdc	16.30 13.34
340590	Measure R35 at CR18.	28 vdc	30.80 25.20
340600	Remove 28 volt stimulus and ground R50 and R58. Measure R36 at CR17.	0.7 vdc	0.77 0.63
340610	Measure R35 at CR18.	0.7 vdc	0.77 0.63

APPENDIX C
SCHEMATIC DIAGRAMS OF THE CCA



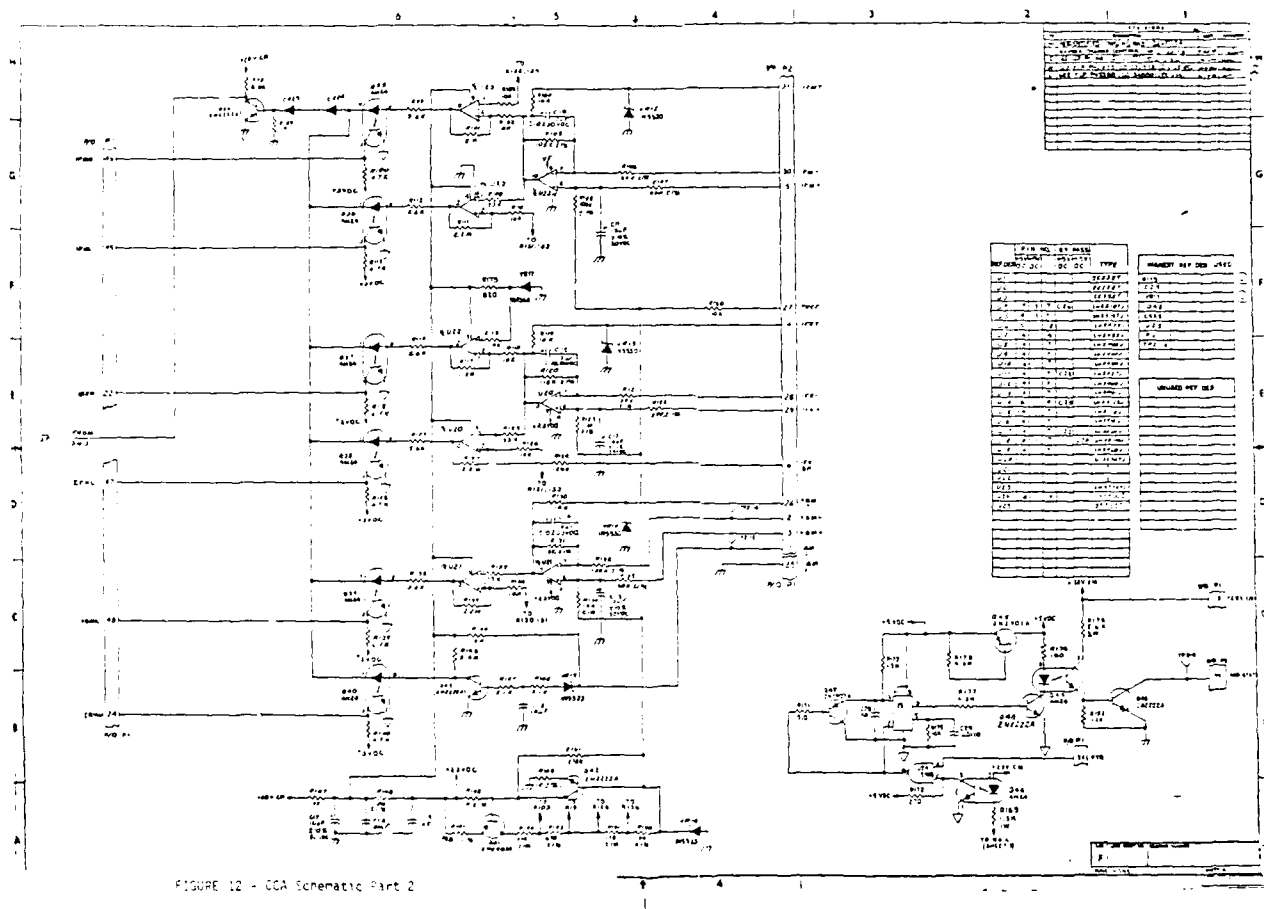


FIGURE 12 - CGA Schematic Part 2

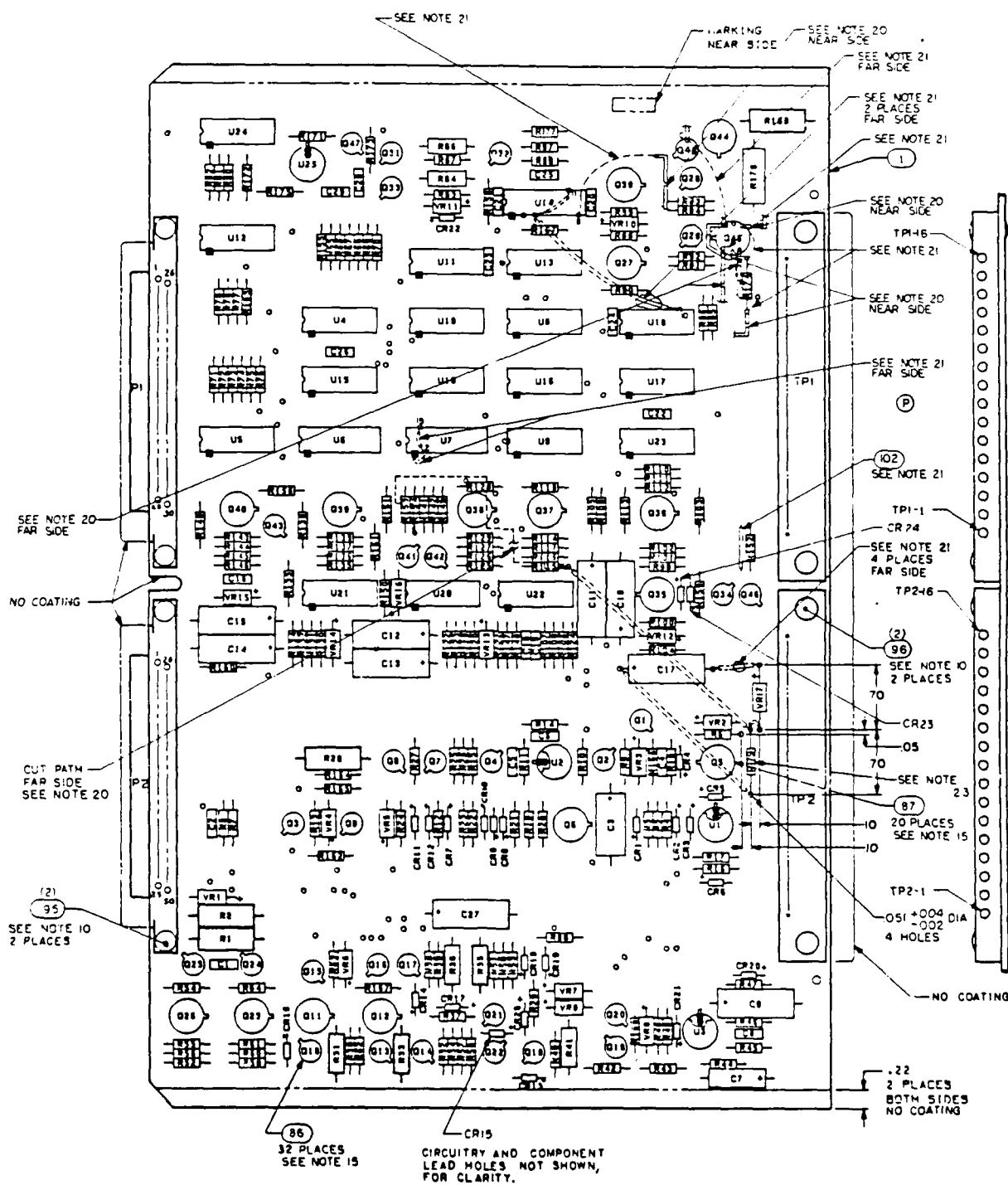


FIGURE 13 - CCA Parts Layout

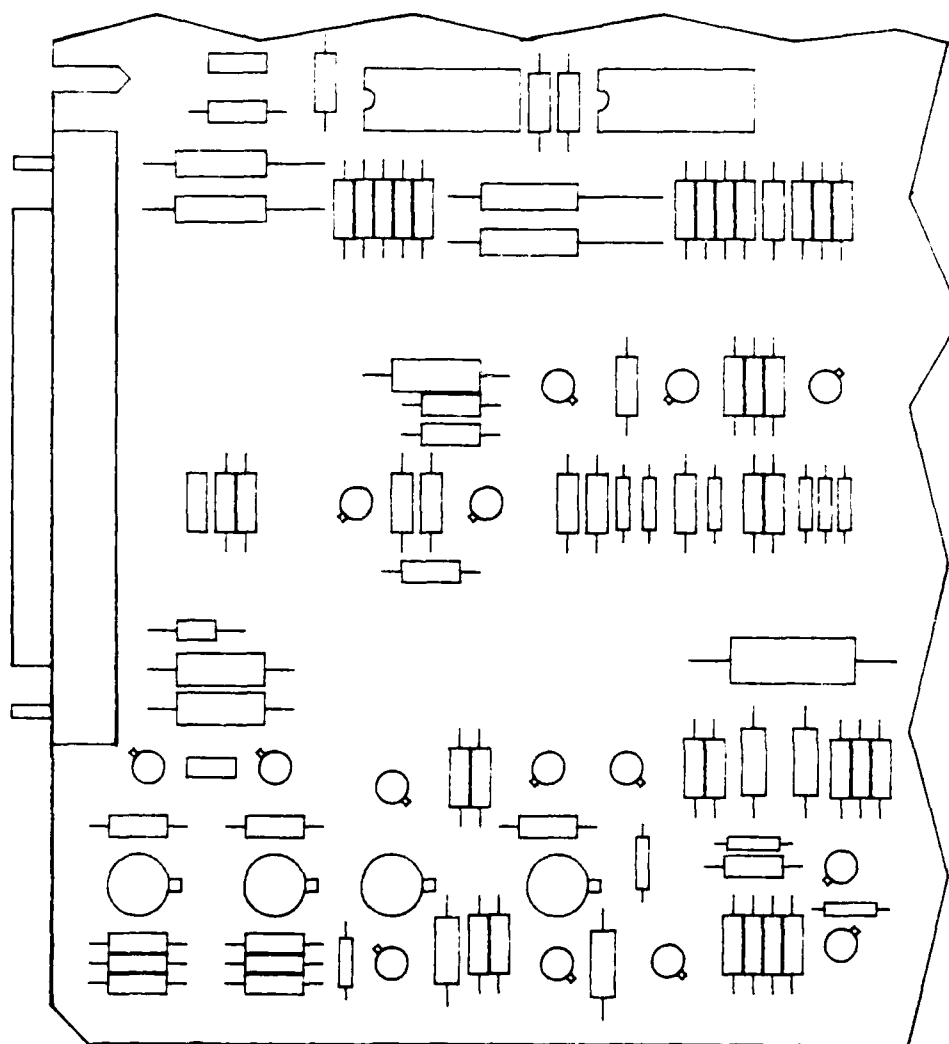


FIGURE 14 - Computer Generated Parts Layout (Quadrant 1)

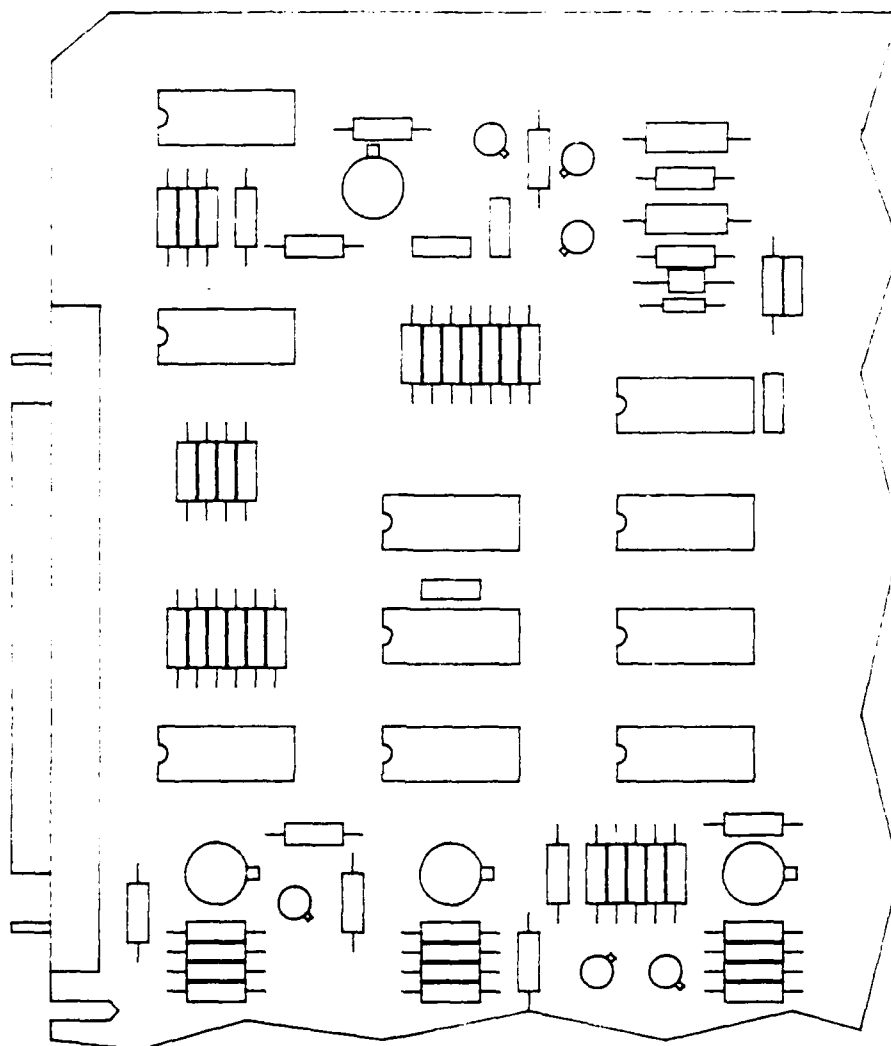


FIGURE 15 - Computer Generated Parts Layout (Quadrant 2)

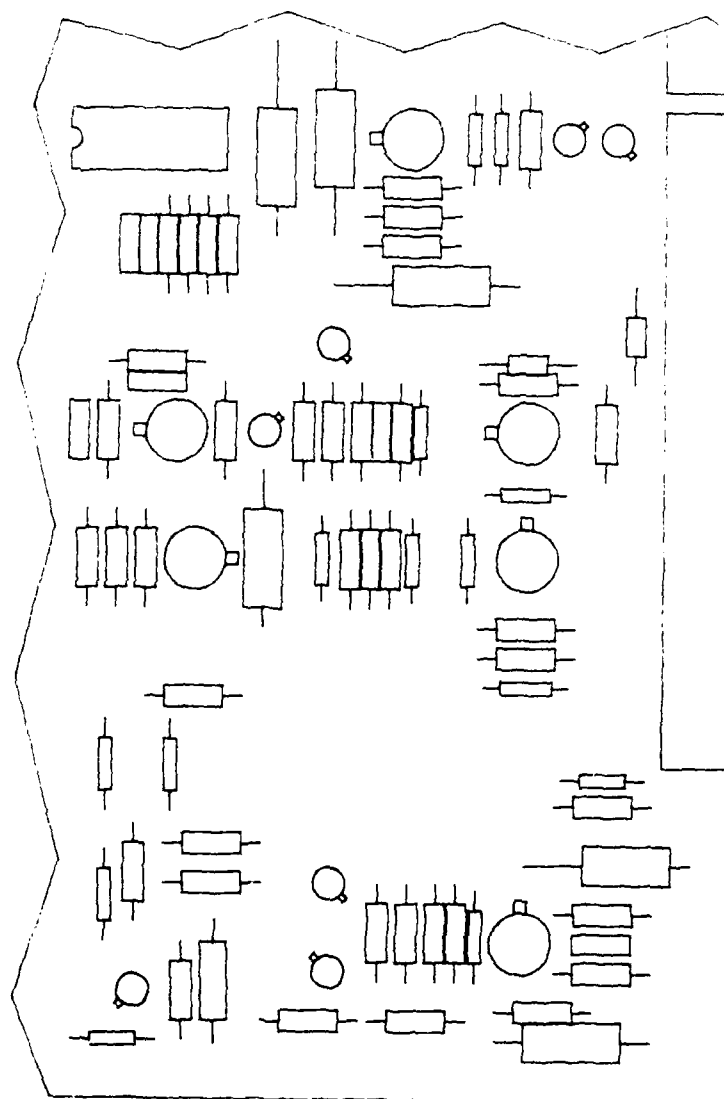


FIGURE 16 - Computer Generated Parts Layout (Quadrant 3)

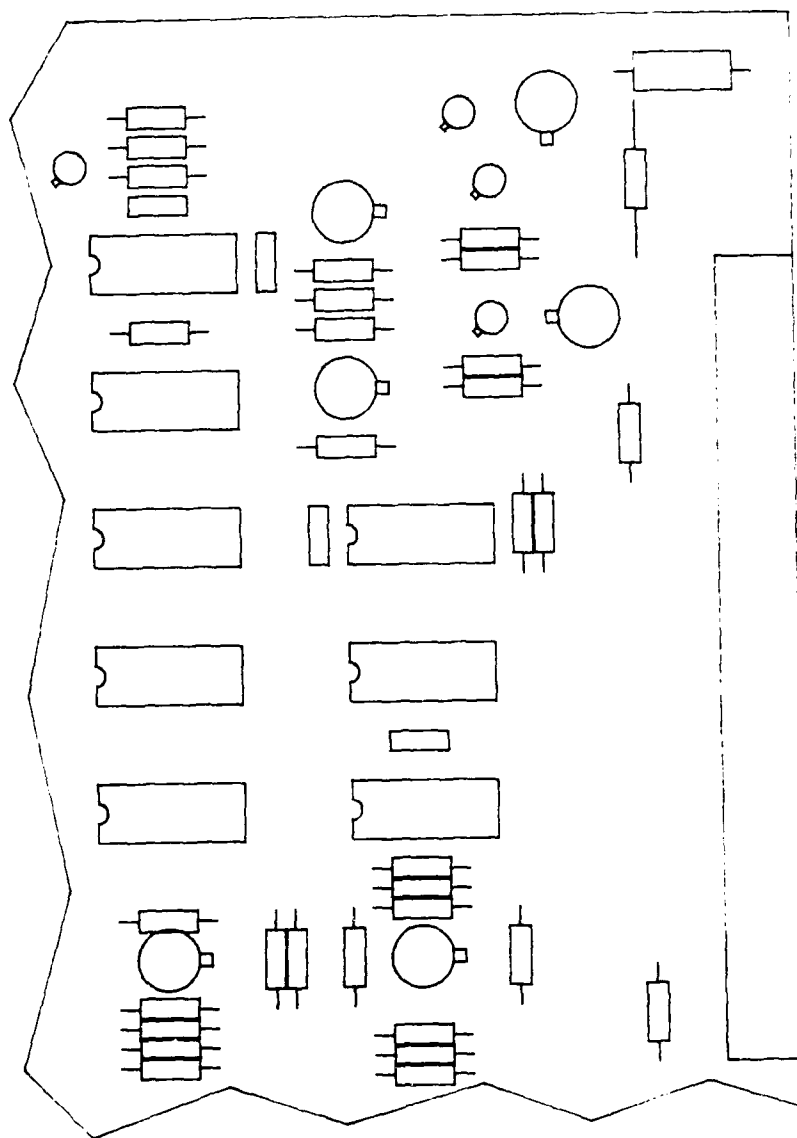


FIGURE 17 - Computer Generated Parts Layout (Quadrant 4)

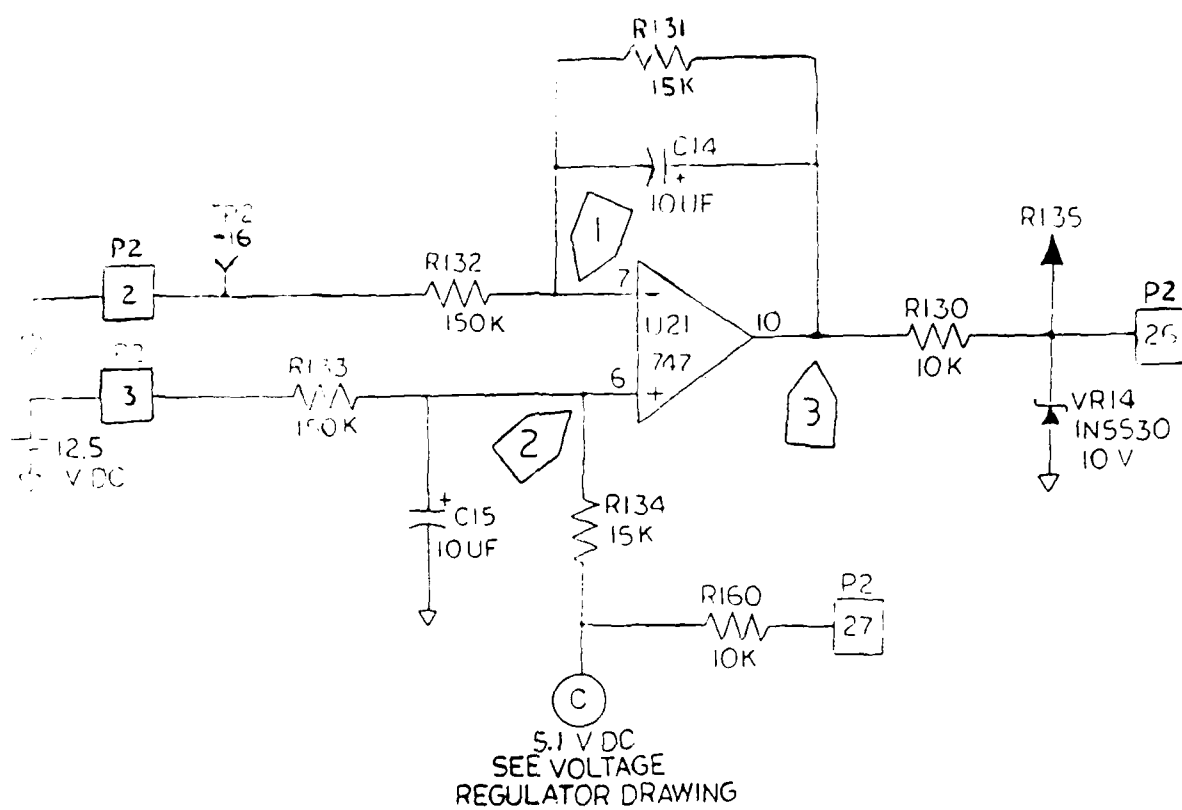


FIGURE 19 - VBMT Op Amp Circuit

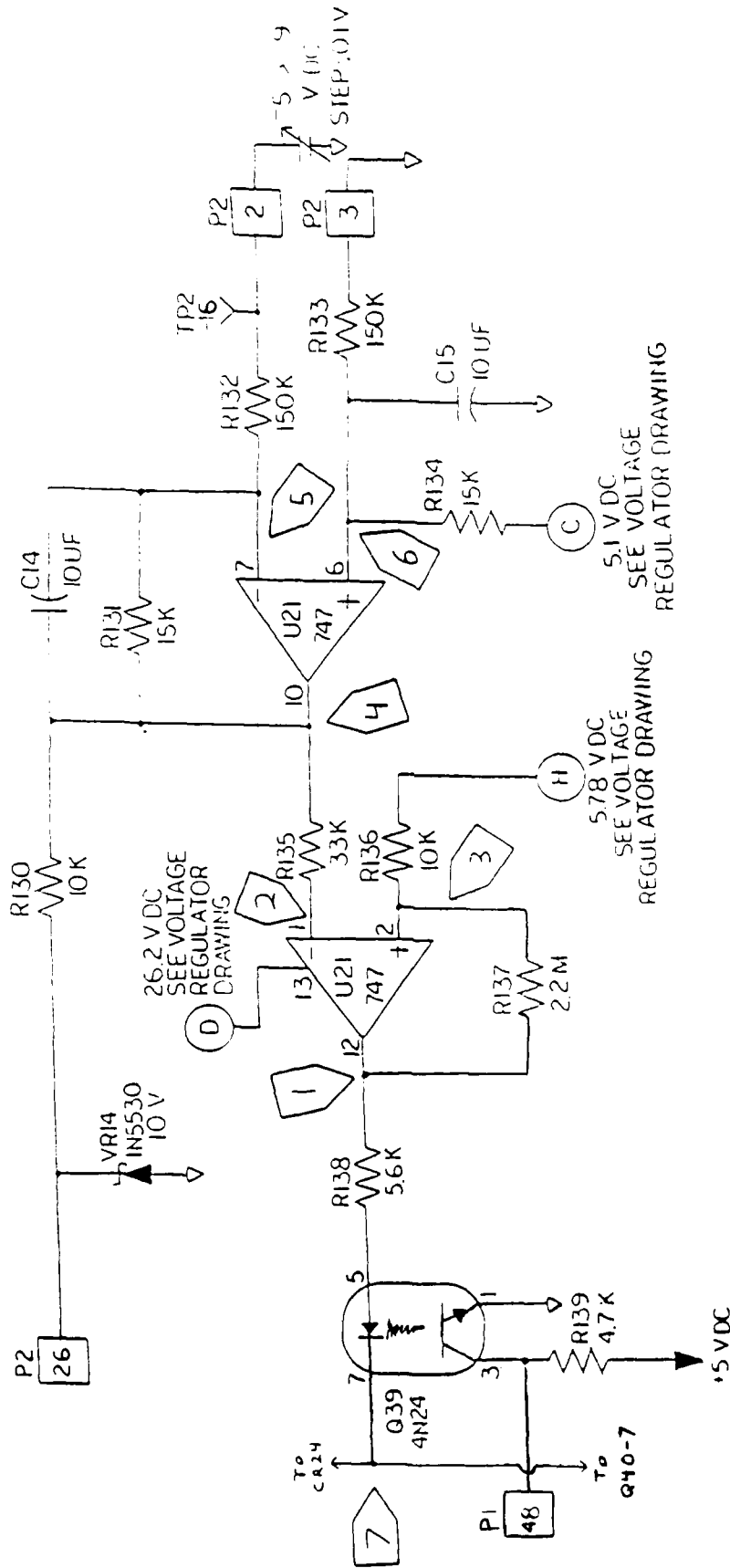


FIGURE 20 - VBMH Comparator Circuit

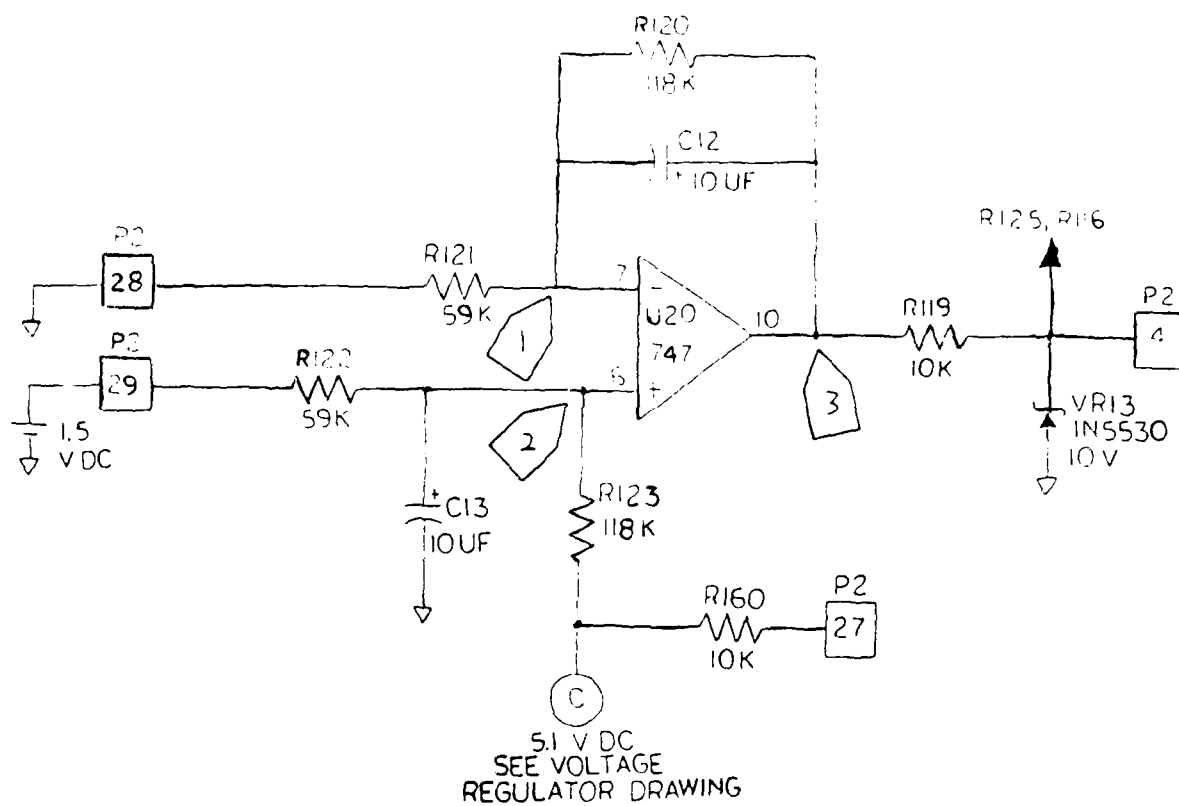


FIGURE 21 - IFKT Op Amp Circuit

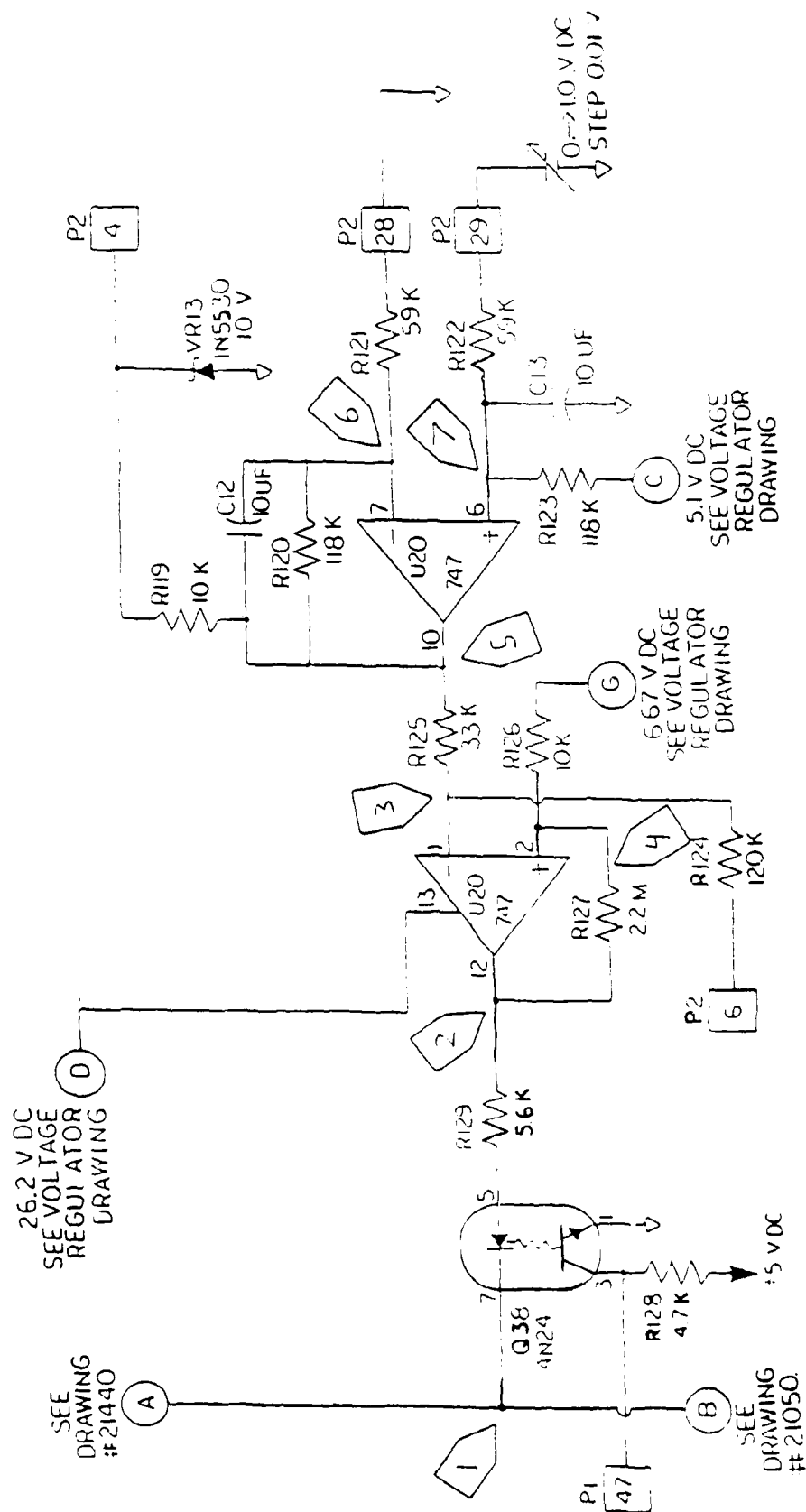


FIGURE 22 - IFKL Comparator Circuit

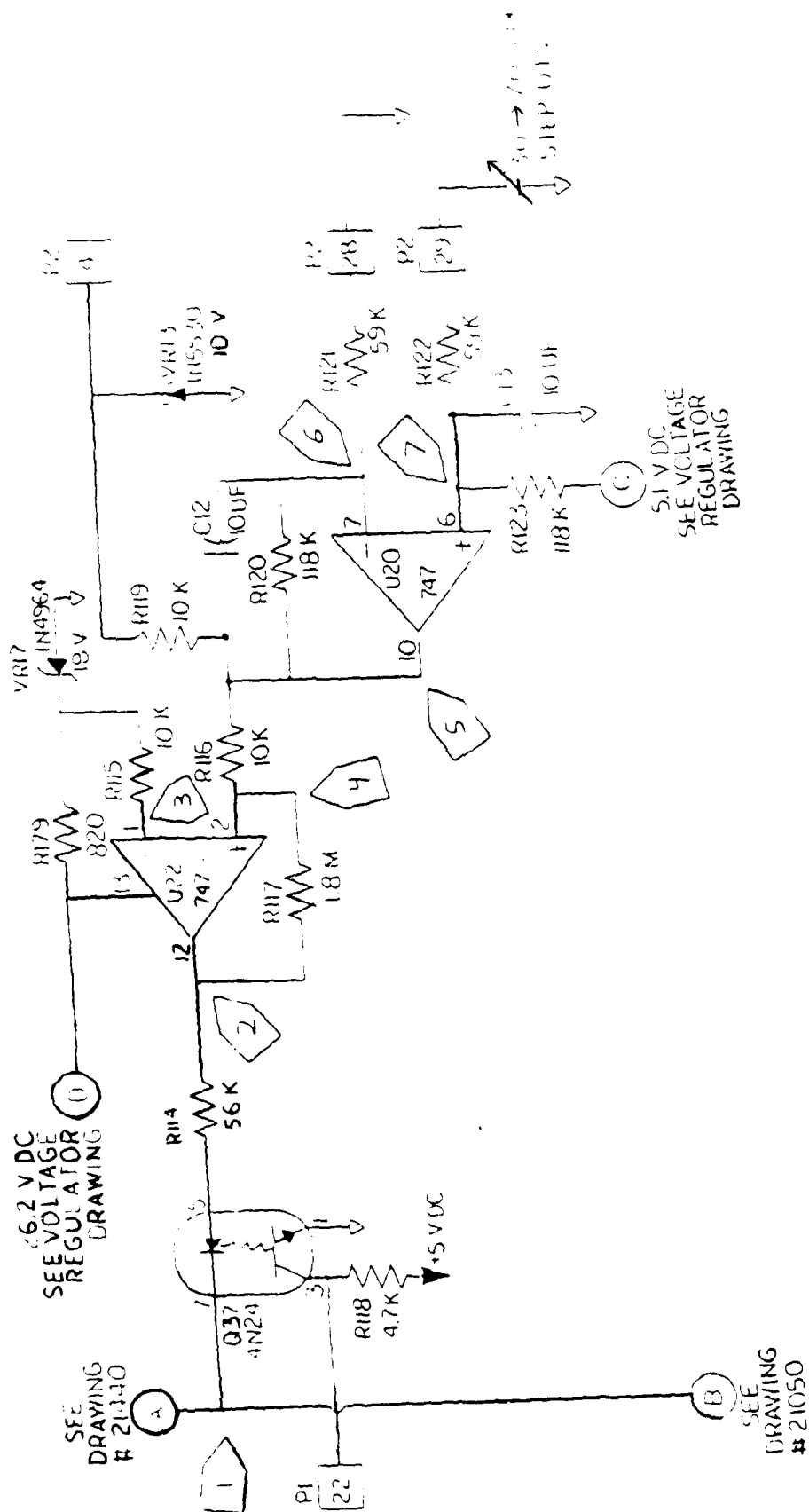


FIGURE 23 - IFKH Comparator Circuit

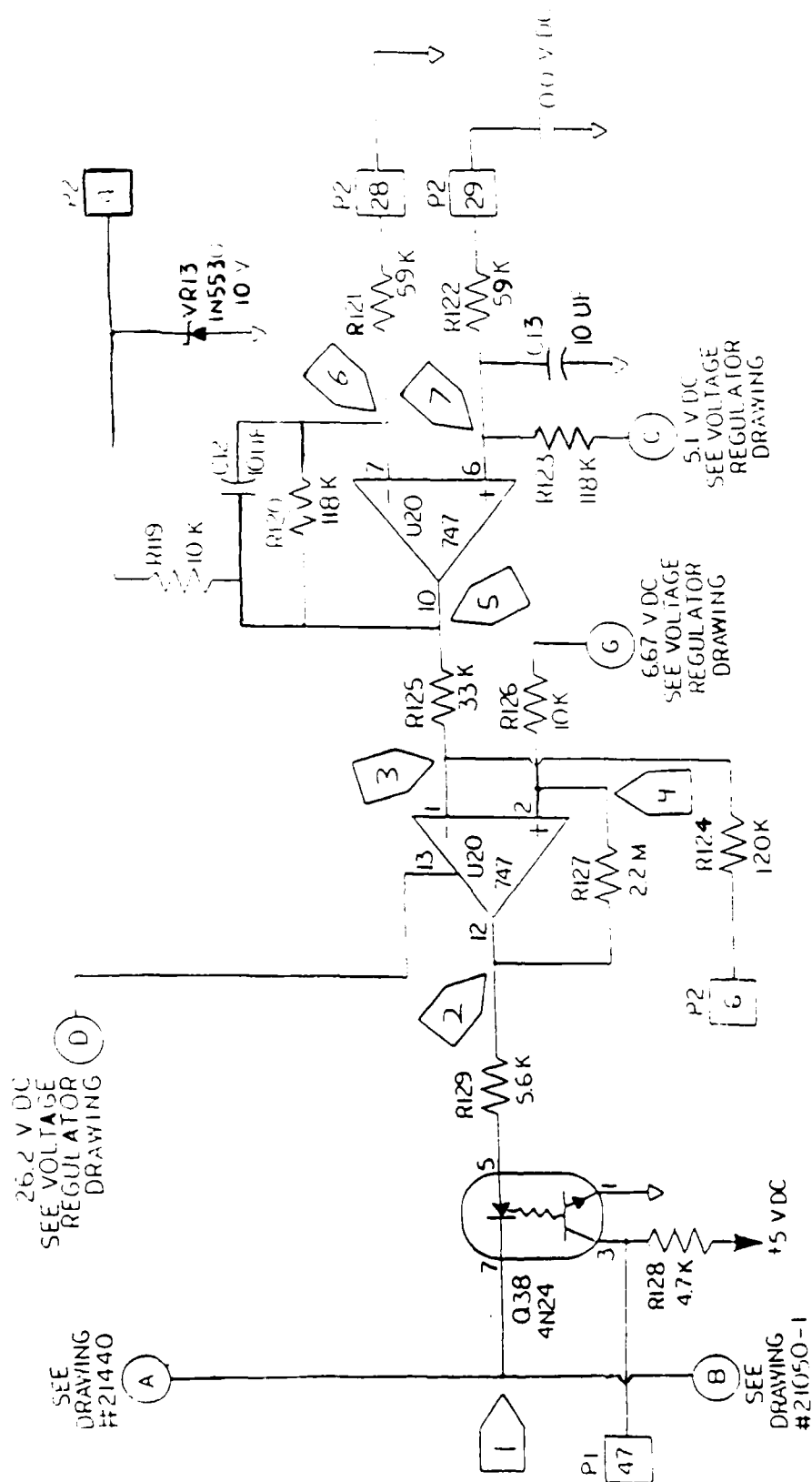


FIGURE 24 - IFKL_TTL Output Circuit

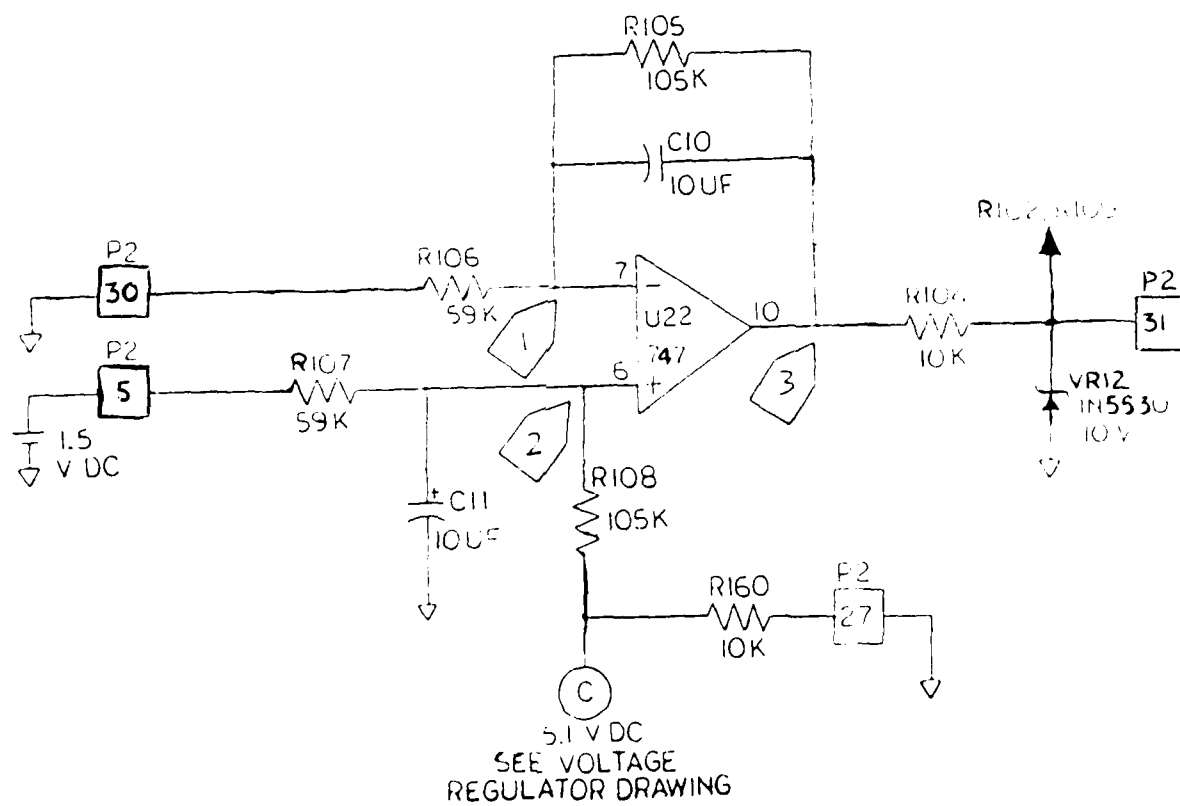


FIGURE 25 - IFMT Op Amp Circuit

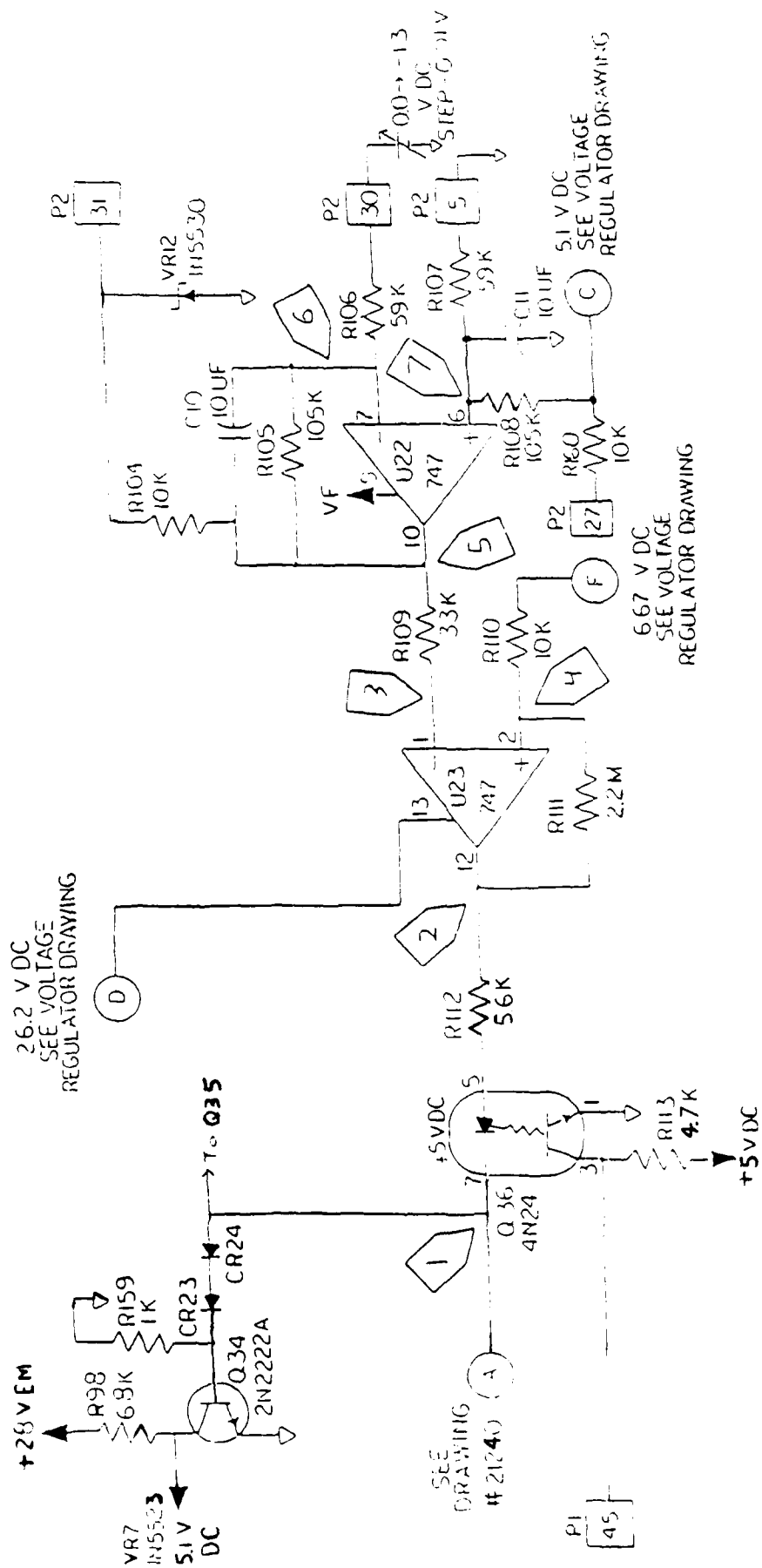


FIGURE 26 - IFML Comparator Circuit

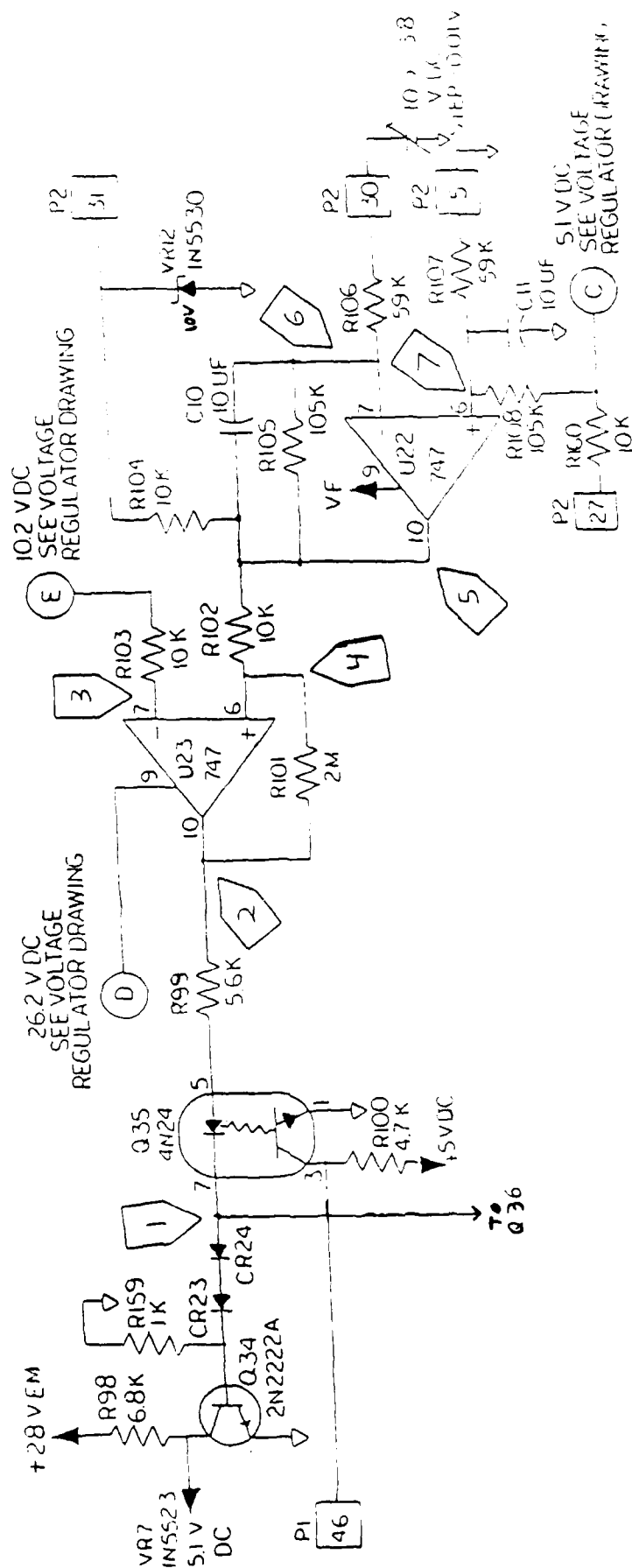


FIGURE 27 - IFMH Comparator Circuit

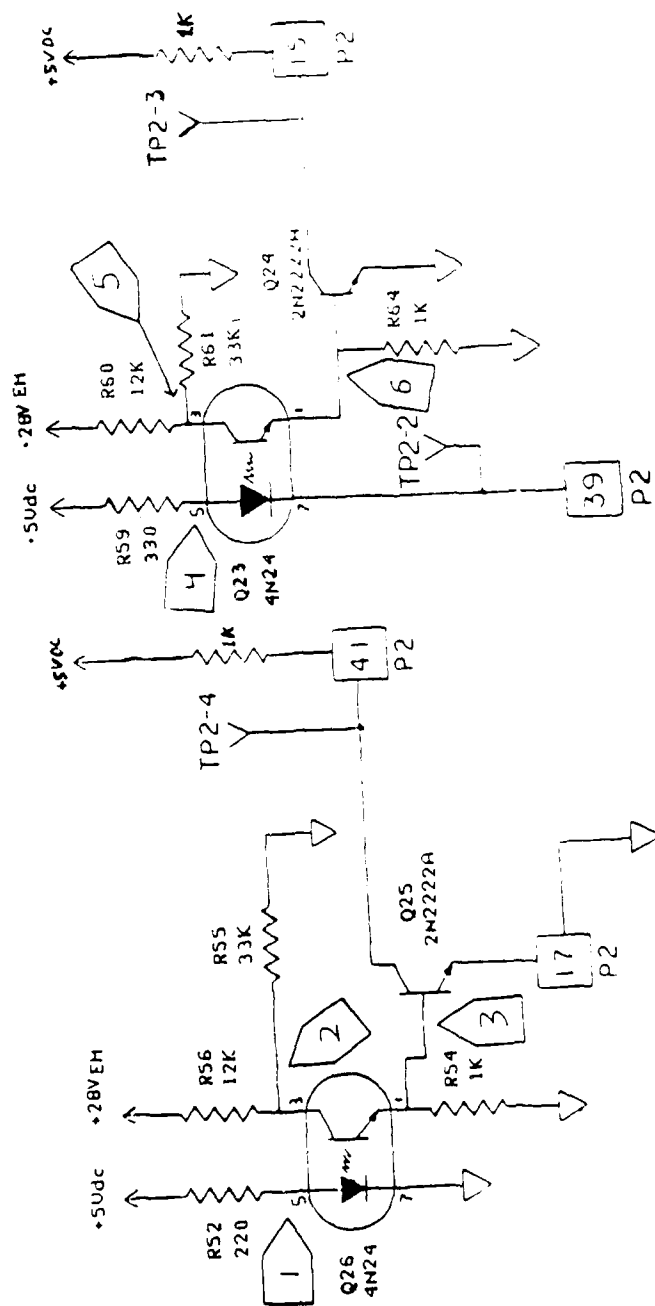


FIGURE 28 - Full Power CDC/FPD Logic Circuits

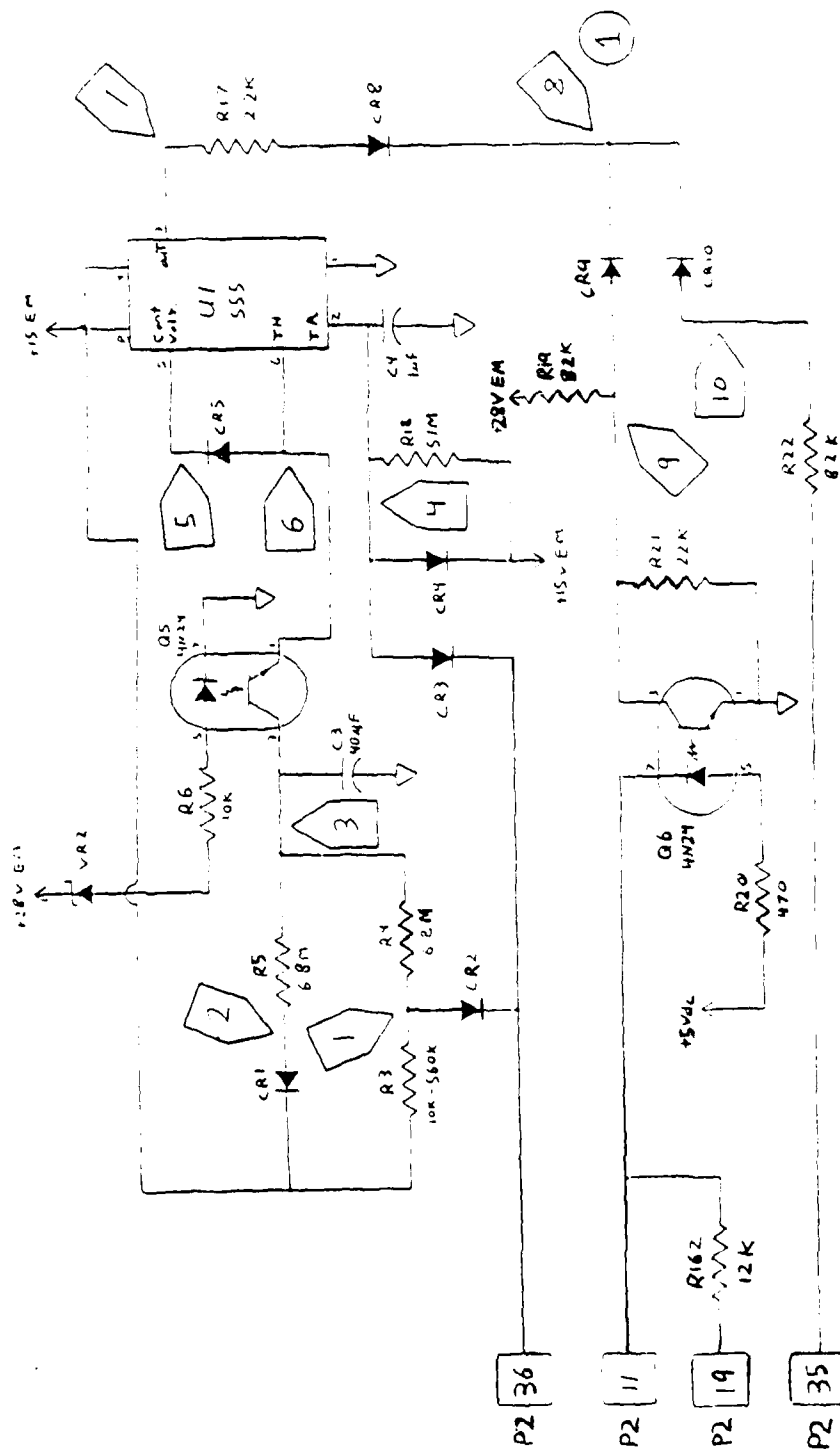


FIGURE 29 - U1 Timer and P2-11/35 Input Circuits

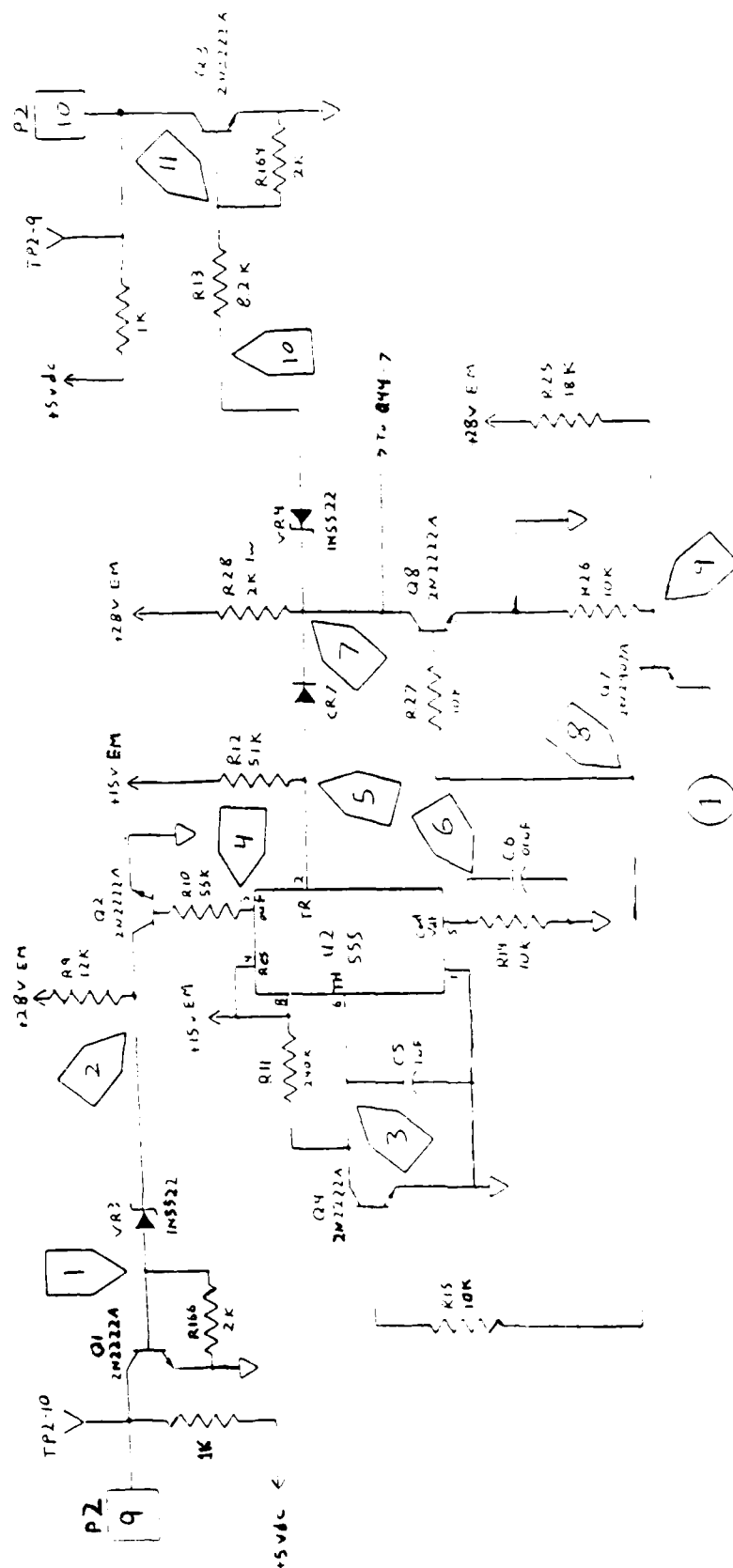


FIGURE 30 - 1/2 Timer and Q7/08 Transistor Circuits

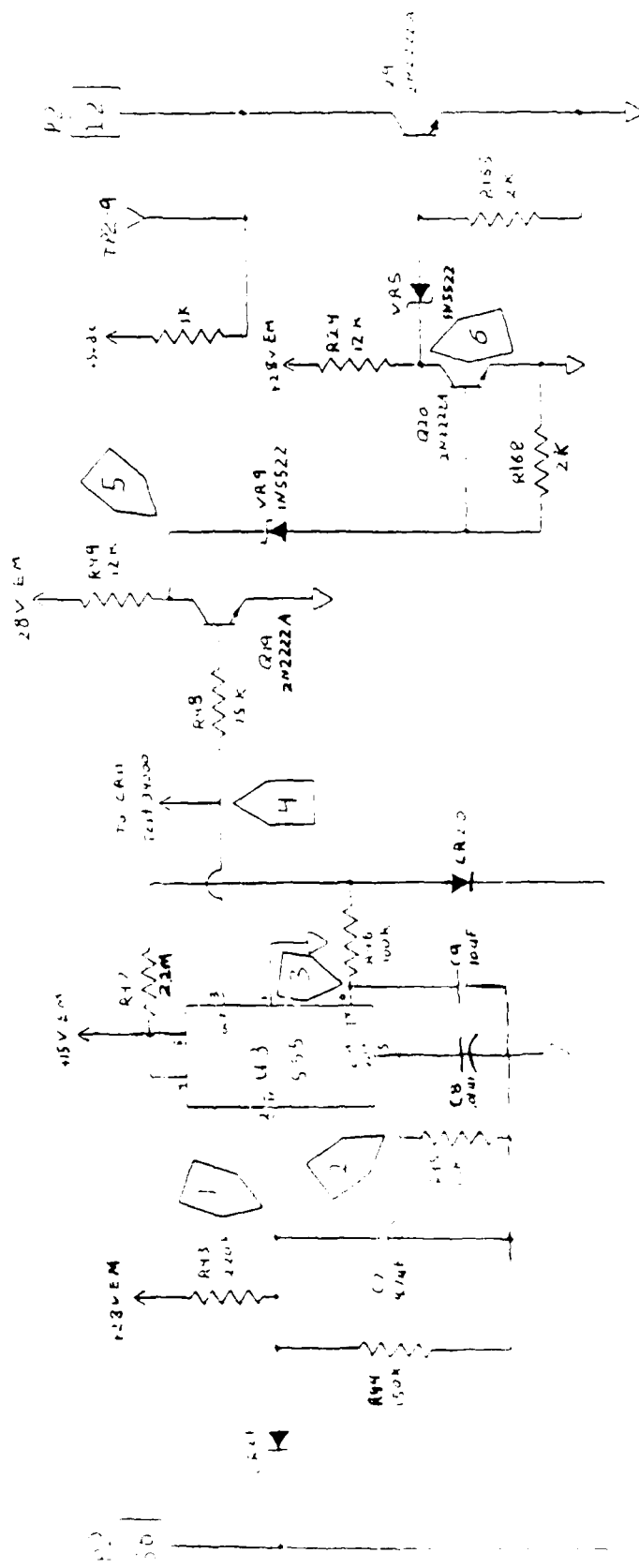
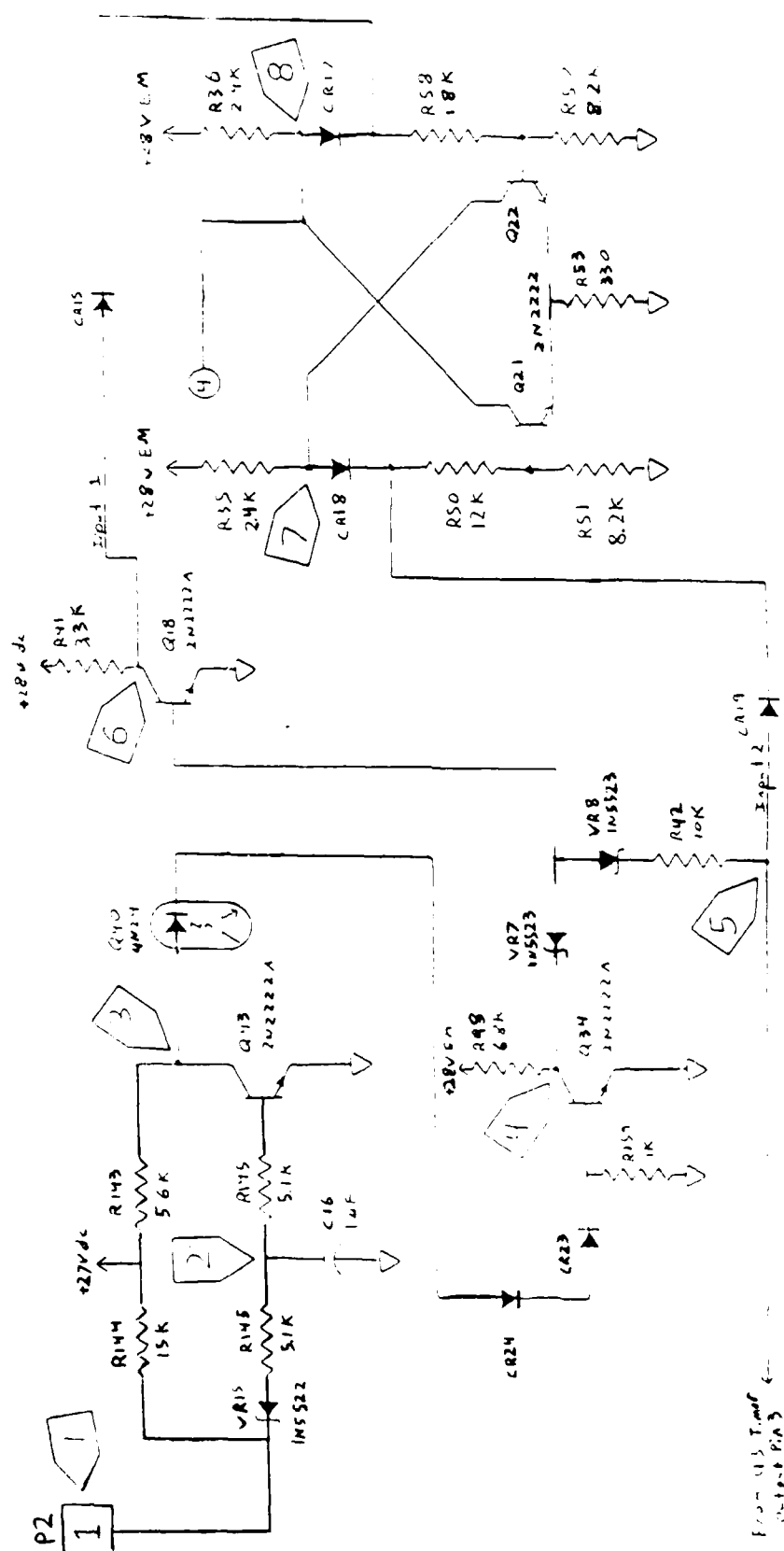


FIGURE 31 - U3 Timer and P2-I2 Output Circuits



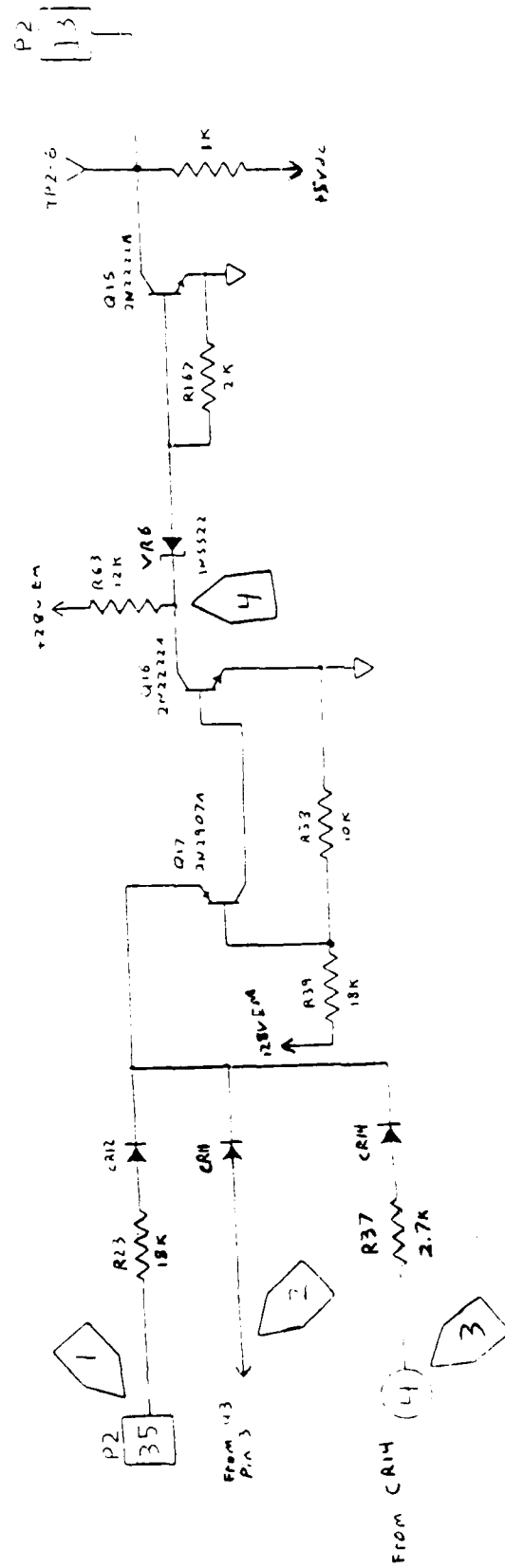


FIGURE 34 - P2-13 Output Circuit

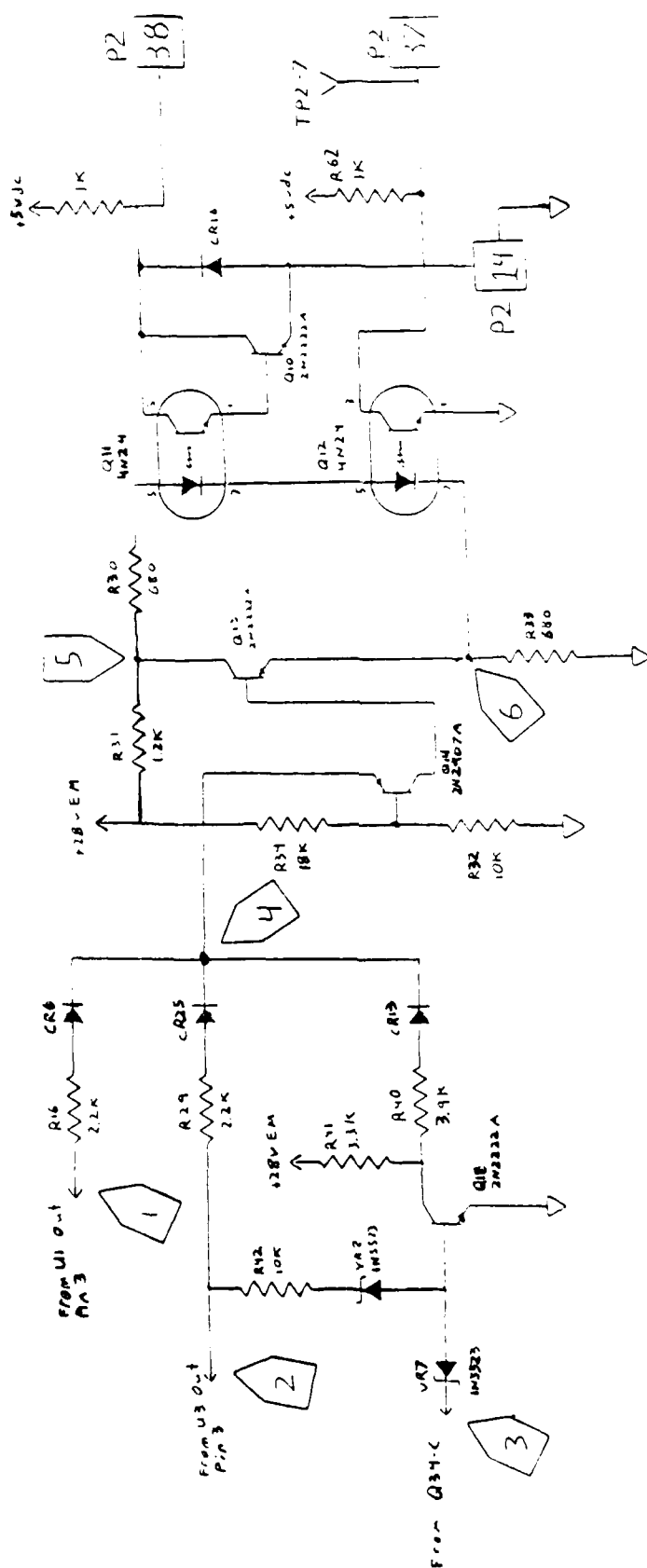


FIGURE 35 - P2-37/38 Outputs Circuit

APPENDIX D
PATCHBOX WIRING LAYOUT AND
ADAPTER CIRCUIT

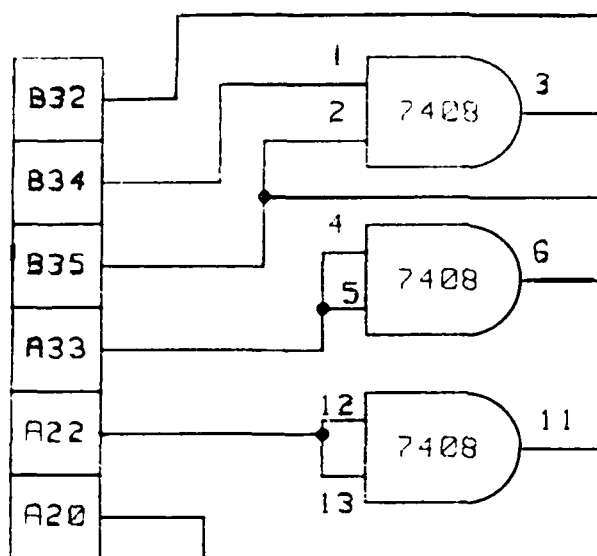
TABLE VI

PATCHBOX JUMPER WIRES

SOURCE	PATCHBOX COORDINATE	PATCHBOX COORDINATE	DESTINATION
P1-1	AA13-----	A10-----	SX 5
		K1-B26-----	ADAPTER
P1-3	AA15-----	A13-----	SX 8
		K1-B27-----	ADAPTER
P1-10	AA22-----	A14-----	SX 9
P1-11	BB13-----	A15-----	SX 10
P1-17	BB19-----	B17-----	SX 29
		AA7-----	GROUND
P1-18	BB20-----	AA10-----	PS1 +
P1-19	BB21-----	K1-A15-----	ADAPTER
P1-43	DD20-----	T13-----	MX 31
		D1-----	RELAY#4
GROUND	JJ7-----	AA11-----	PS1 -
P1-22	CC14-----	A16-----	SX 11
P1-26	CC18-----	A17-----	SX 12
		K1-B25-----	ADAPTER
P1-27	AA24-----	BB7-----	GROUND
P1-34	AA28-----	A18-----	SX 13
P1-42	DD19-----	B16-----	SX 28
		A2-----	RELAY#1
RELAY#1	A1-----	CC7-----	GROUND
P1-45	DD22-----	A19-----	SX 14
P1-46	EE13-----	A20-----	SX 15
P1-47	EE14-----	A21-----	SX 16
P1-48	EE15-----	A22-----	SX 17
TP1-1	LL17-----	B6-----	SX 18
TP1-13	MM19-----	B7-----	SX 19
TP1-14	MM20-----	B8-----	SX 20
TP1-15	MM21-----	B9-----	SX 21
TP1-16	MM22-----	B10-----	SX 22
P2-1	LL16-----	B19-----	SX 31
		J5-----	OC#3
P2-2	GG26-----	A6-----	SX 1
P2-3	GG28-----	A7-----	SX 2
P2-4	GG13-----	B18-----	SX 30
P2-5	GG14-----	A11-----	SX 6
P2-6	GG15-----	D2-----	RELAY#4
P2-7	GG16-----	B13-----	SX 25
P2-8	GG17-----	B14-----	SX 26
P2-9	GG30-----	C19-----	SX 48
		M3-----	DR#12
P2-10	GG18-----	C20-----	SX 49
		P3-----	DR#10
P2-11	GG19-----	B15-----	SX 27
		F2-----	RELAY#6
ADAPTER	K1-A20-----	F1-----	RELAY#6
DW#0	Z4-----	K1-A22-----	ADAPTER
P2-12	GG20-----	T3-----	DR#6
P2-13	GG21-----	R3-----	DR#8
P2-14	GG22-----	B12-----	SX 24

SOURCE	PATCHBOX COORDINATE	PATCHBOX COORDINATE	DESTINATION
P2-15	HH13-----	K3	DR#14
P2-16	HH14-----	B20	SX 32
P2-17	HH15-----	DD7	GROUND
P2-19	HH17-----	B21	SX 33
P2-25	JJ13-----	C21	SX 50
		H2	RELAY#8
GROUND	EE7-----	H1	RELAY#8
P2-26	GG32-----	B22	SX 34
P2-27	JJ14-----	C6	SX 35
P2-28	JJ15-----	A9	SX 4
P2-29	JJ16-----	A8	SX 3
P2-30	JJ17-----	A12	SX 7
P2-31	JJ18-----	C10	SX 39
P2-32	JJ19-----	C11	SX 40
P2-33	GG34-----	C12	SX 41
P2-35	JJ21-----	D6	SX 52
P2-36	JJ22-----	M5	OC#0
P2-37	KK13-----	X3	DR#2
P2-38	KK14-----	Z3	DR#0
		K1-B28	ADAPTER
P2-39	KK15-----	L5	OC#1
P2-41	KK16-----	J3	DR#15
P2-44	KK19-----	V3	DR#4
MX 33	T15-----	C22	SX 51
P2-47	KK22-----	CC11	PS3 -
GROUND	FF7-----	CC10	PS3 +
P2-48	LL13-----	BB10	PS2 +
P2-24	HH22-----	D15	SX A
RELAY#3	C1-----	T14	MX 32
RELAY#3	C2-----	K1-A13	ADAPTER
GROUND	GG7-----	BB11	PS2 -
P2-49	LL14-----	C9	SX 33
		B2	RELAY#2
GROUND	HH7-----	B1	RELAY#2
TP2-1	EE18-----	C14	SX 43
TP2-5	EE22-----	W3	DR#3
TP2-6	FF13-----	S3	DR#7
TP2-7	FF14-----	C13	SX 42
TP2-8	FF15-----	U3	DR#5
TP2-9	FF16-----	Q3	DR#9
TP2-10	FF17-----	N3	DR#11
TP2-11	FF18-----	C15	SX 44
TP2-12	FF19-----	C16	SX 45
TP2-13	FF20-----	C17	SX 46
TP2-14	FF21-----	C18	SX 47
TP2-15	FF22-----	C7	SX 36
TP2-16	DD14-----	C8	SX 37
SX B	D16-----	JJ10	DVS +
SX C	D17-----	DD10	PS4 +
SX D	D18-----	DD11	PS4 -

SOURCE	PATCHBOX COORDINATE	PATCHBOX COORDINATE	DESTINATION
SX E	D19-----	EE10-----	PS5 +
SX F	D20-----	F6-----	DECADE COM
SX G	D21-----	FF10-----	PS6 +
SX H	D22-----	J6-----	DECADE 1MEG
SX I	AA12-----	E26-----	FUNGEN
SX J	BB12-----		
SX K	CC12-----	G32-----	SCOPE CH1
SX L	DD12-----	JJ11-----	DVS -
SX M	EE12-----	W11-----	DVM HI
MX A	W12-----		
SX N	FF12-----	X11-----	DVM LOW
MX B	X12-----		
SX O	GG12-----	Y11-----	DVM S+
MX C	Y12-----		
SX P	HH12-----	Z11-----	DVM S-
RELAY#5	E2-----		
RELAY#5	E1-----	Z12-----	MX D
SX Q	JJ12-----	E24-----	COUNTER A
GROUND	HH9-----		
SX R	KK12-----	G24-----	COUNTER B
SX S	LL12-----	K1-B32-----	ADAPTER
SX T	MM12-----	AA8-----	GROUND
ADAPTER	K1-A17-----	CC8-----	GROUND
PULSE	J30-----	K1-B34-----	ADAPTER
PUL/FUN	J28-----	C30-----	PULSE EXT IN
SX 23	B11-----	K1-B35-----	ADAPTER
DW#1	Y4-----	K1-A24-----	ADAPTER
DW#2	X4-----	K1-A33-----	ADAPTER
JUMPER	MM1-----	MM2-----	JUMPER
MX 99	Z21-----1 Kohm-----	Z20-----	MX 98
MX 100	Z22-----1 Kohm-----		
C1-1	K6-----	Q13-----	MX 1
		D7-----	SX 53
C1-2	L6-----	Q14-----	MX 2
		D8-----	SX 54
C1-6	Q6-----	Q18-----	MX 6
		D9-----	SX 55
C1-7	R6-----	Q19-----	MX 7
C1-10	U6-----	Q22-----	MX 10
C1-12	W6-----	R14-----	MX 12
RED PRB.	N7-----	R17-----	MX 15
		D10-----	SX 56
BLACK PRB.	S7-----	R18-----	MX 16
		C11-----	SX 57
YELLOW PRB.	L7-----	R19-----	MX 17
ORANGE PRB.	M7-----	R20-----	MX 18
GREEN PRB.	R7-----	R21-----	MX 19
BLUE PRB.	Q7-----	R22-----	MX 20
WHITE PRB.	K7-----	S13-----	MX 21
PURPLE PRB.	P7-----	S14-----	MX 22
GROUND	E21-----	Z19-----	MX 97



K1 CONNECTOR

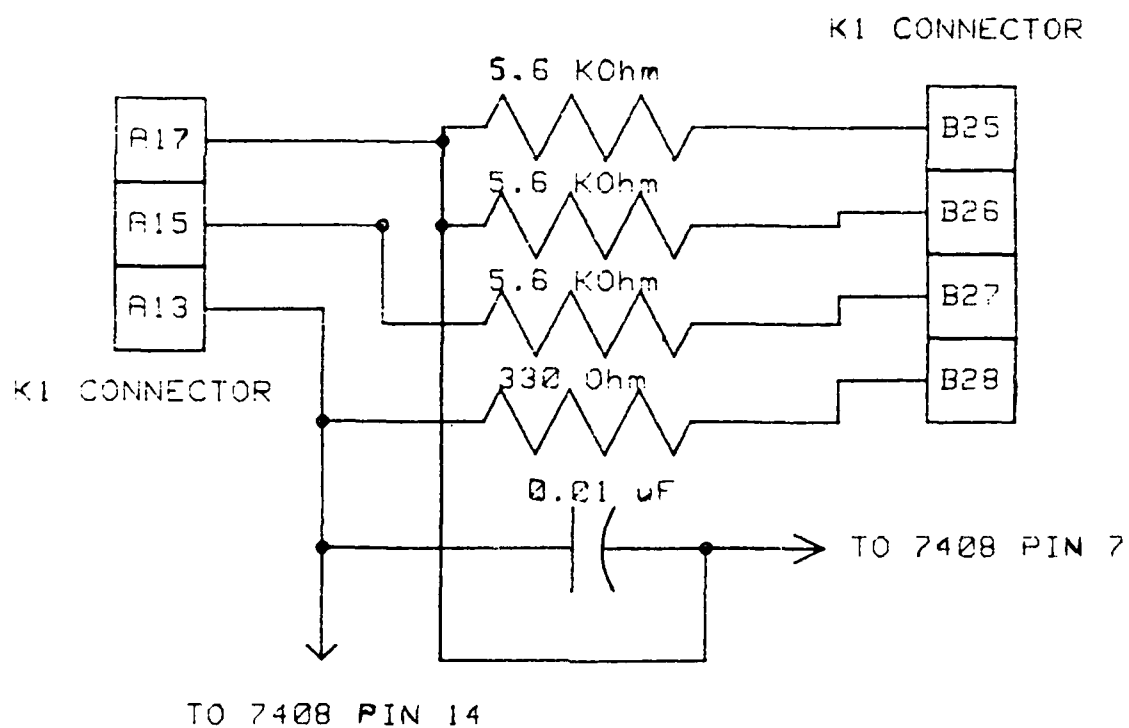


FIGURE 36 - Patchbox Adapter Circuit

APPENDIX E
FAULT ISOLATION FLOWCHARTS

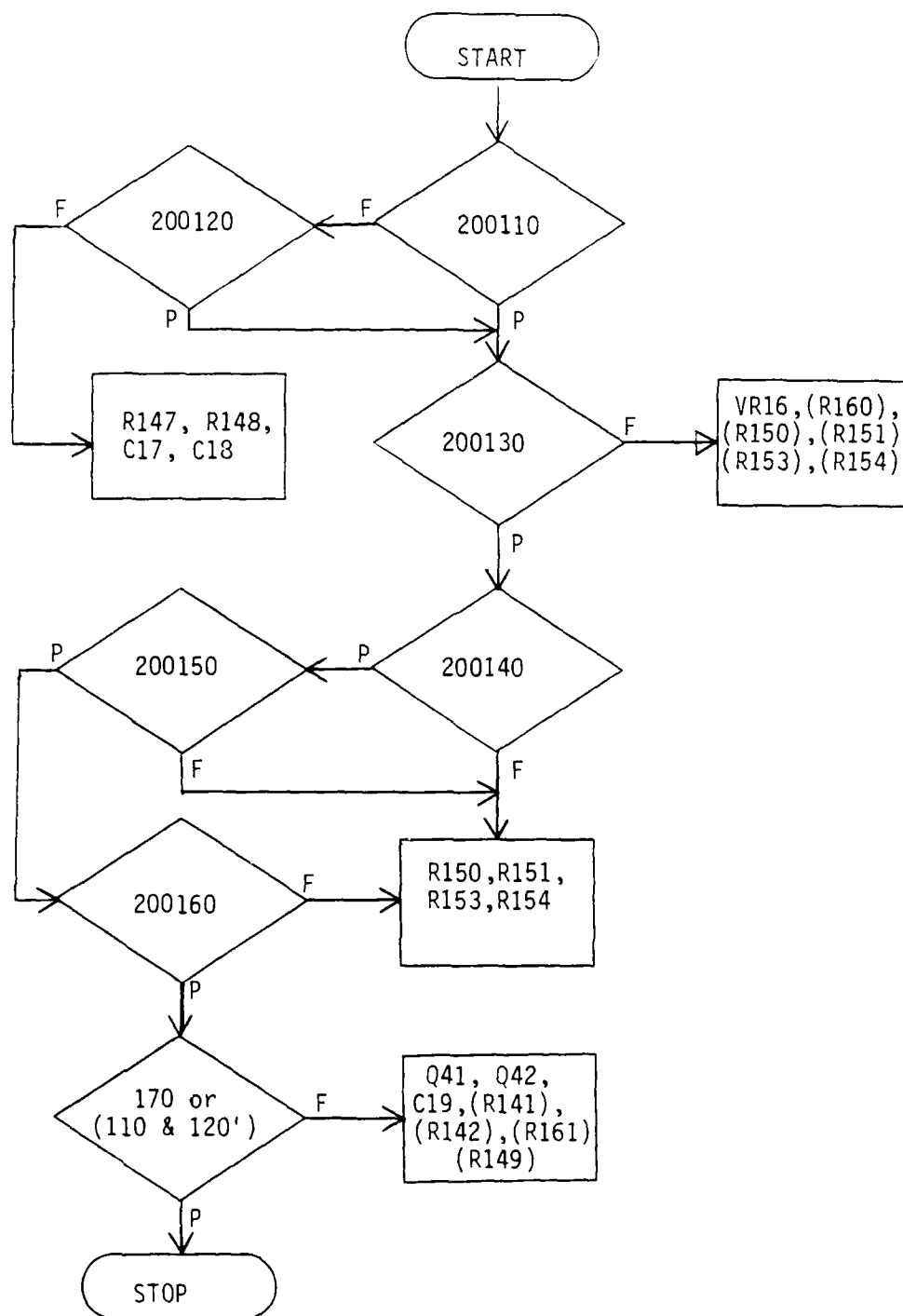


FIGURE 37 - Voltage Regulator Circuit FI Flowchart

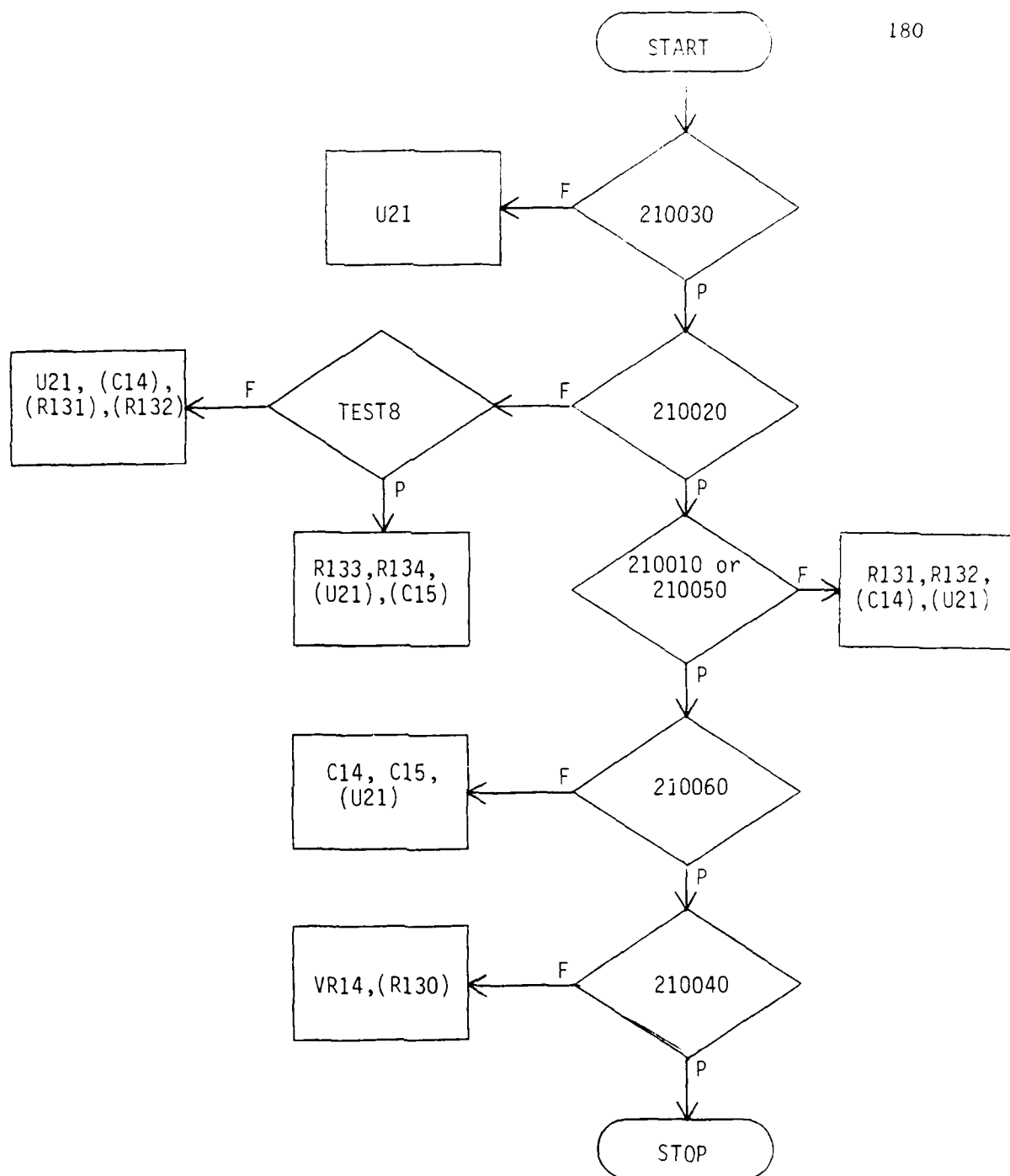


FIGURE 38 - VBMT Op Amp Circuit FI Flowchart

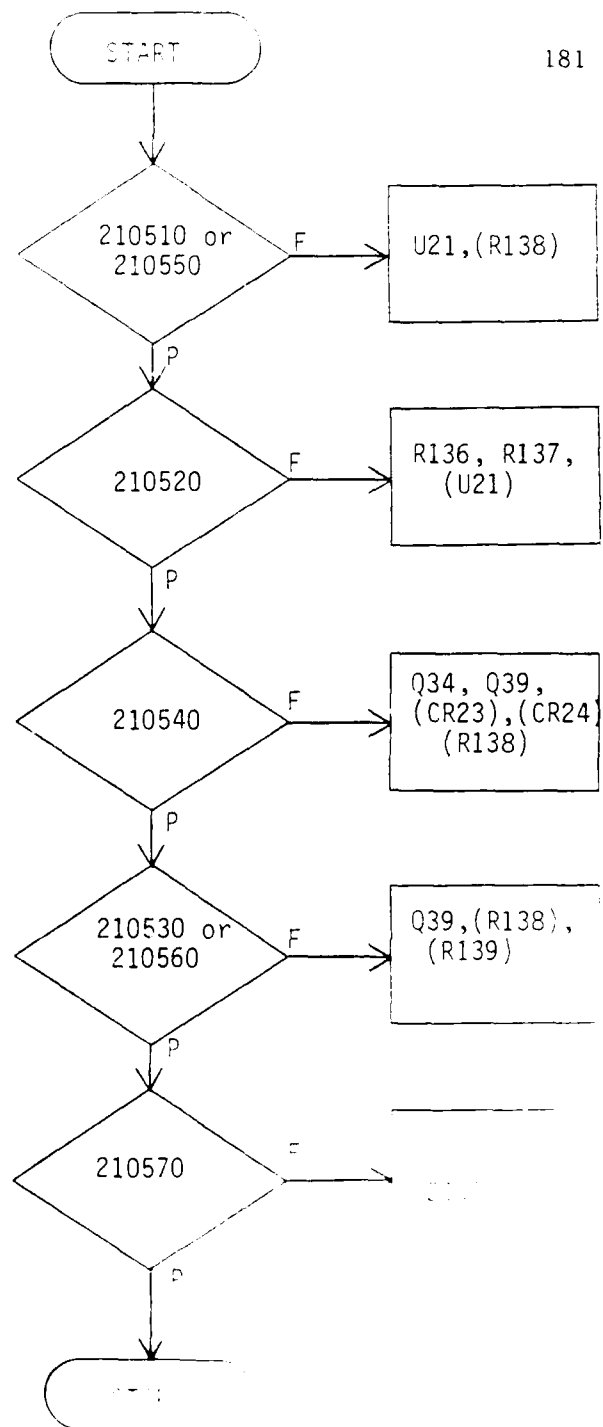


FIGURE 22 - (Continued)

AD-A177 074

AUTOMATED TESTING AND FAULT ISOLATION OF A LOW
FREQUENCY ANALOG CIRCUIT CARD ASSEMBLY (U) LOUISVILLE
UNIV KY M D PILKENTON 17 SEP 86

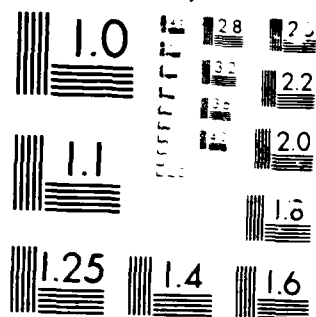
3/3

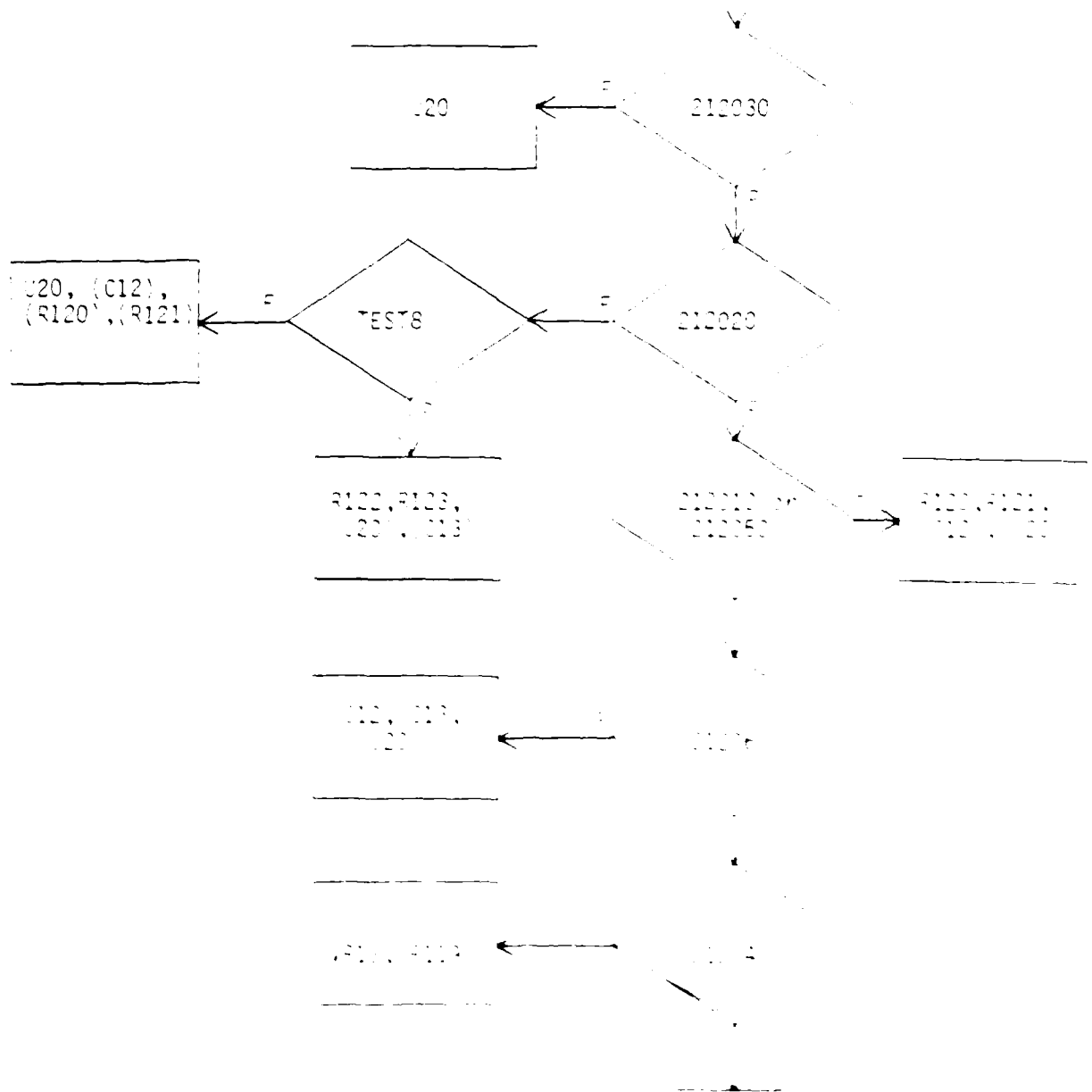
UNCLASSIFIED

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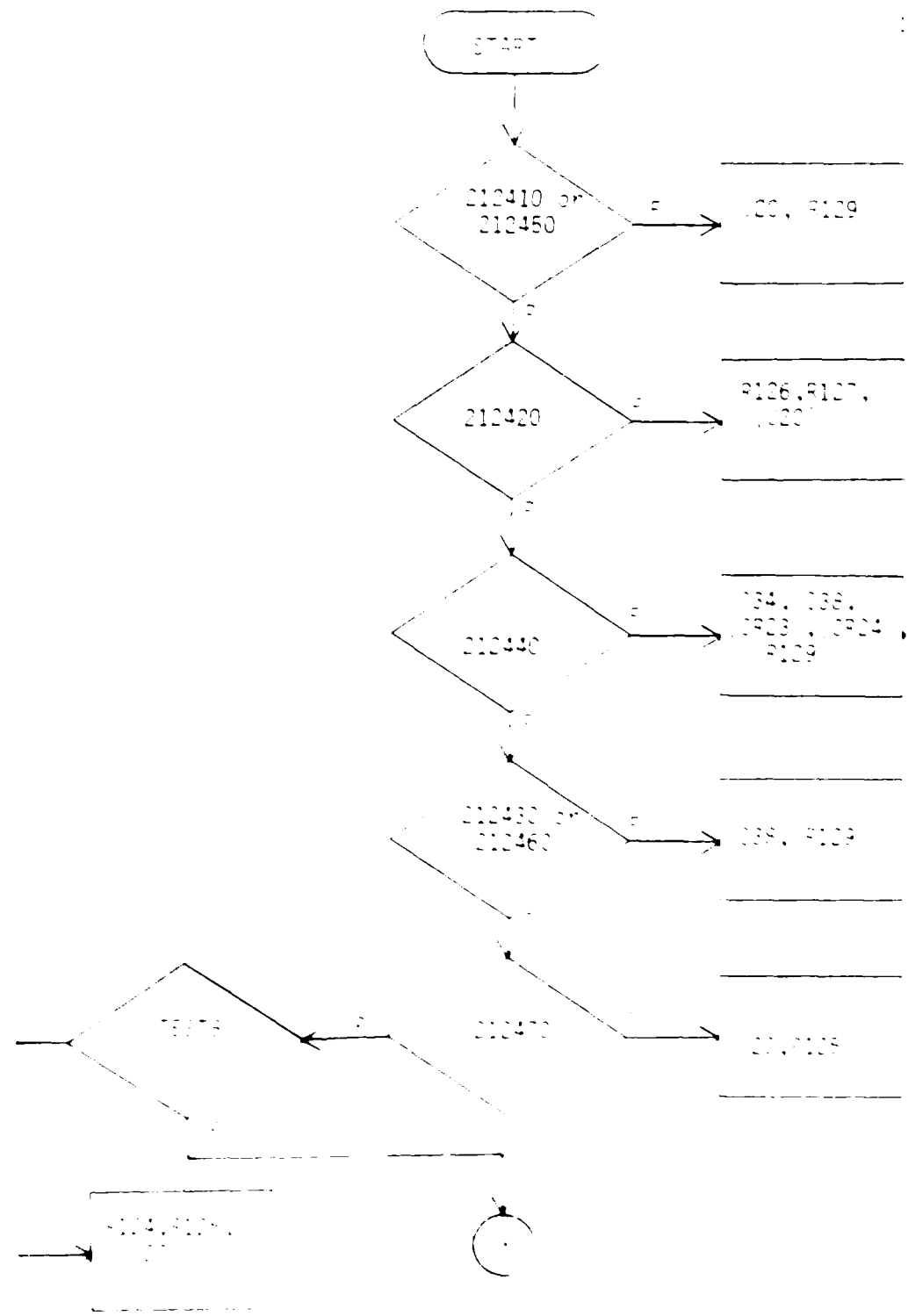


Figure 4: Flowchart of the data processing program for the flow meter

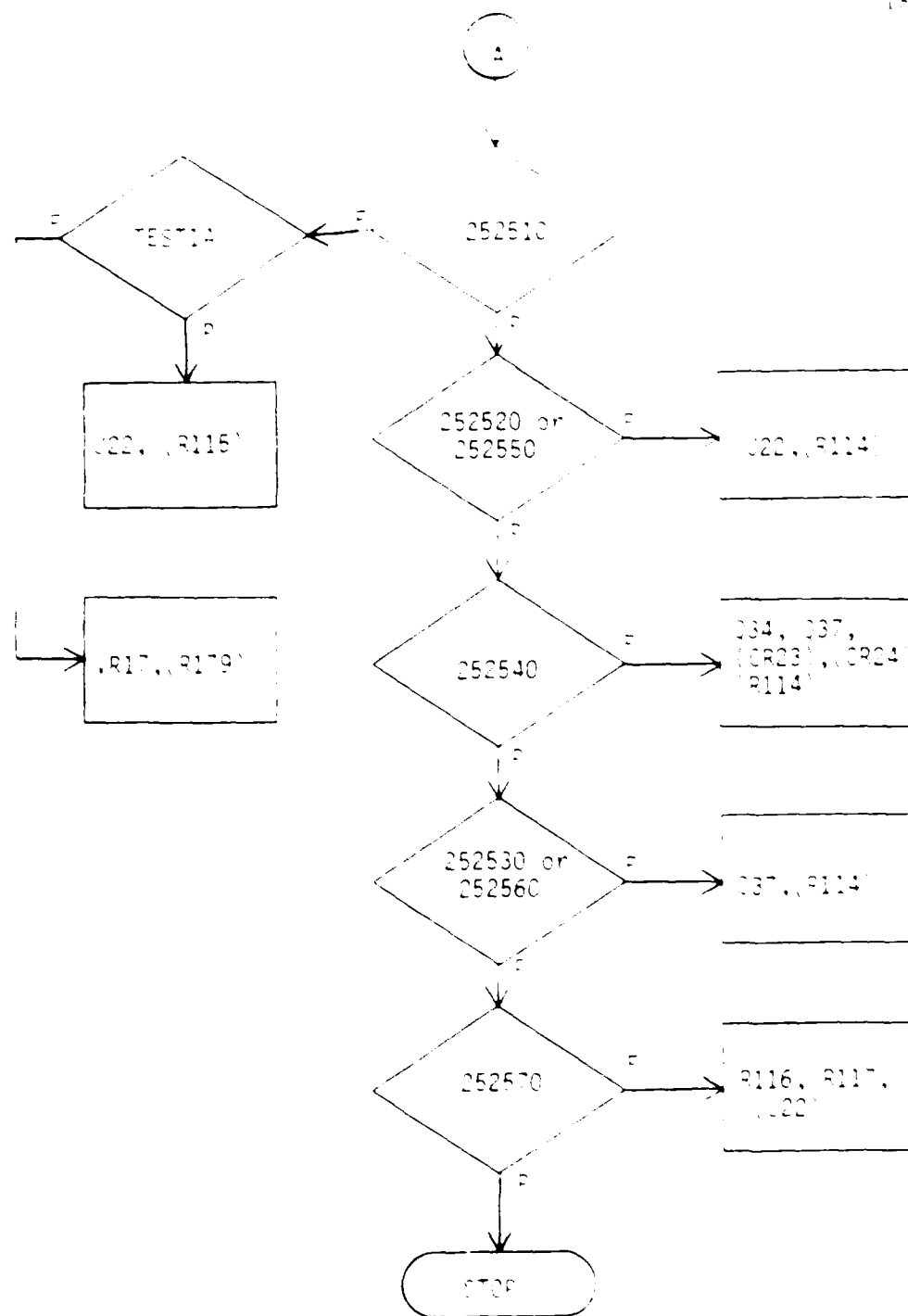


FIGURE 41 - (continued)

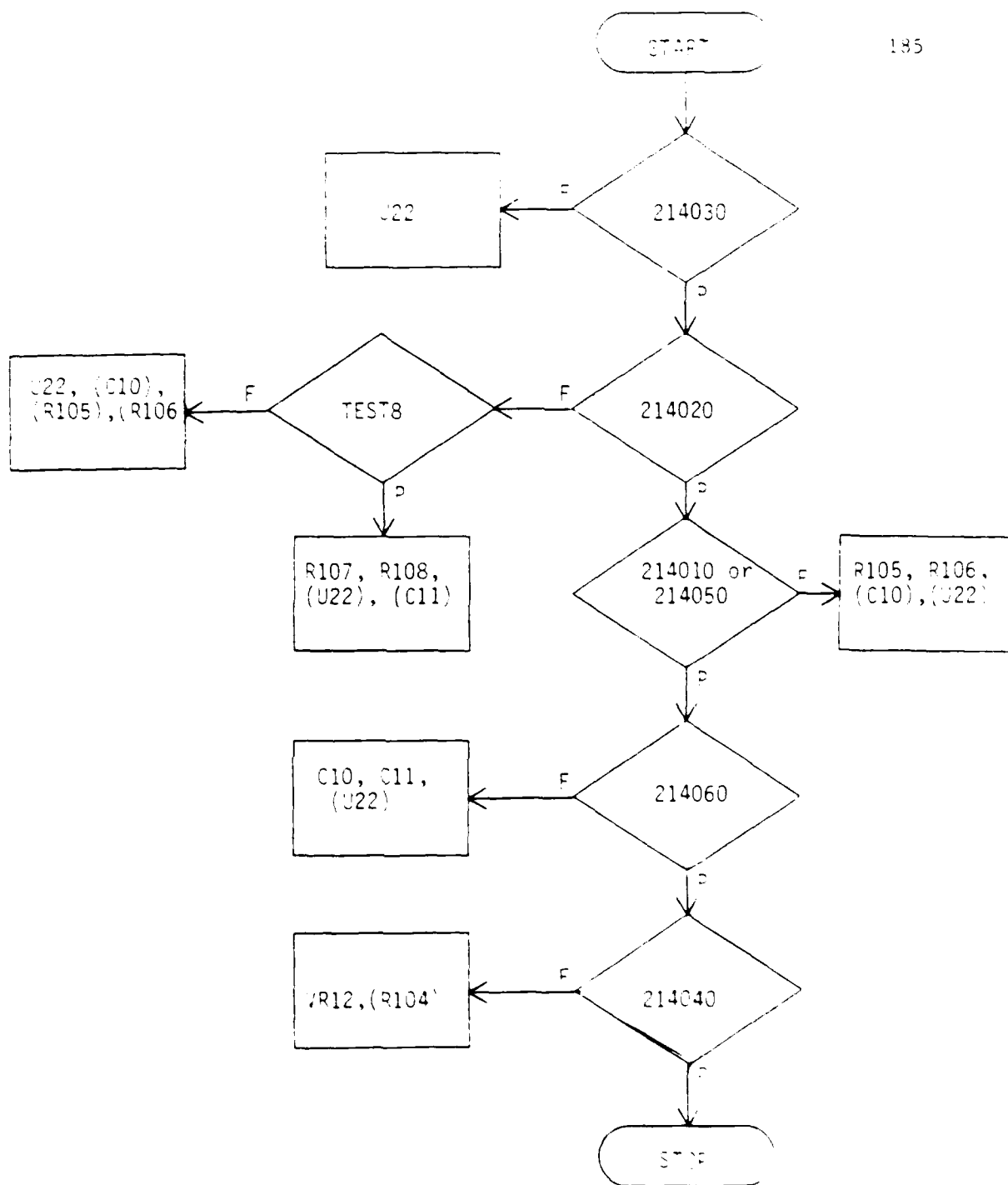


FIGURE 42 - IFMT Op Amp Circuit F1 Flowchart

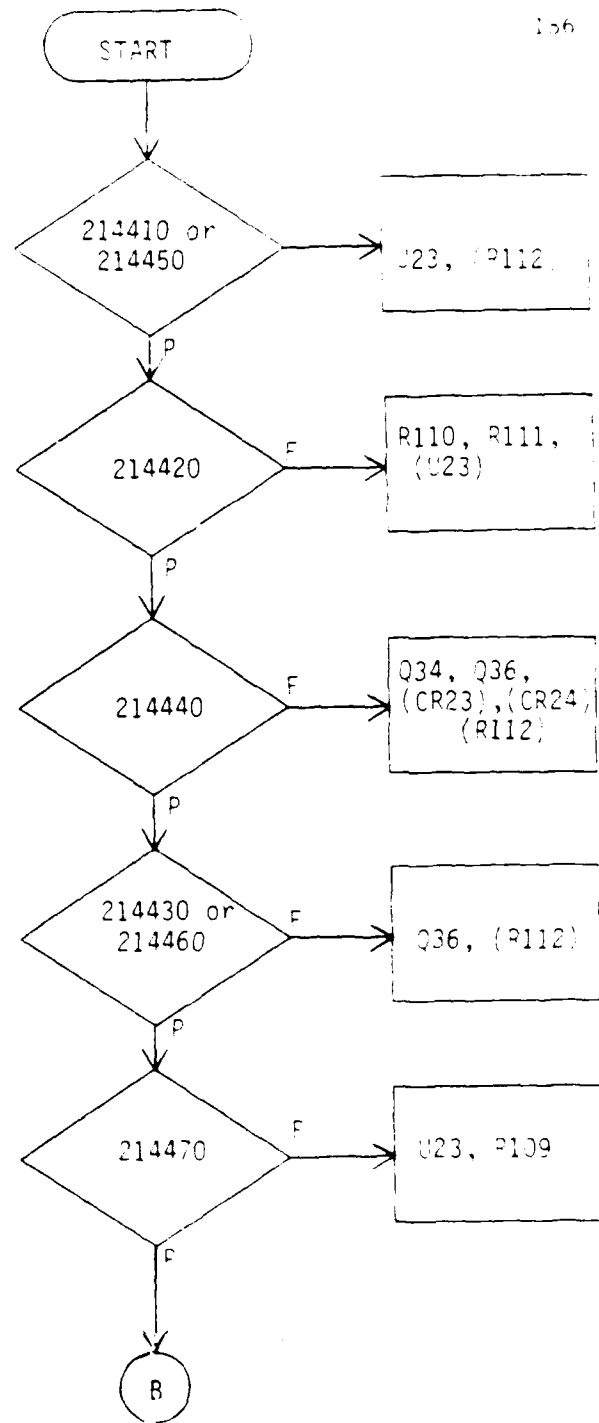


FIGURE 43 - IFML and IFMH Comparator Circuits FI Flowchart

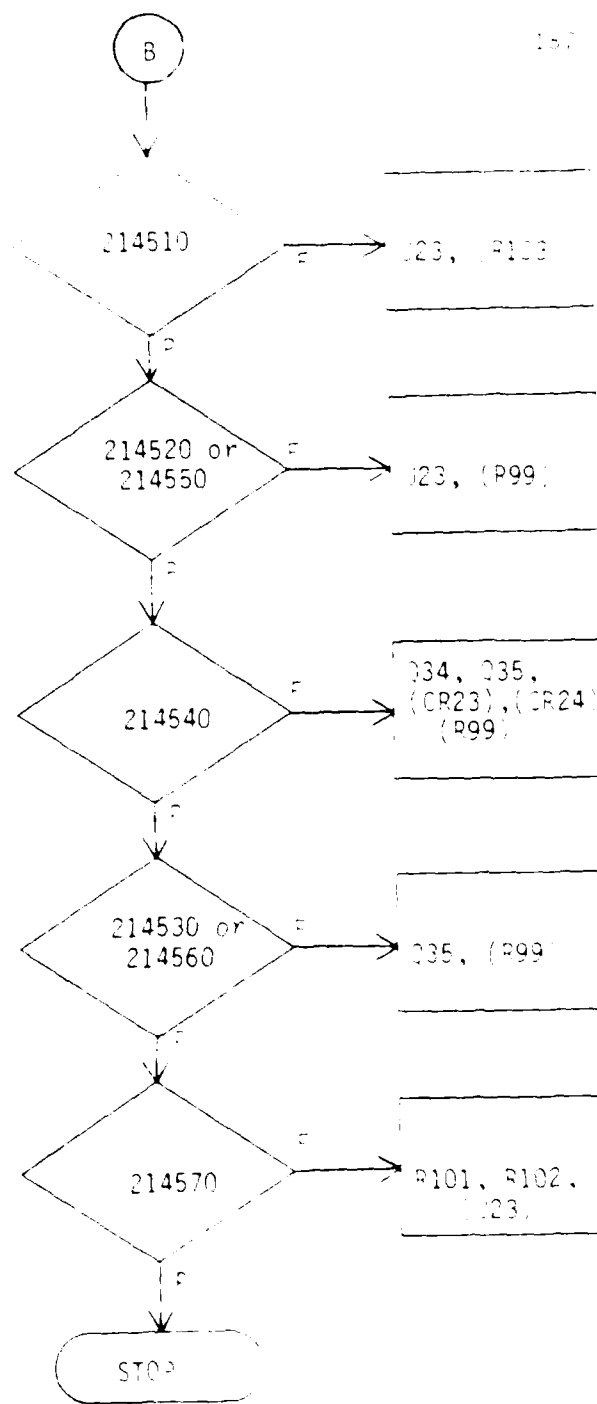


FIGURE 43 - (continued)

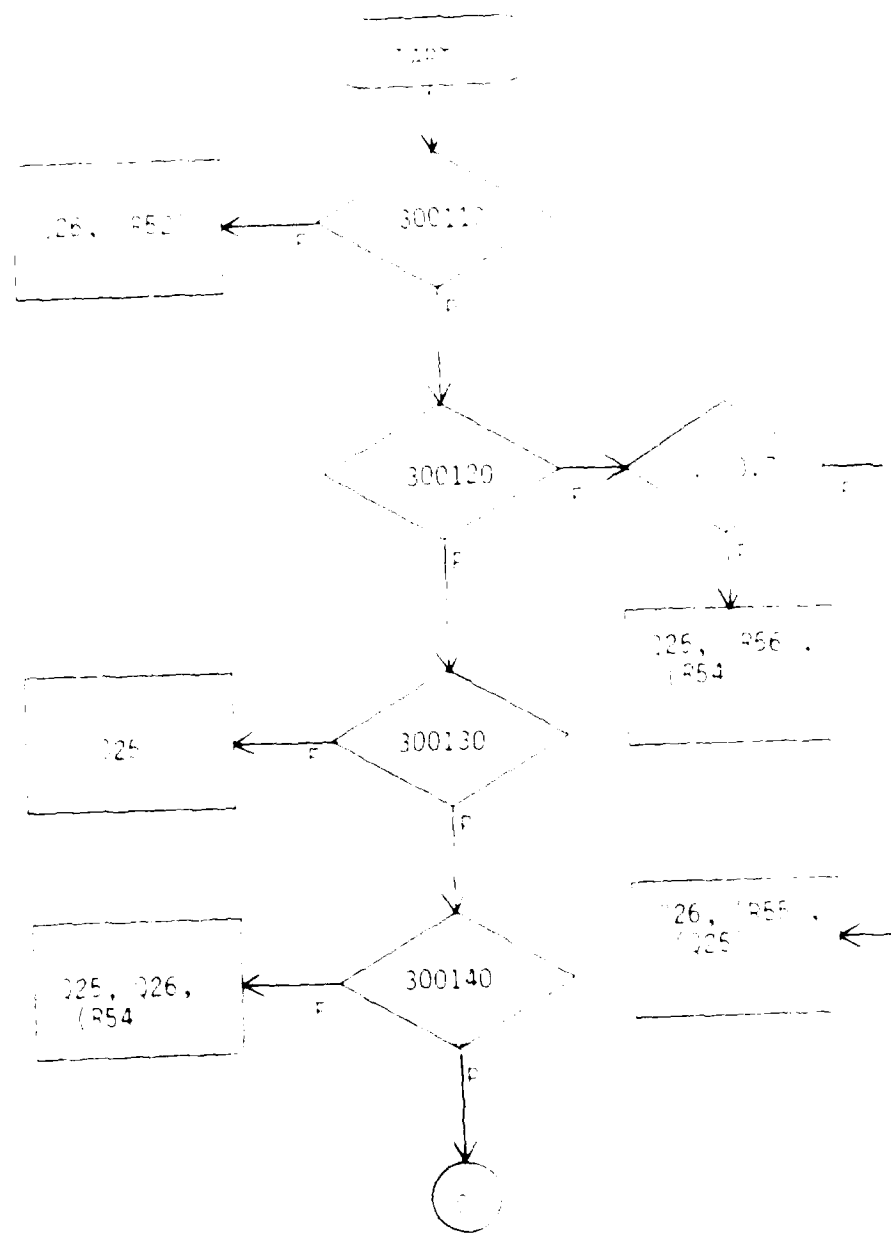


FIGURE 44 - Full Power CDC FPD Logic (Results FI) Flowchart

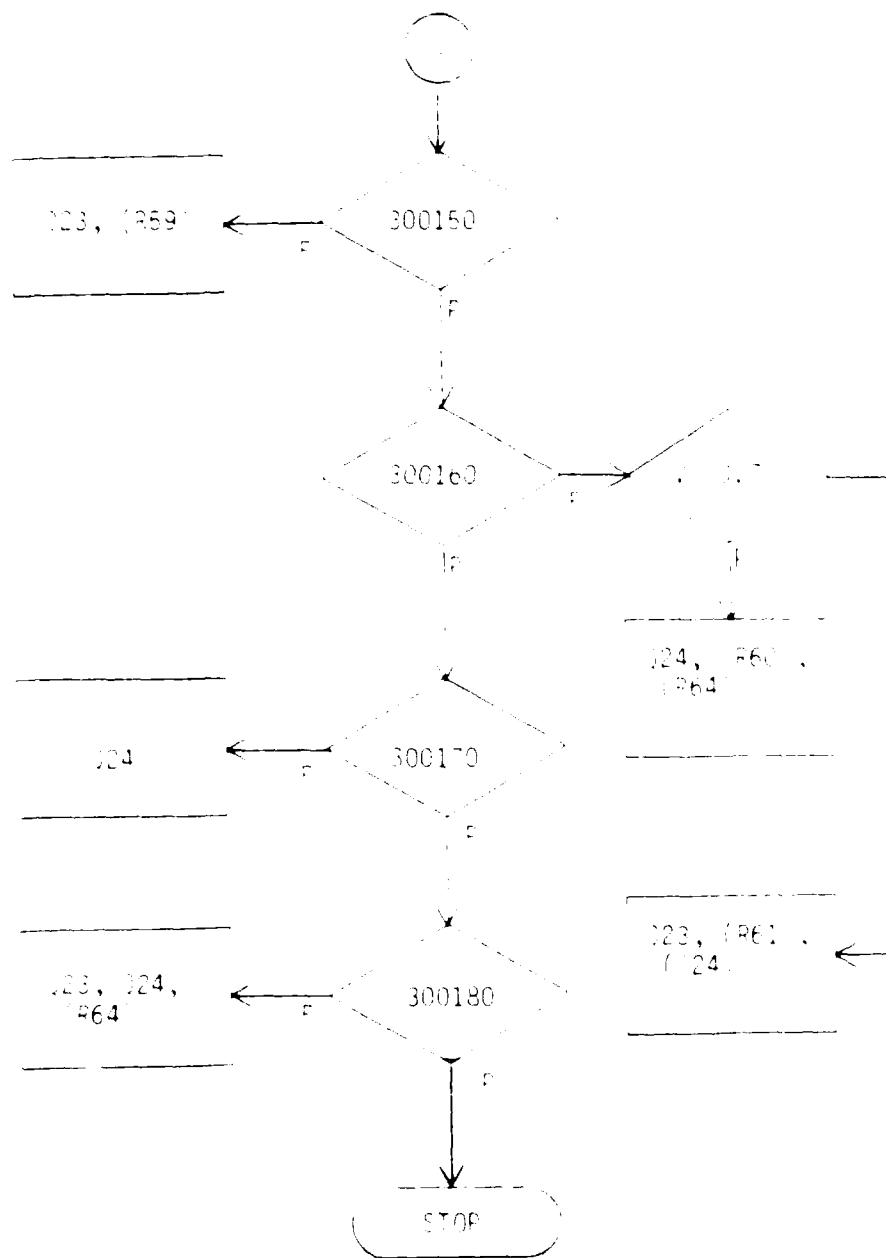


FIGURE 44 - (continued)

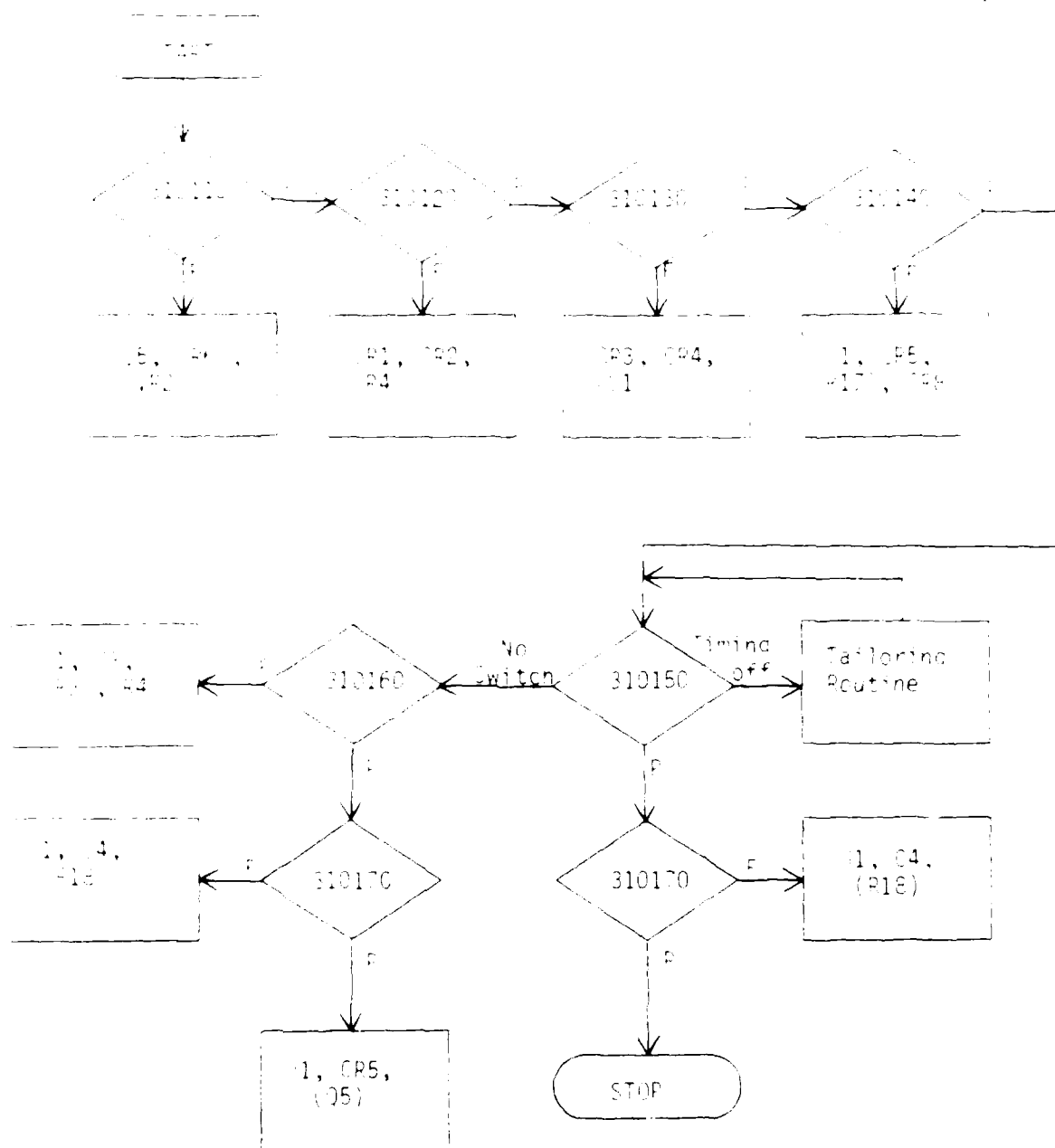


FIGURE 45 - U1 Timer Circuit .1 Flowchart

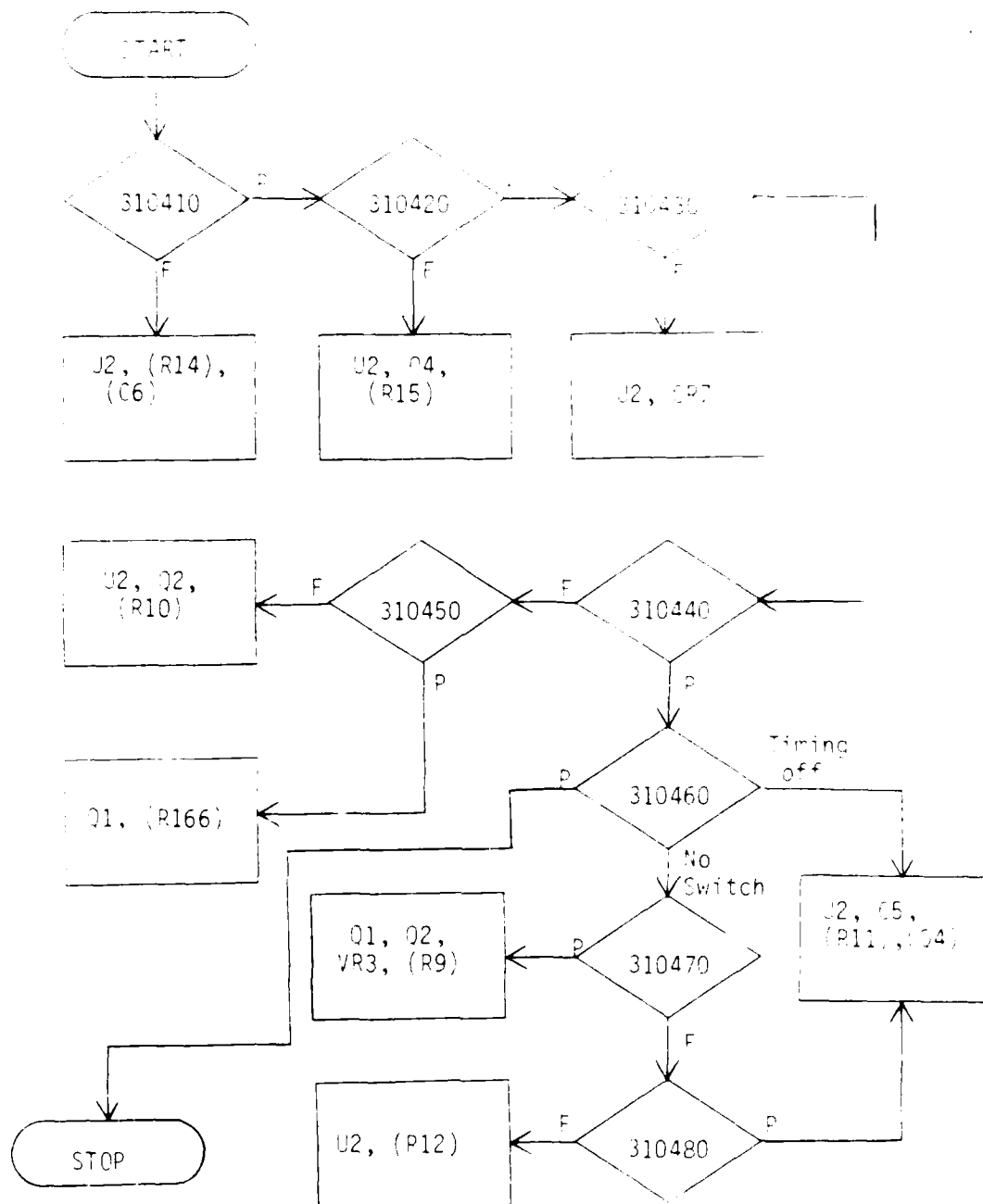


FIGURE 46 - U2 Timer Circuit FI Flowchart

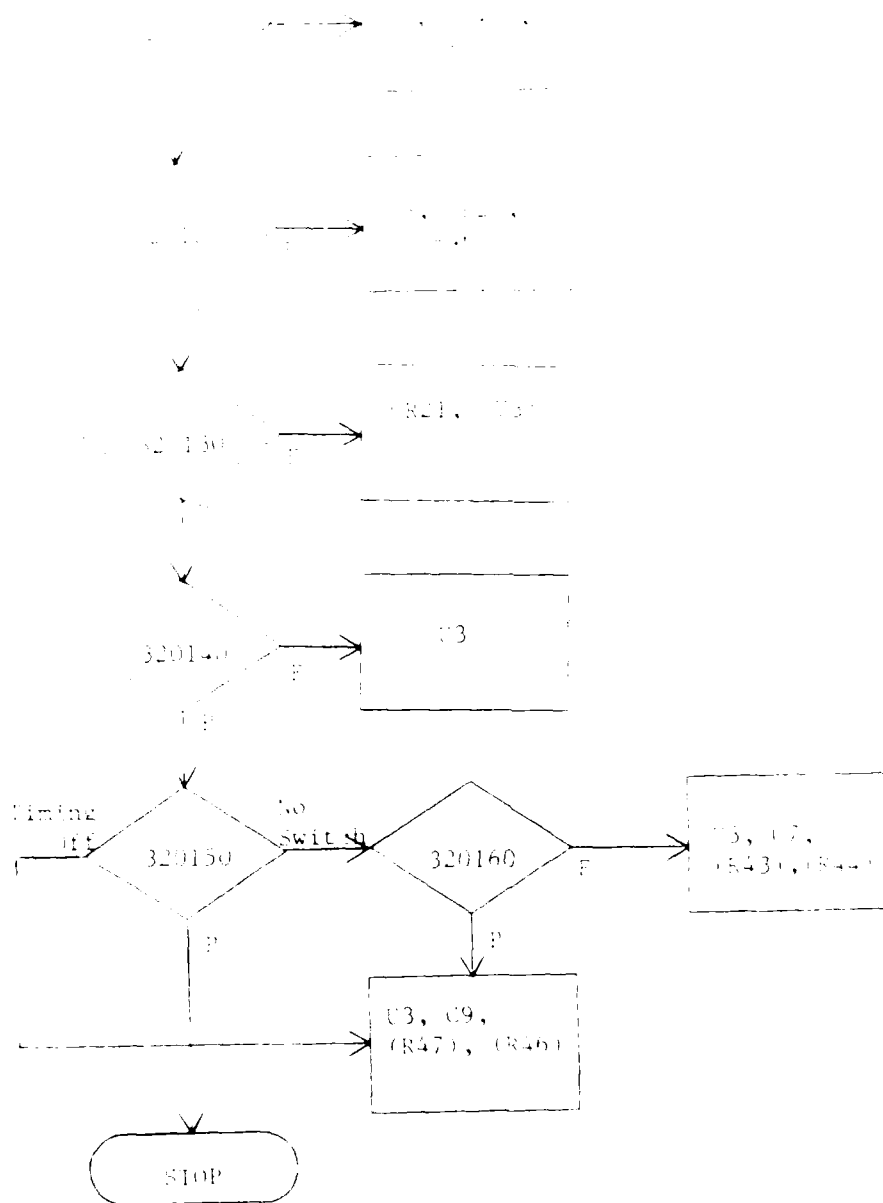


FIGURE 47 - R3 Timer Circuit FI Flowchart

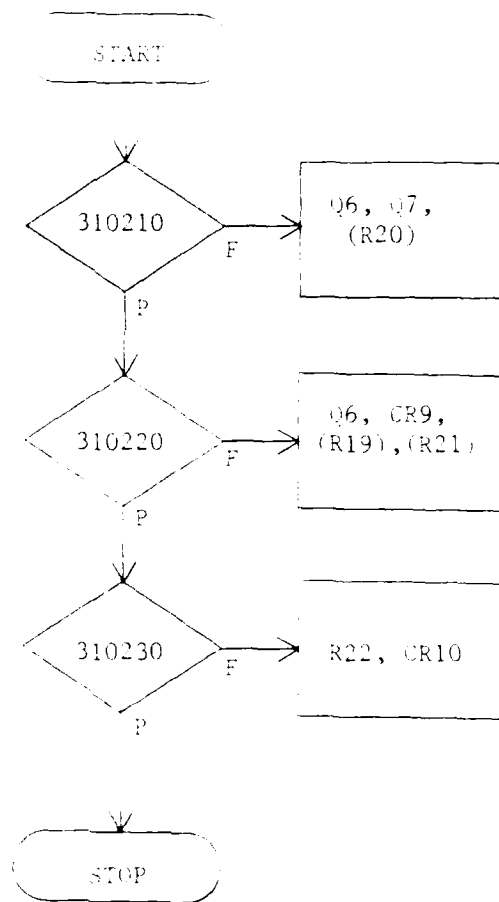
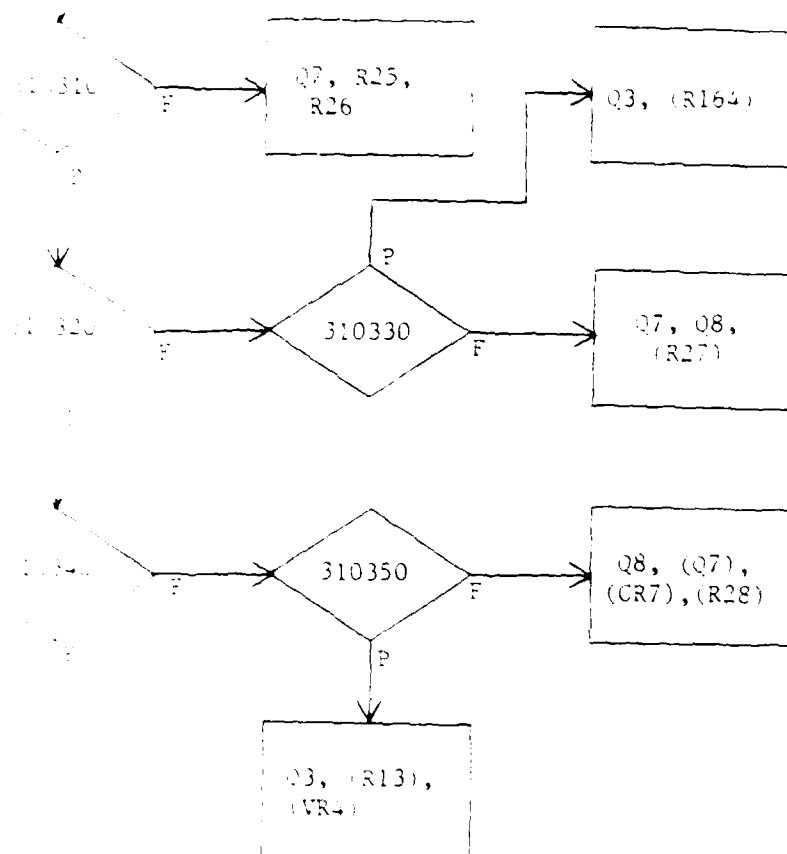


FIGURE 49 - P2-11/35 Inputs Circuit F1 Flowchart

START



END

Figure 2 - 2N408 Transistor Circuit FI Flowchart

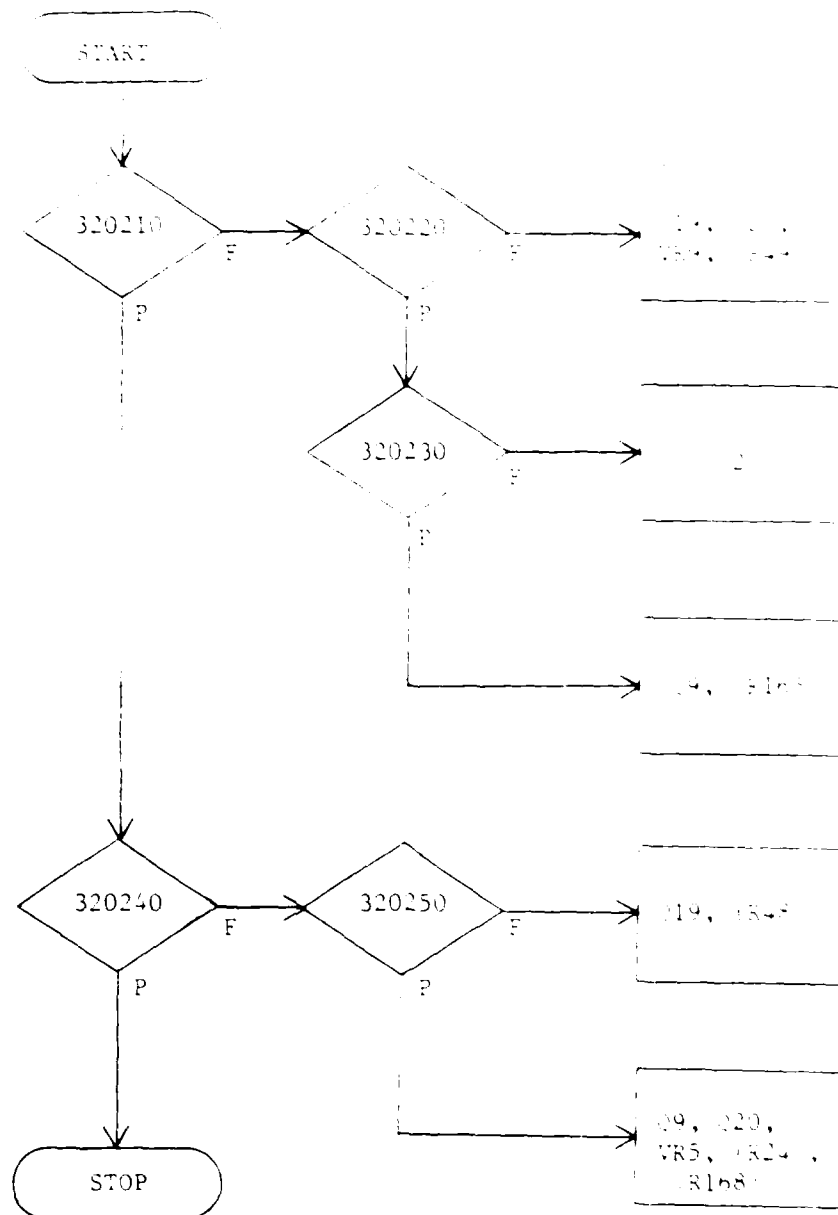


FIGURE 51 - P2-12 Output Circuit F1 Flowchart

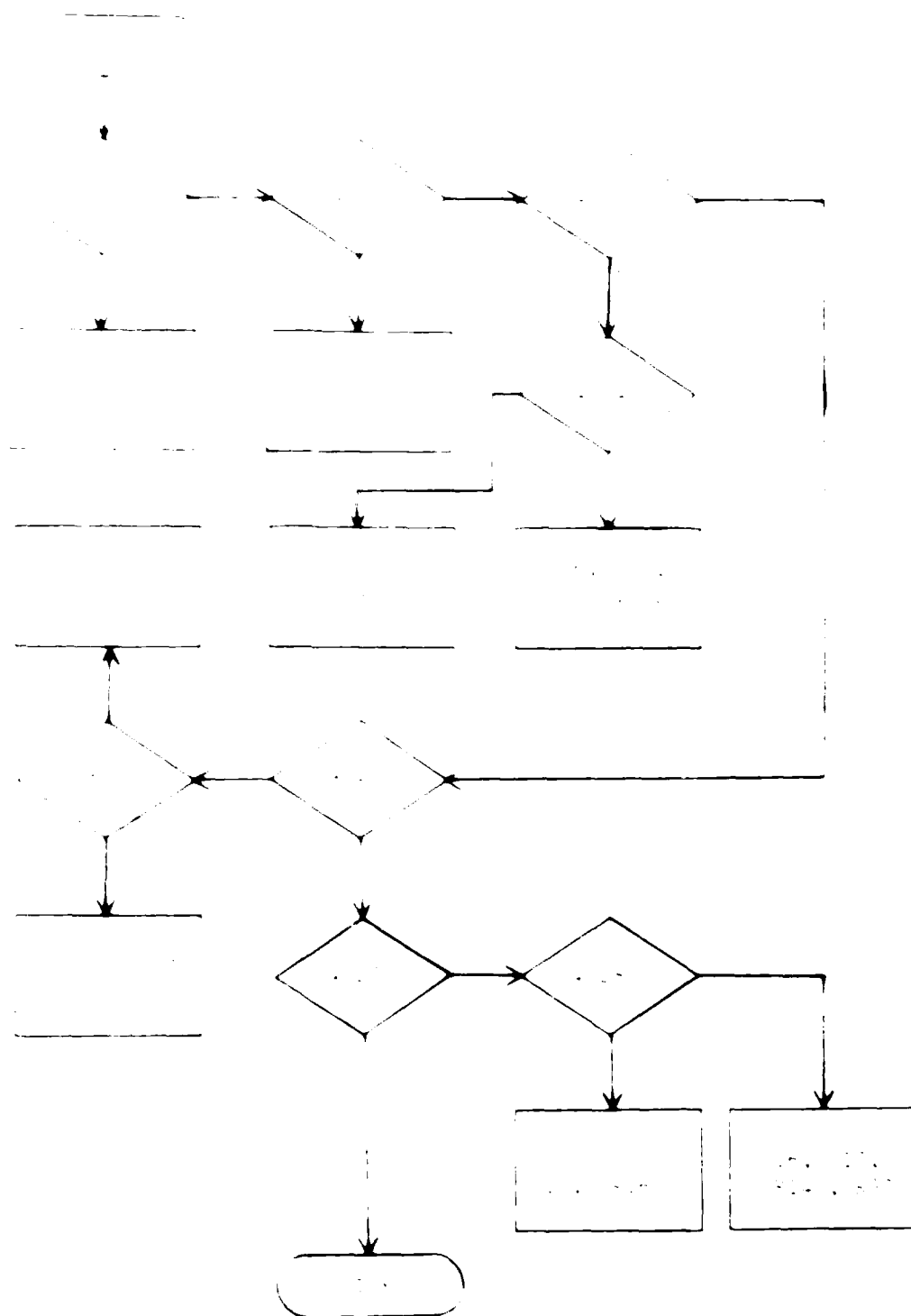


Figure 1. Control Unit Flowchart

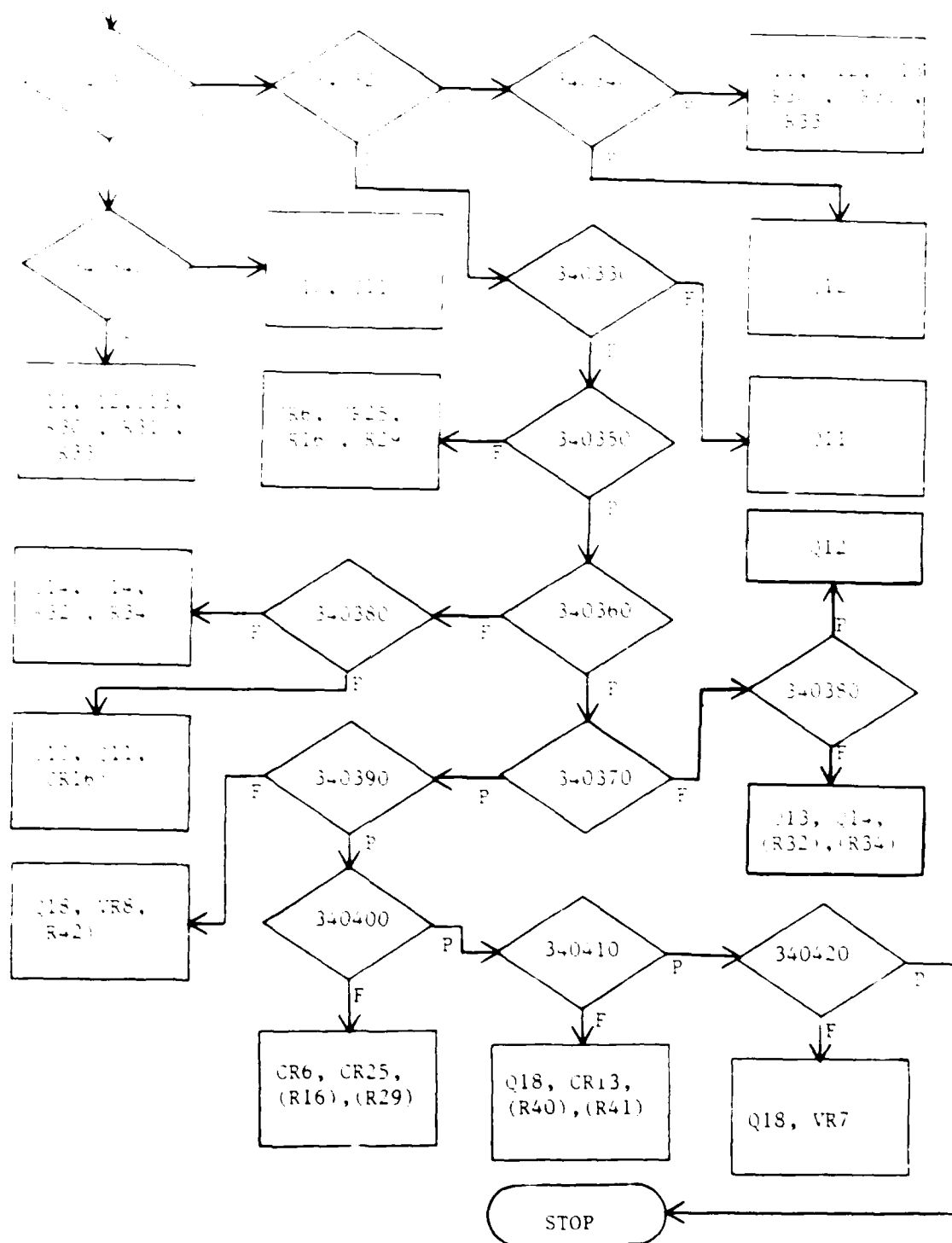


FIGURE 54 - P2-37/38 Outputs Circuit FI Flowchart

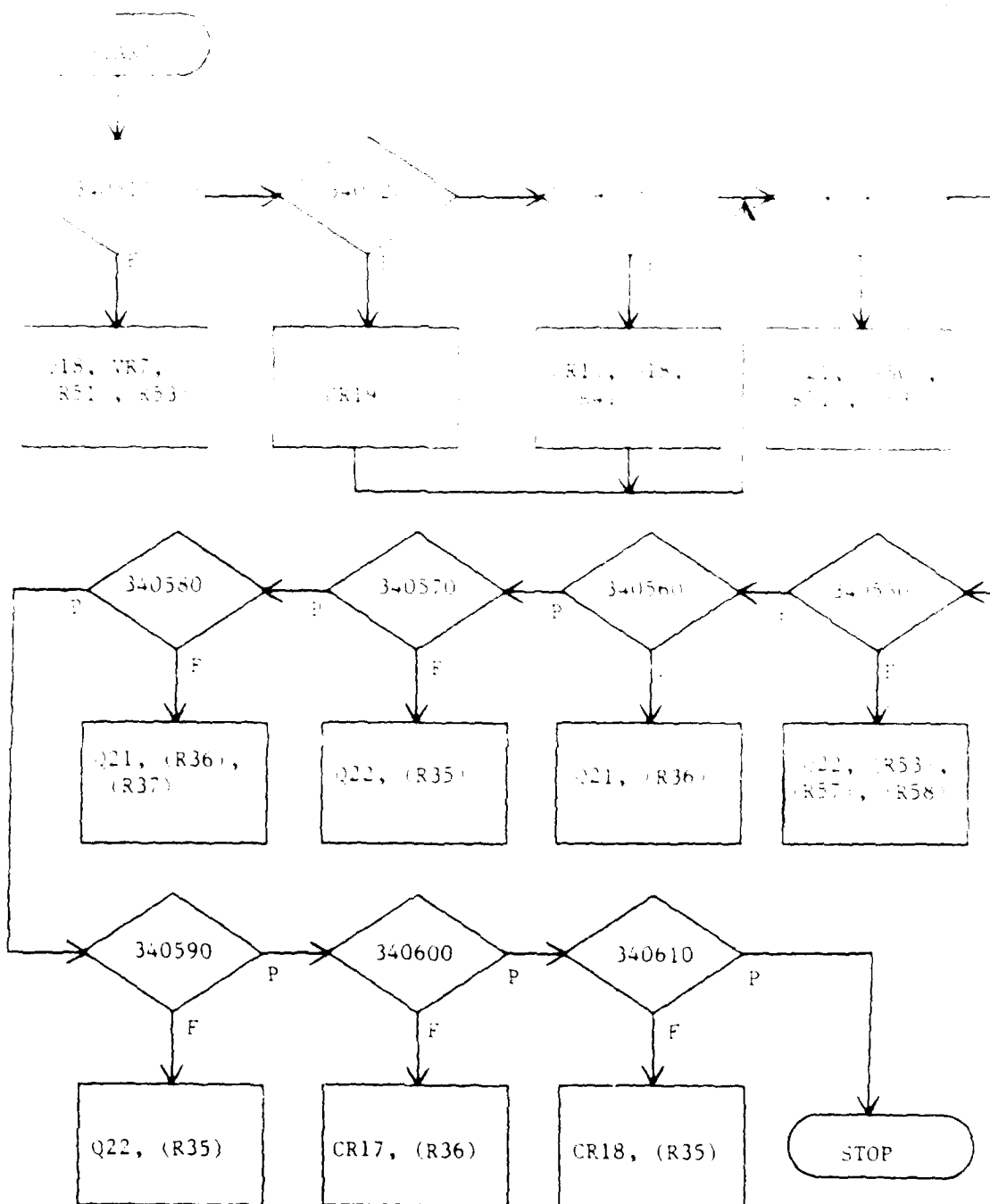


FIGURE 55 - Flip Flop Circuit FI Flowchart

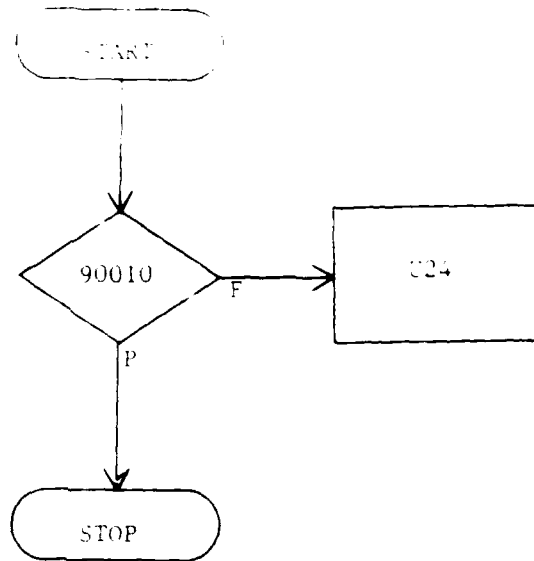


FIGURE 56 - U24 Input Pulse FI Flowchart

APPENDIX F
ACCEPTANCE TEST PROGRAM

```

.....
100
110
120
130
140
150
160
170
180
190
200 !*****
210 !
220 SUSPEND INTERACTIVE, RESET
230 OPTION BASE 1
240 COM /Mass_stor/ System$(16),Test$(16),Data$(16)
250 COM /System_data/ Dept$(4),Co$(4),Te$(10),Dot_d_p,Dot
   _f_p,Pass_word$(10)
260 COM /Board_data/ Bd_no$(15),Rev$(5),Serial$(10),Tps$(
   15),Bd_nm$(20)
270 COM /Test_data/ Run_typ$(5),Awo$(10),Dte$(6),Tme$(5),
   Equip$(17)
280 COM /Softkey/ Hold,No_go,Intermed,Printer,Last_key$(8
   0)
290 COM /Data/ H1,Low,Dat(3,750),Cnt,Repeater
300 COM /Failures/ Bd_p_p,Bad_parts$(100)(6)
310 COM /Variables/ Inter_num,Error_num,Test_Flag
320 COM /Part/ Part$(5,200)(8),INTEGER Pic1(7500),Pic2(75
   00),Pic3(7500),Pic4(7500)
330 COM /Command/ Dvm$(80),Fun$(80),Pul$(80),Pfn$(80),Cnt
   $(80),Scp$(90),Dvs$(80)
340 COM /Supply/ Vlt(6),Crrnt(6),Frr(6),Which$(10)
350 DIM Dummy$(40),Temp2$(24),Temp3$(24)
360 ON ERROR RECOVER 380
370 IF FNSub_check THEN 410
380 LOADSUB ALL FROM "SYS_CONTRL"&System$
390 LOADSUB ALL FROM "TST_CONTRL"&System$
400 LOADSUB ALL FROM "DRIVERS"&System$
410 OFF ERROR
420 CALL Softkey
430 ON KBD ALL CALL Key_stroke
440 ON INTR 7,15 CALL Service

```

```

450 IN INTR 3:15 CALL Service
460 ENABLE INTR 7:2
470 ENABLE INTR 3:2
480
490 -----BEGIN TESTS NOW
500
510 !*****
520 ! CHECK THAT THE RIGHT PATCHBOX IS IN
530 Meas("A98","C98","B99","D99")
540 Relay(5)
550 Dums(4)
560 Fit(FNDumr,900,1100,X1)
570 Meas("-B99","-D99","B100","D100")
580 Dums(4)
590 Fit(FNDumr,900,1100,X2)
600 Meas("-A98","-C98","-B100","-D100")
610 Relay(-5)
620 IF X1 OR X2 THEN
630     Error_num=15
640     LOAD "END_TEST"&System$
650 END IF
660 !*****
670 RESISTANCE MEASUREMENTS SERIES 10000
680 !*****
690 RESTORE 700
700 DATA 10010,18,29,10020,18,28,10030,19,32
710 DATA 10040,20,8,10050,21,12,10060,22,5
720 DATA 10070,43,50,10080,43,38,10090,44,41
730 DATA 10100,45,26,10110,46,40,10120,47,25
740 DATA 10130,36,31,10140,37,1,10150,27,33
750 DATA 10160,9,10
760 Low=0
770 Hi=1
780 FOR N=1 TO 16
790     IF N>=15 THEN
800         Hi=13000
810         Low=11000
820     END IF
830     READ Dat(1,Cnt),A$,B$
840     Stim("M"&A$,"O"&A$,"N"&B$,"P"&B$)
850     Dums(4)
860     Dat(2,Cnt)=FNDumr
870     IF FNTest THEN 840
880     Stim("-M"&A$,"-O"&A$,"-N"&B$,"-P"&B$)
890     IF Dat(3,Cnt-1) THEN
900         Error_num=18
910         LOAD "END_TEST"&System$
920     END IF
930 NEXT N
940 !*****

```

```

950      CURRENT DEMAND SERIES 11100
960      *****
970      Relay(1)
980      Relay(2)
990      Relay(3)
1000     Power_set(1,28,.25,1)
1010     Power_set(2,5,.5,1)
1020     Power_set(3,5,.07,1)
1030     RESTORE 1040
1040     DATA 11010,230,11020,450,11030,60
1050     DATA 27.9,28.1,A31,4.9,5.1,A32,-4.9,-5.1,A33
1060     Low=0
1070     FOR N=1 TO 3
1080         READ Dat(1,Cnt),H1
1090         Dat(2,Cnt)=1000*FNRRd_pwr/N
1100         Dum=FNTest
1110     NEXT N
1120     DVms(1)
1130     Meas("B97")
1140     FOR N=1 TO 3
1150         READ H11,Lol,A$
1160         Meas(A$)
1170         F.t(FNDVmr,H11,Lol,Volts)
1180         IF Volts THEN
1190             Error_num=2
1200             LOAD "END_TEST"&System$
1210         END IF
1220         Meas("-"&A$)
1230     NEXT N
1240     Meas("-B97")
1250     !*****
1260     !PATCHBOX CIRCUIT TEST
1270     !*****
1280     Toggle(-1,-2,-3)
1290     Relay(3)
1300     Toggle(1,2,3)
1310     Stim("Q60","S60","N29")
1320     DVms(1)
1330     Dw("100B")
1340     Pulgen(1,"10MS","1MS",0,5)
1350     Cnts(7,"2.4")
1360     Fit(FNCNtr(3),.5,1.5,X1)
1370     Dw("000B")
1380     Fit(FNCNtr,0,0,X2)
1390     Stim("-Q60","M60")
1400     Fit(FNDVmr,0,.8,X3)
1410     Toggle(-9)
1420     Stim("-M60","-S60","M27")
1430     Relay(6)
1440     Fit(FNDVmr,0,.8,X4)
1450

```

```

1460   Low="1B"
1470   Fit=FNDumr,2.4,5.2,x5
1480   Stim("-M29","N29")
1490   IF X1 OR X2 OR X3 OR X4 OR X5 THEN
1500       Toggle(-1,-2,-3)
1510       Error_num=17
1520       LOAD "END_TEST"&System$
1530   END IF
1540   !*****
1550   ITIM REFERENCE VOLTAGE SERIES 20000
1560   !*****
1570   Dums(1)
1580   Dat(1,Cnt)=20010
1590   H1=0.63
1600   Low=3.57
1610   Stim("M35","N29")
1620   WAIT .5
1630   Dat(2,Cnt)=FNDumr
1640   IF FNTTest THEN 1610
1650   Stim("-M35","N29")
1660   !*****
1670   IAC/DC GAIN TESTS SERIES 21000
1680   !*****
1690   RESTORE 1980
1700   ALLOCATE U_in(1000),U_out(1000)
1710   FOR N=1 TO 12
1720       READ Dat(1,Cnt),H1,Low,Fr$,Am$,P11$,P12$,Po$
1730       Stim("I"&P11$,"J"&P12$)
1740       IF Fr$="0" THEN
1750           Stim("J29")
1760           Fungen(.05,Am$)
1770           Stim("-M"&Po$,"N35","M"&P11$,"N"&P12$)
1780           Uin=FNDumr
1790           Stim("-M"&P11$,"N"&P12$,"M"&Po$,"N35")
1800           Dat(2,Cnt)=FNDumr/Uin
1810           IF FNTTest THEN 1730
1820           Stim("-M"&Po$,"N35","J29")
1830       ELSE
1840           Stim("-M"&Po$,"N35","M"&P11$,"N"&P12$)
1850           Fungen(1.05,Fr$,Am$)
1860           CALL Dum_time("543",1000,1,.002,0,U_in(*))
1870           Uin=FNDumrms(U_in(*))
1880           Stim("-M"&P11$,"N"&P12$,"M"&Po$,"N35")
1890           CALL Dum_time("143",1000,1,.002,0,U_out(*))
1900           Dat(2,Cnt)=FNDumrms(U_out(*))/Uin
1910           IF FNTTest THEN 1730
1920           Stim("-M"&Po$,"N35")
1930       END IF
1940       Toggle(-9)
1950       Stim("-I"&P11$,"J"&P12$)

```

```

1980 NEXT N
1990 DEALLOCATE _110, _120, _130, _140
1990 DATA 21010, .11, .09, 0, 1.5, 1, 1, 34
1990 DATA 21020, .0871, .0575, 1, 1, 1, 2, 34
2000 DATA 21030, .012, .008, 10, 10, 1, 2, 34
2010 DATA 21040, .0817, .0575, 1, 4, 2, 1, 34
2020 DATA 21200, 2.4, 1.6, 0, 1.5, 3, 4, 30
2030 DATA 21210, .32, .211, 1, 4, 4, 3, 30
2040 DATA 21220, .03, .02, 10, 10, 4, 3, 30
2050 DATA 21230, .32, .211, 1, 4, 3, 4, 30
2060 DATA 21400, 2.18, 1.38, 0, 1.5, 6, 7, 34
2070 DATA 21410, .32, .211, 1, 4, 7, 6, 34
2080 DATA 21420, .03, .02, 10, 10, 7, 6, 34
2090 DATA 21430, .32, .211, 1, 4, 6, 7, 34
2100 *****
2110 IOC THRESHOLD TESTS SERIES 21000 CONTINUED
2120 *****
2130 RESTORE 2400
2140 FOR N=1 TO 5
2150   READ Dat(1,Cnt),Hi,Low,Involt,P11$,P12$,P13$,P14$,P15$,P16$,P17$,P18$,P19$,P20$,P21$,P22$,P23$,P24$,P25$,P26$,P27$,P28$,P29$,P30$,P31$,P32$,P33$,P34$,P35$,P36$,P37$,P38$,P39$,P40$,P41$,P42$,P43$,P44$,P45$,P46$,P47$,P48$,P49$,P50$,P51$,P52$,P53$,P54$,P55$,P56$,P57$,P58$,P59$,P60$,P61$,P62$,P63$,P64$,P65$,P66$,P67$,P68$,P69$,P70$,P71$,P72$,P73$,P74$,P75$,P76$,P77$,P78$,P79$,P80$,P81$,P82$,P83$,P84$,P85$,P86$,P87$,P88$,P89$,P90$,P91$,P92$,P93$,P94$,P95$,P96$,P97$,P98$,P99$,P100$,P101$,P102$,P103$,P104$,P105$,P106$,P107$,P108$,P109$,P110$,P111$,P112$,P113$,P114$,P115$,P116$,P117$,P118$,P119$,P120$,P121$,P122$,P123$,P124$,P125$,P126$,P127$,P128$,P129$,P130$,P131$,P132$,P133$,P134$,P135$,P136$,P137$,P138$,P139$,P140$,P141$,P142$,P143$,P144$,P145$,P146$,P147$,P148$,P149$,P150$,P151$,P152$,P153$,P154$,P155$,P156$,P157$,P158$,P159$,P160$,P161$,P162$,P163$,P164$,P165$,P166$,P167$,P168$,P169$,P170$,P171$,P172$,P173$,P174$,P175$,P176$,P177$,P178$,P179$,P180$,P181$,P182$,P183$,P184$,P185$,P186$,P187$,P188$,P189$,P190$,P191$,P192$,P193$,P194$,P195$,P196$,P197$,P198$,P199$,P200$,P201$,P202$,P203$,P204$,P205$,P206$,P207$,P208$,P209$,P210$,P211$,P212$,P213$,P214$,P215$,P216$,P217$,P218$,P219$,P220$,P221$,P222$,P223$,P224$,P225$,P226$,P227$,P228$,P229$,P230$,P231$,P232$,P233$,P234$,P235$,P236$,P237$,P238$,P239$,P240$,P241$,P242$,P243$,P244$,P245$,P246$,P247$,P248$,P249$,P250$,P251$,P252$,P253$,P254$,P255$,P256$,P257$,P258$,P259$,P260$,P261$,P262$,P263$,P264$,P265$,P266$,P267$,P268$,P269$,P270$,P271$,P272$,P273$,P274$,P275$,P276$,P277$,P278$,P279$,P280$,P281$,P282$,P283$,P284$,P285$,P286$,P287$,P288$,P289$,P290$,P291$,P292$,P293$,P294$,P295$,P296$,P297$,P298$,P299$,P300$,P301$,P302$,P303$,P304$,P305$,P306$,P307$,P308$,P309$,P310$,P311$,P312$,P313$,P314$,P315$,P316$,P317$,P318$,P319$,P320$,P321$,P322$,P323$,P324$,P325$,P326$,P327$,P328$,P329$,P330$,P331$,P332$,P333$,P334$,P335$,P336$,P337$,P338$,P339$,P340$,P341$,P342$,P343$,P344$,P345$,P346$,P347$,P348$,P349$,P350$,P351$,P352$,P353$,P354$,P355$,P356$,P357$,P358$,P359$,P360$,P361$,P362$,P363$,P364$,P365$,P366$,P367$,P368$,P369$,P370$,P371$,P372$,P373$,P374$,P375$,P376$,P377$,P378$,P379$,P380$,P381$,P382$,P383$,P384$,P385$,P386$,P387$,P388$,P389$,P390$,P391$,P392$,P393$,P394$,P395$,P396$,P397$,P398$,P399$,P400$,P401$,P402$,P403$,P404$,P405$,P406$,P407$,P408$,P409$,P410$,P411$,P412$,P413$,P414$,P415$,P416$,P417$,P418$,P419$,P420$,P421$,P422$,P423$,P424$,P425$,P426$,P427$,P428$,P429$,P430$,P431$,P432$,P433$,P434$,P435$,P436$,P437$,P438$,P439$,P440$,P441$,P442$,P443$,P444$,P445$,P446$,P447$,P448$,P449$,P450$,P451$,P452$,P453$,P454$,P455$,P456$,P457$,P458$,P459$,P460$,P461$,P462$,P463$,P464$,P465$,P466$,P467$,P468$,P469$,P470$,P471$,P472$,P473$,P474$,P475$,P476$,P477$,P478$,P479$,P480$,P481$,P482$,P483$,P484$,P485$,P486$,P487$,P488$,P489$,P490$,P491$,P492$,P493$,P494$,P495$,P496$,P497$,P498$,P499$,P500$,P501$,P502$,P503$,P504$,P505$,P506$,P507$,P508$,P509$,P510$,P511$,P512$,P513$,P514$,P515$,P516$,P517$,P518$,P519$,P520$,P521$,P522$,P523$,P524$,P525$,P526$,P527$,P528$,P529$,P530$,P531$,P532$,P533$,P534$,P535$,P536$,P537$,P538$,P539$,P540$,P541$,P542$,P543$,P544$,P545$,P546$,P547$,P548$,P549$,P550$,P551$,P552$,P553$,P554$,P555$,P556$,P557$,P558$,P559$,P560$,P561$,P562$,P563$,P564$,P565$,P566$,P567$,P568$,P569$,P570$,P571$,P572$,P573$,P574$,P575$,P576$,P577$,P578$,P579$,P580$,P581$,P582$,P583$,P584$,P585$,P586$,P587$,P588$,P589$,P590$,P591$,P592$,P593$,P594$,P595$,P596$,P597$,P598$,P599$,P600$,P601$,P602$,P603$,P604$,P605$,P606$,P607$,P608$,P609$,P610$,P611$,P612$,P613$,P614$,P615$,P616$,P617$,P618$,P619$,P620$,P621$,P622$,P623$,P624$,P625$,P626$,P627$,P628$,P629$,P630$,P631$,P632$,P633$,P634$,P635$,P636$,P637$,P638$,P639$,P640$,P641$,P642$,P643$,P644$,P645$,P646$,P647$,P648$,P649$,P650$,P651$,P652$,P653$,P654$,P655$,P656$,P657$,P658$,P659$,P660$,P661$,P662$,P663$,P664$,P665$,P666$,P667$,P668$,P669$,P670$,P671$,P672$,P673$,P674$,P675$,P676$,P677$,P678$,P679$,P680$,P681$,P682$,P683$,P684$,P685$,P686$,P687$,P688$,P689$,P690$,P691$,P692$,P693$,P694$,P695$,P696$,P697$,P698$,P699$,P700$,P701$,P702$,P703$,P704$,P705$,P706$,P707$,P708$,P709$,P710$,P711$,P712$,P713$,P714$,P715$,P716$,P717$,P718$,P719$,P720$,P721$,P722$,P723$,P724$,P725$,P726$,P727$,P728$,P729$,P730$,P731$,P732
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3460 *****
3470 Setm("249", "R48")
3480 Tim=1
3490 GOTO 3510
3500 Tim=2
3510 Toggle(-1)
3520 Oc("0")
3530 IF Tim=1 THEN
3540     Start=TIMEDATE
3550     REPEAT
3560         Secs=60-INT((TIMEDATE-Start)/MCD/60)
3570         DISP "" "60 SECOND HOLD" "" :Secs: "seconds to go"
3580     UNTIL TIMEDATE-Start>=61
3590 ELSE BEGIN 330 SECOND WAIT
3600     Start=TIMEDATE
3610     REPEAT
3620         Secs=330-INT((TIMEDATE-Start)/MCD/60)
3630         DISP "" "330 SECOND HOLD" "" :Secs: "seconds to go"
3640     UNTIL TIMEDATE-Start>=331
3650 END IF
3660 Toggle(4,5,9)
3670 Power_set(6,0,.25,1)
3680 Dw("0")
3690 Temp=Intermed
3700 Intermed=0
3710 Oc("1001")
3720 Toggle(1) TURN ON 29 VDC
3730 Start=TIMEDATE
3740 Cnts(10002,".8,.8",11)
3750 REPEAT
3760     Secs=INT((TIMEDATE-Start)/MCD/60)
3770     DISP "300 SECOND TIMER TEST: TIME ELAPSED: Secs:
"seconds"
3780     Dummy$=FNDC$( "8" )
3790     UNTIL NOT VAL(Dummy$(14,14)) OR TIMEDATE-Start>=3
3800     End1=TIMEDATE
3810     End2=FNDCtr
3820     Intermed=Temp
3830     Dat(1,Cnt)=31010
3840     H1=330
3850     Low=300
3860     Dat(2,Cnt)=INT(End1-Start)
3870     IF FNTest THEN 3500
3880     Dat(1,Cnt)=31020
3890     H1=250
3900     Low=150
3910     Dat(2,Cnt)=1000*End2
3920     IF FNTest THEN 3500

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1. The first part of the document is a list of names and addresses, which are arranged in a columnar format. The names are written in a cursive script, and the addresses are written in a more formal, printed style. The list is organized into several groups, with each group separated by a horizontal line.

2. The second part of the document is a series of short, handwritten notes or entries. These are written in a cursive script and are arranged in a columnar format, similar to the first part. The notes appear to be related to the names and addresses listed in the first part.

3. The third part of the document is a series of short, handwritten notes or entries. These are written in a cursive script and are arranged in a columnar format, similar to the second part. The notes appear to be related to the names and addresses listed in the first part.

4. The fourth part of the document is a series of short, handwritten notes or entries. These are written in a cursive script and are arranged in a columnar format, similar to the third part. The notes appear to be related to the names and addresses listed in the first part.

5. The fifth part of the document is a series of short, handwritten notes or entries. These are written in a cursive script and are arranged in a columnar format, similar to the fourth part. The notes appear to be related to the names and addresses listed in the first part.

6. The sixth part of the document is a series of short, handwritten notes or entries. These are written in a cursive script and are arranged in a columnar format, similar to the fifth part. The notes appear to be related to the names and addresses listed in the first part.

7. The seventh part of the document is a series of short, handwritten notes or entries. These are written in a cursive script and are arranged in a columnar format, similar to the sixth part. The notes appear to be related to the names and addresses listed in the first part.

8. The eighth part of the document is a series of short, handwritten notes or entries. These are written in a cursive script and are arranged in a columnar format, similar to the seventh part. The notes appear to be related to the names and addresses listed in the first part.

9. The ninth part of the document is a series of short, handwritten notes or entries. These are written in a cursive script and are arranged in a columnar format, similar to the eighth part. The notes appear to be related to the names and addresses listed in the first part.

10. The tenth part of the document is a series of short, handwritten notes or entries. These are written in a cursive script and are arranged in a columnar format, similar to the ninth part. The notes appear to be related to the names and addresses listed in the first part.

APPENDIX G
FAULT ISOLATION PROGRAM

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950         Error_pum=13
960         LOAD "END_TEST"&System$
970     END IF
980     ---APPLY POWER AND SET CURRENT---
990     DATA 11010,.23,.01,11020,.45,.01,11030,.76,.01
1000     Relay(1)
1010     Relay(2)
1020     Relay(8)
1030     Power_set(1,29,3)
1040     Power_set(2,5,3)
1050     Power_set(3,5,3)
1060     WAIT 2
1070     Flag=0
1080     RESTORE 990
1090     FOR X=1 TO 3
1100         READ Dat(1,Cnt),Hi,Low
1110         Dat(2,Cnt)=FNRead_pwr(X)
1120         IF FNTest THEN Flag=1
1130     NEXT X
1140     IF Flag=1 THEN
1150         PRINT CHR$(12);"ONE OR MORE OF THE POWER SUPPLIES
1160         PRINT "EXCEEDING IT'S CURRENT LIMIT."
1170         PRINT
1180         PRINT "DO YOU WISH TO CONTINUE WITH THE TEST?"
1190         Hun$=FNInput$(40,4)
1200         IF Hun$(1,1)<>"Y" THEN LOAD "END_TEST"&System$
1210     END IF
1220     Toggle(2)
1230     Relay(3)
1240     Toggle(2)
1250     PRINT CHR$(12);"VOLTAGE REGULATOR TEST"
1260     Goon
1270     GOTO T20010
1280
1290 Menu:PRINT CHR$(12)
1300     PRINT "BOARD 5188986 FAULT ISOLATION MENU"
1310     PRINT
1320     PRINT "1) 10010-10160      10) 33010"
1330     PRINT "2) 11010-11030      11) 31010-31020"
1340     PRINT "3) 20010      12) 32010"
1350     PRINT "4) 21010-21040      13) 33010-33020"
1360     PRINT "5) 21050      14) 34010-34040"
1370     PRINT "6) 21200-21230      15) 34050-34100"
1380     PRINT "7) 21240-21270      16) 99010"
1390     PRINT "8) 21400-21430      17) PATCHBOX"
1400     PRINT "9) 21440-21450      18) EXIT"
1410     PRINT
1420     PRINT
1430     PRINT

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1440 PRINT CENTER THE NUMBER FOR THE TEST SERIES.
1450 PRINT "TO RUN:
1460 ON ERROR RECOVER Menu
1470 Sel:=VAL(INPUT$) R,17
1480 OFF ERROR
1490 IF Sel=1 OR Sel=13 THEN Menu
1500 IF Sel=10 THEN 1520
1510 ON Sel GOTO T10000,T11000,T20010,T21100,T21200,T21240,
T21240,T21400,T21440,T30010
1520 ON Sel=10 GOTO T31010,T32010,T33010,T34100,T34100,T34100,
Patchbx,Finished
1530
1540
1550 T10000:PRINT CHR$(12); "Tests 10010-11000 are structural
tests."
1560 PRINT
1570 PRINT "Use the IR AND schematics for board 5138986 to
1580 PRINT "locate any fault."
1590 PRINT
1600 PRINT
1610 PRINT "Replace R162 if test 10150 failed."
1620 PRINT
1630 PRINT "Replace R163 if test 10160 failed."
1640 Goon
1650 GOTO Menu
1660
1670 T11000:PRINT CHR$(12); "Tests 11010-11030 are current de
mand tests"
1680 PRINT
1690 PRINT "Use the schematics for board 5138986 to locate
1700 PRINT "any fault."
1710 Goon
1720 GOTO Menu
1730
1740 T20010:PRINT CHR$(12); "***VOLTAGE REGULATOR***
1750 *****
1760 VOLTAGE REGULATOR TEST SERIES 200100
1770 *****
1780 Dims(1)
1790 Flag=0
1800 Find_it("R148L","RED PROBE",2)
1810 Find_it("R154L","BLACK PROBE",1)
1820 Find_it("R147R","YELLOW PROBE",1)
1830 Find_it("R153R","ORANGE PROBE",1)
1840 Find_it("R151R","GREEN PROBE",1)
1850 Find_it("R150R","BLUE PROBE",3)
1860 RESTORE 1860
1870 DATA 200110,27.58,24.51,A17,200120,26.155,23.348,A17,

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[illegible]

[illegible]

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2810 IF Antest THEN Flag=1
2820 NEXT X
2830 Meas="I3A1"
2840 Toggle=1
2850 Stim1=111,14020,14N351
2860 DEHLLOCATE U_10, U_30, U_40
2870 IF Dat(3,Cnt=4) THEN
2880 Found_bad("U21")
2890 ELSE
2900 IF Dat(3,Cnt=5) THEN
2910 Fit(Dat(2,Cnt=5),Dat(1,Cnt=5),1111,14020,14N351)
2920 IF Tes=3 THEN
2930 Found_bad("U21", "R131", "R132", "R133", "R134")
2940 ELSE
2950 Found_bad("R131", "R132", "R133", "R134")
2960 END IF
2970 ELSE
2980 IF Dat(3,Cnt=6) OR Dat(3,Cnt=7) THEN
2990 Found_bad("R131", "R132", "R133", "R134", "U21")
3000 ELSE
3010 IF Dat(3,Cnt=1) THEN
3020 Found_bad("U14", "U15", "U21")
3030 ELSE
3040 IF Dat(3,Cnt=3) THEN
3050 Found_bad("UR14", "R130")
3060 END IF
3070 END IF
3080 END IF
3090 END IF
3100 END IF
3110 IF Flag THEN T21010
3120 GOTO Menu
3130 T21050:PRINT CHR$(12)
3140 "
3150 "*****
3160 "UBMH COMPARATOR TEST SERIES 21050"
3170 "*****
3180 "
3190 Find_it("U21", "14 PIN CHIP CLIP", 2
3200 Find_it("CR24R", "RED PROBE", 3
3210 Dvms(1)
3220 RESTORE 3220
3230 DATA 210510,27,22,A12,B97,210520,0,0,A1,B7,210530,0,0,
,0,M17,N29,210540,2.4,1.96,A15,B97
3240 DATA 210550,2.35,1.93,A12,B97,210560,5.2,2.4,M17,N29,
210570,-.05,-.05,A1,B10
3250 Meas("A2","B97")
3260 U_a=FNDVmr-.5
3270 Meas("-A2","-B97")
3280 IF U_a=0 THEN U_a=0

```

```

3700  IF C=1 THEN GOTO 3710
3710  IF C=2 THEN GOTO 3720
3720  IF C=3 THEN GOTO 3730
3730  IF C=4 THEN GOTO 3740
3740  IF C=5 THEN GOTO 3750
3750  IF C=6 THEN GOTO 3760
3760  IF C=7 THEN GOTO 3770
3770  IF C=8 THEN GOTO 3780
3780  IF C=9 THEN GOTO 3790
3790  IF C=10 THEN GOTO 3800
3800  IF C=11 THEN GOTO 3810
3810  IF C=12 THEN GOTO 3820
3820  IF C=13 THEN GOTO 3830
3830  IF C=14 THEN GOTO 3840
3840  IF C=15 THEN GOTO 3850
3850  IF C=16 THEN GOTO 3860
3860  IF C=17 THEN GOTO 3870
3870  IF C=18 THEN GOTO 3880
3880  IF C=19 THEN GOTO 3890
3890  IF C=20 THEN GOTO 3900
3900  IF C=21 THEN GOTO 3910
3910  IF C=22 THEN GOTO 3920
3920  IF C=23 THEN GOTO 3930
3930  IF C=24 THEN GOTO 3940
3940  IF C=25 THEN GOTO 3950
3950  IF C=26 THEN GOTO 3960
3960  IF C=27 THEN GOTO 3970
3970  IF C=28 THEN GOTO 3980
3980  IF C=29 THEN GOTO 3990
3990  IF C=30 THEN GOTO 4000
4000  IF C=31 THEN GOTO 4010
4010  IF C=32 THEN GOTO 4020
4020  IF C=33 THEN GOTO 4030
4030  IF C=34 THEN GOTO 4040
4040  IF C=35 THEN GOTO 4050
4050  IF C=36 THEN GOTO 4060
4060  IF C=37 THEN GOTO 4070
4070  IF C=38 THEN GOTO 4080
4080  IF C=39 THEN GOTO 4090
4090  IF C=40 THEN GOTO 4100
4100  IF C=41 THEN GOTO 4110
4110  IF C=42 THEN GOTO 4120
4120  IF C=43 THEN GOTO 4130
4130  IF C=44 THEN GOTO 4140
4140  IF C=45 THEN GOTO 4150
4150  IF C=46 THEN GOTO 4160
4160  IF C=47 THEN GOTO 4170
4170  IF C=48 THEN GOTO 4180
4180  IF C=49 THEN GOTO 4190
4190  IF C=50 THEN GOTO 4200
4200  IF C=51 THEN GOTO 4210
4210  IF C=52 THEN GOTO 4220
4220  IF C=53 THEN GOTO 4230
4230  IF C=54 THEN GOTO 4240
4240  IF C=55 THEN GOTO 4250
4250  IF C=56 THEN GOTO 4260
4260  IF C=57 THEN GOTO 4270
4270  IF C=58 THEN GOTO 4280
4280  IF C=59 THEN GOTO 4290
4290  IF C=60 THEN GOTO 4300
4300  IF C=61 THEN GOTO 4310
4310  IF C=62 THEN GOTO 4320
4320  IF C=63 THEN GOTO 4330
4330  IF C=64 THEN GOTO 4340
4340  IF C=65 THEN GOTO 4350
4350  IF C=66 THEN GOTO 4360
4360  IF C=67 THEN GOTO 4370
4370  IF C=68 THEN GOTO 4380
4380  IF C=69 THEN GOTO 4390
4390  IF C=70 THEN GOTO 4400
4400  IF C=71 THEN GOTO 4410
4410  IF C=72 THEN GOTO 4420
4420  IF C=73 THEN GOTO 4430
4430  IF C=74 THEN GOTO 4440
4440  IF C=75 THEN GOTO 4450
4450  IF C=76 THEN GOTO 4460
4460  IF C=77 THEN GOTO 4470
4470  IF C=78 THEN GOTO 4480
4480  IF C=79 THEN GOTO 4490
4490  IF C=80 THEN GOTO 4500
4500  IF C=81 THEN GOTO 4510
4510  IF C=82 THEN GOTO 4520
4520  IF C=83 THEN GOTO 4530
4530  IF C=84 THEN GOTO 4540
4540  IF C=85 THEN GOTO 4550
4550  IF C=86 THEN GOTO 4560
4560  IF C=87 THEN GOTO 4570
4570  IF C=88 THEN GOTO 4580
4580  IF C=89 THEN GOTO 4590
4590  IF C=90 THEN GOTO 4600
4600  IF C=91 THEN GOTO 4610
4610  IF C=92 THEN GOTO 4620
4620  IF C=93 THEN GOTO 4630
4630  IF C=94 THEN GOTO 4640
4640  IF C=95 THEN GOTO 4650
4650  IF C=96 THEN GOTO 4660
4660  IF C=97 THEN GOTO 4670
4670  IF C=98 THEN GOTO 4680
4680  IF C=99 THEN GOTO 4690
4690  IF C=100 THEN GOTO 4700
4700  IF C=101 THEN GOTO 4710
4710  IF C=102 THEN GOTO 4720
4720  IF C=103 THEN GOTO 4730
4730  IF C=104 THEN GOTO 4740
4740  IF C=105 THEN GOTO 4750
4750  IF C=106 THEN GOTO 4760
4760  IF C=107 THEN GOTO 4770
4770  IF C=108 THEN GOTO 4780
4780  IF C=109 THEN GOTO 4790
4790  IF C=110 THEN GOTO 4800
4800  IF C=111 THEN GOTO 4810
4810  IF C=112 THEN GOTO 4820
4820  IF C=113 THEN GOTO 4830
4830  IF C=114 THEN GOTO 4840
4840  IF C=115 THEN GOTO 4850
4850  IF C=116 THEN GOTO 4860
4860  IF C=117 THEN GOTO 4870
4870  IF C=118 THEN GOTO 4880
4880  IF C=119 THEN GOTO 4890
4890  IF C=120 THEN GOTO 4900
4900  IF C=121 THEN GOTO 4910
4910  IF C=122 THEN GOTO 4920
4920  IF C=123 THEN GOTO 4930
4930  IF C=124 THEN GOTO 4940
4940  IF C=125 THEN GOTO 4950
4950  IF C=126 THEN GOTO 4960
4960  IF C=127 THEN GOTO 4970
4970  IF C=128 THEN GOTO 4980
4980  IF C=129 THEN GOTO 4990
4990  IF C=130 THEN GOTO 5000
5000  IF C=131 THEN GOTO 5010
5010  IF C=132 THEN GOTO 5020
5020  IF C=133 THEN GOTO 5030
5030  IF C=134 THEN GOTO 5040
5040  IF C=135 THEN GOTO 5050
5050  IF C=136 THEN GOTO 5060
5060  IF C=137 THEN GOTO 5070
5070  IF C=138 THEN GOTO 5080
5080  IF C=139 THEN GOTO 5090
5090  IF C=140 THEN GOTO 5100
5100  IF C=141 THEN GOTO 5110
5110  IF C=142 THEN GOTO 5120
5120  IF C=143 THEN GOTO 5130
5130  IF C=144 THEN GOTO 5140
5140  IF C=145 THEN GOTO 5150
5150  IF C=146 THEN GOTO 5160
5160  IF C=147 THEN GOTO 5170
5170  IF C=148 THEN GOTO 5180
5180  IF C=149 THEN GOTO 5190
5190  IF C=150 THEN GOTO 5200
5200  IF C=151 THEN GOTO 5210
5210  IF C=152 THEN GOTO 5220
5220  IF C=153 THEN GOTO 5230
5230  IF C=154 THEN GOTO 5240
5240  IF C=155 THEN GOTO 5250
5250  IF C=156 THEN GOTO 5260
5260  IF C=157 THEN GOTO 5270
5270  IF C=158 THEN GOTO 5280
5280  IF C=159 THEN GOTO 5290
5290  IF C=160 THEN GOTO 5300
5300  IF C=161 THEN GOTO 5310
5310  IF C=162 THEN GOTO 5320
5320  IF C=163 THEN GOTO 5330
5330  IF C=164 THEN GOTO 5340
5340  IF C=165 THEN GOTO 5350
5350  IF C=166 THEN GOTO 5360
5360  IF C=167 THEN GOTO 5370
5370  IF C=168 THEN GOTO 5380
5380  IF C=169 THEN GOTO 5390
5390  IF C=170 THEN GOTO 5400
5400  IF C=171 THEN GOTO 5410
5410  IF C=172 THEN GOTO 5420
5420  IF C=173 THEN GOTO 5430
5430  IF C=174 THEN GOTO 5440
5440  IF C=175 THEN GOTO 5450
5450  IF C=176 THEN GOTO 5460
5460  IF C=177 THEN GOTO 5470
5470  IF C=178 THEN GOTO 5480
5480  IF C=179 THEN GOTO 5490
5490  IF C=180 THEN GOTO 5500
5500  IF C=181 THEN GOTO 5510
5510  IF C=182 THEN GOTO 5520
5520  IF C=183 THEN GOTO 5530
5530  IF C=184 THEN GOTO 5540
5540  IF C=185 THEN GOTO 5550
5550  IF C=186 THEN GOTO 5560
5560  IF C=187 THEN GOTO 5570
5570  IF C=188 THEN GOTO 5580
5580  IF C=189 THEN GOTO 5590
5590  IF C=190 THEN GOTO 5600
5600  IF C=191 THEN GOTO 5610
5610  IF C=192 THEN GOTO 5620
5620  IF C=193 THEN GOTO 5630
5630  IF C=194 THEN GOTO 5640
5640  IF C=195 THEN GOTO 5650
5650  IF C=196 THEN GOTO 5660
5660  IF C=197 THEN GOTO 5670
5670  IF C=198 THEN GOTO 5680
5680  IF C=199 THEN GOTO 5690
5690  IF C=200 THEN GOTO 5700
5700  IF C=201 THEN GOTO 5710
5710  IF C=202 THEN GOTO 5720
5720  IF C=203 THEN GOTO 5730
5730  IF C=204 THEN GOTO 5740
5740  IF C=205 THEN GOTO 5750
5750  IF C=206 THEN GOTO 5760
5760  IF C=207 THEN GOTO 5770
5770  IF C=208 THEN GOTO 5780
5780  IF C=209 THEN GOTO 5790
5790  IF C=210 THEN GOTO 5800
5
```



```

4260 IF Dat(3,Cnt)=1 THEN
4270   Fit_Dat(1,Cnt)=Dat(1,Cnt)
4280   IF Test=3 THEN
4290     Found_bad="U20",R115
4300   ELSE
4310     Found_bad="R122",R123
4320   END IF
4330 ELSE
4340   IF Dat(3,Cnt)=2 IF Dat(3,Cnt)=1 THEN
4350     Found_bad="R120",R121
4360   ELSE
4370     IF Dat(3,Cnt)=1 THEN
4380       Found_bad="D121",D12
4390     ELSE
4400       IF Dat(3,Cnt)=3 THEN
4410         Found_bad="R131",R114
4420       END IF
4430     END IF
4440   END IF
4450 END IF
4460 END IF
4470 IF Flag THEN T21200
4480 GOTO Menu
4490 T21240:PRINT CHR$(12)
4500 !
4510 !*****
4520 !IFKL COMPARATOR TEST          SERIES 21240
4530 !*****
4540 !
4550 Find_it("U20","14 PIN CHIP CLIP",2
4560 Find_it("CR24R","RED PROBE",1
4570 Find_it("R115C","BLACK PROBE",1
4580 Find_it("R116F","YELLOW PROBE",3
4590 Dums(1)
4600 Meas("A2","B97")
4610 U_a=FNDUmr-.5
4620 Meas("-A2","-B97")
4630 IF U_a<0 THEN U_a=0
4640 Stim("I53","J29")
4650 Fungen(0,VAL$(U_a))
4660 RESTORE 4600
4670 DATA 212410,27,22,A12,B97,212420,0,0,A1,B- ,212430,1.15
,0,M16,N29,212440,2.4,1.96,A15,B97
4680 DATA 212450,2.35,1.93,A12,B97,212460,5.1,2.4,M16,N29,
212470,.05,-.05,A1,B10
4690 Flag=0
4700 FOR X=1 TO 7
4710   READ Dat(1,Cnt),Hi,Low,A$,B$
4720   IF X<>3 OR X<>6 THEN CALL Meas A$,B$
4730   IF X=3 OR X=6 THEN CALL Stim A$,B$

```

[illegible]

```

5270
5280 *****
5290 DATA COMPARATOR TEST          SERIES 212500
5300 *****
5310
5320 Find_U22("U22","14 PIN CHIP CLIP")
5330 RESTORE 5290
5340 DATA 212510,19,17,A1,B97,212520,27,22,A12,B97,212530,
5350 13,0,M11,N29,212540,2.4,1.96,A15,B97
5360 DATA 212550,2.35,1.93,A12,B97,212560,5.2,2.4,M11,N29,
5370 212570,0,0,A2,B97
5380 Stim("154","J29")
5390 Flag=0
5400 FOR X=1 TO 7
5410 READ Dat(1,Cnt),Hi,Low,A$,B$
5420 IF X=7 THEN
5430 Toggle(-9)
5440 Stim("-154","-J29")
5450 Meas("A12","B97")
5460 Uo=FNDUmr
5470 Meas("-A12","A17")
5480 U1=FNDUmr
5490 Meas("-A17","-B97")
5500 Cor=INT(1000*(Uo+U1*180)/181+.5)/1000
5510 Hi=1.1*Cor
5520 Low=.9*Cor
5530 END IF
5540 IF X<>3 OR X<>6 THEN CALL Meas(A$,B$)
5550 IF X=3 OR X=6 THEN CALL Stim(A$,B$)
5560 IF X=2 THEN CALL Fungen(0,VAL$(U_a))
5570 IF X=5 THEN CALL Fungen(0,VAL$(U_a-1))
5580 Dat(2,Cnt)=FNDUmr
5590 IF FNTest THEN Flag=1
5600 IF X=3 OR X=6 THEN CALL Stim("-&A$","-&B$")
5610 IF X<>3 OR X<>6 THEN CALL Meas("-&A$","-&B$")
5620 IF X=1 THEN
5630 Meas("A16","B97")
5640 Volt1a=FNDUmr
5650 Meas("-A16","-B97")
5660 U_a=Dat(2,Cnt-1)+.5
5670 IF U_a>20 THEN U_a=20
5680 END IF
5690 NEXT X
5700 IF Dat(3,Cnt-7) THEN
5710 Fit(Volt1a,17,19,Test1a)
5720 IF Test1a THEN
5730 Found_bad("UR17","(R175)")
5740 ELSE
5750 Found_bad("U22","(R115)")
5760 END IF

```

```

5720 ELSE
5730 IF Dat(3,Cnt=6) OR Dat(3,Cnt=7) THEN
5740 Found_bad("U22","R114")
5750 ELSE
5760 IF Dat(3,Cnt=4) THEN
5770 Found_bad("Q34","Q37","R114","CR3")
5780 ELSE
5790 IF Dat(3,Cnt=3) OR Dat(3,Cnt=5) THEN
5800 Found_bad("Q37","R114")
5810 ELSE
5820 IF Dat(3,Cnt=1) THEN
5830 Found_bad("R116","R117","")
5840 END IF
5850 END IF
5860 END IF
5870 END IF
5880 IF Flag THEN 5280
5890 GOTO Menu
5900 T21400:PRINT CHR$(12)
5910
5920
5930 IFMT OP AMP TEST SERIES 21400
5940
5950
5960 ALLOCATE U_in(1000),U_out(1000)
5970 Dims(1)
5980 Find_it("U22","14 PIN CHIP CLIP")
5990 RESTORE 5990
6000 DATA 214010,10.50,8.59,A10,B97,214020,3.78,3.09,A6,B9
7,214030,.01,-.01,A7,B6
6010 DATA 214040,.05,-.05,B10,M39,214050,14.42,11.50,A10,B
97,214060,.0297,.0243,A10,B97
6020 Stim("I6","J29","T2")
6030 Fungen(.05,"2.50")
6040 WAIT 7
6050 Flag=0
6060 FOR X=1 TO 6
6070 READ Dat(1,Cnt),Hi,Low,A$,B$
6080 IF X<6 THEN
6090 IF X<>4 THEN CALL Meas(H$,B$)
6100 IF X=4 THEN
6110 Meas(A$)
6120 Stim(B$)
6130 END IF
6140 IF X=5 THEN
6150 Stim("-T2","B7","L29")
6160 Dims("-2")
6170 WAIT 7

```

```

6180     END IF
6190     Dat(2),Cnt =FNDCvms
6200     Meas = "R3A$,"R3B$
6210     IF X=4 THEN CALL Strm = 321
6220 ELSE
6230     Toggle = 9,-10
6240     Strm = "B7", "C229", "C229", -15
6250     Strm = "I7", "M7", "C6", "No
6260     Fungen = 1,05, "10", "50"
6270     CALL Com_time = 12.5+3, 1000, 1, 1000, 0, _10 *
6280     Cnt = FNDCvms + 2, 10 *
6290     Strm = "M7", "No", "N35"
6300     Meas = A$
6310     CALL Com_time = 12.3, 1000, 1, 1000, 0, _10 *
6320     Dat(2),Cnt = FNDCvms + 2, 10 *
6330 END IF
6340 IF FNTest THEN Flag = 1
6350 NEXT X
6360 Meas = "R3A$,"
6370 Toggle = 9
6380 Strm = "I7", "C6", "N35"
6390 DEHLDDATE 2, 10 * , 1, 1000 *
6400 IF Dat(3),Cnt = 4 THEN
6410     Found_bad("C22")
6420 ELSE
6430     IF Dat(3),Cnt = 5 THEN
6440         Fit(Dat(2),Cnt = Dat(2),Cnt = 5, 3, 053, 1, 5, 1, Test8
6450         IF Test8 THEN
6460             Found_bad("C22", "R105", "R106", "C11")
6470         ELSE
6480             Found_bad("R107", "R108", "C11", "C11")
6490         END IF
6500     ELSE
6510         IF Dat(3),Cnt = 6 OR Dat(3),Cnt = 7 THEN
6520             Found_bad("R105", "R106", "C11", "C11")
6530         ELSE
6540             IF Dat(3),Cnt = 10 THEN
6550                 Found_bad("C10", "C11", "C22")
6560             ELSE
6570                 IF Dat(3),Cnt = 3 THEN
6580                     Found_bad("R107", "R108")
6590                 END IF
6600             END IF
6610         END IF
6620     END IF
6630 END IF
6640 IF Flag THEN T21400
6650 GOTO Menu
6660 T21400:PRINT CHR$(12)

```

[illegible]

```

7235      IF Dat(1,Cnt)=1 THEN Found_bad=1 ELSE
7236      ELSE
7237      IF Dat(3,Cnt)=1 THEN
7238      Found_bad=1 ELSE
7239      END IF
7240      END IF
7241      END IF
7242      END IF
7243      IF Flag THEN 721440
7244
7245      *****
7246      FMH COMPARATOR TEST          SERIES 214500
7247      *****
7248
7249      RESTORE 7320
7250      DATA 214510,10.7,9.7,A7,B97,214520,27.22,A10,B97,2145
7251      30,.9,0,M15,N29,214540,2.4,1.96,A15,B97
7252      DATA 214550,2.35,1.93,A10,B97,214560,5.2,2.4,M15,N29,
7253      214570,0,0,A6,B97
7254      Stim("I55","J29")
7255      Flag=0
7256      FOR x=1 TO 7
7257      READ Dat(1,Cnt),Hi,Low,A$,B$
7258      IF x=7 THEN
7259      Toggle(-9)
7260      Stim("-I55","-J29")
7261      Meas("A10","B97")
7262      Uo=FNDvmr
7263      Meas("-A10","A17")
7264      U1=FNDvmr
7265      Meas("-A17","-B97")
7266      Cor=INT(1000*(Uo+U1*200)/201+.5)/1000
7267      Hi=1.1*Cor
7268      Low=.9*Cor
7269      END IF
7270      IF x<>3 OR x<>6 THEN CALL Meas(A$,B$)
7271      IF x=3 OR x=6 THEN CALL Stim(A$,B$)
7272      IF x=2 THEN CALL Fungen(0,VAL$(U_a))
7273      IF x=5 THEN CALL Fungen(0,VAL$(U_a-1))
7274      Dat(2,Cnt)=FNDvmr
7275      IF FTest THEN Flag=1
7276      IF x=3 OR x=6 THEN CALL Stim("-"&A$,"-&B$")
7277      IF x<>3 OR x<>6 THEN CALL Meas("-"&A$,"-&B$")
7278      IF x=1 THEN
7279      U_a=Dat(2,Cnt-1)+.5
7280      IF U_a>20 THEN U_a=20

```

```

7870     ELSE
7871         IF Dat(1,Cnt)=1 THEN
7872             Found_bad=127, 128, 129
7873         ELSE
7874             IF Dat(1,Cnt)=6 OR Dat(1,Cnt)=7 THEN
7875                 Found_bad=127, 128
7876             ELSE
7877                 IF Dat(1,Cnt)=4 THEN
7878                     Found_bad=134, 135, 136, 137, 138, 139, 140
7879                 ELSE
7880                     IF Dat(1,Cnt)=2 OR Dat(1,Cnt)=3 THEN
7881                         Found_bad=138, 139
7882                     ELSE
7883                         IF Dat(1,Cnt)=1 THEN
7884                             Found_bad=R101, R102, Q23
7885                         END IF
7886                     END IF
7887                 END IF
7888             END IF
7889         END IF
7890     END IF
7891     IF Flag THEN 7330
7892     GOTO Menu
7893 T30010:PRINT CHR$(12)
7894
7895 *****
7896 FULL POWER CDC AND FPD LOGIC SERIES 300100
7897 *****
7898
7899 Flag=0
7900 Find_it(R52F,"RED PROBE",1)
7901 Find_it(R55F,"BLACK PROBE",1)
7902 Find_it(R59C,"YELLOW PROBE",1)
7903 Find_it(R61C,"ORANGE PROBE",1)
7904 RESTORE 7920
7905 DATA R52F,R56,R55F,R64,Q26,Q25,P1-41
7906 DATA 300110,1.39,1.13,A15,300120,.9,.7,A16,300130,0,0
7907 ,0,300140,1,1,0
7908 DATA R59C,R60,R61C,R64,Q23,Q24,P2-16
7909 DATA 300150,1.39,1.13,A17,300160,.9,.7,A18,300170,0,0
7910 ,0,300180,1,1,0
7911 Dims(1)
7912 Dc("01B")
7913 Meas("B97")
7914 FOR N=1 TO 2
7915     READ R1$,R2$,R3$,R4$,Q1$,Q2$,P2$
7916     FOR X=1 TO 4
7917         READ Dat(1,Cnt),Hi,Low,A$
7918         IF X=4 AND N=1 THEN CALL Toggle(-2)

```

```

8090      IF X=4 AND N=1 THEN CALL T31010
8100      IF X=3 THEN
8110          Meas1A$=
8120          Dat(2,Cnt)=FNDVmr
8130          Meas1A$&A$)
8140      ELSE
8150          Bit$=FNDn$("B")
8160          Dat(2,Cnt)=VAL(Bit$(8+N,3+N))
8170      END IF
8180      IF FNTTest THEN Flag=1
8190      IF N=1 AND X=4 THEN CALL Toggle(2)
8200  NEXT X
8210      IF Dat(3,Cnt-4) THEN
8220          Found_bad(Q1$,"(" & R1$(1,3) & ")")
8230      ELSE
8240          IF Dat(3,Cnt-3) THEN
8250              IF Dat(2,Cnt-3) < .7 THEN
8260                  Found_bad(Q2$,"(" & R2$(1,3) & ")")
8270              ELSE
8280                  Found_bad(Q1$,"(" & R3$(1,3) & ")")
8290              Found_bad(Q2$,"(" & R4$(1,3) & ")")
8300          END IF
8310      ELSE
8320          IF Dat(3,Cnt-2) THEN
8330              Found_bad(Q2$)
8340          ELSE
8350              IF Dat(3,Cnt-1) THEN
8360                  Found_bad(Q1$,Q2$,"(" & R4$(1,3) & ")")
8370              ELSE
8380                  Found_bad(Q1$,Q2$,"(" & R3$(1,3) & ")")
8390              END IF
8400          END IF
8410      END IF
8420  NEXT N
8430  IF Flag THEN T30010
8440  GOTO Menu
8450  T31010:PRINT CHR$(12)
8460  !*****
8470  !      5 MINUTE AND 250 MSEC TIMER TEST
8480  !*****
8490  GOSUB U1_timer
8500  GOSUB P2_11_35
8510  GOSUB Q7_q8
8520  GOSUB U2_timer
8530  GOTO Menu
8540  T32010:PRINT CHR$(12)
8550  !*****
8560  !      20 SECOND TIMER TEST
8570  !*****

```

```

8670
8680 GOSUB U3_timer
8690 GOSUB P2_12
8700 GOTO Menu
8710 T33010:PRINT CHR$(12)
8720
8730
8740 1.5 SECOND TIMER TEST
8750
8760
8770
8780 GOSUB U1_timer
8790 GOSUB P2_11_35
8800 GOSUB U7_q8
8810 GOSUB U25_timer
8820 GOTO Menu
8830 T34010:PRINT CHR$(12)
8840
8850
8860 POWER ON SEQUENCE LOGIC TEST SERIES 34000
8870
8880
8890 Stim("C2","D1","E3","T1","T4")
8900 Stim("I6","O2","G52")
8910 Stim("S13")
8920 Power_set(4,9,.5,1)
8930 Power_set(5,2,.5,1)
8940 Fungen(0,"1.30")
8950 Power_set(6,0,.25,1)
8960 Pulgen(151,"20US","800NS",0,5.0,"925","10NS","10NS")
8970 Pulfun(13,"1.46HZ","14V","0V","50%")
8980 RESTORE 9260
8990 Relay(6)
9000 Dums(1)
9010 Stim("N29","T24")
9020 FOR X=1 TO 4
9030 Inttemp=Intermed
9040 READ Dat(1,Cnt),L1$,L2$,L3$,H1
9050 Low=H1
9060 Stim("-M58","M33")
9070 Dw("10"&L1$&"B")
9080 Dc(L2$&"00"&L3$)
9090 IF X=4 THEN CALL Power_set(6,28,.25,1)
9100 WAIT 2
9110 Intermed=0
9120 Temp2$=FNDns("B")
9130 Temp2$=Temp2$(12,24)
9140 Fit(FNDumr,-.1,2.4,P2_19)
9150 Temp2$=Temp2$&VAL$(P2_19)
9160 Stim("-M33","M42")
9170 Fit(FNDumr,-.1,2.4,Tp2_7)
9180 Temp2$(12,12)=VAL$(Tp2_7)

```

```

9100      Temp2$=DUAL(Temp1$)
9110      Temp2$=VAL(TEMP2$)
9120      Intermed=Int(Temp2$)
9130      IF Intermed THEN PRINT "TEST 1: 1:1:Temp2$
9140      Temp=DUAL(Temp2$,2)
9150      Dat(2,Cnt)=VAL(DUAL$Temp,3)
9160      Dum=FNTest
9170      Temp2$=""
9180      IF Dat(3,Cnt-1) THEN
9190          GOSUB Which_One
9200          GOTO 9300
9210      END IF
9220  NEXT X
9230  Toggle(-4,-5,-6,-7,-8,-9)
9240  Stim("C2","D1","E3","T1","T4")
9250  Stim("I6","J7","G52")
9260  Stim("M42","N29","T24","S13")
9270  Dw("0")
9280  DATA 34010,0,1,0,37476
9290  DATA 34020,1,1,0,37477
9300  DATA 34030,0,0,0,37476
9310  DATA 34040,0,1,0,37476
9320  GOTO Menu
9330  T34050:PRINT CHR$(12)
9340  !
9350  !*****
9360  !POWER ON SEQUENCE LOGIC TEST   SERIES 34000
9370  !*****
9380  !
9390  Find_It("C3R","RED PROBE")
9400  Stim("S13")
9410  Stim("C2","D1","E3","T1","T4")
9420  Stim("I6","J7","G52")
9430  Relay(6)
9440  Power_set(4,9,.5,1)
9450  Power_set(5,2,.5,1)
9460  Fungen(0,"1.30")
9470  Pulgen(151,"20US","800NS",0,5.0,"925","10NS","10NS")
9480  Pulfun(13,"1.46HZ","140","00","50%")
9490  Oc("1000")
9500  Oc("1001")
9510  Stim("B60","L29","F60","H56")
9520  Decade("500")
9530  Dvs("12")
9540  WAIT 1
9550  Stim("-B60","-L29","-F60","-H56")
9560  Toggle(-10)
9570  DISP "TIMER HOLD, PLEASE WAIT."
9580  WAIT 30

```

```

9570 DISP ""
9580 RESTORE 10010
9590 Dims(1)
9600 Stim("N29", "T24")
9610 FOR X=5 TO 10
9620   Intemp=Intermed
9630   READ Dat(1,Cnt),L1$,L2$,L3$,L4,H1
9640   Low=H1
9650   Stim("-M58","M33")
9660   Dw("10"&L1$&"B")
9670   Oc(L2$&"00"&L3$)
9680   Power_set(6,L4,.25,1)
9690   Intermed=0
9700   IF X=9 THEN
9710     Stim("-T24")
9720     Oc("1000B")
9730     Oc("1001B")
9740     Temp3$=FNDrs("B")
9750     Toggle(-7,-8)
9760     Start=TIMEDATE
9770     REPEAT
9780       DISP "TIMER HOLD:"; " TIME ELAPSED IS:";INTAT
IMEDATE-Start)
9790       Dummy$=FNDrs("B")
9800       UNTIL NOT VAL(Dummy$[14,14])
9810       DISP ""
9820     END IF
9830   IF X=10 THEN CALL Stim("T24")
9840   WAIT 2
9850   Temp2$=FNDrs("B")
9860   Temp2$=Temp2$[12,24]
9870   Fit(FNDvnr,-.1,2.4,P2_19)
9880   Temp2$=Temp2$&VAL$(P2_19)
9890   Stim("-M33","M42")
9900   Fit(FNDvnr,-.1,2.4,Tp2_7)
9910   Temp2$[12,12]=VAL$(Tp2_7)
9920   Stim("-M42","M58")
9930   Fit(FNDvnr,-.1,2.4,P2_37)
9940   Temp2$[11,11]=VAL$(P2_37)
9950   Intermed=Intemp
9960   IF X=9 OR X=10 THEN
9970     Temp2$[7,7]=Temp3$[13,13]
9980     Temp2$[8,8]=Temp3$[19,19]
9990     Temp2$[9,9]=Temp3$[20,20]
10000    Temp2$[10,10]=Temp3$[21,21]
10010   END IF
10020   IF Intermed THEN PRINT "TEST":X:":":Temp2$
10030   Temp=DVAL(Temp2$,2)
10040   Dat(2,Cnt)=VAL(DVAL$(Temp,3))
10050   Dum=FNTst

```

```

10105         FndCt1=
10106         IF Dat(3,Cnt1)=FNDEN
10107             Toggle=4,-6,-8,-7,-6,-7
10108             RelA=-6
10109             X=FNDMatch
10110             GOSUB Which_Pone
10111             GOTO Menu
10112     END IF
10113 NEXT X
10114 Toggle=4,-6,-8,-7,-6,-7
10115 Stim1="Q2",1-Q17,1-E3,1-T1,1-T4,1
10116 Stim2="Q1",1-Q7,1-S13,1
10117 Stim3="M2",1-N29,1-G52,1
10118 Dwr=100B
10119 Relay=6
10120 DATA 34050,0,1,1,0,300
10121 DATA 34060,1,1,1,0,36361
10122 DATA 34070,0,1,1,28,32760
10123 DATA 34080,0,0,1,0,1216
10124 DATA 34090,0,1,1,0,2
10125 DATA 34100,0,1,1,0,0
10126 GOTO Menu
10127 T90010: PRINT CHR$(12);"024 PULSE TRAIN INPUT TEST"
10128
10129 *****
10130 PULSE TRAIN INPUT TEST                SERIES 90010
10131 *****
10132
10133 Stim("S13","Q13")
10134 Pulgen(151,"20US","800NS",0,5.0,"925","10NS","10NS")
10135 PulFun(13,"1.46HZ","140","90","50%")
10136 Dwr=100B
10137 Cnts(7,"2.4",1)
10138 Dat(1,Cnt)=90010
10139 H1=2.2E-5
10140 Low=1.5E-5
10141 Dat(2,Cnt)=FNContr
10142 Stim("S13","Q13")
10143 IF FNTest THEN T90010
10144 IF Dat(3,Cnt)=1 THEN CALL Found_bad("024")
10145 GOTO Menu
10146 Patchbx:PRINT CHR$(12);"PATCHBOX TEST"
10147
10148 *****
10149 PATCHBOX ADAPTER TEST
10150 *****
10151
10152 Stim("Q60","S60","N29")
10153 Dwr=100B
10154 Dwr=100B
10155

```



```

11060 IF X=1 THEN
11070   Do(1)
11080   Meas(A13,A14,A15)
11090   WAIT 5
11100   Meas(A13,A14,A15)
11110   WAIT 5
11120   Meas(A5,B5)
11130   IF X=5 THEN
11140     Do(11)
11150     Temp=Intermed
11160     Intermed=0
11170     Start=TIMEDATE
11180     REPEAT
11190       Secs=INT (TIMEDATE-Start)
11200       DISP "300 SECOND TIMER TEST:  TIME ELAPSED:
;Secs;"seconds"
11210       Volt5=FNDVmr
11220       UNTIL Volt5<.5 OR TIMEDATE-Start<30
11230       Dat(2,Cnt)=INT(TIMEDATE-Start)
11240       IF Volt5>.5 THEN No_switch=1
11250       Intermed=Temp
11260     ELSE
11270       Dat(2,Cnt)=FNDVmr
11280     END IF
11290   IF FNTTest THEN Flag=1
11300   Meas(A1,A5,A6,B1,B5,B6)
11310 NEXT X
11320 Stim("F56","H57")
11330 IF Dat(3,Cnt-2) THEN
11340   Found_bad("Q5","R6","R2")
11350   Subber=1
11360 ELSE
11370   IF Dat(3,Cnt-6) THEN
11380     Found_bad("CR1","CR2")
11390     Subber=1
11400   ELSE
11410     IF Dat(3,Cnt-5) THEN
11420       Found_bad("CR3","CR4")
11430       Subber=1
11440     ELSE
11450       IF Dat(3,Cnt-4) THEN
11460         Found_bad("Q1","Q5")
11470         Subber=1
11480       ELSE
11490         IF Dat(3,Cnt-3) THEN
11500           IF NOT No_switch THEN
11510             GOTO Tailor
11520           ELSE
11530             IF Dat(3,Cnt-2) THEN

```



```

12090 Toggle=1,2,3
12100 PRINT CHR$(12):"THE TIMING FOR THIS CIRCUIT IS OFF SL
12110
12120 PRINT "THE TIMING RESISTOR (R3) MUST BE TAILORED."
12130 PRINT
12140 PRINT "CLIP THE RIGHT SIDE OF THE RESISTOR R3 WHICH"
12150 PRINT "NOW HAS THE PURPLE PROBE CONNECTED TO IT."
12160 PRINT "LEAVE AS MUCH LEAD ON THE RESISTOR AS POSSIBLE
12170
12180 PRINT "AND ALSO LEAVE THE PURPLE PROBE ATTACHED TO TH
12190
12200 PRINT "CLIPPED END."
12210 Goto
12220 Toggle=1,2,3
12230 Meas="A22","C22","B16","D16")
12240 Relay(5)
12250 OCmds(4)
12260 R3_old=FNDcmr
12270 PRINT
12280 PRINT "THE RESISTANCE OF THE PRESENT R3 IS: ";R3_old
12290 R3_new=315/Dat(2,Cnt-3)*(6.8E+6+R3_old)-6.8E+6
12300 Meas="A22","C22","B16","D16")
12310 Relay(-5)
12320 PRINT "A NEW RESISTANCE OF ";ROUND(R3_new,6); " WILL
NOW BE TRIED."
12330 WAIT 5
12340 IF R3_new>560000 THEN
12350     Minum=300/Dat(2,Cnt-3)*(6.8E+6+R3_old)-6.8E+6
12360     IF Minum<560000 THEN
12370         R3_new=560000
12380     ELSE
12390         GOTO Toobad
12400     END IF
12410 END IF
12420 IF R3_new<10000 THEN
12430     Maximum=330/Dat(2,Cnt-3)*(6.8E+6+R3_old)-6.8E+6
12440     IF Maximum>10000 THEN
12450         R3_new=10000
12460     ELSE
12470         GOTO Toobad
12480     END IF
12490 END IF
12500 St.m=5600,14500)
12510 Decade=VAL$(R3_new)
12520 RESTORE 10960
12530 Tailored=1
12540 GOTO 10930
12550 Toobad:
12560 Found_bad("R1","R3","R4","R3","R5")
12570 GOTO Menu

```

```

12440
12450 J2_timer:
12460
12470 *****
12480 U2 TIMER TEST                      SERIES 310400
12490 *****
12500
12510 Flag=0
12520 Subber=0
12530 Dums(1)
12540 Dc("1")
12550 Find_it("R14C","GREEN_PROBE",2)
12560 Find_it("R11R","BLACK_PROBE",1)
12570 Find_it("R12R","YELLOW_PROBE",1)
12580 Find_it("R9L","ORANGE_PROBE",1)
12590 Find_it("R10L","BLUE_PROBE",1)
12600 Find_it("C3R","RED_PROBE",3)
12610 RESTORE 12610
12620 DATA 310410,8.25,6.75,A19,310420,.05,0,A16,310430,.95
, .55,A17
12630 DATA 310440,5.2,2.4,M48,310450,.25,0,A18,310460,.25,.
15,M48
12640 DATA 310470,.1,0,A20,310480,15.5,12,A17
12650 Meas("B97")
12660 No_switch=0
12670 FOR X=1 TO 8
12680     READ Dat(1,Cnt),Hi,Low,AS
12690     IF X=4 THEN CALL Stim(AS)
12700     IF X<>4 AND X<>6 THEN CALL Meas(AS)
12710     IF X<>6 THEN
12720         Dat(2,Cnt)=FNDumr
12730     ELSE
12740         Stim("Q49","R48","T52")
12750         Stim("E60","F60","H56")
12760         Decade("500")
12770         Power_set(5,12.1)
12780         WAIT .5
12790         Toggle(-5)
12800         Stim("-E60","-F60","-H56")
12810         Cnts(10002,".8,.8",11) TIME A 0 B
12820         Stim("T27")
12830         Dat(2,Cnt)=FNChtr
12840         IF Dat(2,Cnt)=0 THEN No_switch=1
12850     END IF
12860     IF FNTest THEN Flag=1
12870     IF X=4 THEN CALL Stim("-AS")
12880     IF X<>4 AND X<>6 THEN CALL Meas("-AS")
12890 NEXT X
12900 Stim("-Q49","-R48","-T27","-T52")
12910 IF Dat(3,Cnt=8) THEN

```

```

12920 Found_bad("U2","Q4","(R15)")
12930 Subber=1
12940 ELSE
12950 IF Dat(3,Cnt-7) THEN
12960 Found_bad("U2","Q4","(R15)")
12970 Subber=1
12980 ELSE
12990 IF Dat(3,Cnt-6) THEN
13000 Found_bad("U2","CR7")
13010 Subber=1
13020 ELSE
13030 IF Dat(3,Cnt-5) THEN
13040 IF Dat(3,Cnt-4) THEN
13050 Found_bad("U2","Q2","(R10)")
13060 Subber=1
13070 ELSE
13080 Found_bad("Q1","(R166)")
13090 Subber=1
13100 END IF
13110 ELSE
13120 IF Dat(3,Cnt-3) THEN
13130 IF NOT No_switch THEN
13140 Found_bad("U2","Q5","(R11)","(Q4)")
13150 Subber=1
13160 ELSE
13170 IF NOT Dat(3,Cnt-2) THEN
13180 Found_bad("Q1","Q2","UR3","(R9)")
13190 Subber=1
13200 ELSE
13210 IF Dat(3,Cnt-1) THEN
13220 Found_bad("U2","(R12)")
13230 Subber=1
13240 ELSE
13250 Found_bad("U2","Q5","(R11)","(Q4)")
13260 Subber=1
13270 END IF
13280 END IF
13290 END IF
13300 END IF
13310 END IF
13320 END IF
13330 END IF
13340 END IF
13350 IF Flag THEN U2_timer
13360 IF Subber THEN Menu
13370 RETURN
13380 !
13390 U3_timer:

```

```

13400
13410 *****
13420 U3 TIMER TEST                      SERIES 320130
13430 *****
13440
13450 Dums(1)
13460 Subber=0
13470 Flag=0
13480 No_switch=0
13490 Find_it("R45F","RED_PROBE",2)
13500 Find_it("C9F","BLACK_PROBE",1)
13510 Find_it("C7C","YELLOW_PROBE",1)
13520 Find_it("R48L","BLUE_PROBE",3)
13530 RESTORE 13530
13540 DATA 320110,8.25,6.25,A15,320120,.77,.3,A16,320130,.7
7,.3,A17
13550 DATA 320140,15,11,A20,320150,30,10,A20,320160,15,10,A
17
13560 Meas("B97")
13570 Qc("0")
13580 WAIT 10
13590 FOR X=1 TO 6
13600     READ Dat(1,Cnt),H1,Low,A$
13610     Meas(A$)
13620     IF X<>5 THEN
13630         Dat(2,Cnt)=FNDumr
13640     ELSE
13650         Temp=Intermed
13660         Intermed=0
13670         Qc("1")
13680         Start=TIMEDATE
13690         REPEAT
13700             Secs=INT(TIMEDATE-Start)
13710             DISP "15 SECOND TIMER: TIME ELAPSED:";Secs;"
seconds"
13720             Volt5=FNDumr
13730             UNTIL Volt5<.5 OR TIMEDATE-Start>45
13740             Dat(2,Cnt)=INT(TIMEDATE-Start)
13750             IF Volt5>.5 THEN No_switch=1
13760             Intermed=Temp
13770         END IF
13780     IF FNTest THEN Flag=1
13790     Meas("-"&A$)
13800 NEXT X
13810 Meas("-B97")
13820 IF Dat(3,Cnt-6) THEN
13830     Found_bad("U3","(R45)","(C8)")
13840     Subber=1
13850 ELSE
13860     IF Dat(3,Cnt-5) THEN

```

```

1387 Found_bad("U3","R21","R46")
1388 Subber=1
1389 ELSE
1390 IF Dat(3,Cnt-4) THEN
1391 Found_bad("R21","U3")
1392 Subber=1
1393 ELSE
1394 IF Dat(3,Cnt-3) THEN
1395 Found_bad("U3")
1396 Subber=1
1397 ELSE
1398 IF Dat(3,Cnt-2) OR Dat(3,Cnt-1) THEN
1399 IF No_switch AND Dat(3,Cnt-1) THEN
1400 Found_bad("U3","C7","P43","P44")
1401 )
1402 Subber=1
1403 ELSE
1404 Found_bad("U3","C9","R47","R46")
1405 )
1406 Subber=1
1407 END IF
1408 END IF
1409 END IF
1410 END IF
1411 IF Flag THEN U3_timer
1412 IF Subber THEN Menu
1413 RETURN
1414 !
1415 U25_timer: !
1416 !
1417 !*****
1418 U25 TIMER TEST SERIES 330100
1419 !*****
1420 !
1421 Dums(1)
1422 Flag=0
1423 Subber=0
1424 Find_it("U24","14 PIN CHIP CLIP",2)
1425 Find_it("R125C","BLUE PROBE",1)
1426 Find_it("R123L","BLACK PROBE",1)
1427 Find_it("R124R","YELLOW PROBE",1)
1428 Find_it("C3R","RED PROBE",1)
1429 Find_it("R127F","ORANGE PROBE",3)
1430 Stim("T27","T52","I13","J29")
1431 Stim("E60","F60","H56")
1432 Decade("500")
1433 Oc("1")
1434 Power_set(5,12,.1)

```

```

14350 WAIT 1
14360 Toggle(-5)
14370 Fungent(0,"4")
14380 RESTORE 14380
14390 DATA 330110,.8,0,A6,B97,330120,5.2,2.4,A6,B97,330130,
5.2,2.4,A6,B97
14400 DATA 330140,2.25,2.25,A20,B97,330150,.77,.6,A16,B97,3
30160,.8,0,0,0
14410 DATA 330170,1.57,1.29,A17,B97,330180,1.25,.75,0,0,330
190,.25,0,A18,B97
14420 DATA 330200,5,3.3,A16,B97,330210,5,4.8,A17,B97
14430 FOR X=1 TO 11
14440     READ Dat(1,Cnt),Hi,Low,A$,B$
14450     IF X<>6 AND X<>8 THEN CALL Meas(A$,B$)
14460     IF X=6 THEN CALL Stim("M51","N29")
14470     IF X=2 THEN CALL Toggle(-9)
14480     IF X=3 THEN
14490         Toggle(9)
14500         Stim("-T27")
14510     END IF
14520     IF X=5 THEN CALL Stim("T27")
14530     IF X=8 THEN
14540         Stim("Q13","R51")
14550         Cnts(10002,".8,2.4",10)
14560         Toggle(-9)
14570         WAIT 3
14580         Dat(2,Cnt)=FNCntr
14590         Stim("-Q13","-R51")
14600     END IF
14610     IF X<>8 THEN Dat(2,Cnt)=FNDumr
14620     IF FNTest THEN Flag=1
14630     IF X<>6 AND X<>8 THEN CALL Meas("-" & A$, "-" & B$)
14640     IF X=6 THEN CALL Stim("-M51","-N29")
14650 NEXT X
14660 Stim("-T27","-T52","-I13","-J29")
14670 Stim("-E6U","-F6U","-H50")
14680 IF Dat(3,Cnt-11) THEN
14690     Found_bad("U24","Q44","(U25)","(R172)")
14700     Subber=1
14710 ELSE
14720     IF Dat(3,Cnt-10) THEN
14730         Found_bad("U24","(U25)")
14740         Subber=1
14750     ELSE
14760         IF Dat(3,Cnt-9) THEN
14770             Found_bad("U24","Q44","(U25)","(R169)")
14780             Subber=1
14790         ELSE
14800             IF Dat(3,Cnt-8) THEN
14810                 Found_bad("U25","(U29)","(R175)")

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```

14820         Subber=1
14830     ELSE
14840         IF Dat(3,Cnt-7) THEN
14850             Found_bad("Q47","U25","(R171)")
14860             Subber=1
14870     ELSE
14880         IF Dat(3,Cnt-6) THEN
14890             IF Dat(3,Cnt-5) THEN
14900                 Found_bad("U25","Q45","Q48","(R1
14910 771)","(R174)")
14920                 Subber=1
14930             ELSE
14940                 Found_bad("Q45","Q46","(R176)")
14950                 Subber=1
14960             END IF
14970     ELSE
14980         IF Dat(3,Cnt-4) THEN
14990             IF Dat(2,Cnt-4)=0 THEN
15000                 Found_bad("U25","Q47","C28","(
15010 R173)")
15020                 Subber=1
15030             ELSE
15040                 IF Dat(3,Cnt-3) THEN
15050                     IF Dat(3,Cnt-2) THEN
15060                         Found_bad("U25","Q47","
15070 C28","(R173)")
15080                         Subber=1
15090                     ELSE
15100                         Found_bad("U25"
15110 Subber=1
15120                     END IF
15130                 ELSE
15140                     Found_bad("Q45","Q46","
15150 (R152)")
15160                     Subber=1
15170                 END IF
15180             END IF
15190         END IF
15200     END IF
15210 END IF
15220 END IF
15230 END IF
15240 END IF
15250 END IF
15260 END IF
15270 IF Flag THEN U25_timer

```

```

15250 IF Subber THEN Menu
15260 RETURN
15300 P2_11_35:
15310
15320 *****
15330 P2-11-35 INPUT TEST SERIES 310200
15340 *****
15350
15360 Doms(1)
15370 Find_it("Q3R","RED_PROBE",2)
15380 Find_it("CPBR","ORANGE_PROBE",3)
15390 Meas("B92")
15400 Stim("E60","F60","H56")
15410 Decade("500")
15420 Power_set(5,12,.1)
15430 WAIT .5
15440 Toggle(-5)
15450 Stim("-E56","-F60","-H56")
15460 WAIT 1
15470 Subber=0
15480 Flag=0
15490 RESTORE 15500
15500 DATA 310210,2.90,0,T27,T52,310220,11.55,9.45,-T27,T52
15510 DATA 310230,11.55,9.45,T27,-T52
15520 Meas("A18","B92")
15530 FOR X=1 TO 3
15540 READ Dat(1,Cnt),H1,Low,A$,B$
15550 Stim(A$,B$)
15560 IF X=3 THEN
15570 Stim("E52")
15580 Power_set(5,15,.1)
15590 END IF
15600 Dat(2,Cnt)=F Doms
15610 IF FNTTest THEN Flag=1
15620 IF A$(1,1)="" THEN CALL Stim("-E56")
15630 IF B$(1,1)="" THEN CALL Stim("-F60")
15640 NEXT X
15650 Toggle(-5)
15660 Stim("-E52")
15670 Meas("-A18","-B92")
15680 IF Dat(3,Cnt-3) THEN
15690 Found_bad("Q6","Q7","R20")
15700 Subber=1
15710 ELSE
15720 IF Dat(3,Cnt-2) THEN
15730 Found_bad("Q6","CP9","R19","R21")
15740 Subber=1
15750 ELSE
15760 IF Dat(3,Cnt-1) THEN
15770 Found_bad("R22","LR1")

```

```

15790         Subber=1
15790     END IF
15800     END IF
15810     END IF
15820     IF Flag THEN P2_11_35
15830     IF Subber THEN Menu
15840     RETURN
15850     !
15860 Q7_q8: !
15870     !
15880     !*****
15890     !Q7/Q8 TRANSISTOR CIRCUIT TEST SERIES 310300
15900     !*****
15910     !
15920     Dums(1)
15930     Flag=0
15940     Subber=0
15950     Find_it("R25L","YELLOW_PROBE",2)
15960     Find_it("C3R","RED_PROBE",1)
15970     Find_it("R28F","BLACK_PROBE",3)
15980     Meas("B97")
15990     Stim("E60","F60","H56")
16000     Decade("500")
16010     Power_set(5,12,.1)
16020     WAIT .5
16030     Toggle(-5)
16040     Stim("-E56","-F60","-H56")
16050     RESTORE 16050
16060     DATA 310310,11,9,310320,5.2,2.4,310330,.5,0
16070     DATA 310340,.8,0,310350,27.94,22.86
16080     FOR X=1 TO 5
16090         READ Dat(1,Cnt),Hi,Low
16100         IF X=4 THEN CALL Stim("T27")
16110         IF X=1 THEN
16120             Meas("A17")
16130             Dat(2,Cnt)=FNDvmr
16140             Meas("-A17")
16150         ELSE
16160             IF X=2 OR X=4 THEN
16170                 Stim("M49")
16180                 Dat(2,Cnt)=FNDvmr
16190                 Stim("-M49")
16200             ELSE
16210                 Meas("A16")
16220                 Dat(2,Cnt)=FNDvmr
16230                 Meas("-A16")
16240             END IF
16250         END IF
16260         IF FNTest THEN Flag=1
16270     NEXT X

```

```

16211 Meas = 0
16212 sum = 0
16213 IF Dat 3, Cont = 1 THEN
16214     Round_Load = 100, 100, 100, 100
16215     Subber = 1
16216 ELSE
16217     IF Dat 3, Cont = 1 THEN
16218         IF Dat 3, Cont = 1 THEN
16219             Round_Load = 100, 100, 100, 100
16220             Subber = 1
16221         ELSE
16222             Round_Load = 100, 100, 100, 100
16223             Subber = 1
16224         END IF
16225     ELSE
16226         IF Dat 3, Cont = 1 THEN
16227             IF Dat 3, Cont = 1 THEN
16228                 Round_Load = 100, 100, 100, 100
16229                 Subber = 1
16230             ELSE
16231                 Round_Load = 100, 100, 100, 100
16232                 Subber = 1
16233             END IF
16234         END IF
16235     END IF
16236 END IF
16237 IF Flag THEN W_Lad
16238 IF Subber THEN Meas
16239 RETURN
16240
16241 P2_12:
16242 *****
16243 P2-12 OUTPUT TEST *****
16244 *****
16245
16246 Qums = 1
16247 Subber = 1
16248 Flag = 0
16249 Find_1 = PR400, REC_PROBE 1
16250 Find_1 = PR400, REC_PROBE 1
16251 Find_1 = PR400, REC_PROBE 1
16252 Meas = 0
16253 Cont = 1
16254 Temp = Intermed
16255 Intermed = 0
16256 REPEAT
16257     O16P TIMER HOLD, 1 ELSE 1
16258 UNTIL END Qums
16259 O16P

```



```

17750 P146
17760 Subber=1
17770 ELSE
17780 IF Car=1,2,3,4,5 THEN
17790 Subber=1
17800 PRINT "CAR# 11: THERE IS A PROBLEM WITH THE
COMPARATOR CIRCUITS"
17810 PRINT
17820 PRINT "YOU MUST RETURN TO THE MENU AND RE-
N THE TEST SERIES:"
17830 PRINT "2109,2110,AND 2144"
17840 PRINTER IS 1
17850 PRINT "THERE IS A PROBLEM WITH THE COMPAR-
OR CIRCUITS"
17860 PRINT
17870 PRINT "YOU MUST RETURN TO THE MENU AND RE-
N THE TEST SERIES:"
17880 PRINT "2109,2110,AND 2144"
17890 PRINTER IS 1
17900 Goon
17910 ELSE
17920 Found_bad =234 + 113 + 113 + 113 + 113
OR2)"
17930 Subber=1
17940 END IF
17950 END IF
17960 END IF
17970 END IF
17980 IF Flag THEN P2_1
17990 IF Subber THEN Menu
18000 RETURN
18010 "
18020 P2_13: "
18030 "
18040 "*****
18050 "P2-13 OUTPUT TEST" SERIES 3411
18060 "*****
18070 "
18080 Dums(1)
18090 Subber=0
18100 Flag=0
18110 Find_it("R63R","BLACK PROBE",2)
18120 Find_it("R48L","GREEN PROBE",1)
18130 Find_it("R38L","YELLOW PROBE",3)
18140 Stim("C2","D1","T1","E3","T4")
18150 Stim("G6","T7","I52","J29")
18160 Power_set(4,9,.1)
18170 Power_set(5,2,.1)
18180 Power_set(6,1.3,.1)
18190 Fungen(0,"150")

```

1. The first part of the report deals with the general situation of the country and the progress of the work during the year. It is divided into two main sections: the first section deals with the general situation of the country and the progress of the work during the year, and the second section deals with the specific results of the work.

2. The second part of the report deals with the specific results of the work. It is divided into three main sections: the first section deals with the results of the work in the field of agriculture, the second section deals with the results of the work in the field of industry, and the third section deals with the results of the work in the field of commerce.

3. The third part of the report deals with the financial results of the work. It is divided into two main sections: the first section deals with the income of the organization, and the second section deals with the expenditure of the organization.

4. The fourth part of the report deals with the administrative results of the work. It is divided into two main sections: the first section deals with the organization of the work, and the second section deals with the management of the work.

5. The fifth part of the report deals with the social results of the work. It is divided into two main sections: the first section deals with the social conditions of the country, and the second section deals with the social progress of the country.

6. The sixth part of the report deals with the cultural results of the work. It is divided into two main sections: the first section deals with the cultural conditions of the country, and the second section deals with the cultural progress of the country.

7. The seventh part of the report deals with the educational results of the work. It is divided into two main sections: the first section deals with the educational conditions of the country, and the second section deals with the educational progress of the country.

8. The eighth part of the report deals with the health results of the work. It is divided into two main sections: the first section deals with the health conditions of the country, and the second section deals with the health progress of the country.

9. The ninth part of the report deals with the housing results of the work. It is divided into two main sections: the first section deals with the housing conditions of the country, and the second section deals with the housing progress of the country.

10. The tenth part of the report deals with the transportation results of the work. It is divided into two main sections: the first section deals with the transportation conditions of the country, and the second section deals with the transportation progress of the country.

[illegible]

[illegible]

```

20170 Subber=1
20180 ELSE
20190 IF Dat(3,Int=3) THEN
20200 Found_bad="R6",R15,R16,R17
20210 Subber=1
20220 ELSE
20230 IF Dat(3,Int=2) THEN
20240 IF Dat(3,Int=6) THEN
20250 Found_bad="R11",R14,R15,R16
20260 Subber=1
20270 ELSE
20280 Found_bad="R11",R12,R15
20290 Subber=1
20300 END IF
20310 ELSE
20320 IF Dat(3,Int=6) THEN
20330 IF Dat(3,Int=6) THEN
20340 Found_bad="R13",R14,R15,R16
20350 Subber=1
20360 ELSE
20370 Found_bad="R12"
20380 Subber=1
20390 END IF
20400 ELSE
20410 IF Dat(3,Int=4) THEN
20420 Found_bad="R13",R19,R41
20430 Subber=1
20440 ELSE
20450 IF Dat(3,Int=3) THEN
20460 Found_bad="R6",R15,R16
20470 Subber=1
20480 ELSE
20490 IF Dat(3,Int=2) THEN
20500 Found_bad="R18",R19,R41
20510 Subber=1
20520 END IF
20530 END IF
20540 END IF
20550 END IF
20560 END IF
20570 END IF
20580 END IF

```

```

20610     END IF
20620     END IF
20630     END IF
20640     IF Flag THEN PL_17_38
20650     IF Subber THEN Menu
20660     RETURN
20670
20680 Flip_top:
20690
20700 *****
20710 FLIP FLIP CIRCUIT TEST          SERIES 340500
20720 *****
20730
20740 Dims 1
20750 Flag=0
20760 Subber=0
20770 Find_it "R50R", "RED PROBE", 1
20780 Find_it "R58R", "BLACK PROBE", 1
20790 Find_it "R51L", "YELLOW PROBE", 1
20800 Find_it "R52L", "ORANGE PROBE", 1
20810 Find_it "R53L", "BLUE PROBE", 1
20820 Find_it "R41R", "GREEN PROBE", 1
20830 Find_it "R35L", "WHITE PROBE", 1
20840 Find_it "R36L", "PURPLE PROBE", 1
20850 Strm "C2", "D1", "T1", "B3", "T4"
20860 Strm "G6", "T7", "I52", "D22", "I24"
20870 Power_set 14, 9, 10
20880 Ovs ("28", 1)
20890 Power_set 16, 1.3, 10
20900 Ocl "1000"
20910 RESTORE 20890
20920 DATA 340510, .1, 0, A19, B97, 340520, 25.35, 21.15, A15, B97, 3
40530, 22, 13, A19, B97
20930 DATA 340540, .27, .63, A17, B20, 340550, .1, .16, A16, B20, 14
3560, .2, 0, A22, B20
20940 DATA 340570, .2, 0, A21, B20, 340580, 16.3, 13.34, A22, B97, 34
0590, 30.8, 25.2, A21, B97
20950 DATA 340600, .27, .63, A22, B97, 340610, .27, .63, A21, B97
20960 FOR X=1 TO 11
20970     READ Dat(1, Ent 1, H1, Low, A$, B$)
20980     Meas(A$, B$)
20990     IF X=3 THEN
21000         Ocl "0001"
21010         DISP "TIMER HOLD, PLEASE WAIT."
21020         WAIT 30
21030         DISP ""
21040     END IF
21050     IF X=4 THEN
21060         Strm "E56", "E57"
21070         Power_set 15, 28, 10

```



```

21560 Found_bad = 1
21570
21580 Subben=1
21590 ELSE
21600 IF Dat(3),Cnt=3 THEN
21610 Found_bad = 1
21620 Subben=1
21630 ELSE
21640 IF Dat(3),Cnt=2 THEN
21650 Found_bad = 1
21660 Subben=1
21670 ELSE
21680 IF Dat(3),Cnt=1 THEN
21690 Found_bad = 1
21700 Subben=1
21710 END IF
21720 END IF
21730 END IF
21740 END IF
21750 END IF
21760 END IF
21770 END IF
21780 END IF
21790 END IF
21800 IF Flag THEN Flip_Flop
21810 IF Subben THEN Menu
21820 RETURN
21830
21840 Which_One:
21850
21860 .....
21870 WHICH OUTPUT FAILED?
21880 .....
21890
21900 Right$=DUAL$(DUAL(DUAL$(CH1),8),2)
21910 Right$=Right$(19,32)
21920 Wrong$=DUAL$(DUAL(DUAL$(Dat(2),Cnt),8),2)
21930 Wrong$=Wrong$(19,32)
21940 RESTORE 21950
21950 DATA P2-9,P2-10,P2-13,P2-12,P2-44,P2-30,P2-38
21960 READ Outputs$(*)
21970 FOR x=1 TO 13 STEP 2
21980 IF Wrong$(x,x) <> Right$(x,x) THEN
21990 Bad_out$=Outputs$(x+1)/2
22000 PRINT "THE ";Bad_out$;" OUTPUT IS NOT WORKING"
22010 PRINT "PROPERLY"

```

```

22020         WFL:
22030         GOTO 22060
22040     END IF
22050 NEXT X
22060 IF Bad_out$="P2-2" OR Bad_out$="P2-10" THEN GOTO 22100
22070 IF Bad_out$="P2-12" THEN GOTO 22060
22080 IF Bad_out$="P2-44" THEN GOTO 22060
22090 IF Bad_out$="P2-13" THEN
22100     GOSUB U3_timer
22110     GOSUB P2_1
22120     GOSUB Flip_flop
22130     GOSUB P2_13
22140 END IF
22150 IF Bad_out$="P2-37" OR Bad_out$="P2-38" THEN
22160     GOSUB U1_timer
22170     GOSUB U3_timer
22180     GOSUB P2_1
22190     GOSUB P2_37_38
22200 END IF
22210 RETURN
22220
22230 Finished:
22240 LOAD "END_TEST"&System$
22250 END

```

The author of this thesis, Michael D. Pilkenton, was born on December 18, 1962 to Mr. and Mrs. Marvin D. Pilkenton in Louisville, Kentucky. He attended Serena high school in Louisville and graduated in 1981 from the advanced program. Mr. Pilkenton then entered the University of Louisville Speed Scientific School in the fall of 1981 and received a Bachelor of Science degree in May of 1986.

Mr. Pilkenton entered the Air Force ROTC program at the University of Louisville in the Spring of 1983 and was commissioned as a Second Lieutenant in the United States Air Force in March of 1986. He is also a member of the Institute of Electrical and Electronics Engineers and was elected to the Eta Kappa Nu and Tau Beta Pi honor societies.

Michael D. Pilkenton was married to Elizabeth R. Patterson on May 17, 1986 and received his Master of Engineering degree with specialization in Electrical Engineering from the University of Louisville Speed Scientific School in December of 1986.

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