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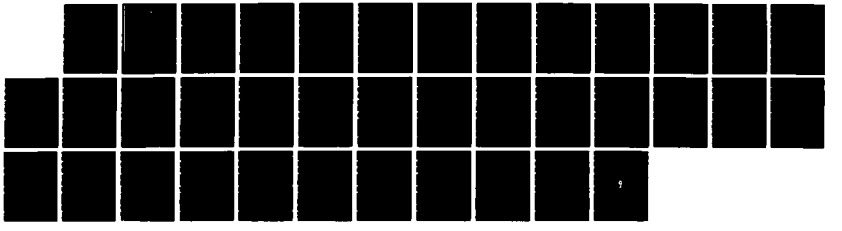

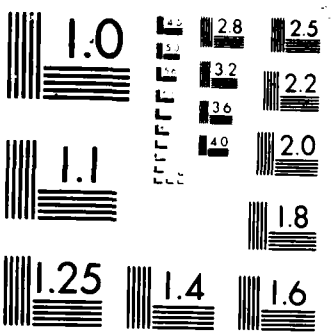

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011LB11

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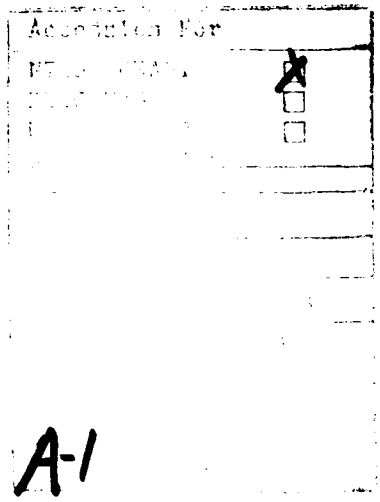
ACKNOWLEDGEMENT

The author wishes to acknowledge the suggestions made by R. Robinson of DREO and D. Roy of Interactive Circuits and Systems Ltd.



ABSTRACT

The design of the interface electronics for an Avalanche Photodiode (APD) array is discussed in the context of an Acousto Optic spectrum analyzer. The attainable performance includes a Noise Effective Power on the order of 10^{-14} W/$(H_z)^{1/2}$, an optical dynamic range of 40-45 dB and a bandwidth of 3 MHz.

RÉSUME

Ce rapport traite de la conception de circuits électroniques pour faire l'interface à une barette linéaire de photodiodes avalanches dans le contexte d'un système acousto-optique analyseur de spectre. La performance atteinte inclus une puissance de bruit de l'ordre de 10^{-14} W/$(H_z)^{1/2}$, une plage dynamique des signaux optiques de l'ordre de 40-45 dB et une largeur de bande de 3 MHz.

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1.0 INTRODUCTION

The properties of Avalanche Photodiode (APD) arrays are substantially different from those of conventional photodetector arrays, especially those providing serial access to individual outputs. In the context of an acousto-optic spectrum analyzer it is necessary to adopt a different implementation approach to exploit the capabilities of the APD array, especially the relatively large dynamic ranges possible without unnecessarily incurring the limitations of other photodetector array architectures.

The APD arrays are fundamentally parallel devices, each photodetector provides a unique continuous time output; no possibility of integrating additional electronics on the detector array for amplification or time division multiplexing of output lines exists. Even if external multiplexers or analog shift registers for parallel input to serial output conversion are used, it is difficult to preserve the 40 dB optical dynamic range of the APD array, especially if a sufficiently high serial data rate is used to provide an adequate sampling rate for good Time of Arrival (TOA) resolution.

Furthermore the performance of individual APD elements is sufficiently sensitive to small variations in the manufacturing process that it is difficult to produce arrays with more than 2^5 or 2^7 elements. Therefore considerable parallelism in the APD interface electronics is both feasible and desirable.

The proposed architecture for the APD interface electronics is illustrated in Figure 1. Each APD output is amplified by a low noise transimpedance preamplifier whose low input impedance minimizes crosstalk problems due to stray capacitance between the APD outputs. The large dynamic range at the preamplifier output (80 dB for a 40 dB optical dynamic range) is compressed by a logarithmic amplifier to permit subsequent processing using 8-bits of resolution provided by a flash A/D converter. The sampling rate of the A/D converter can be on the order of 10 MHz to minimize the information lost due to aliasing. The peak detection logic permits a reduction in the data react to 1 MHz by identifying the largest of every 10 samples. The preprocessor operates on the raw data from all channels to arrange the relevant information into a format compatible with further processing.

2.0 ANALOG SIGNAL PROCESSING

2.1 Requirements

The APD preamplifier has a number of technical requirements, some of which are mutually conflicting. They include:

(i) Large Dynamic Range: An electrical dynamic range of 80 dB is required to achieve a 40 dB optical dynamic range due to the square law relationship between the output power of a photodetector dissipated in a resistive load and the input light intensity. It is desirable to minimize sources of noise and achieve high sensitivity to minimize potential light budget problems in the AO RESM system application.

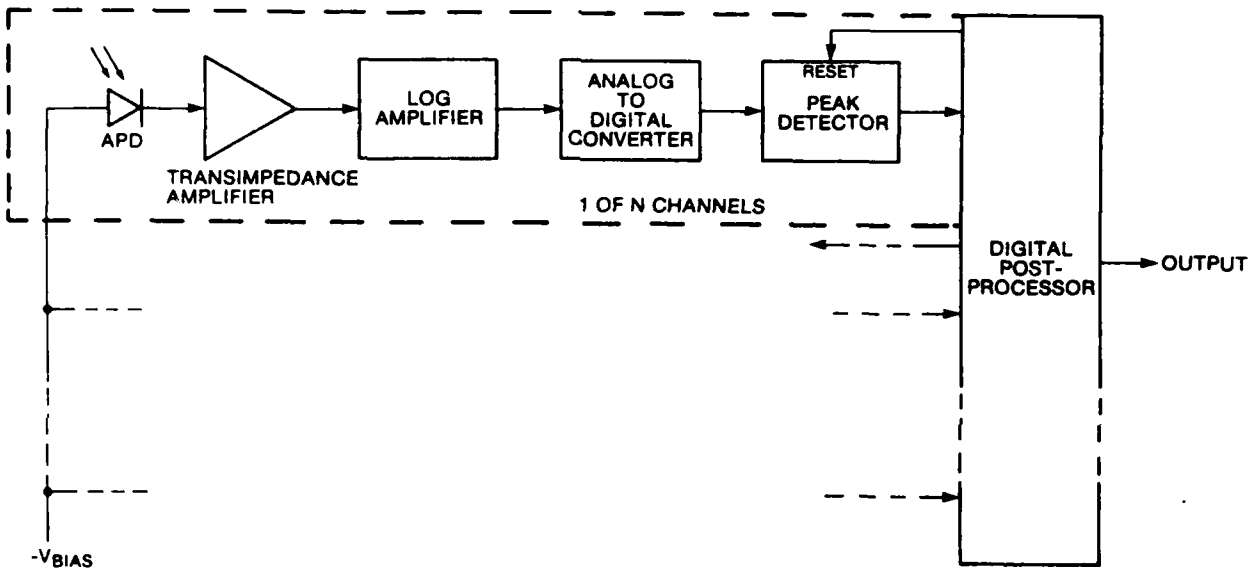


FIG. 1: ARCHITECTURE OF APD INTERFACE ELECTRONICS

(ii) Large Bandwidth: A bandwidth extending from DC to at least several MHz is required. A DC frequency response is desirable to avoid apparent level shifts dependent on the duty cycle of the input signal. The upper limit is needed to permit accurate Time of Arrival (TOA) measurements for pulse-like signals and to minimize the dispersion of short duration pulse-like signals which would tend to reduce their apparent peak power. Some uncertainty exists concerning the optimal choice of bandwidth. In the ESM application it is desirable to handle pulsed signals whose pulse widths may be less than 100 ns. However the greater than 10 MHz bandwidth that is required to preserve information about the shape of narrow pulses necessarily increases the noise level, complicates the design of the transimpedance amplifier and requires that subsequent A/D conversion be performed at rates exceeding 20 MHz. In practice it is probably preferable to restrict the bandwidth to a few MHz and accept the loss in sensitivity caused by dispersion or stretching of very narrow pulses. It should be noted that the Bragg cell transit time will introduce some optical stretching of the pulse.

(iii) Low Crosstalk: In a practical system the electrical interaction between photodetectors and their interconnections introduces significant crosstalk between the electrical output signals. In particular the output of each APD element is effectively coupled to each adjacent element by a series combination of a 5K ohm resistor and .16 pf capacitance which is shunted by 200M ohms [1] and additional parasitic capacitances will exist in the external interconnections. This is a potentially serious problem in the RESM system application since it becomes difficult or impossible to resolve two nearby peaks in the optical intensity distribution illuminating the photodetector array when one peak is much larger than the other. Aside from the obvious measure of minimizing parasitic capacitances between external interconnections, it is desirable to load each photodetector with a low impedance. This is a result of the linear and square law voltage relationships with load impedance which exist for the desired output signal and the crosstalk signal from an adjacent photodetector.

2.2 Preamplifier Implementation Approach

Practical amplifiers are non-ideal in many respects; they possess many sources of error. Because of the complex interdependence between the factors affecting performance parameters, the design problem effectively involves the optimization of a multi-dimensional function. It is therefore necessary to base the design of the preamplifier on a sound understanding of the system performance goals and the factors affecting it.

The most straightforward way of meeting the required performance specifications is to use a transimpedance amplifier implemented using a high speed operational amplifier with a JFET input stage. A transimpedance amplifier has a low input impedance while avoiding the current noise of low value input shunt resistors required for current to voltage conversion if a simple open loop voltage amplifier is used. The basic transimpedance amplifier circuit is illustrated in Figure 2. If the amplifier is assumed to have infinite gain, a common assumption in designing circuits with operational amplifiers, the input impedance is zero and the transimpedance gain Vo/i is simply R_F.

2.3 Design Considerations

The implementation of a practical high performance amplifier involves a number of technical issues.

2.3.1 Stability and Bandwidth

Real amplifiers have finite gains and in the frequency domain their transfer functions contain poles and zeros. As a result the attainable performance will fall short of the theoretical ideal and potential stability problems exist. A more complete model of the APD preamplifier is illustrated in Figure 3. The stray capacitance on the APD output and amplifier input is represented by capacitor C_S and a capacitance C_F in parallel with resistor R_F is included to improve stability and/or control the circuit bandwidth. The resultant circuit is very similar to the infinite gain multiple feedback lowpass filter [2]. The transimpedance transfer function is given by:

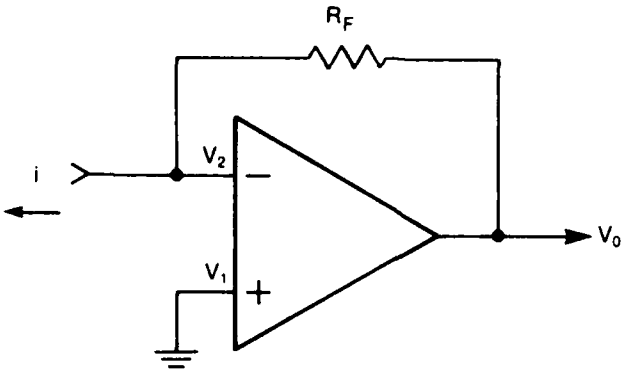
$$\frac{V_o(S)}{i(S)} = \frac{-R_F}{s(R_F\ C_F(1 + 1/A(s)) + R_F C_S/A(s)) + (1 + 1/A(s))} \qquad (1)$$

where A(s) is the open loop transfer function of the operational amplifier.

The input impedance is given by:

$$Z_i(s) = \frac{R_F/A(s)}{s\ (R_F\ C_F(1 + 1/A(s) + R_F\ C_S/A(s)) + (1 + 1/A(s))} \qquad (2)$$

If the operational amplifier is assumed to have a large real valued open loop voltage gain A and C_F is neglected, (1) simplifies to the approximation:



BASIC EQUATIONS

$$V_0 = A(V_1 - V_2)$$

$$\frac{V_0}{I} = -\frac{AR_F}{(1+A)} \longrightarrow -R_F : A \longrightarrow \infty$$

$$Z_{in} = \frac{V_2}{I} = \frac{R_F}{(1+A)} \longrightarrow 0 : A \longrightarrow \infty$$

NOTE: 1. Input bias currents and offset voltages are assumed to be 0

FIG. 2: IDEAL TRANSIMPEDANCE AMPLIFIER

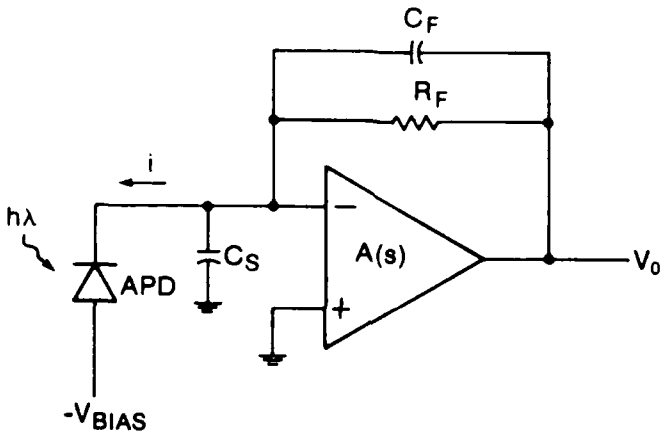


FIG. 3: TRANSIMPEDANCE AMPLIFIER MODEL

$$\frac{V_o(s)}{i(s)} = \frac{-R_F}{1 + s(C_S R_F/A)} \quad (3)$$

which is the transfer function of a single pole lowpass filter with a -3 dB bandwidth given by:

$$3\ dB = A/R_F C_S \quad (4)$$

Since the passband transimpedance gain V_o/i is simply R_F, this suggests that a figure of merit relating sensitivity is given by the current gain bandwidth product (CGBP):

$$CGBP = A/C_S \quad (5)$$

Unfortunately it is not possible to obtain an arbitrarily CGBP in practice. Although C_S can be minimized by careful layout and the use of an amplifier with low input capacitance transistors operated in a cascode configuration, it is difficult to reduce it below several picofarads. The gain of the operational amplifier is a function of the number of stages of amplification, but as each stage introduces at least one pole in the amplifier transfer function, the open loop voltage gain is limited by stability considerations. Consequently the amplifier voltage gain bandwidth product is probably a more significant parameter than the low frequency gain. In a general sense this is related to the design tradeoffs seen in the high speed monolithic operational amplifier integrated circuits such as the LM6161 and RCA CA 3450 which have low open loop voltage gains of 550 and 50 respectively [3]. A reasonable representation of the transfer function of a practical operational amplifier is given by

$$A(s) = \frac{A_{DC}}{(1 + sT_1)(1 + sT_2)(1 + sT_3)} \quad (6)$$

where A_{DC} is the DC open loop voltage gain and T_i is the time constant associated with the with pole.

The inclusion of the poles in the operational amplifier open loop transfer function and their implications on the stability of the transimpedance amplifier circuit considerably complicates the analysis. For a given choice of operational amplifier the circuit design issues are limited to the choices of R_F, C_F and the operational amplifier frequency compensation. The latter normally determines the largest T_i in the open loop transfer function and in consequence the amplifier open loop gain bandwidth product and slew rate.

In this application standard unity gain frequency compensation providing a phase margin of 45 degrees is a reasonable compromise between stability and bandwidth requirements. This generally forces one T_i to be sufficiently large in comparison with the others that the magnitude of the open loop transfer function decreases to unity at a rate significantly less than 12 dB per octave with respect to frequency. Since the 12 dB per octave slope corresponds to a phase shift of 180°, this constraint satisfies the Barkhausen criterion for stable operation.

The use of input lag frequency compensation where the open loop gain of the operational amplifier is reduced by shunting the input(s) to ground with a resistor or resistor-capacitor network is undesirable in this application due to the thermal noise contribution of the resistor. A practical strategy to optimize the transimpedance gain bandwidth product is to select an operational amplifier with a large open loop voltage gain bandwidth product for unity gain frequency compensated operation, and select R_F empirically to yield the desired bandwidth. C_F is then selected to control the relative magnitude of a peak in the transimpedance amplifier frequency response by reducing the phase shift in the RC network formed by R_F and C_S. The physical layout is critical; it is important to minimize C_S without creating crosstalk or thermal problems.

Reasonable choices of operational amplifiers include the Teledyne Philbrick 1437, the Harris 2541 and National Semiconductor LM6161. The former requires a 27 picofarad frequency compensation capacitor while the other two devices would need an external Junction Field Effect Transistor (JFET) input circuit to provide a good input bias and noise current performance. These devices offer a gain bandwidth product on the order of 40 MHz with unity gain frequency compensation; this is not significantly inferior to the performance of ultra high speed operational amplifiers such as the Analog Devices AD 3554 when they are operated with unity gain frequency compensation.

2.3.2 DC Errors

The requirements associated with the RESM application for an AO spectrum analyzer necessitate a frequency response extending to DC. Therefore the error sources which must be considered include the operational amplifier input bias current I_B and input offset voltage V_{OS}. For the transimpedance amplifier configuration, the output error voltage V_{OE} is given by

$$V_{OE} = V_{OS} + I_B R_F \qquad (5)$$

With current technology, input offset voltages on the order of 1 mV are attainable while the use of amplifiers with JFET input stage allows input bias currents on the order of 100 pA at 25°C. Unfortunately the JFET input bias current typically doubles for each 10°C rise in temperature. Consequently it is necessary to avoid combinations of environmental and operating conditions that will result in high device junction temperatures during operation. This suggests that it may be desirable to use a JFET input stage that is external to the operational amplifier to avoid the temperature rise due to the power dissipation of the latter. It may be possible to implement a number of input stage circuits as a hybrid integrated circuit possibly with the photodetector array on the same substrate. Other ways of alleviating undesirable thermal effects involve reducing the power dissipation of the operational amplifiers. Low power devices such as the National Semiconductor LM6161 and Harris 2544 are attractive in this respect. Another idea is to make use of the unipolar nature of the signal to reduce one of the two power supply voltages to the operational amplifiers. It is expected that calibration techniques can be developed to permit all DC errors to be corrected at periodic intervals during normal system operation.

2.3.3 Sensitivity and Dynamic Range

The sensitivity of the transimpedance amplifier is proportional to the transimpedance gain which is equal to R_F at low frequencies where the operational amplifier has a large open loop gain. Since the thermal noise current of R_F is proportional to $R_F^{-1/2}$ this suggests that the sensitivity and noise performance both improve with increasing R_F. However as discussed in Section 2.3.1 bandwidth and stability considerations limit the usable upper value of R_F. In addition dynamic range considerations may be a significant factor as well. The transimpedance gain and the thermal current noise contribution of resistor R_F for a given bandwidth are dependent on R_F by powers of 1 and -1/2 respectively. Therefore the noise output of the transimpedance amplifier is proportional to $R_F^{1/2}$ even if other noise sources independent of R_F are not significant. Since the output voltage swing of a high speed operational amplifier is typically limited to $\pm$ 10V, the dynamic range is an inverse function of transimpedance gain or sensitivity even though the output noise referred to the input signal current decreases with increasing R_F.

The noise performance of the transimpedance amplifier can be analyzed using the model shown in Figure 4. The noise equivalent circuit of the APD is essentially a noise current generator i_{n1} with a typical value of .07 pA $Hz^{1/2}$ [4]. The operational amplifier noise equivalent circuit is an ideal noise free amplifier with a noise current generator i_{n2} and a noise voltage generator e_{n1}. If a JFET input amplifier stage is used the former term is generally negligible. The feedback resistor R_F is effectively shunted by a noise current generator i_{nR}:

$$i_{nR} = (4KTB/R_F)^{1/2} \qquad (8)$$

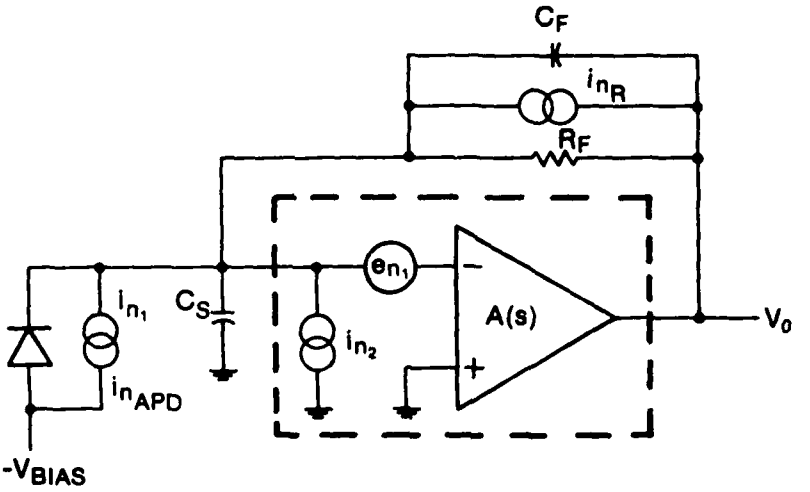


FIG. 4: NOISE MODEL OF TRANSIMPEDANCE AMPLIFIER

where K is Boltzmann's constant (1.38×10^{-23}VA/S), T is the absolute temperature and B is the bandwidth in Hz. If a noise bandwidth of 3 MHz is assumed, this relationship simplifies to:

$$i_{nR} = (2.33 \times 10^{-7}/(R_F)^{1/2}) \quad (9)$$

This is the largest equivalent current noise source provided R_F does not exceed approximately 3×10^6 ohms.

The passband contribution of the equivalent noise current sources to the transimpedance amplifier noise voltage output is approximately:

$$R_F\, i_{nR} = 2.23 \times 10^{-7} \times R_F^{\,1/2} \quad (10)$$

For R_F = 100K ohms, this would be approximately 71 microvolts which corresponds to a dynamic range of approximately 100 dB if a 10 volt output swing is possible.

This analysis has neglected the amplifier equivalent input noise voltage. In the passband the effective voltage gain is unity and using a conservative figure of 20 nV $(Hz)^{1/2}$ the noise output voltage due to this source alone is 35 microvolts which is of limited significance. However, as pointed out in [5] the amplifier equivalent input noise voltage can be significant outside the amplifier passband. At high frequencies the network consisting of R_F, C_F and C_S behaves as a voltage divider and the noise gain of the operational amplifier is no longer unity but $(C_S + C_F)/C_F$. If $C_S \gg C_F$, this source of noise can be significant.

This result shows that C_S should be kept as small as possible, for noise as well as bandwidth considerations. In addition it may be desirable to limit the bandwidth by increasing C_F.

In practice other noise sources may be significant. In a DC coupled system the operational amplifier offset voltage should be considered. This can be nulled to zero by suitable adjustment circuits, but temperature coefficients for matched JFET pairs may be on the order of 10 microvolts/°C. Another problem concerns electromagnetic interference from other circuits in the system. Consequently considerable attention to layout and shielding may be required to approach theoretical performance figures.

The analysis of the transimpedance amplifier suggests that dynamic ranges exceeding 90 dB may be possible with values of R_F less than or equal to 100 K ohms for a 3 MHz noise bandwidth. This translates to a noise effective power of approximately 10^{-14}W/$Hz^{1/2}$ for an APD array with a sensitivity of 50 A/W at 900 nm. This can be compared to the

published results for a parallel photodetector array developed by Harris [6]. Here a minimum detectable power (signal-to-noise ratio of 1) of 10^{-8} W was reported for a 840 nm laser source. If the noise bandwidth is assumed to be the same as the 2.2 MHz photodetector amplifier bandwidth, this suggests that the NEP is $6.7 \times 10^{-12} W/Hz^{1/2}$, a performance that is approximately two orders of magnitude inferior to that attainable with the APD.

2.4 Logarithmic Amplifier

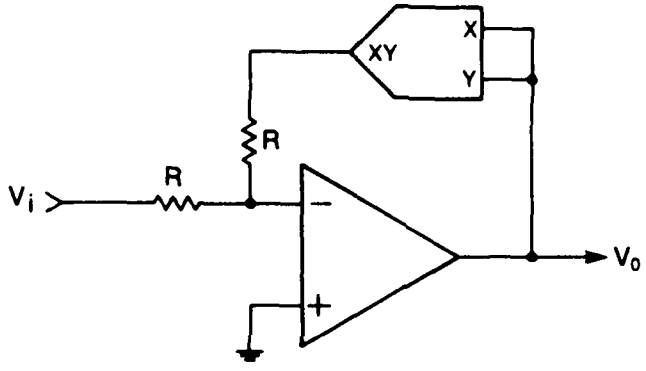
The square law relationship between light intensity and photodetector electrical output power necessitates the use of interface electronics having a large dynamic range. In practice it is necessary to compress the dynamic range of the signal at the output of the photodetector transimpedance amplifier to achieve an optical dynamic range exceeding 40 dB with existing A/D converter technology.

Logical choices for a suitable compression characteristic include square-root and logarithmic functions.

The square root function is conceptually attractive since it is the inverse of the square law relationship between incident light intensity and photodetector output power. A standard approach for implementing a square root characteristic is to place an analog multiplier in the feedback loop of an operational amplifier as shown in Figure 5. Analog multipliers can be easily implemented by using the linearly proportional relationship of transconductance to emitter current for bipolar transistors.

However it is difficult to obtain large dynamic range and bandwidth with practical circuits due to the errors introduced by input offset voltages of the amplifier and multiplier and the amplifier frequency compensation required for stable operation. In addition, even with an ideal square root characteristic, the dynamic range compression is insufficient to allow the use of cost effective 8-bit flash A/D converter technology for optical dynamic ranges much exceeding 40 dB.

A logarithmic characteristic is more commonly used in signal processing for dynamic range compression. It provides more compression than a square root function and permits simple and direct implementations of computational operations such as multiplication by a constant or raising to a power. It should be noted that a logarithmic characteristic can only be realized over a limited dynamic range since the logarithms of zero or negative quantities are undefined.



Notes: 1. $V_I \leq 0$
2. $V_o = (-V_I)^{1/2}$

FIG. 5: SQUARE ROOT AMPLIFIER

A well known way of implementing a logarithmic characteristic is to use the exponential relationship between current and voltage of a forward biased semiconductor pn junction diode:

$$I_o = I_s \left(e^{qV/mKT} - 1\right) \tag{11}$$

where I_s is the diode saturation current, q is the charge of an electron, K is Boltzmann's Constant and T is the absolute temperature in degrees Kelvin. The logarithmic characteristic can be approximated by using a forward biased diode as a non-linear load for converting a signal current to voltage or as a non-linear element in the feedback loop of an operational amplifier as shown in Figure 6. This implementation has significant practical limitations. The diode characteristics are a function of temperature. This is primarily due to I_s which approximately doubles for every 10°C temperature rise. Another problem is that the factor m becomes a function of current at low current levels while at high currents the series bulk ohmic resistance becomes significant. Circuit design techniques have been developed which improve accuracy but adversely affect the practical usable bandwidth [7]. Consequently video bandwidth logarithmic amplifiers using this approach such as the Optical Electronic Incorporated 2920 [8] tend to be poorly suited for applications where a DC frequency response is desired.

Another technique is to implement the logarithmic characteristic using a piecewise linear approximation. The general concept is illustrated in Figure 7. At low input signal levels none of the amplifier output voltages reach the threshold V_L at which limiting occurs and the gain for an incremental change in the input signal voltage is:

$$\frac{dV_{out}}{dV_{in}} = \sum_{n=1}^{N} A^n = \frac{(A^{N+1} - 1)}{A - 1} - 1 \tag{12}$$

where N amplifiers and limiters are used.

If A is assumed to be much larger than unity, the gain expression approaches A^N and the circuit functions as a high gain amplifier. Conversely for large input signals where all of the amplifier outputs undergo limiting, the output is a constant voltage NV_L and the gain becomes

$$\left.\frac{dV_{out}}{dV_{in}}\right|_{minimum} = 0 \tag{13}$$

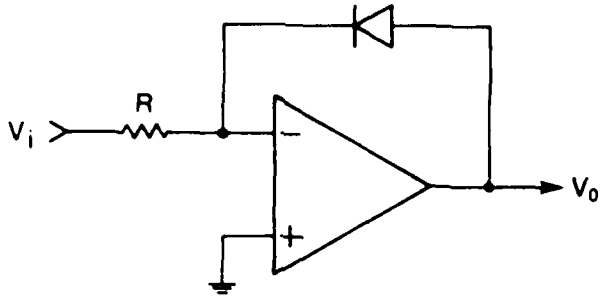


FIG. 6: LOGARITHMIC AMPLIFIER USING SEMICONDUCTOR DIODE CHARACTERISTIC

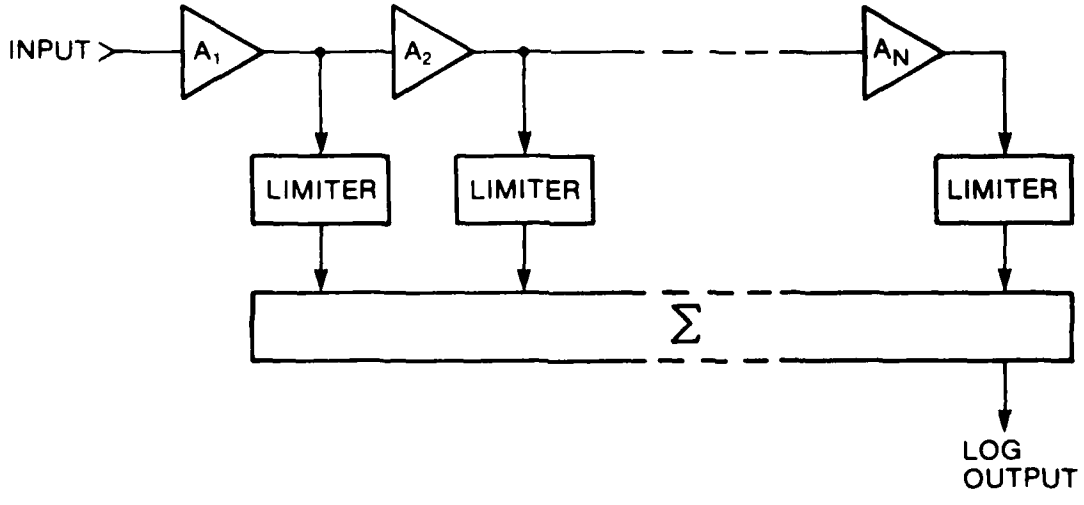


FIG. 7: TECHNIQUE FOR APPROXIMATING A LOGARITHMIC TRANSFER FUNCTION

The limiting and amplification functions can be realized by circuit topologies based on differential amplifiers. High speed operation is attainable since circuit time constants can be kept small and the absence of closed loop feedback avoids the need to introduce poles in the frequency response transfer function to achieve stable operation. This approach has been implemented in low cost monolithic integrated circuits such as the Plessey SL1531 logarithmic IF amplifier. Unfortunately it is not easy to achieve a wide bandwidth coupled with a DC frequency response with a full monolithic implementation due to the need for level shifting circuits. The Texas Instruments TL441 is capable of providing a dynamic range exceeding 80 dB with a bandwidth from DC to 40 MHz, but requires 3 operational amplifiers [9]. It differs from the other devices in using logarithmic rather than linear segments. A hybrid integrated circuit implementation may be feasible using the National Semiconductor LM6161 operational amplifier which is potentially attractive for this application due to its high speed, low power consumption and low cost.The concept has been applied, apparently with some success to an integrated photodetector/amplifier array [10] and merits further attention.

The concept can also be implemented using diode bridges for the limiting function. The basic diode bridge limiter is illustrated in Figure 8. If ideal diodes are assumed, it can be shown from symmetry considerations that

$$I_{D1} = I_{D2} = I_{D3} = I_{D4} = I_B/2 \quad (I_{IN} = 0) \tag{14}$$

$$I_{out} = I_{IN} \qquad (I_{IN} < I_B) \tag{15}$$

$$I_{out} = I_B \qquad (I_{IN} > I_B) \tag{16}$$

In practice the diodes will have some current dependent voltage drop and the transition from (15) to (16) will not be abrupt. Nevertheless this circuit has many desirable properties. Provided the diodes are well matched electrically and thermally, the effects of temperature variations are relatively small. High speed operation is feasible if small signal Schottky Barrier Diodes (SBDs) are used.

Figure 9 illustrates a practical logarithmic amplifier using diode bridges. The output currents of an array of diode bridges are summed and converted to a voltage by the transimpedance amplifier realized with a high speed operational amplifier and a feedback resistor R_F. Each diode bridge is operated with a current I_B determined by resistors R_B and the associated precision power supplies. The maximum output current from any diode bridge I_B defines the maximum output voltage swing resulting from the input signal driving a single diode bridge, where,

$$V_M = I_B R_F$$

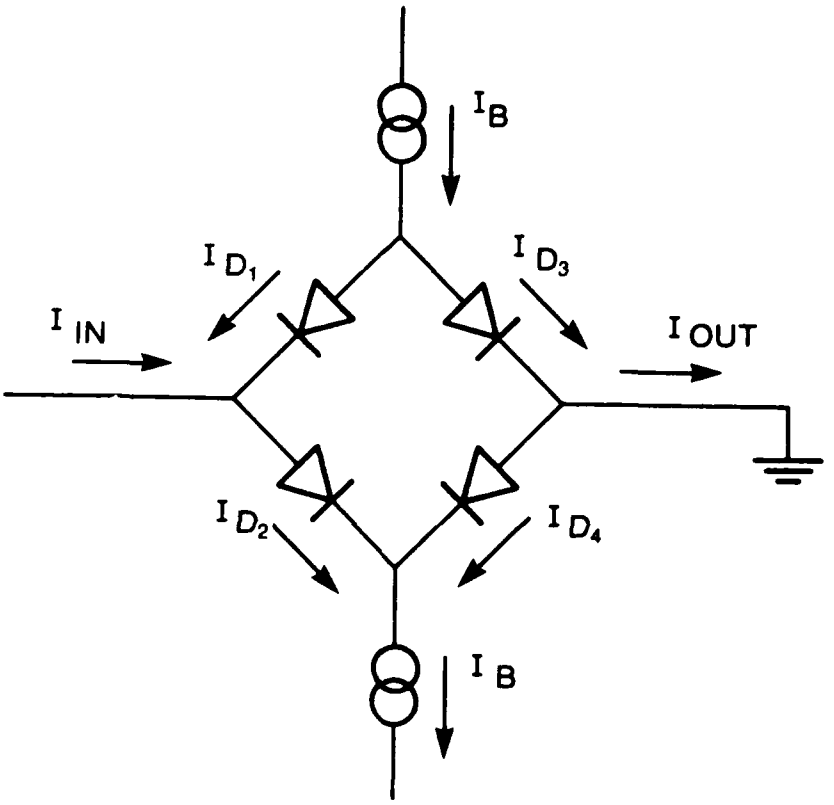
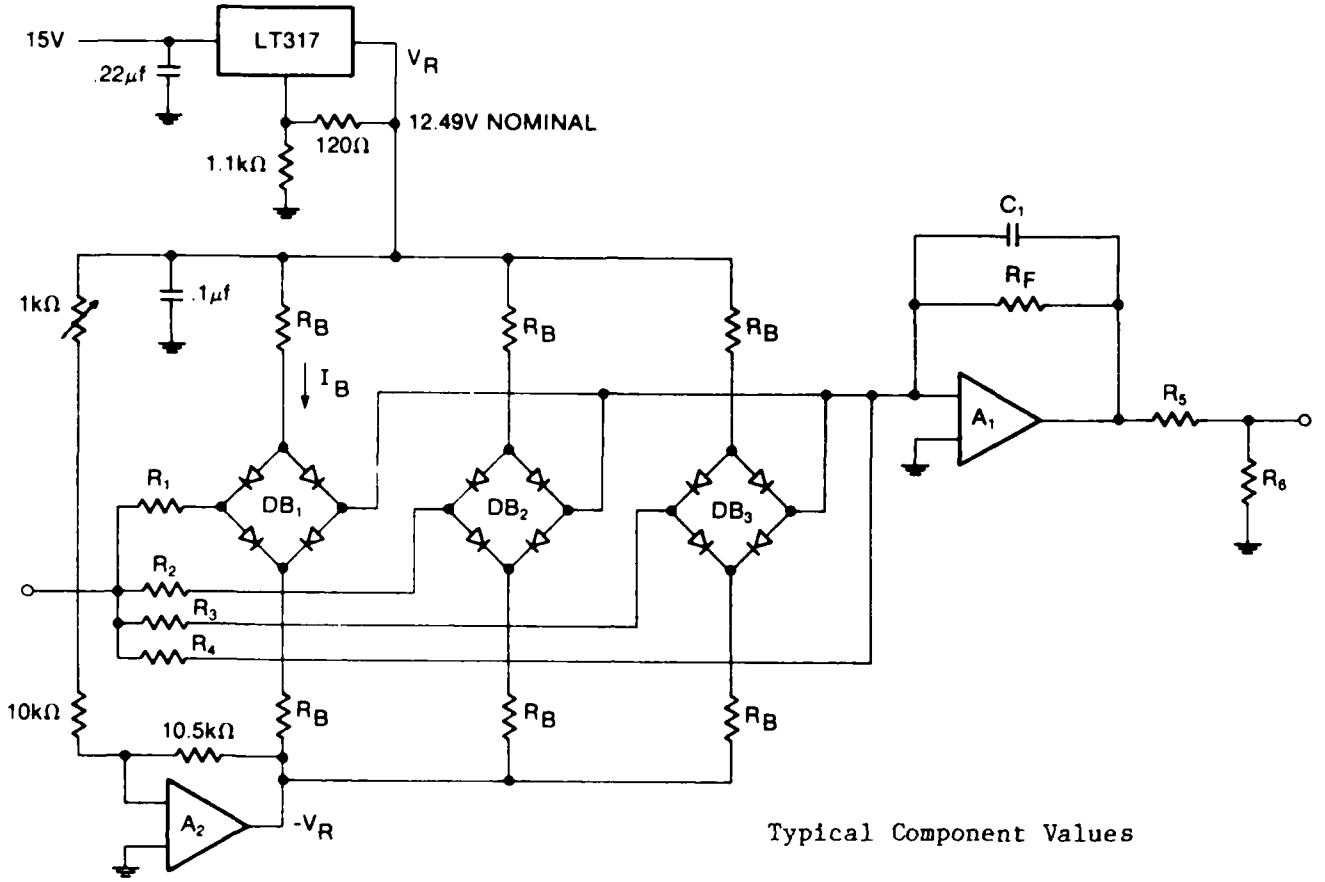


FIG. 8: DIODE CURRENT LIMITER



Typical Component Values

R_1 = 0
R_2 = 332
R_3 = 3670
R_4 = 37K
R_B = 12K
R_F = 2K

FIG 9: PRACTICAL WIDE BANDWIDTH LOGARITHMIC AMPLIFIER

The breakpoints in the transfer function occur at V_M, $2V_M$ and $3V_M$ with the 3 diode bridge limiters.

The input resistors R_1 - R_3 determine the gains associated with their corresponding diode bridges.

$$G = \frac{dV_{out}}{dV_{in}} = -\frac{R_F}{R_1} \left(\frac{V_{IN}}{R_1} \pm I_B \right) \tag{18}$$

Additional dynamic range is provided by resistor R_4 which does not drive a diode bridge limiter and therefore provides a non-zero minimum gain

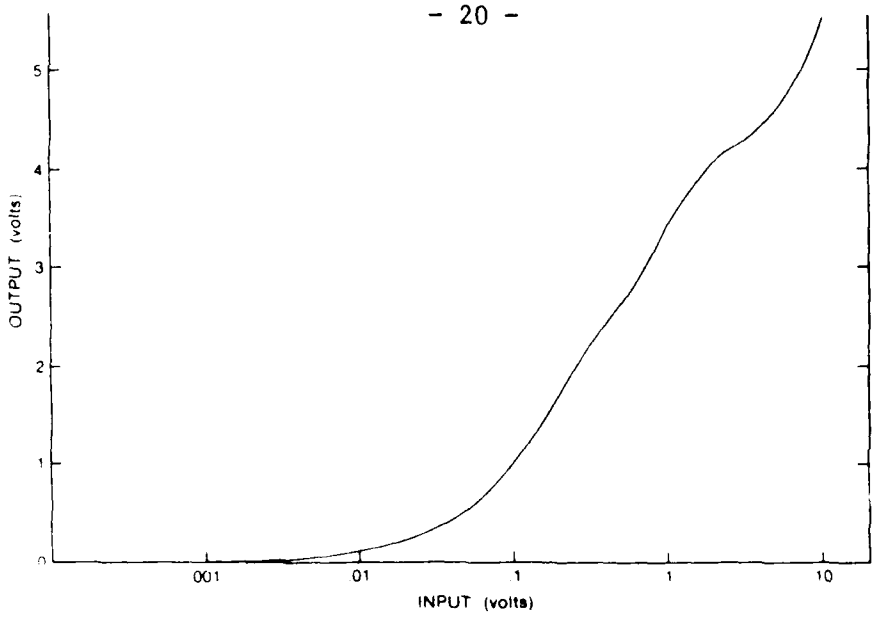
$$G_{MIN} = - R_F/R_4 \tag{19}$$

Figure 10 plots measured results obtained for a DC transfer function of this amplifier for the circuit parameters listed. Although only 3 diode bridges are used, the 80dB input dynamic range is compressed to 44 dB.

If the circuit is implemented with Schottky Barrier Diodes (SBDs) and the Comlinear CL200 series operational amplifier, high speed operation should be possible. The latter are especially appropriate since their special circuit topology permits both high slew rate and closed loop bandwidth independent of the closed loop gain without stability problems. They also have a useful capability for driving low impedance lines and/or A/D converter inputs.

2.5 A/D Conversion

The most appropriate A/D converter technology for digitizing the output of the logarithmic amplifiers is the flash A/D converter. It permits A/D converters with 8-bit resolution and sampling rates on the order of 20MHz to be implemented as relatively low cost monolithic, integrated circuits without the need for sample and hold circuits. Figure 11 shows the functional block diagram of the basic flash A/D converter. A monotonic sequence of the possible input voltages to be encoded as unique binary outputs is produced by an external voltage reference and a resistor divider chain. These are used as reference voltages for an array of analog comparators. The remaining comparator inputs are driven in parallel by the input signal to be digitized. The output of the comparator with the reference voltage nearest but still below the signal voltage determines the binary output generated by encoder logic. Note that 2^N-1 comparators are required for N-bit resolution.



(a) LOGARITHMIC SCALE

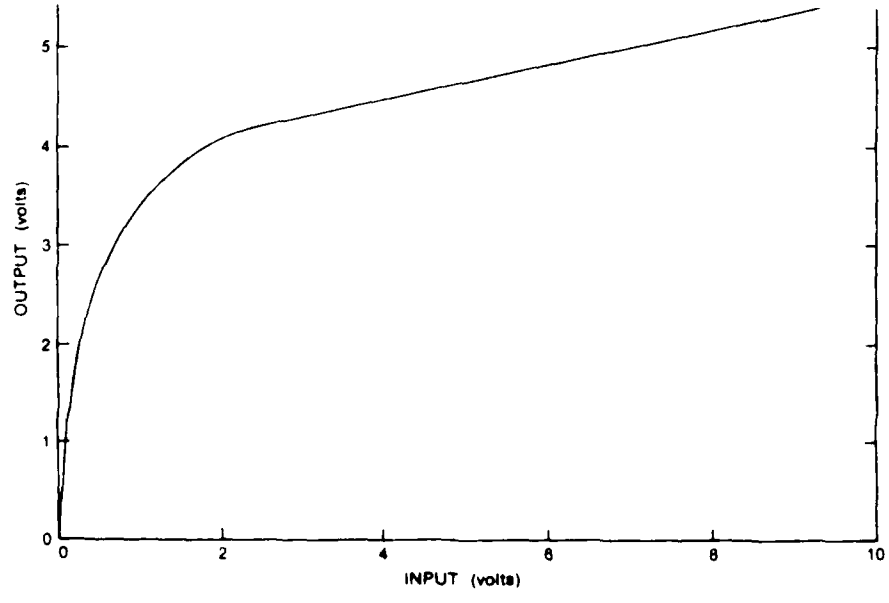


FIG. 10 TRANSFER FUNCTION OF LOGARITHMIC AMPLIFIER

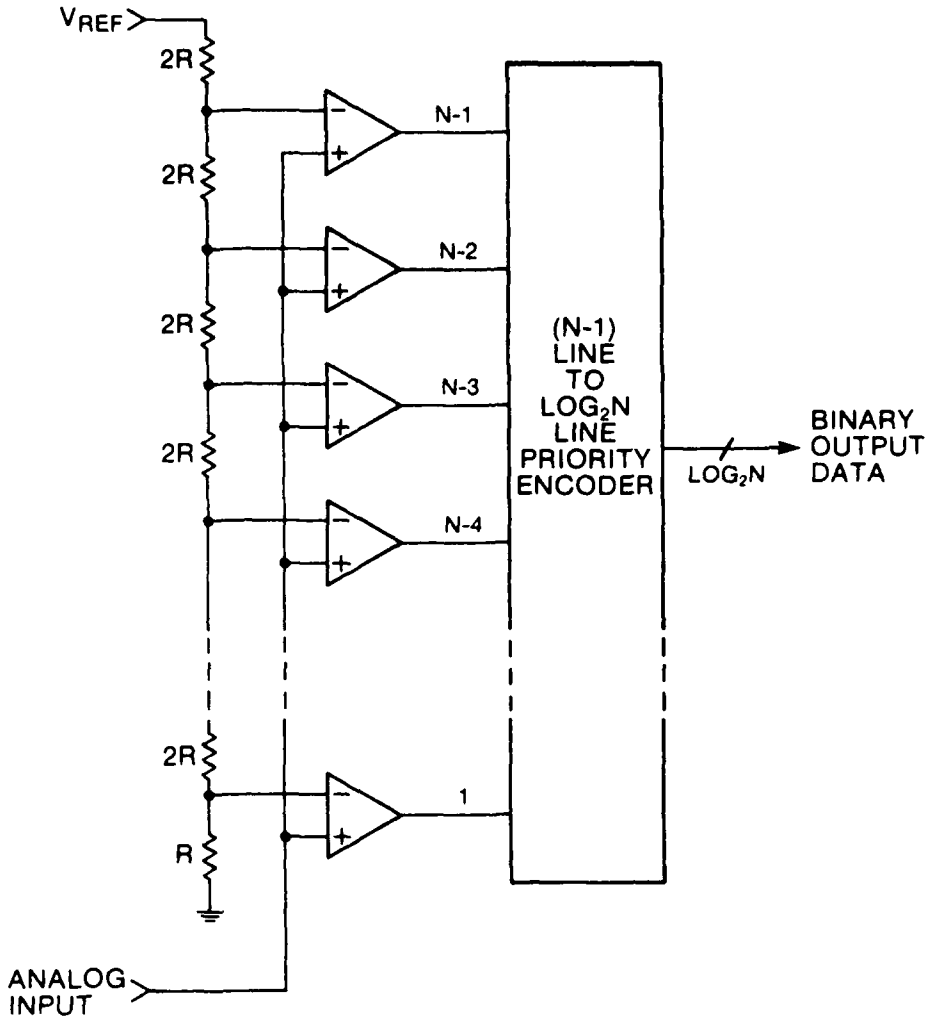


FIG. 11: FLASH A/D CONVERTER

The parallelism implicit in the flash A/D converter permits high speed operation without using sample and hold circuits to hold the input signal constant during the sample period. The technique does have some significant limitations. The cost and to some extent the conversion speed are extremely sensitive to the resolution required; each additional bit resolution necessitates twice as many comparators, and error sources such as comparator input offset voltages become more critical. In addition special buffer amplifiers are often required to drive the A/D input due to the capacitive loading resulting from many comparator inputs being in parallel.

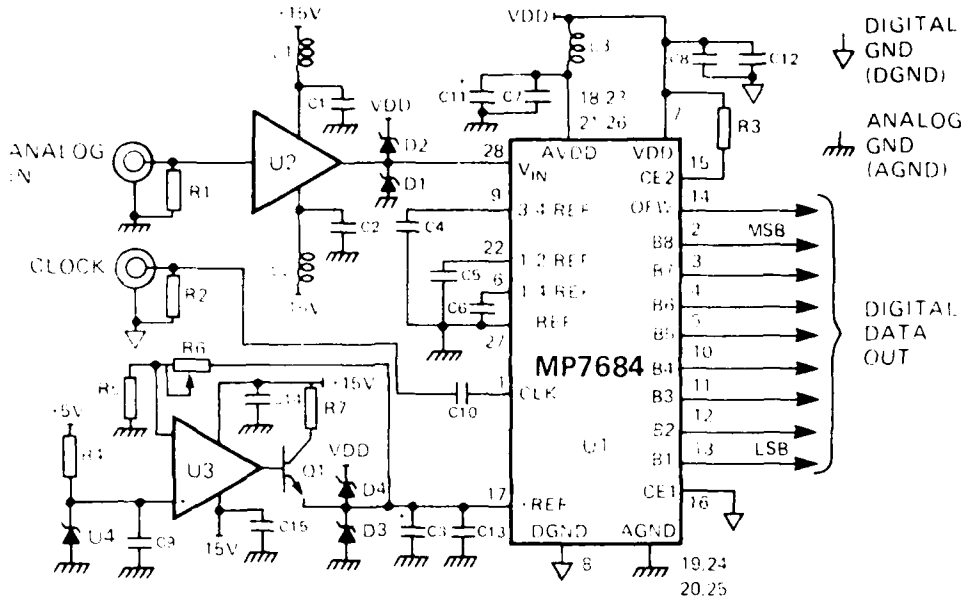
With current technology 8-bit A/D converters which have a 20 MHz maximum sampling rate such as the Micropower Systems MPS 7864 warrant attention for the A/D conversion of APD output signals. Simple non-ideal logarithmic amplifiers with transfer functions like that shown in Figure 9 are adequate while 6 bit A/D converters would be suitable only with a logarithmic amplifier of near ideal characteristics. A practical circuit for the MPS 7864 is shown in Figure 12.

The development of a linear flash A/D converter with the 14-bit resolution needed to eliminate the need for a logarithmic amplifier is not feasible, but a possibility which merits attention is to design a non-linear flash A/D converter with a logarithmic transfer function by suitably selecting the resistor values in the voltage divider chain; the number of comparators could be substantially reduced for a given dynamic range. However, aside from the TRW TDC 1029 6-bit converter which provides external taps connected to the resistor divider chain at 1/4, 1/2 and 3/4 scale to allow some modification of the normally linear transfer function, this idea does not seem to have been considered in practice.

3.0 DIGITAL PROCESSING

3.1 The A/D converters in this AO system configuration can generate data at a rate of 3.2×10^8 samples/second over a communication path consisting of 256 parallel lines if it is assumed that each of 32 photodetector outputs is sampled at a rate of 10 MHz and converted to 8-bit binary data. It is necessary to develop strategies to reduce this data rate and to provide information in a format usable for classifying the signal environment.

A simple initial strategy is to divide each stream of samples into groups or frames of perhaps 10 contiguous samples. The largest sample in each frame is identified using the circuit of Figure 13 and is selected to represent its data frame, thereby achieving an order of magnitude reduction in data rate while simultaneously maintaining one microsecond TOA resolution. The resulting 10^6 sample/second data rate is low enough to allow a



APPLICATION NOTES:

1. **A ceramic DC blocking capacitor (.01μf) must be used at the clock input pin.**
2. The power supplies and reference voltages should be decoupled with a ceramic (.01 to .1μf) and tantalum (10μf) capacitor as close to the device as possible
3. The digital output should not be driven by long wires as the capacitive coupling and reflection will contribute noise to the conversion. When driving distant loads, buffers should be used
4. Sensitive signals such as clock, analog input and reference should be properly routed and terminated to minimize ground noise pick-up and crosstalk. (Wire wrap is not recommended for these signals)
5. Analog and digital ground planes should be substantial and common at one point only. Analog and digital power supplies should be referenced to their respective ground planes
6. Reference voltage should be stable and free of noise. Accuracy of the conversion is highly dependent on the integrity of this signal
7. The analog input should be driven from a low-impedance source (< 25 Ω). This will minimize the possibility of picking up extraneous noise
8. An inductor (100μh) should be used to block clock noise on AV_{DD} pin, to feed into V_{DD}
9. 50% clock duty cycle is recommended, but tweaking of the clock by ± 10% at certain sampling rates may further improve performance

PARTS LIST:

Resistors

R1	75Ω	1/8W metal film 5%
R2	50Ω	1/8W metal film 5%
R3	1KΩ	1/8W metal film 1%
R4	5KΩ	1/8W metal film 1%
R5	1KΩ	1/8W metal film 1%
R6	5KΩ	10 Turn Trimpot
R7	100Ω	1/8W metal film 5%

Capacitors

C1 - C9	0.1μf mylar
C10	0.01μf ceramic
C11 - C13	tantalum (10μf)
C14 - C15	0.1μf mylar

I. C.'s

U1	MP7684 A/D
U2	MP0033 Buff. Amp
U3	MPOP02 Op Amp
U4	MP5010 Voltage Reference
Q1	2N2222 NPN Transistor
D1-D4	schottky barrier diodes (HP 5082-2835)

Inductors

L1 - L3	100μh inductors

FIG. 12: PRACTICAL 8-BIT FLASH A/D CONVERTER CIRCUIT

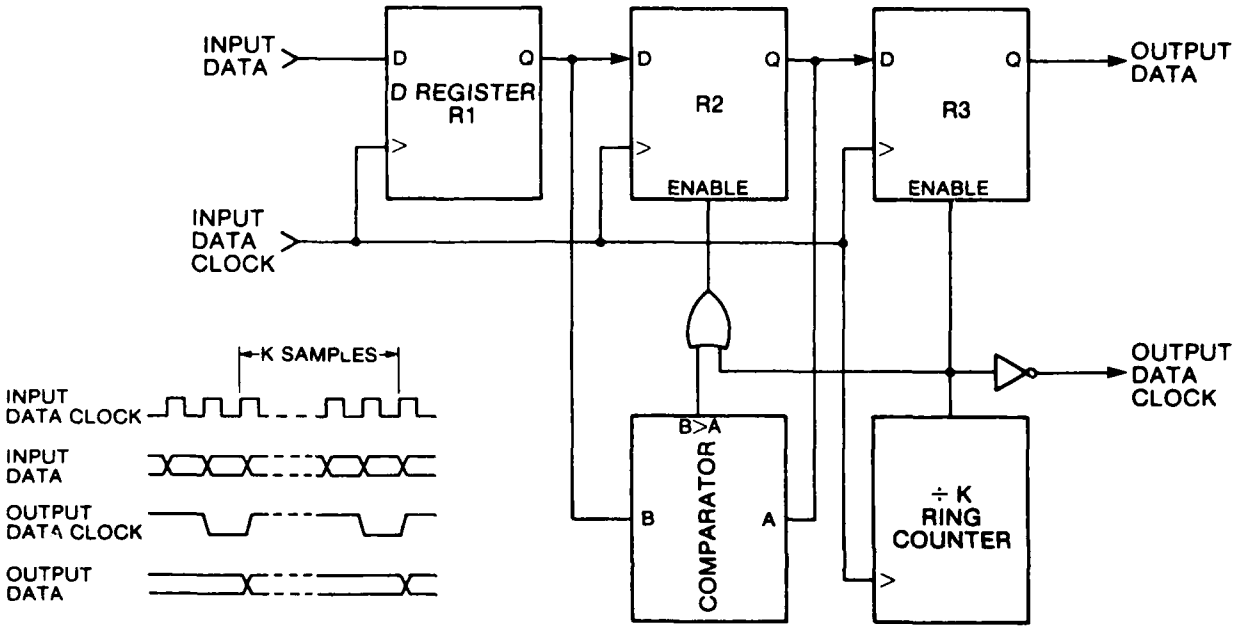


FIG. 13: PEAK DETECTOR

series-parallel architecture for subsequent communication and processing. This can be implemented by dividing the photodetector elements and their analog interface hardware into blocks. For each block a multiplexer or serial input parallel output shift register sequentially transfers the peak output sample from each photodetector over a bus dedicated to that group. The reduction in data rate to 32×10^6 samples/second (for the 32 element array) and the series - parallel data communication approach permit real-time processing operations such as gain correction, spatial or time-domain filtering, peak detection and thresholding to be efficiently carried out using the techniques proposed in [11] for conventional series-parallel photodetector arrays.

4.0 SUMMARY

The design issues for the analog and digital interface electronics needed for the use of an APD array in an AO spectrum analyzer suitable for RESM application are outlined. A practical system can be constructed as a parallel array of channels, each of which is associated with a single APD element. The set of functional modules required for each channel includes the following:

1. Transimpedence Amplifier: The current output of the APD element is converted to a voltage output by a transimpedance amplifier. A suitable design approach is to use a wide bandwidth operational amplifier with a JFET input stage. The choice of the feedback resistor is critical; it affects the sensitivity, dynamic range and bandwidth that can be achieved. A value of 100K ohms is consistent with a Noise Equivalent Power of $10^{14} W/Hz^{1/2}$ referenced to the photodetector input signal power, an optical dynamic range exceeding 40 dB and a bandwidth of 3 MHz.

2. Logarithmic Amplifier: The dynamic range of the transimpedance amplifier should be compressed to allow subsequent processing operations such as A/D conversion to be performed with low cost non-critical hardware. For this application it is most appropriate to use piecewise approximation techniques to realize a logarithmic transfer function.

3. A/D Converter: The output of the logarithmic amplifier can be digitized by a flash A/D converter with 8 bit resolution at sampling rates on the the order of 10 MHz.

4. Digital Processor: The high data rates generated by the A/D converters can be reduced by using only the largest sample from frames or groups of contiguous samples. This reduced data rate is determined by the desired Time of Arrival resolution rather than the duration of the shortest signals to be detected. Subsequent processing can be performed using a series parallel hardware architecture where the number of parallel channels can be much smaller than the number of photodetector elements.

The system can be implemented with commercially available technology if size and power consumption are not major considerations. Hybrid integrated circuit packaging techniques offer some possibilities of saving space. Unfortunately it does not appear to be possible to easily implement all of the analog functions on a monolithic integrated circuit without accepting a significant performance degradation. However the development of a monolithic integrated circuit logarithmic amplifier optimized for this application should be considered.

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A-1150

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DEFENCE RESEARCH ESTABLISHMENT OTTAWA NATIONAL DEFENCE OTTAWA, ONTARIO K1A 0Z4 CANADA	2a. DOCUMENT SECURITY CLASSIFICATION UNCLASSIFIED 2b. GROUP

3. DOCUMENT TITLE

THE APPLICATION OF AVALANCHE PHOTODIODE ARRAYS TO ACOUSTO-OPTIC SIGNAL PROCESSING (U)

4. DESCRIPTIVE NOTES (Type of report and inclusive dates)

TECHNICAL NOTE

5. AUTHOR(S) (Last name, first name, middle initial)

INKOL, Robert J.

6. DOCUMENT DATE DECEMBER 1986	7a. NO. OF PAGES 33	7b. NO. OF REFS 11
8. PROJECT OR GRANT NO. 011LB11	9a. ORIGINATOR'S DOCUMENT NUMBER(S) TN 86-26	
	9b. OTHER DOCUMENT NO(S). (Any other numbers that may be assigned this document)	

10. DISTRIBUTION STATEMENT

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11. SUPPLEMENTARY NOTES	12. SPONSORING ACTIVITY DREO

13. ABSTRACT

(U) The design of the interface electronics for an Avalanche Photodiode (APD) array is discussed in the context of an Acousto-Optic spectrum analyzer. The attainable performance includes a Noise Effective Power on the order of 10^{-14} W/$(H_z)^{1/2}$, an optical dynamic range of 40-45 dB and a bandwidth of 3 MHz.

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Avalanche Photodiode
Transimpedance Amplifier
Logarithmic Amplifier
Analog to Digital Converter

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