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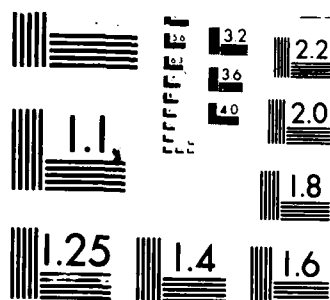
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REPORT DOCUMENTATION PAGE		READ INSTRUCTIONS BEFORE COMPLETING FORM
1. REPORT NUMBER RITRC 010	2. GOVT ACCESSION NO.	3. RECIPIENT'S CATALOG NUMBER
4. TITLE (and Subtitle) Noise Characteristics of MOS Devices Degraded by Electrical Overstressings		5. TYPE OF REPORT & PERIOD COVERED Tech. Report #10
		6. PERFORMING ORG. REPORT NUMBER
7. AUTHOR(s) Perambur S. Neelakantaswamy Ibrahim R. Turkman		8. CONTRACT OR GRANT NUMBER(s) N00014-84-K-0532
9. PERFORMING ORGANIZATION NAME AND ADDRESS RIT Research Corporation 75 Highpower Rd. Rochester, N.Y. 14623-3435		10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS NR 613-005
11. CONTROLLING OFFICE NAME AND ADDRESS Office of Naval Research Arlington, VA. 22217		12. REPORT DATE January 1987
		13. NUMBER OF PAGES 10
14. MONITORING AGENCY NAME & ADDRESS (if different from Controlling Office)		15. SECURITY CLASS. (of this report) Unclassified
16. DISTRIBUTION STATEMENT (of this Report) Scientific Officer N00014 Administrative Contract Officer S3305A Director, Naval Research Laboratory N00173 Defense Tech. Inform Center S47031		15a. DECLASSIFICATION/DOWNGRADING SCHEDULE
17. DISTRIBUTION STATEMENT (of the abstract entered in Block 20, if different from		
18. SUPPLEMENTARY NOTES		
19. KEY WORDS (Continue on reverse side if necessary and identify by block number) Electrical Overstressings (EOS), MOS Devices, Performance Degradation, Noise Characteristics		
20. ABSTRACT (Continue on reverse side if necessary and identify by block number) The endochronic degradation of MOS devices arising from the global response of the device parameters collectively deteriorating under the repetitive influence of electrical over stresses (at subcatastrophic levels) such as electrostatic discharge (ESD), electromagnetic pulsing (EMP), etc., is quantified in terms of noise characteristics. Life-time studies depicting the degradation of a test device are presented. Computed and experimental data are furnished.		

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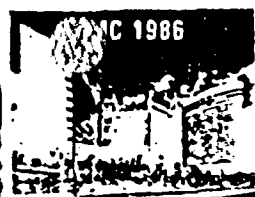
NOISE CHARACTERISTICS OF MOS DEVICES

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NOISE PERFORMANCE STUDIES TO ASSESS MOS-DEVICE DEGRADATION DUE TO IMPULSIVE OVERSTRESSES

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ABSTRACT

The endochronic degradation of MOS devices arising from the global response of the device parameters collectively deteriorating under the repetitive influence of electrical overstresses (at subcatastrophic levels) such as electrostatic discharge (ESD), electromagnetic pulsing (EMP), etc., is quantified in terms of noise characteristics. Life-time studies depicting the degradation of a test device are presented. Computed and experimental data are furnished.

INTRODUCTION

Studies on gate-oxide degradation of electrically overstressed MOS devices subjected to ESD/EMP environments are useful to establish design-reviews required to achieve reduced device instabilities and improved performance reliability.

The effect of electrical-overstressing of gate-oxides primarily causes charge-trapping in the oxide-region together with the corresponding changes in the interface states.¹ In general, intensity, polarity and the rate of occurrence of overstressing voltages would determine the extent of damage to the insulator integrity.² While high-level zaps would cause oxide puncture(s) with catastrophic (irreversible) damages, subcatastrophic transients occurring repeatedly may cause a cumulative growth of device degradation and the time-dependent or endochronic damage of the device would be reflected in measurable parameters,³ such as trans conductance (g_m), threshold voltage (V_t), etc. Inasmuch as all the degrading device parameters are interdependent, the cohesive damage of the device should be assessed by an appropriate characteristic function which collectively represents the net physical damage due to overstressings. It is presently demonstrated that noise characteristics can depict the global representation of the stochastic variations in charge-trapping and interface generation under external overstressings; and noise measurements of degraded devices can therefore be useful for accelerated test procedures adopted in life-time modeling strategies.

THEORETICAL CONSIDERATIONS

The ESD phenomena normally encountered can be simulated by three well-established models, namely,⁴ (a) human-body model, (b) charged-device model, and (c) field-induced model. The human-body model (Fig. 1) depicts the transfer of

static from a charged individual to ground via the test device.

Charged-device⁵ model represents the bleed-off of accumulated charge upon the device-surface to ground through the pin and conductive parts of the active device (Fig. 2). The third model simulates the effect of the charge distribution and discharge when a device is exposed to a static-electric field (Fig. 3).

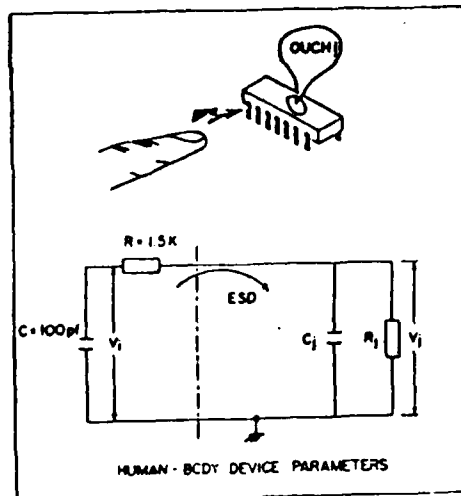


FIG 1 HUMAN-BODY MODEL

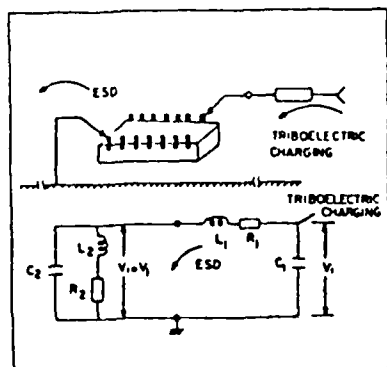


FIG 2 CHARGED-DEVICE MODEL

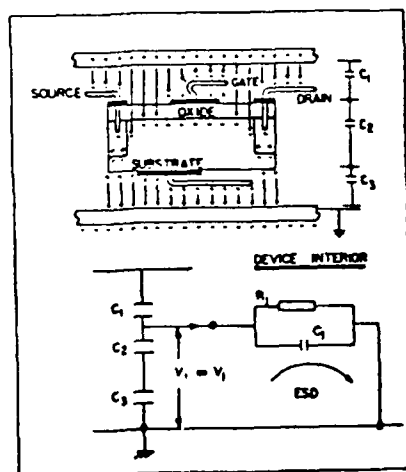


FIG 3: FIELD-INDUCED MODEL

When a MOS device is subjected to an electrical overstressing at the gate due to an impulsive transient caused by an ESD (or an EMP), the corresponding induction of charge-trapping and generation of interface states can be equivalently represented by an input noise resistance R_N given by⁶

$$R_N = \left(\frac{N_s}{4kT} \right) \left(\frac{q t_{ox}}{\epsilon_{ox}} \right)^2 \left(\frac{\mu_s}{\mu_0} \right)^2 \quad (1)$$

where k is the Boltzmann constant, T is the temperature (~ 300 K) and q is the electronic charge. Further, t_{ox} and ϵ_{ox} are the thickness and the permittivity of the gate-oxide, respectively; N_s is the surface-state density and μ_s/μ_0 refers to the field-effect mobility to low field-mobility ratio.

Eq. (1) indicates that R_N is directly proportional to N_s concurring with the

experimental results due to Abovitz⁷ et al (Fig. 4). Hence the time-dependent history of N_s as controlled by any external overstressings can be tracked via the assessment of R_N .

The field-effect mobility is also dependent on N_s and is therefore linked^{3,8} with the device parameters g_m and V_t . Explicitly,

$$\frac{\mu_s}{\mu_0} = \frac{1}{1 + \alpha N_s} = \frac{g_m}{g_{m0}} = \frac{1}{1 + \beta(V_G - V_t)} \quad (2)$$

Here α and β are constants and g_{m0} refers to the value of g_m under unstressed conditions. Further, V_G is the applied gate potential.

From Eq. (1) and (2), the following relation can be obtained:

$$\frac{\Delta R_N}{R_N} = \frac{\Delta g_m}{g_m} \left[2 - \frac{1}{\beta V_t (V_G - V_t)} \right] \quad (3)$$

The constant β has the approximate values of 0.138 and 0.308 for the n-channel and p-channel MOSFETs, respectively.⁸

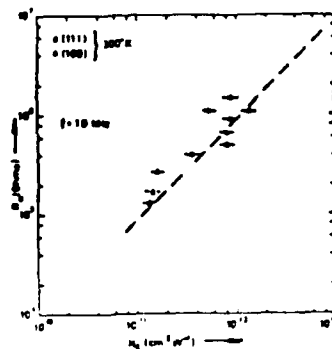


FIG 4 SURFACE STATE DENSITY VERSUS NOISE RESISTANCE: MOS DEVICE (REF 7)

EXPERIMENTAL STUDIES

A typical n-channel (enhancement mode) MOSFET was subjected to subcatastrophic zaps at its gate-input using a human-body ESD simulator (Fig. 1). Variations of g_m and V_t were measured as the functions of the number of zaps. Fig. 5 illustrates the relevant results.

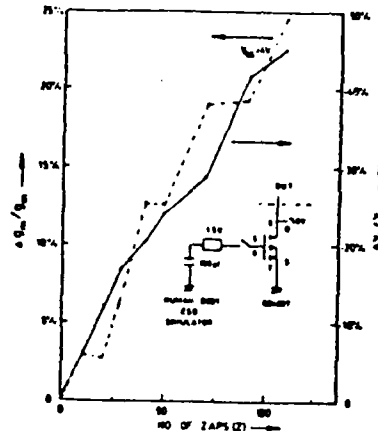


FIG. 5 VARIATION OF g_m & V_i WITH RESPECT TO NUMBER OF ZAPS

NOISE PARAMETER VERSUS AGING

Using the results presented in Fig. 5, the fractional change in R_N as a function of the number of zaps (Z) can be calculated via Eq. (3). Thus Fig. 6 depicts the relevant computed data showing that the rate of variation of R_N is approximately twice as that of g_m . Further, $\Delta R_N / R_N$ is linearly proportional to Z confirming the observations of Abovitz, et al.⁷ Hence, the present study indicates the plausibility of assessing the EOS-based degradation via noise characterization.

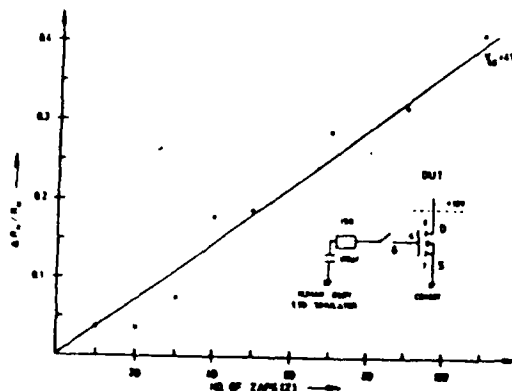


FIG. 6 INCREASE IN NOISE RESISTANCE WITH NUMBER OF ZAPS

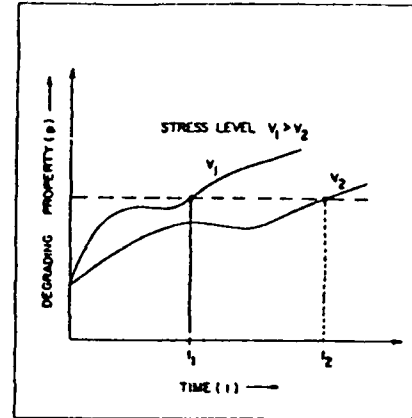


FIG. 7 DEGRADATION VERSUS TIME UNDER TWO DISTINCT STRESS LEVELS

AGING MODEL

Cumulative build-up of degradation with the recurrence of zaps amounts to a dormant stage of failure during which the device would exhibit a performance degradation leading to out-of-spec condition(s). This device-aging can be assessed by measuring the time variation of a nondestructive property (p) such as a noise parameter as indicated in the present analysis. Suppose two time-variation curves are obtained corresponding to two distinct (subcatastrophic) stress-levels. The functional form of p will be independent of the stress magnitude and the two curves will have the same shape, but different length (along the time axis) as shown in Fig. 7. The times corresponding to same (extent of) aging under two distinct stress levels can be denoted as t_1 and t_2 (Fig. 7) and are known as

"equivalent times."⁹ By the application of "equivalent aging principle," it is possible to relate the equivalent times in terms of their corresponding stress levels, namely, V_1 and V_2 .

It is given by⁹

$$V_1^n t_1 = V_2^n t_2 = K_1 \text{ (Constant)} \quad (4)$$

where n is the endurance coefficient. Eq. 4 can also be written in terms of the average numbers of zaps Z_1 and Z_2 occurred during the period t_1 and t_2 , respectively. That is,

$$V_1^n Z_1 = V_2^n Z_2 = K_2 \text{ (Constant)} \quad (5)$$

Thus, from Eq. 4 or 5, for a given severity level, the corresponding value of failure-time (or average number zaps during the period of failure-time) can be assessed by determining the values of n and K.

Further, the device reliability relevant to the endochronic degradation can be modeled by assuming that degradation rate is proportional to the existing degradation.¹⁰ The proportionality constant is a positively distributed random variable and the extent of degradation would tend to be asymptotically log-normal. Hence the general form of life distribution Z (number of zaps) is given by

$$G(Z, p_c) = 1 - \Phi \left[\frac{\ln(p_c) - \mu}{\sigma} \right] \quad (6)$$

where Φ is the standard normal distribution and $p_c = r - r_c$. Here $r = \Delta R_N / R_N$ and the suffix c depicts the critical value of r. Further $\ln(p_c)$ has a mean value of μ and a standard deviation of σ . This log-normal aspect of life-time statistics as applied to endochronic degradation has been verified by the authors (with the MOS input leakage current as the control parameter, p) and the results are presented elsewhere.¹¹

CONCLUSIONS

From the results presented here, the following conclusions can be inferred:

1. Noise parameter changes in a MOS device subjected to electrical overstressings represent the global, time-dependent degradation.
2. Such noise parameter variation expressed in terms of the fractional change in the noise resistance (R_N), is explicitly related to two major MOS-device parameters, namely, g_m and V_t (Eq. 3).
3. The rate of change of R_N with respect to the number of zaps is approximately linear.
4. Further, this rate of change of R_N is approximately twice the corresponding change in g_m .
5. Using $\Delta R_N / R_N$ as a control parameter (p), the principle of equivalent aging can be applied to MOS degradation for accelerated aging studies.
6. The degradation process can be modeled with log-normal distribution for relevant lifetime statistical analysis.

ACKNOWLEDGEMENT

This work was supported by a grant from the Office of Naval Research (No. 613-005) which is gratefully acknowledged.

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3. P.C. Hsu and S. Tam, "Relationship Between MOSFET Degradation and Hot-Electron-Induced Interface Generation," IEEE Electron Device Letters, 1984, Vol. EDL-5, pp. 50-52.
4. B. Hyatt, et al, "A Closer Look at the Human ESD Event," Proc. Electrical Overstress/Electrostatic Discharge Symp., 1981, Vol. EOS-3, pp. 1-8.
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11. P.S. Neelakantaswamy, et al, "Susceptibility of On-Chip Protection Circuits to Latent Failures Caused by Electrostatic Discharge," Solid State Electronics. (In press)

GATE-INSULATOR DEGRADATION IN MOS-DEVICES DUE TO ELECTRICAL OVERSTRESSINGS:

CHARACTERIZATION VIA NOISE PERFORMANCE STUDIES

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ABSTRACT - Design-reviews required to achieve improved performance reliability warrant the assessment of gate-insulator degradation in metal-oxide semiconductors (MOS) subjected to electrical overstressing (EOS) environments involving electrostatic discharges (ESD) and/or electromagnetic pulsing (EMP). The collective response of all the degrading parameters of the stressed devices can be cohesively studied via noise performance characteristics, as indicated in the present analysis. The global influence of overstressing quantified in terms of degrading noise parameters is useful in life-time prediction efforts. Relevant test calculations and experimental data are presented.

INTRODUCTION

Assessment of gate-insulator degradation in metal-oxide semiconductor (MOS) devices caused by electrical overstresses (EOS), such as electrostatic discharge (ESD), electromagnetic pulsing (EMP), etc., is essential for necessary design-reviews required to achieve reduced device-instabilities and improved performance reliability.

The primary effect of electrical overstressing is to cause a charge-trapping phenomenon in the gate-oxide film [1]. The extent of gate-oxide degradation arising from electrical overstressing would depend on the cumulative magnitude of charge-trapping and the corresponding changes in the interface-states; and hence, it is directly dependent on the intensity and rate of occurrence of electrical overstressings.

In the existing studies [1,2] on gate-oxide degradation, the parameters normally considered to characterize the influence of overstressing and the resulting charge-trapping/surface-state effects are [3], (a) device transconductance, g_m ; (b) gate-current due to pumped-in charges, I_{cp} ; (c) gate-oxide capacitance, C_{ox} ; and (d) threshold voltage, V_t . Inasmuch as the aforesaid parameters are largely interdependent, the estimation of one of these parameters (to depict the degradation) as a function of overstressing does not explicitly account for the deviatory characteristics of the rest of the parameters.

Hence, it is purported in the present investigations to develop a new and cohesive formulation in terms of noise performance of the MOS device to characterize the overall degradation due to overstressing. The noise characteristics of a MOS device would, in general, depict the collective response of all the degrading parameters. This is because the net effects of charge-trapping and the

associated occupation of surface states can be viewed as random/fluctuating phenomena which manifest as the device-noise with a typical $1/f$ type power-spectrum. That is, noise characterization would present the global influence of overstressing unlike the other parameters (specified earlier) which would rather represent the partial effects only.

In the present studies, an analytical formulation relating the charge-trapping and the electrical overstressing is derived in terms of an equivalent noise resistance. Measured data acquired from a typical MOS integrated circuit subjected to electrical overstressings are presented.

ANALYSIS

The ESD phenomena normally encountered can be simulated by three well-known models, namely, (a) human-body model [4], (b) charged-device model [5], and (c) field-induced model [6]. The human-body model (Fig. 1) depicts the transfer of static from a charged individual to ground via the test device. Charged device model represents the bleed-off of accumulated charge upon the device-surface to ground through the pin(s) and conductive parts of the active device (Fig. 2). The third model simulates the effect of the charge distribution and discharge when a device is exposed to static electric field (Fig. 3).

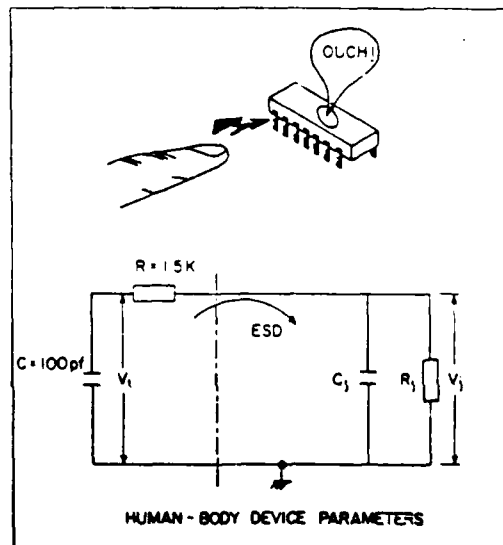


FIG 1 : HUMAN-BODY MODEL

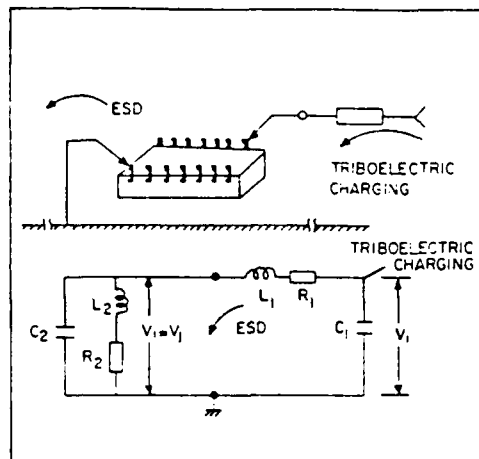


FIG 2 CHARGED-DEVICE MODEL

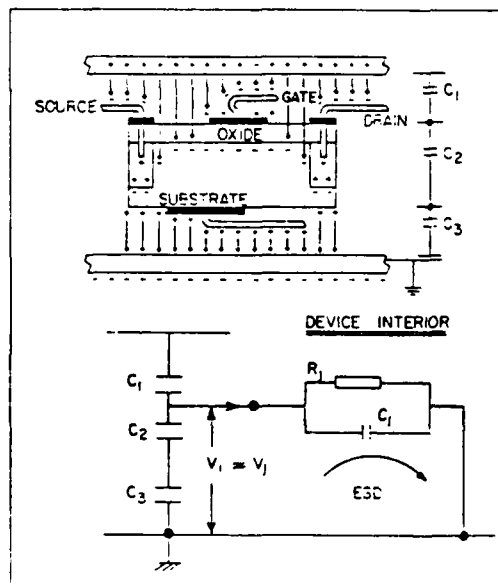


FIG 3 FIELD-INDUCED MODEL

When a MOS device is subjected to electrical overstressings at the gate due to impulsive transients caused by electrostatic discharges (ESD), the corresponding induction of charge-trapping and generation of interface-states can be specified in terms of the stochastic aspects of charge-accumulation represented by the device noise characteristics. Than is, under identical pumped-in current by repetitive transients, Leventhal [6] has shown that the resulting input noise resistance R_N is given by

$$R_N = \left(\frac{1}{4kT} \right) \left(\frac{q t_{ox}}{\epsilon_{ox}} \right)^2 \left(\frac{N_s \mu_s^2}{\mu_o^2} \right) \quad (1)$$

where k is the Boltzman constant, T is the temperature (~ 300 K) and q is the electronic charge. Further, t_{ox} and ϵ_{ox} are the thickness and

permittivity of the gate-oxide, respectively; N_s is the surface-state density and μ_s / μ_o refers to the field-effect mobility to low-field mobility-ratio.

Eqn. (1) indicates that R_N is directly proportional to N_s concurring with the experimental results due to Abovitz, et al [7], (Fig. 4). Hence the endochronic history of N_s as dictated by external overstressings can be tracked via noise parameter measurements.

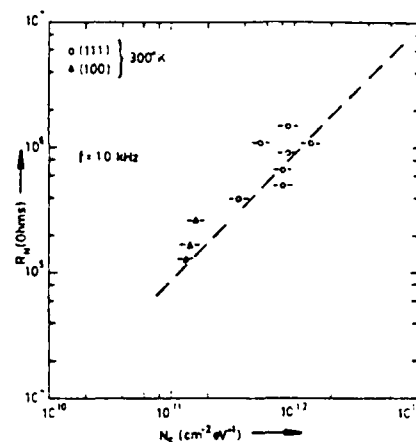


FIG 4 SURFACE STATE DENSITY VERSUS NOISE RESISTANCE: MOS DEVICE (REF. 7)

The field-effect mobility is itself dependent on N_s as well as on the other device parameters, namely, the transconductance (g_m) and the threshold voltage (V_t). Explicitly, by using the results of Hsu and Tam [3] and Akers, et al [8], one obtains

$$\frac{\mu_s}{\mu_o} = \frac{1}{1 + \alpha N_s} = \frac{g_m}{g_{m0}} = \frac{1}{1 + \beta(V_g - V_t)} \quad (2)$$

where α and β are constants and g_{m0} refers to g_m under unstressed conditions. Further, V_g is the applied gate potentials.

Combining Eqs. (1) and (2), the following relation is obtained for the fractional values of R_N , V_t and g_m .

$$\frac{\Delta R_N}{R_N} = \frac{\Delta g_m}{g_m} \left[2 - \frac{1}{1 - \frac{\Delta V_t}{\beta V_t} \left(\frac{1}{V_g - V_t} \right)} \right] \quad (3)$$

EXPERIMENTAL STUDIES

A typical n-channel (enhancement mode) MOSFET was subjected to subcatastrophic saps at its gate-input using a human-body simulator (Fig. 1). Variations of g_m and V_t measured as the functions of the number of saps. Fig. 5 illustrates the relevant results.

endocronic degradation has been verified by the authors (with the MOS input leakage current as the control parameter, p) and the results are presented elsewhere [11].

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