(12)

RADC-TR-86-217
Final Technical Report
February 1987

SILICON OXYNITRIDE STABILITY

Westinghouse Electric Corporation

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REPORT DOCUMENTATION PAGE

1a REPORT SECURITY CLASSIFICATION UNCLASSIFIED	1b RESTRICTIVE MARKINGS N/A
2a SECURITY CLASSIFICATION AUTHORITY N/A	3 DISTRIBUTION / AVAILABILITY OF REPORT Approved for public release; distribution unlimited.
2b DECLASSIFICATION / DOWNGRADING SCHEDULE N/A	
4 PERFORMING ORGANIZATION REPORT NUMBER(S) N/A	5 MONITORING ORGANIZATION REPORT NUMBER(S) RADC-TR-86-217
6a NAME OF PERFORMING ORGANIZATION Westinghouse Electric Corporation 6b OFFICE SYMBOL (If applicable)	7a NAME OF MONITORING ORGANIZATION Rome Air Development Center (RBRP)
6c ADDRESS (City, State, and ZIP Code) Advanced Technology Division, MS 3531 Baltimore MD 21203	7b ADDRESS (City, State, and ZIP Code) Griffiss AFB NY 13441-5700
8a NAME OF FUNDING / SPONSORING ORGANIZATION Rome Air Development Center 8b OFFICE SYMBOL (If applicable) RBRP	9 PROCUREMENT INSTRUMENT IDENTIFICATION NUMBER F30602-84-C-0084
8c ADDRESS (City, State, and ZIP Code) Griffiss AFB NY 13441-5700	10 SOURCE OF FUNDING NUMBERS PROGRAM ELEMENT NO: 62702F; PROJECT NO: 2338; TASK NO: 01; WORK UNIT ACCESSION NO: 4C

11 TITLE (Include Security Classification)
SILICON OXYNITRIDE STABILITY

12 PERSONAL AUTHOR(S)
Paul G. McMullin, John W. Dzimianski, Jin S. Kim* (See Reverse)

13a. TYPE OF REPORT	13b TIME COVERED	14 DATE OF REPORT (Year, Month, Day)	15 PAGE COUNT
Final	FROM Aug 84 TO Jun 86	February 1987	60

16 SUPPLEMENTARY NOTATION
N/A

17 COSATI CODES			18 SUBJECT TERMS (Continue on reverse if necessary and identify by block number)
FIELD	GROUP	SUB-GROUP	Dielectric Breakdown; Ramp Test; Silicon Oxynitride
14	04		
20	12		

19 ABSTRACT (Continue on reverse if necessary and identify by block number)

The objective of the program was to study the stability and failure mechanism of oxynitride dielectric film of 5 to 30 nanometer thickness under various stresses of interest. Initially, a survey of the literature was carried out on silicon oxynitride thin films, their physical characteristics and important parameters affecting stability or electrical properties. Two types of silicon oxynitride test structures were fabricated. The first type consisted of various size aluminum dot capacitors. The second type provided insulated gate field effect transistor with a series of different channel lengths and a group of test capacitors with polysilicon electrodes. Electrical tests on the capacitor structures included ramp voltage breakdown measurements, C-V measurements, observation of tunneling current and stability of the oxynitride to passing of current. Characterization curves were taking on some of the sample transistor with silicon oxynitride gate dielectric. It was concluded from the study that the intrinsic breakdown strength of the nitrided silicon dioxide was about 10 percent greater than that of the thin gate oxide prior to nitridation. C-V analysis showed a

20 DISTRIBUTION / AVAILABILITY OF ABSTRACT ☐ UNCLASSIFIED/UNLIMITED ☒ SAME AS RPT ☐ DTIC USERS	21 ABSTRACT SECURITY CLASSIFICATION UNCLASSIFIED
22a NAME OF RESPONSIBLE INDIVIDUAL Clyde H. Lane	22b TELEPHONE (Include Area Code) (315) 330-4102 22c OFFICE SYMBOL RADC (RBRP)

DD FORM 1473, 84 MAR 83 APR edition may be used until exhausted
All other editions are obsolete

building of positive charge in the dielectric during nitridation cycle of one hour at 1000°C, and uncharged dielectric for a 2-hour nitridation cycle at 1000°C; and an apparent negative charge in the dielectric for a 5-hour nitridation at 1000°C. Stressing of the silicon oxynitride dielectric by tunneling current resulted in accumulation of negative charge by electron capture at neutral traps; however, samples subjected to a 1-hour nitridation at 1000°C showed positive charging which was attributed to non-thermal activation of chemical processes in the dielectric. Recommendations derived from this program suggest a further study of methods and processes to reduce the defect density in oxynitride film; a determination of the optimal process and quality obtainable for oxynitride film fabricated at 900°C; and a study comparing stress testing by tunneling current with radiation hardness testing.

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1.0 INTRODUCTION

The growth of reliable, high quality gate dielectric in the 10 to 30 nanometer (nm) thickness range is of great importance for implementing VLSI MOS structure in the submicron range. Thermally grown silicon dioxide films have been the prime gate insulator material used in insulated gate field effect transistor (IGFET) structure to date. However, technological and reliability problems escalate for very thin silicon dioxide. The growth of high-quality very thin silicon dioxide is rather difficult because of defect density, integrity, and yield problems. Also very thin layers of thermal silicon dioxide are poor masks against impurity diffusion and as a consequence constraints on the processing steps following the growth of gate oxides are required. The tendency of thin silicon dioxide films to react with electrode material further limit its application.

The inadequate properties of very thin silicon dioxide have resulted in search for a more reliable and better very thin insulators to replace silicon dioxide in VLSI IGFETs. A possible gate dielectric candidate that is being studied by a number of people is silicon oxynitride thin film dielectric that is formed from an initial thermal silicon dioxide by thermal nitridation in an ammonia ambient. Silicon oxynitride is attractive because of its resistance to impurity diffusion, high dielectric breakdown strength, good process yield, and is readily producible in film thicknesses ranging from a few nm to more than 50nm. Also, silicon oxynitride has a high radiation tolerance.

The objective of the program covered in this report was to study the stability and failure mechanism of oxynitride dielectric films of 5.0 to 30.0 nanometer thickness under various stresses of interest. During the period of the contract, the effort was focused on the following areas.

1. Survey of the literature on silicon oxynitride thin films, their physical state and the important parameter affecting stability and electrical properties.

2. Fabrication of two types of silicon oxynitride test structures. The first type consisted of various size aluminum dot capacitor

structures. The second type had insulated gate field effect transistor with a series of different channel lengths. Also, a series of test capacitors with polysilicon electrodes.

3. Electrical testing of the silicon oxynitride test structures. These included ramp voltage breakdown tests, C-V measurements, observation of tunneling current, and tunneling current stress testing of the test capacitors, and characterization of sample transistors.

2.0 SILICON OXYNITRIDE TEST STRUCTURES

2.1 SILICON OXYNITRIDE FORMATION

Oxynitride layers were grown and characterized in two kinds of runs. In the experimental runs, thin gate oxides were grown on unpatterned substrates at the (W) R&D Center, and the oxides were immediately nitrided. The device lot runs, on the other hand, were processed at (W) Advanced Technology Laboratory (ATL) to completion of the gate oxide growth, then carried to the R&D Center for nitridation. After cleaning and nitridation, the device lot wafers were returned to ATL for completion of device fabrication and testing. The runs are shown in Table 1 and are described below.

2.1.1 Experimental Runs

Several types of substrates were used for oxynitride layer experiments. The early experimental runs TR900, TR1000, and TR1100, used 0.1 ohm-cm p type Czochralski wafers from existing stock. The oxygen content of the wafers was not specified in the order and was not measured. All later experimental runs included wafers that were characterized as part of the preceding program on dielectric reliability. Such wafers are labelled with prefix A, for the n type float zone; B, for the p type medium oxygen Czochralski; and C, for the n type high oxygen Czochralski. All of the A, B, and C wafers were of 10 ohm-cm resistivity. Additional wafers in the later runs, given prefix H, were 10 ohm-cm Czochralski material with no oxygen specification, but a normal oxygen content ranging 28 to 32 ppm, old ASTM, according to the vendor.

The wafers were prepared for processing by a conventional surface clean comprising solvent rinses, chelating with ammonium hydroxide and hydrogen peroxide, further chelating with hydrochloric acid and hydrogen peroxide, and a final dip in hydrofluoric acid, followed by DI water rinse and drying in clean nitrogen. Aside from a few wafers in early runs, all of the experimental wafers were then thermally oxidized at 1000°C for 52 minutes in dry oxygen. This initial oxide, about 50 nm thick, was then etched away in HF immediately before the thin gate oxide step. Comparisons of gate oxides grown on wafers with and

Table 1. NITRIDATION RUNS

EXPERIMENTAL RUNS

RUN NUMBER	TEMPERATURE	TIME
TR900	900°C	5 HR
TR1000	1000°C	2
TR1100	1100°C	2
OXIN3	1100°C	2
OXIN4	1000°C	2
OXIN5	1100°C	2
OXIN6	1000°C	1
OXIN7	1000°C	5
OXIN8	1000°C	5
OXIN9	1000°C	2
(OXIN9) Reoxidized	1000°C	0.5 (Dry 02)
DEVICE LOT RUNS		
DEVL1	1000°C	2
DEVL2	1100°C	2
DEVL3	1000°C	2
DEVL4	1100°C	2

without the sacrificial initial oxide did not show any difference in characteristics. The sacrificial oxide step was continued, however, as being a more conservative approach to surface cleaning before thin gate oxidation.

The gate oxidation began with the stripping of the sacrificial oxide in fresh 1:1 HF:H20 in a precleaned quartz beaker. The wafers were then rinsed for 15 minutes in DI water, and blown dry with clean nitrogen. The wafers were then inserted in the furnace, and brought to temperature in flowing nitrogen. Dry oxygen gas was turned on for the run duration, which was 30 minutes at 900°C for the earliest experimental runs, and 40 minutes at 900°C for the later runs. Following oxidation, the wafers were annealed in nitrogen for 10 minutes, then moved to the cold zone and cooled in flowing nitrogen.

The nitridation cycles were performed immediately after oxidation for all experimental runs. The wafers were inserted in nitrogen purge gas, brought to temperature in nitrogen, then nitrided in 99.999 per cent pure annhydrous ammonia. Following the nitridation, the wafers were annealed for 15 minutes in nitrogen. One experimental run, OXIN9 was reoxidized by replacing the wafers in the hot zone at 1000°C, flowing dry oxygen for 30 minutes, followed by a 15-minute anneal in nitrogen.

The experimental wafers were metallized with 1μm of E-beam evaporated aluminum, patterned into C-V dots of various sizes, and sintered at 450°C in hydrogen for 30 minutes, prior to testing.

2.1.2 Device Lot Runs

The substrates for all device lot runs were selected from the previously characterized wafers. In each lot, wafers 1-4 correspond to the type A experimental wafers, i.e., nFZ, wafers 5-8 are Type B, pCZ medium oxygen, and wafers [illegible] are type C, nCZ high oxygen. The wafers were transported to the (W) R&D Center in fluoroware cases. To ensure a properly cleaned surface, the run wafers were given the solvent rinse and chelating cleaning cycle that was used for the experimental wafers, omitting the final HF dip. The cleaned wafers were rinsed in DI water, blown dry with clear nitrogen, and inserted into the

furnace. The wafers were brought to temperature in nitrogen, and then nitrided for the indicated time and temperature in flowing ammonia. After the nitridation, the wafers were annealed for 15 minutes in nitrogen, cooled in nitrogen, and replaced in the fluoroware cases for return to ATL. Each of the device lots was split between 1000°C, 2 hr, and 1100R, 2 hr nitridations. In the split, two wafers from each wafer type were taken for each nitridation cycle, so that for example, p CZ wafers 5 and 6 received a 1000°C cycle, while p CZ wafers 7 and 8 were nitrided at 1100°C. In Table 1, the run numbers DEVL1 and DEVL2 refer to the splits of the first lot of wafers from ATL and DEVL3 and DEVL4 refer to the second lot of wafers.

2.1.3 Composition of Nitrided Layer

The nitridation process involves replacement of oxygen by nitrogen in the silicon dioxide. The replacement process is driven by the abundant supply of nitrogen from the process gas, while the limited supply of oxygen in the dielectric is depleted by loss at the surface or reaction at the silicon interface. The conversion is not uniform in the depth of the film. Increased nitrogen content is observed at the surface and at the interface regions, while the central bulk portion of the film typically has a lower concentration. The bulk portion of the film comprises the greatest volume fraction, compared to surface or interface regions, and can be expected to have a predominating influence on the film properties.

To characterize the oxynitride films prepared for this program, several samples were submitted for Auger Electron Spectroscopic (AES) analysis. The samples are listed in Table 2 and the profiles are shown in Figures 1 and 2. Our data typically show a relatively high nitrogen concentration at the surface, a decreased concentration below the surface, and a broad internal maximum in nitrogen concentration. The bottom interface is not well defined in any of our data. This is due to the formation of a rough surface during the sputtering run, because of the differing sputtering rates of the dielectric material and the silicon substrate. As a result, we do not observe the local peak of nitrogen concentration at the interface that others have reported. A comparison of our results with others is shown in Figure 3. In the Figure, the bulk

Table 2. SAMPLES PROFILED BY AUGER ELECTRON SPECTROSCOPY

SAMPLE NUMBER	NITRIDATION CONDITIONS TEMPERATURE	TIME
A3	1100°C	2 hr
B3	1100	2 hr
C3	1100	2 hr
B7	1100	2 hr
A5	1000°C	2 hr
B5	1000	2 hr

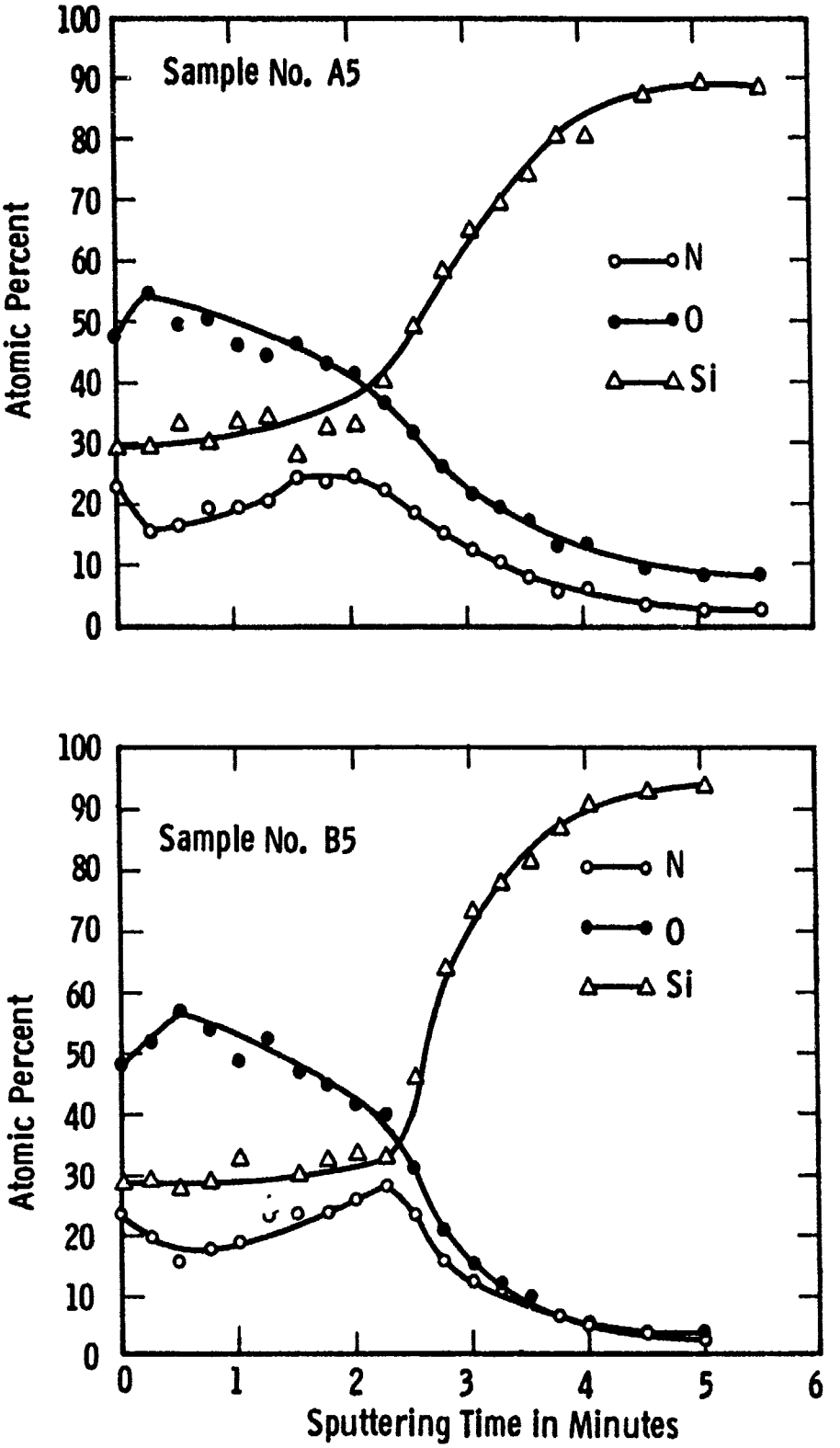

Fig. 1 – Auger profiles for samples nitrided at 1000°C for 2 hours

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Curve 752260-A

Curve 752261-B

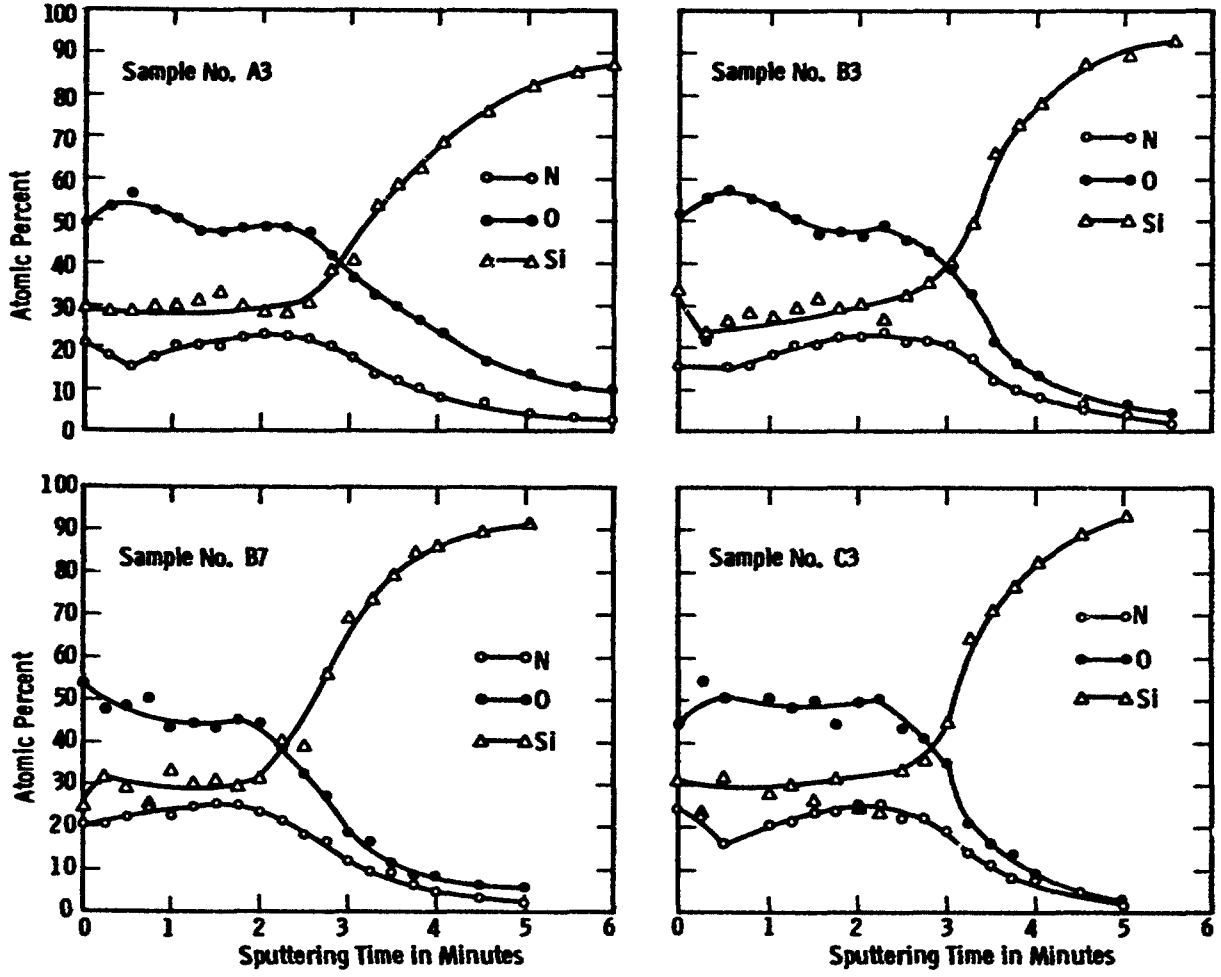

Fig. 2. – Auger profiles for samples nitrided at 1100°C for 2 hours

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Curve 752261-B

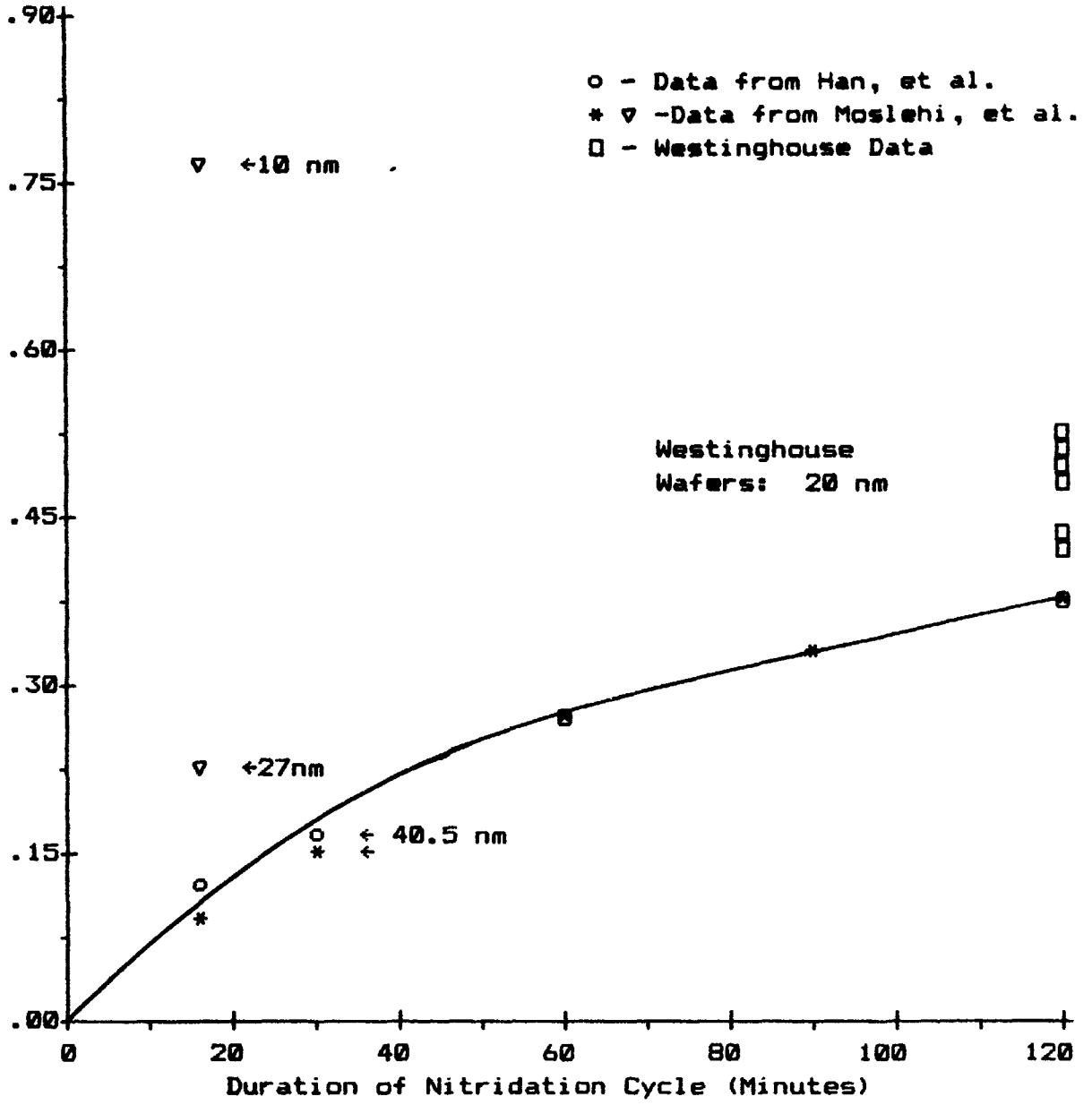

Figure 3. Comparison of the composition of the bulk regions of the oxynitride layer for different nitridation cycles.

composition of various oxynitrides, as reported by Han[1] and Moslehi[2], is shown plotted against the duration of the nitridation cycle, for nitridation at 1100°C. The data points for our samples all lie above the curve for the 40.5nm thick layer, indicating the greater replacement of oxygen by nitrogen in our thinner 20nm layers.

2.1.4 Estimation of Oxynitride Film Thickness

Measuring the thickness of a 20 nm oxynitride film is a difficult task. The conventional ellipsometer method is not sensitive enough to simultaneously determine both film thickness and index of refraction for such thin films. Attempts to do so give a "bad data" response, or thickness and index values that are obviously spurious. Stable, repeatable ellipsometer thickness data can be obtained if the layer index is given a fixed value. All of the layer thickness ellipsometer data for this program has been taken using the same index value, 1.458, used for measurement of thin oxide films. However, since the index of refraction is known to increase upon nitridation, this data represents an overestimate of the true film thickness. In this section, a method of estimating the true film thickness is described.

The optical thickness of a dielectric layer is the product of the physical thickness and the index of refraction. It is assumed that the oxynitride layer has the optical thickness determined by the ellipsometer measurement using the fixed oxide index. Then the true layer thickness d is given by

$$d = \frac{n_{ox}}{n_{nit}} \cdot t_{ell} = t_{ell}/b$$

---

1. C. J. Han, M. M. Moslehi, C. R. Helms, and K. C. Saraswat, "Time Dependent Compositional Variations in Silicon Dioxide Films Nitrided in Ammonia," Appl. Phys. Lett. 46:G42 (1985).

2. M. M. Moslehi, and K. C. Saraswat, "Thermal Nitridation of Si and SiO2 for VLSI," IEEE J. Sol. State Circuits, SC-20:26 (1985).

where t_{ell} is the indicated thickness using fixed oxide index of refraction, and the oxynitride index n_{nit} is assumed to be a factor b greater than the oxide index n_{ox}. Next, b is determined from capacitance data. The capacitance C of an MOS dot of area A is given by

$$C = \epsilon A/d$$

The optical dielectric constants are related by the factor b through $\epsilon_{nit} = n^2_{nit} = b^2\epsilon_{ox}$ and it is assumed that the same relationship holds true at the frequency of the capacitance measurement. The capacitance data can be expressed as

$$d = b^2\epsilon_{ox} A/C = b^2 t_{CV}$$

where t_{CV} is the layer thickness calculated using the oxide dielectric constant. Combining the expressions to eliminate the unknown ratio b gives the final estimator of film thickness

$$d^3 = t_{CV}\, t^2_{ell}$$

Thus the capacitance thickness is a lower bound for the true thickness, the ellipsometer reading is an upper bound, and the estimated value is the geometric mean as shown.

Table 3 shows a compilation of data from the most recent nitridation runs. Each run is represented by a wafer of Type A (n_{FZ}), Type B (p_{CZ}, standard oxygen), type C (n_{CZ}, high oxygen), and type H (p_{CZ}, standard oxygen). Wafer A 11 is absent because no good capacitors were found on the wafer section tested. Also included are two wafers, H1 and H10, with oxide films, showing about a 5 per cent error in the consistency of the estimate. Table 4 summarizes the data by runs. The average correction factor is shown for each run, together with the nitridation conditions. The correction is least for the reoxidized run, greater for the shortest nitridation, slightly larger for the 2-hour nitridation, and substantially greater for the longest nitridation. This is consistent with a change in the dielectric constant that increases with increasing nitrogen content in the film.

Table 3. ESTIMATED OXYNITRIDE FILM THICKNESS
(NANOMETERS)

Run	Wafer	Capacitance Thickness tcv	Ellipsometer Thickness tell	Estimated Thickness d	Correction Ratio d/tell
OXIN6	A9	14.16	19.4	17.47	.81
	B9	15.75	18.2	17.34	.91
	C9	19.48	23.2	21.89	.89
	H3	18.93	20.5	19.96	.95
OXIN7	A10	14.08	20.0	17.79	.79
	B10	18.02	23.3	21.39	.84
	C10	18.02	26.3	23.18	.78
	H6	19.93	25.1	23.24	.86
OXIN8	B11	16.39	19.0	18.09	.91
	C11	15.01	20.0	18.18	.83
	H9	19.09	22.9	21.55	.89
OXIN9	A12	20.85	24.0	22.9	.91
	B12	29.25	33.8	32.2	.91
	C12	24.75	27.3	26.42	.94
	H12	21.25	21.9	21.68	.98
Oxides	H1	20.36	19.0	19.44	1.05
	H10	38.83	41.5	40.59	.96

Table 4. ESTIMATED THICKNESS CORRECTION FACTORS

Run	Nitridation Conditions		Correction Factor
OXIN6	1000°C	1 hour	89
OXIN7	1000°C	5 hours	.82
OXIN8	1000°C	2 hours	.87
OXIN9	1000°C	2 hours	.94
Reoxidized	1000°C	30m Dry O2	

2.2 MOS CAPACITOR TEST PATTERN

A new mask was used for rapid turnaround fabrication of MOS capacitors for electrical testing. The test pattern comprised octagonal dots ranging in diameter from 100 to 1000 micrometers, in logarithmic steps. The dot diameters are 100, 178, 316, 562, and 1000 microns, for nominal dot areas of 8.3E-5, 2.6E-4, 8.3E-4, 2.6E-3, and 8.3E-3 cm^2, respectively. The dots are arranged in cells each labeled with a letter and number for positive identification of each test site. Figure 4 shows the pattern arrangement. Each cell has five 100 μm dots, five 178 μm dots, five 316 μm dots, two 562 μm dots, and three 1000 μm dots.

2.3 TRANSISTOR TEST PATTERN

The transistor test structure chip provided two types of devices: polysilicon-silicon oxynitride-silicon capacitors, and n-channel insulated gate field effect transistors (IGFETs) with silicon oxynitride dielectric and a polysilicon gate. A total of 27 capacitors and 20 IGFETs were fabricated on each test pattern using 2 micrometer (μm) design rules. Table 5 lists the devices and their dimensions. A body or substrate contact is provided for each device. Figure 5 shows a complete test pattern cell.

The capacitor size and shape varied from 50 μm x 100 μm to 3000 μm x 3333 μm. Among these capacitors, a set of 10 square capacitors (1000 μm x 1000 μm) were used for the electrical breakdown tests. The long, narrow capacitors were included for possible testing of enhanced dielectric breakdown at the capacitor perimeters.

All of the IGFETs in the test pattern have a fixed channel width of 40 μm. The channel length varies from 1 μm to 20 μm. Figure 6 shows a typical IGFET.

2.3.1 Transistor Test Pattern Wafer Processing

Two lots consisting of 12 3-inch wafers each, were processed using part of Westinghouse CMOS processing technology. The lot-wafer mix is shown in Table 6.

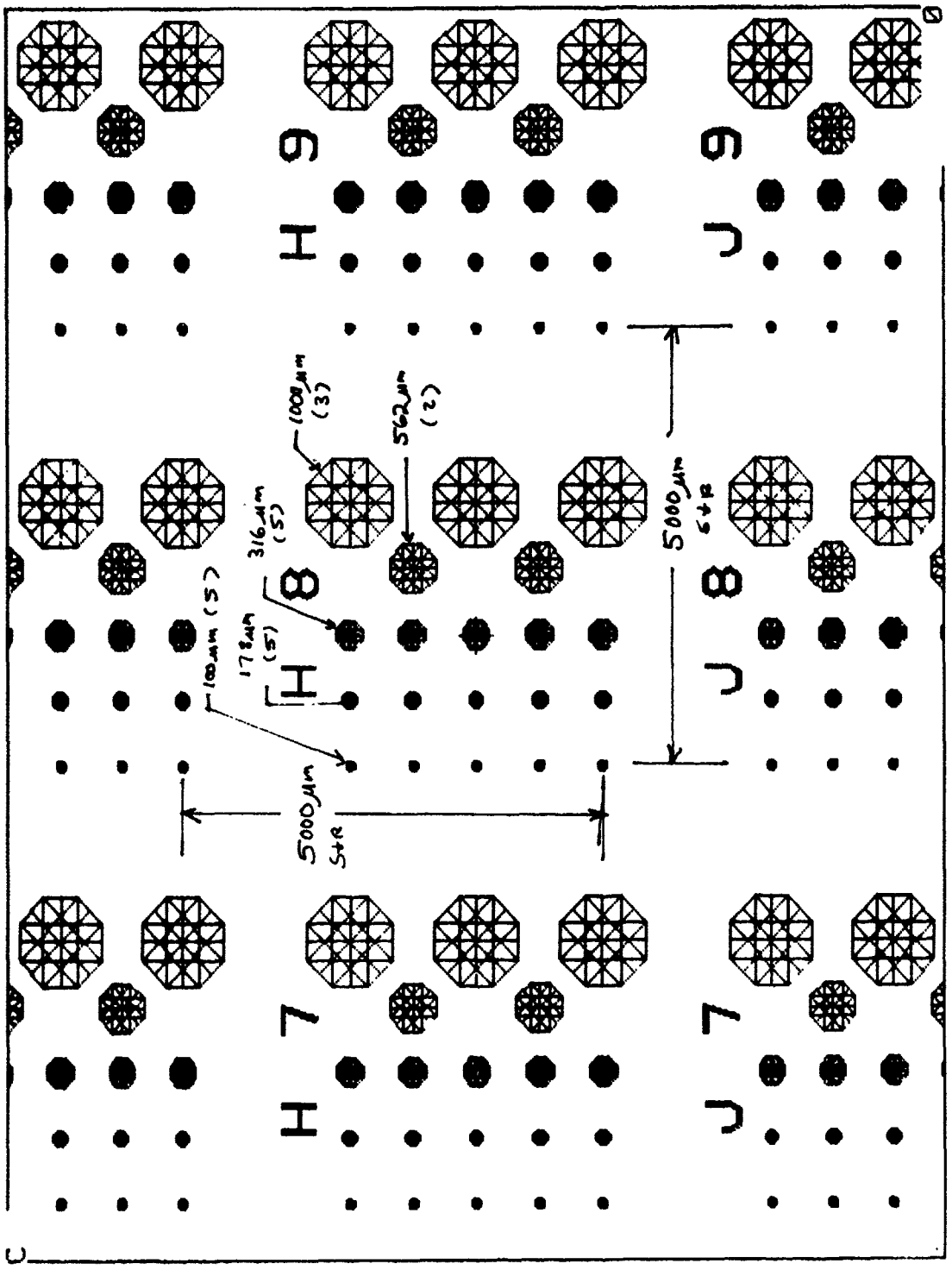

Figure 4. MOS CAPACITOR TEST PATTERN

Table 5. LIST OF DEVICES IN THE TEST PATTERN

MOS Capacitors:	
Size (μm^2)	Number
1000x1000	10
3333x3000	1
3000x2000	1
2000x2000	1
4000x1000	1
4000x500	1
4000x250	1
4000x125	1
2000x1000	1
2000x500	1
2000x250	1
2000x125	1
16300x100	1
8300x100	1
4100x100	1
4050x50	1
8150x50	1
12250x50	1

MOSFETs:		
Channel Length (μm)	Channel Width (μm)	NO.
20	40	2
15	40	2
10	40	2
8	40	2
5	40	2
4	40	2
3	40	2
2	40	2
1.5	40	2
1	40	2

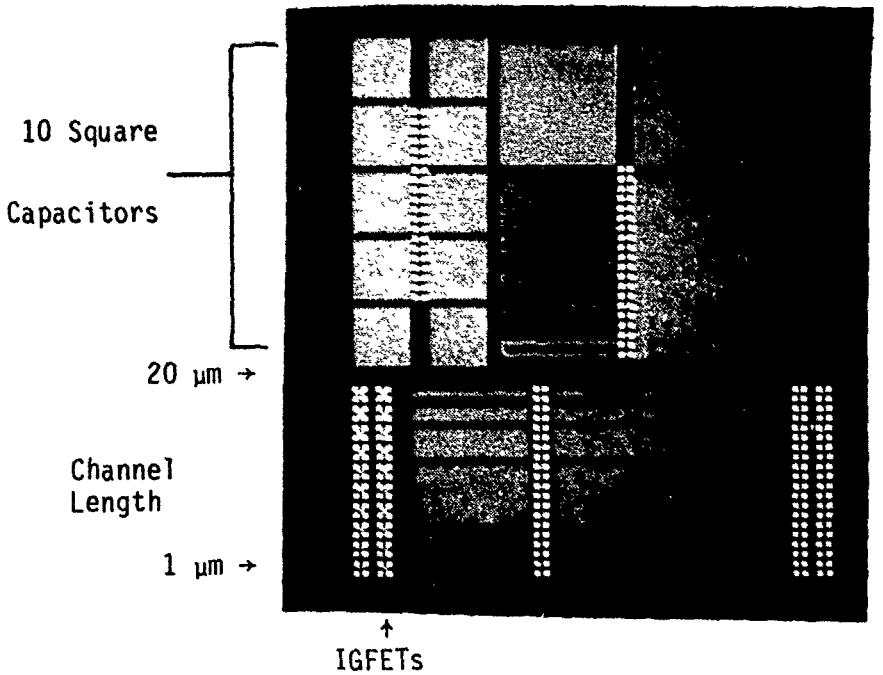

Figure 5. TEST PATTERN CELL

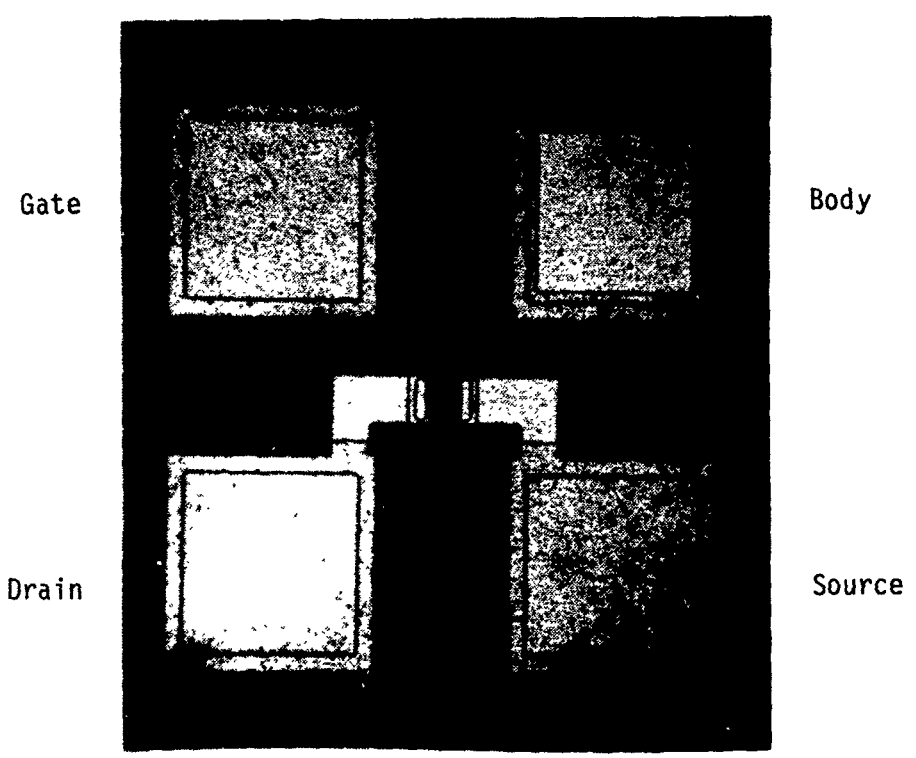

Figure 6. PICTURE OF TYPICAL IGFET

Table 6. LOT WAFER MIX

Wafer Type	Wafer Number
Float Zone, N-type (Low Oxygen)	1-4
Czochralski, N-type (Medium Oxygen)	5-8
Czochralski, P-type (High Oxygen)	9-12

The processing required seven photo steps using five different photomasks and six ion implant steps. Table 7 shows an overview of the key processing steps

Table 7. KEY PROCESS STEPS

1.	Body Implant	Boron, $2x10^{13}$, 60KeV, thru 20nm oxide
2.	Drive-in/Anneal	1150°C, 8 hrs., Xj = 2.7 μm
3.	Field Oxide	1000°C, 100 minutes, 330nm
4.	Gate Oxide	Dry O_2, Target 15nm
5.	Nitridation	2 hrs. at 1000°C or 1100°C
6.	Polysilicon Deposition	650nm, 9.7$\Omega/\square$
7.	Source/Drain Implant	Arsenic, $1.4x10^{15}$ 80KeV, thru 20nm oxide
8.	Silox Deposition	500nm
9.	Silox Densification	900°C, 30 minutes
10.	Source/Drain Contact Implant	Phosphorous, $1.4x10^{15}$, 80KeV, plus Phosphorous, $2x10^{14}$, 140KeV
11.	Body Contact Implant	Boron, $4x10^{14}$, 80KeV plus Boron, $4x10^{13}$, 140KeV
12.	Anneal	900°C, 30 minutes
13.	Metallization	Al/Si, 700nm

N+ polysilicon was used as gate or capacitor electrode. Dry oxide followed by nitridation in an ammonia ambient, as discussed in section 2.1, was used to form transistor gate and capacitor dielectric. The dry oxide in the gate area was grown after a 350-400nm field oxide was etched away in the active device area to eliminate the bird beak or Kooi effect. Also, wet oxide for the field oxide, silox for isolation of metal lines and Al/Si for metallization were employed.

The dopant concentration in the body (tub) of the IGFET and under the gate electrod of the capacitor was determined primarily by a single ion implant of $2x10^{13}$ @ 60KeV followed by a drive-in anneal of 8 hours @ 1150°C. This implant and drive-in anneal process provided a $2\mu m$ thick layer p-region of approximately $8x10^{16}/cm^3$.

The drain/source were formed by a single shallow implant through the gate dielectric of arsenic $1.4x10^{15}$ @ 80KeV, while the drain/source contacts were formed by two successive implants through the contact windows of phosphorous to $1.4x10^{15}$ @ 80KeV plus phosphorous of $2x10^{14}$ @ 140KeV. The body (tub) contacts utilized two successive implants of boron to $4x10^{14}$ @ 80KeV plus boron to $4x10^{13}$ @ 140KeV. These implants were followed by an activation anneal for 30 minutes @ 900°C in N_2 gas.

The gate and capacitor dielectric layers were formed by growing an oxide in dry oxygen at 900°C. Then, this oxide was subjected to a nitridation cycle in ammonia for two hours, where wafers 1,2,5,6,9,10 were heated at 1000°C and wafers 3,4,7,8,11,12 were heated at 1100°C.

3.0 TESTING

3.1 WAFER OXYGEN CONCENTRATION

The interstitial oxygen concentration was measured on selected wafers as part of an earlier program[3]. Oxygen determinations were carried out by the method of infrared absorption. Each wafer was mounted in a Nicolet model 7000 Fourier Transform Infra Red (FTIR) spectrometer for measurement of the magnitude of the oxygen absorption peak at 1105 cm-1. The infrared beam diameter is about 3 μm, located at the center of the wafer. The background silicon absorption was subtracted by using a purified silicon wafer as a reference standard. The reference wafer was a float-zone sample that had been subjected to six-pass zone refining and had been characterized for extremely low levels of oxygen and carbon. The Nicolet instrument utilizes digital signal acquisition and data storage for drift-free long term signal averaging. The stored data was analyzed using the built-in data processing capability of the Nicolet to subtract the interference fringes due to sample and reference wafer thickness, to subtract the silicon baseline, and to compute the absorbance at the oxygen peak. Absorbance A is defined as

$$A = \log I_o/I_t$$

where I_t is the transmitted intensity at the wavelength of the oxygen peak, and I_o is the incident intensity. The absorbance is related to the absorption coefficient α by

$$\alpha = \frac{1}{t} \ln \frac{I_o}{I_t} = \frac{2.30A}{t}$$

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[3] Final Technical Report, RADC-TR-85-16, A153200.

where t is the sample thickness in centimeters. The thickness t is taken as 508 micrometers, which corresponds to the nominal 20 mil thickness specification of the wafers. The thickness was checked on selected wafers by mechanical measurement and by the interference fringe pattern observed in the FTIR measurements. The thickness was within 10 micrometers of nominal, giving a maximum two percent error in a due to neglecting this source of variation.

The results of measurements on ten wafers of each type are summarized in Figure 7. The figure shows the specification range for four grades of Cz silicon as quoted at the time of the order, with the expected "typical" value shown by an X. The data for B type wafers, the medium oxygen grade, are summarized as a heavy bar showing the range of measured values, and a circle indicating the mean value of ten measurements. It can be seen that the data is tightly clustered, but lies at the top extreme of the specification range. The data for the C-type, high oxygen grade wafers, are similarly summarized, and it is seen that these wafers lie closer to the expected value near the middle of the specification range. As a result, although the B and C wafers are from non-adjacent ranges, the measured oxygen contents are very close. The mean value of oxygen content for B-type wafers is 33.5 ppmA and for C-type wafers is 37.2 ppmA, in the old ASTM calibration ($[O] = 9.63\alpha$). Several type A float zone wafers were also measured, but the oxygen content was below the detection limit of 0.5 ppmA, as expected.

3.2 CAPACITOR RAMP BREAKDOWN MEASUREMENTS

An extensive series of ramp breakdown voltage tests on the silicon oxynitride dielectric test capacitor was performed by using a Keithly automatic test system. The ramp test was made destructively at room temperature on wafers which were vacuum mounted on a test chuck. The voltage ramp used for this test ranged from 0-32 volts with a 0.2 volt increment per step and a 10 millisecond dwell time. The polarity of the electrode voltage was chosen to provide an accumulation mode for the wafer under test, thus assuring maximum voltage across the silicon oxynitride dielectric. The breakdown events were summed over the whole wafer for each size capacitor tested by the DEC PDP-11 computer of the Keithly system. The processed test information was printed out to provide the

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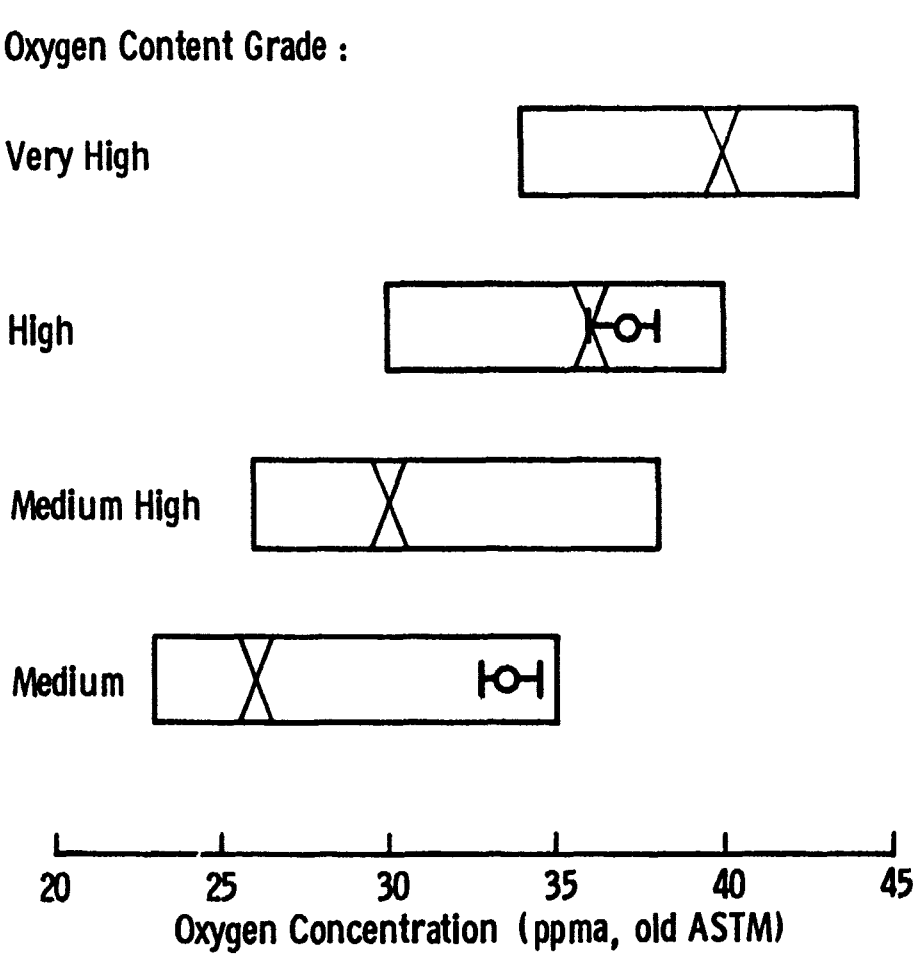

Fig. 7 —Measured oxygen content compared to vendor specification ranges

P. McMullin

Curve 748051-A

mean breakdown voltage, standard deviation and a histogram of breakdown events in each voltage range. The breakdown events near zero volts, ich are associated with gross oxide defects are of no interest and were excluded by setting a cutoff voltage of two volts in the histogram. Also, events due to open probe contacts, which piled up at the top of the range at 32 volts, were also excluded. However, analysis of the data and measured dielectric thickness in a few test wafers indicated that the breakdown voltage was greater than 32 volts and in those samples the 32 volt reading represented a limit of the test.

3.2.1 Dot Test Capacitors

As described in Section 2.2, the dot test patterns contained five different sizes of test capacitors. Ramp tests were run so as to test one capacitor of each size in each cell. This provided for up to 73 data points for each dot size per wafer. Tables 8-11 summarize the measurements.

All wafers in each of the four process cycle groups were thermally oxidized together. Then one wafer was held out while the other five wafers were subjected to a nitridation cycle. Finally, the aluminum dots were evaporated on all six wafers in the group. This was done to have a reference oxide wafer to compare with the oxynitride wafers.

Analysis of the histogram of breakdown events and the mean breakdown voltage for the different size dots indicated that the mean breakdown voltage reflected the dielectric defect densities rather than the intrinsic dielectric strength of the silicon oxynitride. To provide a better indication of the intrinsic dielectric strength of silicon oxynitride, the highest breakdown voltage level was extracted from each wafer/process type breakdown histogram and a comparison made in Table 12 of the mean breakdown field in volts per centimeter for the smallest size test capacitor and the maximum breakdown field shown in the histogram. This comparison shows that the intrinsic dielectric strength of silicon oxynitride is approximately 10% greater than the dielectric strength of thermally grown silicon dioxide.

Oxynitride Sample	Wafer Type	Dielectric* Thickness	Mean Breakdown Voltage - Nominal Size Indicated 1000μm	562μm	316μm	178μm	100μm	Oxygen
A9	N-FZ	17.3nm	6.89V ± 4.17	10.19V ± 4.81	12.14V ± 5.03	14.55V 5.09	16.12V ± 4.84	Low
B9	P-CZ	16.2nm	12.03V ± 3.23	13.19V ± 2.85	14.49V ± 3.37	15.47V 3.41	15.49V ± 3.26	Medium
C9	N-CZ	20.6nm	12.79V ± 7.64	12.51V ± 4.84	12.43V ± 6.28	13.84V 5.28	13.84V ± 5.59	High
H2	P-CZ	16.9nm	8.16V ± 4.35	11.45V ± 4.83	14.15V ± 4.37	17.08V 3.03	17.10V ± 3.58	Medium
H3	P-CZ	18.2nm	11.18V ± 3.98	12.67V ± 3.54	14.55V ± 4.18	15.72V 4.54	17.55V ± 4.72	Medium
Oxide H1	P-CZ	19.0nm	17.05V ± 4.44	18.81V ± 4.38	19.87V ± 3.79	21.19V 3.74	21.26V ± 4.46	Medium

*Silicon oxynitride dielectric thickness represents ellipsometer measured thickness adjusted for nitridation model.

Table 9. DOT CAPACITOR BREAKDOWN VOLTAGE: NITRIDATION - 1000°C/2 HOUR

Oxynitride Sample	Wafer Type	Dielectric* Thickness	Mean Breakdown Voltage - Nominal Size Indicated 1000μm	562μm	316μm	178μm	100μm	Oxygen
A11	N-FZ	18.5nm	12.03V ± 5.90	15.62V ± 5.60	17.69V ± 4.40	19.11V 5.10	20.58V ± 4.81	Low
B11	P-CZ	16.0nm	9.81V ± 4.62	11.33V ± 5.12	12.20V ± 4.93	14.32V 4.44	14.64V ± 4.46	Medium
C11	N-CZ	18.5nm	8.87V ± 4.77	13.69V ± 6.54	16.89V ± 6.29	-	-	High
H8	P-CZ	18.0nm	12.89V ± 5.43	15.76V ± 5.33	17.73V ± 5.84	19.02V 5.40	22.15V ± 4.95	Medium
H9	P-CZ	19.9nm	12.94V ± 5.96	14.38V ± 5.85	17.01V ± 5.59	19.65V 5.41	21.06V ± 5.26	Medium
Oxide H7	P-CZ	22.1nm	18.82V ± 4.99	20.55V ± 4.69	23.44V ± 1.72	24.04V 3.14	24.79V ± 2.57	Medium

*Silicon oxynitride dielectric thickness represents ellipsometer measured thickness adjusted for nitridation model.

Table 10. DOT CAPACITOR BREAKDOWN VOLTAGE: NITRIDATION - 1000°C/5 HOUR

Oxynitride Sample	Wafer Type	Dielectric* Thickness	Mean Breakdown Voltage - Nominal Size Indicated 1000μm	562μm	316μm	178μm	100μm	Oxygen
A10	N-FZ	16.4nm	5.22V ± 2.96	8.04V ± 4.03	9.80V ± 4.01	13.24V 4.38	16.05V ± 4.89	Low
B10	P-CZ	19.1nm	15.28V ± 4.68	16.93V ± 4.84	18.79V ± 4.75	21.26V 4.43	23.63V ± 3.76	Medium
C10	N-CZ	21.6nm	15.95V ± 6.08	19.69V ± 4.81	21.69V ± 3.44	22.89V 2.59	23.79V ± 2.19	High
H5	P-CZ	17.9nm	10.14V ± 4.88	11.50V ± 4.72	14.08V ± 4.86	16.21V 5.16	17.48V ± 5.05	Medium
H6	P-CZ	20.6nm	10.46V ± 4.56	14.09V ± 5.39	16.34V ± 5.81	20.18V 5.10	23.96V ± 4.58	Medium
Oxide H4	P-CZ	18.5nm	6.04V ± 7.45	6.15V ± 7.77	5.44V ± 6.13	11.08V 7.57	14.47V ± 6.90	Medium

*Silicon oxynitride dielectric thickness represents ellipsometer measured thickness adjusted for nitridation model.

Table 11. DOT CAPACITOR BREAKDOWN VOLTAGE: NITRIDATION - 1000°C/1 HOUR+ 1000°C/1 HOUR IN O_2

Oxynitride Sample	Wafer Type	Dielectric* Thickness	Mean Breakdown Voltage - Nominal Size Indicated 1000μm	562μm	316μm	178μm	100μm	Oxygen
A12	N-FZ	24.6nm	6.83V ± 2.62	10.61V ± 5.34	14.00V ± 5.60	16.99V 5.22	20.47V ± 3.79	Low
B11	P-CZ	35.7nm	3.41V ± 1.49	4.84V ± 6.34	17.93V ± 10.99	22.78V 8.70	24.19V ± 9.10	Medium
C11	N-CZ	27.6nm	4.18V ± 1.75	7.05V ± 4.16	11.65V ± 6.39	16.80V 6.40	19.75V ± 6.18	High
H11	P-CZ	32.1nm	7.16V ± 3.54	11.19V ± 8.43	17.92V ± 6.07	21.36V 6.79	22.37V ± 7.74	Medium
H12	P-CZ	22.6nm	5.94V ± 2.91	8.60V ± 3.98	13.32V ± 6.15	16.22V 6.97	20.04V ± 7.09	Medium
Oxide H10	P-CZ	41.5nm	16.16V ± 8.63	21.22V ± 7.82	24.15V ± 6.56	24.15V 7.01	26.56V ± 4.40	Medium

*Silicon oxynitride dielectric thickness represents ellipsometer measured thickness adjusted for nitridation model.

Table 12. COMPARISON OF THE SMALL DOT CAPACITOR BREAKDOWN FIELD AND THE MAXIMUM BREAKDOWN FIELD

Sample	Description	Small Capacitor Mean Breakdown Field	Small Capacitor Maximum Breakdown Field
Nitridation 1000°C/1 hr.			
A9	N-FZ	9.32×10^6 V/cm	1.41×10^7 V/cm
B9	P-CZ	9.56×10^6 V/cm	1.51×10^7 V/cm
C9	N-CZ	6.72×10^6 V/cm	1.26×10^7 V/cm
H2	P-CZ	1.01×10^7 V/cm	1.45×10^7 V/cm
H3	P-CZ	9.64×10^6 V/cm	1.51×10^7 V/cm
H1	Oxide P-CZ	1.12×10^7 V/cm	1.37×10^7
Nitridation 1000°C/5 hrs.			
A10	N-FZ	9.79×10^6 V/cm	1.50×10^7 V/cm
B10	P-CZ	1.24×10^7 V/cm	1.44×10^7 V/cm
C10	N-CZ	1.10×10^7 V/cm	1.28×10^7 V/cm
H5	P-CZ	9.77×10^6 V/cm	1.62×10^7 V/cm
H6	P-CZ	1.16×10^7 V/cm	1.41×10^7 V/cm
H4	Oxide P-CZ	7.82×10^6 V/cm	1.49×10^7
Nitridation 1000°C/2 hrs.			
A11	N-FZ	1.11×10^7 V/cm	1.40×10^7 V/cm
B11	P-CZ	9.15×10^6 V/cm	1.62×10^7 V/cm
C11	N-CZ	9.13×10^6 V/cm	1.56×10^7 V/cm
H8	P-CZ	1.23×10^7 V/cm	1.61×10^7 V/cm
H9	P-CZ	1.05×10^7 V/cm	1.38×10^7 V/cm
H7	Oxide P-CZ	1.12×10^7 V/cm	1.24×10^7
Nitridation 1000°C/1 hr. + 1000°C/1 hr. in O_2			
A12	N-FZ	8.32×10^6 V/cm	1.12×10^7 V/cm
B11	P-CZ	6.78×10^6 V/cm	$> 8.97 \times 10^6$ V/cm*
C11	N-CZ	7.16×10^6 V/cm	1.05×10^7 V/cm
H11	P-CZ	6.97×10^6 V/cm	$> 9.98 \times 10^6$ V/cm*
H12	P-CZ	8.87×10^6 V/cm	1.28×10^7 V/cm
H10	Oxide P-CZ	6.40×10^6 V/cm	$> 7.70 \times 10^6$ V/cm*

*Exceeded the 32V Test Range

Some effects of variation in the nitridation cycle can be seen in Table 13. The 2-hour nitridation cycle gives a maximum average breakdown voltage; the longer 5-hour cycle appears to have suffered some deterioration while the 1-hour cycle was insufficient to give optimum results. On the other hand, the 1-hour post bake in oxygen appear to have significantly degraded the breakdown level. The "Average Breakdown Field for Nitridation Cycle" column averages the values for all the five capacitor test pattern sizes in each type of nitridation cycle. The dot size average for the first three nitridation cycles represent the average for all five wafer types measured. The dot size average for the oxygen post bake cycle averaged only wafers A12, C12, and H12. Wafers B12 and H11 dielectric thickness exceeded the 32 volt test limit and thus did not represent valid data.

3.2.2 Capacitors In Transistor Test Pattern Cells

The test capacitors fabricated in the same test cell as the IGFETs were previously described in Section 2.3. They had a polysilicon top electrode and were subjected to the complete process cycle that was required to fabricate the IGFETs. The ten 1000μm capacitors were subjected to ramp voltage breakdown test. Table 14 provides the fabrication parameters and lists the test results. Each breakdown voltage value represents the mean for approximately 250 measurements. As was noted for the dot capacitor measurements, the defect density appears to be the controlling factor in establishing the mean breakdown field. For this size capacitor, even the maximum breakdown field fell substantially short at the intrinsic breakdown strength established by the dot capacitor measurements.

A comparison of the ramp breakdown strength of the 1000 μm nominal dot capacitor size (actual area 8.28×10^{-3}/sq cm) and the 1000 μm x 1000 μm (actual area 1×10^{-2}/sq cm) capacitors on the transistor test patterns is shown in Table 15. The mean breakdown voltage for the 1000°C and 1100°C nitradation cycles are about the same. However, the dot capacitor mean breakdown voltage is about a factor of two greater. It appears that the additional high temperature processing the transistors test cells received may be responsible for introducing a higher defect density. The 20% greater area of the square capacitor also contributed to the lower breakdown mean.

Table 13. AVERAGE SILICON OXYNITRIDE BREAKDOWN STRENGTH AS A FUNCTION OF NITRIDATION CYCLE AND DOT SIZE

Nitridation Cycle	Nominal Dot Size					Average Breakdown Field For Nitradation Cycle
	1000μm	562μm	316μm	178μm	100μm	
1000°C/1 hr	5.72×10^6V/cm	6.77×10^6V/cm	7.07×10^6V/cm	8.68×10^6V/cm	9.07×10^6V/cm	7.58×10^6V/cm
1000°C/2 hr	6.22×10^6V/cm	7.78×10^6V/cm	8.98×10^6V/cm	9.93×10^6V/cm	1.08×10^7V/cm	8.74×10^6V/cm
1000°C/5 hr	5.86×10^6V/cm	7.23×10^6V/cm	8.32×10^6V/cm	9.73×10^6V/cm	1.09×10^7V/cm	8.41×10^6V/cm
1000°C/2 hr + 1000°C/1 hr in O_2	2.31×10^6V/cm*	3.56×10^6V/cm*	5.27×10^6V/cm*	6.73×10^6V/cm*	8.12×10^6V/cm*	5.20×10^6V/cm

*Average only three wafer types. The other lines averaged five wafer types.

Table 14. CAPACITOR BREAKDOWN VOLTAGE ON TRANSISTOR TEST PATTERNS

Sample Lot/Wafer	Wafer Type	Nitridation Cycle	Dielectric Thickness*	Mean Breakdown Voltage	Maximum Breakdown Voltage	Mean Breakdown Field	Maximum Breakdown Field
1 - 3	N-FZ	1100°C/2 hr	26.7nm	6.70V	17V	2.51×10^6V/cm	6.37×10^6
2 - 1	N-FZ	1000°C/2 hr	26.7nm	4.90V	11V	1.84×10^6V/cm	4.12×10^6
2 - 3	N-FZ	1100°C/2 hr	31.2nm	7.64V	24.5V	2.45×10^6V/cm	7.85×10^6
2 - 4	N-FZ	1100°C/2 hr	31.2nm	8.02V	27.5V	2.57×10^6V/cm	8.81×10^6
2 - 7	P-CZ	1100°C/2 hr	31.2nm	9.55V	20V	3.00×10^6V/cm	6.41×10^6
2 - 8	P-CZ	1100°C/2 hr	31.2nm	7.76V	20V	2.49×10^6V/cm	6.41×10^6
2 - 9	N-CZ	1000°C/2 hr	26.7nm	8.38V	24.5V	3.14×10^6V/cm	9.18×10^6
2 - 10	N-CZ	1000°C/2 hr	26.7nm	7.64V	18.5V	2.86×10^6V/cm	6.93×10^6
2 - 11	N-CZ	1100°C/2 hr	31.2nm	7.01V	21.5V	2.25×10^6V/cm	6.89×10^6
2 - 12	N-CZ	1100°C/2 hr	31.2nm	10.08V	26V	3.23×10^6V/cm	8.32×10^6

*Ellipsometer measurement (Not corrected for nitridation)

Table 15. COMPARISON OF CAPACITOR BREAKDOWN FIELDS
LARGE DOT CAPACITOR AND AND 1mm SQUARE CAPACITOR

Sample	Description	Mean Breakdown Field	Maximum Breakdown Field
Large Dot Capacitor (1000 μm nominal) Nitridation 1000°C/2 hrs.			
A11	N-FZ	6.49×10^6V/cm	1.16×10^7V/cm
B11	P-CZ	6.13×10^6V/cm	9.68×10^6V/cm
C11	N-CZ	4.78×10^6V/cm	1.24×10^7V/cm
H8	P-CZ	7.16×10^6V/cm	1.20×10^7V/cm
H9	P-CZ	6.49×10^6V/cm	1.08×10^7V/cm
	Av.	6.21×10^6V/cm	Av. 1.13×10^7V/cm
H7	Oxide P-CZ	8.52×10^6V/cm	
Square Capacitor (1000 μm x 1000 μm) On Transistor Test pattern Nitridation 1000°C/2 hrs.			
2-1	N-FZ	1.84×10^6V/cm	4.12×10^6V/cm
2-9	N-CZ	3.14×10^6V/cm	9.18×10^6V/cm
2-10	N-CZ	2.86×10^6V/cm	6.93×10^6V/cm
	Av.	2.61×10^6V/cm	Av. 6.74×10^6V/cm
Nitridation 1100°C/2 hrs.			
1-3	N-FZ	2.50×10^6V/cm	6.37×10^6V/cm
2-3	N-FZ	2.45×10^6V/cm	7.85×10^6V/cm
2-4	N-FZ	2.57×10^6V/cm	8.81×10^6V/cm
2-7	P-CZ	3.06×10^6V/cm	6.41×10^6V/cm
2-8	P-CZ	2.49×10^6V/cm	6.41×10^6V/cm
2-11	N-CZ	2.25×10^6V/cm	6.89×10^6V/cm
2-12	N-CZ	3.23×10^6V/cm	8.33×10^6V/cm
	Av.	2.65×10^6V/cm	Av. 7.30×10^6V/cm

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3.3 TRANSISTOR CHARACTERISTICS

Curve tracer measurements were taken on a number of IGFETs with silicon oxynitride dielectric that were fabricated by the process described in Section 2.3.1. Figures 8, 9, and 10 show sets of curves for three transistors with channel lengths of 3,4, and 5 μm. All had a channel width of 40 μm. These curves clearly demonstrate that silicon oxynitride performs satisfactorily as a gate dielectric in an IGFET. Also, it may be noted that because the dielectric constant of silicon oxynitride is somewhat greater than that of silicon dioxide, the gm of these transistors is somewhat greater than if silicon dioxide was used under the gate electrode.

3.4 C-V MEASUREMENTS

Samples fabricated in the experimental runs were further characterized to determine the initial dielectric quality and the dielectric behavior under stress. As described in Section 2.2, aluminum dots were defined on the unpatterned wafers by e-beam evaporation and etching. The metal dots were octagons ranging in diameter from 1000 to 100 mm in 5 logarithmic steps. The deposited metal was annealed at 450°C for 20 minutes in hydrogen.

Capacitance-Voltage (C-V) data were taken graphically using a Boonton 92 B capacitance meter with a measurement frequency of 1 MHz. The measured curves were compared with predicted C-V curves derived from textbook expressions, taking into account the substrate doping and metal work function, but assuming that the dielectric constant of the gate dielectric is the same as silicon dioxide. The error thus introduced is interpreted as an effectively thinner dielectric than the true thickness. Quasistatic C-V curves were also taken, with an applied voltage ramp rate of 80 mV/s provided by a Wavetek function generator, and the displacement current measured through a Keithley 927 Current Amplifier set at 1010 V/A. By careful shielding and by single point grounding technique, an open circuit noise level below 10 fA was obtained.

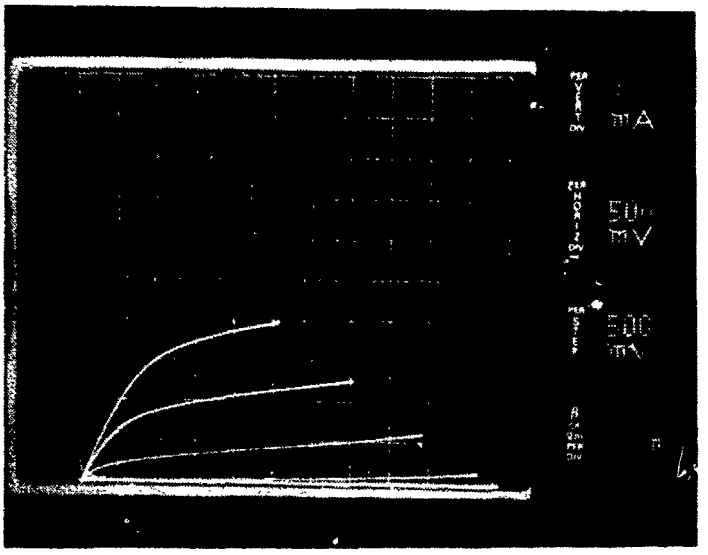

Figure 8. IGFET - Gate Dielectric 31.2nm Silicon Oxynitride
3μm Channel Length
V_T - 0.21 Volts, g_m - 3400μm

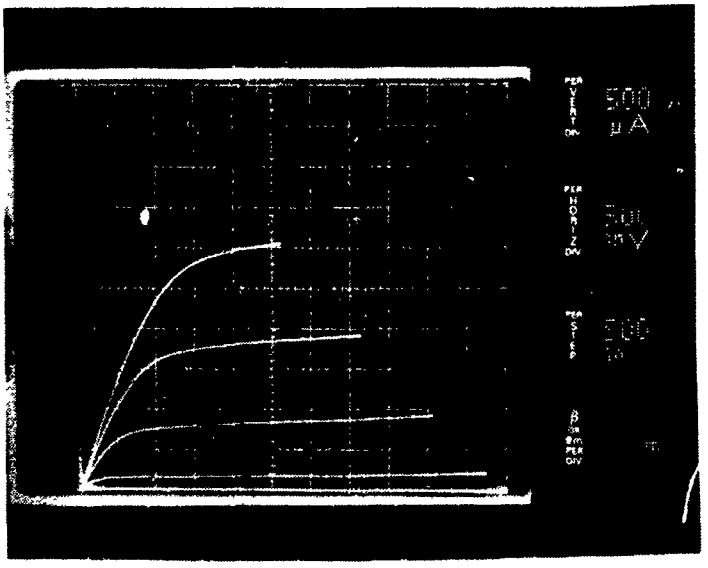

Figure 9. IGFET - Gate Dielectric 31.2nm Silicon Oxynitride
4μm Channel Length
V_T - 1.06 Volts, g_m - 2400μm

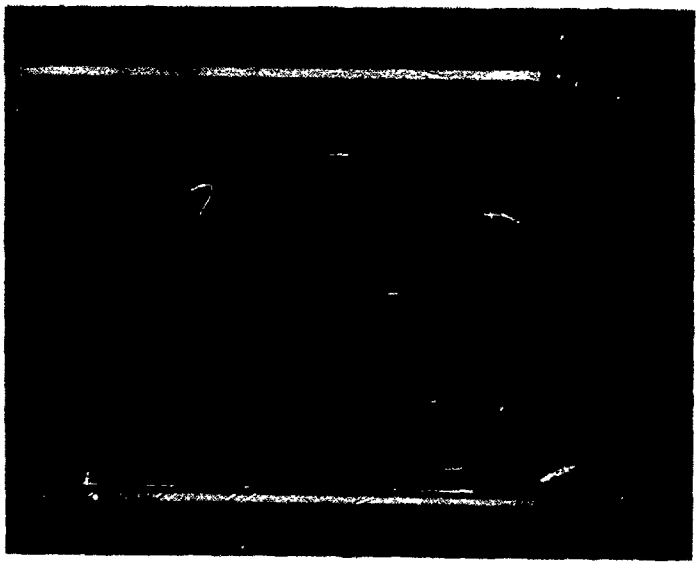

Figure 10. IGFET - Gate Dielectric 31.2nm Silicon Oxynitride
5μm Channel Length
V_T - 1.24 Volts, g_m - 1360μm

The results of the C-V measurements are summarized in Table 16. The flat band voltage shifts are averages of several dots on each wafer. The shift is found with reference to the predicted values, which vary according to wafer type and resistivity. The average values shown for each nitridation condition are the ensemble averages, that is, the wafer average is weighted by the number of samples tested on the wafer. Note that wafer types A and C are n-type, while wafer types B and H are p-type. It can be seen that the wafers from a given nitridation run show a very consistent shift of flat band voltage, regardless of type, corresponding to fixed charge in the dielectric. The magnitude of the fixed charge can be found from the expression Q=CV. An oxide 200nm thick will have a capacitance of 170 nF/cm^2, so a one volt shift corresponds to 1.7×10^{-7} $Coul/cm^2$ or 1.0×10^{12} electron charges/cm^2. The charge densities inferred from Table 16 thus range from $+6.3 \times 10^{11}$ to $-4.0 \times 10^{11}/cm^2$. Note that a negative shift corresponds to positive fixed charge.

The general behavior of the fixed charge with respect to nitridation conditions is consistent with other recent work. Ruggles and Monkowski[4] carried out nitridation cycles in ammonia at 950, 1050, and 1150°C, for 10, 30, 90, and 240 minutes. They observed a large buildup of positive charge for short nitridation cycles, with a reduction in the total positive charge for longer cycles at the same temperature. Pan and Paquette[5] also report an initial positive charge buildup that decreases upon longer nitridation. The maximum charge buildup is about $14 \times 10^{11}/cm^2$ for 950 or 1050°C nitridations, and is relatively independent of the thickness of the initial oxide and the oxidation conditions. Our data also show the positive charge for the shortest nitridation, and a pronounced shift for longer cycles or higher temperatures. The reoxidized run shows again a large amount of positive charge in the dielectric.

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4 G. A. Ruggles and J. R. Monkowski, "An Investigation of Fixed Charge Buildup in Nitrided Oxides," J. Electrochem. Soc., 133:787 (1986).

5 P. Pan and C. Paquette, "Positive Charge Generation in Thin SiO2 Films During Nitridation Process," Appl. Phys. Lett, 47:473 (1985).

Table 16. AVERAGE FLAT BAND VOLTAGE SHIFT COMPARED TO PREDICTED VALUES, FOR VARIOUS NITRIDATION CONDITIONS

Temp.	Time	Wafer	Flat Band Voltage Shift
1000°C	1 hour	A9	-.37 Volt
		B9	-.30
		C9	-.15
		H3	-.10
		Average	-.30
1000°C	2 hours	B11	.04
		H9	.20
		Average	.07
1000°C	5 hours	A10	.36
		B10	.13
		C10	.37
		H6	.40
		Average	.32
1100°C	2 hours	A7	.20
		A8	.18
		B8	.14
		C7	.19
		C8	.32
		Average	.19
1000°C (Reoxidized)	2 hours	A12	-.43
		B12	-.63
		C12	-.50
		H11,H12	-.40
		Average	-.42

One feature of our data that must be examined carefully is the apparent generation of negative charge in the dielectric, as there is no readily apparent model for such charge generation. The data were reviewed for correctness of the model, sources of experimental error, and direct comparison of measured C-V curves. In the model, the predicted flat band voltage depends only on the gate metal and the substrate doping. For aluminum, the expression used was

$$W_{ms} = -0.6 + v_{th} \times u_b$$

where the work function W_{ms} equals the predicted flat band voltage, v_{th} is the thermal voltage, and u_b is the normalized bulk potential of the substrate. The predicted values are -0.33 and -0.90 volts for n- and p- type substrates, respectively. Observed flat band voltages on the thin gate oxides of wafers H1 and H7 agree with the predicted values within 0.05 V. Thus there is no evident discrepancy with respect to the predicted flat band voltages.

One source of experimental error has been identified. The series resistance of the capacitance test station is known to interfere with accurate measurement of the oxide capacitance when the sample is biased into accumulation. The resistance is due mainly to contact resistance between the tungsten probe and the aluminum metal dot. The net effect is to cause a low reading of the capacitance. This effect is only seen when the sample capacitance is above 1000 pF. The high frequency C-V curves are thus distorted, with the correct capacitance shown when the sample is depleted or inverted, and a low capacitance shown at the opposite bias condition of accumulation.

Since the predicted flat band capacitance is expressed as a fraction of the oxide capacitance, a spuriously low measured oxide capacitance will cause an error in determining the measured flat band voltage. To compensate for this source of error, additional readings were taken with the flat band capacitance expressed as a multiple of the minimum high frequency capacitance. The discrepancy between the two measured values ranged from 0 to 0.3 V depending on the sample. This source of error is not large enough to account for the magnitude of the positive shift in the measured flat band voltage shown in Table 16.

Additional verification of the positive flat band voltage shift comes from direct comparison of measured C-V curves. Figure 11 shows measured data for sample B10 from the 5-hour nitridation that showed the maximum positive shift, along with data for a thin gate oxide on wafer H7. Both C-V curves are normalized by their measured oxide capacitances to facilitate the comparison. It is very clear that the nitrided sample B10 has undergone a positive shift of a few tenths of a volt with respect to the thin gate oxide.

3.5 OBSERVATION OF TUNNELING IN OXYNITRIDE FILMS

Tunneling current was measured vs applied voltage for samples from several nitridation runs. A Keithley constant current supply was used to drive an initial current of 0.1 nA through the dielectric. A sufficient time must be allowed for the sample capacitance to charge up in order to be sure the current is tunneling current and not displacement current. The voltage is measured at the compliance voltage output of the Keithley. The voltage cannot be measured directly across the sample as this would create a shunt current path. The Keithley instrument is then programmed to increase the current stepwise in logarithmic increments up to 10 microamps. At each increment the voltage is measured after a sufficient dwell time for charging. An example of data obtained in this way is shown in Figure 12. The voltage across the sample increases steadily up to about 12 volts, where the dielectric fails and breakdown occurs.

The same data set is shown in Figure 13, plotted in a way to show conformity to the predicted dependent of tunneling current density J on applied voltage V

$$J = aV^2 e^{-bV}$$

where a and b are constants. The straight line fit of the data for more than three orders of magnitude range in current indicates that it is indeed Fowler-Nordheim tunneling that is observed. Several samples from different wafers were tested in this way, and excellent straight line fits were obtained in all cases. Many of the samples were able to support about 100 μA/cm2 of tunneling current before failure.

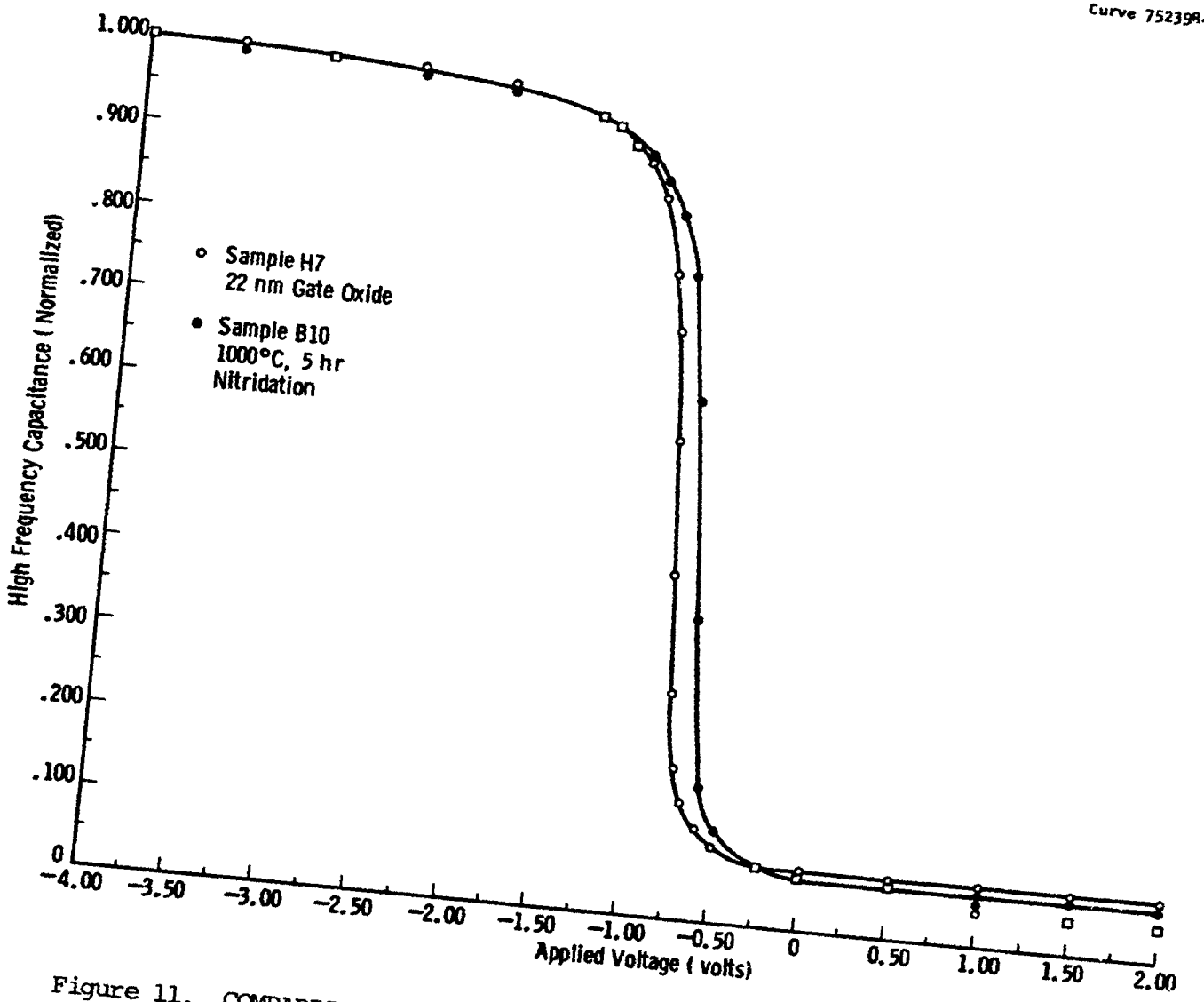

Figure 11. COMPARISON OF C-V CURVES FROM OXIDE AND OXYNITRIDE SAMPLES

Curve 752398-B

P.G. McMullin
m.m.- jd 7-24-86

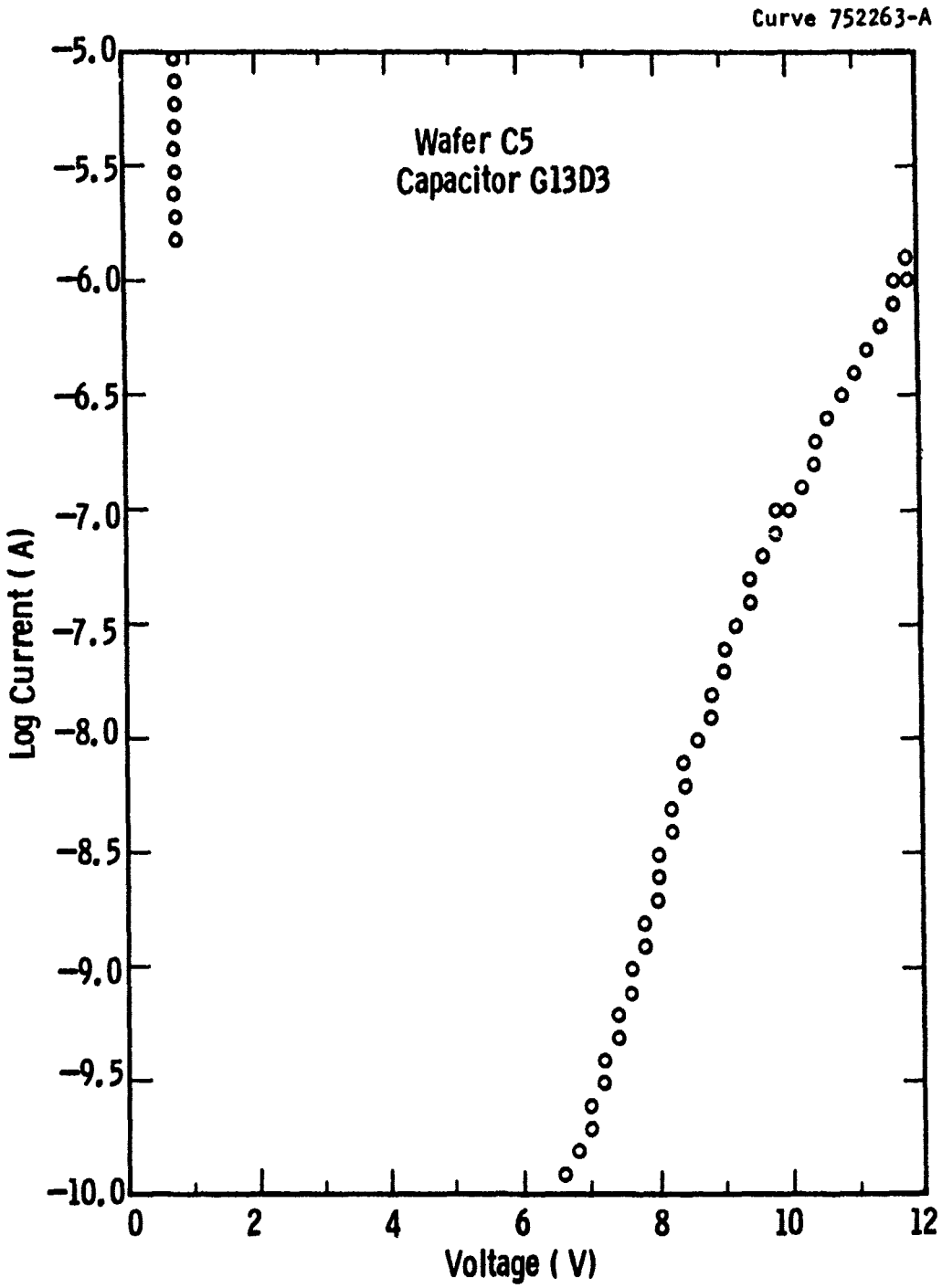

Fig. 12 – Tunneling current vs. voltage

P. McMullin
m.m.- jd 6-23-86

Curve 752263-A

Curve 752262-A

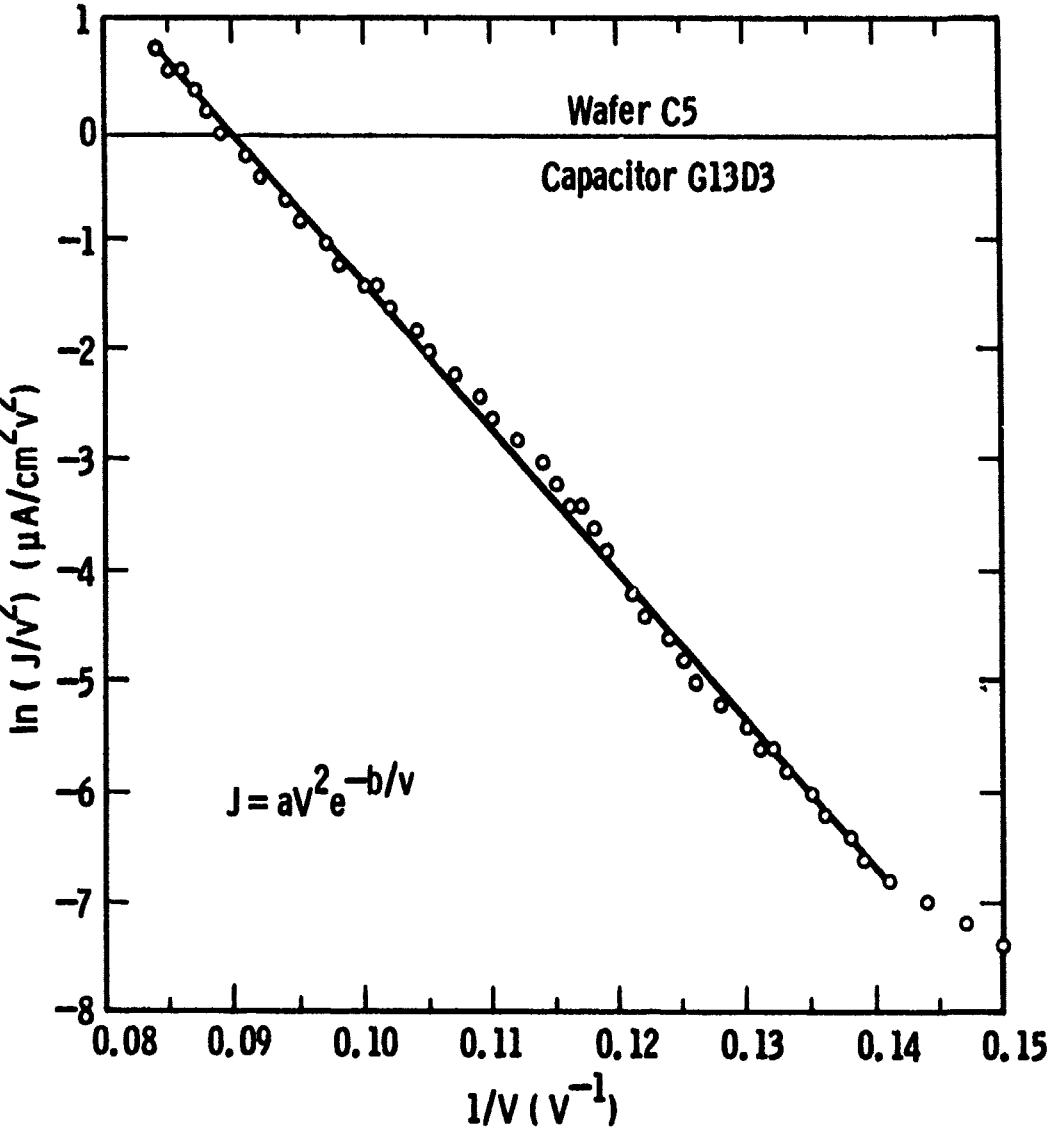

Fig. 13 — Tunneling current data replotted to show conformance to predicted Fowler-Nordheim tunneling expression

P. McMullin
m.m.- jd 6-23-86

Curve 752262-A

3.6 STRESS TESTING

The stability of the oxynitride dielectric was tested under stress by passing current through the dielectric and observing the change in C-V characteristics. A constant current supply was used for driving 0.1 nA of current through selected MOS capacitors. Positive voltage was applied to the metal dot, causing electron tunneling from the substrate. The mechanism is Fowler-Nordheim tunneling, described previously. During the stressing interval, the applied voltage was recorded on a strip chart. Samples which showed a breakdown or irregularity in the applied voltage record were discarded. The initial stress interval was 5 minutes long, but several samples were further stressed for one or two 40-minute intervals. A summary of the stress test results is presented in Table 17. Most of the samples exhibit a positive shift in the flat band voltage when remeasured after the stress interval. This corresponds to accumulation of negative charge in the dielectric, and is consistent with the charging of neutral traps by electrons. The samples from the 1100°C run show a larger positive shift, which may indicate a higher density of neutral traps created by the higher temperature nitridation.

Four of the wafers show negative flat band voltage shifts, corresponding to positive charge buildup in the dielectric. Two wafers, H6 and H9, show unusually large flat band shifts. The H type wafers are p-type CZ 10 ohm-cm silicon, practically identical to the B-type wafers. Wafer H6 was processed simultaneously with wafer B10, and H9 simultaneously with B11. The difference in the results is thus hard to interpret on the basis of initial specification or process variation. Further, wafer H3 is very similar to B9 and does not show the same large shift as H6 and H9. It must be concluded that the very large shifts of H6 and H9 are due to an incidental factor, such as contamination of the metal dots with a mobile ion species such as sodium.

Table 17 also shows a small negative flat band voltage shift for both wafers from the 1000°C, 1 hour nitridation cycle. Samples from this run also show a strong accumulation of positive charge due to the nitridation cycle itself, as previously described. In this case, the flow of electrons may be acting as a non-thermal activation mechanism for the chemical processes involved

Table 17. SUMMARY OF STRESS TEST RESULTS

TEMP.	TIME	WAFER	FLAT BAND VOLTAGE SHIFT
1000°C	1 Hour	B9	-.2 Volt
		H3	-.3
1000°C	2 Hours	B11	.2
		C5	.2
		H9	-1.25
1000°C	5 Hours	B10	.2
		C10	.2
		H6	-1.4
1100°C	2 Hours	A8	.3
		B8	.55
		C8	.4

Each Sample Stressed at .1 nA Current
Duration of Stress Cycle is 5 Minutes

in generating positive charge during nitridation. For other runs at the same temperature, the greater duration of the nitridation cycle would allow the chemical processes to go to completion. It could be expected that longer stress intervals for the 1 hour nitridation samples might produce a saturation of positive charge accumulation corresponding to the completion of the chemical reactions of nitridation. This supposition, however, was not tested during the program.

4.0 CONCLUSIONS AND RECOMMENDATIONS

4.1 CONCLUSIONS

Based on the experimental findings, the following conclusions may be drawn. The intrinsic breakdown strength of the nitrided dielectrics is slightly greater than that of the thin gate oxide prior to nitridation. The increase in dielectric breakdown voltage is about 10 percen. The best results were obtained with a 2-hour nitridation cycle at 1000°C. This nitridation is significantly better from the standpoint of breakdown voltages than the 1-hour cycle, and slightly better than the 5-hour cycle. Reoxidation after a nitridation cycle gave significantly lower breakdown voltages.

Characterization of the sample by C-V analysis showed a buildup of positive charge in the dielectric during nitridation cycles of 1 hour duration at 1000°C. A 2-hour nitridation cycle at 1000°C gave an uncharged dielectric, and nitridation cycles at 1000°C for 5 hours and at 1100°C for 2 hours gave an apparent negative charge in the dielectric, as seen in direct comparison of measurement data. No model is available to explain the apparent negative charge.

Electron tunneling was observed in selected samples. The tunneling mechanism was identified as Fowler-Nordheim tunneling by analysis of the data. Stressing of the dielectric by tunneling current resulted in accumulation of negative charge by electron capture at neutral traps. Samples from the short, 1-hour nitridation at 1000°C showed positive charging under stress. This is attributed to non-thermal activation of chemical processes in the dielectric.

4.2 RECOMMENDATIONS

The results of this program point to several areas where further work would be useful. The recommended topics are as follows:

1. The voltage breakdown data show a pronounced dependence on capacitor area, and a large difference between the mean value of breakdown voltage and the maximum voltage observed for a given capacitor size. This is due to a high area density of defects that cause locally lower breakdown voltages. A further study of methods and processes to reduce the defect density in oxynitride films would address this problem.

2. Most of the runs for this program involved nitridation at temperatures of 1000°C or above. Advanced VLSI fabrication processes require limiting the temperature, to the 900 - 1000°C range, or lower. A second useful area of study would be the determination of the optimal process and the quality obtainable for oxynitride films fabricated at 900°C.

3. The results of stress testing on selected samples show that oxynitride films are stable under the passage of tunneling current. The comparison of stress testing by tunneling current with radiation hardness testing would also be an important area of study.

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