

AD-A182 486

IN-SITU MOS GATE ENGINEERING IN A NOVEL RAPID
THERMAL/PLASMA MULTIPROCESSING REACTOR(U) STANFORD UNIV
CA CENTER FOR INTEGRATED SYSTEMS M M MOSLEH ET AL
23 JAN 87

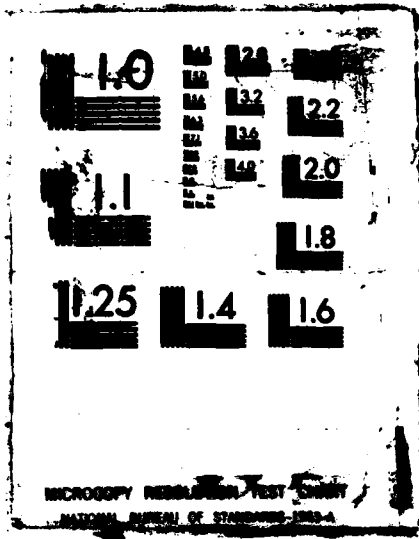
1/1

UNCLASSIFIED

F/G 20/2

ML





①
DTIC FILE COPYIN-SITU MOS GATE ENGINEERING IN A NOVEL
RAPID THERMAL/PLASMA MULTIPROCESSING
REACTOR

Mehrdad M. Moslehi Man Wong Krishna C. Saraswat

Steven C. Shatas

Center for Integrated Systems, Stanford University, CA 94305

January 23, 1987

DTIC
ELECTE
JAN 29 1987

AD-A182 486

Low temperatures and short times are essential requirements of future VLSI processing and the use of plasma in conjunction with single-wafer lamp heating is a major step to realize this goal. *In-situ* multiprocessing reduces contamination and enhances yield. Reproducible growth of thin oxides in hot-wall furnaces is difficult due to long transient times and constant furnace temperatures. Since furnaces are not designed for single-wafer processing, no extensive *in-situ* real-time measurements can be performed. RTP of Si in O_2 and NH_3 ambients is an attractive technique for the growth of silicon nitride, silicon dioxide, nitrated oxides, oxidized nitrides, and application-specific insulators [1]. We have also demonstrated the feasibility of low-temperature nitridation of Si in nitrogen plasma generated by microwave discharge [2]. LPCVD of tungsten (W) has emerged as a viable technology for VLSI. The conventional hot-wall furnaces are not suitable for reproducible high-rate W deposition and nonselective formation of W on insulators.

Based on our experiences with microwave plasma nitridation and the rapid thermal dielectric growth and anneal processes, we have developed a novel cold-wall single-wafer rapid thermal/plasma multiprocessing reactor for *in-situ* growth and deposition of dielectrics, silicon, and metals (Fig. 1). This equipment is the result of an attempt to enhance equipment versatility, to improve process reproducibility and uniformity, to increase growth and deposition rates, and to achieve *in-situ* multiprocessing. The water-cooled stainless steel chamber provides various ports for gas injection, optical heating of the wafer, pump, and *in-situ* process monitoring. The wafer sits on low thermal mass pins facing the end cone of a discharge tube and is heated on the other side by tungsten-halogen lamps. The optical flux reaches the wafer through a water-cooled quartz window. The wafer temperature can be controlled in a range from room temperature to 1150 for seconds up to many minutes. Any combination of

Ar, N₂, O₂, NH₃, WF₆, WCl₆, H₂, SiH₄, and SF₄ can be injected into the chamber either through a quartz tube at the bottom of the chamber or through the side port nonplasma injectors. Remote plasma can be generated inside the tube by a microwave discharge cavity. The availability of plasma processing not only allows low-temperature dielectric growth but also has enabled us to develop several new processes for nonselective deposition of W and its compounds on insulating layers for MOS gate applications. This system configuration is very flexible for *in-situ* multiprocessing because it allows rapid cycling of ambient gases, temperature, and plasma with negligible cross-contamination. The details of this reactor are presented elsewhere [3].

The rapid thermal oxidation (RTO) process is a viable technique for growing thin . The MOS devices with rapidly grown were found to have larger charge-to-breakdown and lower electron trapping compared to furnace oxides. As an example, the charge-to-breakdown vs RTO temperature shown in Fig. 2 indicates a higher breakdown charge when the surface is free of native oxide prior to gate oxidation. This demonstrates the importance of *in-situ* preoxidation surface cleanliness because the chemical oxide simulates the oxide grown in a furnace when the wafers see uncontrolled ambient and temperature during loading and unloading. As compared to the devices with preoxidation removal of native oxide, the presence of a chemical oxide prior to RTO reduced Q_f and D_{it} , and their dependencies on the RTO temperature. Multicycle rapid thermal growth processes are suitable for dielectric engineering and *in-situ* formation of thin layered insulators with a variety of controllable oxygen and nitrogen compositional depth profiles by appropriate design of the temperature and gas cycles. In the rapid thermal nitridation (RTN) of , N-rich layers form at the surface and interface (Fig. 3(a)). RTN of slows down the generation rate of new surface states caused by high-field electrical stress (Fig. 3(b)). To demonstrate the multiprocessing capabilities of RTP, we have fabricated various NMOS transistors where RTP was employed for growth and annealing of gate oxides and nitrides, activation and redistribution of dopant in source/drain and polysilicon gates, growth of polysilicon oxides, and forming gas anneals. Some results regarding electrical performance, hot-carrier degradation, and surface mobilities of IGFETs with rapidly grown gate insulators will be presented.

The main objective of our work was to develop reliable processes for *in-situ* fabrication of W-gate MOS devices which requires the growth of gate dielectric by RTO and RTN cycles followed by a nonselective W deposition process to form the gate electrode. W is quite attractive as an MOS gate material [4]; however, a reliable process for *in-situ* formation of W gate electrodes has not been developed. W-gate MOS VLSI can be realized if some of the major problems related to the poor adhesion of W to insulating layers, channeling of

implanted dopants through W gate, and lack of oxidation resistance are overcome. We have used two approaches to solve this problem: one by using a Si glue layer and the other by the use of RTP/microwave plasma technology.

H₂ reduction of WF₆ can not occur on insulators unless some layer of metal or Si is used for initial nucleation. In a series of experiments, W deposition by a conventional hot-wall LPCVD furnace on using amorphous Si as a glue layer was investigated. For 30 min of W deposition, the W films on oxidized wafers coated with 340 and 430 of LPCVD amorphous Si successfully passed the transparent tape adhesion test. An average sheet resistance of 0.9 Ω/□ for 1300 W films was obtained. W peeled off from wafers coated with 250 of amorphous Si after only 20 min of W deposition which indicated that the presence of some amorphous Si was needed for adequate adhesion. W-gate MOS capacitors were fabricated using this technique and Fig. 4 illustrates the typical C-V characteristics. The densities of midgap D_{it} were in the range of (2.5-3.5)10¹⁰ eV⁻¹cm⁻². The insulator thickness estimated by the C-V method was consistently thicker (by as much as 30 to 55 %) than the oxide thickness measured before the amorphous Si deposition which is an indication of some remaining excess amorphous Si; however, this Si was completely consumed during subsequent thermal annealing.

As a result of the process limitations of the above technique a variety of selective and nonselective processes were investigated in this work using the novel reactor. Table 1 presents a summary list of the W deposition processes developed using our multiprocessing reactor. These techniques are grouped based on the plasma condition and the injection mode of various ambient gases. These depositions were studied extensively in a wide range of gas flows, pressure, and temperature. Several of these novel nonselective processes are reported for the first time in this work. When WF₆ or a mixture of WF₆+H₂ was injected through the nonplasma port, generation of H₂ plasma, Ar plasma, or Ar+H₂ plasma in the quartz tube promoted nonselective W deposition on insulating surfaces. Addition of Ar to H₂ enhances the plasma emission intensity and density of available atomic hydrogen. Another nonselective deposition technique developed in this work employed WF₆+Ar plasma along with nonplasma H₂. Under appropriate experimental conditions none of these nonselective deposition techniques caused W deposition on the chamber walls or inside the quartz tube. The mixture of NH₃+H₂ and WF₆ always resulted in nonselective deposition for both plasma and nonplasma types of processes. Moreover, the combination of N₂+H₂ plasma and WF₆ also resulted in nonselective metallic film deposition. The films deposited by any of the last three techniques in Table 1 (rows J,K,L) had higher resistivities compared to pure W and were expected to be W nitride compounds. W nitride may exhibit useful properties such as oxidation resistance, diffusion barrier, and ion implant channeling stop. W nitride films could also be formed by

Table 1: Various types of plasma and nonplasma tungsten LPCVD experiments performed in this work.

FUNCTIONAL DEPOSITION PROCESSES				
Deposition Type	Gases through the Quartz Tube	Gases through the Side Ports	Monitors Power	Deposition Conditions
A	None	WF ₆ +Ar	OFF	Solvent
B	None	WF ₆ +Si ₂ H ₆	OFF	Solvent
C	Ar	WF ₆ +Si ₂ H ₆	OFF	Solvent
D	SiF ₄	WF ₆ +Si ₂ H ₆	OFF	Solvent
E	H ₂	WF ₆	OFF	Solvent
F	H ₂	WF ₆	ON	Nonoxidative
G	Ar+H ₂	WF ₆	ON	Nonoxidative
H	Ar	WF ₆ +H ₂	ON	Nonoxidative
I	WF ₆ +Ar	H ₂	ON	Nonoxidative
J	WF ₆ +H ₂	WF ₆	ON	Nonoxidative
K	WF ₆ +H ₂	WF ₆	ON	Nonoxidative
L	WF ₆ +H ₂	WF ₆	OFF	Nonoxidative

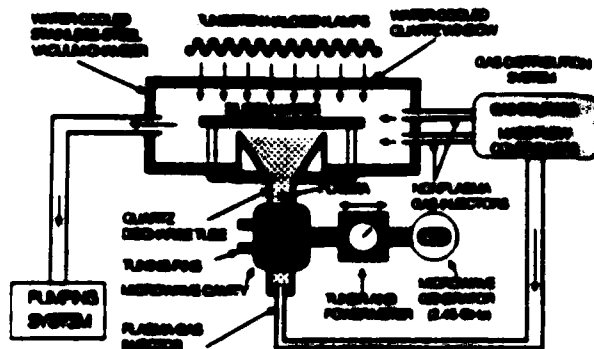


Figure 1. Schematic of the novel cold-wall single-wafer lamp-heated rapid thermal/plasma multiprocessor reactor.

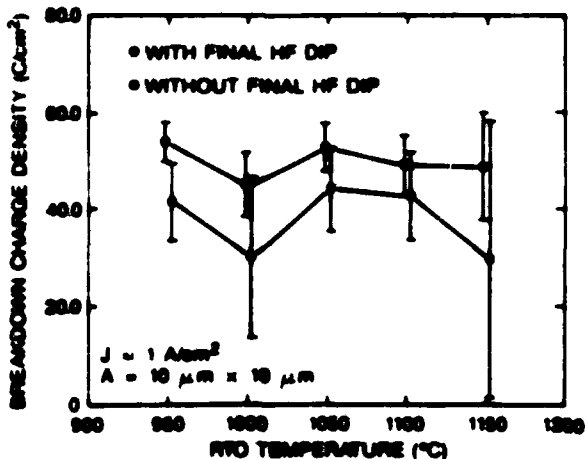


Figure 2. Breakdown charge density vs RTO temperature determined from constant-current TDDB measurements at 1 A/cm² in 10 μm x 10 μm unannealed MOS devices (rapidly grown gate oxides) with and without final preoxidation HF dip. No HF dip simulates the surface condition with native oxide such as in the hot-wall furnace oxidations and HF dipped wafers correspond to the in-situ cleaned surfaces prior to oxidation in cold-wall lamp-heated single-wafer reactors.

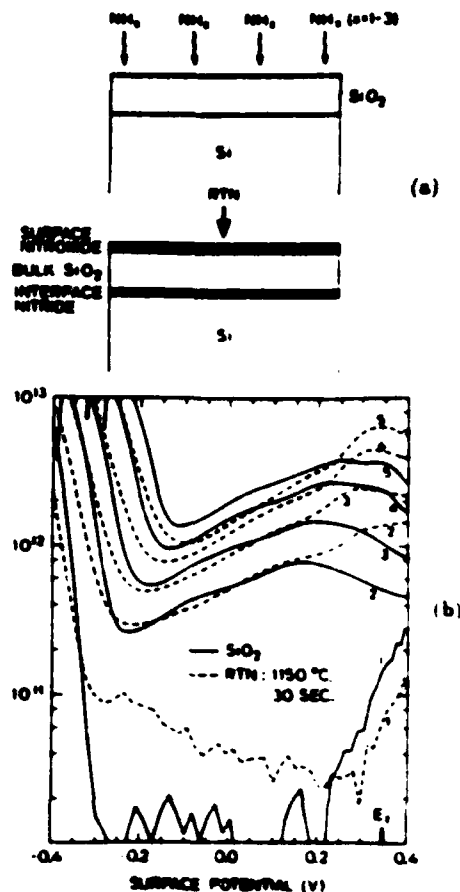


Figure 3. (a) Structural model for nitride insulators formed by RTN of SiO₂. (b) Effect of step-by-step high-field constant-current stress on surface-state density in MIS devices (gate area=7.85 x 10⁻³ cm²) with 95 Å SiO₂ and nitride prepared by RTN at 1150°C for 30 sec.

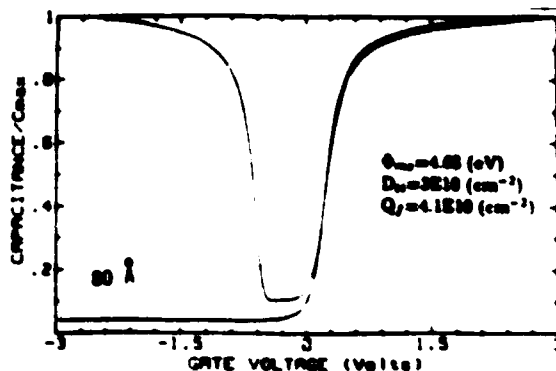


Figure 4. Typical high- and low-frequency C-V characteristics of MOS devices with subnanometer amorphous SiO₂ gate insulator and tungsten gate electrode fabricated by formation of amorphous silicon glass layer followed by selective hot-wall LPCVD furnace tungsten deposition.