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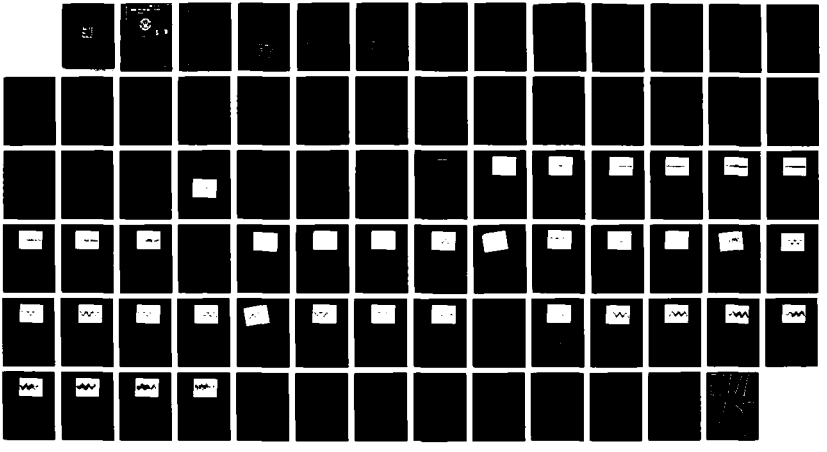

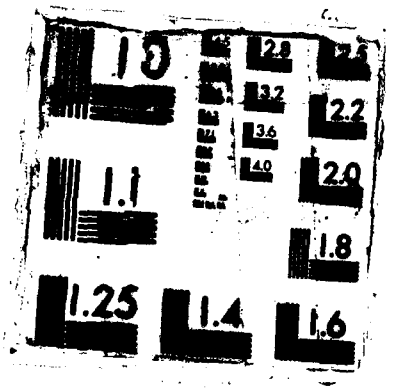
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NAVAL POSTGRADUATE SCHOOL

Monterey, California

THESIS

MEASURED PROBABILITY DENSITY FUNCTION OF A PHASE-LOCKED LOOP (PLL) OUTPUT

by

Mehmet Topcu

March 1987

Thesis Advisor Glen A. Myers

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In this report, the noise behavior of the PLL is determined experimentally. Experimental results show that the probability density function of the PLL output for a variety of input signals which are each corrupted by additive Gaussian noise resembles the Gaussian density function.

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Measured Probability Density Function of a Phase-Locked Loop (PLL) Output

by

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Submitted in partial fulfillment of the
requirements for the degree of

MASTER OF SCIENCE IN ELECTRICAL ENGINEERING

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ABSTRACT

The behavior of the Phase-Locked Loop (PLL) is difficult to describe analytically, especially when noise is present at the input because the system is non-linear.

In this report, the noise behavior of the PLL is determined experimentally. Experimental results show that the probability density function of the PLL output for a variety of input signals which are each corrupted by additive Gaussian noise resembles the Gaussian density function.

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I. INTRODUCTION

A. GENERAL WORKING PRINCIPLES OF A PHASE-LOCKED LOOP

A Phase Locked-Loop (PLL) is an electronic servo mechanism system that consists of three major componets: a multiplier, a loop filter, and a voltage conrolled oscillator, as shown in Fig. 1.1

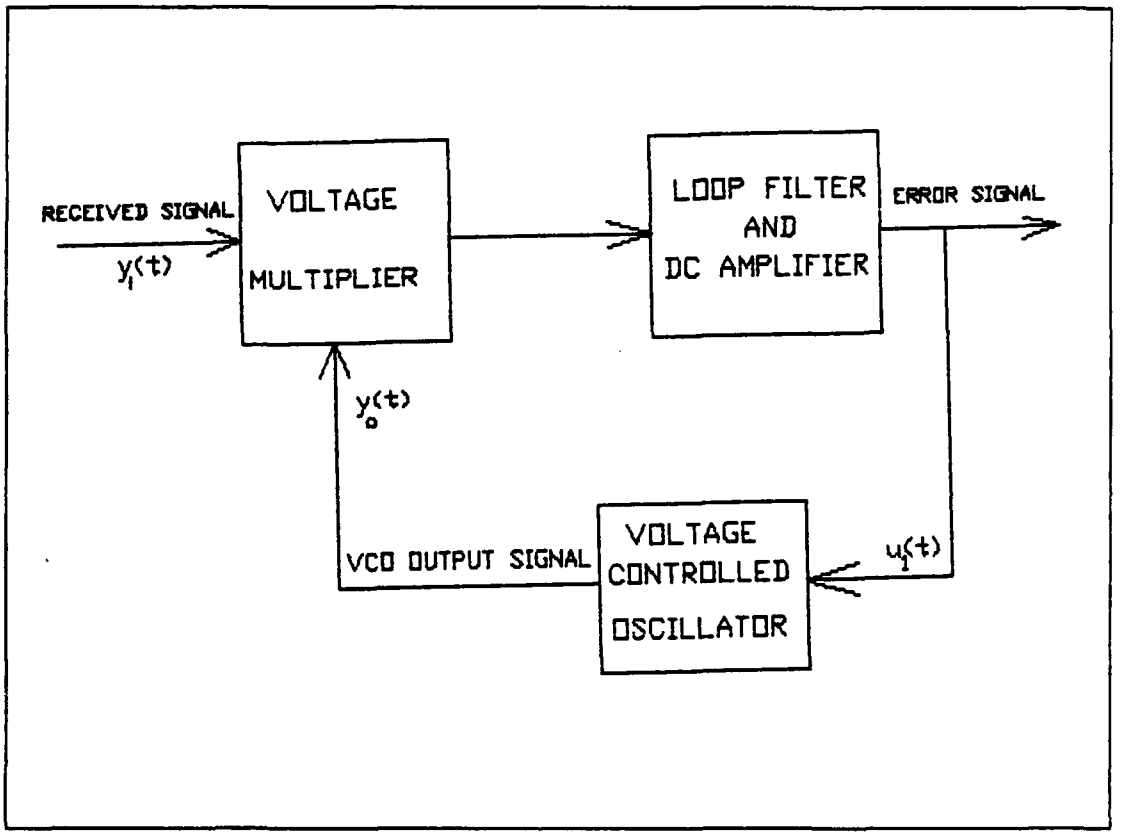


Figure 1.1 General Block Diagram of a Phase Locked-Loop.

We assume that both input signals to the voltage multiplier are sinusoidal. This way it is easy to describe system behavior analytically. Let us suppose that initially the loop is unlocked. Then we can express both input signals to the voltage multiplier as

$$y_i(t) = A\cos(w_i t + \theta_i)$$

$$y_o(t) = B\cos(w_o t + \Phi_o)$$

where w_i is the radian frequency of the incoming signal, and

w_o is the voltage controlled oscillator (VCO) rest radian frequency.

The voltage multiplier and loop filter form a phase detector. The output of the phase detector is

$$u_1(t) = K_1 \cos[(w_i - w_o)t + \theta_i - \Phi_o)]$$

where K_1 is the phase detector sensitivity.

If the radian frequency difference $(w_i - w_o)$ does not exceed a certain value, then after a period of time the VCO output signal $y_o(t)$ becomes synchronous with the input signal $y_i(t)$. Then the VCO output signal $y_o(t)$ can be expressed as

$$y_o(t) = B\cos(w_i t + \theta_o)$$

So, Φ_o has become the linear function of time

$$\Phi_o = (w_i - w_o)t + \theta_o \tag{1.1}$$

The phase detector output becomes a DC signal, when the VCO is locked to incoming signal, having value

$$\overline{u}_1 = K_1 K_2 \cos(\theta_i - \theta_o) \tag{1.2}$$

where, K_2 is the gain of the loop filter

Typically the instantaneous radian frequency (w_{inst}) of the VCO is a linear function of its applied voltage about its rest angular frequency w_o.

$$w_{inst} = \frac{d}{dt}(w_o t + \Phi_o) = w_o + K_3 u_2$$

Thus,

$$\frac{d\Phi_o}{dt} = K_3 u_2 \tag{1.3}$$

where K_3 is the VCO modulation sensitivity.

By substituting Eq.1.1 and Eq.1.2 in Eq.1.3 we find

$$\frac{d}{dt}[(w_i - w_o)t + \theta_o] = K_1 K_2 K_3 \cos(\theta_i - \theta_o)$$

Thus,

$$w_i - w_o = K_1 K_2 K_3 \cos(\theta_i - \theta_o)$$

Then the phase difference becomes

$$\theta_i - \theta_o = \text{Arc cos} \frac{w_i - w_o}{K_1 K_2 K_3} \tag{1.4}$$

Since the initial radian frequency $w_i - w_o$ is much smaller than $K_1K_2K_3$ then the phase difference becomes

$$\theta_i - \theta_o = \text{Arc cos} 0 = \frac{\pi}{2}$$

This means that when the frequency difference between the incoming signal and the VCO output is slight when the loop is out of lock, the VCO signal is 90^o diffirent from incoming signal when loop is in lock. Eq. 1.4 is valid when the loop is in lock. When the frequency difference ($w_i - w_o$) exceeds the loop gain ($K_1K_2K_3$) then the argument of the arc cos function exceeds one, which is not possible. Therefore, Eq. 1.4 is not valid for $|w_i - w_o| > |K_1K_2K_3|$. In this case, the loop behavior is described by a non-linear equation, for which an analytical solution is complicated.

B. PHASE-LOCKED LOOP (PLL) APPLICATIONS

Phase Locked Loops (PLL's) are used widely in modern communication systems for various purposes, [Ref. 1]

1. Carrier Tracking; Coherent communication systems require a carrier reference be recovered from a noisy received signal. The VCO output of a PLL can be use to track the noisy carrier.
2. Demodulation; The loop filter output of a PLL can be use to obtain the information signal from a frequency modulated or phase modulated carrier.
3. Frequency Synthesis; The PLL is an important building block of frequency synthesizers. Frequency multiplication or division may be performed using a PLL by connecting a frequency divider to the VCO output of the PLL.

C. ANALYSIS OF THE PLL

Non-linear loop analysis of the PLL results in the Fokker-Planck equation. The main goal of the theoretical analysis of the PLL is solution of the Fokker-Planck equation for given PLL charecteristics [Ref. 2]. In some analyses a Markov proccess is assumed to determine the probability density function of the phase error for a noise corrupted input signal which satisfies the Fokker-Planck equation [Refs. 3,4].

In this research, the output probability density function of the PLL is determined experimentally.

II. DESCRIPTION OF THE EXPERIMENTAL SYSTEM

A. GENERAL DIAGRAM OF THE EXPERIMENTAL SYSTEM

The experimental system schematic diagram is shown as Fig 2.1. The system includes a band pass filter (BPF), summer, hard limiter, and phase locked-loop (PLL).

The BPF creates narrow band Gaussian noise from a wide band Gaussian noise generator (Elgenco 603A). The summer adds the output of the BPF to the sinusoidal carrier or modulated sinusoidal carrier. The phase detector in the PLL circuit is designed for two-level voltages. The hard limiter converts the sinusoid plus noise voltage to a two-level voltage. The usable output of a PLL used as a demodulator occurs out of the loop lowpass filter. This output is again filtered to remove DC and amplified. All plots of probability density functions were of the voltage out of this amplifier.

B. BUILDING BLOCKS OF A PHASE-LOCKED LOOP

The PLL consists of a phase detector, a loop filter, and a VCO.

1. Phase Detector

There are two kinds of phase detectors which are distinguished by their output voltage functions of input signal phase. If the inputs are sinusoids, the output of the phase detector is a sinusoidal function of phase difference. If the inputs are square waves, the output is a triangular function. In the experimental system the inputs are square waves, an XOR logic gate is used as a phase detector and this provides a triangular output.

The input signals are,

received signal $= y_i(t) = A\,\mathrm{Sign}[V_i]$

output of VCO $= y_o(t) = B\,\mathrm{Sign}[V_o]$

where V_i is the signal plus noise voltage, V_o is the VCO output signal voltage, and Sign represents the signum function.

The output of the phase detector is the product of these two function which for two-level voltage, can be expressed as

Sign V_i	Sign V_o	XOR
+	+	0
+	−	1
−	+	1
−	−	0

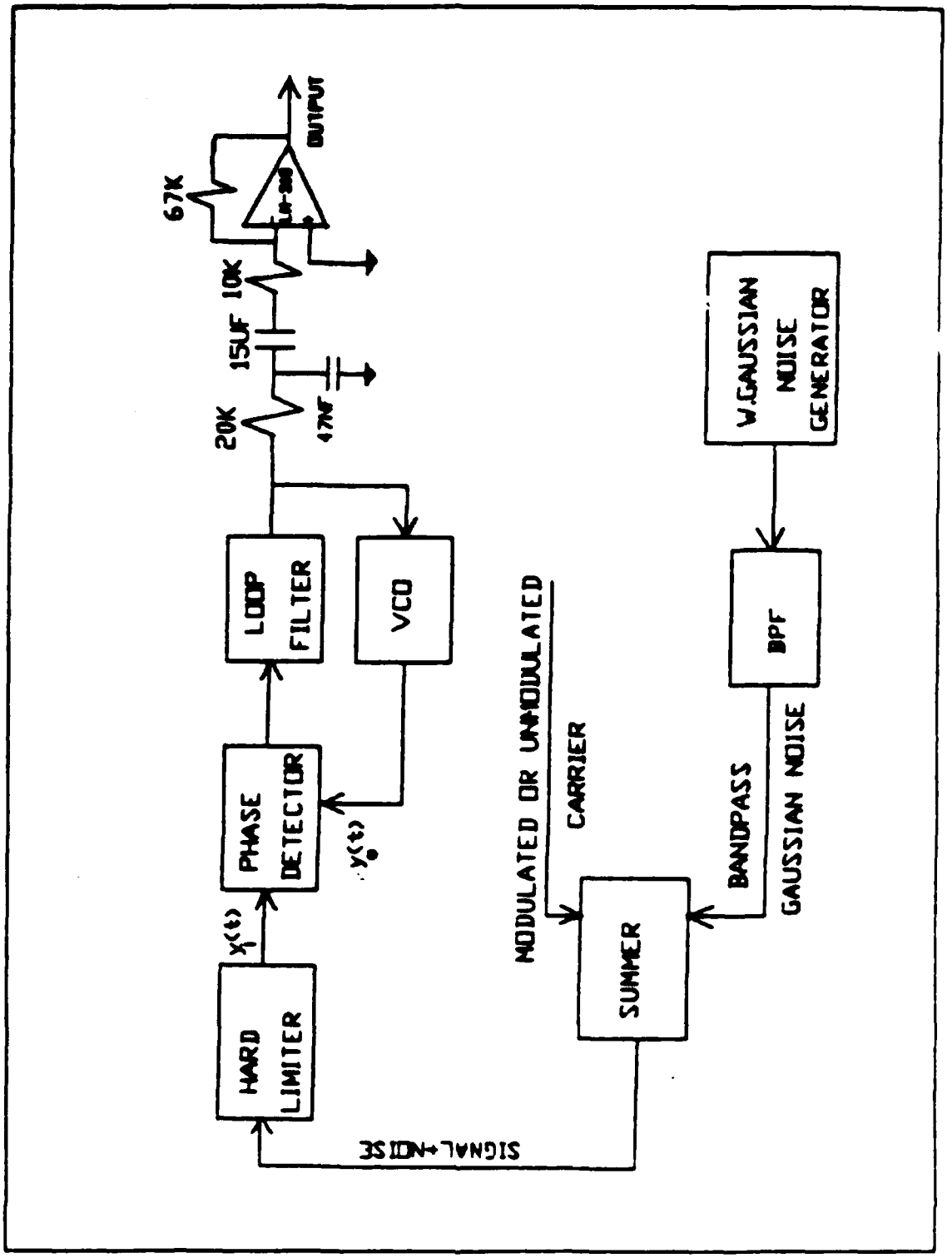


Figure 2.1 General Schematic Diagram of the Experimental System.

$u_1(t) = C\{\text{Sign}[V_i] \bullet \text{Sign}[V_o]\}$

where $\bullet$ represents the XOR logic operation.

The received signal, VCO output signal, and the output of the phase detector are depicted in Fig. 2.2.

During lock, the DC level (avarage or expected value) of the error signal u_1 is proportional to the phase difference of the phase detector input signals. The phase difference versus DC level of the error signal is the characteristic of the phase detector. From Fig 2.2 (c).

$$\bar{u}_1 = C\left(\frac{4t_0}{T} - 1\right) = \text{average value of } u_1 \qquad (2.1)$$

where t_0 is the time delay between the two signals at the phase detector input and T is the period of the input and ouput signals.

A phase difference θ can be expressed in terms of time delay t_0 as

$\theta = wt_0$, where $w = 2\pi/T$

Then Eq. 2.1 becomes

$$\bar{u}_1 = \frac{2C}{\pi}(\theta - \pi/2) \quad \text{for } 0 < \theta < \pi \qquad (2.2)$$

Similarly, for $\pi < \theta < 2\pi$

$$\bar{u}_1 = \frac{2C}{\pi}(\theta - 3\pi/2) \quad \text{for } \pi < \theta < 2\pi \qquad (2.3)$$

Fig. 2.3 is a plot of $\bar{u}_1$ vs θ and is called the phase detector characteristic.

The phase detector sensitivity K_1 is the magnitude of the the slope of its characteristic, which is

$$K_1 = \left|\frac{d\bar{u}_1}{d\theta}\right| = \frac{d}{d\theta}\left|\frac{2C}{\pi}\left(\theta - \frac{\pi}{2}\right)\right| = \frac{2C}{\pi} \qquad (2.4)$$

In the experimental circuit C is 5V, and so the phase detector sensitivity is

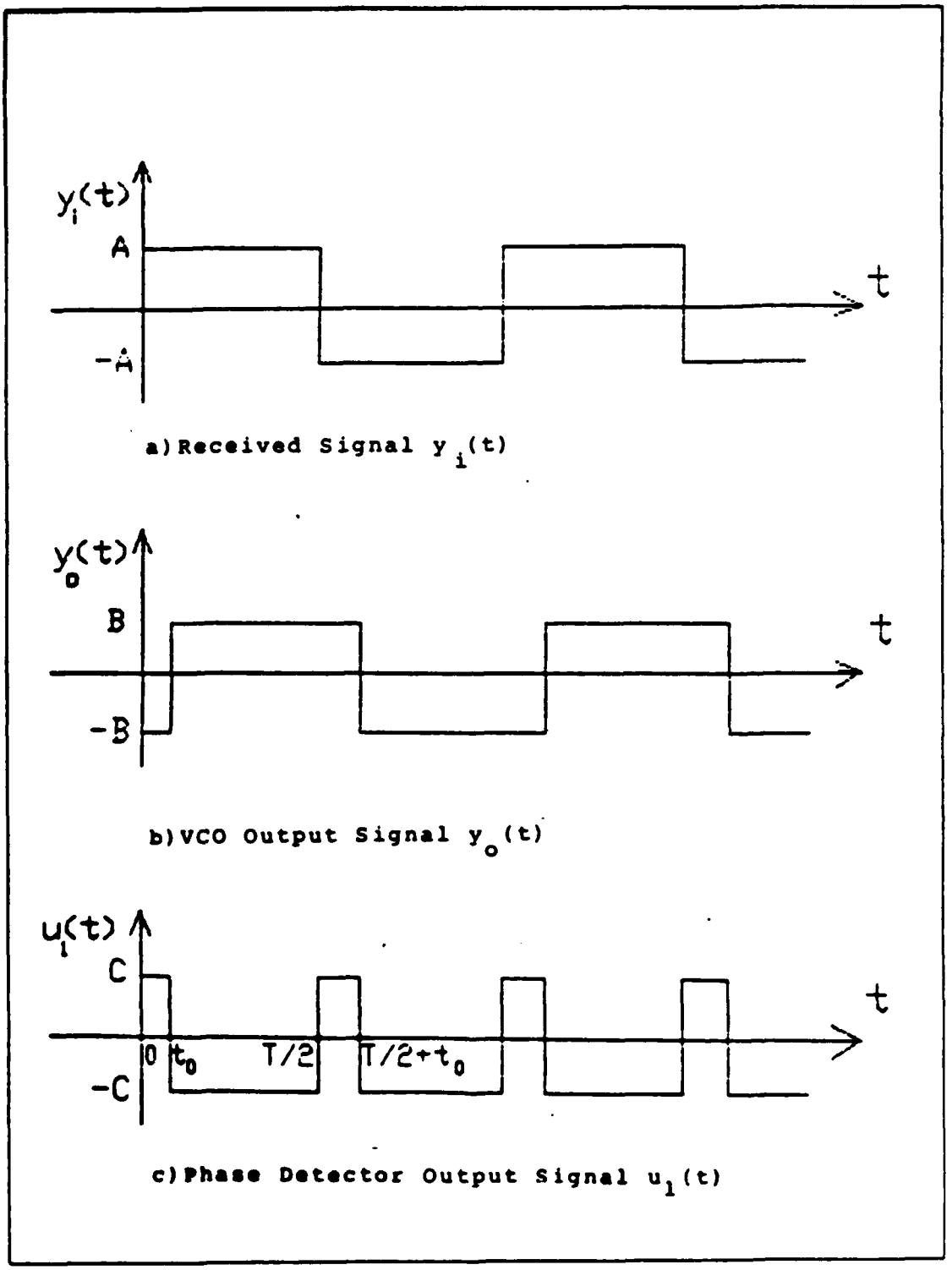


Figure 2.2 Phase Detector Waveforms.

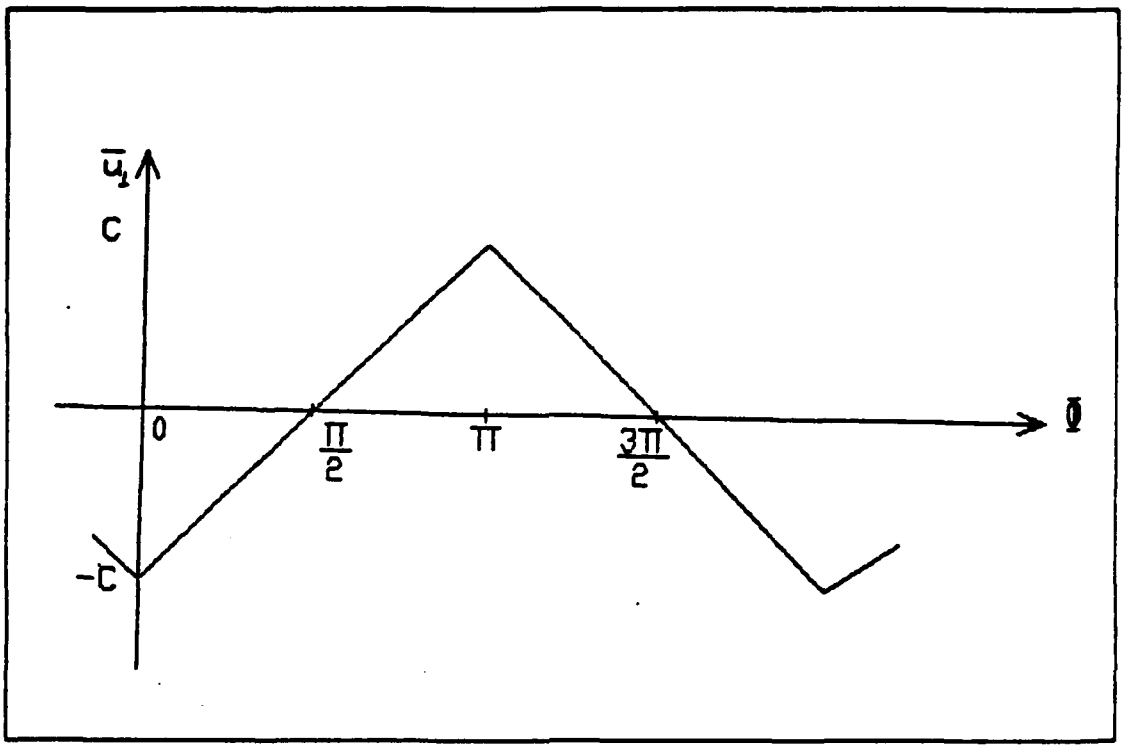


Figure 2.3 Charecteristic of the Phase Detector (XOR Gate).

$$K_1 = \frac{10}{\pi} = 3.183 \text{ rad/sec/volt.}$$

Fig. 2.3 depicts that without any disturbance at the phase detector input, its charecteristic is piecewise linear. But as soon as noise is present at the phase detector input, its response becomes non-linear as seen in Fig. 2.4 [Ref. 5].

2. **Loop Filter and DC Amplifier**

The loop filter of Fig. 2.1 is a lowpass filter (LPF). It has a considerable effect on loop behavior. The loop filter and DC amplifier are analyzed in this section. Their circuits are shown as Fig. 2.5.

A passive lowpass filter stage, summer amplifier, and another passive lowpass filter are cascaded. The 5.1 kohm resistance in Fig. 2.5 serves to easily modify loop response. Use of a summing amplifier instead of a DC amplifier permits control (adjustment) of the VCO rest frequency (open loop frequency).

Calculation of the loop transfer function proceeds as follows:
The transfer function of the first LPF is

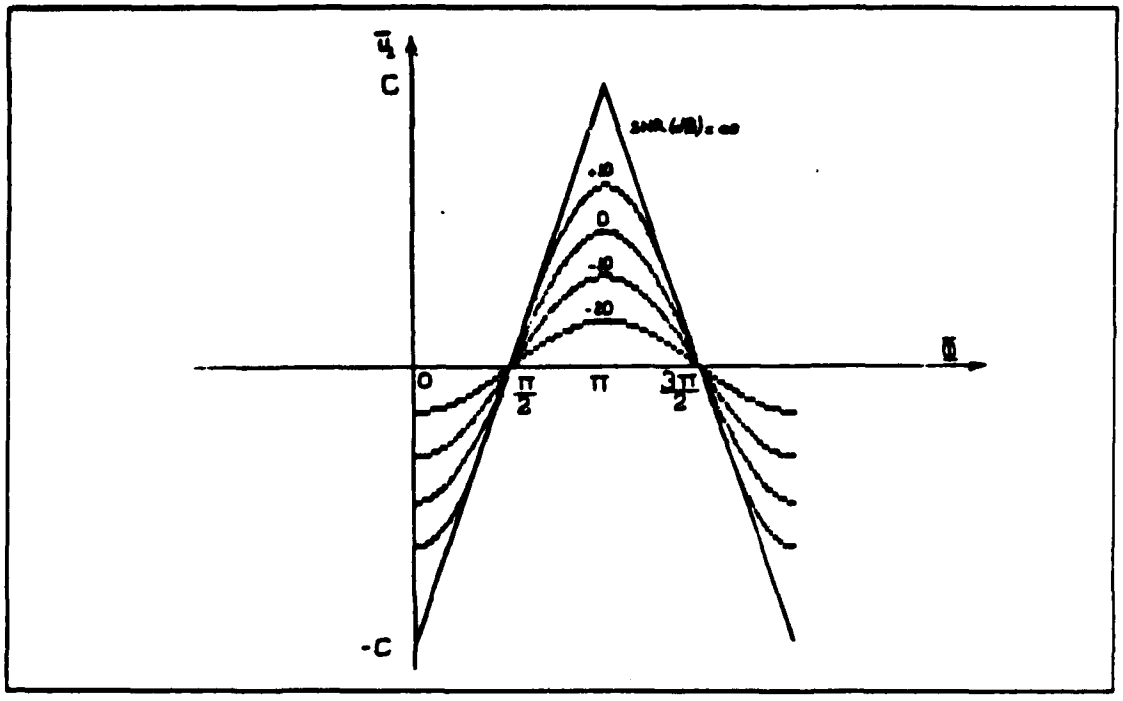


Figure 2.4 Response of a Phase Detector in Presence of Noise.

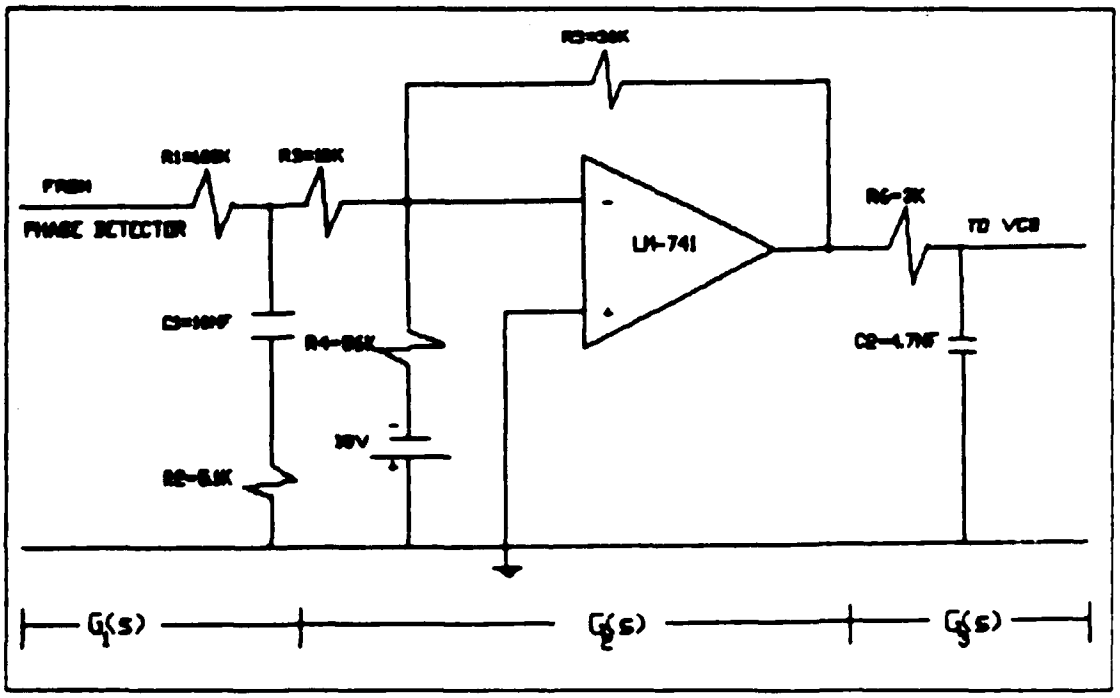


Figure 2.5 Loop Filter and DC Amplifier.

$$G_1(s) = \frac{R_2[s + 1/(R_2C_1)]}{(R_1 + R_2)[s + 1/(R_1 + R_2)C_1]}$$

Substituting the values shown in Fig. 2.5 gives

$$G_1(s) = 0.0485 \frac{s + 19607.8}{s + 951.47}$$

The DC amplifier transfer function is

$$G_2(s) = \frac{-R_5}{R_3} = -3$$

That of the second LPF is

$$G_3(s) = \frac{1}{(R_6C_2)(s + 1/R_6C_2)}$$

$$= \frac{70921.98}{s + 70921.98}$$

The transfer function G(s) of the loop filter is the product of $G_1(s)$, $G_2(s)$, and $G_3(s)$.

$$G(s) = G_1(s)G_2(s)G_3(s)$$

$$G(s) = -10319.15 \frac{s + 19607.8}{s^2 + 71873.45s + 67480136.31} \qquad (2.5)$$

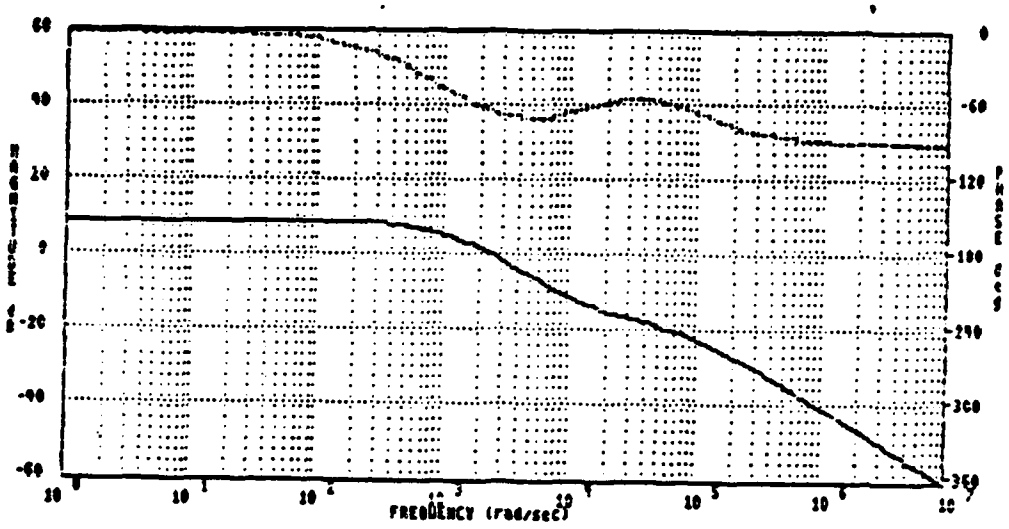
Figs. 2.6 (a) and (b) show the results of computer simulation of |G(f)| and measurement of |G(f)| respectively where $s = j2\pi f$. The filter 3dB cut-off frequency is about 170 Hz.

3. **Voltage Controlled Oscillator** (VCO)

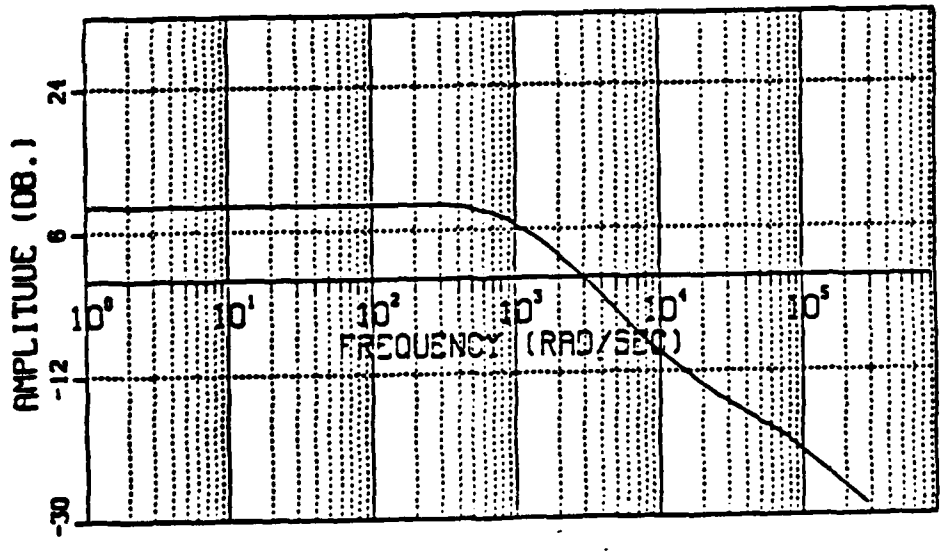
Fig. 2.7 shows the VCO circuit used in the experimental system. The LF-13741 is an integrator. The LM-311 are operational amplifiers.

The VCO output frequency is controlled by the error voltage. The main requirements of the VCO are as follows [Ref. 5].

(1) Adequate central frequency stability.



a)Computer Simulation



b).Measured.

Figure 2.6 Transfer Function of the Loop Filter.

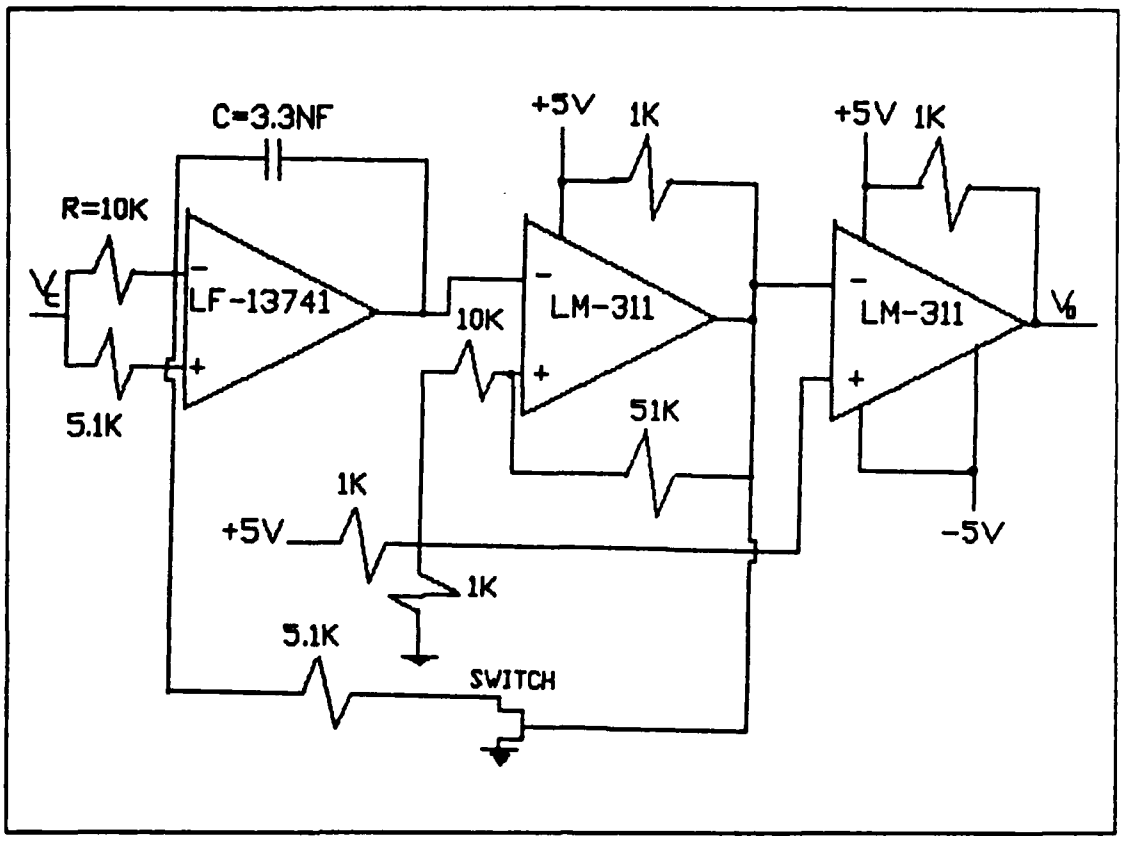


Figure 2.7 Voltage Controlled Oscillator.

(2) The widest possible frequency deviation which is theoretically $\pm K$, in order to derive maximum benefits from the whole synchronization range of the loop.

(3) A relative high modulation sensitivity K_3 (in Hz/V or rad/sec/V) because K_3 enters directly in the expression of the open-loop gain K. But for sake of stability, we can make a fairly poor modulation sensitivity and use an operational amplifier preceding the VCO to provide gain.

In the experimental system, the VCO sensitivity was chosen to lie between 8 kHz/V and 10 kHz/V to obtain stable operation.

The VCO operates as follows [Ref. 6]: Assume that the first comparator (LM-711) output initially is positive. This positive voltage level turns the analog switch to on, which causes the integrator output to be a positive going ramp voltage. When this ramp level exceeds the voltage level on the (+) terminal of the first comparator, its output goes low and turns the switch off. The integrator output then decreases until the analog switch is again turned on and the cycle repeats.

A triangular wave is generated at the integrator output. Fig. 2.8 shows an equivalent circuit of the integrator when V_1 is increasing when the analog switch is closed. In this circuit V_c is the control voltage of the VCO. By using the Thevenin equivalent circuit of Fig. 2.8 (b), we can express the output waveform as

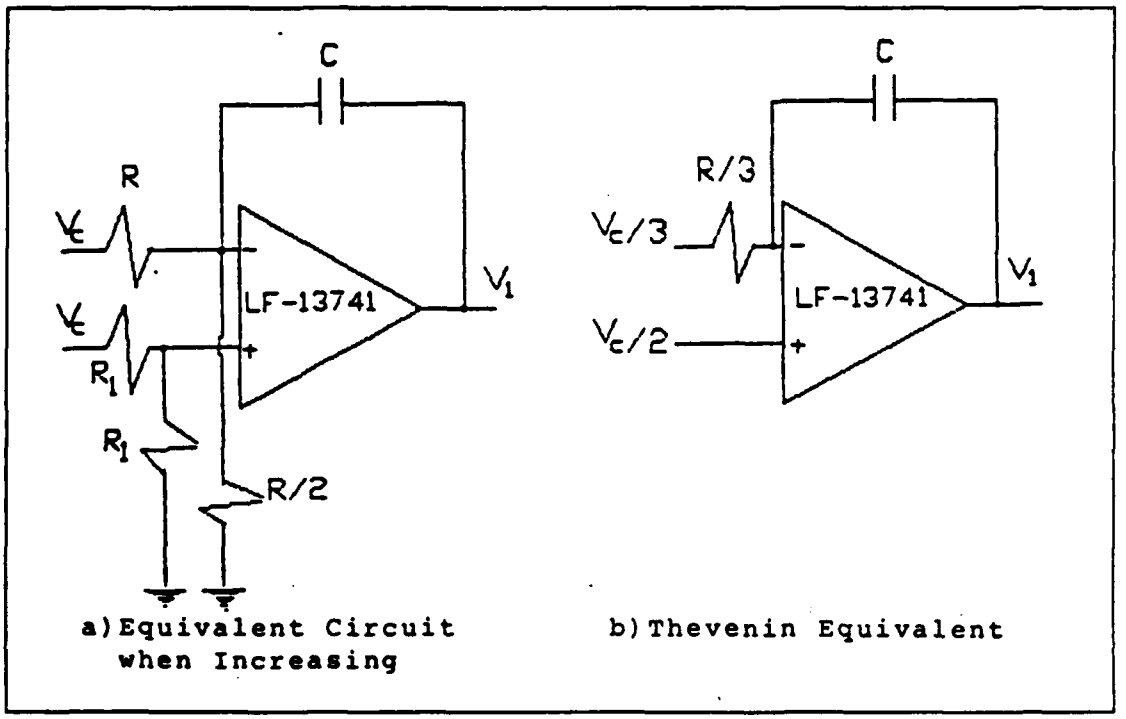


Figure 2.8 Integrator Circuit Diagram.

$$V_1 = \mathcal{L}^{-1}[-\frac{V_c}{RCs} + \frac{V_c}{2s}(1 + \frac{3}{RCs})] = -\frac{V_c}{RC}t + \frac{V_c}{2} + \frac{V_c}{2RC}t$$

$$V_1 = \frac{V_c}{2}(1+\frac{t}{RC}) \quad \text{(when increasing)} \qquad (2.6)$$

The equation for the output of the integrator is calculated when V_1 is decreasing by the same method and is found to be

$$V_1 = \frac{V_c}{2}\left(1 - \frac{t}{RC}\right) \text{ (when decreasing)} \qquad (2.7)$$

The second operation amplifier in the VCO circuit is a comparator. Its output is a square wave whose level is positive whenever the (-) terminal voltage level is more negative than the (+) terminal voltage level. As seen in Fig. 2.9, there is a reference voltage level (V_3) on the (+) terminal. Its value equals half the positive voltage supply value ($V^+/2 = 2.5V$), which provides a 50% duty cycle of the square wave at the comparator output. The (+) terminal voltage level varies around this reference voltage level. When the analog switch is on, a 51 kohm resistance is connected to ground as seen in Fig. 2.9 (a). The voltage level at the (+) terminal is then

$$V_2 = \frac{51 \times 10^3}{(51+10) \times 10^3} \times 2.5 = 2.1V$$

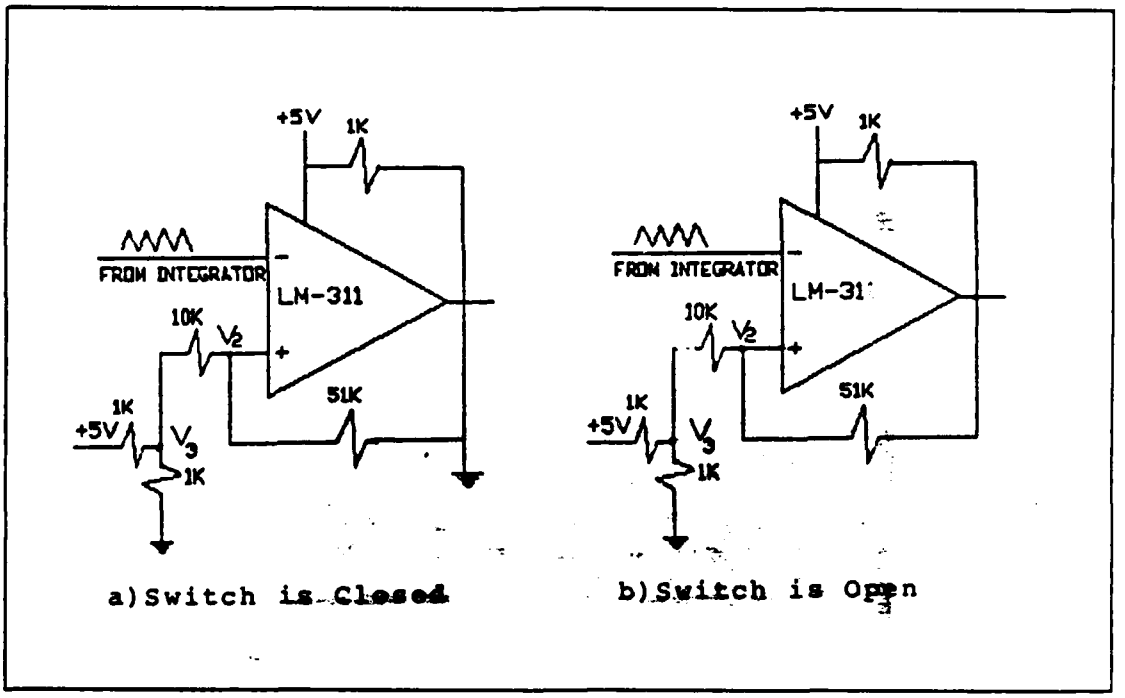


Figure 2.9 Comparator Circuit Diagram.

When the analog switch is off, then the 51 kohm resistance is connected to +5V via the 1 kohm resistor. Superposition gives for V_2,

$$V_2 = [\frac{(51+1) \times 10^3}{(51+1+10) \times 10^3}] \times 2.5 + [\frac{10 \times 10^3}{(51+10+1) \times 10^3}] \times 5 = 2.9V$$

As the switch condition changes, the output voltage levels of the comparator and integrator change. During that time the voltage level changes approximately 0.8V at both outputs. In the experimental circuit this value was measured as 0.85V. By using this result we can calculate the input voltage level versus output frequency of the VCO as

$V_1 = V_c/2$ from Eq. 2.6, when $t = 0$

$V_1 = V_c/2 - 0.85 = (V_c/2)[1-(T/2)/(RC)]$ from Eq. 2.7, when $t = T/2$. Therefor, the characteristic equation for the VCO is

$$f = \frac{V_c}{3.4RC} \tag{2.8}$$

The third operational amplifier of Fig. 2.7 is also a comparator used to convert the unipolar square wave output of the second operation amplifier to a bipolar square wave required for the CMOS XOR (phase detector) input.

Calculated and measured input voltage versus output frequency characteristic of the VCO is shown on Fig. 2.10. Sensitivity of the VCO is the frequency deviation at the output for various input control voltage and is the slope of the characteristic. For the experimental system VCO, the modulation sensitivity (K_3) is calculated to be 8.9 kHz/V while the measured value is approximately 8.1 kHz/V.

C. STABILITY ANALYSIS OF THE PLL

We consider the behavior of the PLL when locked and while a modulation or disturbance is applied to the input signal phase. In this condition the general linear equation (from Ref.5) is

$$\frac{d\Phi_o}{dt} = K[\Phi_i(t) - \Phi_o(t)] * g(t)$$

where, * represents convolution, Φ_o is the phase of the VCO output signal, Φ_i is the phase of the input signal, K is open loop gain, and g(t) is the loop filter impulse response.

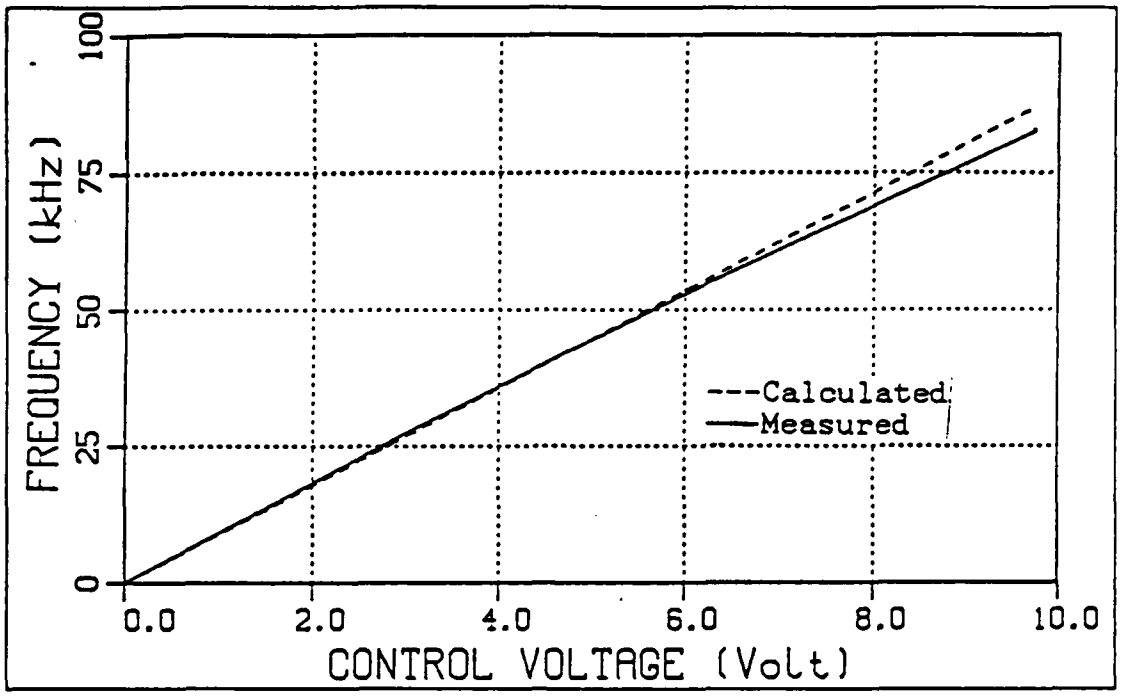


Figure 2.10 Charecteristic of VCO.

It is easy to solve this differential equation using the Laplace transform to find the loop transfer function. Laplace transformation yields

$$s\Phi_o(s) = K[\Phi_i(s) - \Phi_o(s)]G(s)$$

Then, the transfer function of the PLL becomes

$$H(s) = \frac{\Phi_o(s)}{\Phi_i(s)} = \frac{KG(s)}{s + KG(s)} \qquad (2.9)$$

Fig. 2.11 shows this linear model of the PLL.

The filter transfer function G(s) is given by Eq. 2.5. K is the product of the phase detector sensitivity K_1, DC amplifier gain K_2, and the VCO modulation sensitivity K_3. K_2 was selected as unity (The actual value of K_2 is -3 which is included in G(s) of Eq. 2.5. In the realization of the circuit of Fig. 2.11, a summing junction is used instead of a difference amplifier and K_2 provides the negative feedback.)

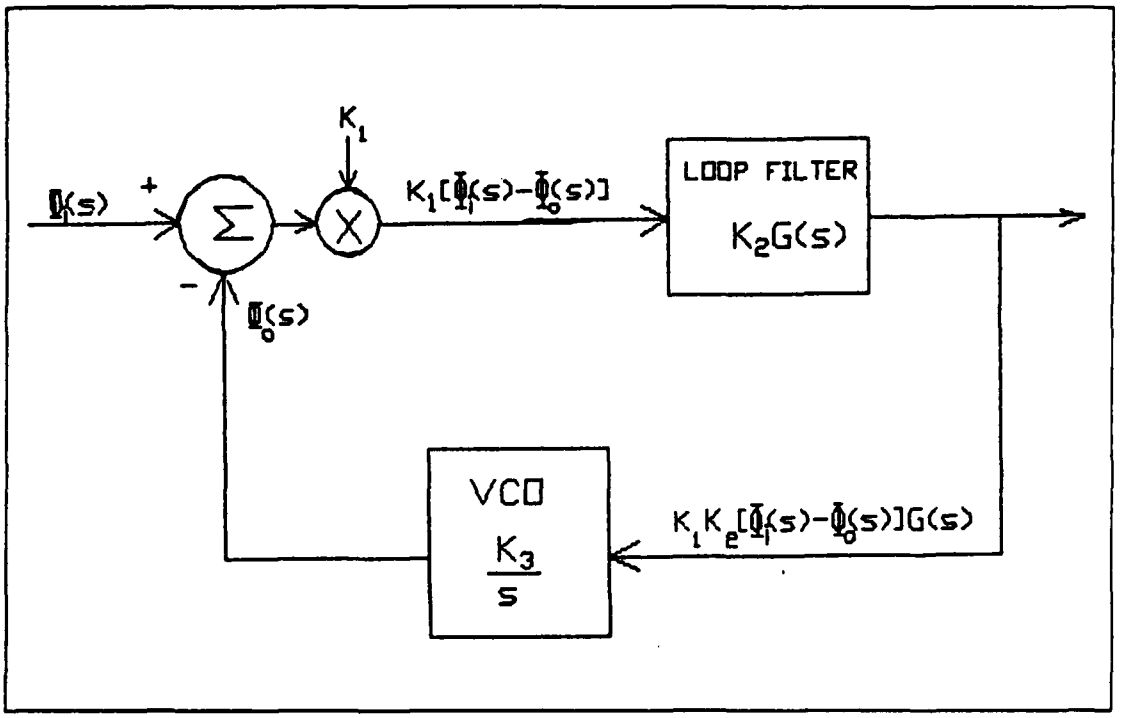


Figure 2.11 Linear Model of the PLL.

From before, $K_1 = 3.18$ V/rad, and $K_3 = 8.1 \times 10^3 \times 2\pi$ rad/sec/V. Therefore,

$$K = K_1K_2K_3 = 3.18 \times 1 \times 8.1 \times 10^3 \times 2\pi = 161842.28 \text{ rad/sec.}$$

So, the transfer function of the experimental PLL is;

$$H(s) = \frac{1670074528(s + 19607.8)}{s^3 + 71873.45s^2 + 1737554973s + 3.2746493 \times 10^{13}}$$

Computer simulation results for the Bode plot and the step response of this transfer function are shown as Fig. 2.12 and Fig. 2.13 (a) respectively. The measured step response is shown on Fig. 2.13 (b). As seen on the Bode plot the PLL is stable because of the positive phase margin.

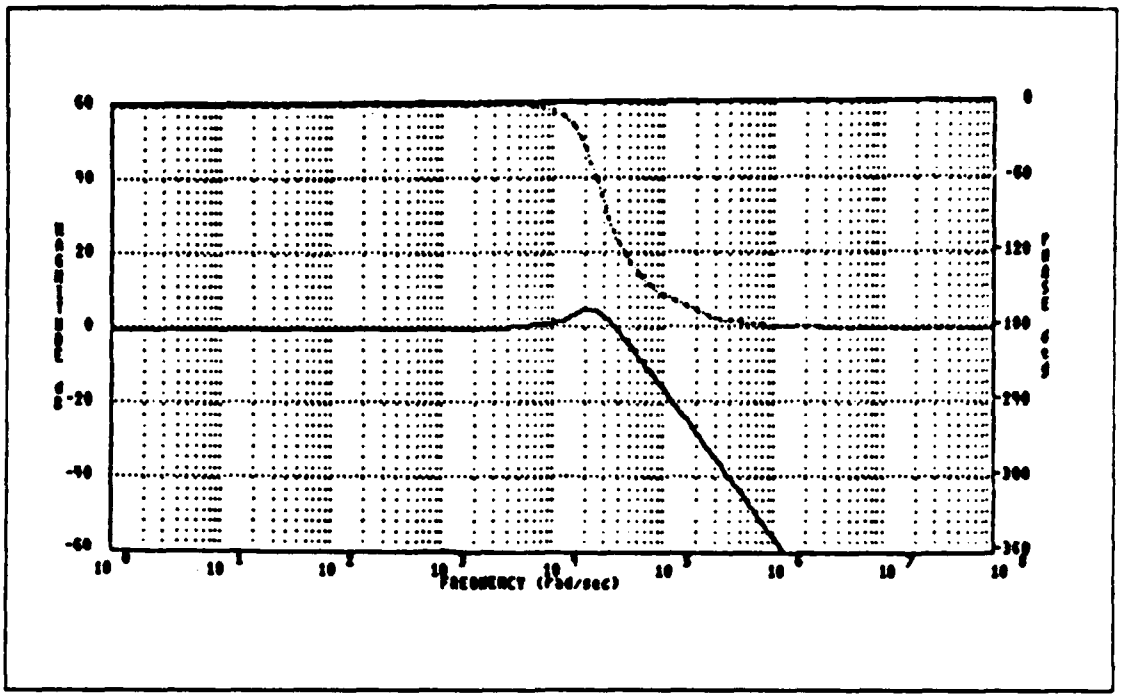


Figure 2.12 Bode Plot of the Experimental PLL.

D. THE EXPERIMENTAL CIRCUIT BANDPASS FILTER AND SUMMER

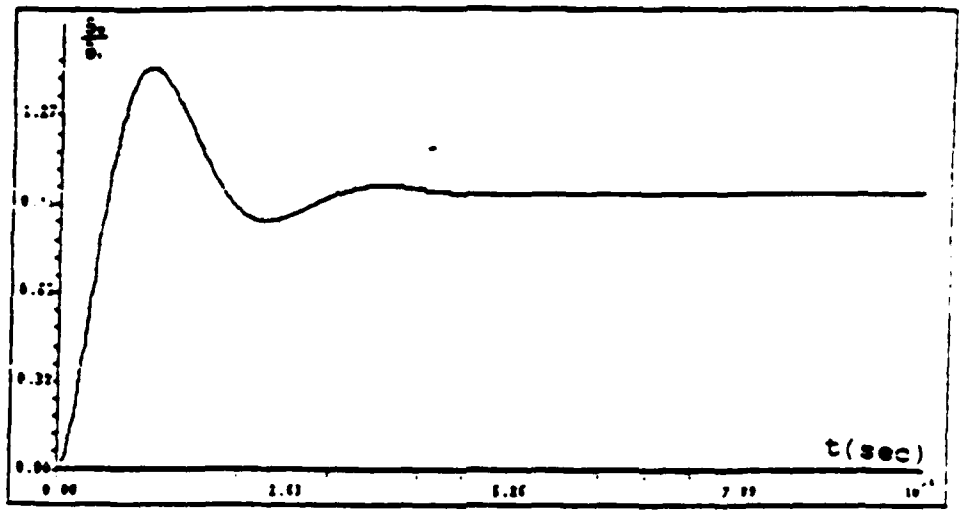
A bandpass filter was used between the white Gaussian noise generator (Elgenco-603a) and summer to obtain narrow band Gaussian noise. See Fig. 2.1. A biquad General Immittance Converter (GIC) bandpass filter was constructed [Ref. 7]. Circuit diagram of this filter is shown in Fig. 2.14.

The transfer function of the filter is

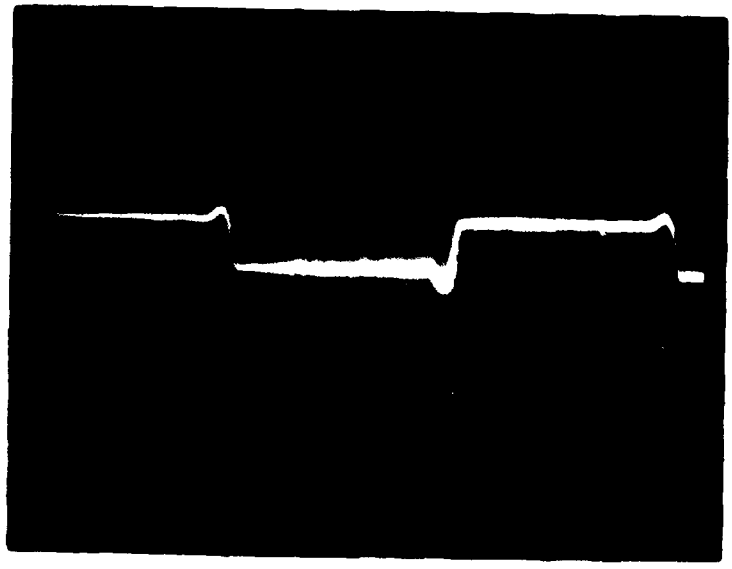
$$H(s) = \frac{2(w_p/Q)s}{s^2 + (w_p/Q)s + w_p^2}$$

where, $w_p = 1/(RC)$ = pole radian frequency, and Q = quality factor.

Frequency Shift Keying (FSK) modulation was used during the probability density function measurement at the PLL output. Frequency deviation for FSK modulation was ± 2.5 kHz, so the filter bandwidth was chosen to be 5 kHz. The pole frequency was set at 60 kHz. Capacitance and resistance values were chosen to be 2 nF and 1.4 kohm respectively. Since $w_p = 1/RC$, then $w_p = 357142.86$ rad/sec and Q = (pole frequency/bandwidth) = 12. Thus the filter transfer function becomes



a) Computer Simulation



b) Measured

Figure 2.13 Step Response of the Experimental PLL.

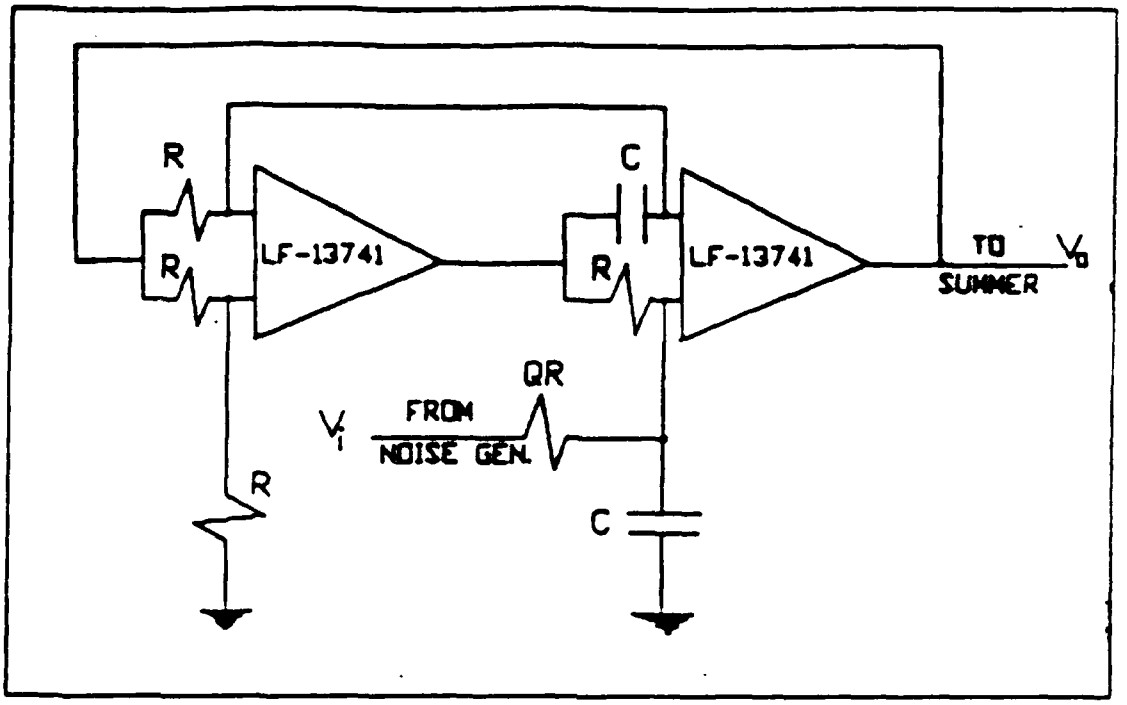


Figure 2.14 Biquad GIC Bandpass Filter.

$$H(s) = \frac{59523.8s}{s^2 + 29761.9s + 1.2755102 \times 10^{11}}$$

Fig. 2.15 shows a computer plot of H(s), and Fig. 2.16 shows the measured magnitude of the transfer function obtained from a digital signal processor (SD-360). Measured pole frequency of the BPF is 59 kHz. The difference between the calculated and measured transfer functions comes from non ideal effects of the operational amplifier. Also the BPF circuit companent values are not exactly the same as the calculated values.

An analog voltage multiplier (AD-534J) was used as a summer. Its circuit diagram is shown in Fig. 2.17. The output function of this circuit is [Ref. 8]

$$V_{out} = 10(Z_2 - Z_1) / (X_1 - X_2) + Y_1$$

In the experimental circuit, Z_2 is ground, Z_1 is the noise input, Y_1 is the carrier or modulated signal input, X_1-X_2 is set equal to 1.5V.

The output of the summer is applied to a zero crossing comparator used as a hard limiter to obtain a square wave for the phase detector input.

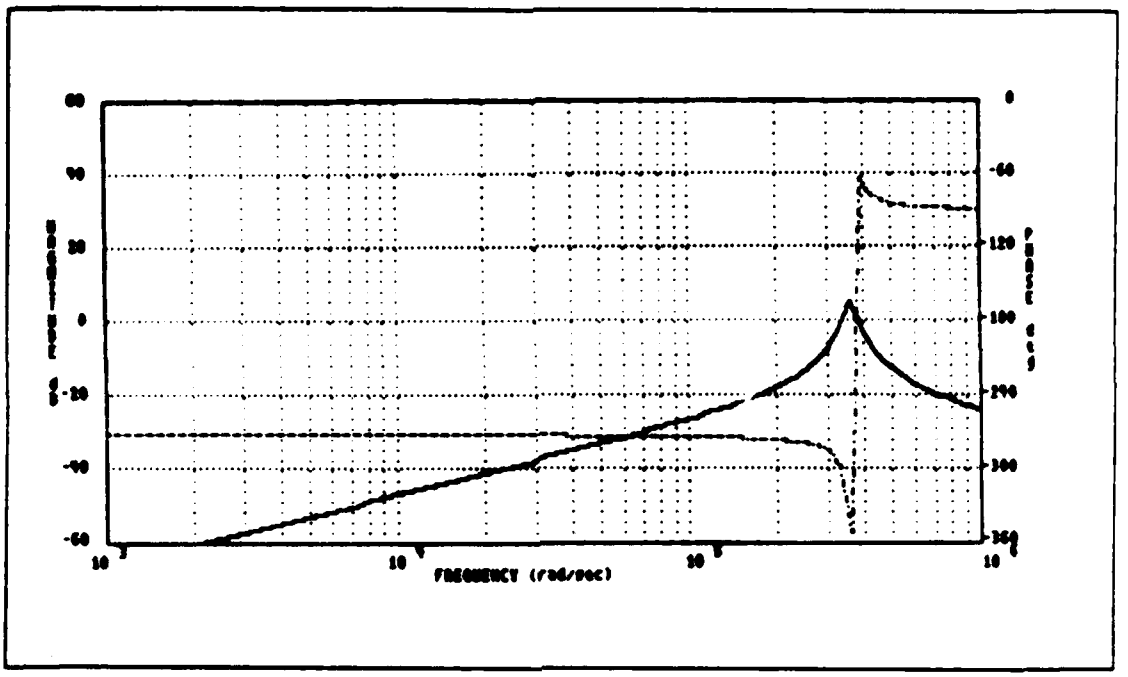


Figure 2.15 Transfer Function Of The BPF(Computer Simulation).

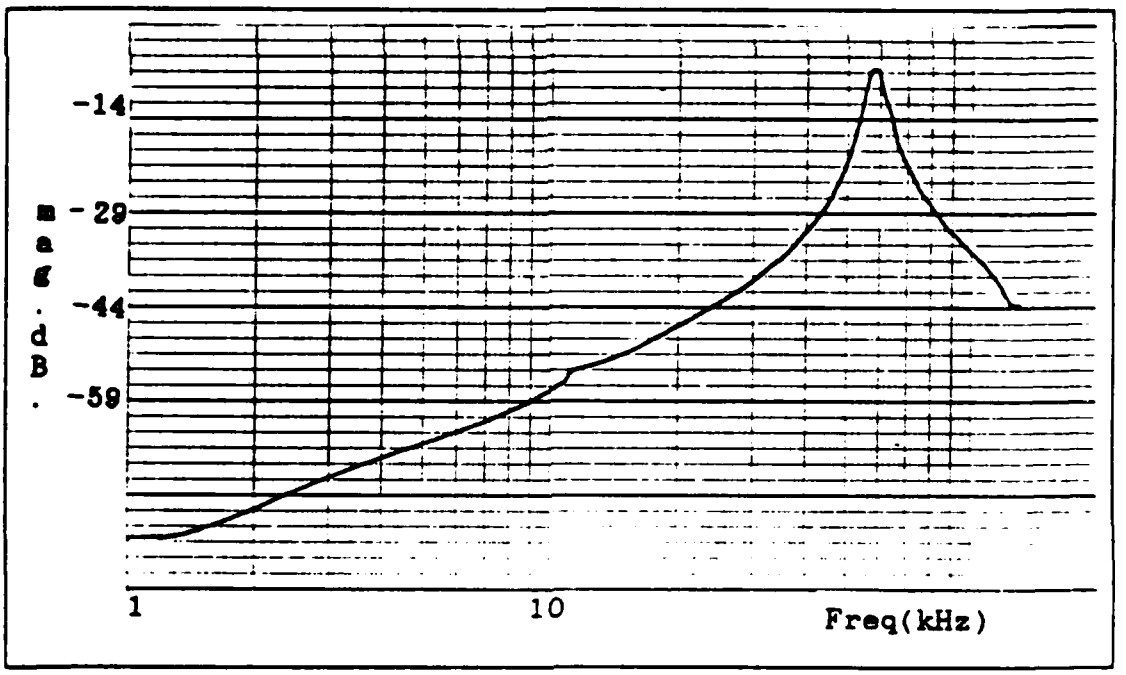


Figure 2.16 Measured Transfer Function Of the BPF.

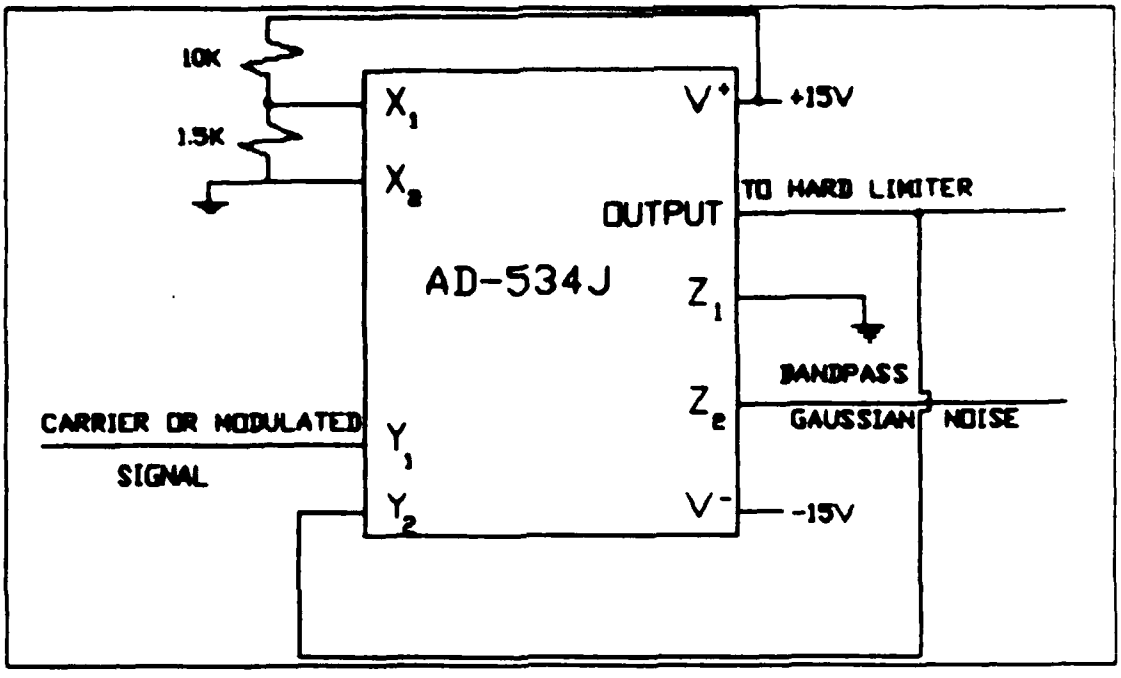


Figure 2.17 Circuit Diagram Of The Summer..

III. MEASUREMENT OF THE PROBABILITY DENSITY FUNCTION OF THE PLL OUTPUT

Probability density functions of the PLL output were measured using the digital signal processor (SD-360). All measurements were made of the output of the filter and amplifier following the PLL. Three kinds of input signals were used: carrier only (no-modulation), frequency shift keying (binary data), frequency modulated signal (triangular wave modulating voltage). In all cases, measurements were made for various levels of the noise power added to these signals.

A. CARRIER ONLY

The system is shown in Fig. 3.1.

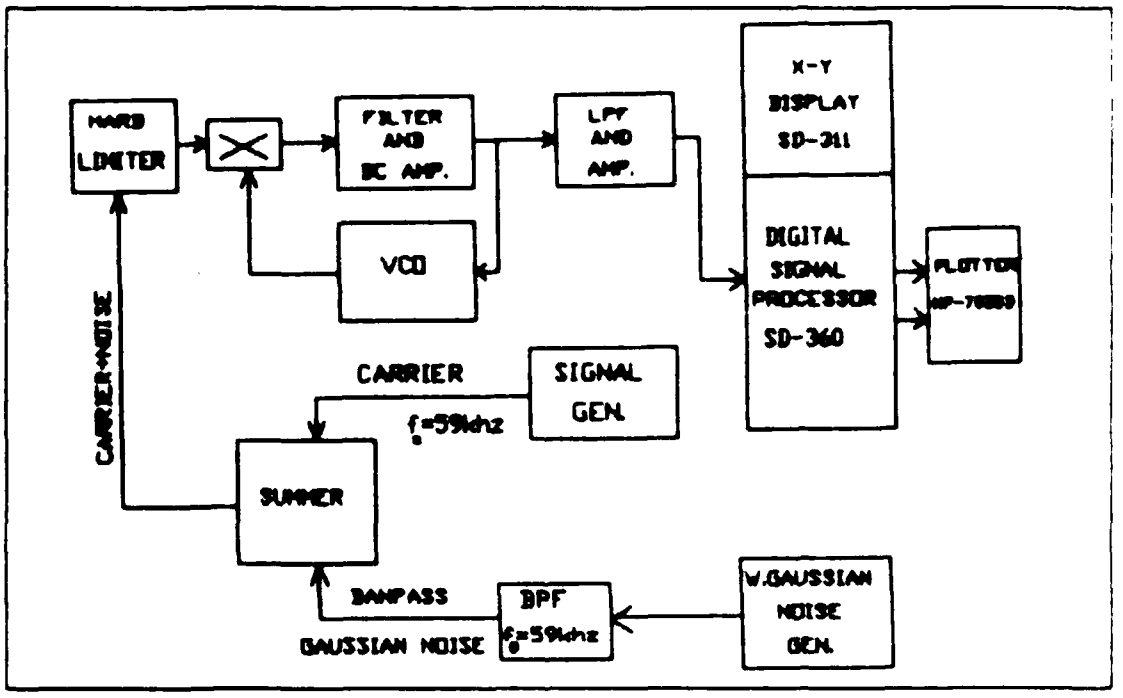


Figure 3.1 System for Unmodulated Carrier.

The carrier is a sinusoidal wave with frequency set to 59 khz which equals the bandpass filter center frequency. Figs 3.2 through 3.19 show output voltage and its probability density function for various values of input signal-to-noise ratios.

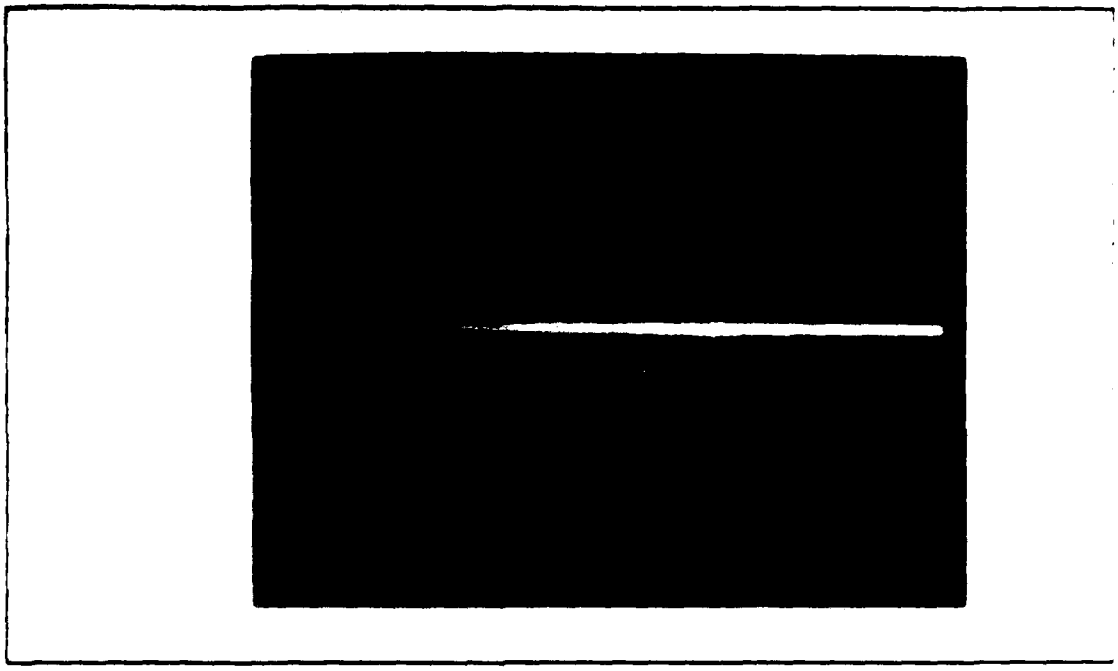


Figure 3.2 Output of the PLL for Carrier (No Noise).

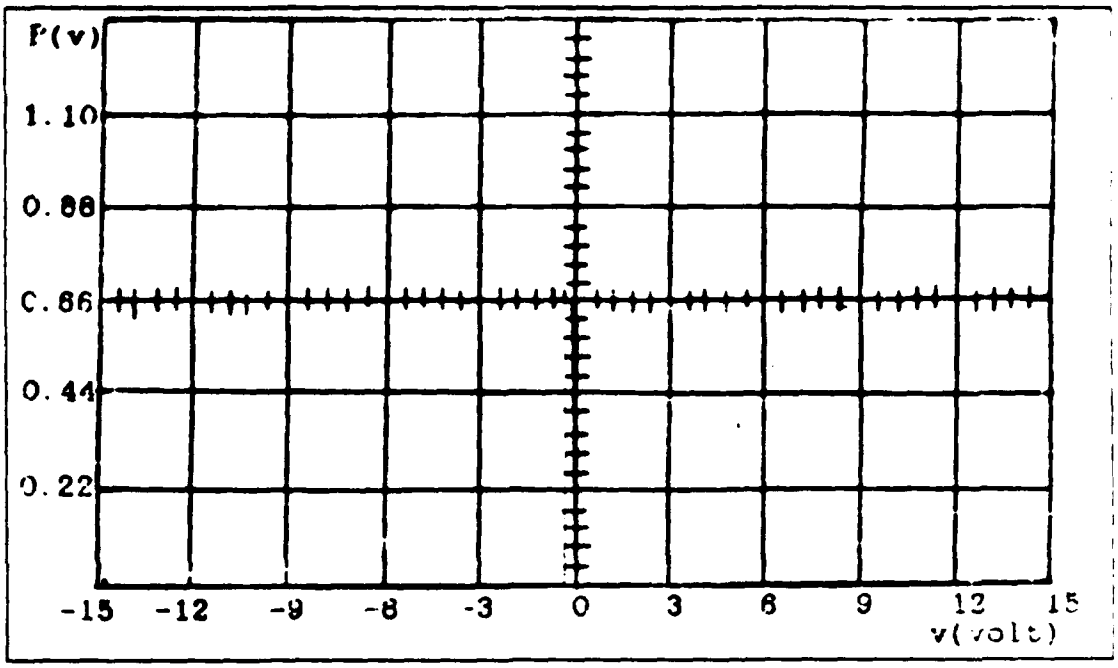


Figure 3.3 Probability Density Function for Carrier (No Noise).

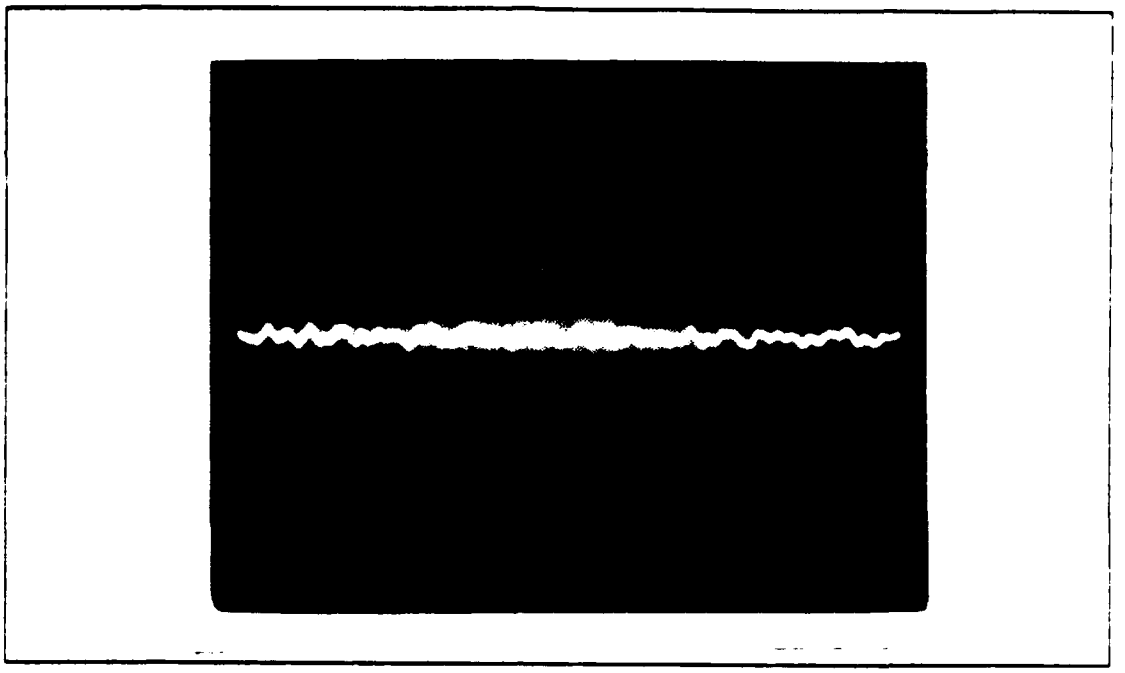


Figure 3.4 Output of the PLL for Carrier Plus Noise (SNR = 20 dB).

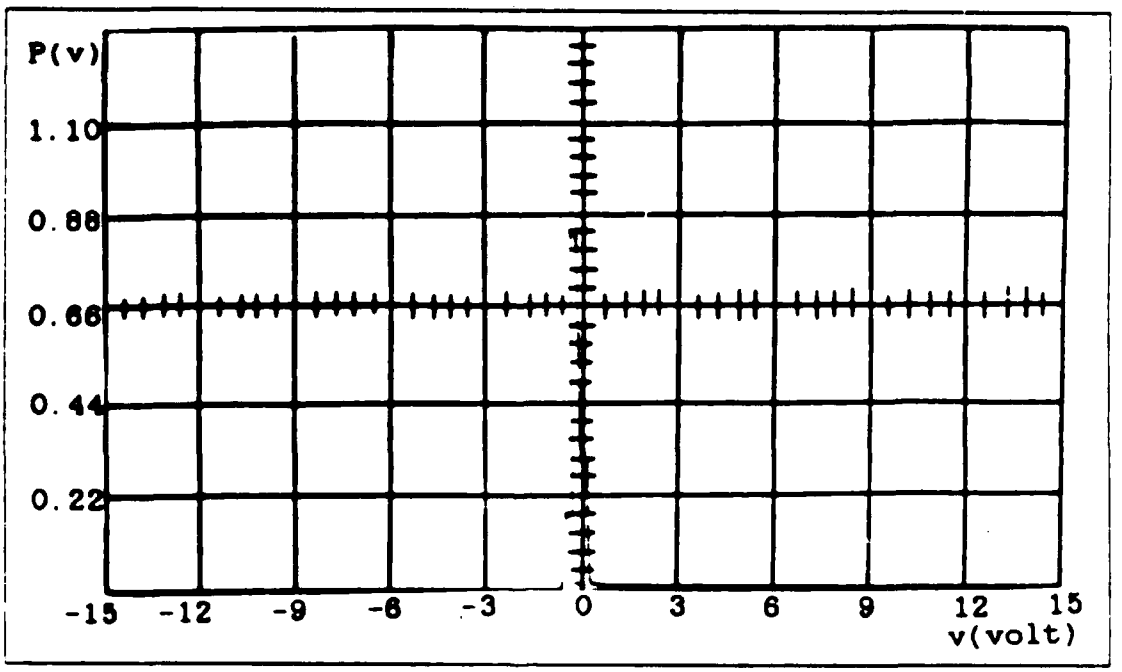


Figure 3.5 Probability Density Function for Carrier Plus Noise (SNR = 20 dB).

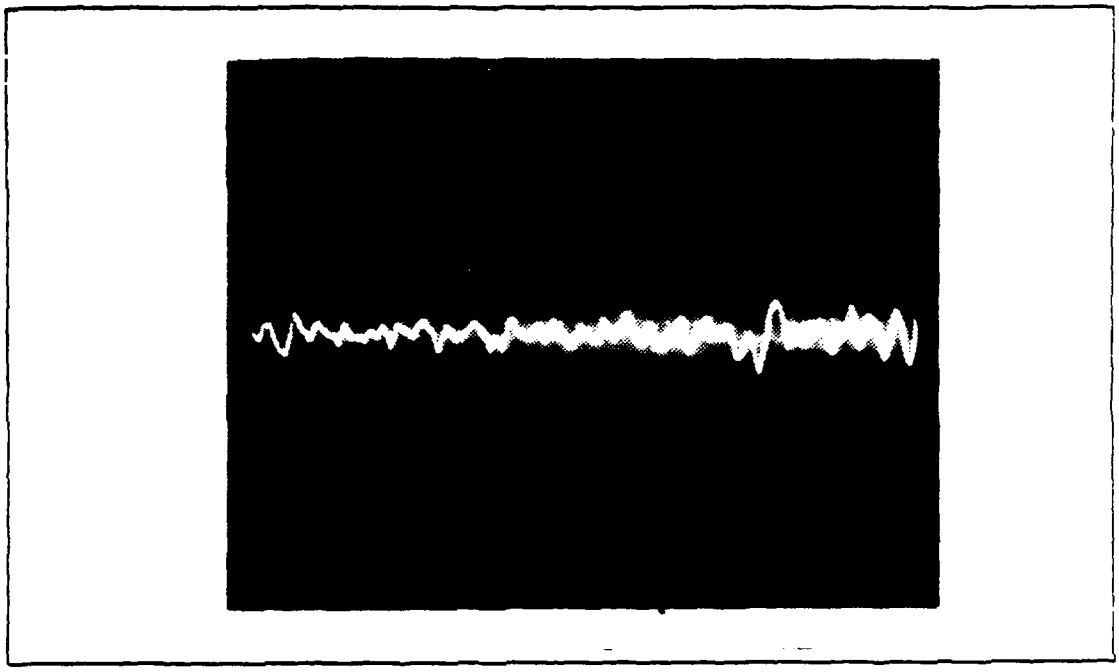


Figure 3.6 Output of the PLL for Carrier Plus Noise (SNR = 10 dB).

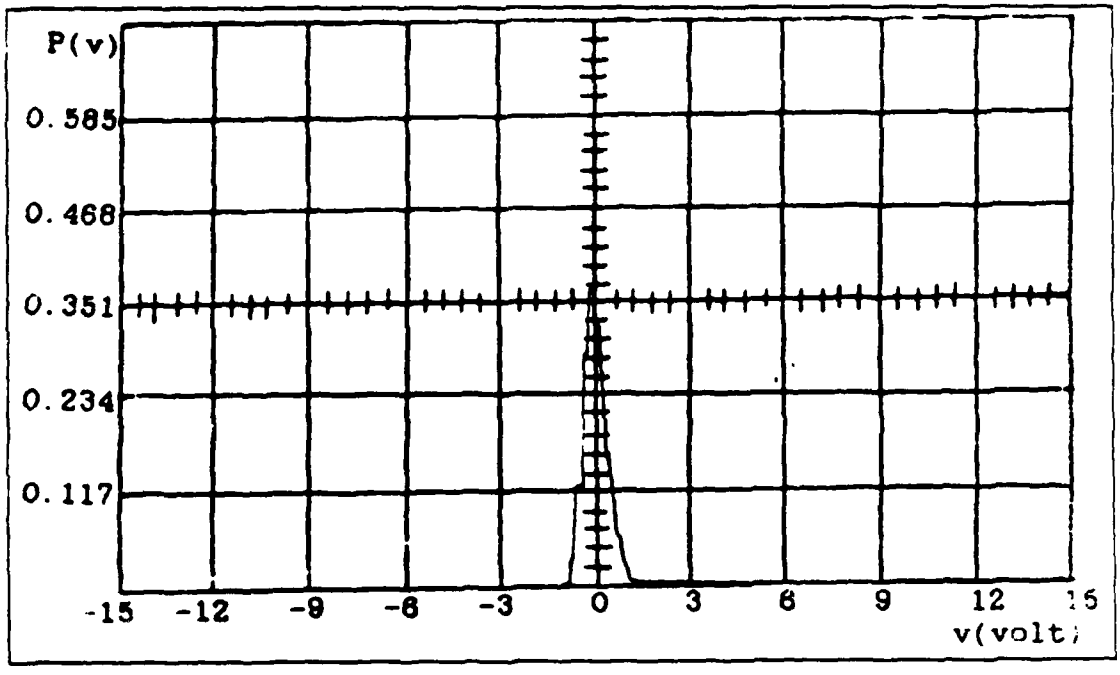


Figure 3.7 Probability Density Function for Carrier Plus Noise (SNR = 10 dB).

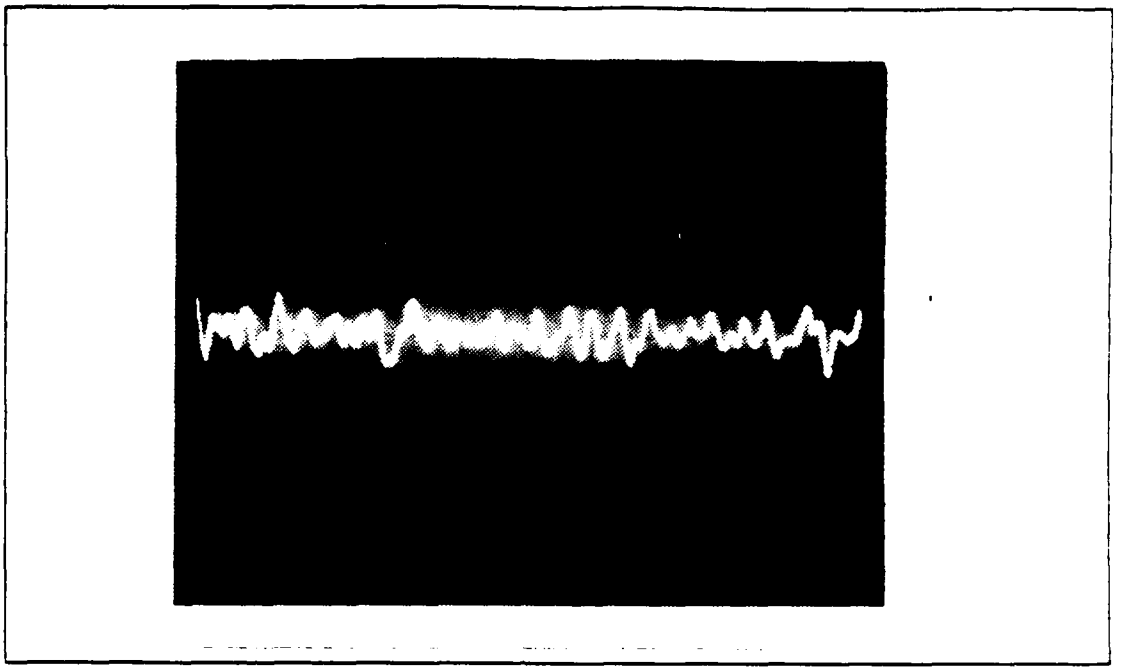


Figure 3.8 Output of the PLL for Carrier Plus Noise (SNR = 8 dB).

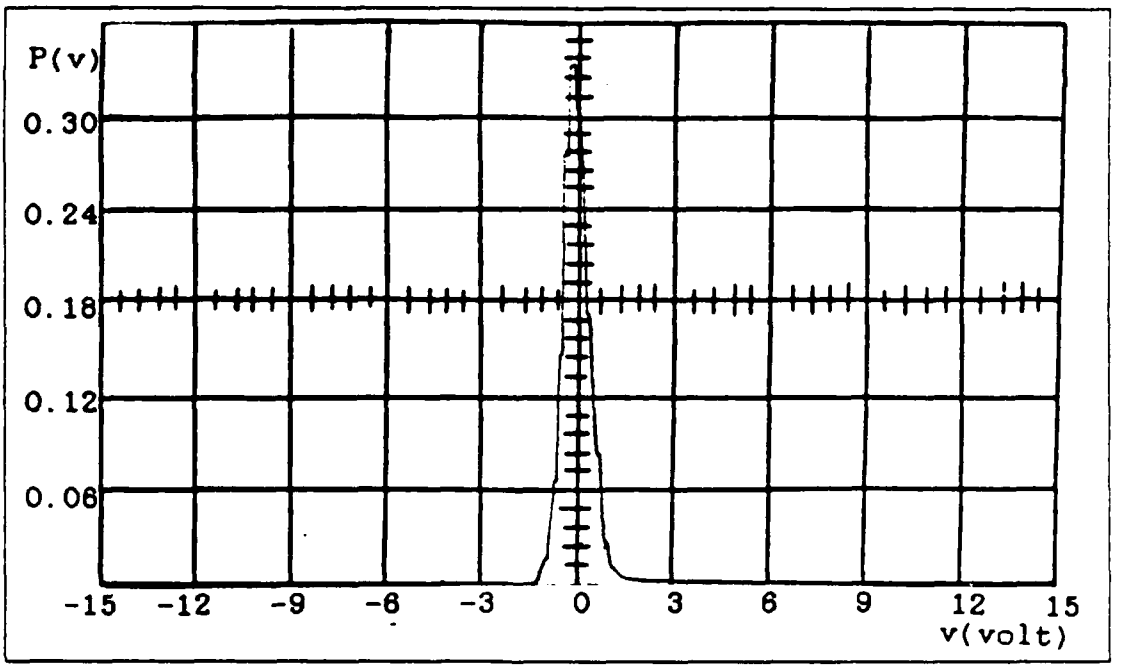


Figure 3.9 Probability Density Function for Carrier Plus Noise (SNR = 8 dB).

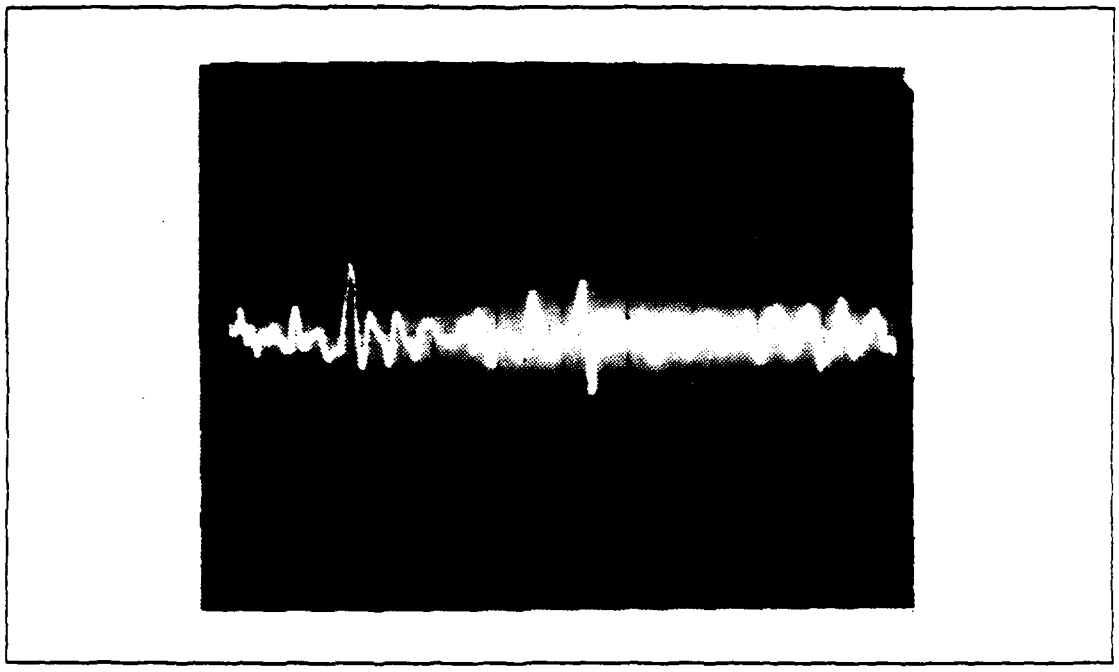


Figure 3.10 Output of the PLL for Carrier Plus Noise (SNR = 6 dB).

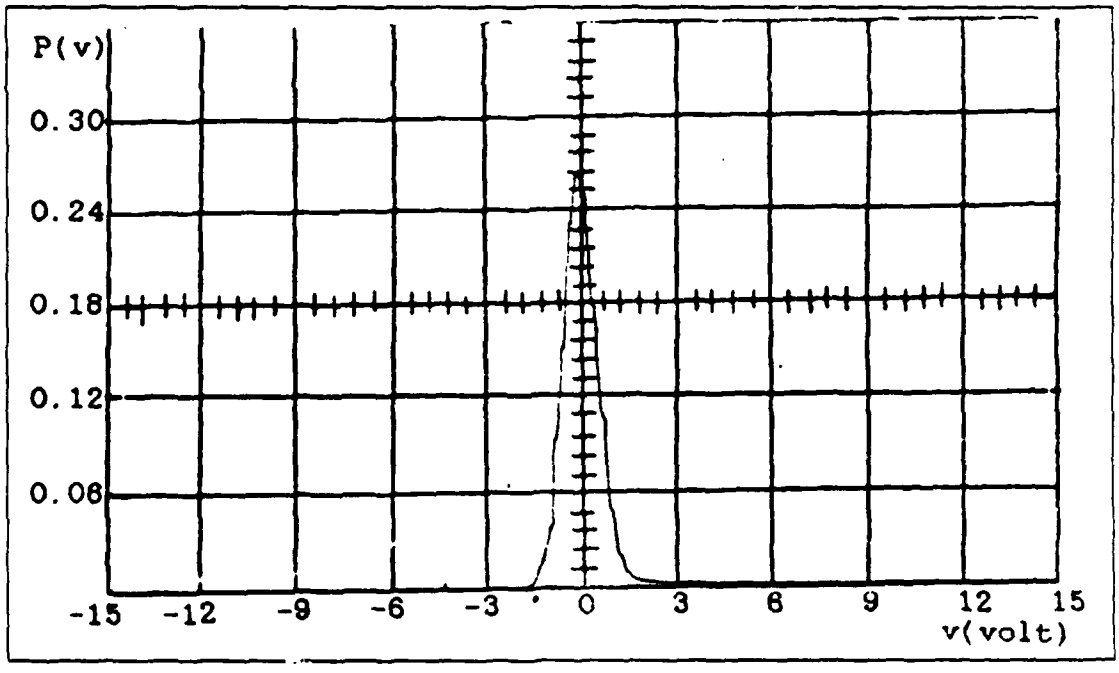


Figure 3.11 Probability Density Function for Carrier Plus Noise (SNR = 6 dB).

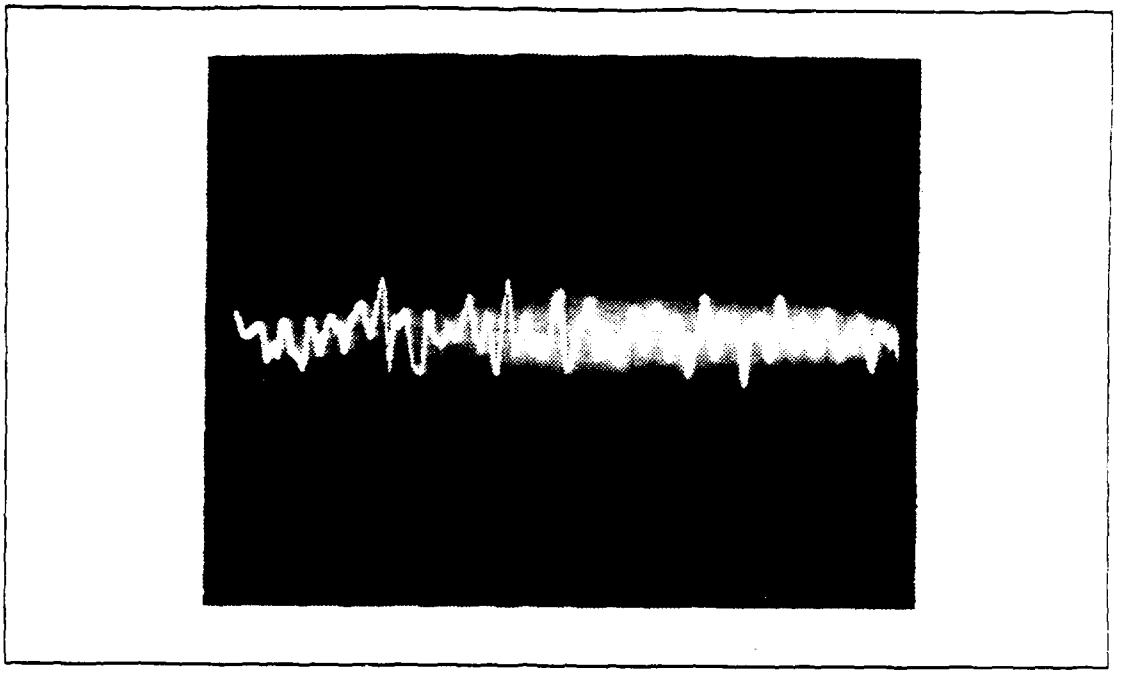


Figure 3.12 Output of the PLL for Carrier Plus Noise (SNR = 4 dB).

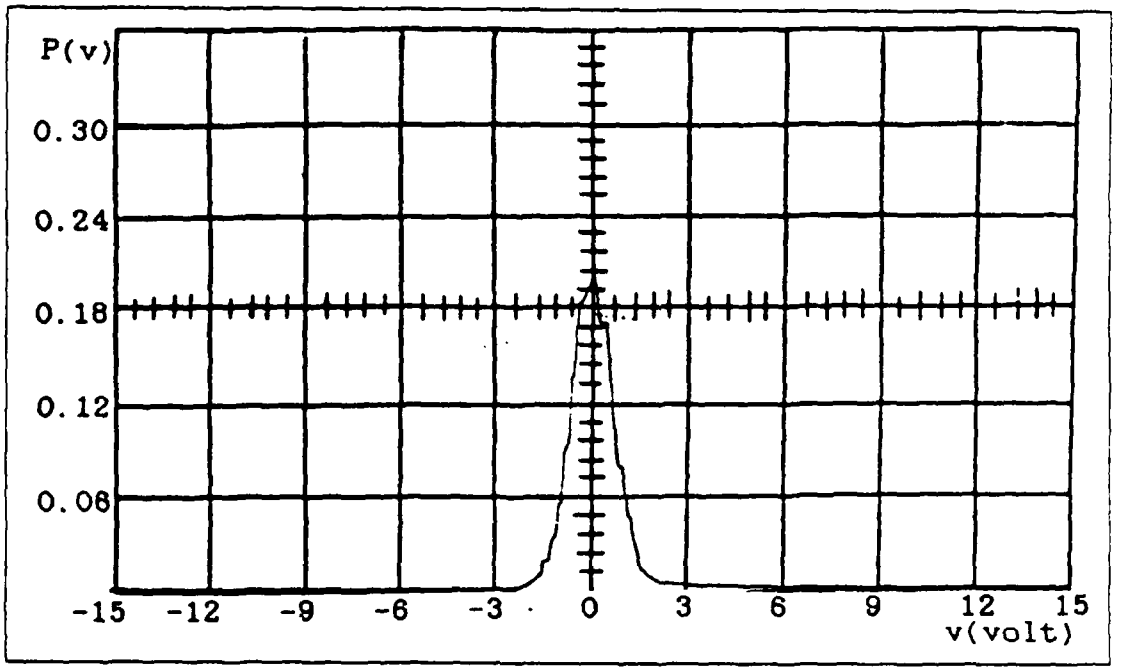


Figure 3.13 Probability Density Function for Carrier Plus Noise (SNR = 4 dB).

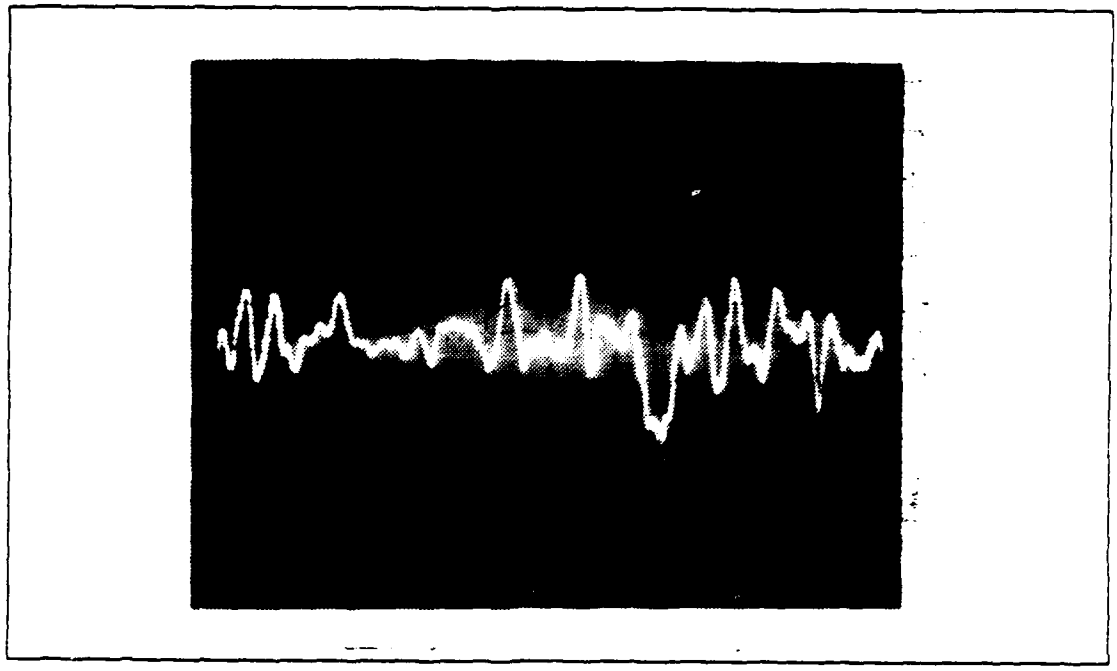


Figure 3.14 Output of the PLL for Carrier Plus Noise (SNR = 2 dB).

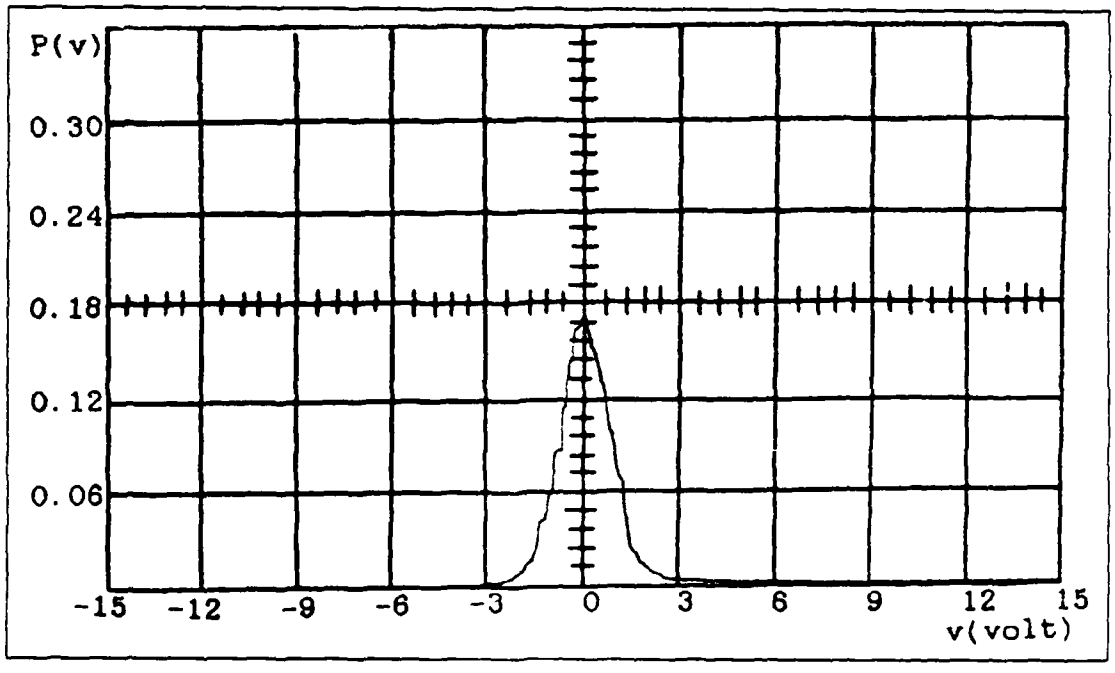


Figure 3.15 Probability Density Function for Carrier Plus Noise (SNR = 2 dB).

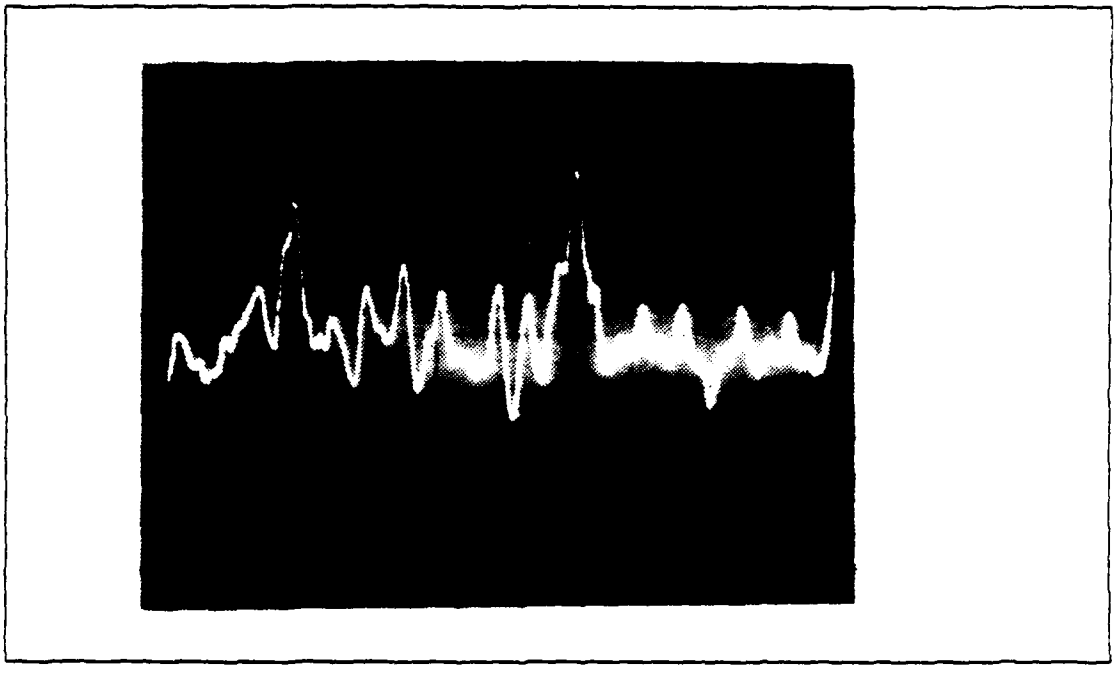


Figure 3.16 Output of the PLL for Carrier Plus Noise (SNR = 0 dB).

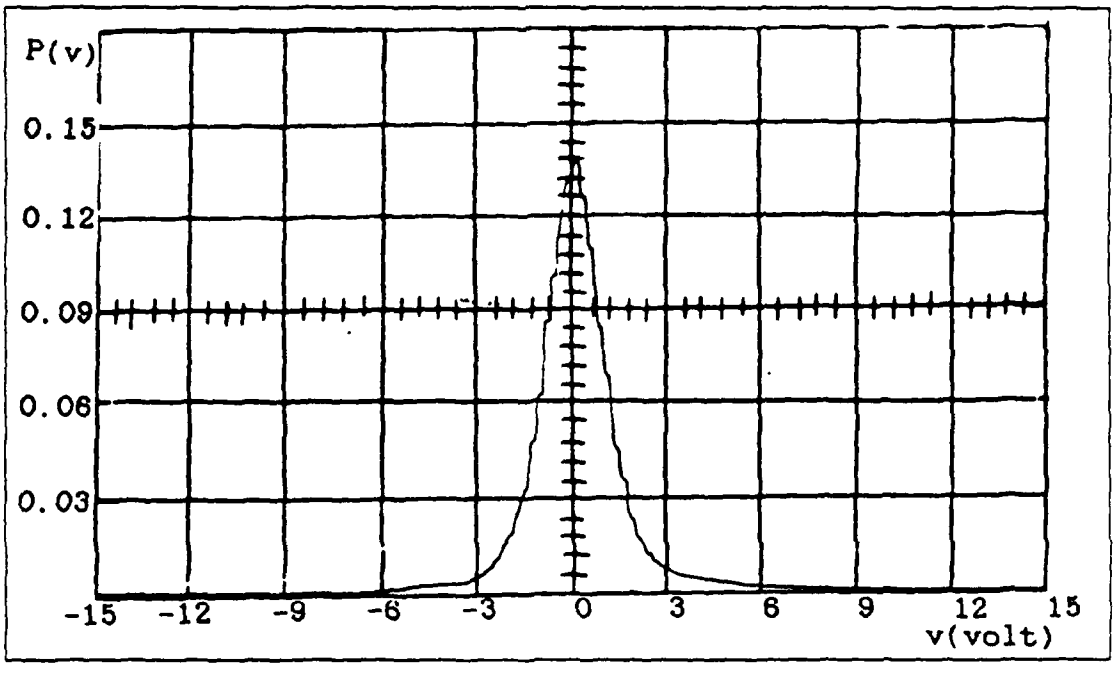


Figure 3.17 Probability Density Function for Carrier Plus Noise (SNR = 0 dB).

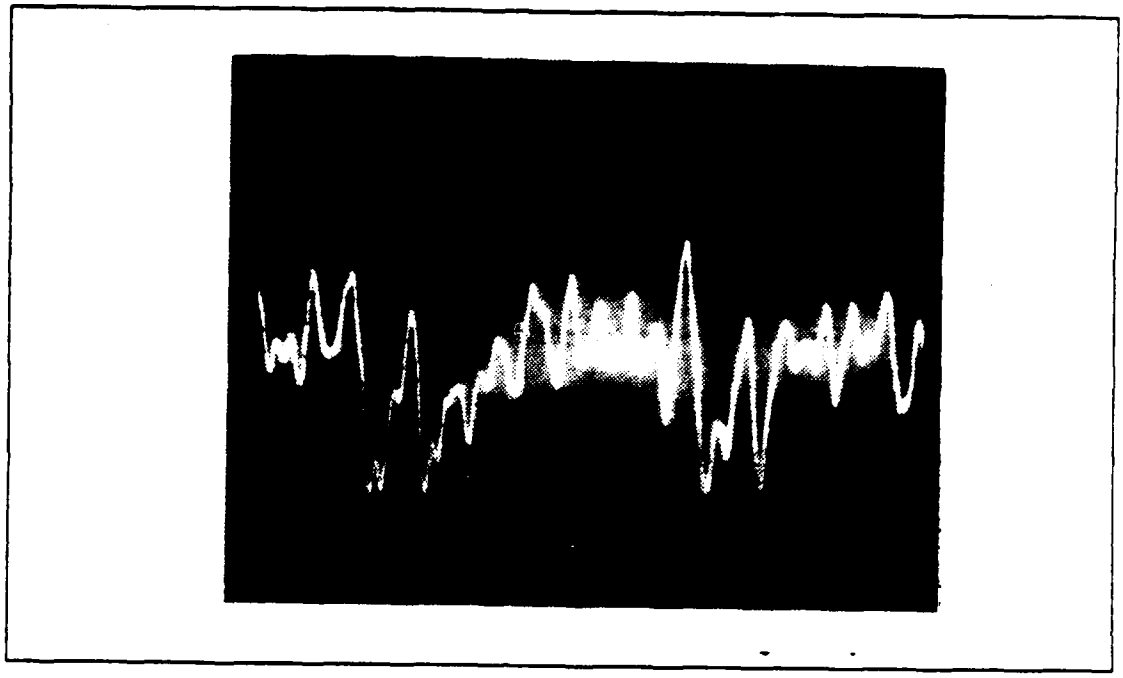


Figure 3.18 Output of the PLL for Carrier Plus Noise (SNR = -5 dB).

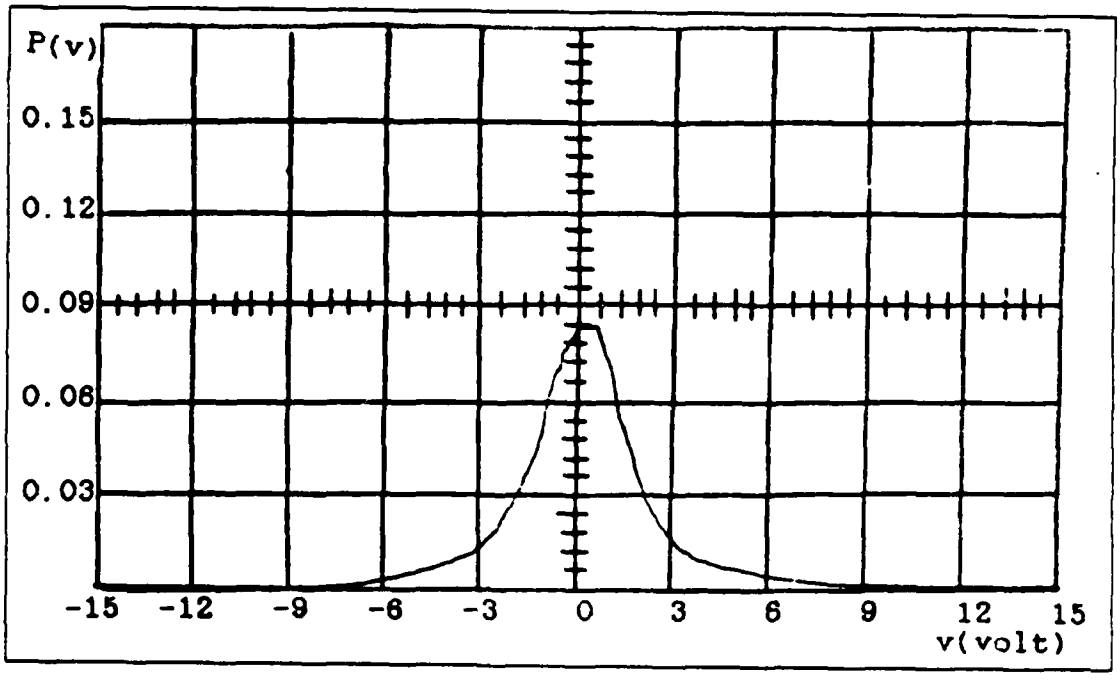


Figure 3.19 Probability Density Function for Carrier Plus Noise (SNR = -5 dB).

B. FREQUENCY SHIFT KEYING (FSK) MODULATED CARRIER

The modulated signal for this measurement was obtained by using two signal generators (Wavetek Model 142) as shown in Fig. 3.20. One provided the square-wave modulating voltage having a frequency of 700 Hz. The other one provided the carrier (sinusoidal wave) of frequency 59 kHz. The square-wave voltage when applied to the carrier signal generator VCG input created FSK modulated carrier. The square wave voltage levels define the frequency deviation of the carrier. Measurements were made for two different values of frequency deviation. The first measurements were made for a 5 kHz frequency deviation. The second measurements were for a 3.7 kHz frequency deviation. For the second measurements the BPF bandwith was set to 3.7 kHz by changing the value of resistance QR in Fig. 2.14. This changed the filter Q (quality factor) to 59/3.7 = 15.9. Figs. 3.21 through 3.38 show the output voltage and its probability density function for a frequency deviation of 5 kHz, and Figs. 3.39 through 3.56 for a frequency deviation of 3.7 kHz.

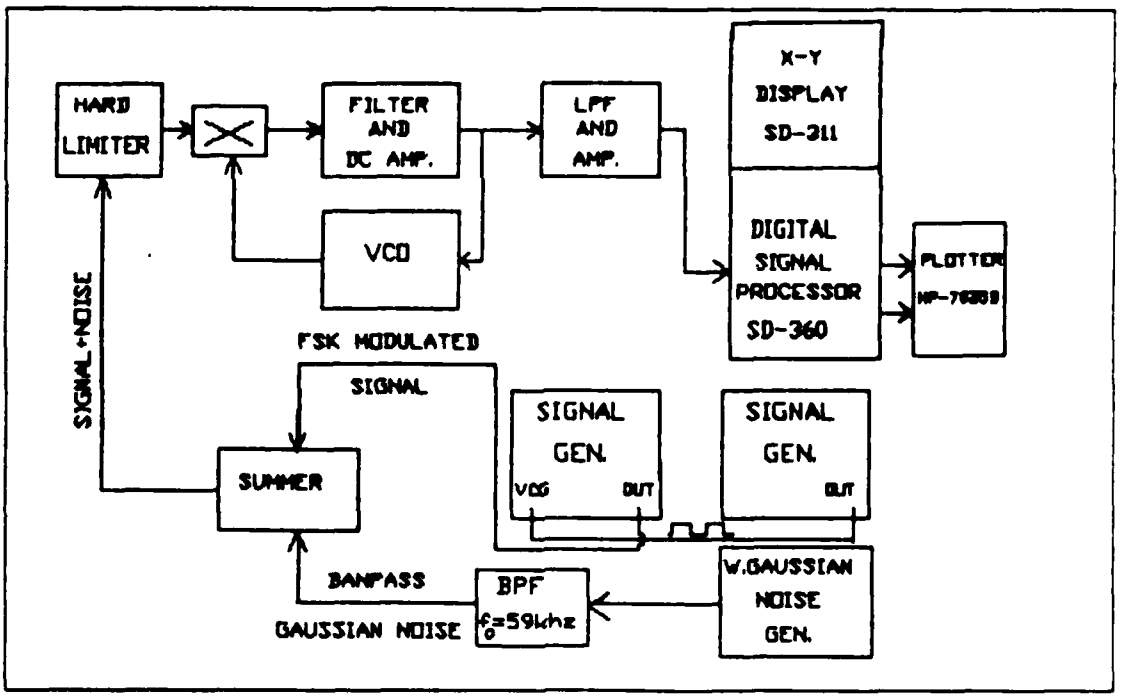


Figure 3.20 System for FSK Modulated Carrier.

1. **Output for FSK Modulation (Frequency Deviation = 5 kHz)**

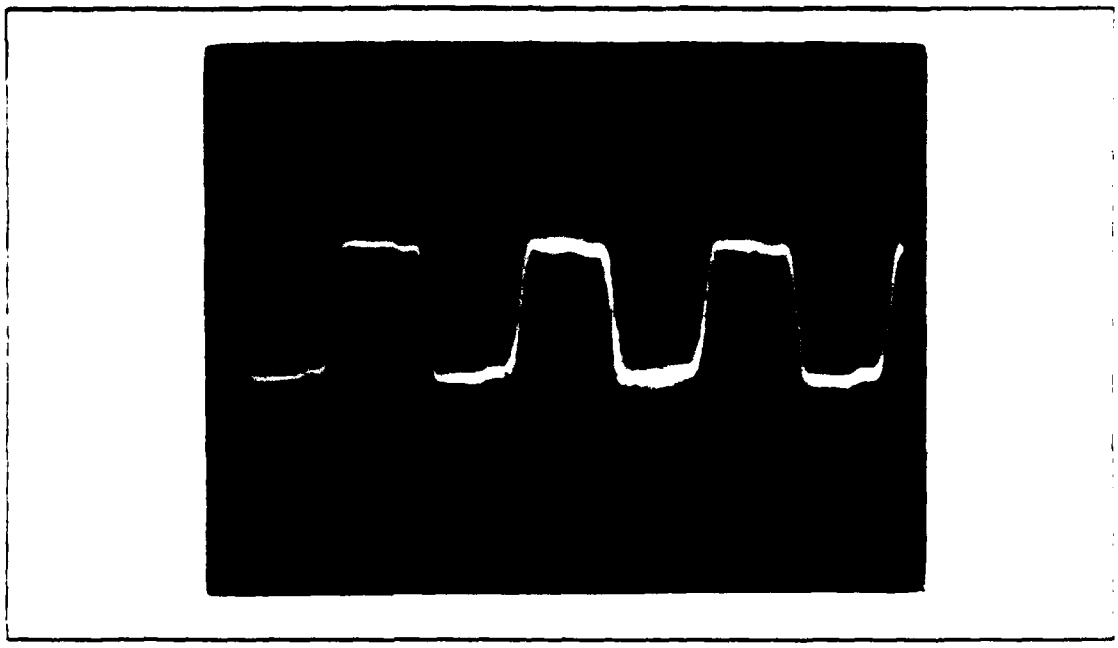


Figure 3.21 Output of the PLL for FSK Modulation (No Noise).

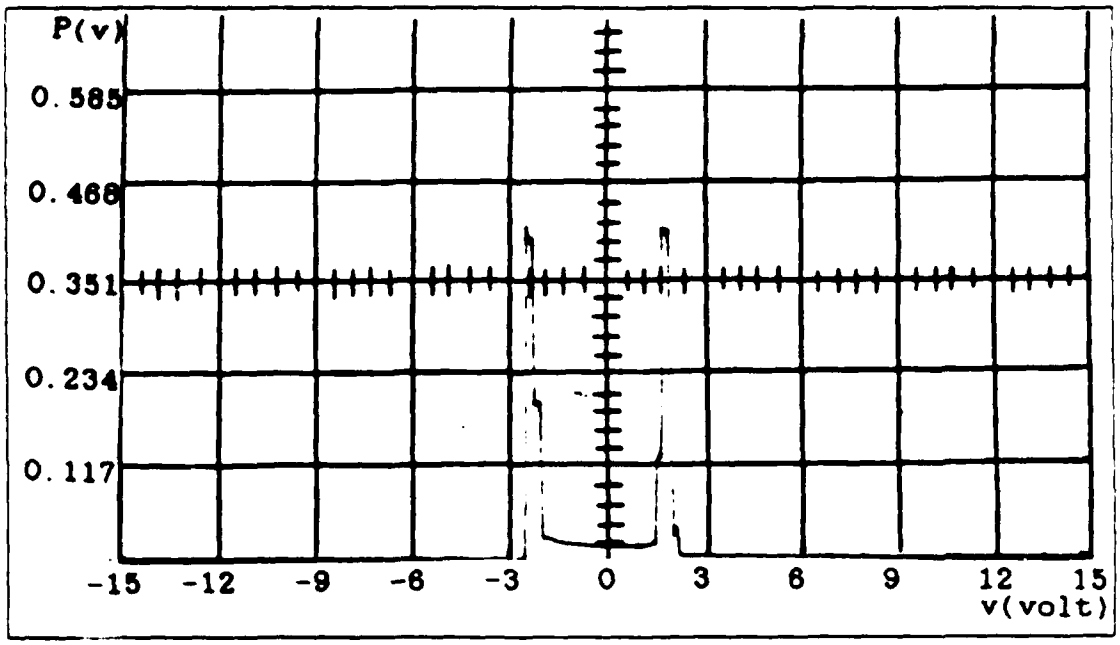


Figure 3.22 Probability Density Function for FSK Modulation (No Noise).

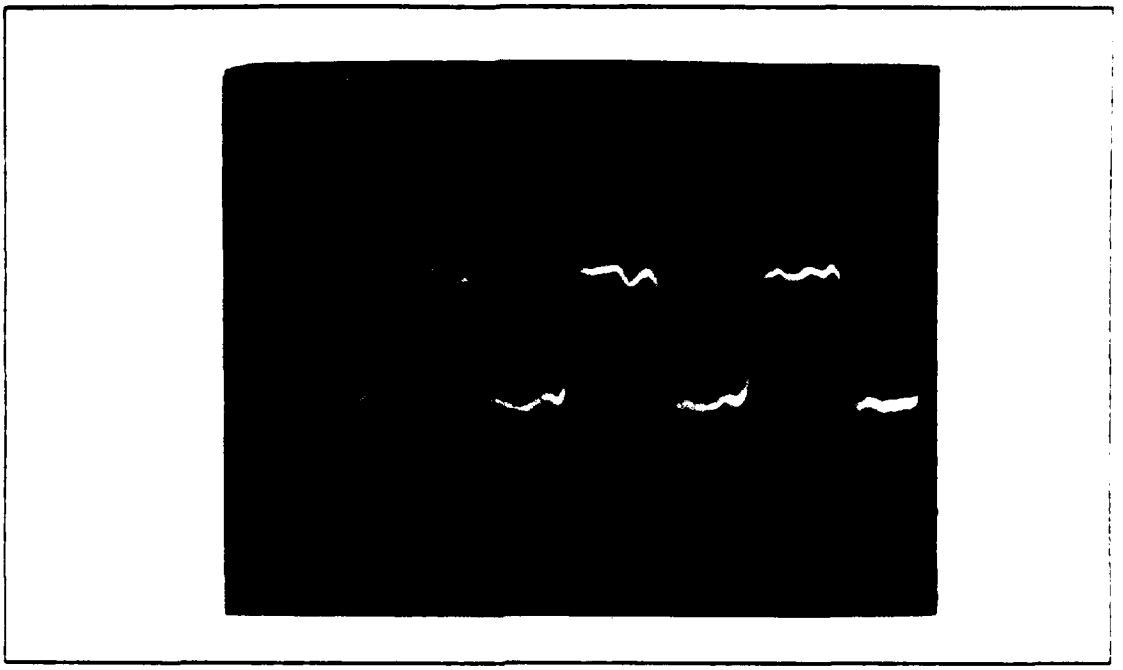


Figure 3.23 Output of the PLL for FSK Modulation Plus Noise (SNR = 20 dB).

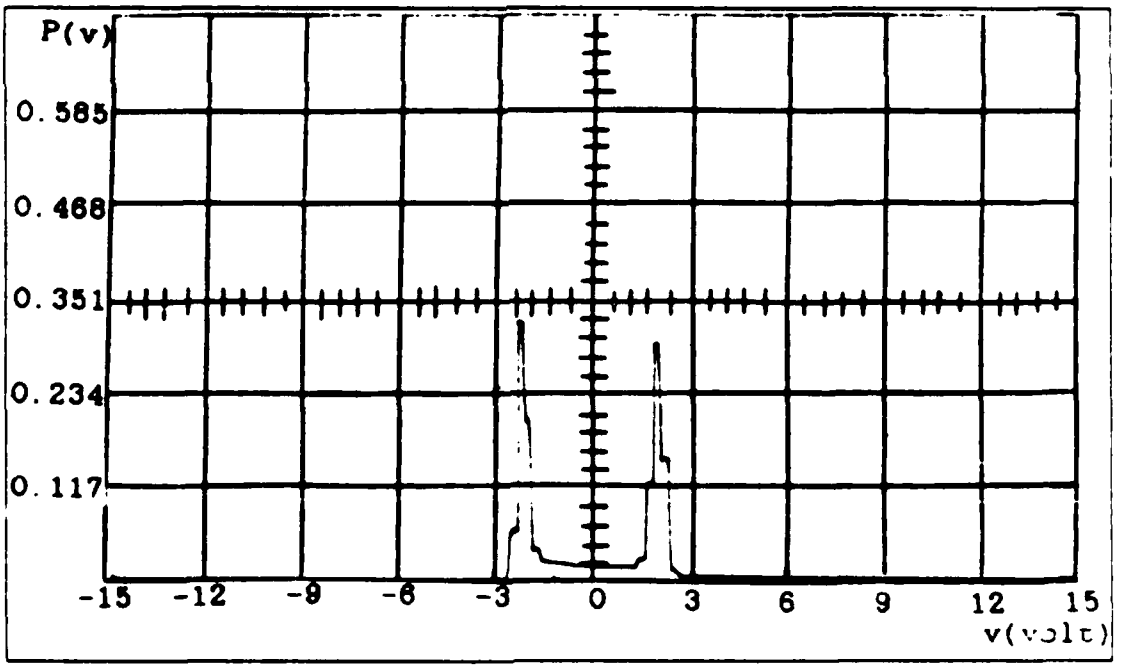


Figure 3.24 Probability Density Function for FSK Modulation Plus Noise (SNR = 20 dB).

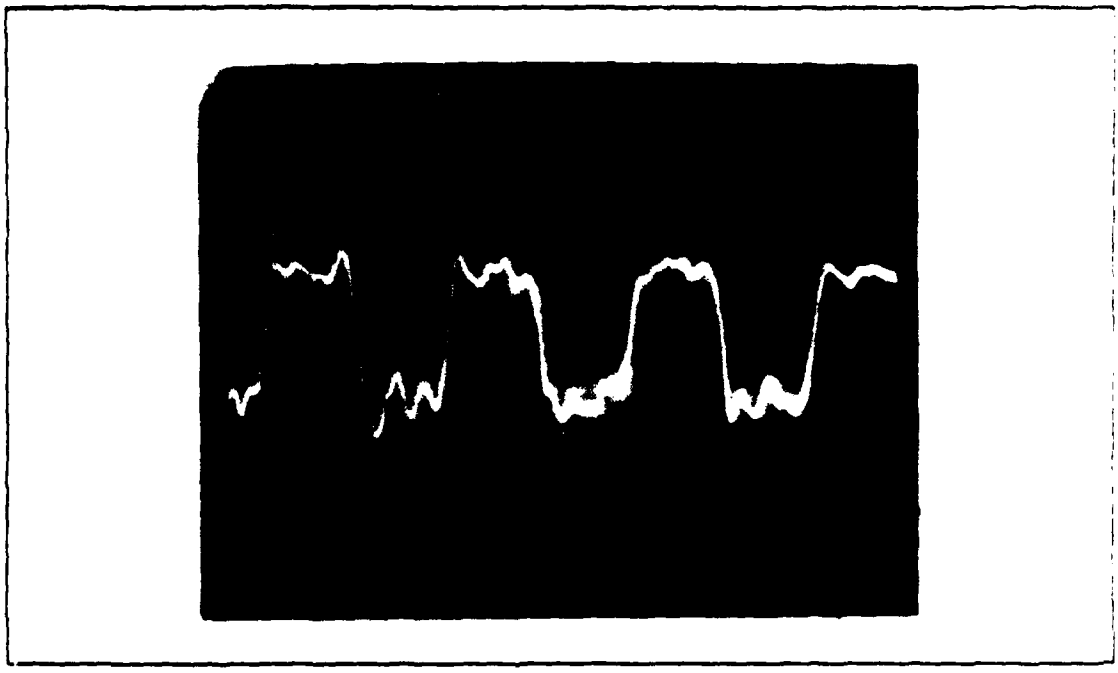


Figure 3.25 Output of the PLL for FSK Modulation Plus Noise (SNR = 10 dB).

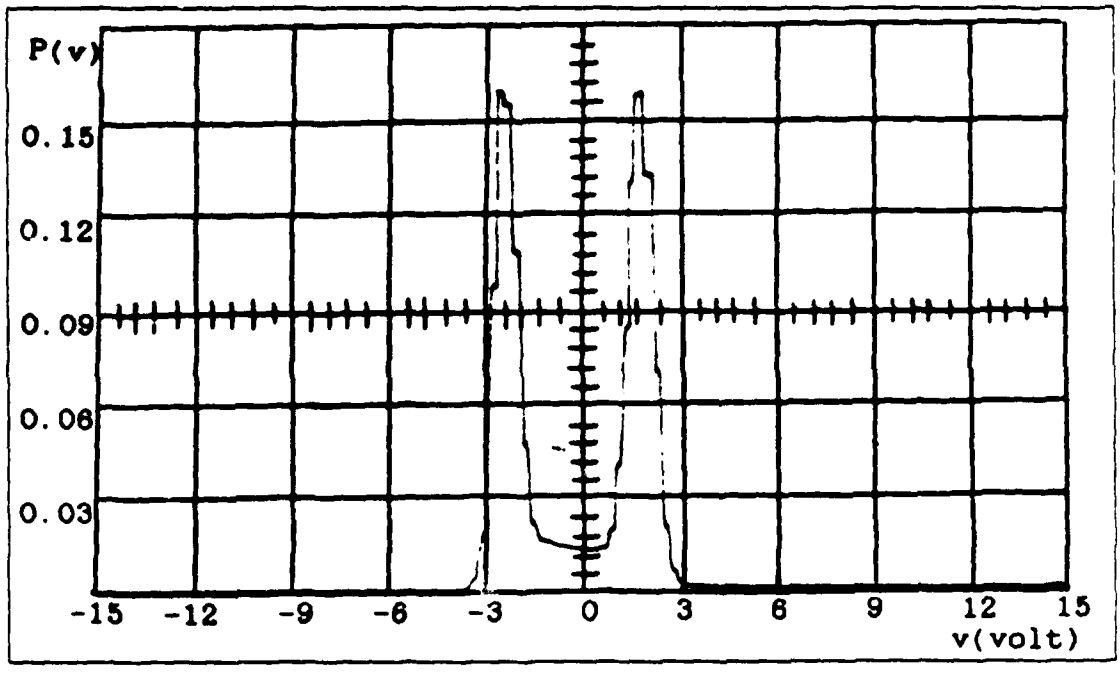


Figure 3.26 Probability Density Function for FSK Modulation Plus Noise (SNR = 10 dB).

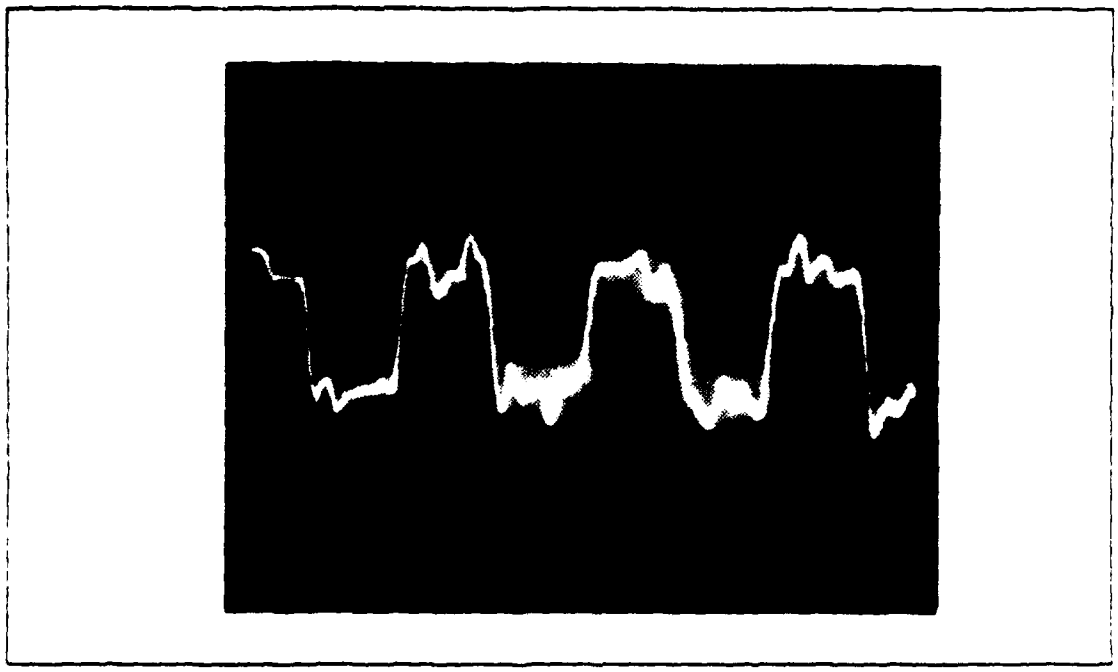


Figure 3.27 Output of the PLL for FSK Modulation Plus Noise (SNR = 8 dB).

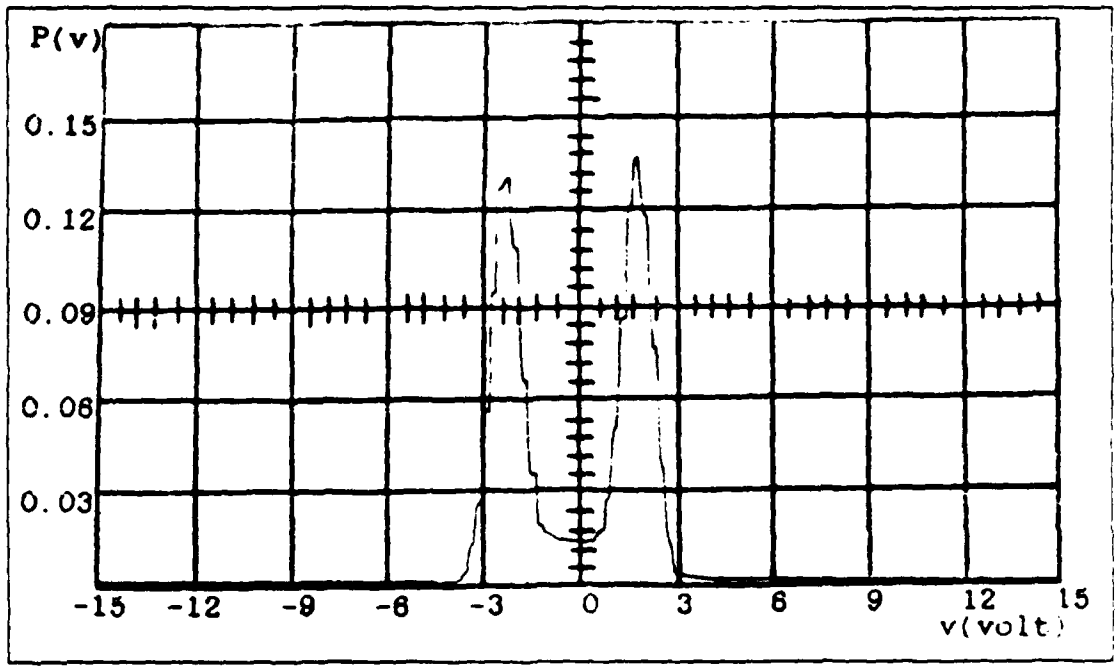


Figure 3.28 Probability Density Function for FSK Modulation Plus Noise (SNR = 8 dB).

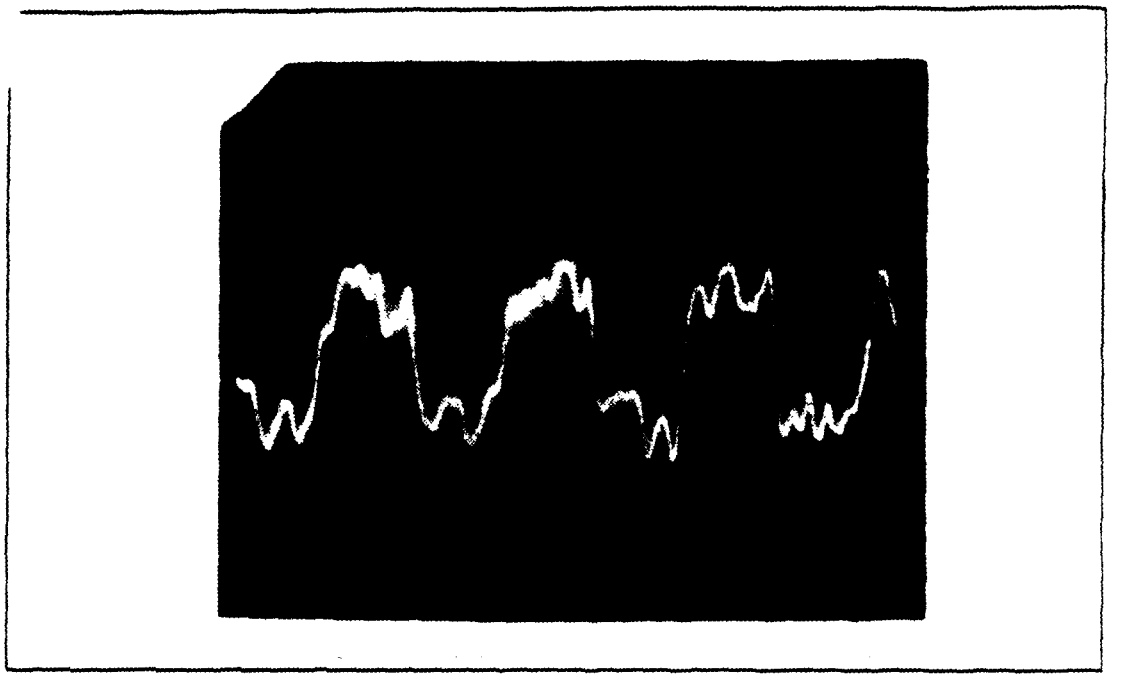


Figure 3.29 Output of the PLL for FSK Modulation Plus Noise (SNR = 6 dB).

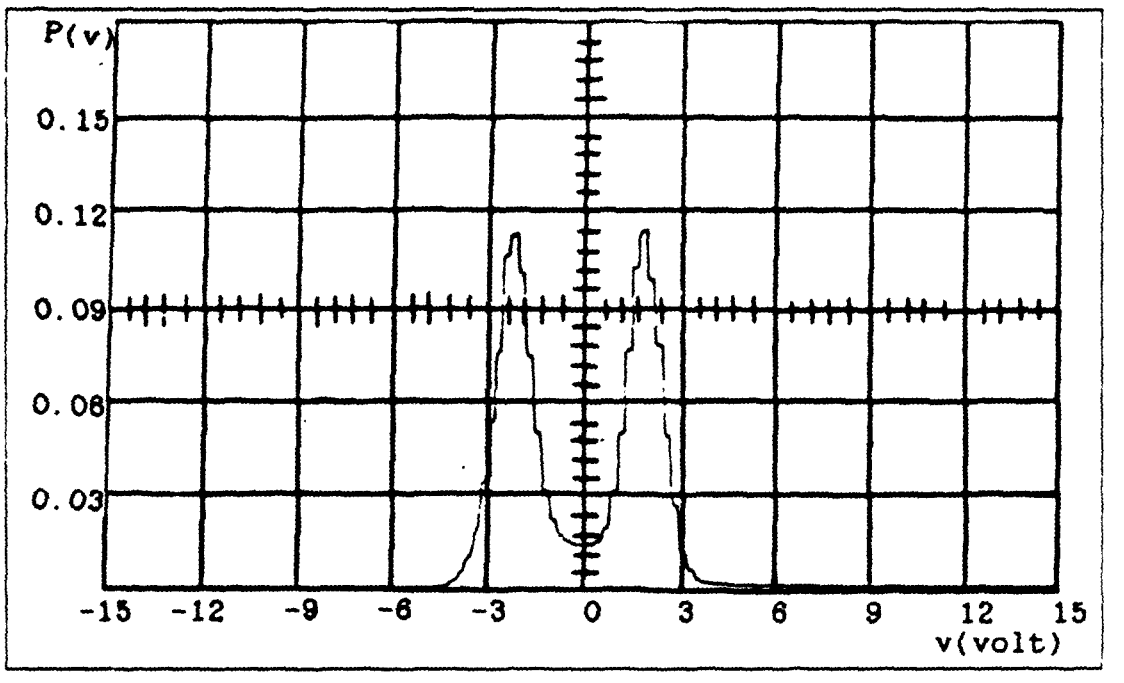


Figure 3.30 Probability Density Function for FSK Modulation Plus Noise (SNR = 6 dB).

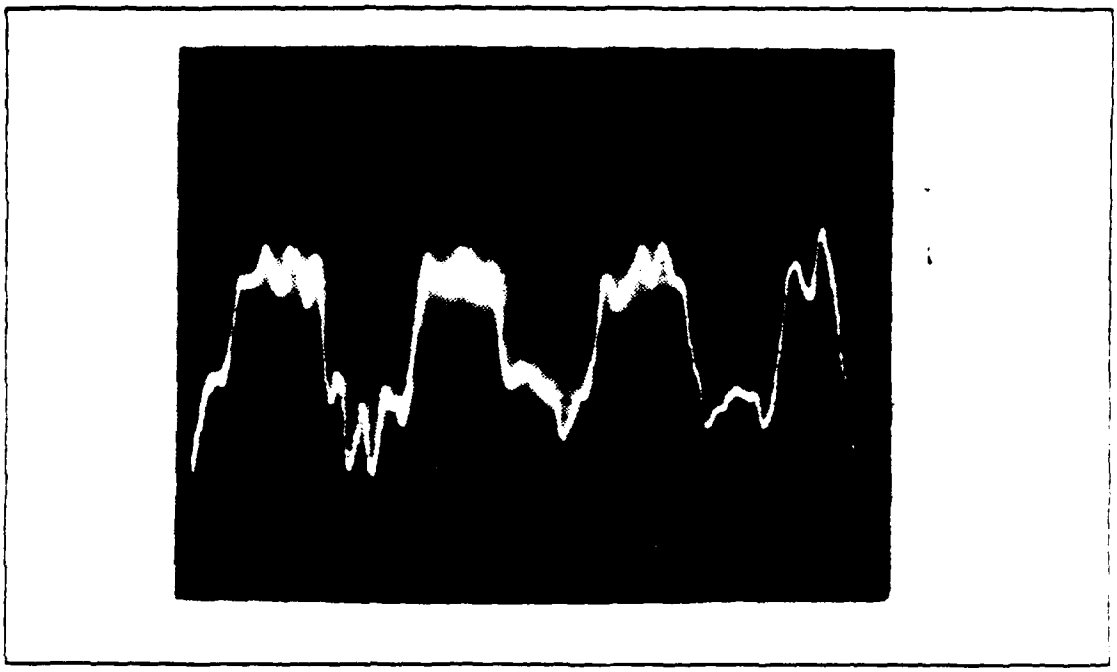


Figure 3.31 Output of the PLL for FSK Modulation Plus Noise (SNR = 4 dB).

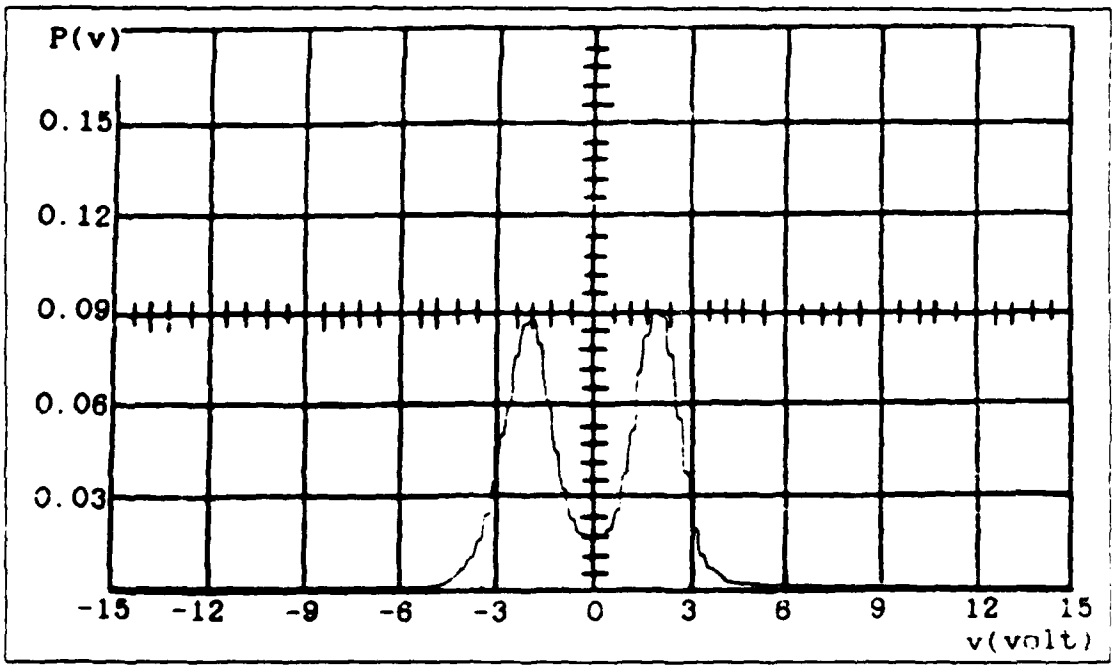


Figure 3.32 Probability Density Function for FSK Modulation Plus Noise (SNR = 4 dB).

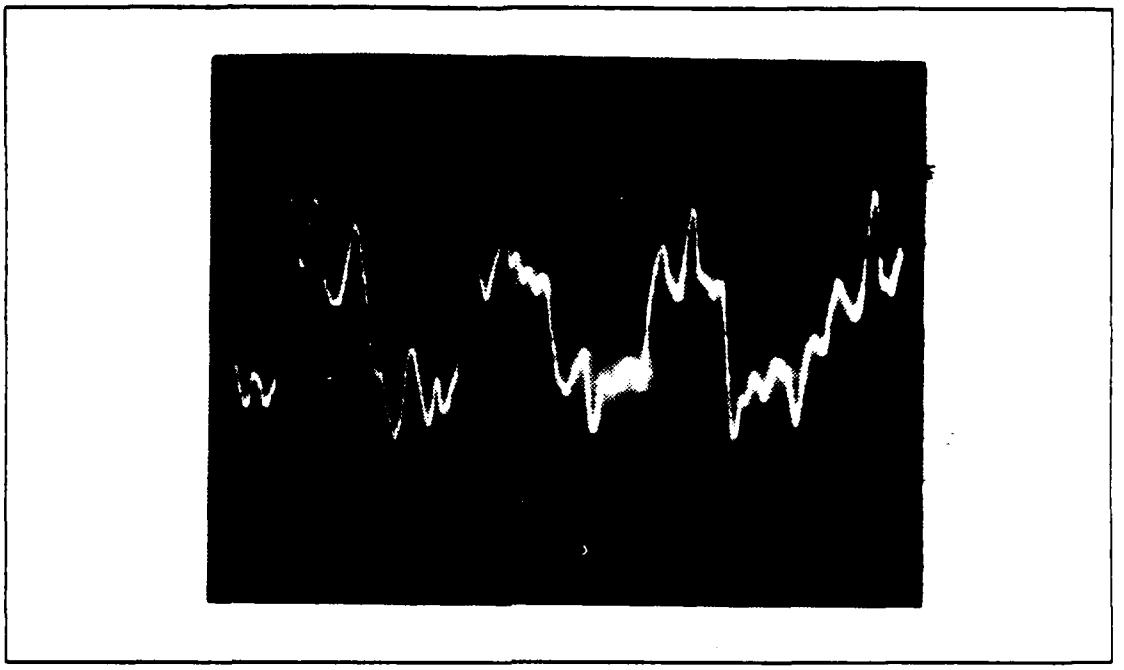


Figure 3.33 Output of the PLL for FSK Modulation Plus Noise (SNR = 2 dB).

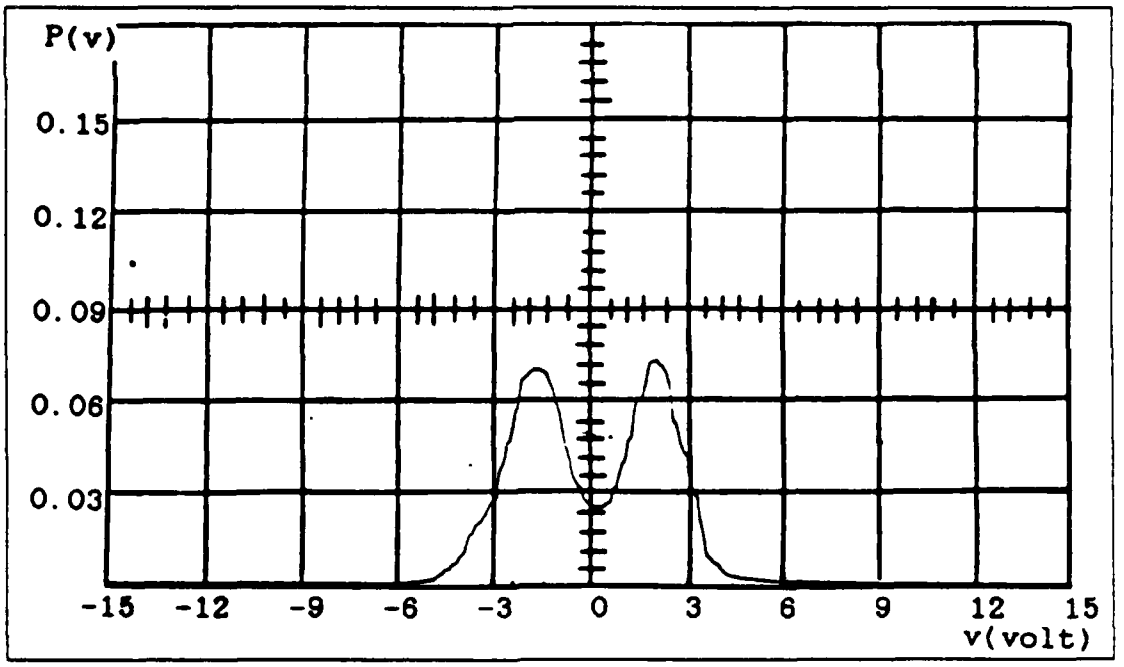


Figure 3.34 Probability Density Function for FSK Modulation Plus Noise (SNR = 2 dB).

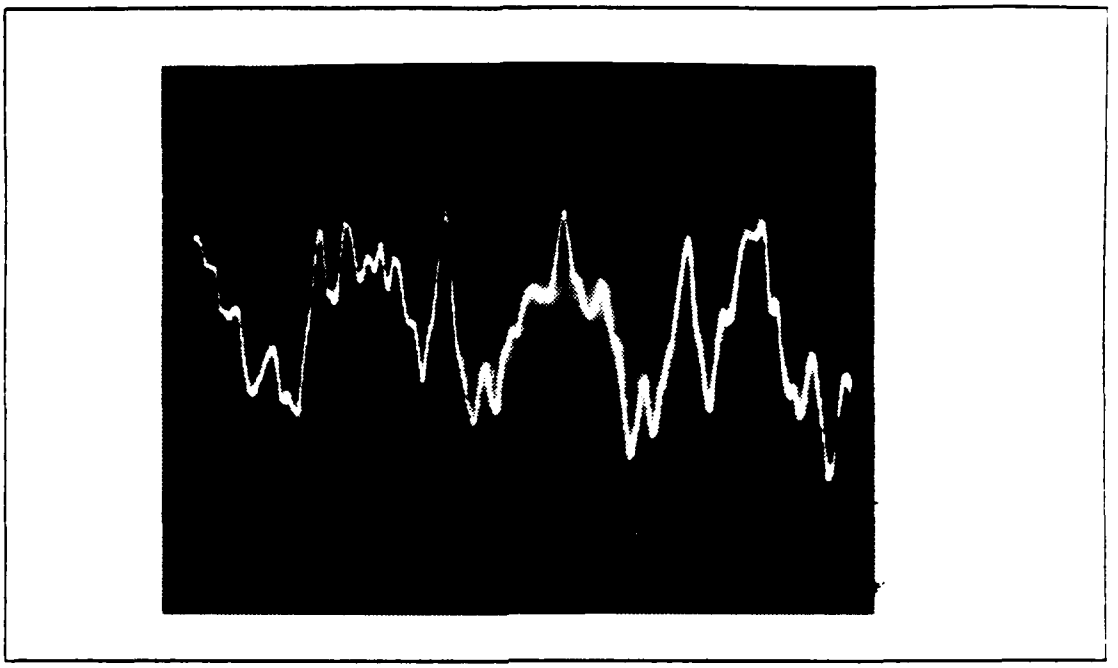


Figure 3.35 Output of the PLL for FSK Modulation Plus Noise (SNR = 0 dB).

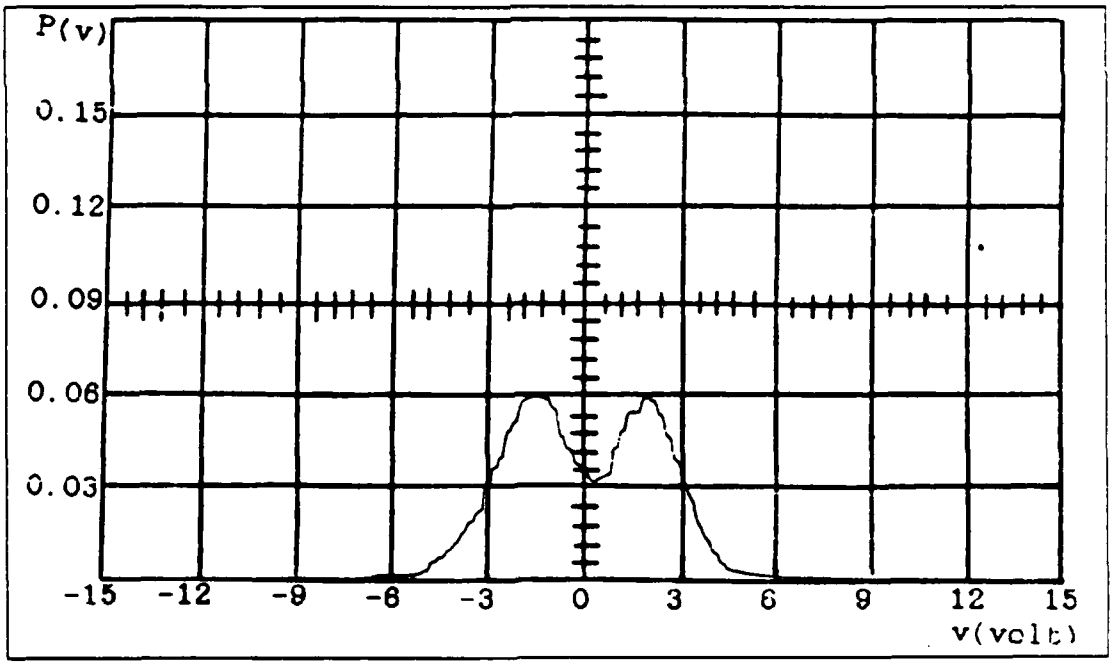


Figure 3.36 Probability Density Function for FSK Modulation Plus Noise (SNR = 0 dB).

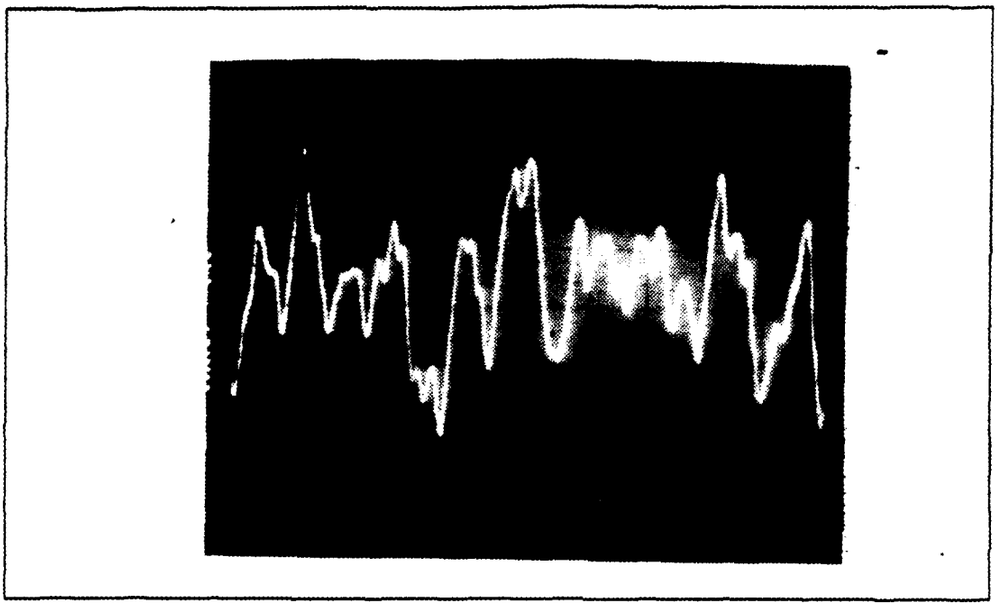


Figure 3.37 Output of the PLL for FSK Modulation Plus Noise (SNR = -5 dB).

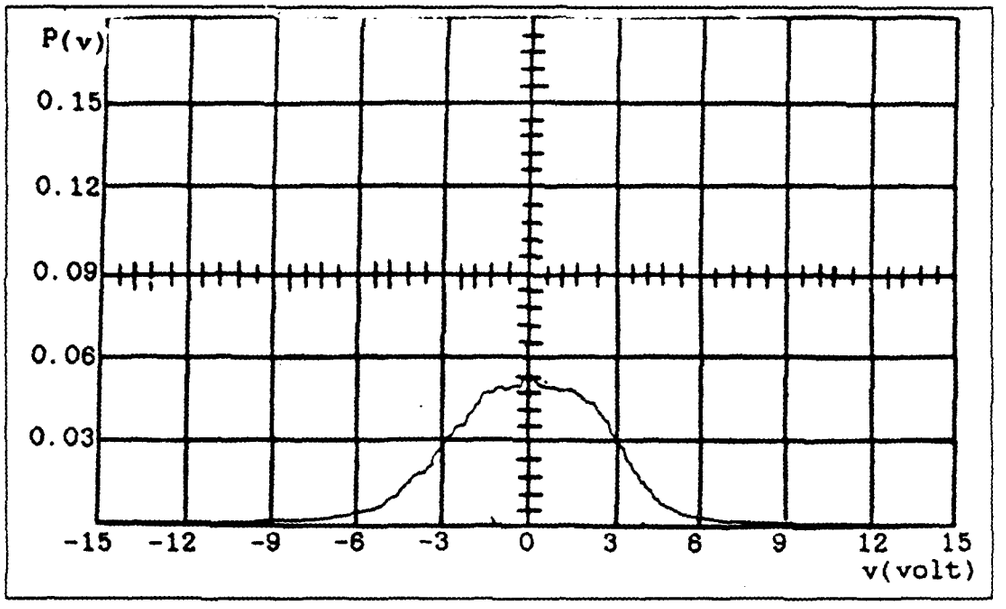


Figure 3.38 Probability Density Function for FSK Modulation Plus Noise (SNR = -5 dB).

2. **Output for FSK Modulation (Frequency Deviation = 3.7 kHz)**

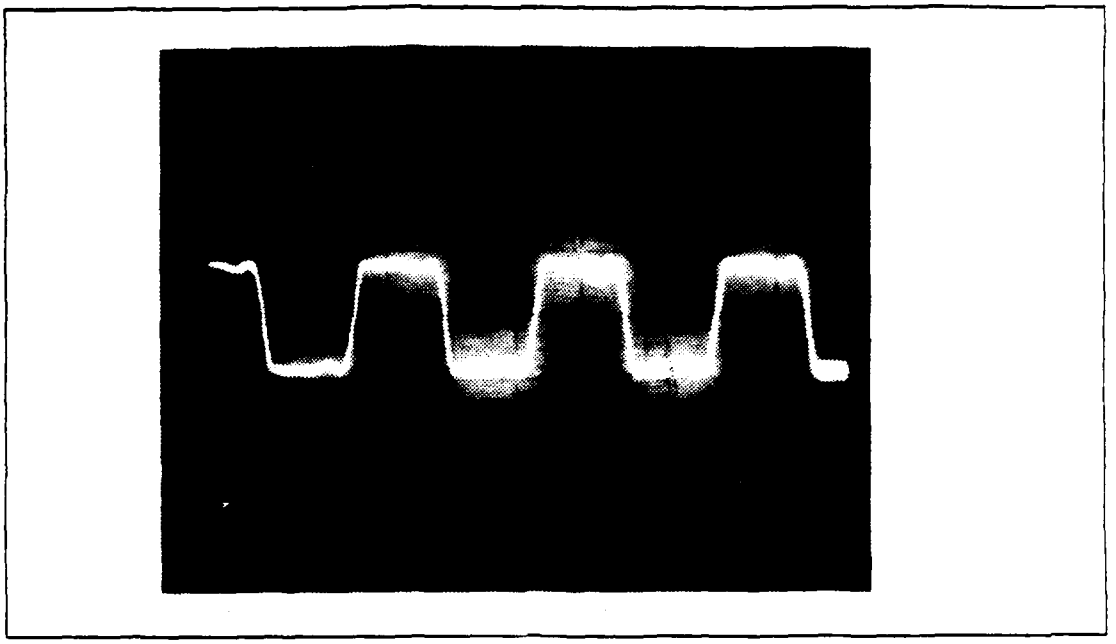


Figure 3.39 Output of the PLL for FSK Modulation (No Noise).

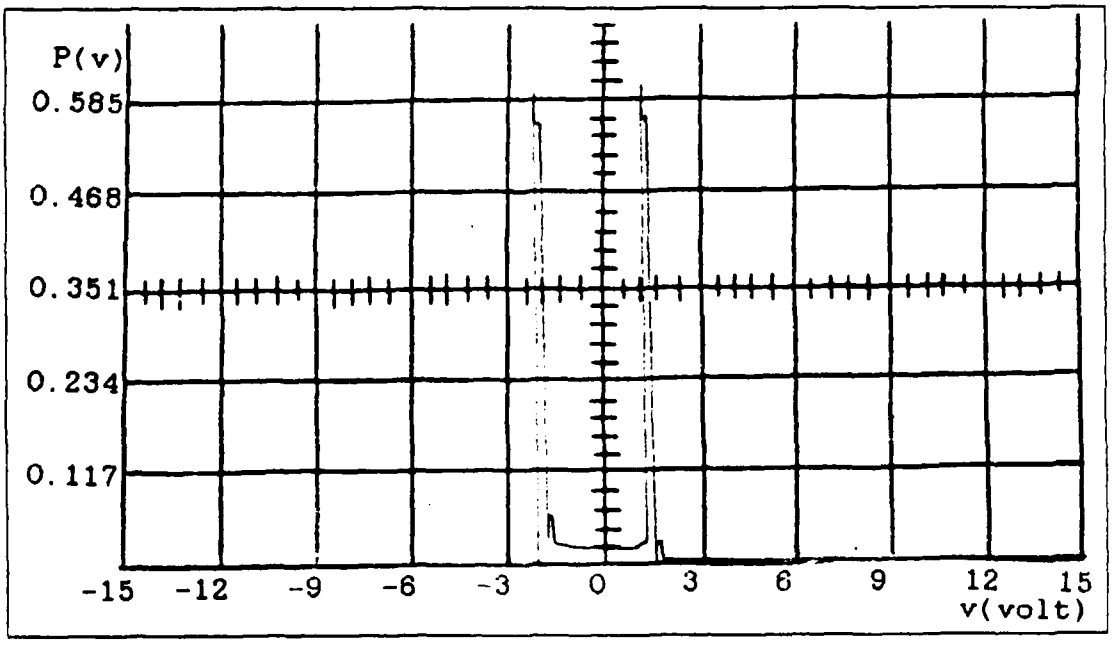


Figure 3.40 Probabiliyty Density Function for FSK Modulation (No Noise).

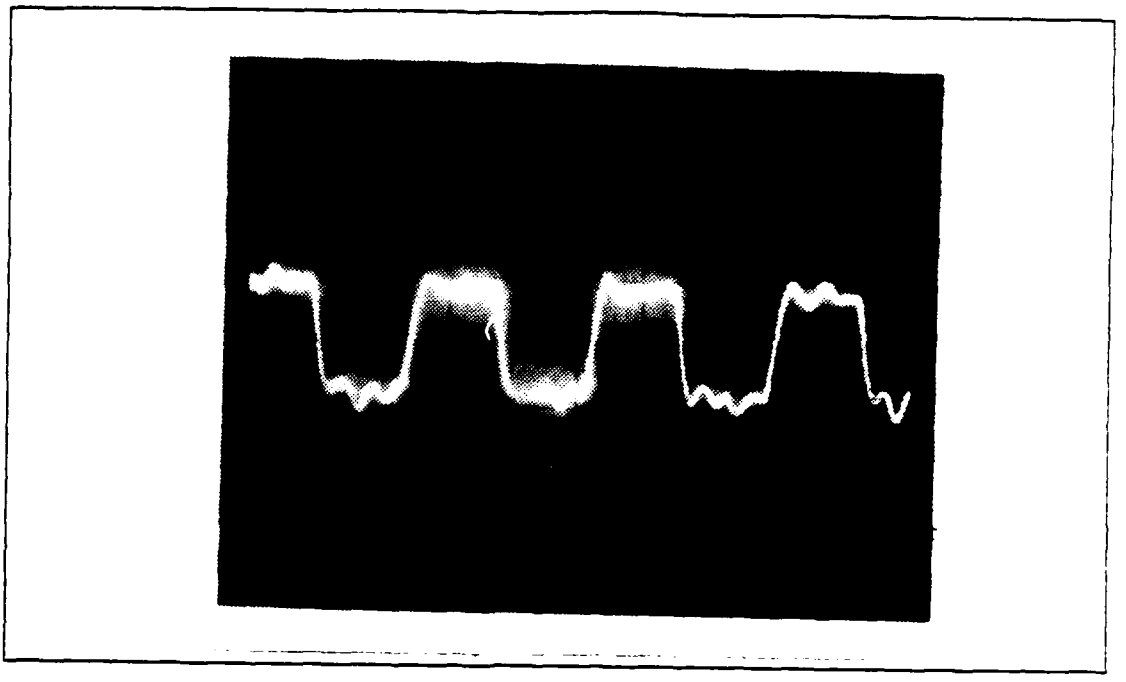


Figure 3.41 Output of the PLL for FSK Modulation Plus Noise (SNR = 20 dB).

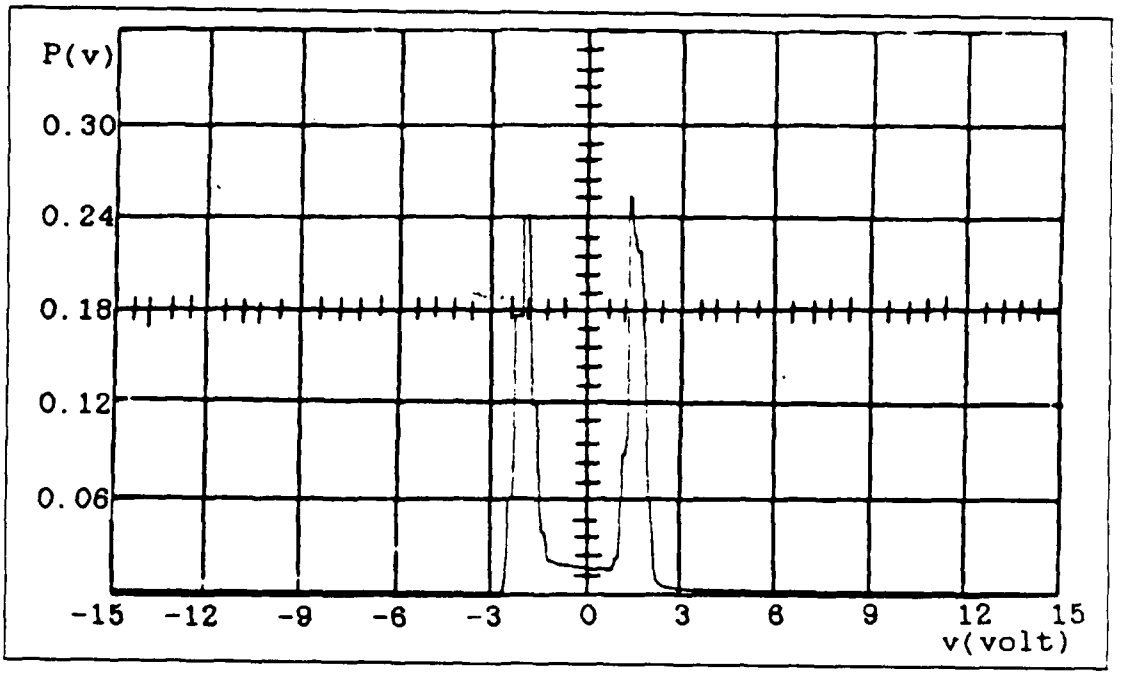


Figure 3.42 Probability Density Function for FSK Modulation Plus Noise (SNR = 20 dB).

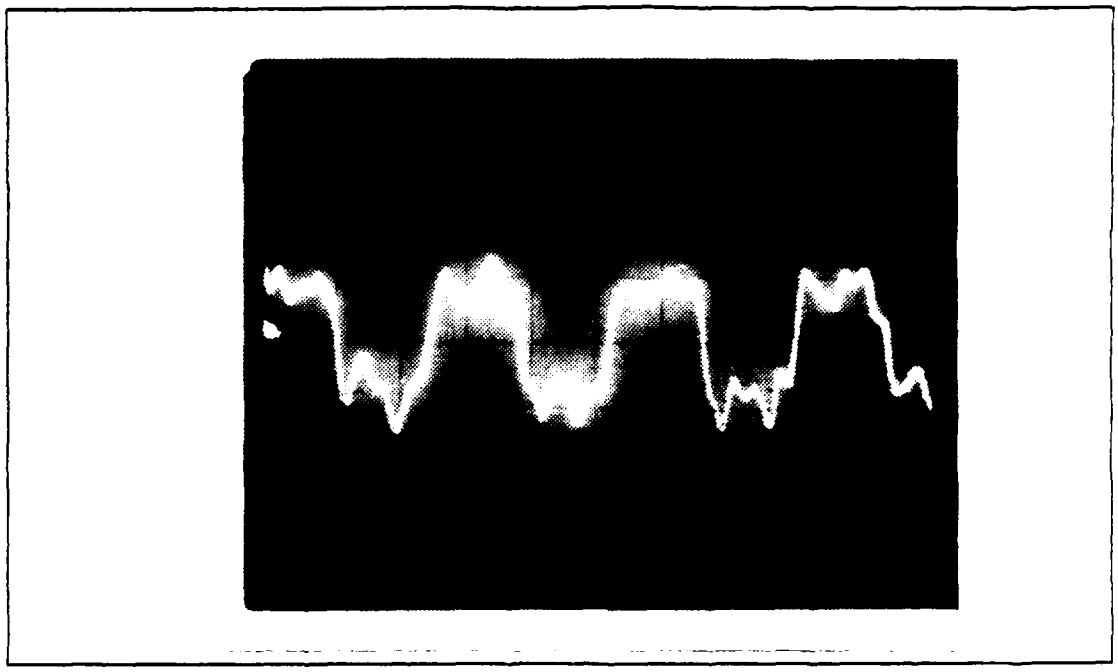


Figure 3.43 Output of the PLL for FSK Modulation Plus Noise (SNR = 10 dB).

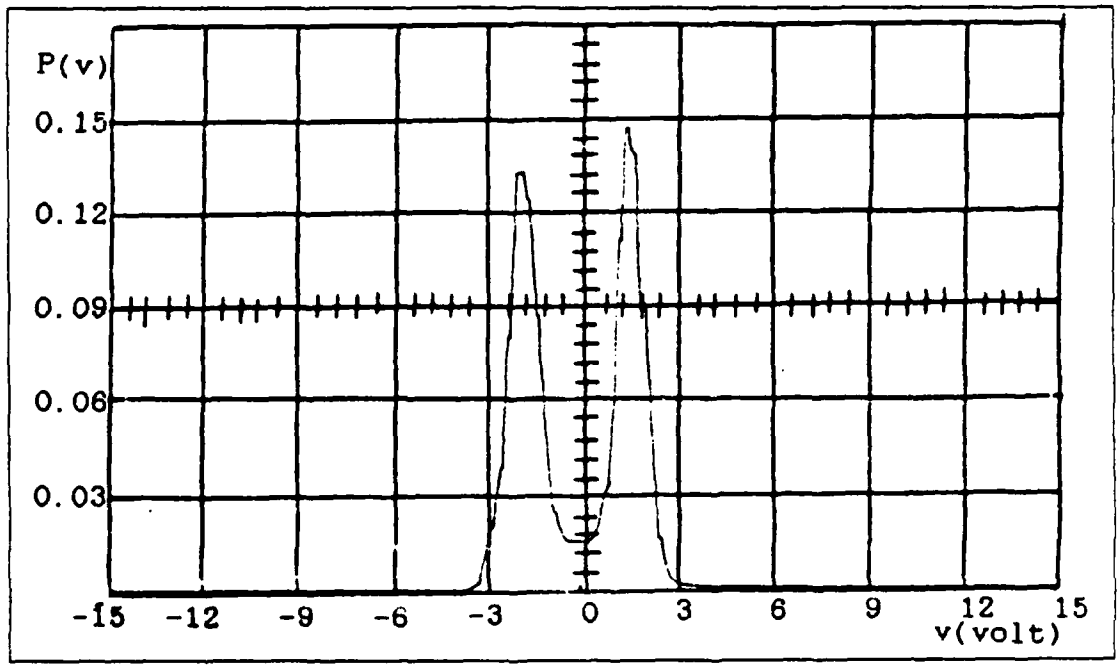


Figure 3.44 Probability Density Function for FSK Modulation Plus Noise (SNR = 10 dB).

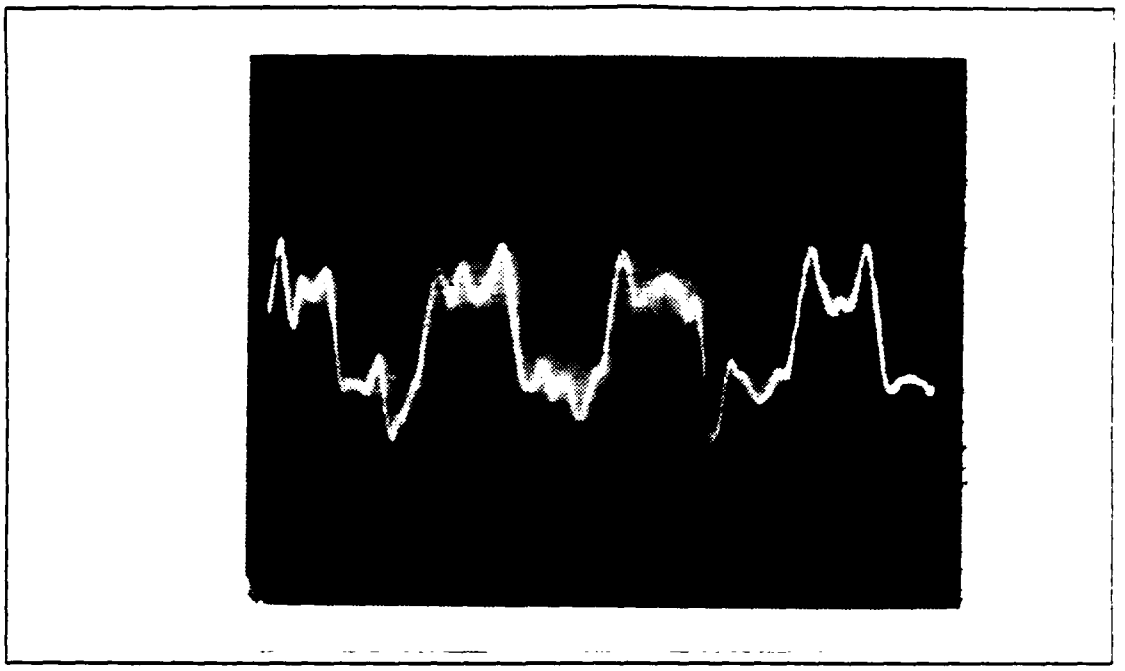


Figure 3.45 Output of the PLL for FSK Modulation Plus Noise (SNR = 8 dB).

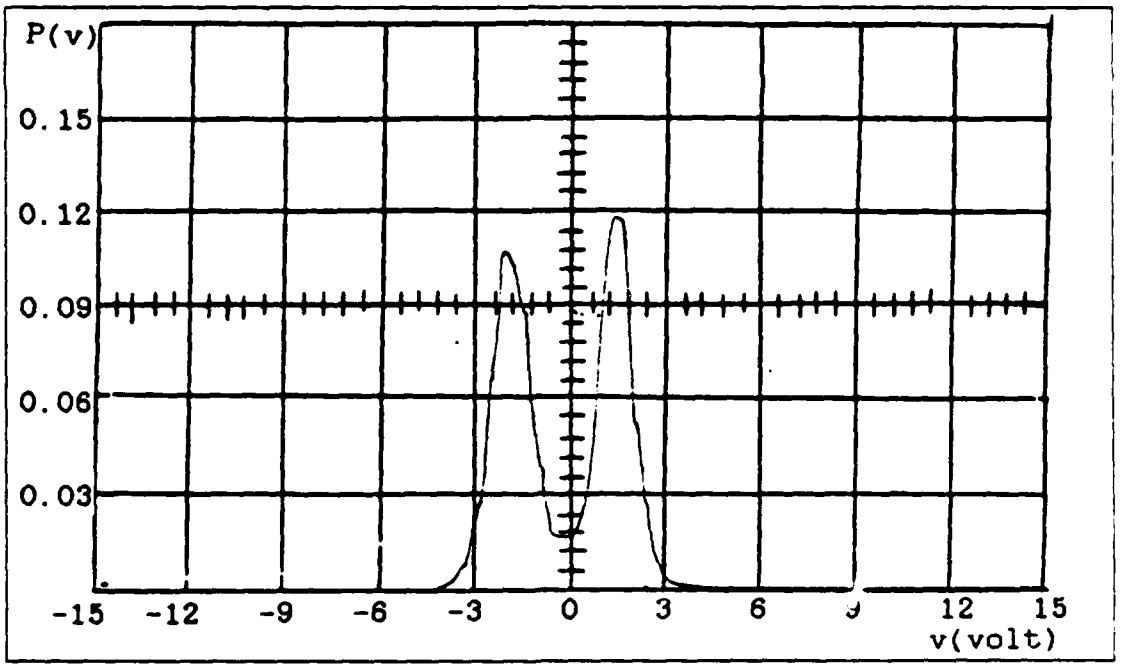


Figure 3.46 Probability Density Function for FSK Modulation Plus Noise (SNR = 8 dB).

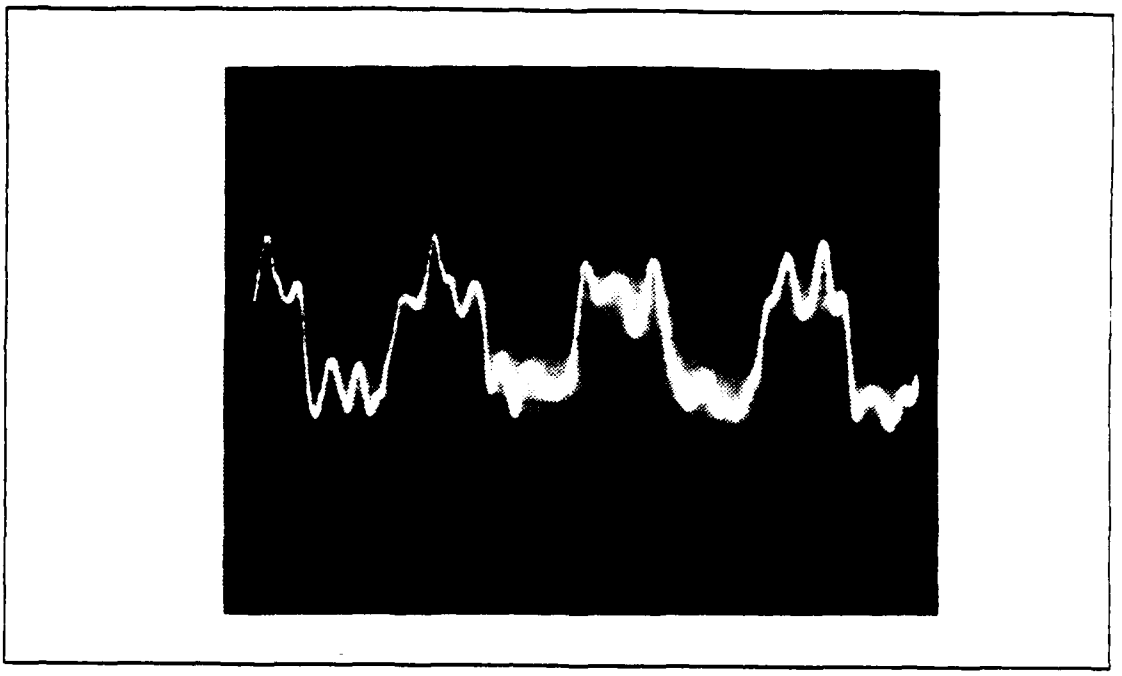


Figure 3.47 Output of the PLL for FSK Modulation Plus Noise (SNR = 6 dB).

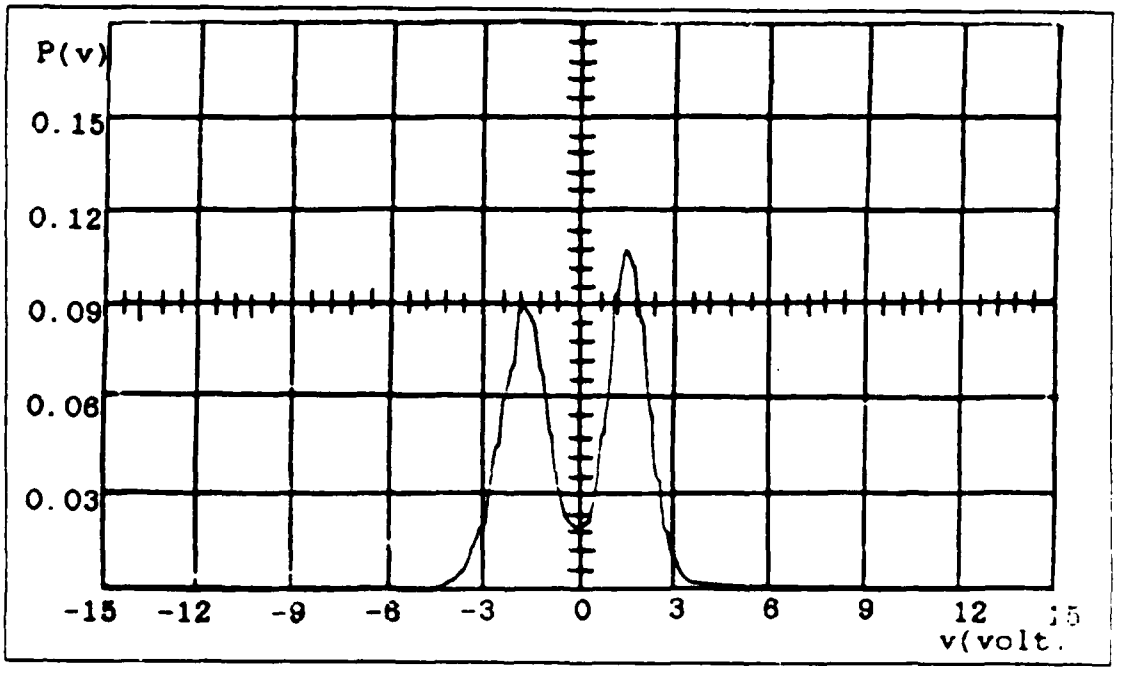


Figure 3.48 Probability Density Function for FSK Modulation Plus Noise (SNR = 6 dB).

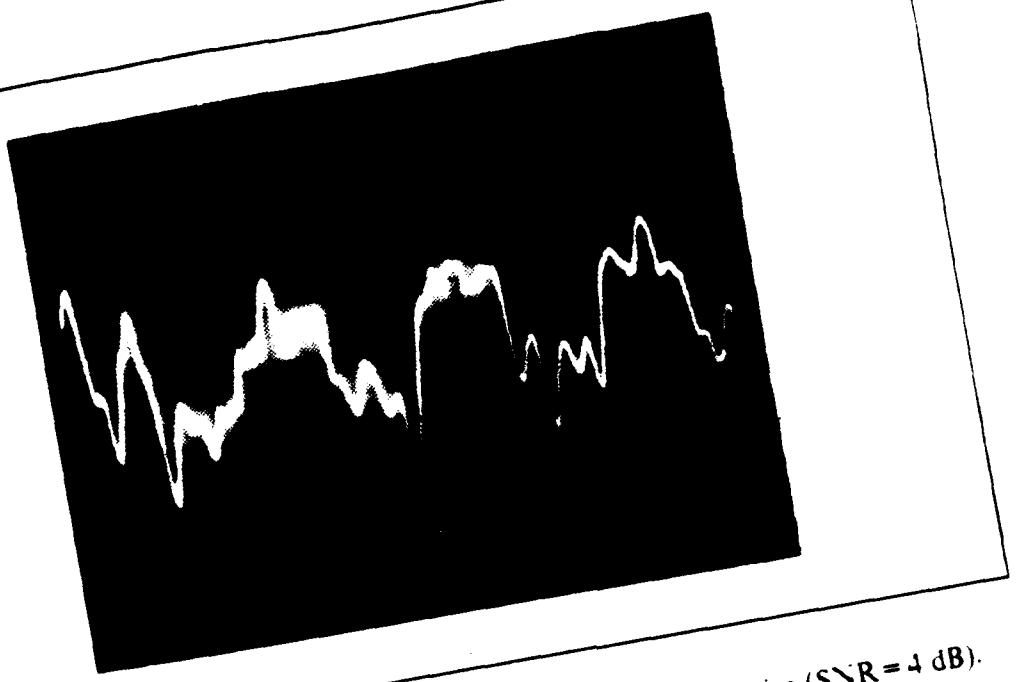


Figure 3.49 Output of the PLL for FSK Modulation Plus Noise (SNR = 4 dB).

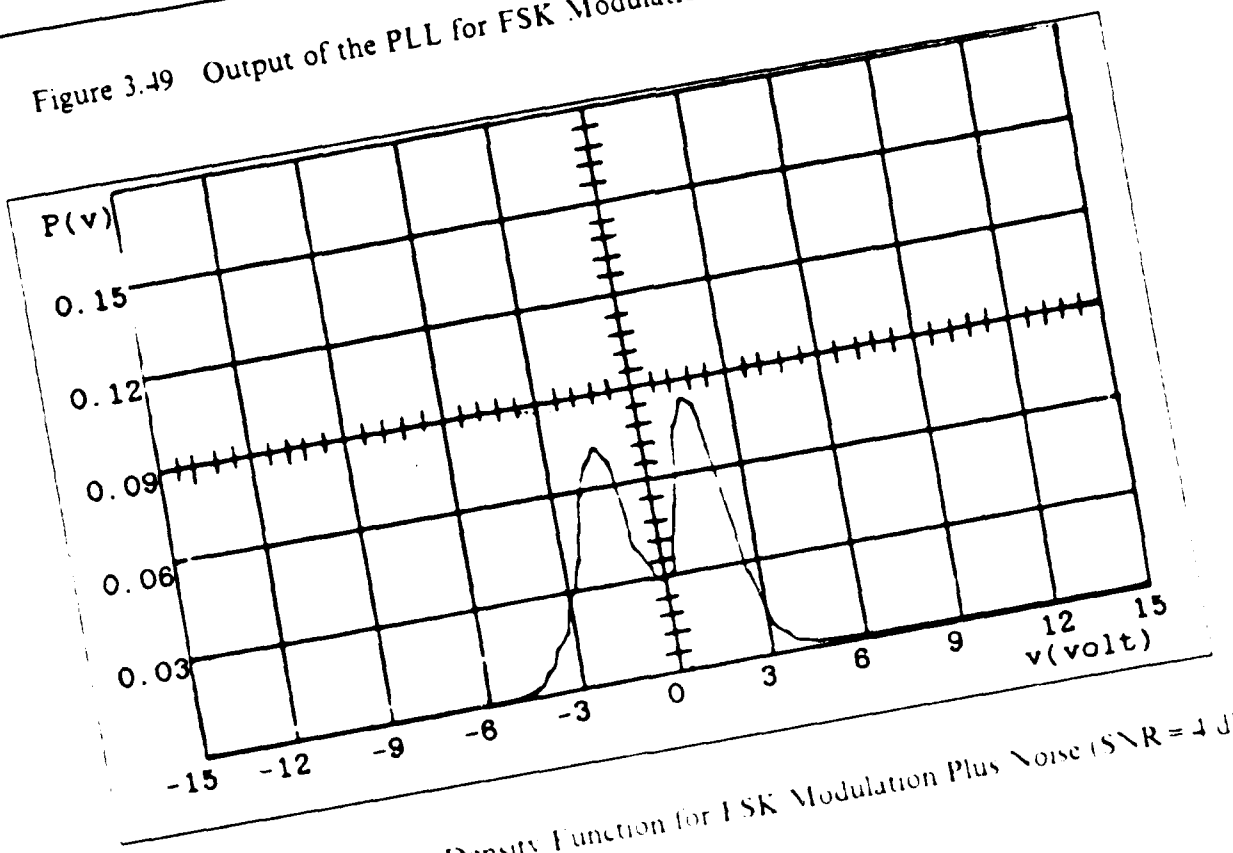


Figure 3.50 Probability Density Function for FSK Modulation Plus Noise (SNR = 4 dB).

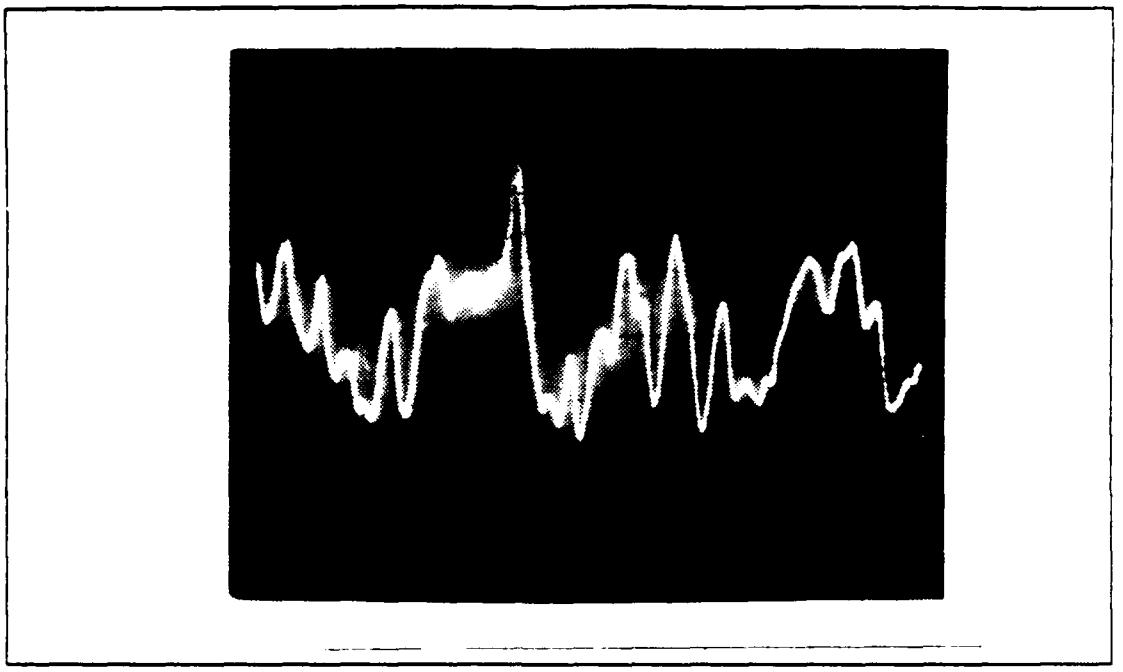


Figure 3.51 Output of the PLL for FSK Modulation Plus Noise (SNR = 2 dB).

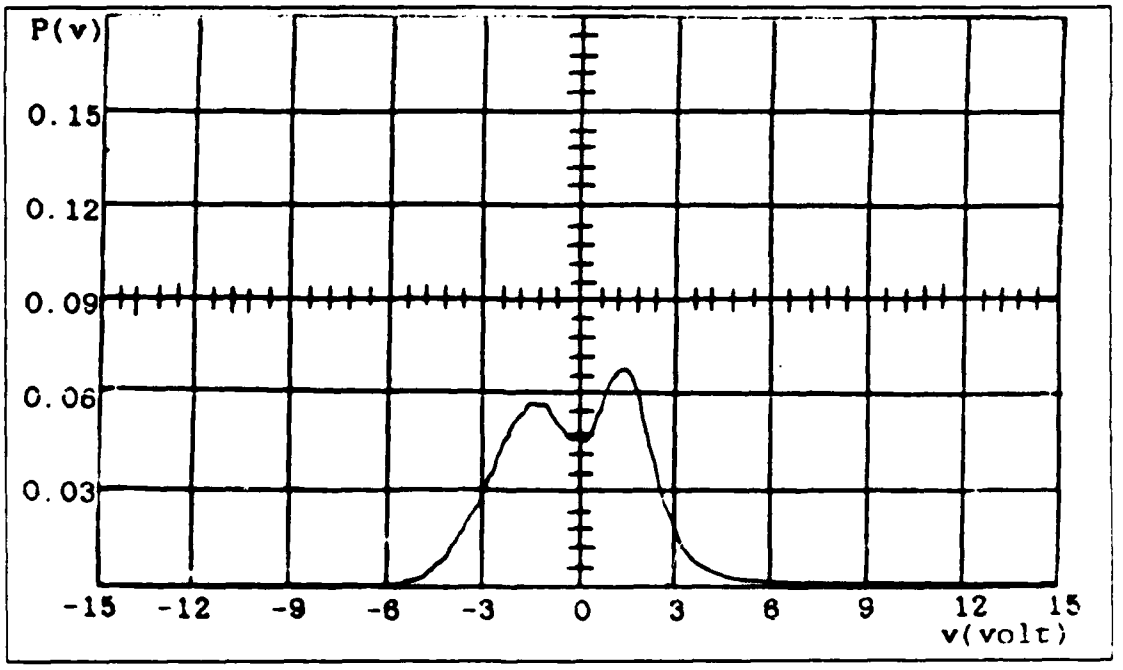


Figure 3.52 Probability Density Function for FSK Modulation Plus Noise (SNR = 2 dB).

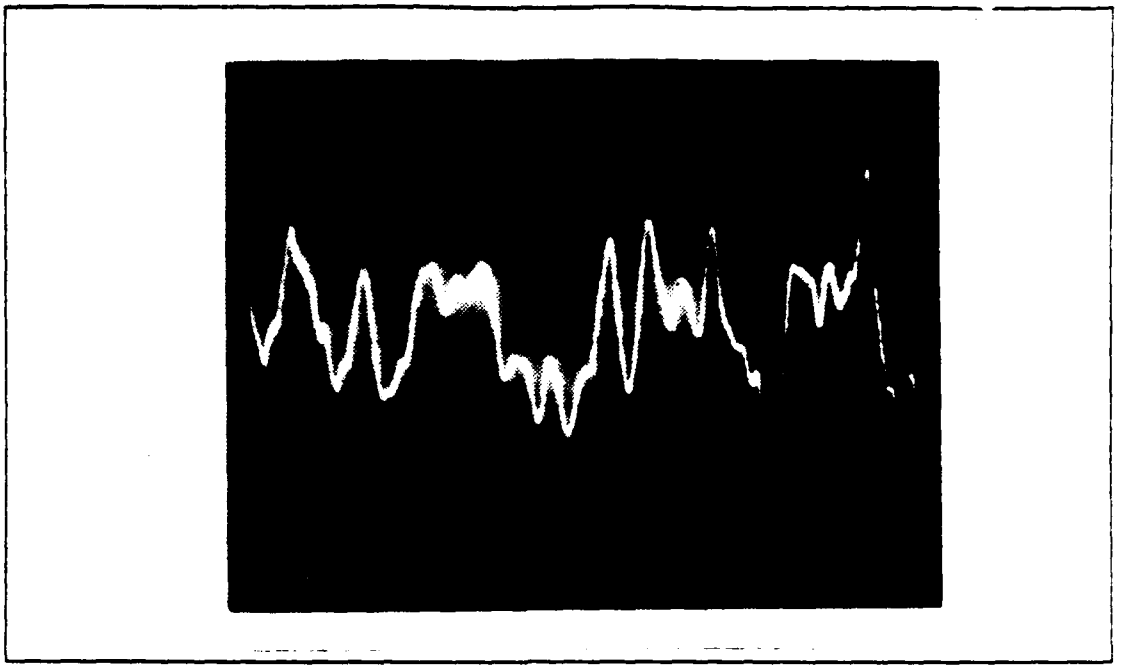


Figure 3.53 Output of the PLL for FSK Modulation Plus Noise (SNR = 0 dB).

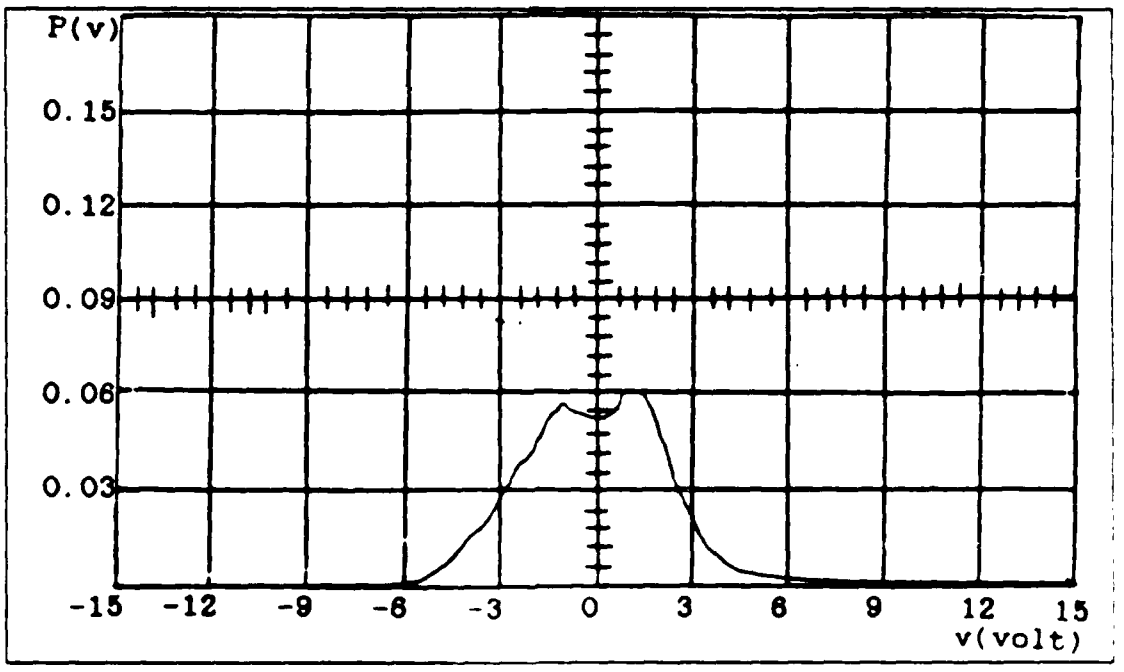


Figure 3.54 Probability Density Function for FSK Modulation Plus Noise (SNR = 0 dB).

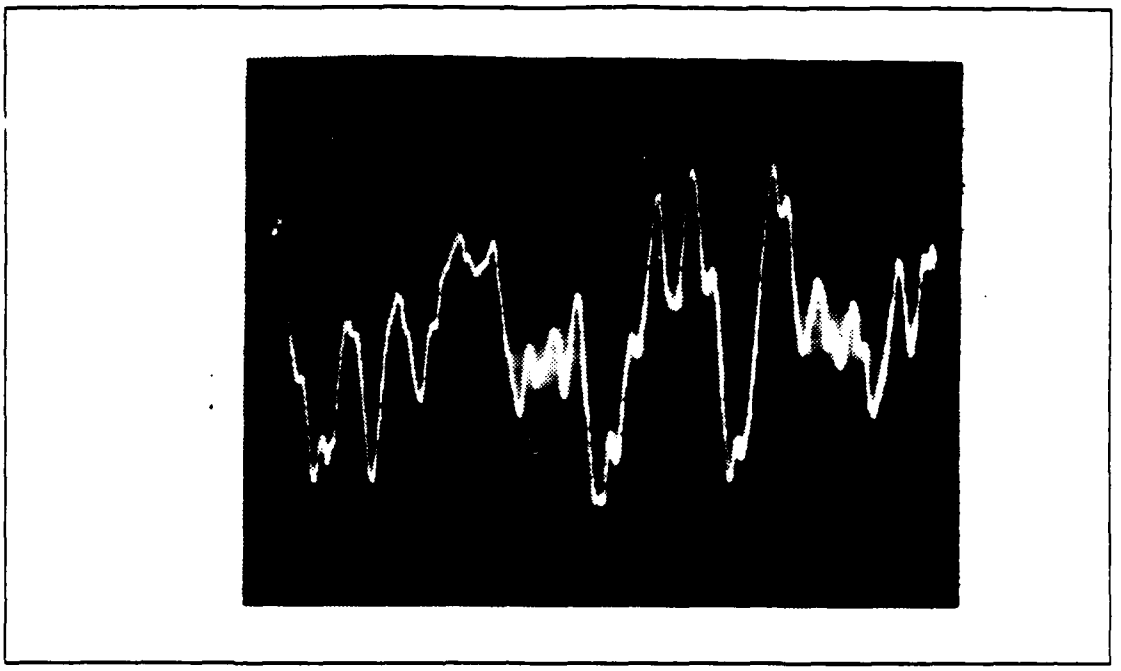


Figure 3.55 Output of the PLL for FSK Modulation Plus Noise (SNR = -5 dB).

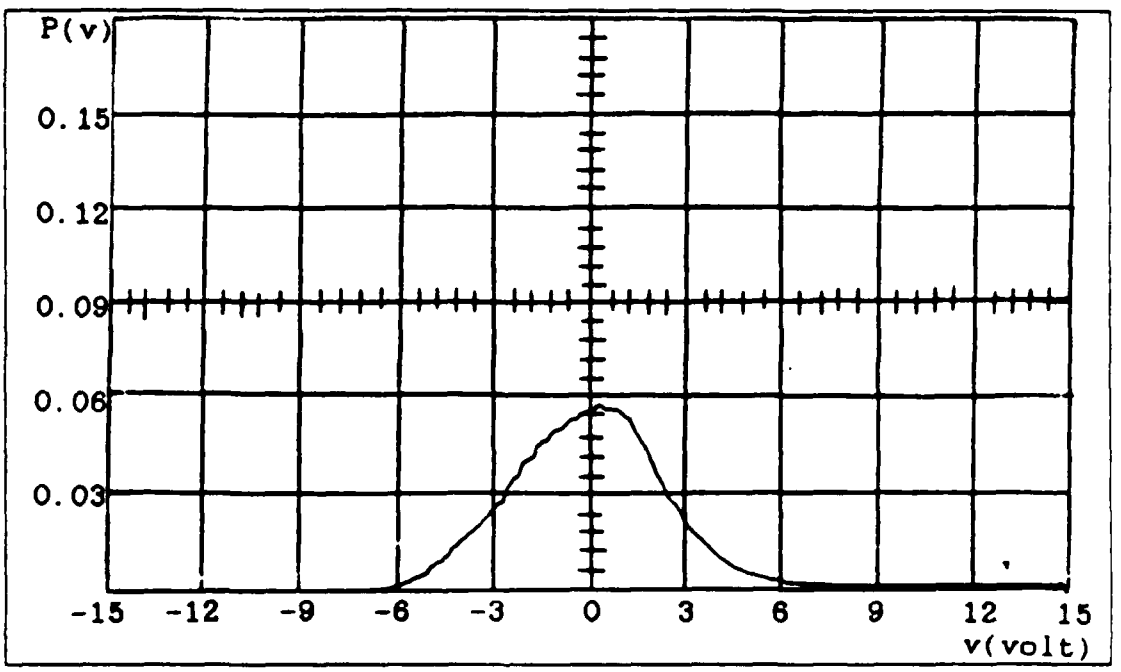


Figure 3.56 Probability Density Function for FSK Modulation Plus Noise (SNR = -5 dB).

C. FREQUENCY MODULATED CARRIER, TRIANGULAR WAVE MODULATING VOLTAGE

Measurements were made for a carrier frequency modulated by a triangular wave voltage to determine the PLL response to a changing frequency when noise is added. A signal generator provided a triangular wave of frequency 700 Hz. The triangular wave peak-to-peak voltage level was adjusted to obtain a 5 kHz peak-to-peak frequency deviation of the carrier. First measurement was made just for modulated signal (no-noise) at the input, and then noise was added to input signal according to the desired input signal-to-noise ratio. Fig. 3.57 shows the system set up for this measurement. Figs. 3.58 through 3.75 show the output voltage and its probability density function.

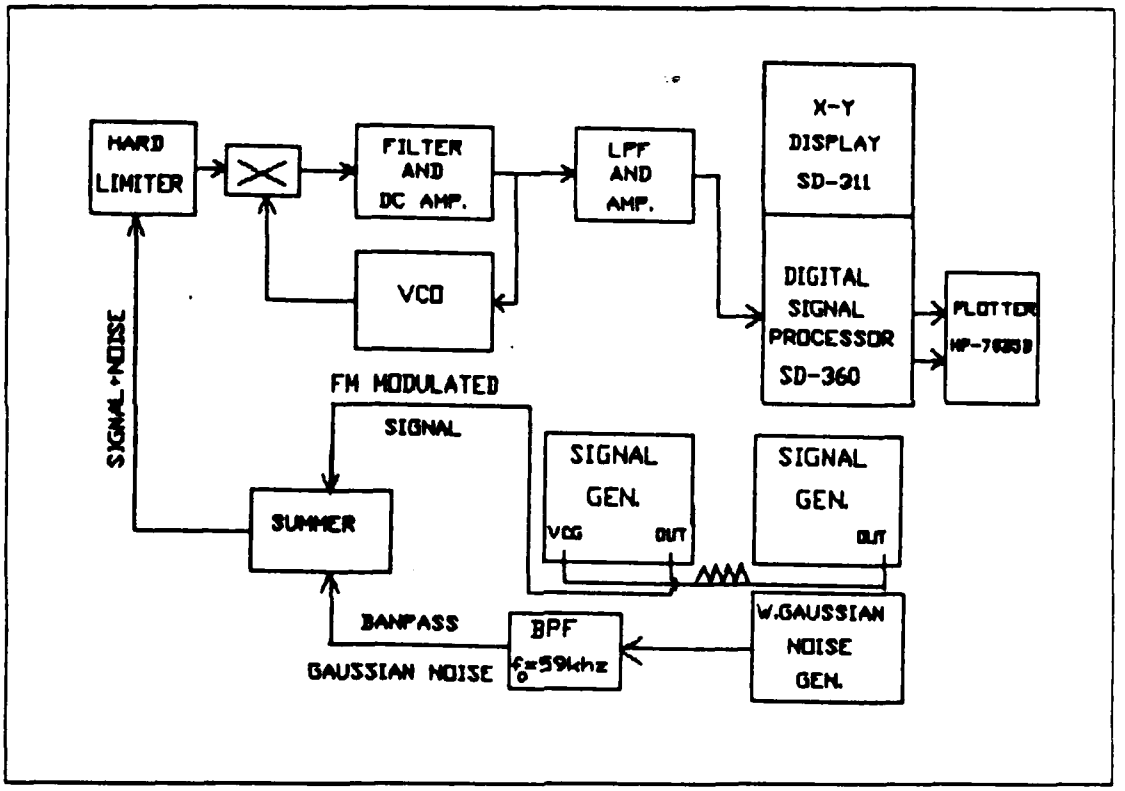


Figure 3.57 System for Frequency Modulated Carrier.

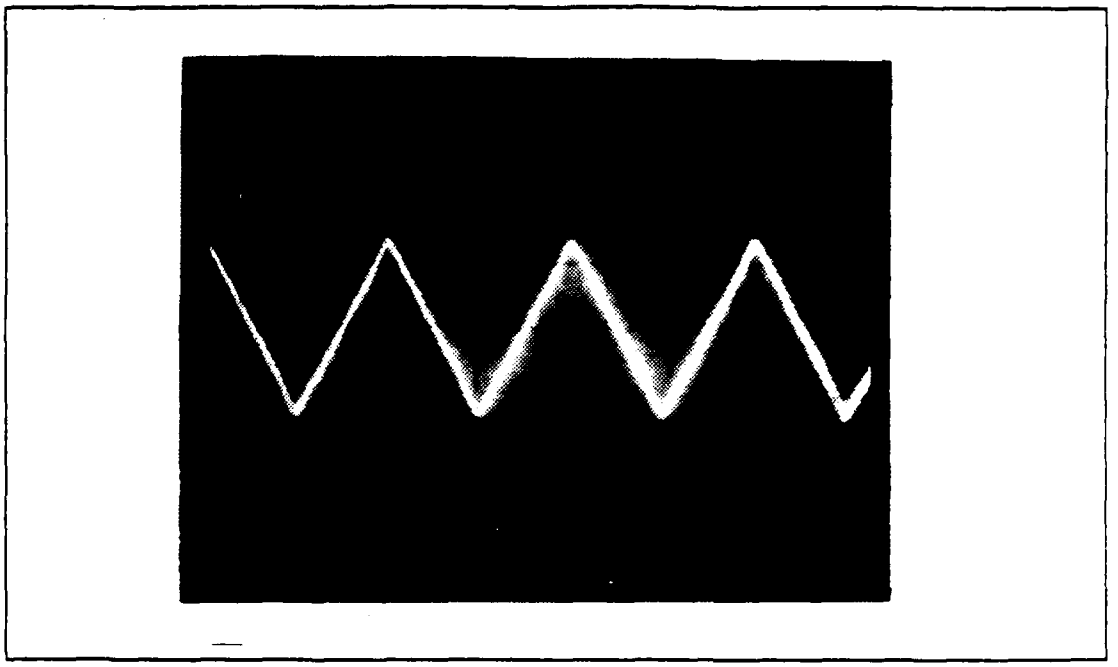


Figure 3.58 Output of the PLL for Frequency Modulated Carrier (No Noise).

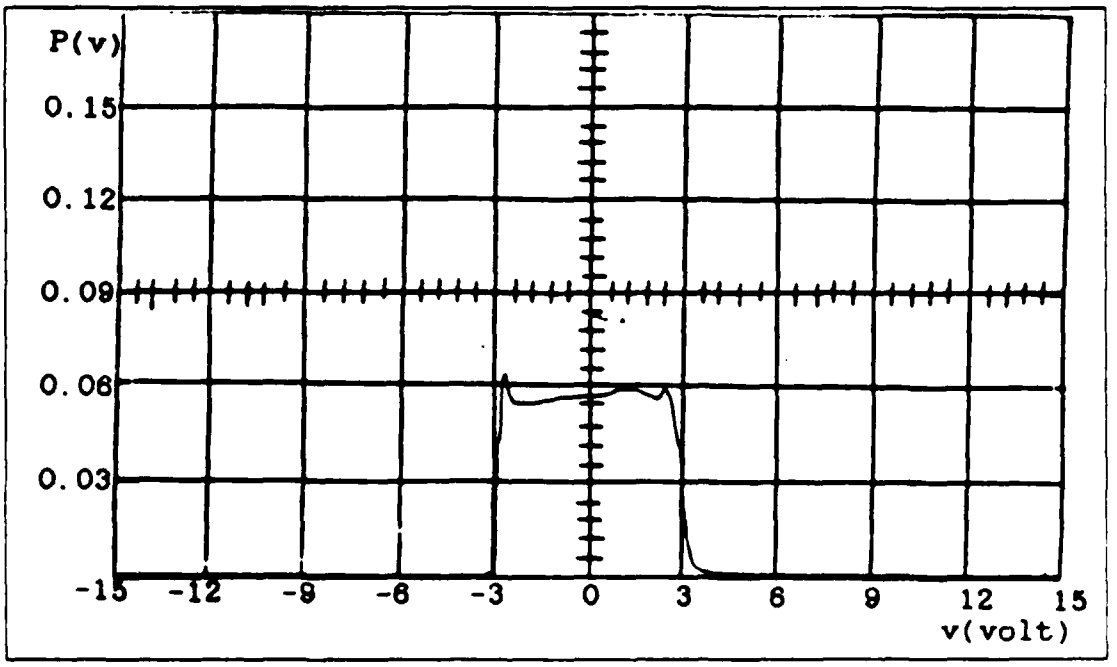


Figure 3.59 Probability Density Function for Frequency Modulated Carrier (No Noise).

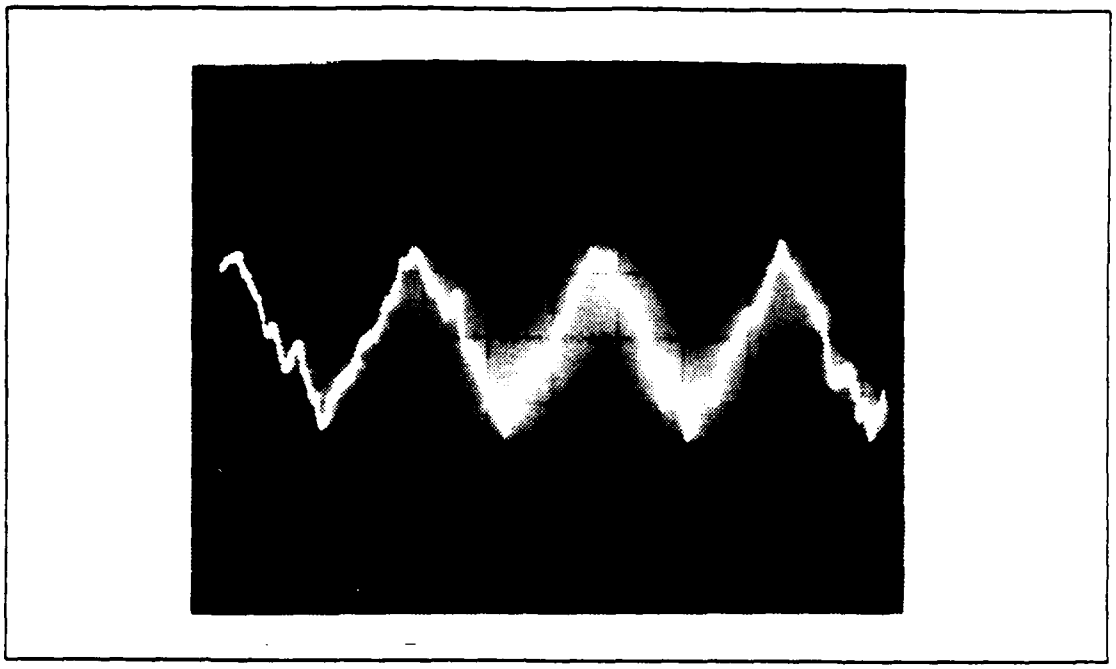


Figure 3.60 Output of the PLL for Frequency Modulated Carrier Plus Noise (SNR = 20 dB).

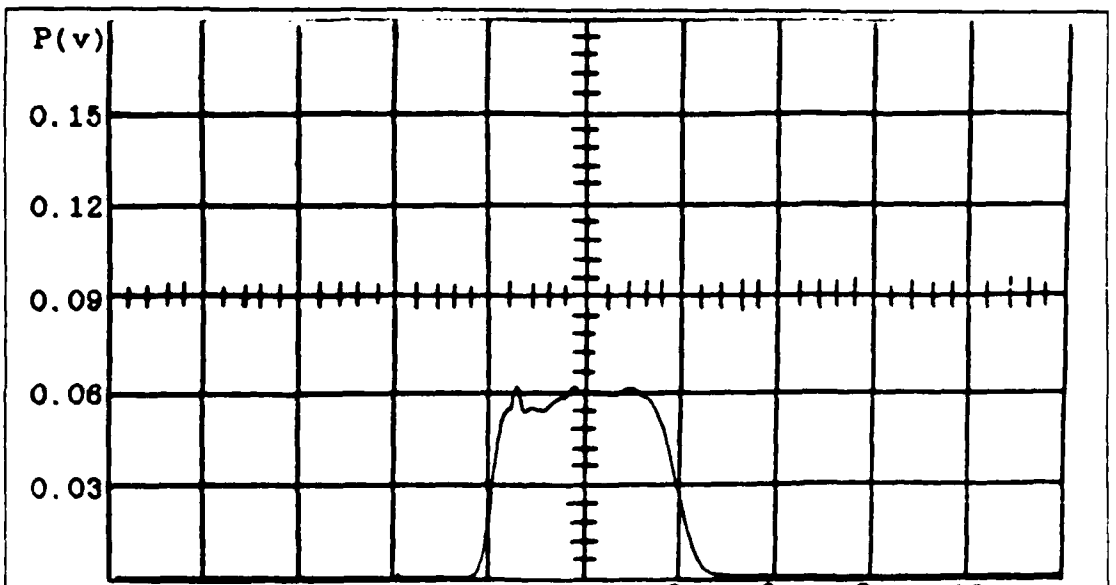


Figure 3.61 Probability Density Function for Frequency Modulated Carrier Plus Noise (SNR = 20 dB

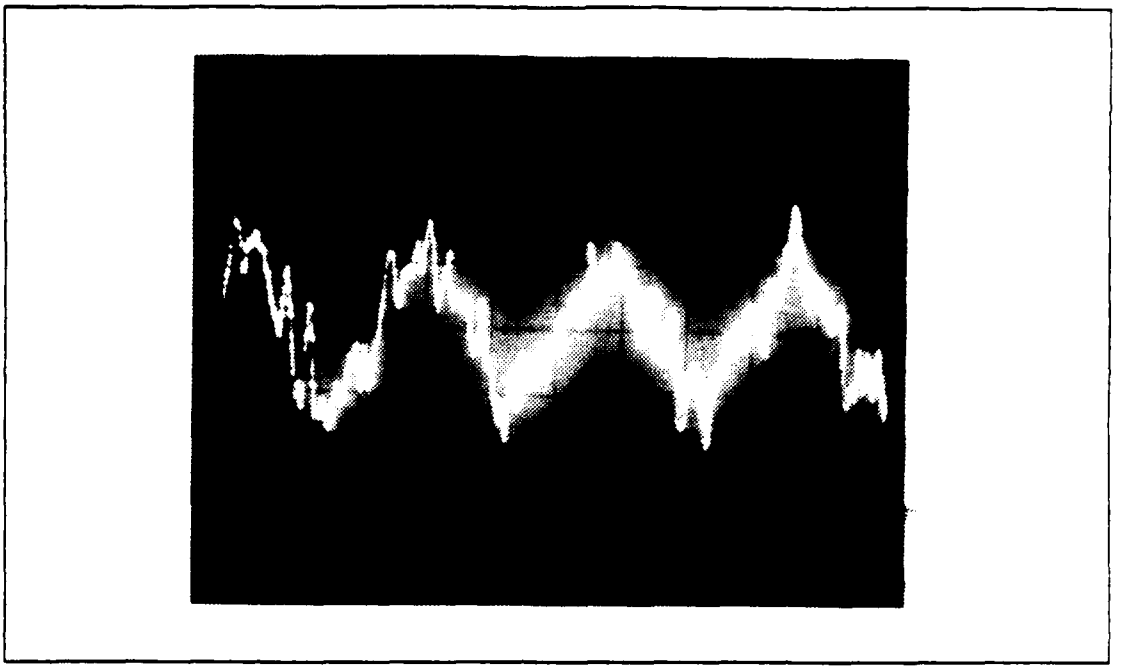


Figure 3.62 Output of the PLL for Frequency Modulated Carrier Plus Noise (SNR = 10 dB).

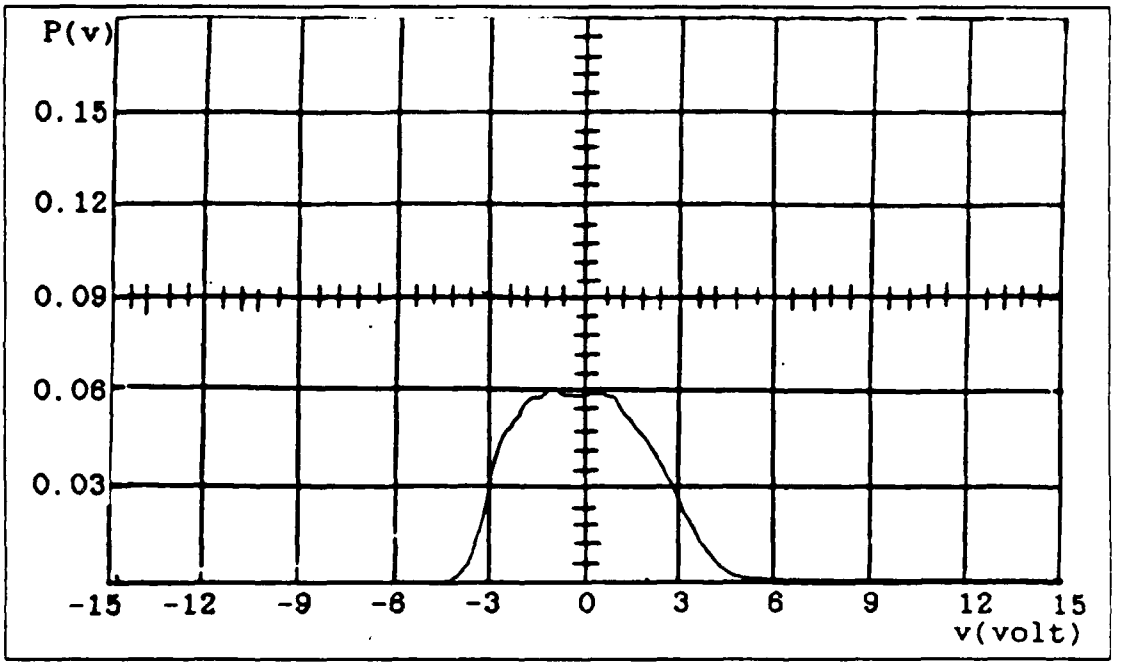


Figure 3.63 Probability Density Function for Frequency Modulated Carrier Plus Noise (SNR = 10 dB

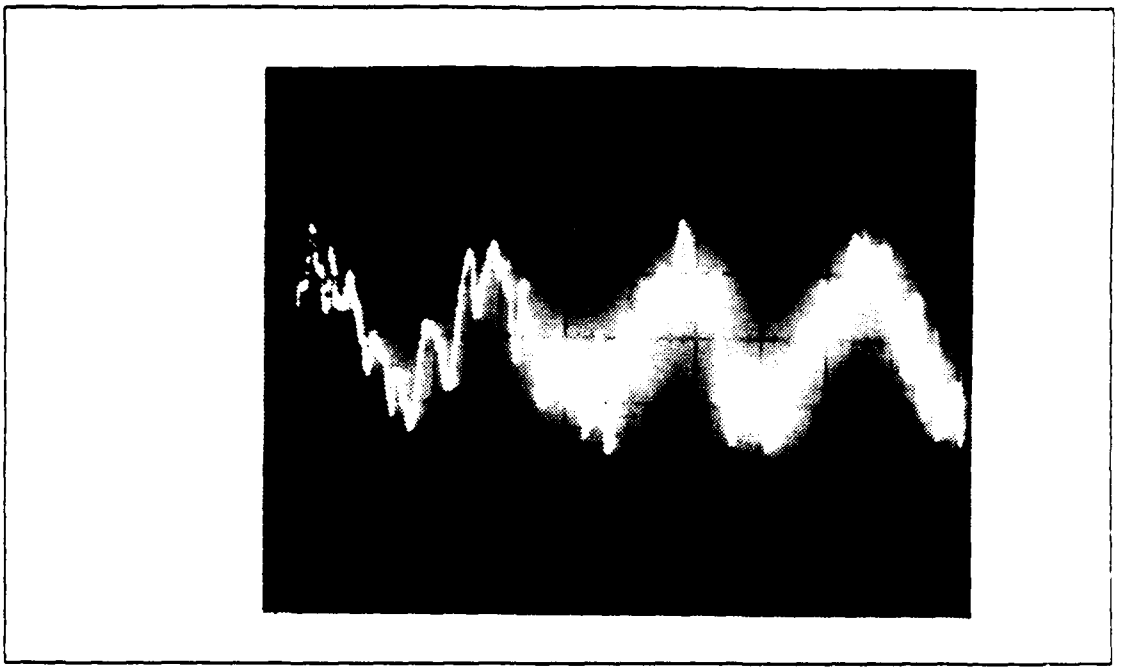


Figure 3.64 Output of the PLL for Frequency Modulated Carrier Plus Noise (SNR = 8 dB).

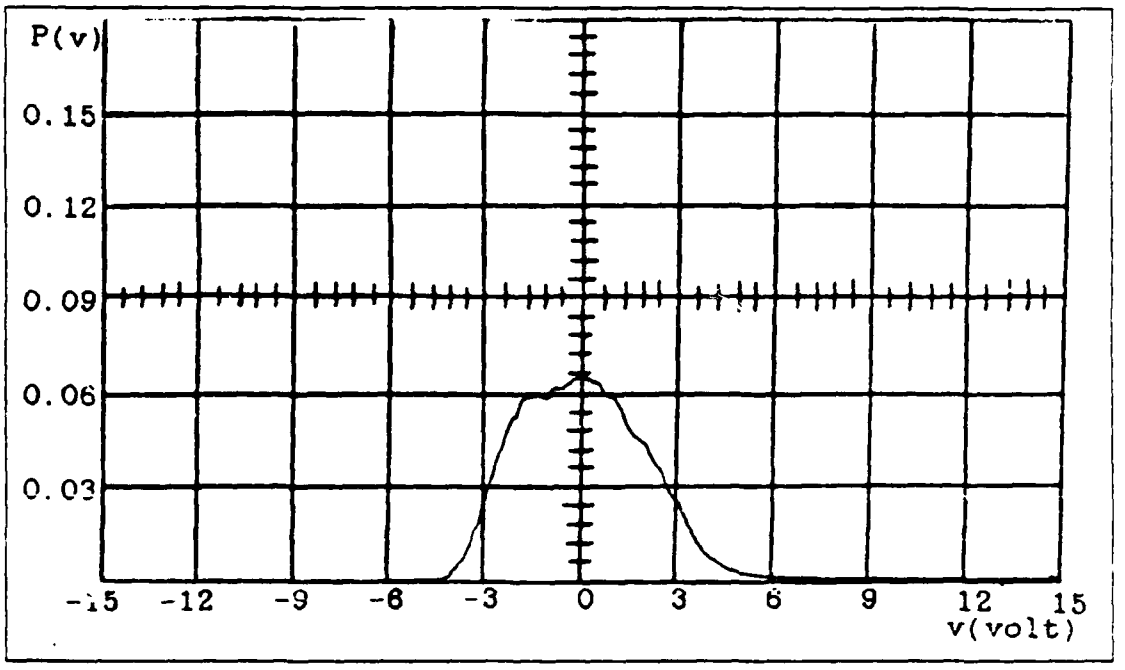


Figure 3.65 Probability Density Function for Frequency Modulated Carrier Plus Noise (SNR = 8 dB).

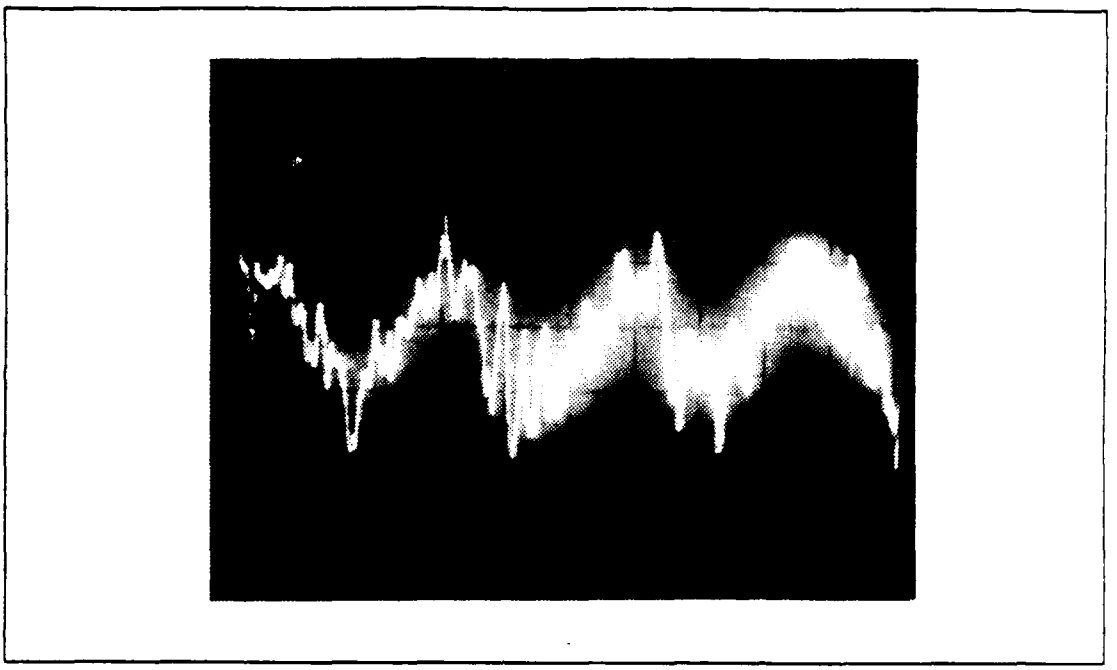


Figure 3.66 Output of the PLL for Frequency Modulated Carrier Plus Noise (SNR = 6 dB).

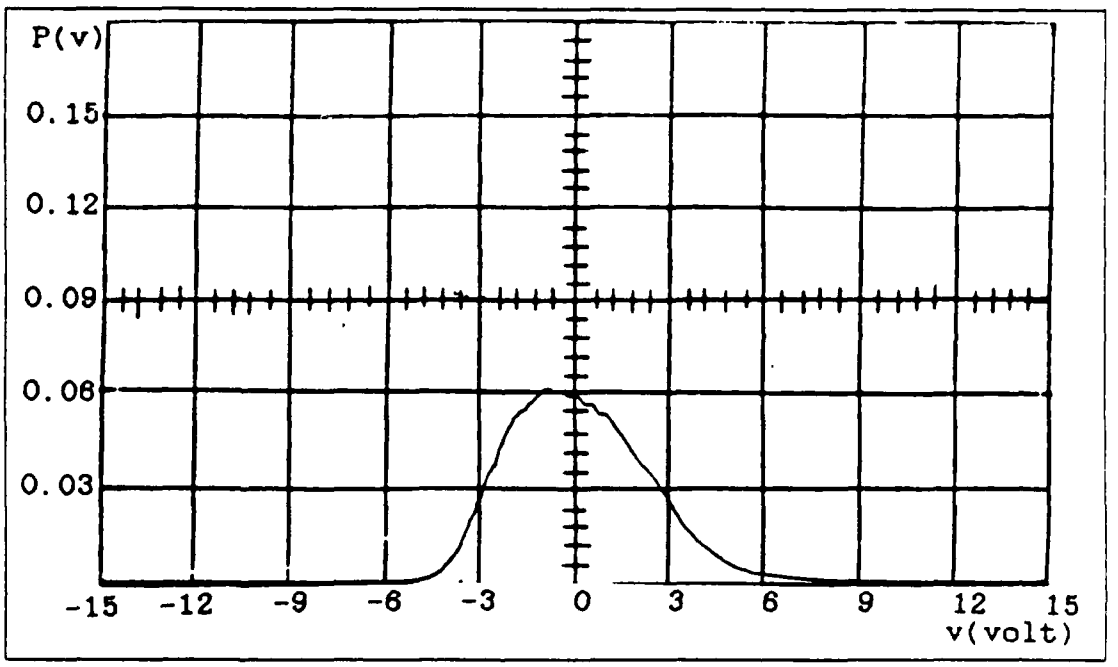


Figure 3.67 Probability Density Function for Frequency Modulated Carrier Plus Noise (SNR = 6 dB

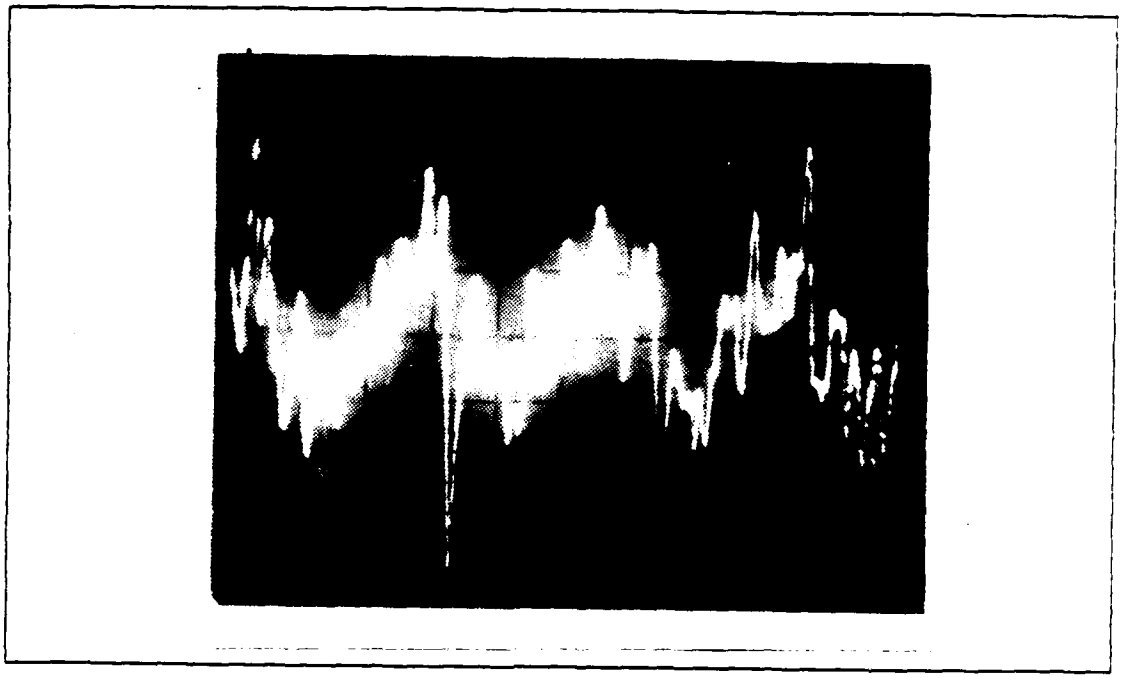


Figure 3.68 Output of the PLL for Frequency Modulated Carrier Plus Noise (SNR = 4 dB).

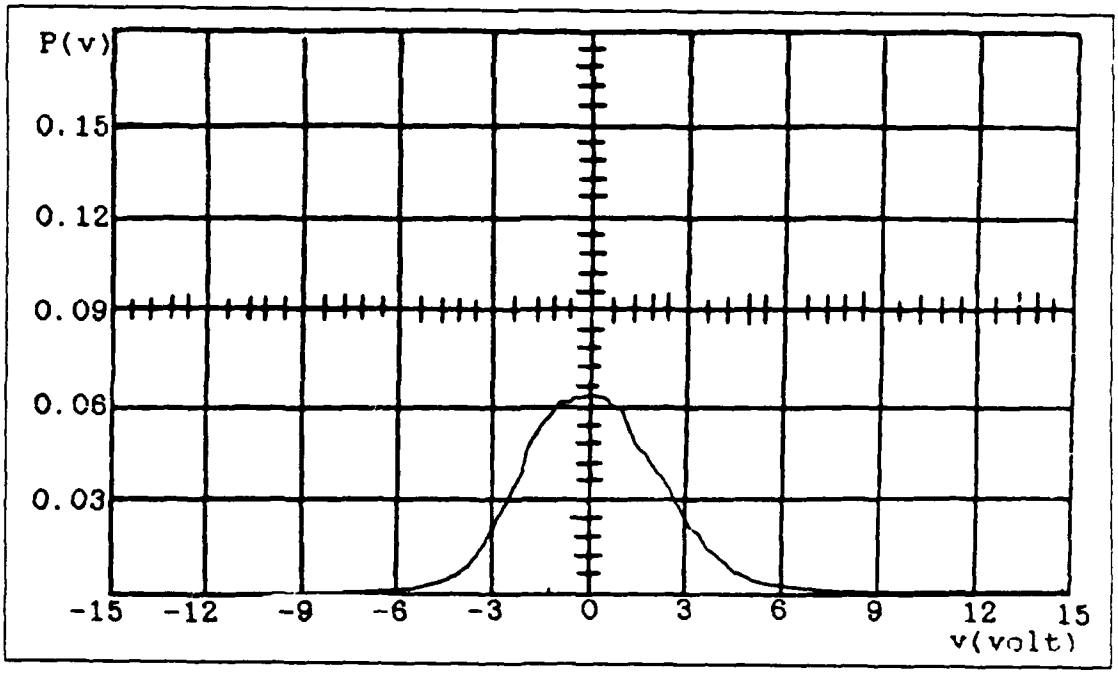


Figure 3.69 Probability Density Function for Frequency Modulated Carrier Plus Noise (SNR = 4 dB).

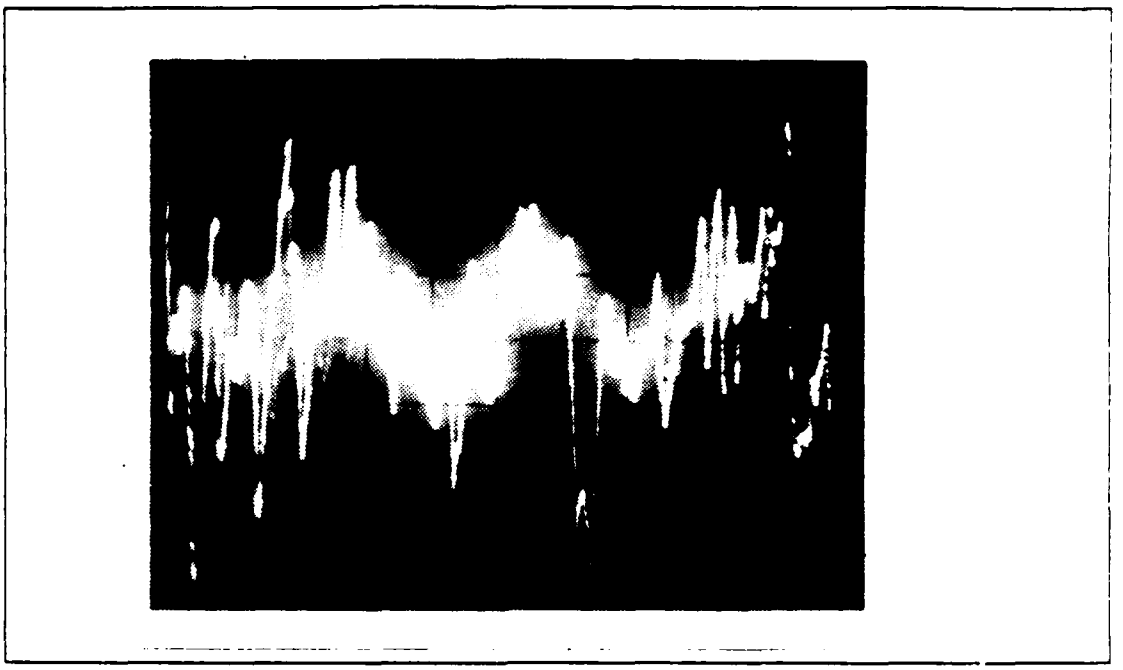


Figure 3.70 Output of the PLL for Frequency Modulated Carrier Plus Noise (SNR = 2 dB).

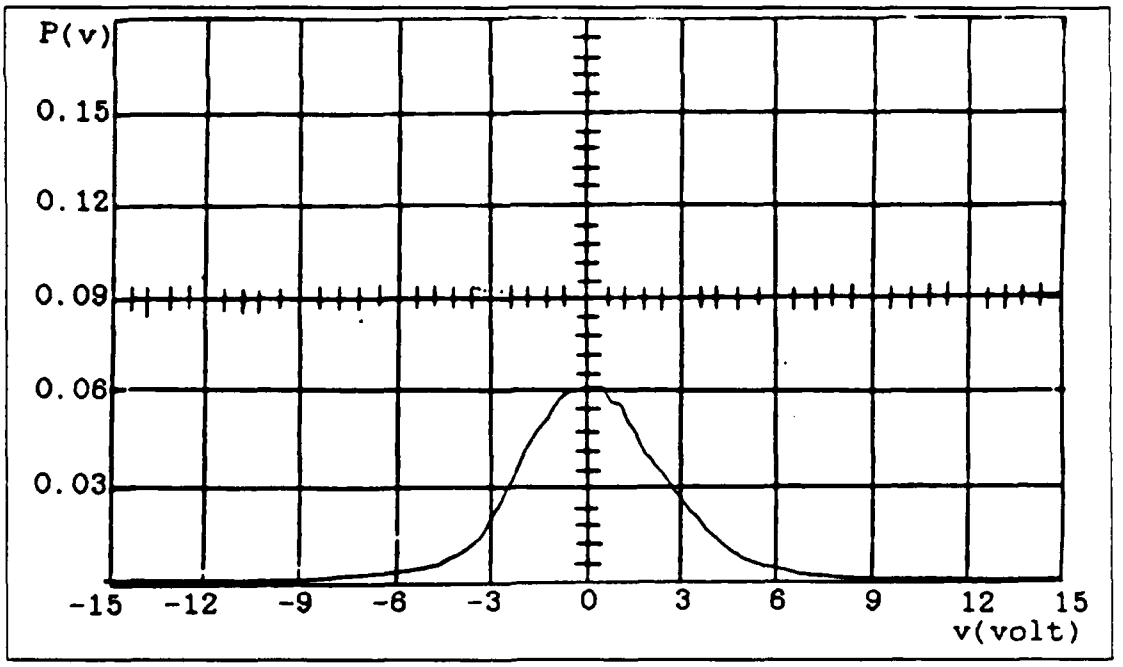


Figure 3.71 Probability Density Function for Frequency Modulated Carrier Plus Noise (SNR = 2 dB

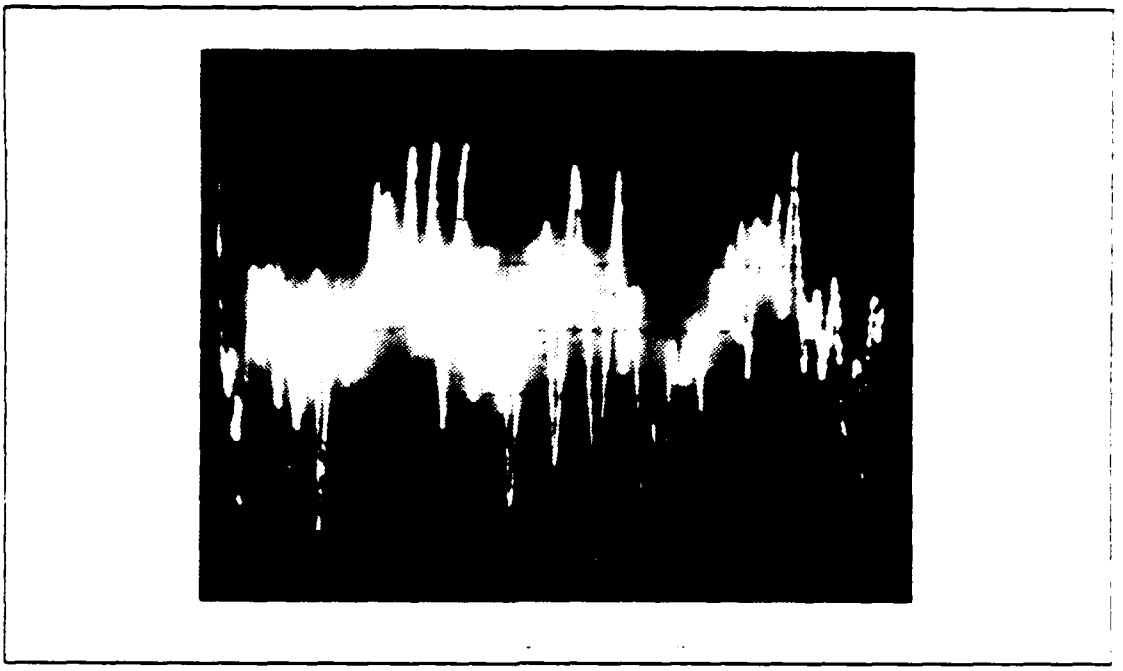


Figure 3.72 Output of the PLL for Frequency Modulated Carrier Plus Noise (SNR = 0 dB).

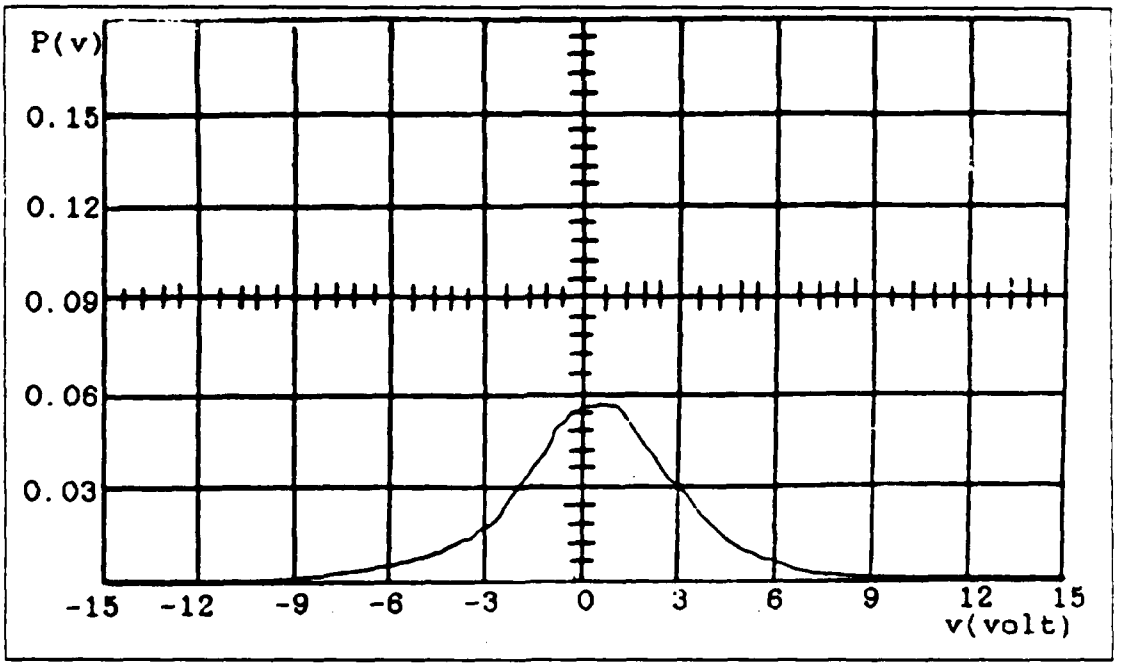


Figure 3.73 Probability Density Function for Frequency Modulated Carrier Plus Noise (SNR = 0 dB).

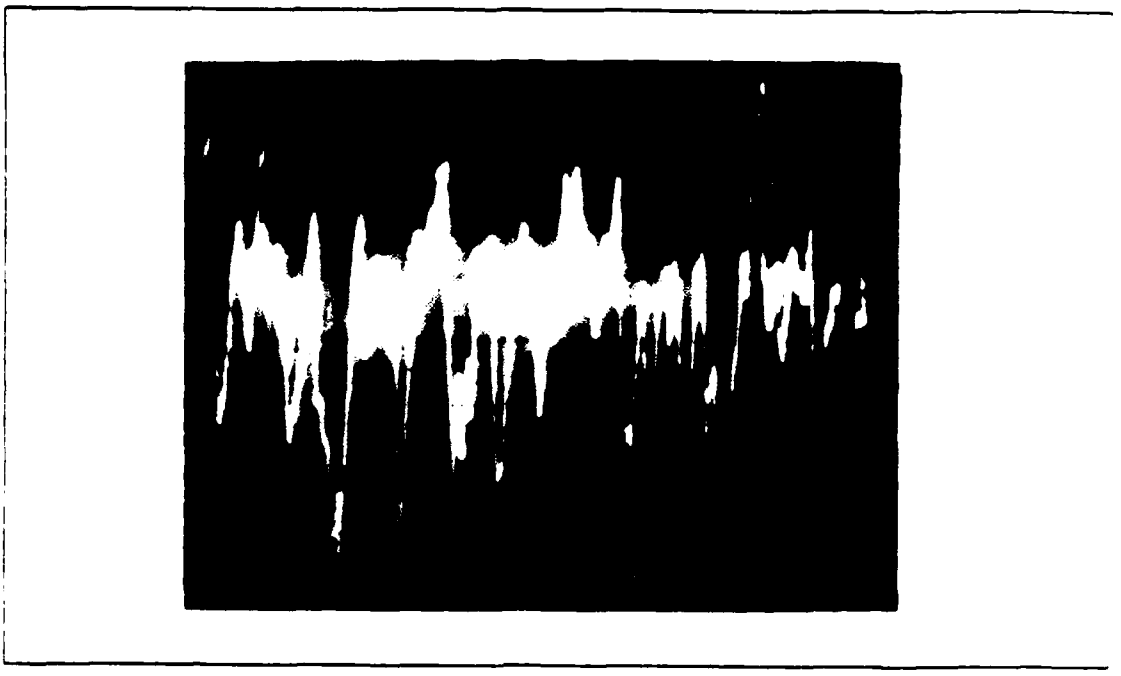


Figure 3.74 Output of the PLL for Frequency Modulated Carrier Plus Noise (SNR = -5 dB).

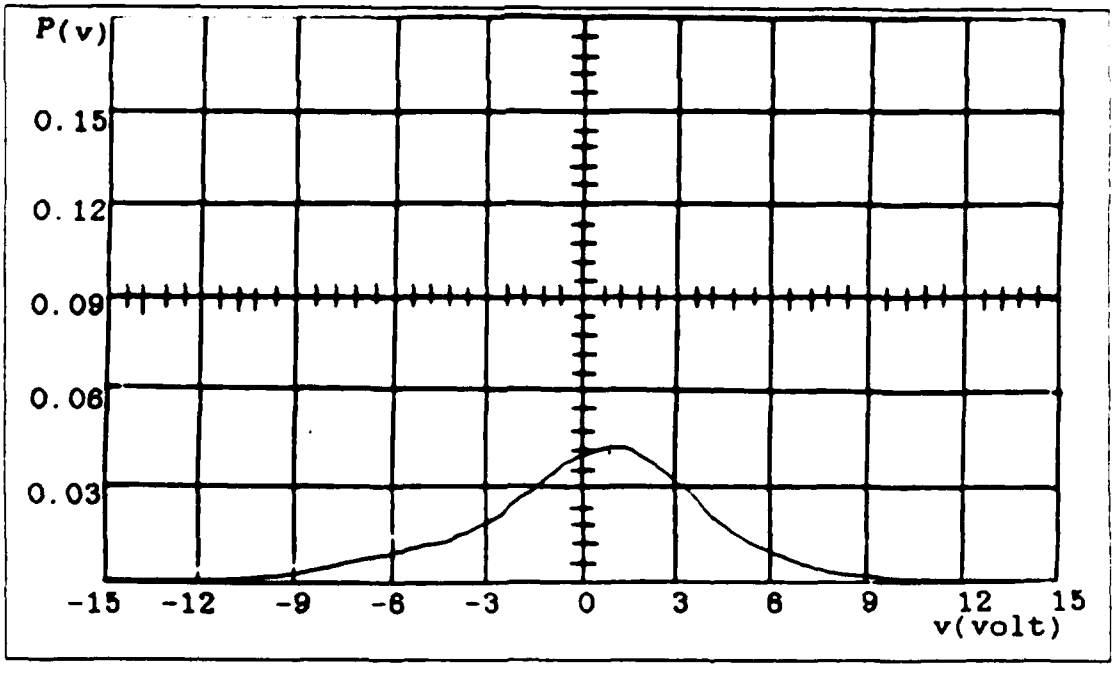


Figure 3.75 Probability Density Function for Frequency Modulated Carrier Plus Noise (SNR = -5 dI

IV. RESULTS AND CONCLUSIONS

A. RESULTS

1. Measurement of the Probability Density Functions

a. Carrier Plus Noise.

As seen in the Figs. 3.4 through 3.19, the probability density function of the PLL output for carrier plus noise input resembles the Gaussian probability density function. Also these figures show that when input signal-to-noise ratio decreases, output variance increases.

b. FSK Carrier Plus Noise.

Figs. 3.21 and 3.39 show the recovered square wave modulating voltage from the PLL output when there is no noise at the input. The probability density function of the square wave is impulses at the peak voltage levels of the square wave as seen in Figs. 3.22 and 3.40. When noise is added to the input signal, the probability density function of the PLL output resembles the Gaussian density function centered at these voltage levels as seen in Figs. 3.24 through 3.38 and Figs. 3.42 through 3.56. The probability density function plots of the FSK carrier plus noise show that as the frequency deviation of the carrier increases, the deviation of the output signal levels increases. This is an increase in output signal power. Also, these figures show that the variance of the output increases as the input noise power increases.

c. FM by Triangular Wave Plus Noise

Fig. 3.58 shows the recovered triangular wave modulating voltage from the PLL output. Fig. 3.59 shows the probability density function of it which is a uniform distribution. When noise power is increased at the input, the probability density function of the PLL output is getting closer to the Gaussian probability density function as seen in Figs. 3.60 through 3.75.

2. Output SNR Calculation for FSK Modulated Carrier.

For this calculation, the output signal level was measured using the digital signal proccessor (SD-360), and X-Y display (SD-311). The average power level of the output signal plus noise was measured using a true RMS voltmeter (HP-3400A). To use the measurement on the X-Y display, scaling of the abscissa is necessary. For this purpose, a sinusoidal wave was used. The probability density function of a sinusoid $x(t) = A\sin\omega t$ is, [Ref. 9]

$$f_x(x) = \frac{1}{\pi\sqrt{(A^2 - x^2)}} \qquad |x| < a$$

A graph of this function is shown in Fig. 4.1. As seen on the graph, the maximum point on the x-axis is 1.414σ. The x-axis was scaled by changing the input sinusoidal wave RMS value.

The output signal power and output signal plus noise power were calculated as the square of measured RMS values. Then the output noise power was calculated as the difference in these noise powers. The output signal-to-noise ratio was then calculated.

Input and output SNR values for a FSK modulated carrier are given in Table 3 of the Appendix for a peak frequency deviation of 5 kHz. Table 4 of the Appendix shows these SNR values for a peak frequency deviation of 3.7 kHz. Fig. 4.2 is a plot of these data.

B. CONCLUSIONS

Experimental results show that the probability density functions of the PLL output for a variety of input signals which are each corrupted by additive bandpass Gaussian noise resembles a Gaussian probability density function (FSK and carrier only). This result agrees with the theoretical results of [Ref. 3] and [Ref. 4]. The results also show the output SNR of a PLL increases with the peak frequency deviation of applied FSK modulated carrier. This result was expected.

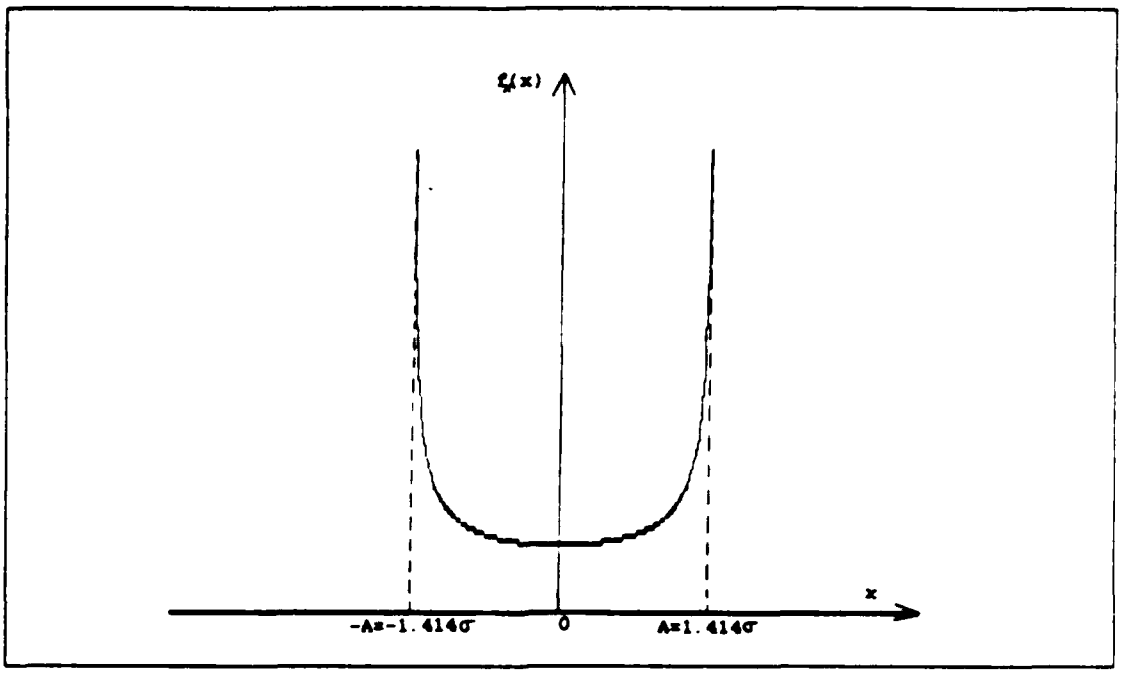


Figure 4.1 Probability Density Function of the Sinusoidal Wave.

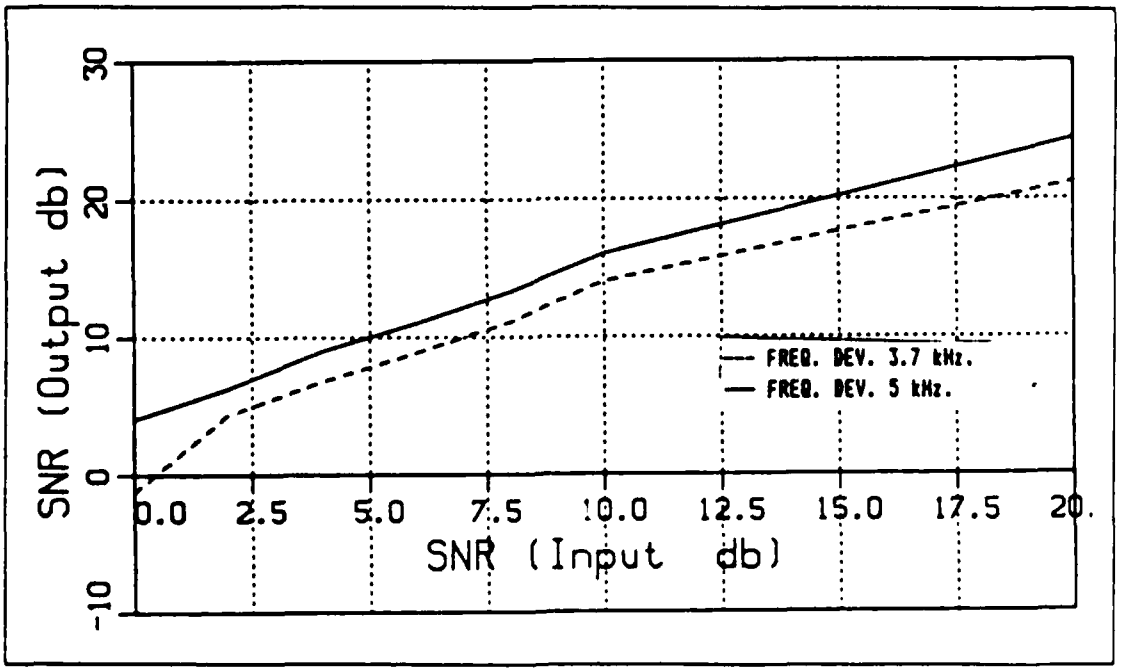


Figure 4.2 Input SNR vs. Output SNR for FSK Modulated Carriers.

APPENDIX
TABLES

TABLE 1
MEASURED DATA OF THE LOOP FILTER

Input voltage to the filter (V_{in}) = 2.75V.

Frequency(Hz)	Output Voltage(Volt)	Output Voltage(dB.)
10	8.0	9.27
20	8.0	9.27
50	8.0	9.27
70	7.85	9.10
104	7.0	8.11
133	6.5	7.47
156	6.0	6.77
182	5.5	6.0
215	5.0	5.19
251	4.5	4.3
298	4.0	3.25
425	3.0	0.75
666	2.0	-2.76
1389	1.0	-8.78
4000	0.5	-14.8
11627	0.3	-19.2

TABLE 2

CALCULATED AND MEASURED DATA OF THE VCO

Control Voltage(Volt)	Measured Output Frequency (kHz)	Calculated Output Frequency (kHz)
3.00	27.3	26.7
4.00	36.0	35.65
4.50	40.26	40.1
5.00	44.47	44.56
5.50	48.60	49.02
6.00	52.81	53.47
6.25	54.89	55.7
6.50	56.92	57.93
6.75	58.94	60.16
7.00	60.97	62.38
7.25	62.96	64.61
7.50	64.93	66.84
7.75	66.88	69.07
8.00	68.84	71.30
8.25	70.81	73.53
8.50	72.77	75.75

TABLE 3

SNR VALUES FOR FSK MODULATED CARRIER

Frequency Deviation = 5 kHz.

Input SNR Values(dB)	Output SNR values(dB)
20	24.35
10	16.00
8	13.30
6	11.00
4	9.00
2	6.25
0	4.00

TABLE 4

INPUT OUTPUT SNR VALUES FOR FSK MODULATED CARRIER

Frequency Deviation = 3.7 kHz

Input SNR Values(dB)	Output SNR Values(dB)
20	21.20
10	14.00
8	11.10
6	8.85
4	6.75
2	4.34
0	-1.3

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6.	Department Chairman, Code 62 Naval Postgraduate School Monterey, California 93943	2
7.	LTJG. M.Topcu, Turkish Navy Rustempasa mah, Kumbaz cad, No = 2/A, Sapanca, Sakarya, Turkey	6

END

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