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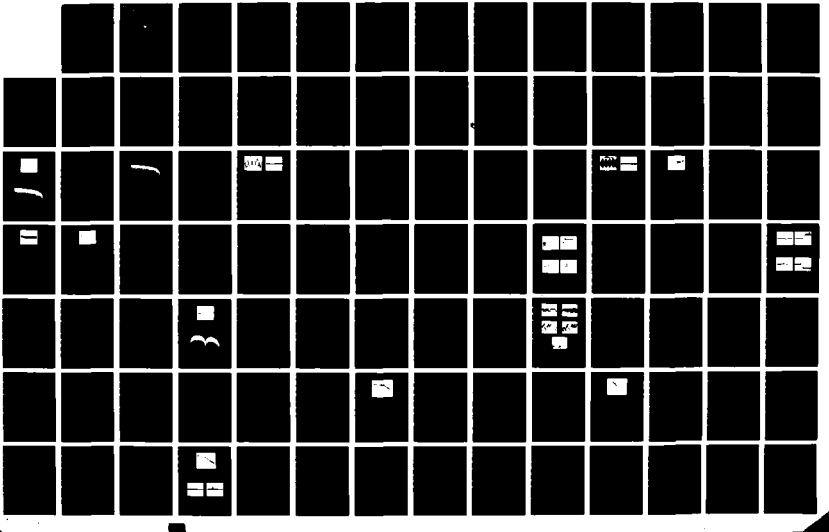

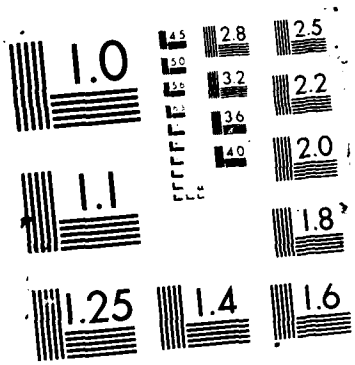
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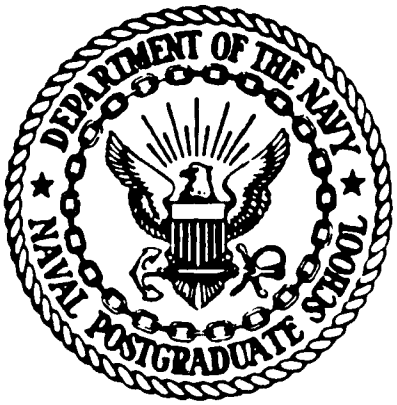

THESIS

MEASURED NOISE PERFORMANCE OF A DIRECT-SEQUENCE SPREAD-SPECTRUM SYSTEM AND A COMPARISON OF SINGLE- VICE DUAL-CHANNEL DELAY-LOCK LOOPS

by

Chris G. Bartone

September 1987

Thesis Advisor: Glen Myers

UNCLASSIFIED

SECURITY CLASSIFICATION OF THIS PAGE

REPORT DOCUMENTATION PAGE

1a REPORT SECURITY CLASSIFICATION Unclassified	1b RESTRICTIVE MARKINGS
2a SECURITY CLASSIFICATION AUTHORITY	3 DISTRIBUTION/AVAILABILITY OF REPORT Approved for public release; distribution is unlimited
2b DECLASSIFICATION/DOWNGRADING SCHEDULE	
4 PERFORMING ORGANIZATION REPORT NUMBER(S)	5 MONITORING ORGANIZATION REPORT NUMBER(S)
6a NAME OF PERFORMING ORGANIZATION Naval Postgraduate School 6b OFFICE SYMBOL (If applicable) 62	7a NAME OF MONITORING ORGANIZATION Naval Postgraduate School
6c ADDRESS (City, State, and ZIP Code) Monterey, California 93943-5000	7b ADDRESS (City, State, and ZIP Code) Monterey, California 93943-5000
8a NAME OF FUNDING/SPONSORING ORGANIZATION 8b OFFICE SYMBOL (If applicable)	9 PROCUREMENT INSTRUMENT IDENTIFICATION NUMBER
8c ADDRESS (City, State, and ZIP Code)	10 SOURCE OF FUNDING NUMBERS PROGRAM ELEMENT NO / PROJECT NO / TASK NO / WORK UNIT ACCESSION NO

11 TITLE (Include Security Classification)
Measured Noise Performance of a Direct-Sequence Spread-Spectrum System and a Comparison of Single- vice Dual-Channel Delay-Lock Loops

12 PERSONAL AUTHOR(S)
Bartone, Chris G.

13a TYPE OF REPORT	13b TIME COVERED	14 DATE OF REPORT (Year Month Day)	15 PAGE COUNT
Master's Thesis	FROM ____ TO ____	September 1987	104

16 SUPPLEMENTARY NOTATION

17 COSATI CODES			18 SUBJECT TERMS (Continue on reverse if necessary and identify by block number)
FIELD	GROUP	SUB GROUP	Direct-Sequence Spread-Spectrum, BPSK, LPI, Communications, Delay-Lock Loop, Processing Gain Spread Spectrum, AJ, AM, AM-DSB-SC

19 ABSTRACT (Continue on reverse if necessary and identify by block number)

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20 DISTRIBUTION/AVAILABILITY OF ABSTRACT	21 ABSTRACT SECURITY CLASSIFICATION
☒ UNCLASSIFIED/UNLIMITED ☐ SAME AS RPT ☐ DTIC USERS	Unclassified
22a NAME OF RESPONSIBLE INDIVIDUAL Glen A. Myers	22b TELEPHONE (Include Area Code) 408-646-2325 22c OFFICE SYMBOL 62Mv

DD FORM 1473, 84 MAR 83 APR edition may be used until exhausted
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SECURITY CLASSIFICATION OF THIS PAGE
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Measured Noise Performance of a Direct-Sequence Spread-Spectrum System and a Comparison of Single- vice Dual-Channel Delay-Lock Loops

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Submitted in partial fulfillment of the
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MASTER OF SCIENCE IN ELECTRICAL ENGINEERING

from the

NAVAL POSTGRADUATE SCHOOL
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TABLE OF CONTENTS

LIST OF SYMBOLS AND ABBREVIATIONS

ACF	Autocorrelation Function
AJ	Anti-Jam
AM	Amplitude Modulated
AVM	Analog Voltage Multiplier
AWGN	Additive White Gaussian Noise
A	Amplitude of an Arbitrary Pulse
A_c	Amplitude of the Composite M-Sequence
A_o	Amplitude of the Carrier
A_l	Amplitude of a Locally Generated M-Sequence
A_r	Amplitude of the Received Sequence $v_r(t)$
A_v	Amplitude of a Bipolar M-Sequence
BER	Bit Error Ratio
BPF	Bandpass Filter
bps	Bits per Second
BPSK	Binary Phase Shift Keying
BSG	Binary Sequence Generator
BW	Bandwidth
CCR	Coherent Carrier Recovery
$c(t)$	Carrier Oscillator
DCDLL	Dual-Channel Delay-Lock Loop
DIP	Dual-in-Line Package
DLL	Delay-Lock Loop
DS	Direct-Sequence

DSB	Double-Sideband
$d(t)$	Unipolar Pseudorandom Data
$\hat{d}(t)$	Estimate of Original Unipolar Pseudorandom Data
E_b	Energy per Bit
FSR	Feedback Shift Register
f_c	Center Frequency of a Bandpass Filter
f_d	The Rate of the Data Clock
f_ℓ	The Rate of the Local (Receiver) Clock and Sequences
f_o	Operating Carrier Frequency, (f_o = 455 kHz)
f_r	The Rate of the Received Sequence
f_t	The Rate of the Transmitter Clock and Sequence
$f_{3\text{dB}}$	The 3 dB Cutoff Frequency of a Filter
G	Gain
HP	Hewlett-Packard
IC	Integrated Circuit
IF	Intermediate Frequency
K	Constant Gain of IF Bandpass Filter
L	Length of the M-Sequence in Chips Before Repeating, (L = 255)
LO	Local Oscillator
LPF	Lowpass Filter
LPI	Low Probability of Intercept
m	Maximal-Length
$m(t)$	Unipolar M-Sequence
$\overline{m}(t)$	Inverted Unipolar M-Sequence
$m_\ell(t + T_c)$	Unipolar Locally Generated Early M-Sequence
$m_\ell(t)$	Unipolar Locally Generated Punctual M-Sequence

$m_\ell(t - T_c)$	Unipolar Locally Generated Late M-Sequence
$m_c(t)$	Unipolar Composite M-Sequence
N_o	Magnitude of the Noise Spectral Density Function
$n(t)$	Bandpass White Gaussian Noise
$n_r(t)$	Baseband White Gaussian Noise (in-phase component)
$n_s(t)$	Baseband White Gaussian Noise (quadrature-phase component)
P_e	Probability of Bit Error
PG	Processing Gain
Pr	Probability
PSD	Power Spectral Density Function
PSK	Phase Shift Keying
P_T	rms Value of the Total Voltage (Signal Plus Noise)
$\overline{P_T}$	Averaged rms Value of the Total Voltage
R_d	Data Bit Rate, (R_d = 62.75 bps)
$R_x(\tau)$	Autocorrelation Function of the signal $x(t)$
$R_{v_m}(\tau)$	Autocorrelation Function of the signal $v_m(t)$
SCDLL	Single-Channel Delay-Lock Loop
SNR	Signal-to-Noise Ratio
S	rms Value of the Signal Voltage
$s(t)$	Transmitted Signal
$S_n(f)$	Bandpass Noise Power Spectral Density Function of $n(t)$
$S_{m_c}(f)$	Baseband Power Spectral Density Function of $m_c(t)$
$S_m(f)$	Baseband Power Spectral Density Function of $m(t)$
$S_d(t)$	Baseband Power Spectral Density Function of $d(t)$
τ	Relative Time Difference
TTL	Transistor-Transistor Logic

T_b	Duration of a Data Bit, (T_b = 15.94 msec)
T_c	Duration of a Chip
T_m	Duration of the M-Sequence Before Repeating
T_u	Upper Limit of Integration
UBC	Unipolar-to-Bipolar Converter
VCO	Voltage Controlled Oscillator
$v_b(t)$	Bipolar Baseband Sequence After Carrier Demodulation
$v_d(t)$	Bipolar Pseudorandom Data Sequence
$v_e(t)$	Error Voltage Generated by the Delay-Lock Discriminator
$v'_e(t)$	Error Voltage Generated at the Output of the Loop Lowpass Filter
$v_{\mathrm{ID}}(t)$	Voltage at the Output of the Integrate and Dump Matched Filter
$v_i(t)$	Voltage at the Input to the DLL and Data Recovery System
$v_\ell(t + T_c)$	Bipolar Locally Generated Early M-Sequence
$v_\ell(t)$	Bipolar Locally Generated Punctual M-Sequence
$v_\ell(t - T_c)$	Bipolar Locally Generated Late M-Sequence
$v_m(t)$	Bipolar M-Sequence
$\overline{v_m}(t)$	Inverted Bipolar M-Sequence
$v_{mm}(t)$	Voltage of the Three-Level Sequence Used in the SCDLL
$v_{m_c}(t)$	Composite Bipolar M-Sequence
$v_r(t)$	Voltage of the Received M-Sequence at the Input to the DLL and Punctual Correlator
$v_{\mathrm{SH}}(t)$	Voltage at the Output of the Sample and Hold Integrated Circuit
$v_1(t)$	Voltage Within the Early Channel of the Delay-Lock Discriminator
$v_2(t)$	Voltage Within the Late Channel of the Delay-Lock Discriminator
$v_3(t)$	Voltage Within the Single-Channel Delay-Lock Discriminator
$v_4(t)$	Voltage Within the Punctual Correlator

WB	Wideband
WGN	White Gaussian Noise
XNOR	Exclusive NOR
XOR	Exclusive OR
*	Convolution Operation

I. INTRODUCTION

A spread spectrum communication system may use any modulation technique to produce a transmitted spectrum that is much larger than the minimum bandwidth (BW) required to transmit the information. One of the more popular choices is the direct-sequence (DS) spread spectrum system. In this technique, digital data directly modulates a high rate binary sequence (code). The resulting waveform then modulates a carrier. Phase shift keying modulation is a popular choice of carrier modulation because of its superior noise performance. Demodulation of the DS spread spectrum signal usually involves a correlation or matched filter operation. [Ref. 1: pp. 328-344]

DS spread spectrum systems are used because they have processing gain (PG), an improvement in signal-to-noise ratio (SNR) which provides anti-jam (AJ)/interference rejection capabilities. Moreover, because the signal is spread over a large BW, the power density with respect to frequency is decreased which may result in low probability of intercept (LPI) or covert communications. In addition, proper signal design can provide more accurate time/ranging information when compared with narrowband systems.

The purpose of this research effort is to investigate the application of the DS spread spectrum system to a superheterodyne amplitude modulated (AM) radio system that uses an intermediate frequency (IF) of 455 kHz and clock rate of 16 kHz. (Most AM radios use an IF of 455 kHz; the 16 kHz clock rate is chosen for convenience.) This system may be used when a normal AM voice radio is rendered useless because of interference.

A DS spread spectrum system was designed, constructed, and tested. The effort emphasized the spread spectrum aspects and all tests were limited to laboratory testing. This experimental DS spread spectrum system sends data at a rate less than that of digitized voice while utilizing its full radio frequency (RF) bandwidth to achieve processing gain. A spreading factor of 255 was implemented by using a maximal-length binary sequence generator. Binary phase shift keying (BPSK) modulation was used. This results in an increased probability of correct message reception.

The DS spread spectrum receiver utilizes a code tracking loop for synchronization and timing; the delay-lock loop (DLL) (typically a two-channel system) is a popular choice. Data collection was limited to two main areas of interest: 1) the noise performance of a single-channel delay-lock loop (SCDLL) in comparison with a dual-channel delay-lock loop (DCDLL) (with no data transmitted), and 2) the noise performance of the DS spread spectrum system while transmitting data using a DCDLL. Bandlimited white gaussian noise (WGN) was added to the transmitted signal to assess the system noise performance.

The results of data collection indicate that the SCDLL will maintain lock with up to 0.64 dB more noise power at the input to the receiver (prior to demodulation). When data is transmitted, data bit recovery can be accomplished at approximately a SNR $= -13$ dB with probability of bit error $P_e = 1 \times 10^{-5}$. This provides for a processing gain of approximately 18.5 dB.

A conclusion of this research effort is that apart from hardware simplicity, the SCDLL provides, in practice, a noise performance advantage relative to the DCDLL. (However, its application is limited.) Another conclusion is that the DS spread spectrum system designed, built, and tested can be used to transmit low rate digital data reliably at values of SNR much less than unity and could be

implemented by a conventional AM radio system with an IF of 455 kHz and a clock rate of 16 kHz.

Chapter II presents the background needed to understand a typical DS spread spectrum system operation. All chapters are divided into transmitter, channel, and receiver sections. Chapter III presents the system design and theory of operation. This chapter includes signal representation as equations, photographs, and frequency spectrum plots as necessary. Chapter IV supports Chapter III and deals with the detailed design, construction and operation of the hardware which was built; it includes circuit performance photographs, plots, and graphs. The Method of Test (Chapter V) and Results and Discussion (Chapter VI) follow which contain information on data collection and interpretation. Conclusions and recommendations are presented in Chapter VII.

II. BACKGROUND

A. DIRECT-SEQUENCE SPREAD SPECTRUM

In a DS spread spectrum system, binary data modulates a binary sequence having a higher bit rate. The resulting binary waveform then modulates a carrier which is transmitted over the channel. Upon reception, the receiver demodulates the carrier and then synchronously demodulates the high rate binary sequence to recover the data. Figure 1 illustrates a typical DS spread spectrum system.

1. Transmitter Subsystem

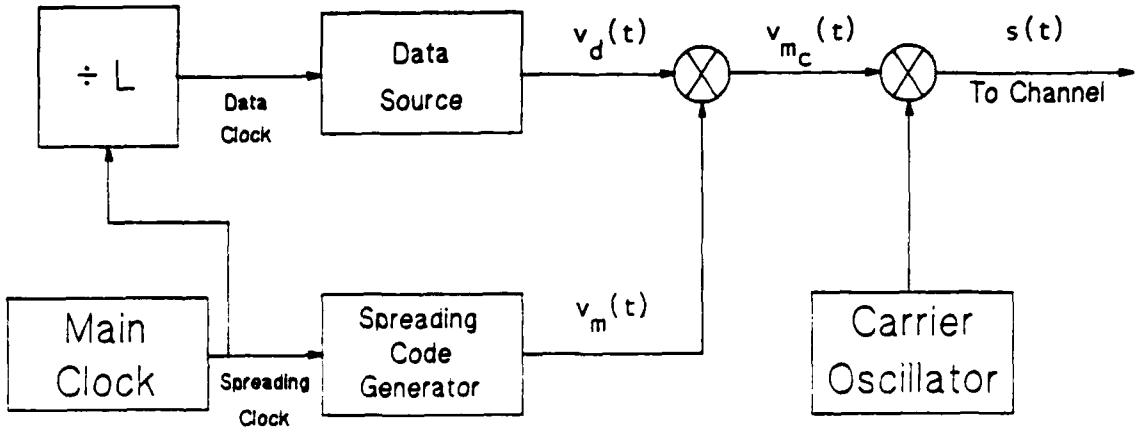
An important parameter of the DS spread spectrum system is the spreading binary sequence. The choice of the sequence $v_m(t)$ used for spreading affects the noise performance of the system, ease of synchronization and even the maximum number of users the system can accommodate.

The most popular choice of binary sequence is a maximal length or m-sequence. The m-sequence, by definition, is the longest sequence (maximum period or maximum number of chips[1] per bit) that can be generated by a delay element or shift register of a given length [Ref. 2: p. 58].

It is desirable that the binary sequence have a "good" autocorrelation function (ACF). In general the ACF of a wide sense stationary (stationary to the order two) known signal $x(t)$ of finite duration is defined as

$$R_x(\tau) = \int_{-\infty}^{\infty} x(t)x(t-\tau)dt \tag{1}$$

[1] The binary elements of the sequence are called chips. The binary elements of the data are called bits. DS spreading implies there are many chips per bit.



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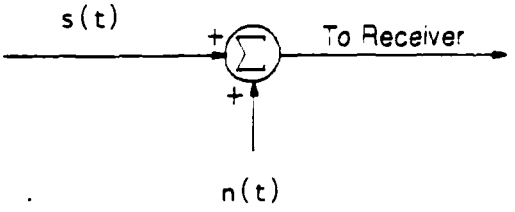

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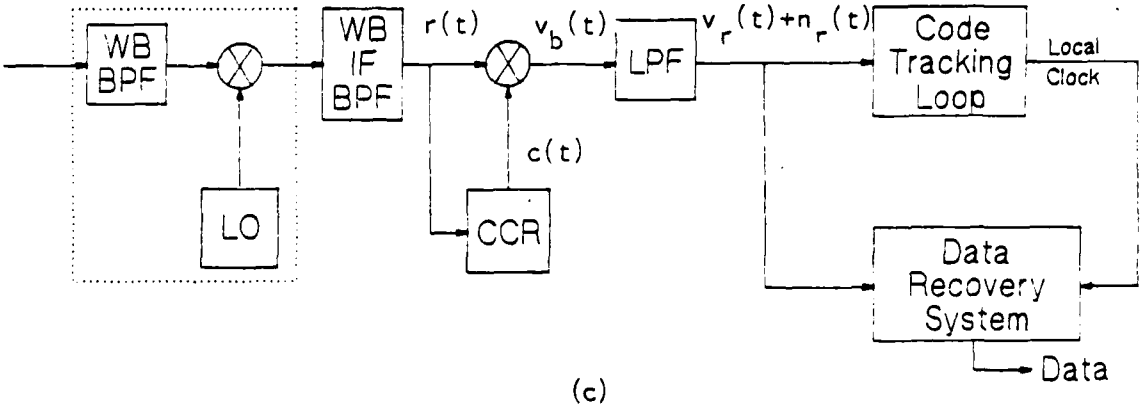


(c)

Figure 1. Typical Direct Sequence Spread Spectrum System, a) Transmitter, b) Channel, and c) Receiver.

where τ is a relative time delay in seconds [Ref. 3: pp. 85-86]. If we now consider an m-sequence having constant amplitude values of $\pm$ 1 volts, then we obtain the well known ACF of an m-sequence

$$R_{v_m}(\tau) = \begin{cases} 1 - \frac{\tau}{T_c}\left(1 + \frac{1}{\mathrm{L}}\right) & \text{for} \quad 0 \leq \tau \leq T_c \\ -\frac{1}{\mathrm{L}} & \text{for} \quad T_c < \tau < \frac{T_m}{2} \end{cases} \tag{2}$$

where

T_c = duration of one chip

L = length of the sequence = number of chips in one period.

Thus,

$$T_m = \mathrm{L}T_c$$

Since the m-sequence repeats with period T_m, then $R_{v_m}(\tau)$ is also periodic with the same period. This ACF is an even function and is plotted in Figure 2 along with $v_m(t)$. [Ref. 1: p. 387]

In practice, one period T_m of $v_m(t)$ is used to represent one data bit interval so that T_m = data bit duration = T_b. This will allow a data 1 to be represented by the sequence $v_m(t)$ and a data 0 to be represented as the inverse of the sequence denoted $\overline{v_m}(t)$. This produces a composite m-sequence $v_{m_c}(t)$ which is illustrated in Figure 1a and can be represented by

$$v_{m_c}(t) = v_m(t) \cdot v_d(t) \tag{3}$$

The composite m-sequence of constant amplitude values $\pm A_c$ is now placed on a carrier of the form

$$c(t) = A_o \cos 2\pi f_o t. \tag{4}$$

A popular choice of modulation in DS spread spectrum systems is BPSK. The modulated carrier $s(t)$, shown in Figure 3, is essentially an AM double-sideband

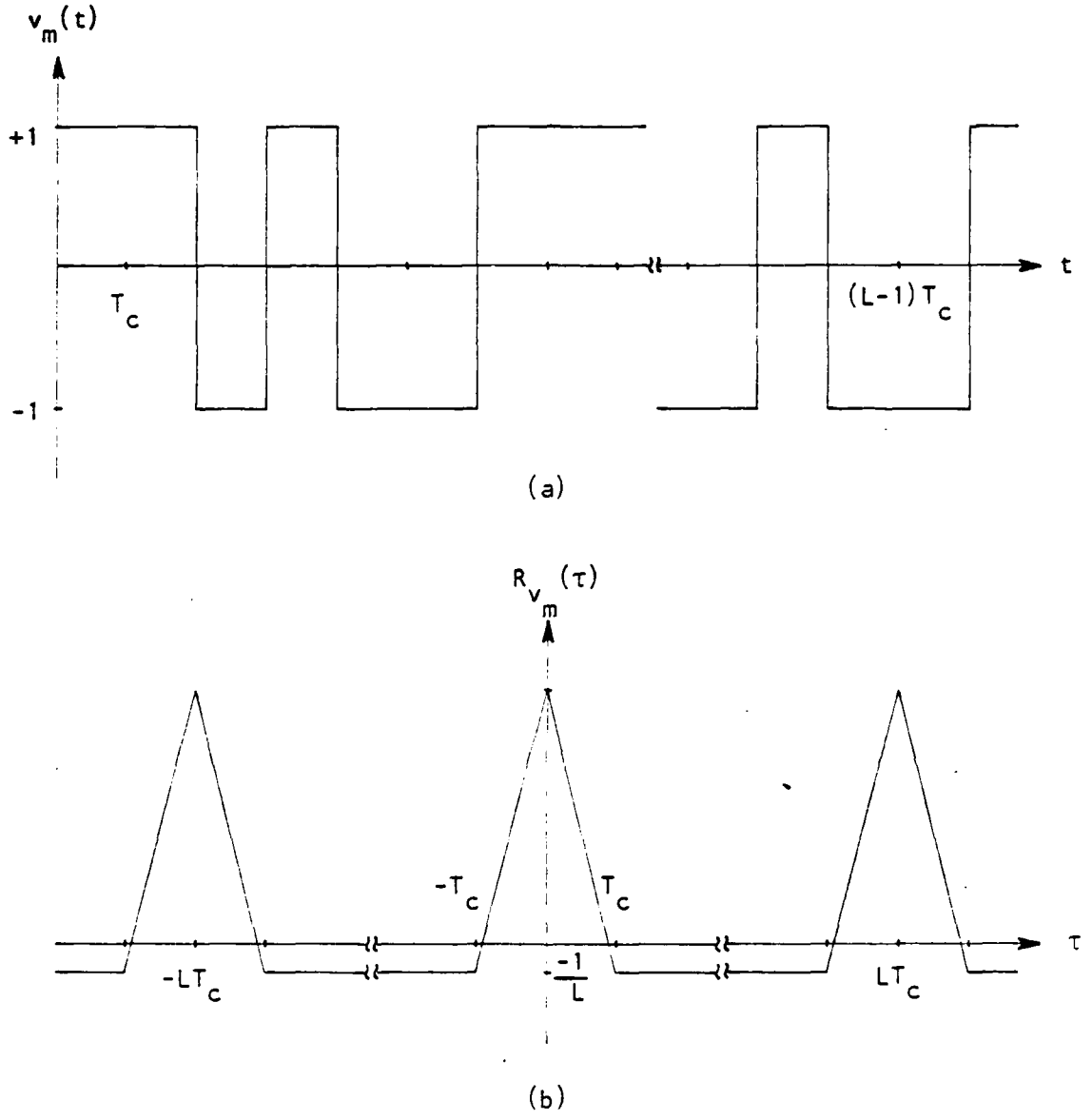


Figure 2. Illustration of a) M-Sequence $v_m(t)$ having amplitude values of $\pm$ 1 volts, and b) its Autocorrelation Function $R_{v_m}(\tau)$.

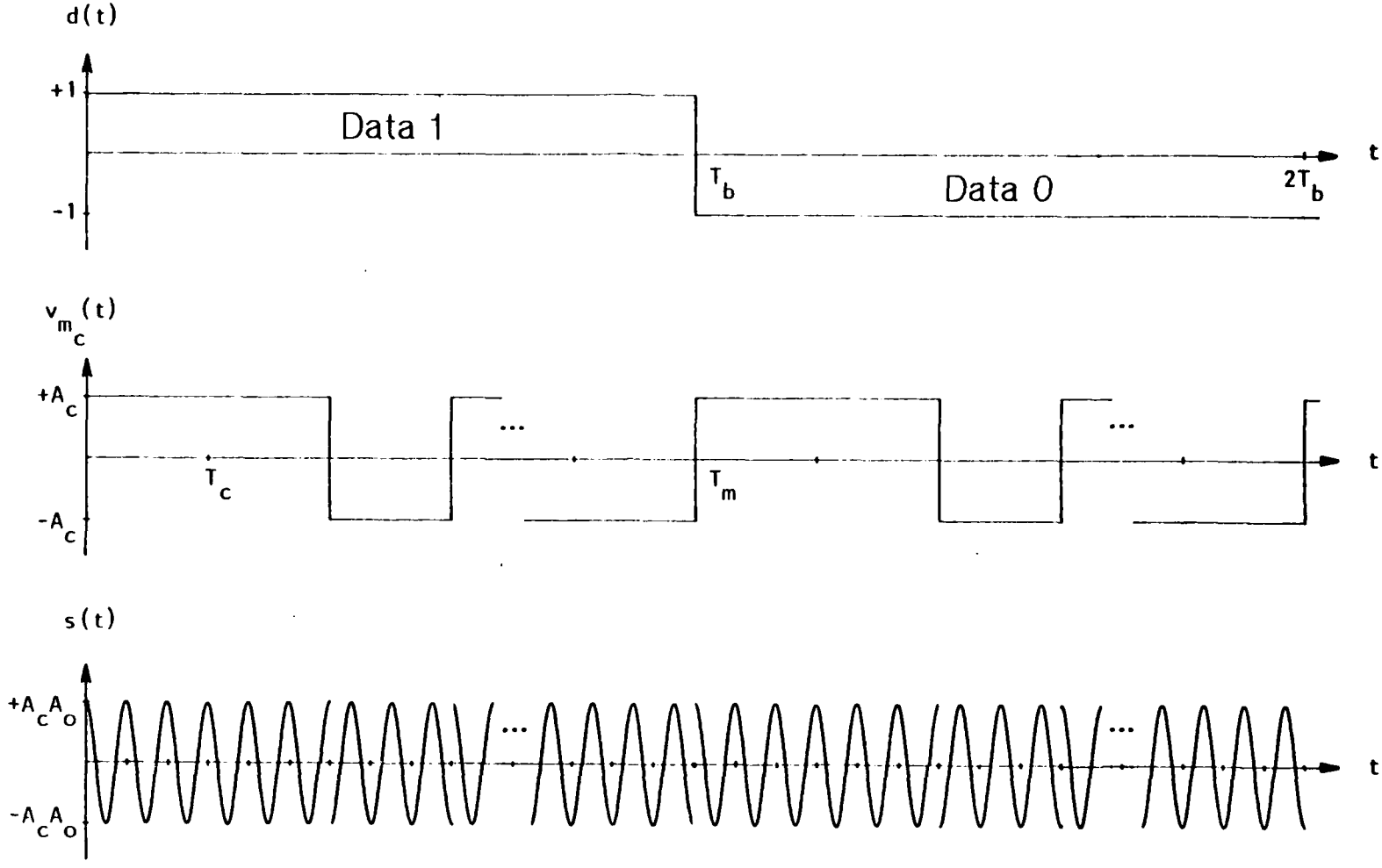


Figure 3. Illustration of Binary Phase Shift Keyed Modulation in a Direct-Sequence Spread-Spectrum System. (Not to Scale).

(DSB) suppressed carrier signal. BPSK modulation is used to provide a signal of "constant" amplitude as it propagates through the channel, and it enables recovery of the modulated waveform when the SNR is less than unity.

The power spectral density (PSD) function at the output of a DS spread spectrum transmitter is well known and easily obtained. The approach is to find the ACF of $v_{m_c}(t)$, take the Fourier transform to obtain a baseband PSD function, and then obtain a bandpass PSD by conversion to a carrier frequency of f_o. The result is

$$S_s(f) = \frac{A_c^2 A_o^2 T_c}{4} \left[\text{sinc}^2(f - f_o)T_c + \text{sinc}^2(f + f_o)T_c\right] \tag{5}$$

This PSD function is illustrated in Figure 4. [Ref. 1: p. 336], [Ref. 3: p. 314]

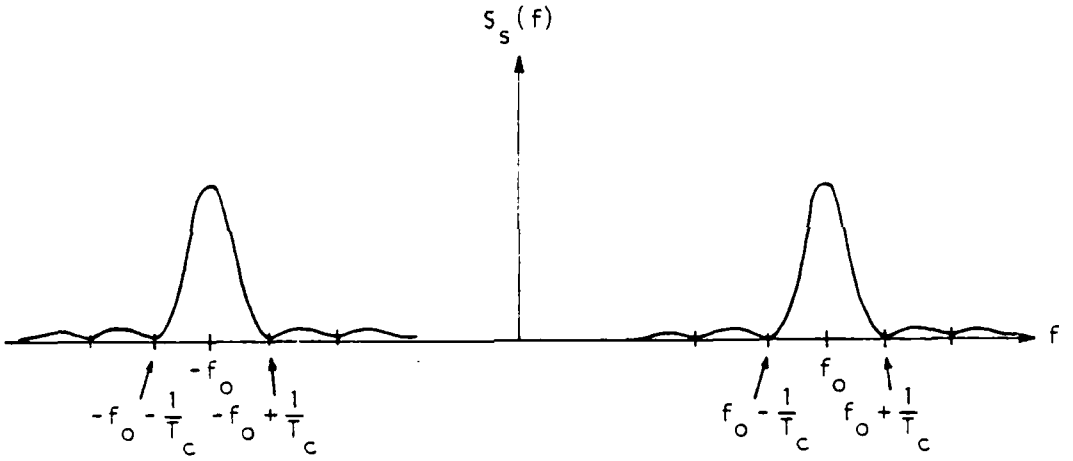


Figure 4. Power Spectral Density Function of Transmitted Signal.

2. Channel Subsystem

For this research effort, a bandlimited additive white gaussian noise (AWGN) model for the channel was assumed, as shown in Figure 1b.

3. Receiver Subsystem

The DS spread spectrum receiver is a conventional superheterodyne system using a wideband (WB) IF amplifier/filter as shown in Figure 1c. After filtering

by a WB bandpass filter (BPF) and non-coherent down-conversion by the local oscillator (LO) (not performed in this research effort), then coherent demodulation of the carrier is accomplished. Coherent demodulation is required because of the choice of BPSK modulation. A coherent reference is provided by the coherent carrier recovery (CCR) system. The demodulator output is filtered by a lowpass filter (LPF) and then applied simultaneously to the code tracking loop and data recovery system. The recovered binary sequence plus noise $v_r(t)+n_r(t)$ is correlated with locally generated sequences to obtain sequence synchronization which then allows data recovery. The DCDLL and the tau-dither (single-channel loop) are the most popular tracking loops for DS spread spectrum receivers. A part of this research effort is the investigation of a SCDLL which can be used to synchronize two binary sequences.

By definition, the PG of a system is[2]

$$\text{PG} = \frac{\text{Output SNR}}{\text{Input SNR}}.$$

DS spread spectrum systems are used because they provide PG which is a direct function of the ratio of radio frequency (RF) BW to the data bit rate. Dixon [Ref. 2: p. 25] concludes that

$$\text{PG} = \frac{\text{3 dB RF BW}}{\text{Data Rate}} = \frac{\text{(0.88) Clock Rate}}{\text{Data Rate}}$$

Thus, when $T_m = T_b$,

$$\text{PG} = 10\log[(0.88)\text{L}] \quad \text{in dB.} \tag{6}$$

[2] A net improvement in SNR occurs when the BW of the interference is much less than the BW of the spread signal. Consequently, the PG concept is sometimes used only for narrowband interference. When the interference is white (constant PSD function over the spread BW; i.e., thermal noise-limited receiver) there is no net improvement in SNR and hence PG = 1. In this report, PG is referred to as the SNR in the data BW divided by the SNR in the BW of the spread signal.

III. SYSTEM DESIGN AND THEORY OF OPERATION

A. TRANSMITTER SUBSYSTEM

The transmitter subsystem is composed primarily of 1) a high rate BSG, 2) a low rate pseudorandom data bit stream generator, and 3) a carrier modulator. Figure 5 is a general block diagram of the transmitter used in this research.

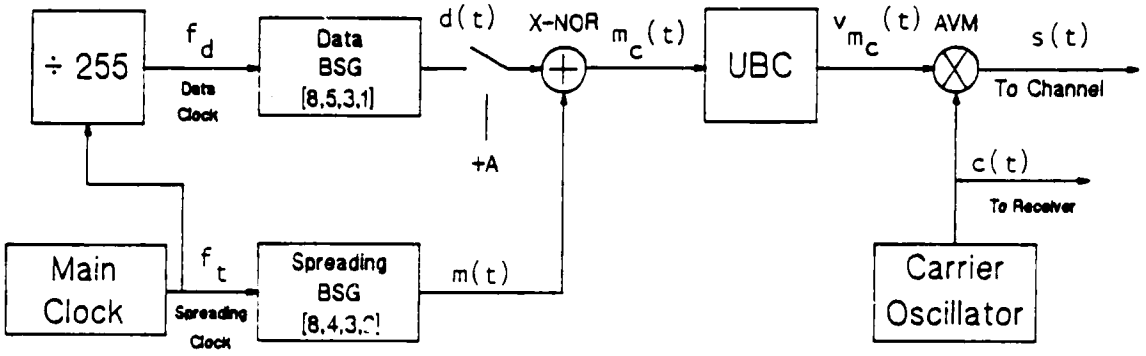


Figure 5. Transmitter General Block Diagram.

1. Binary Sequence Generator

The main clock is at a rate f_t = 16,000 Hz and drives the BSG which is used for spectrum spreading. This clock rate will determine the bandwidth of all signals as well as the data rate. The BSG consists of a binary feedback shift register (FSR) with exclusive OR (XOR) or exclusive NOR (XNOR) logic in the feedback path. In this work, an n = 8 stage serial in, parallel out binary shift register with XNOR logic is used. This produces an L = 2^{n-1} = 255 chip long sequence. (The all 1's state of the FSR is forbidden.) Thus, from equation (6) the PG of our system should be

$$\text{PG} = 10\log[(255)(0.88)] = 23.51 \text{ dB}. \quad (7)$$

Dixon [Ref. 2: pp. 87-88] presents the possible feedback taps for a FSR of length n for n from 2 to 28. The feedback taps [8,4,3,2] are used here. Figure 6 illustrates this BSG. The BSG produces a unipolar m-sequence $m(t)$ with period $T_m = LT_c =$ 15.94 msec where $T_c = 1/f_t = 62.5$ μsec.

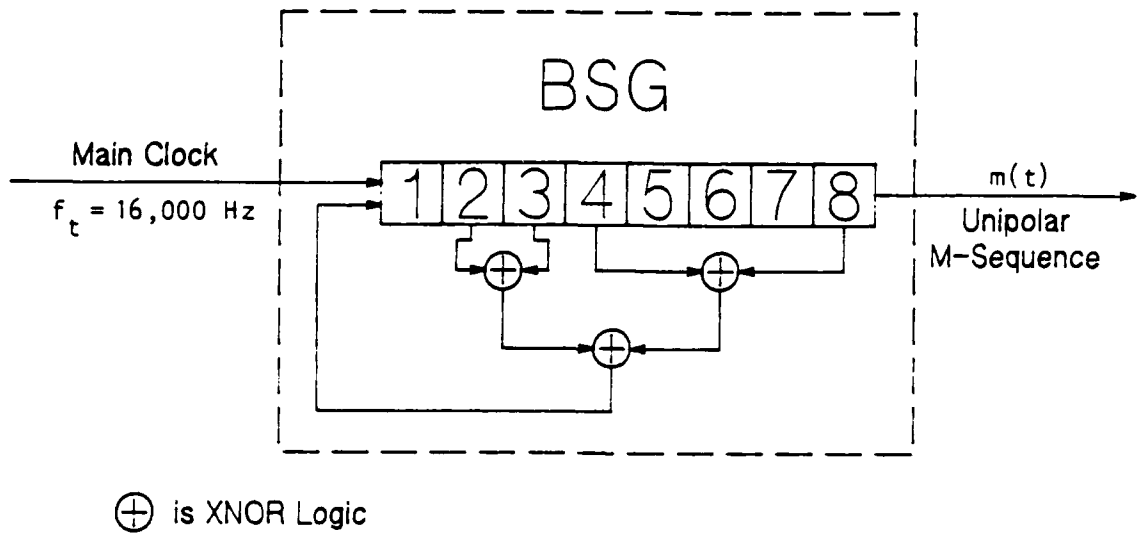


Figure 6. 8-Bit Maximal Length Binary Sequence Generator with Feedback Connections [8,4,3,2].

2. Data Generator

In Figure 6 the main clock is also applied to a divide-by-255 counter to produce a synchronous data clock. The rate of this data clock is the same as the data rate which is $R_d = f_d = f_t/L = 67.75$ bits/sec (bps). Pseudorandom data is generated by another 8 stage BSG, similar to the spreading BSG, except the feedback taps of [8,5,3,1] are used to generate a unipolar data sequence $d(t)$.

3. Composite Sequence Generation

Referring to Figure 5, the spreading m-sequence $m(t)$ and the data bit stream $d(t)$ are applied to an XNOR circuit to produce a composite unipolar sequence $m_c(t)$. Thus, when a data 1 is transmitted, $m_c(t) = m(t)$ and when a data 0 is transmitted $m_c(t) = \overline{m}(t)$, each of duration 255 chips. The unipolar composite

sequence $m_c(t)$ is converted to a bipolar sequence with the unipolar-to-bipolar converter (UBC) to produce $v_{m_c}(t)$. This produces $v_{m_c}(t) = v_m(t) \cdot v_d(t)$ as shown in Figure 7 and illustrates an equivalence between a unipolar/XNOR/UBC operation and bipolar/voltage multiplication. Moreover, when considering the "good" ACF of an m-sequence, a bipolar format is preferred. Figure 8 illustrates $v_{m_c}(t)$ and its Fourier transform. In Figure 8, $A_c = 5.8$ volts (V). The frequency spectrum plot was measured on a Hewlett-Packard (HP) 8566B Spectrum Analyzer and is for one sweep of the voltage. Figure 8b illustrates the measured line spectrum of the signal from 0 to 16 kHz; there are L = 255 discrete lines separated by 62.75 Hz. Figure 8c is the maximum (envelope) of the spectrum in the range 0 to 48 kHz.

When data is part of $v_{m_c}(t)$, then from equation (3)

$$v_{m_c}(t) = v_m(t) \cdot v_d(t).$$

By Fourier transform theory, this multiplication corresponds to convolution in the frequency domain, so the PSD function of the baseband composite sequence is

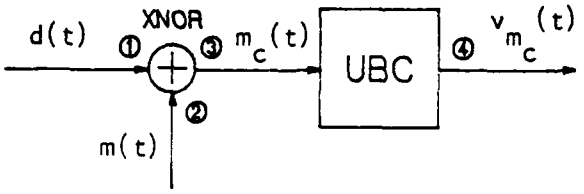
$$S_{m_c}(f) = S_m(f) * S_d(f).$$

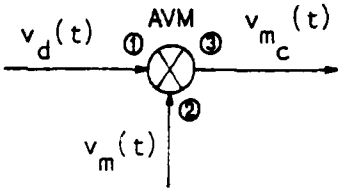
Because the rate of the sequence $v_{m_c}(t)$ is much higher than the data rate and because the data is pseudorandom, $S_{m_c}(f)$ becomes continuous. This is illustrated in Figure 9.

4. Carrier Modulation

From equation (4), the IF carrier oscillator in Figure 5 is represented by $c(t) = A_o \cos 2\pi f_o t$ where $f_o = 455$ kHz. Therefore the transmitted signal can be represented as

$$\begin{aligned} s(t) &= v_{m_c}(t) \cos 2\pi f_o t \\ &= \begin{cases} +A_c A_o \cos 2\pi f_o t & \text{when} \quad v_{m_c}(t) = +1 \\ -A_c A_o \cos 2\pi f_o t & \text{when} \quad v_{m_c}(t) = -1 \end{cases} \end{aligned}$$

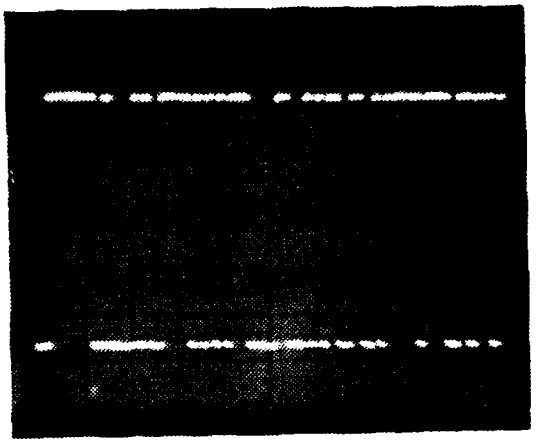




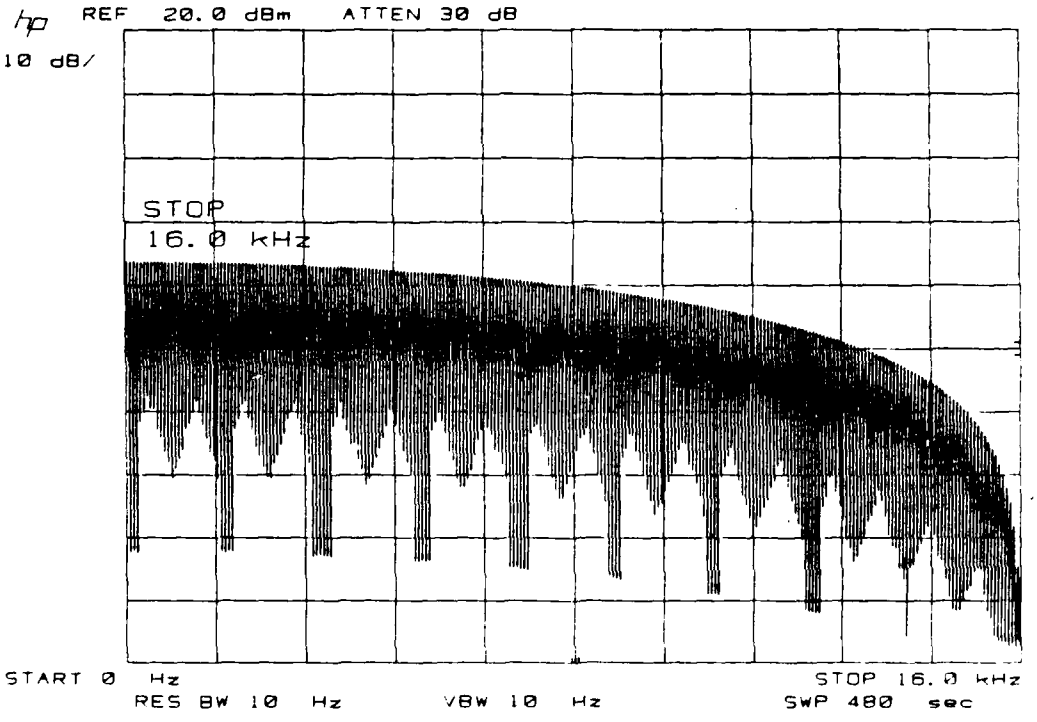
STATE			
1	2	3	4
0	0	A	$+A_v^2$
0	A	0	$-A_v^2$
A	0	0	$-A_v^2$
A	A	A	$+A_v^2$

STATE		
1	2	3
$-A_v$	$-A_v$	$+A_v^2$
$-A_v$	$+A_v$	$-A_v^2$
$+A_v$	$-A_v$	$-A_v^2$
$+A_v$	$+A_v$	$+A_v^2$

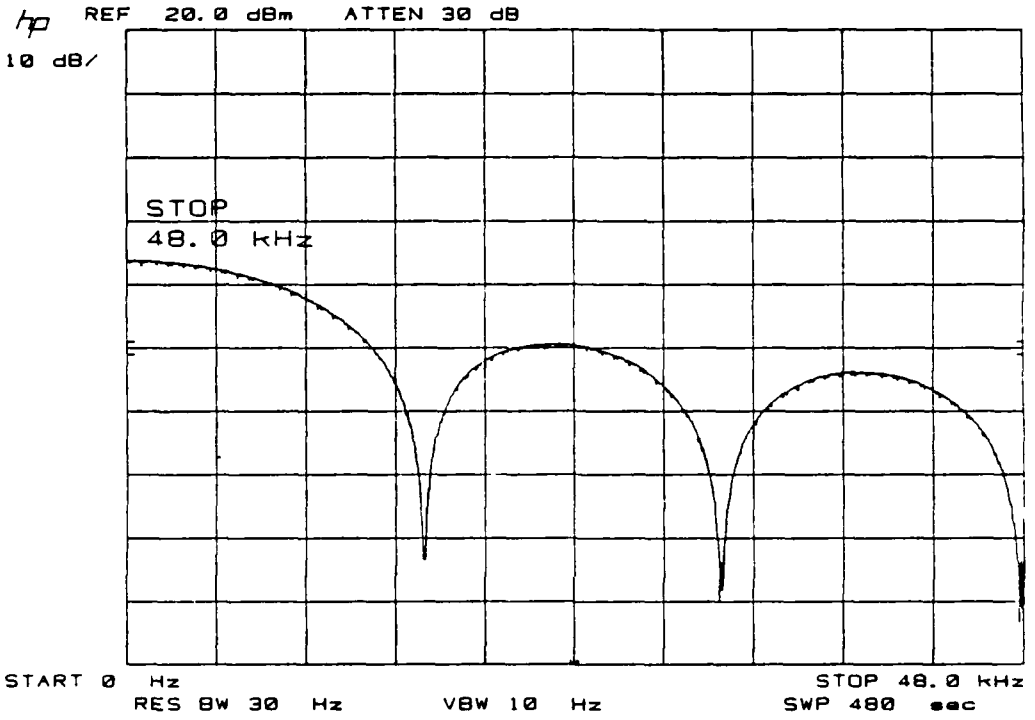
Figure 7. Illustration of the Equivalence Between Unipolar/XNOR/UBC and Bipolar/Analog Voltage Multiplication Operations.



(a)

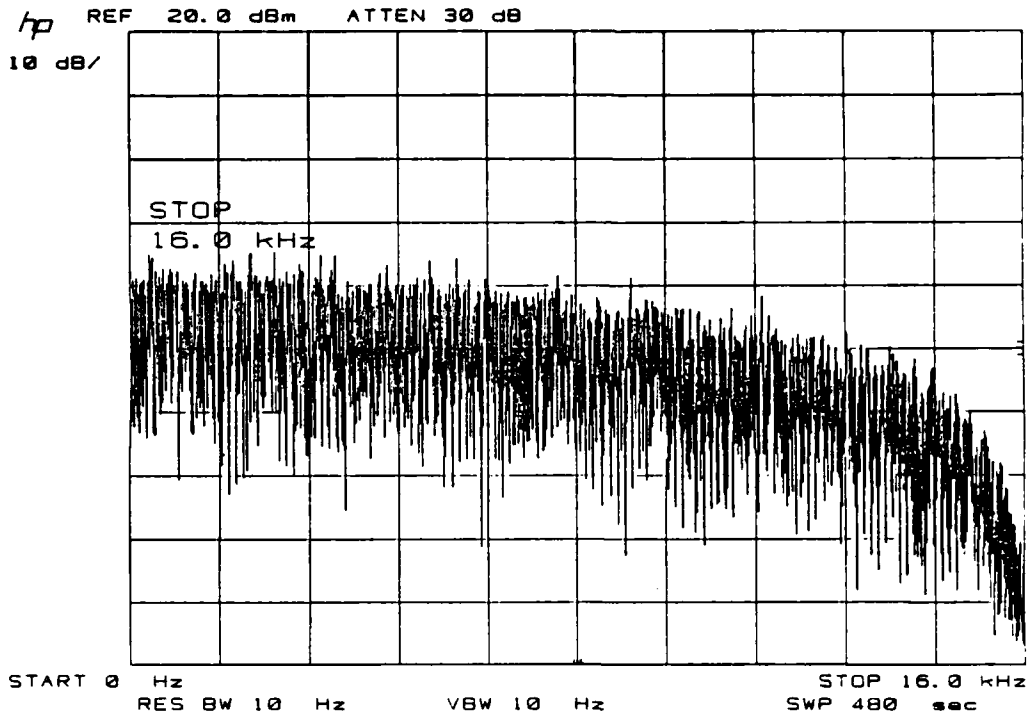

REF 20.0 dBm
ATTEN 30 dB
10 dB/
STOP
16.0 kHz
START 0 Hz
STOP 16.0 kHz
RES BW 10 Hz
VBW 10 Hz
SWP 480 sec

(b)

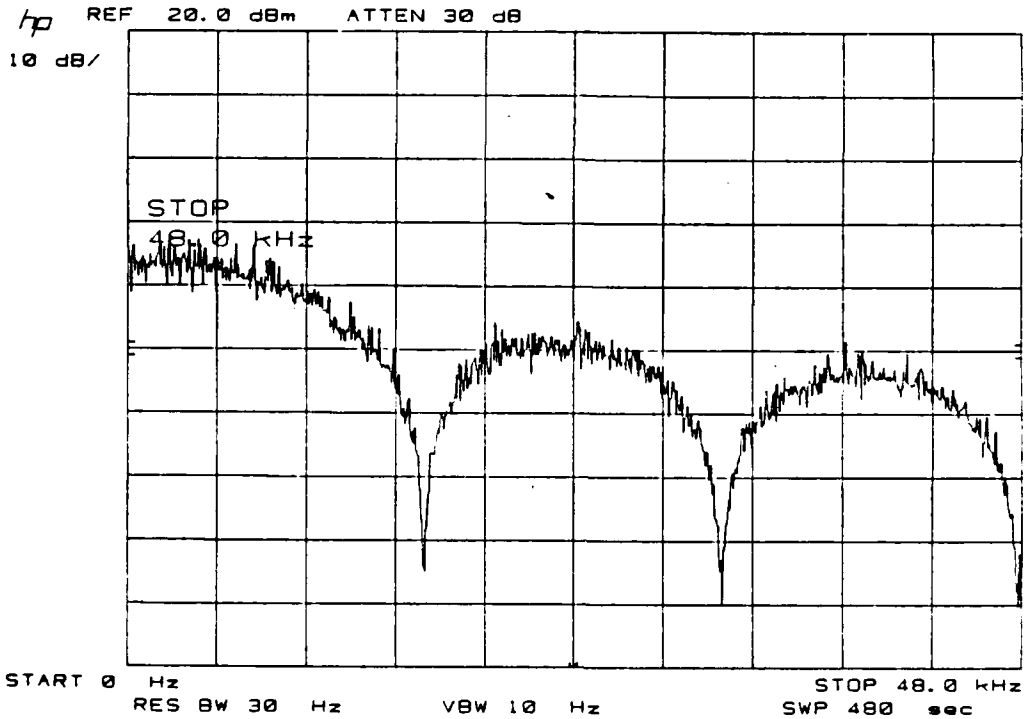


(c)

Figure 8. Representation of the Bipolar Composite M- Sequence $v_{m_c}(t)$ with no Data a) Time Domain (Scales: Horizontal; 5msec/div., Vertical; 2 V/div.), b) Frequency Spectrum (0 to 16 kHz), c) Envelope of Frequency Spectrum (0 to 48 kHz).



(a)



(b)

Figure 9. Representation of the Composite Sequence $v_{m_c}(t)$ with Data a) Frequency Spectrum (0 to 16 kHz), b) Envelope of Frequency Spectrum (0 to 48 kHz).

where

$$(n-1)T_c < t < nT_c \quad \text{for} \quad n = 1, 2, 3, \ldots$$

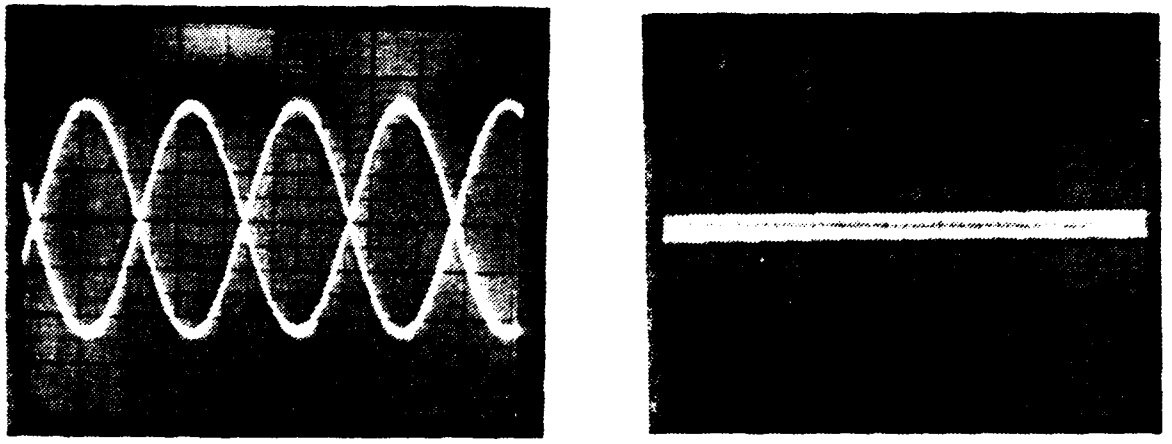
The PSD function of $s(t)$ is given by equation (5) where $T_c = 62.5$ μsec and $f_o = 455$ kHz. This leads to a spectrum that has a null-to-null BW about f_o of 32 kHz and a 3 dB BW of 14.1 kHz. Figure 10 illustrates the measured transmitted signal in the time and frequency domain.

B. CHANNEL SUBSYSTEM

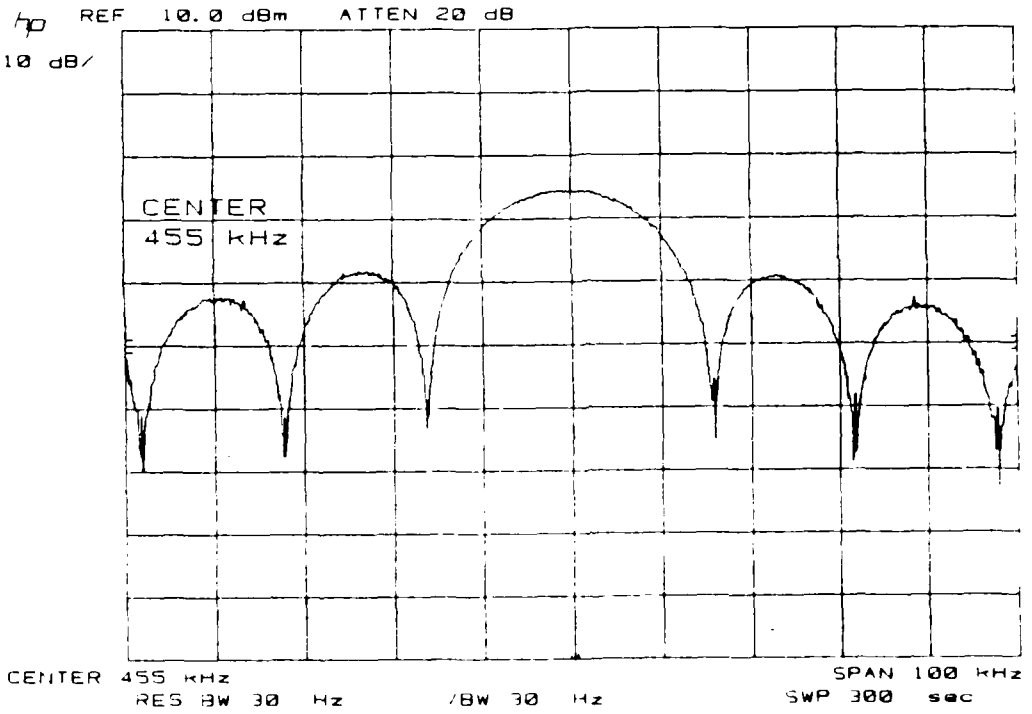
For this research effort, bandlimited WGN $n(t)$ is added to the transmitted signal $s(t)$ as represented in Figure 11. Because small values of SNR are needed during testing, the WGN signal is first filtered and then applied to an amplifier having 40 dB of gain (G). The theoretical PSD of this bandpass noise is illustrated in Figure 12. Figure 13 illustrates the measured noise spectrum as measured on the HP 8566B Spectrum Analyzer at a noise power level that produced a SNR = -13 dB. When this noise is added to the transmitted signal $s(t)$, the envelope of the resulting frequency spectrum is that which is illustrated in Figure 14. This figure indicates that when the DS spread spectrum signal passes through a noisy channel, it may be heavily masked by the noise and covert/LPI communication may result.

C. RECEIVER SUBSYSTEM

The receiver subsystem is comprised primarily of 1) a carrier demodulation and filtering network which recovers the noisy spread sequence, 2) a DLL used to synchronize the received spread sequence with a locally generated replica, and 3) a punctual correlator which is used for data recovery. The receiver general block diagram is presented as Figure 15.



(a) (b)



(c)

Figure 10. Representation the Transmitted Signal $s(t)$ with no Noise (no Data in $v_{m_c}(t)$), a) Time Domain (Scales: Horizontal: 0.5 μsec/div., Vertical: 0.5 V/div.), b) Time Domain (Scales: Horizontal: 2 msec/div. (X10), Vertical: 1 V/div.), c) Envelope of Frequency Spectrum.

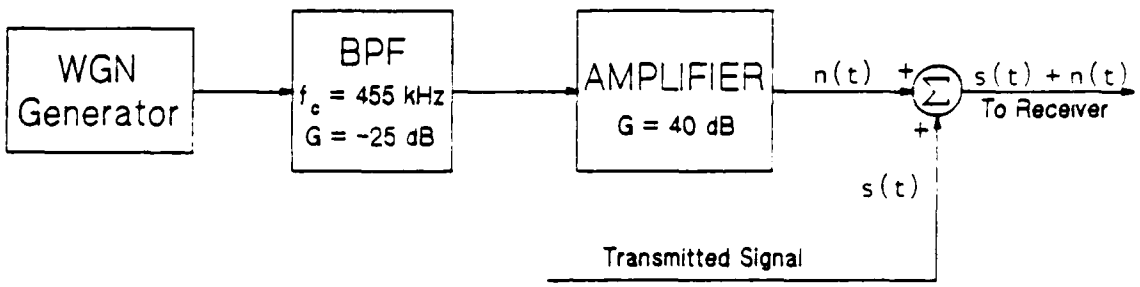


Figure 11. Block Diagram of the Additive White Gaussian Noise Channel.

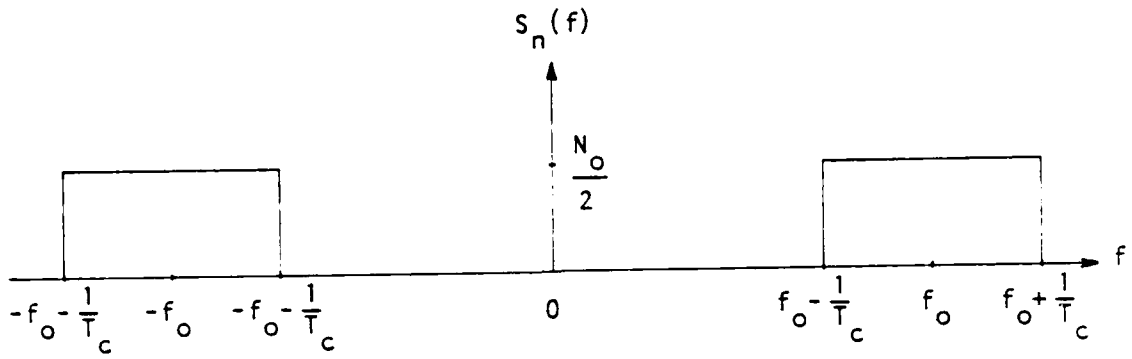


Figure 12. Calculated Power Spectral Density $S_n(f)$ of $n(t)$.

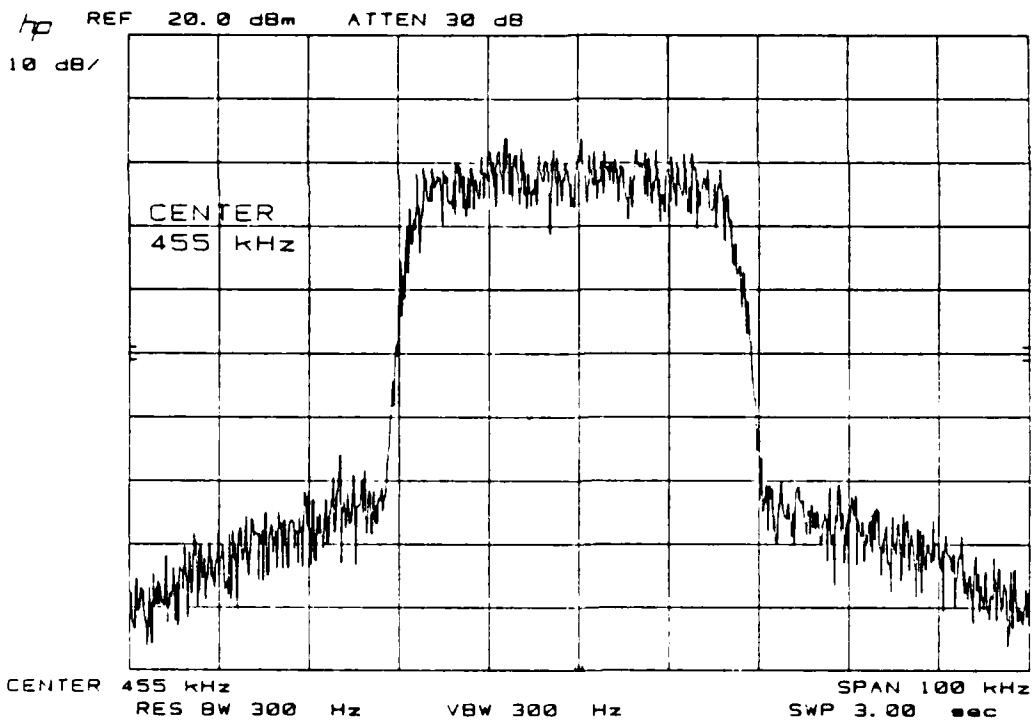


Figure 13. Envelope of Frequency Spectrum for the Bandlimited WGN $n(t)$ corresponding to SNR $= -13$ dB.

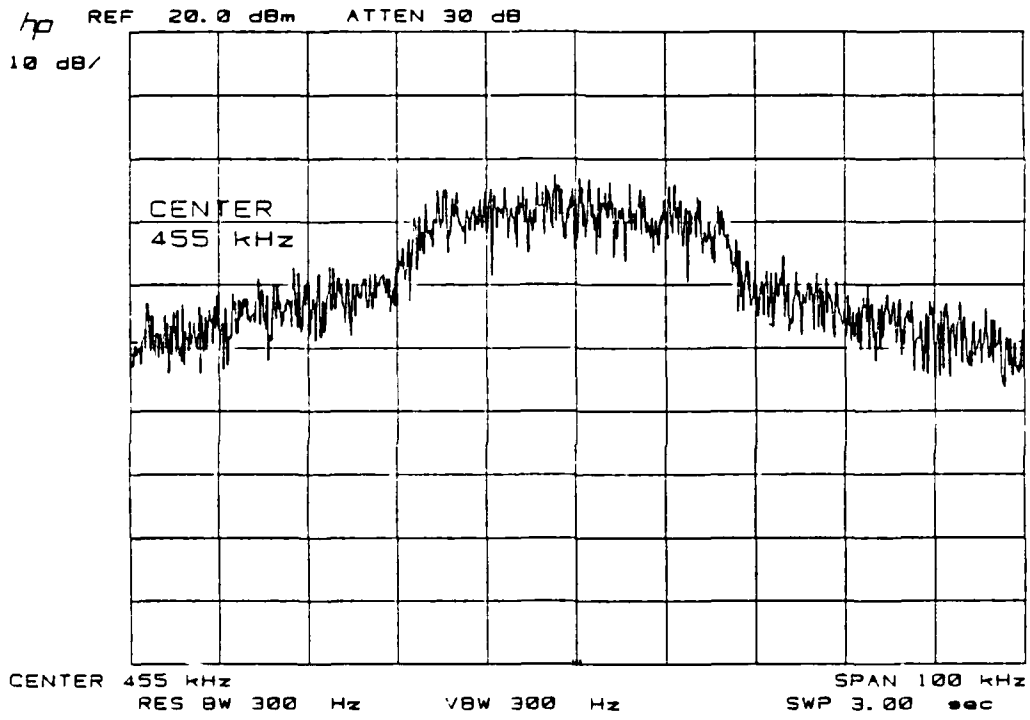


Figure 14. Envelope of Resulting Frequency Spectrum of $s(t) + n(t)$ for SNR $= -13$ dB.

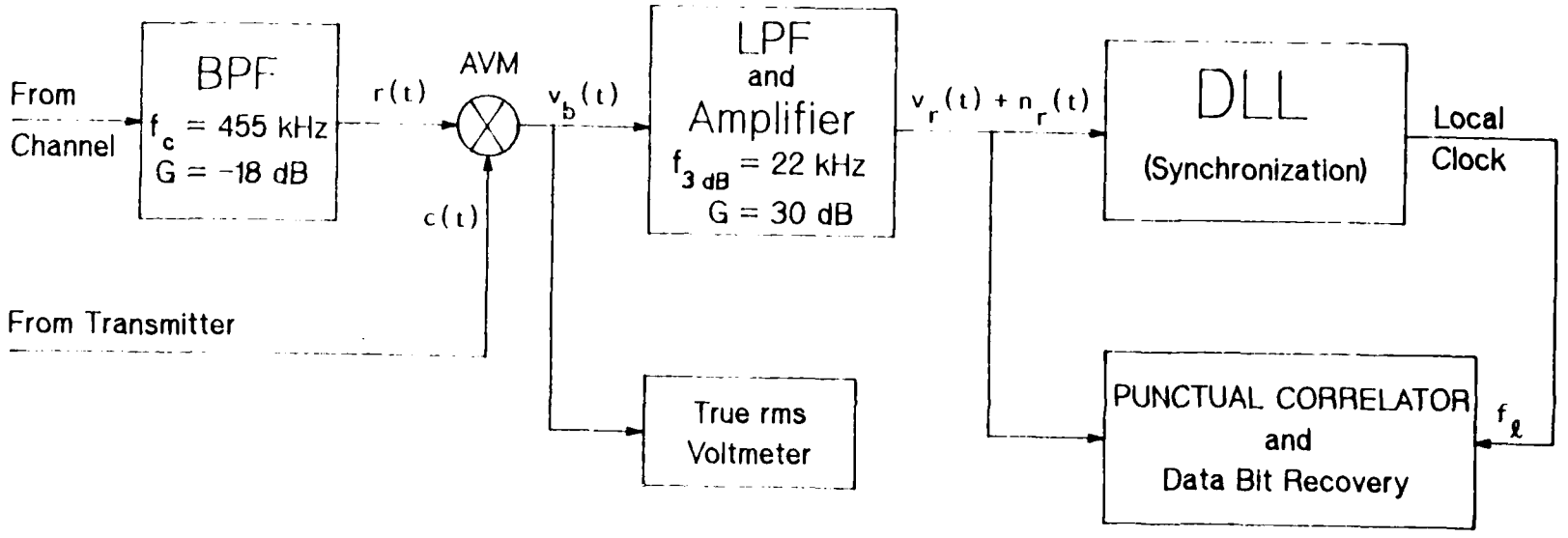


Figure 15. Receiver General Block Diagram.

1. Carrier Demodulation and Filtering Network

In this experiment, the transmitted signal was not radiated. A wire connects the transmitter to the "channel" and another wire connects the channel to the receiver. The BPF of Figure 15 functions as the IF amplifier/filter in a typical superheterodyne receiver. This filter functions to pass most of the signal and reject noise. The bandlimited signal is illustrated in Figure 16 in the time and frequency domain with no noise. Once noise is added, the resulting time and frequency domain representations are shown in Figure 17 at a SNR = -13 dB.

The filtered voltage $r(t)$ is then demodulated. BPSK requires a coherent reference for demodulation. The interest of this research is the spread spectrum aspects of the system. Therefore, the carrier oscillator signal in the transmitter also serves as the coherent reference in the receiver; typically a Costas or squaring loop will perform this function [Ref. 2, p. 279].

The baseband signal (demodulator output) can be expressed as

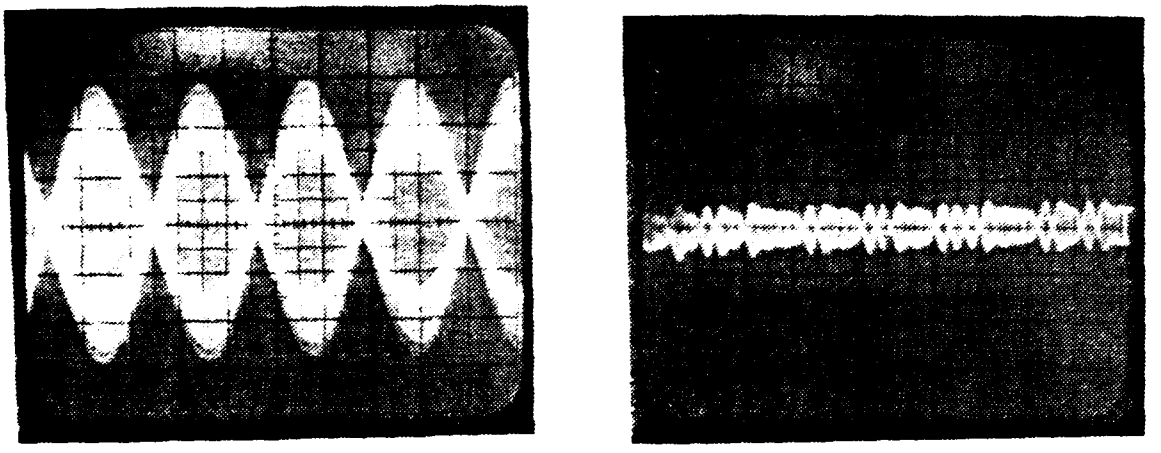
$$\begin{aligned} v_b(t) &= r(t) \cdot c(t) \\ &= K[s(t) + n(t)]c(t) \\ &= K[v_{m_c}(t)\cos 2\pi f_o t + n(t)]\cos 2\pi f_o t \end{aligned}$$

where

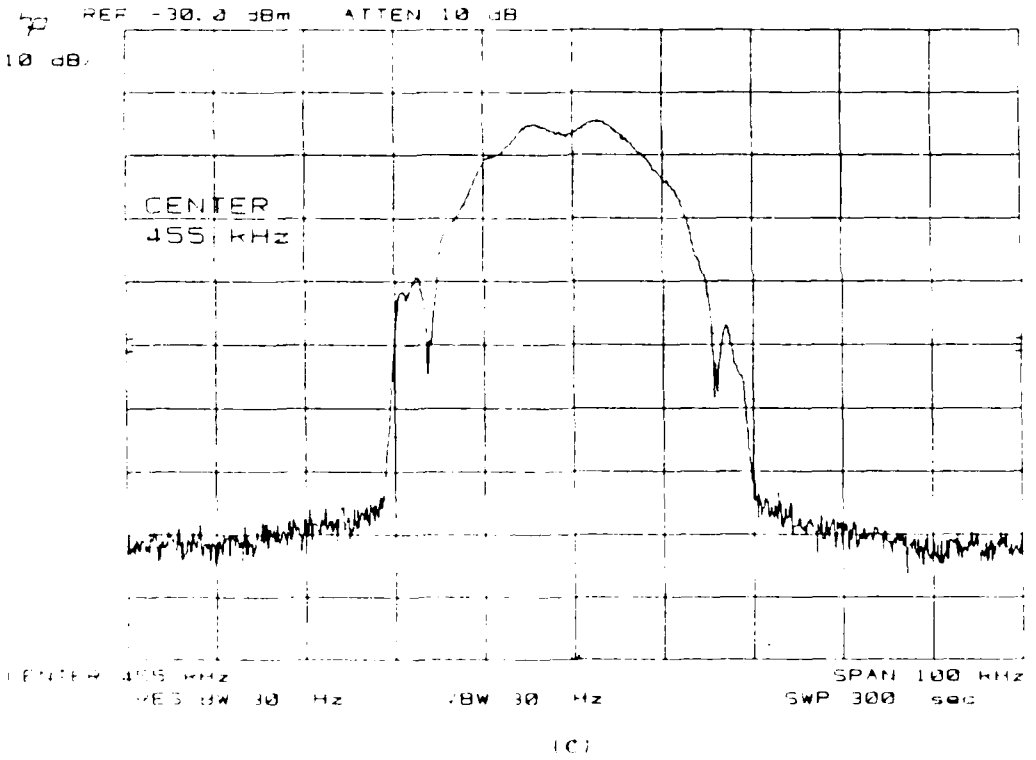
K = constant gain of the IF BPF.

If we use the Rician noise model for a narrow-band process [Ref. 4: pp. 154-156] to express the bandpass noise as

$$n(t) = n_r(t)\cos 2\pi f_o t - n_s(t)\sin 2\pi f_o t$$



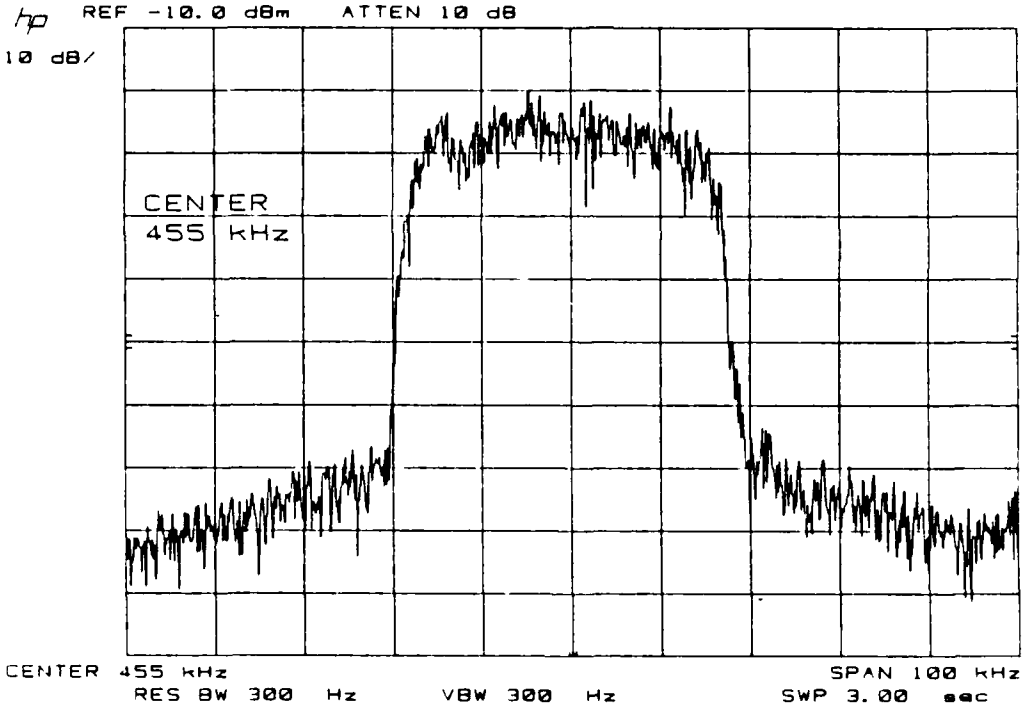
(a) (b)



(c)

Figure 16. Representation of the Filtered Received Signal $r(t)$ (no Data) with no Noise, a) Time Domain (Scales: Horizontal: 5 μsec/div., Vertical: 0.5 V/div.), b) Time Domain (Scales: Horizontal: 2 msec/div. (X10), Vertical: 1 V/div.), c) Envelope of Frequency Spectrum.

(a)



(b)

Figure 17. Representation of the Filtered Received Signal $r(t)$ (no Data) with Noise (SNR = -13 dB), a) Time Domain (Scales: Horizontal; 2 msec/div. (X10), Vertical: 1 V/div.), b) Envelope of Frequency Spectrum.

where the term of interest $n_r(t)$ (in-phase component), plotted in Figure 18, and $n_s(t)$ (quadrature-phase component) are lowpass noise, then

$$v_b(t) = \frac{K}{2}\Big[v_{m_c}(t) + v_{m_c}(t)\cos 4\pi f_o t + n_r(t) + n_r(t)\cos 4\pi f_o t - n_s(t)\sin 4\pi f_o t\Big]. \tag{8}$$

This signal is illustrated in Figure 19 in the time and frequency domain. Figure 19b shows the 910 kHz term as well as a 455 kHz term which is a feed through term resulting from the hardware components. After the LPF, we have

$$v_r(t) + n_r(t) = \frac{K}{2}[v_{m_c}(t) + n_r(t)] \tag{9}$$

which is illustrated in Figure 20 in time and frequency.

The LPF has a gain of 30 dB and a 3 dB cutoff frequency $f_{3\text{dB}} = 22$ kHz. A value $f_{3\text{dB}} >$ chip rate of 16 kHz is used to reduce variations in the amplitude of $v_r(t)$ which occur for different combinations of consecutive chips. The measured in-band amplitude variations of $v_r(t)$ is less than 0.4 dB from 0 to 16 kHz.

2. <u>The Delay-Lock Loop</u>

The DLL synchronizes a local sequence with the received sequence. In the absence of doppler, the rate of the received sequence $v_r(t)$ is $f_r = f_t = 16.000$ Hz. The DLL must first determine the phase of the received sequence (synchronization detection) and then track the received sequence in phase and frequency (code tracking). Code tracking is accomplished by generating an error voltage which adjusts the local clock frequency rate of $f_\ell = 16.000 \pm 10$ Hz to equal $f_r = 16.000$ Hz. This local clock provides timing for a BSG having feedback taps identical to those of the transmitter BSG. The operation of the two different DLL's are described in more detail in the following paragraphs.

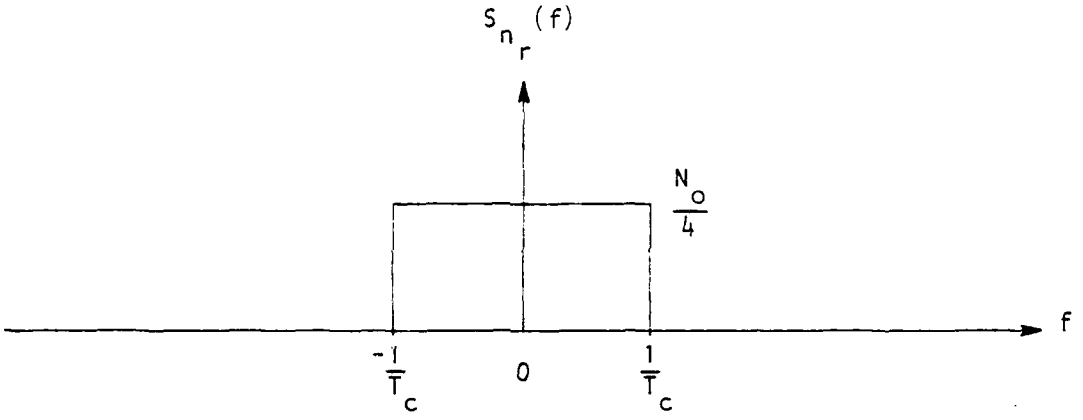
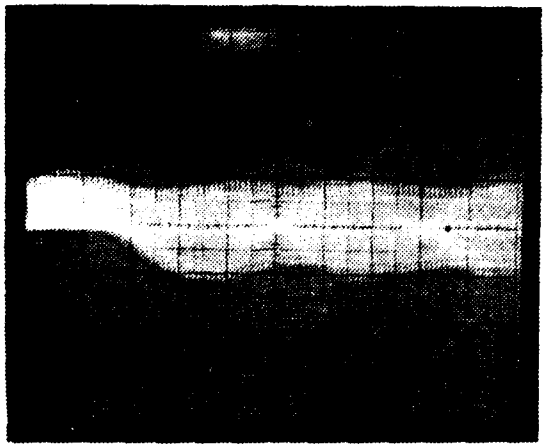
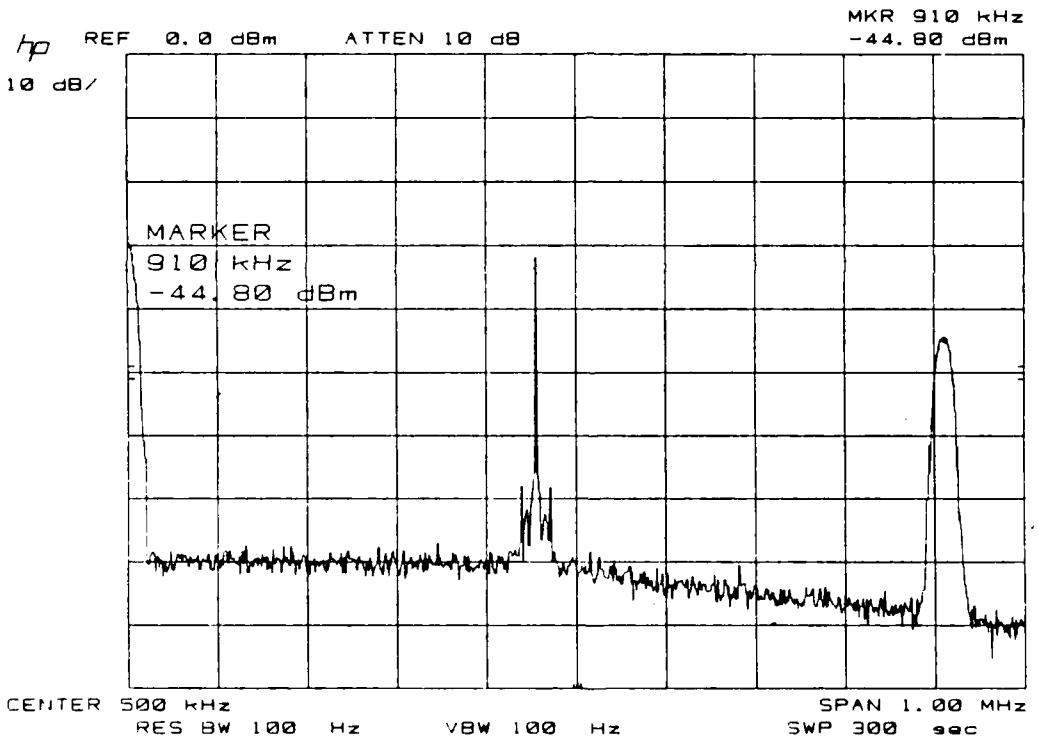


Figure 18. Calculated Power Spectral Density Function of $n_r(t)$.

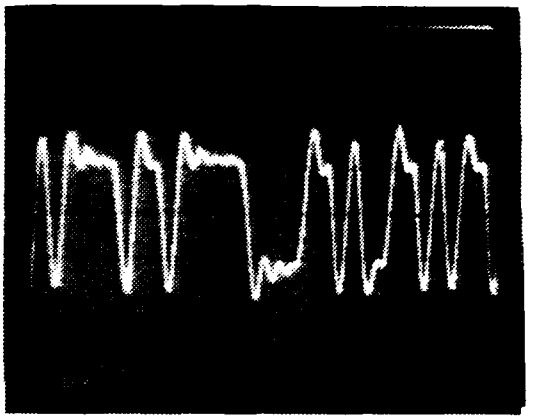


(a)

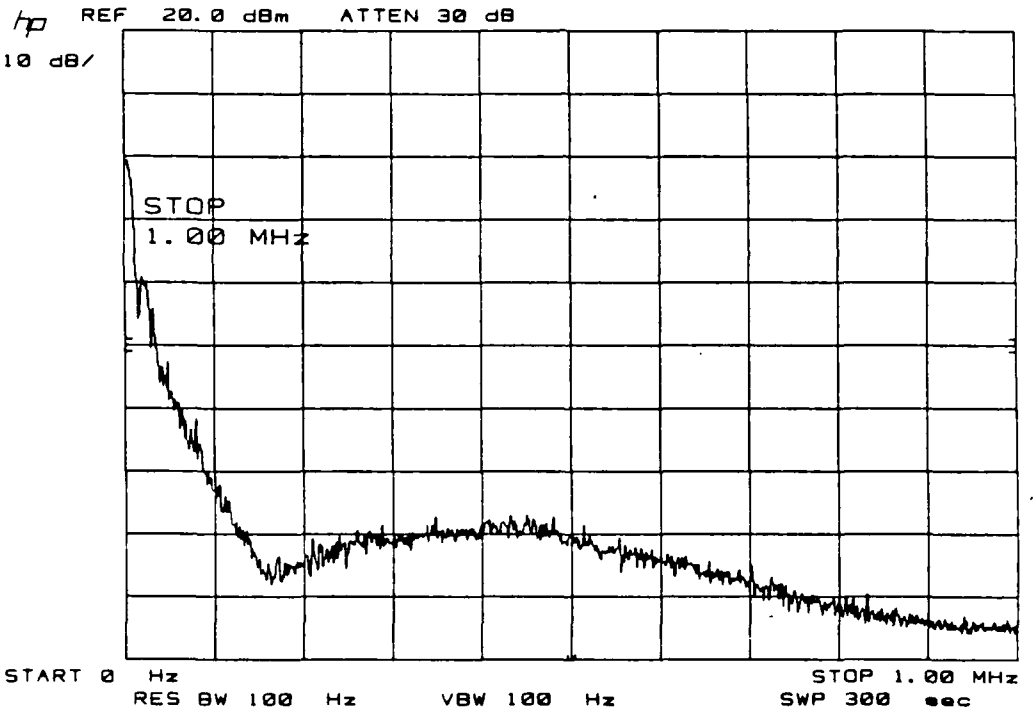


(b)

Figure 19. Representation of the Demodulator Output $v_b(t)$ (no Data and no Noise), a) Time Domain (Scales: Horizontal; 20 μsec/div., Vertical; 0.1 V/div.). b) Envelope of Frequency Spectrum.



(a)



(b)

Figure 20. Representation of the Recovered M-Sequence $v_r(t)$ (no Data and no Noise) After the LPF, a) Time Domain (Scales: Horizontal; 2 μsec/div. (X10). Vertical; 1 V/div.), b) Envelope of Frequency Spectrum.

a. Dual-Channel Delay-Lock Loop Operation

(1) No Data Transmitted. To understand the operation of the DCDLL we first consider a received sequence $v_r(t)$ which is not modulated with data so that $v_{m_c}(t) = v_m(t)$. This type of DLL can be used in systems that transmit a preamble for clock synchronization or provide accurate time/range information. Figure 21 is an illustration of such a DCDLL.

From Figure 21, the received sequence is applied to the delay-lock discriminator where it is simultaneously multiplied by an early version $v_\ell(t+T_c)$ of the locally generated m-sequence and a late version $v_\ell(t-T_c)$ of the m-sequence. The resulting voltages $v_1(t)$ and $v_2(t)$ are then subtracted to produce an error voltage $v_e(t)$. That is,

$$v_e(t) = v_1(t) - v_2(t) \tag{10}$$

where

$$v_1(t) = [v_r(t) + n_r(t)][v_\ell(t+T_c)]$$

$$v_2(t) = [v_r(t) + n_r(t)][v_\ell(t-T_c)].$$

Therefore,

$$v_e(t) = [v_r(t) + n_r(t)][v_\ell(t+T_c) - v_\ell(t-T_c)]. \tag{11}$$

Now if we pass this error signal through an integrating loop filter, essentially a LPF, where the upper limit of integration is determined by the cutoff frequency $f_{3\text{dB}}$ of the filter ($f_{3\text{dB}} = 10$) Hz, we can express the final error signal at the output of the loop filter as

$$v_e'(t) = \int_0^{T_u} v_i(\lambda) v_\ell(\lambda + T_c)\, d\lambda - \int_0^{T_u} v_i(\lambda) v_\ell(\lambda - T_c) d\lambda$$

where

$$v_i(t) = v_r(t) + n_r(t)$$

$$T_u = 1/f_{3\text{dB}} = (1/10) \text{ sec.}$$

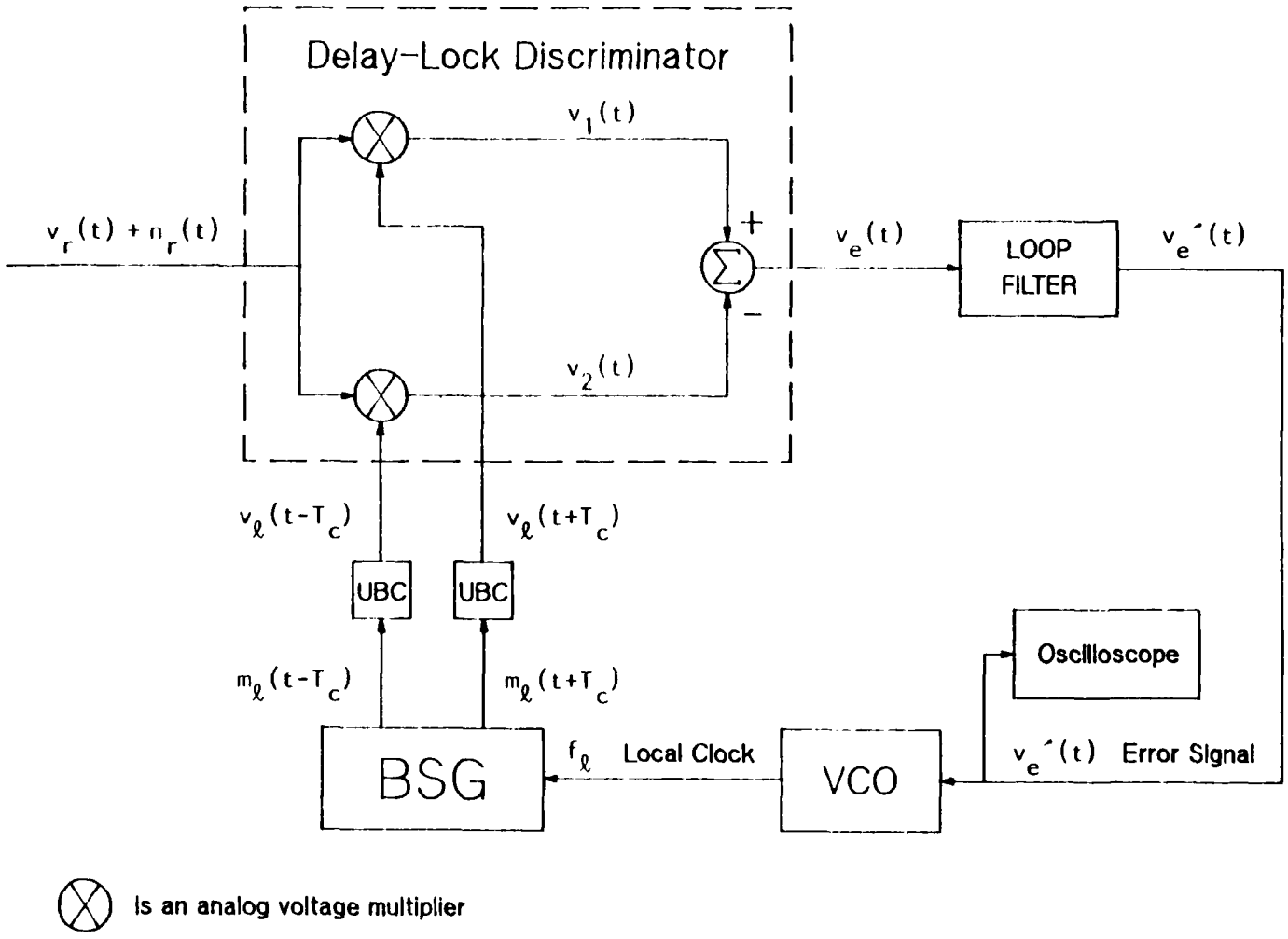


Figure 21. Dual-Channel Delay-Lock Loop Block Diagram (Synchronization Version).

Thus we see the final error signal is the input signal $v_i(t)$ correlated with the late m-sequence $v_\ell(t - T_c)$ and then subtracted from the correlation between the input signal and the early m-sequence $v_\ell(t + T_c)$. When $n(t) = 0$, then $v_e'(t)$ is the ACF of the m-sequence subtracted from another ACF delayed by 2 chip intervals. This signal is illustrated in Figure 22 and can be represented by

$$v_e'(t) = R_{v_m}(\tau + T_c) - R_{v_m}(\tau - T_c).$$

This error voltage is applied to a VCO having a rest frequency $f_\ell = 16,000$ Hz. A typical operating characteristic of the VCO is shown in Figure 23.

Because the loop is a closed feedback system, when the VCO frequency matches that of the received sequence a constant voltage or bias is maintained at the input to the VCO. An interesting characteristic of the error signal can be observed by considering 2 cases: 1) the received sequence rate is less than the local clock rate ($f_\ell > f_r$) and 2) when the received sequence rate is greater than the local clock rate ($f_r > f_\ell$). In Figure 24, when $f_\ell > f_r$ (case I) then the early and late sequences move to the right faster than $v_r(t)$. When $f_r > f_\ell$ (case II), then the early and late sequences move to the left, relative to $v_r(t)$. For case I, the locally generated m-sequence catches up to the received sequence $v_r(t)$ and correlates first with the late sequence $v_\ell(t - T_c)$ and then with the early sequence $v_\ell(t + T_c)$. This is illustrated in Figure 24. When $f_r > f_\ell$ (case II) then the received sequence catches up with the locally generated m-sequence and the early sequence correlates first. Furthermore because the operating characteristic of the VCO has a negative slope, the error signal is inverted such that for case I a positive voltage stable operating point is maintained to slow down the VCO clock rate to match f_r. This is illustrated in Figure 25a where $\tau_\Delta = 1/(f_\ell - f_r)$. For case II, a negative voltage stable operating point is needed to increase the VCO clock rate

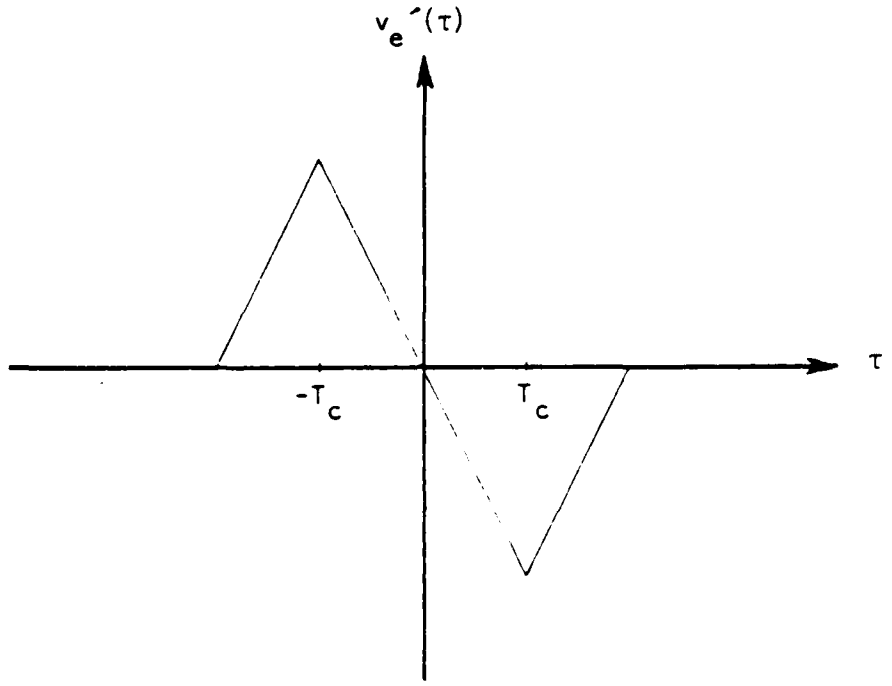


Figure 22. Typical Error Signal Generated by DLL ($f_r > f_\ell$).

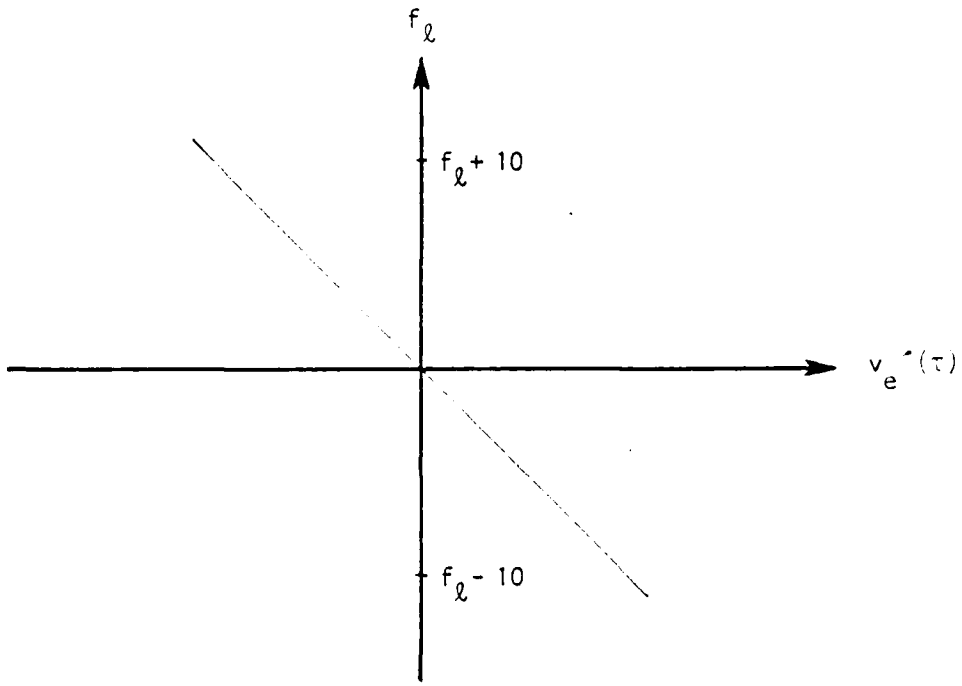


Figure 23. Typical Voltage Controlled Oscillator Operating Characteristics.

to maintain synchronization. See Figure 25b. Figure 26 illustrates the final error voltage $v_e'(t)$ for both open and closed loop conditions and for case I ($f_\ell > f_r$), and case II ($f_r > f_\ell$). For all of these photographs, $f_\ell = 16{,}000$ Hz and $f_r = 15{,}995$ or 16,005 Hz such that $f_\Delta = 1/\tau_\Delta = f_\ell - f_r = \pm\ 5$ Hz.

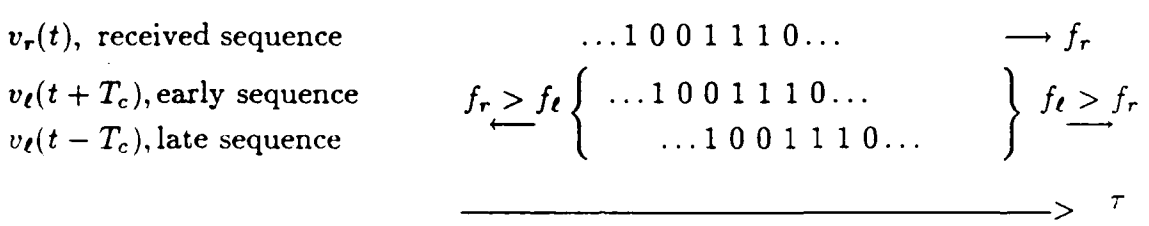


Figure 24. Illustration of Early and Late Correlation.

The VCO produces a square wave clock that is applied to the local BSG. The BSG is identical in design to that in Figure 6. The early sequence is the output of stage 6 and the late sequence is taken from stage 8, 2 chips later. These outputs of the BSG are in unipolar format and are converted to bipolar format by the UBC prior to correlation. See Figure 21.

As a final note, let us consider the noise that will be on the error signal $v_e'(t)$. The amount of noise at the output of the loop filter will limit the achievable noise performance of the loop. If we allow the locally generated sequences to have constant amplitude values $\pm A_\ell$ volts, then the noise component of $v_1(t)$ is $\pm A_\ell n_r(t)$; similarly for $v_2(t)$. Thus, the noise component of $v_e(t)$ has three possible values at any one time: $+2A_\ell n_r(t)$, $-2A_\ell n_r(t)$, and 0 volts. Ideally we would like the transmitter clock rate to be very close to the receiver clock rate so that the DLL can operate around its rest frequency. This requires near zero correlation of $v_\ell(t + T_c)$ and $v_\ell(t - T_c)$. Since all four values of the early and late binary sequences are equiprobable, the noise components of $v_e'(t)$ are,

$+2A_\ell n_r(t), -2A_\ell n_r(t)$, and 0 volts, and these values occur with probability 1/4, 1/4, and 1/2, respectively. Therefore, the average noise value of $v_e'(t)$ is zero, and the average noise power of $v_e'(t)$ is $2A_\ell^2\overline{n_r^2(t)} = 2A_\ell^2\sigma^2$. Now if we assume the received sequence $v_r(t)$ has constant amplitude values of $\pm A_r$ volts, then by the same process we determine that the signal components of $v_e'(t)$ have average power $2A_r^2A_\ell^2$. A measure of quality of $v_e'(t)$ is the SNR and can be expressed as

$$\text{SNR} = \frac{2A_r^2A_\ell^2}{2A_\ell^2\sigma^2} = \frac{A_r^2}{\sigma^2}.$$

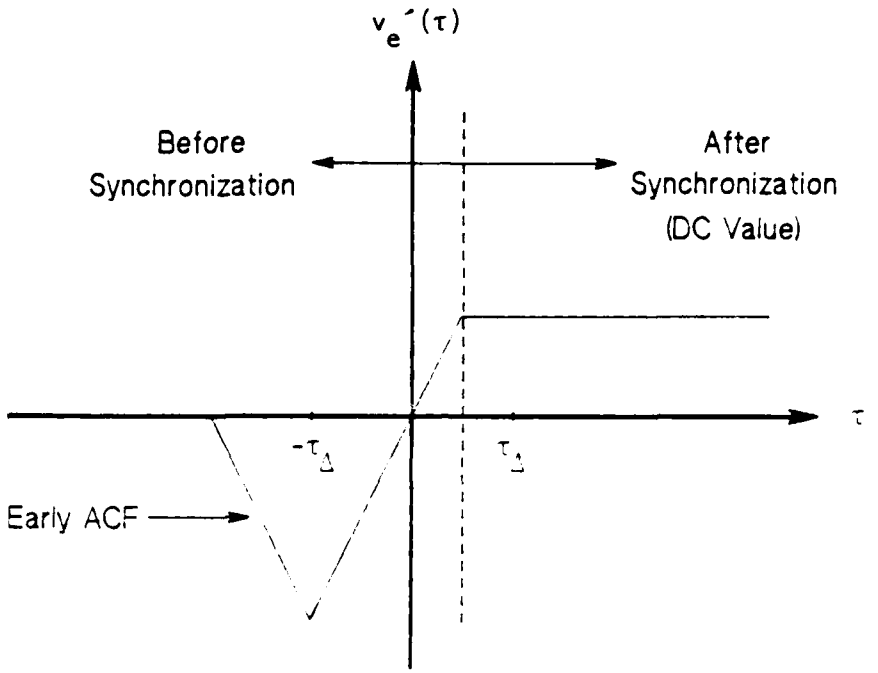
It should be noted that the DLL input SNR is also A^2/σ^2; hence, the delay-lock discriminator provides no improvement in SNR.

(2) Operation with Data (Synchronization and Data Version). If we now allow the received sequence $v_r(t)$ to be modulated with data such that there are inversions in the sequence, i.e., the switch in Figure 5 is back to the $d(t)$ position, we must now modify the delay-lock discriminator of Figure 21 to be that in Figure 27.

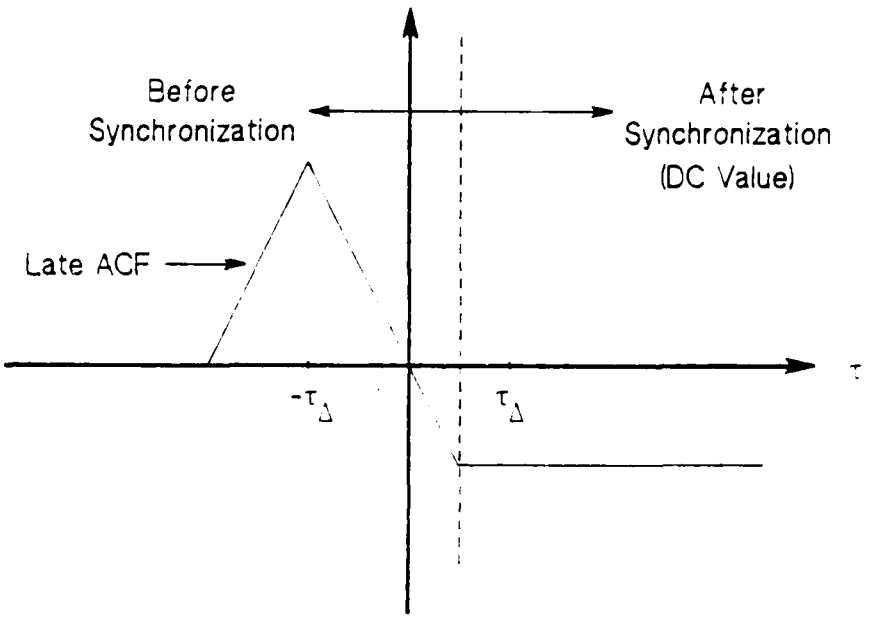
It should be emphasized that the DCDLL function has not changed: it still must provide synchronization, but it will not demodulate the actual data. The correlation operation is now performed within the delay-lock discriminator prior to the summing junction in each channel of the DCDLL. Considering just the early channel, we see that the input signal $v_r(t) + n_r(t)$ is multiplied by the locally generated m-sequence $v_\ell(t + T_c)$ to produce $v_1(t)$, which is integrated via a LPF. This correlation operation can be expressed as

$$v_1(t) = \int_0^{T_u} [v_r(t) + n_r(t)][v_\ell(t + T_c)]dt.$$

The upper limit of integration is set equal to the reciprocal of the cutoff frequency of the LPF which is equal to the data bit rate ($T_u = 1/f_{3\text{dB}} = 1/R_d = (1/62.75)$



(a)



(b)

Figure 25. Illustration of the Two Cases Which Produce a Stable Operating Point for the VCO, a) $f_\ell > f_r$, and b) $f_r > f_\ell$.

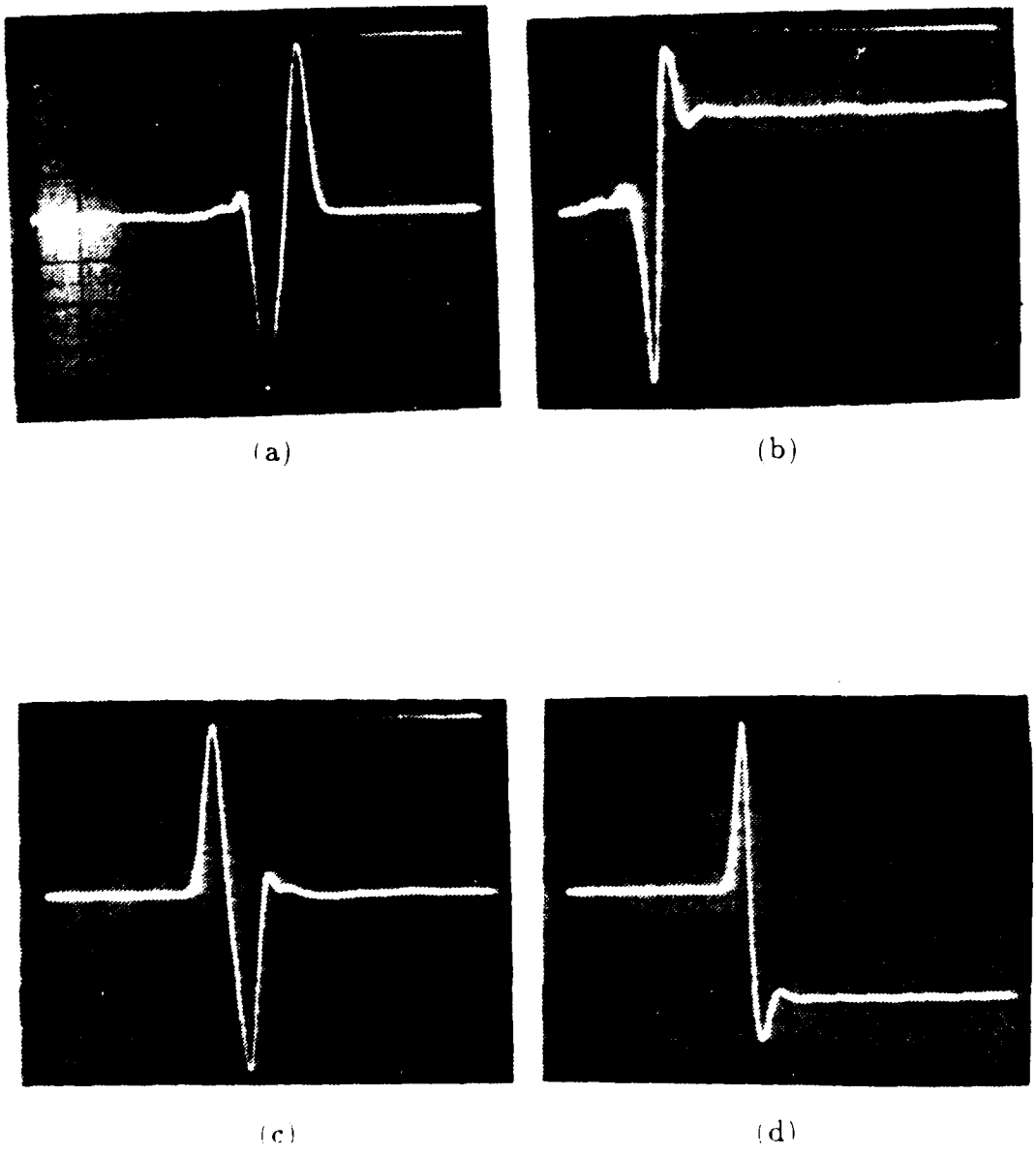


Figure 26. Error Voltage $v_e'(t)$ for DCDLL (no Data) for a) Case I ($f_\ell > f_r$) Open Loop, b) Case I Closed Loop, c) Case II ($f_r > f_\ell$) Open Loop,) Case II Closed Loop, (Scales: Horizontal: 0.5 sec/div., Vertical: 0.2 V/div.), Storage: On.

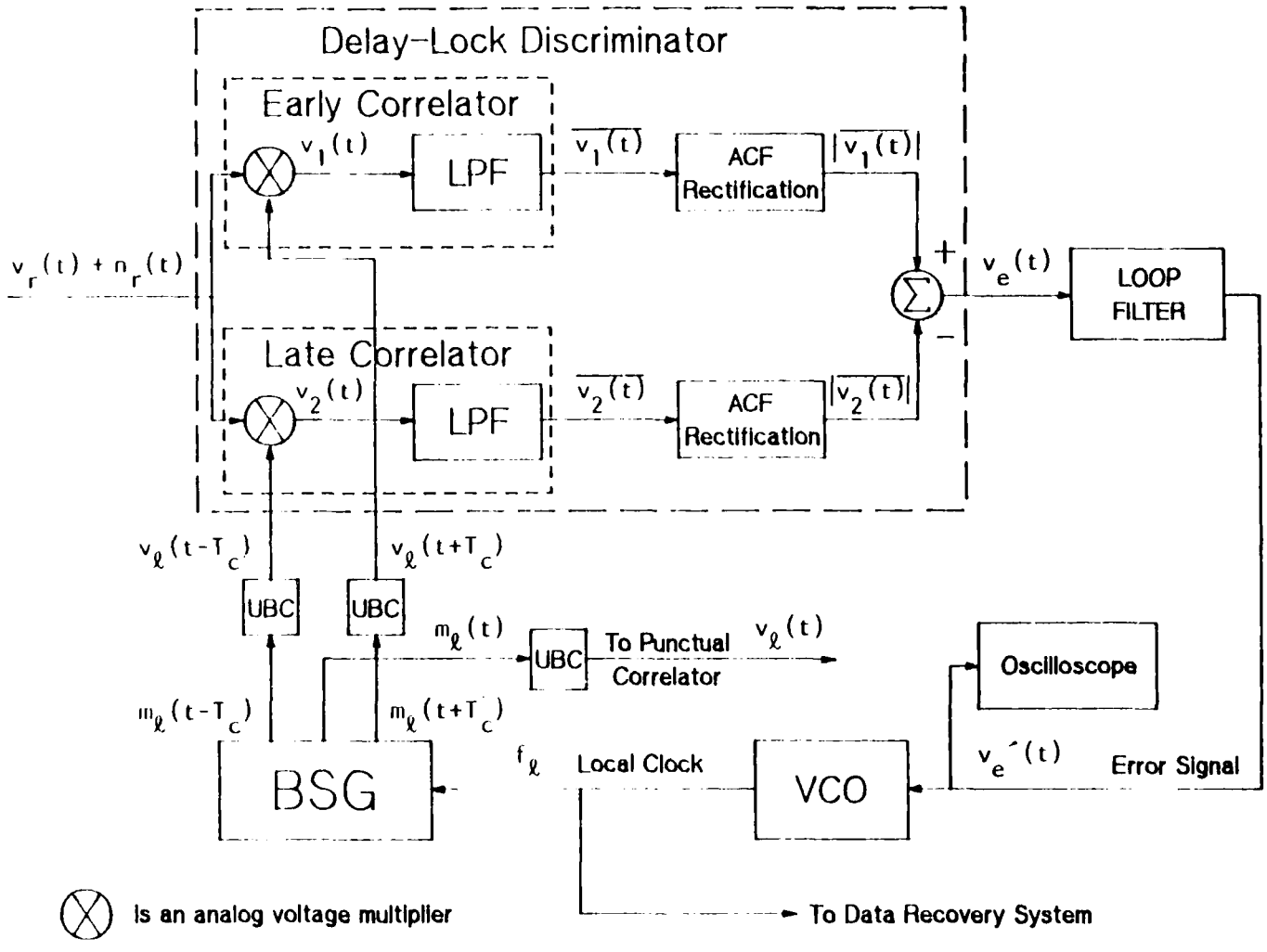


Figure 27. Dual-Channel Delay-Lock Loop Block Diagram (Synchronization and Data Version).

sec. Because of the data transitions there are polarity inversions of the ACF at the output of the LPF which need to be eliminated (rectified) for code tracking purposes. Recall that Figure 2 illustrates the ACF of an m-sequence (with no data inversions). When the m-sequence is modulated with data, random inversions of the ACF result in positive and negative voltage values (correlations) as illustrated in Figure 28a. The output of the ACF rectification circuit produces the absolute value of the input as displayed in Figure 28b. Once rectified, the signals in each channel are subtracted, then passed through the loop filter to reduce the signal bandwidth to 10 Hz. It should be noted that the correlator LPF BW should be greater than or equal to the data bit rate to allow effective ACF rectification while the loop LPF BW determines the maximum passing rate that the loop can accommodate (obtain lock). It should also be noted that some systems use envelope detectors [Ref. 2: p. 253] or squaring devices [Ref. 1: p. 434] to obtain this ACF rectification.

There is switching of the signal caused by data in each channel of the DCDLL. The cutoff frequency of the integrating data LPF is such that a sinusoidal (not a square wave) signal is passed. Therefore, after rectification, there is "self-made" noise in the final error signal $v_e'(t)$. Figure 29 illustrates the error signal for both open and closed loop conditions and for case I ($f_\ell > f_r$), and case II ($f_r > f_\ell$). For these photographs $f_\Delta = \pm 5$ Hz as before. Note that for the closed loop condition, there is slightly more ripple after lock because the time delay through the loop has increased, thus decreasing the time response of the loop.

The DCDLL will now provide a synchronous clock and locally generated m-sequence $v_\ell(t)$ that when synchronized is in phase ($\pm T_c$) with and equal in frequency to the sequence that is received by the data recovery system, as shown in Figure 27.

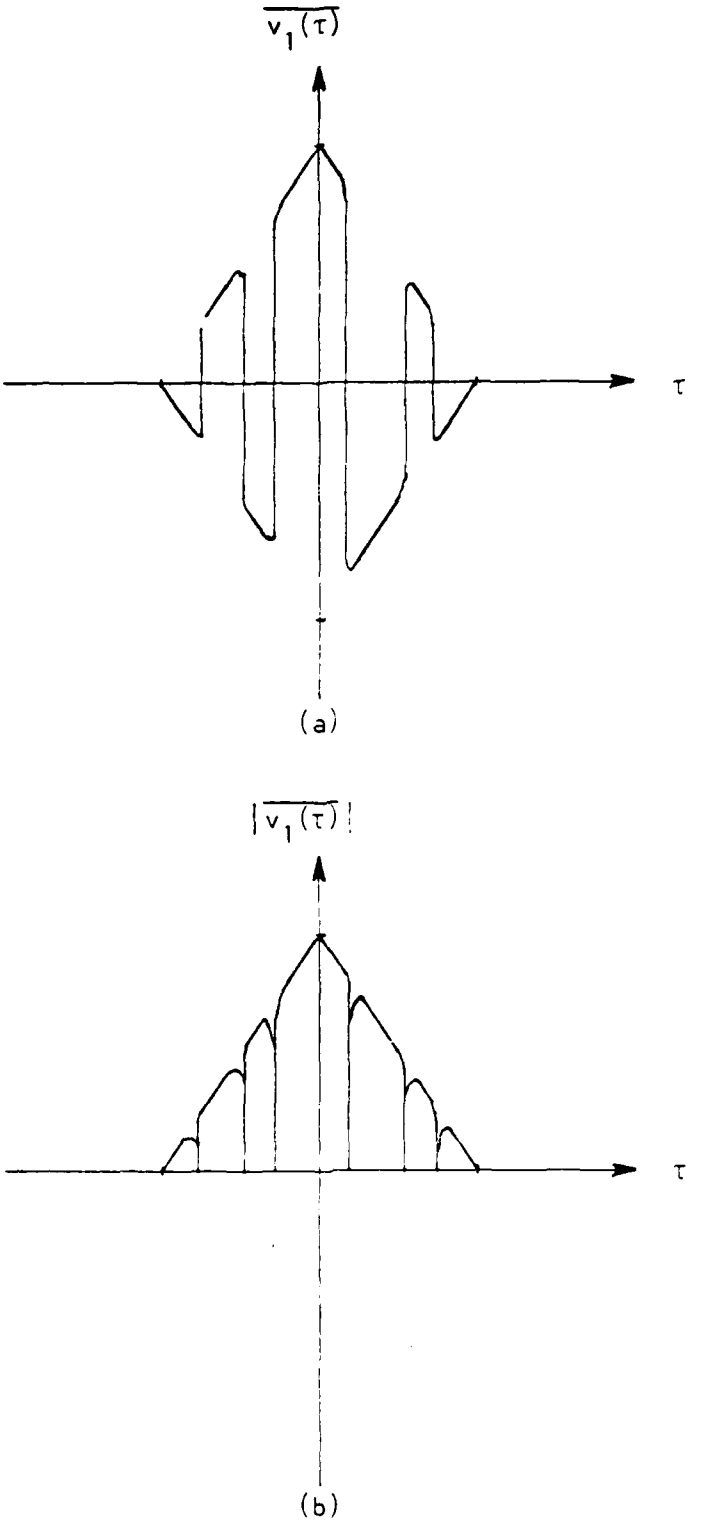
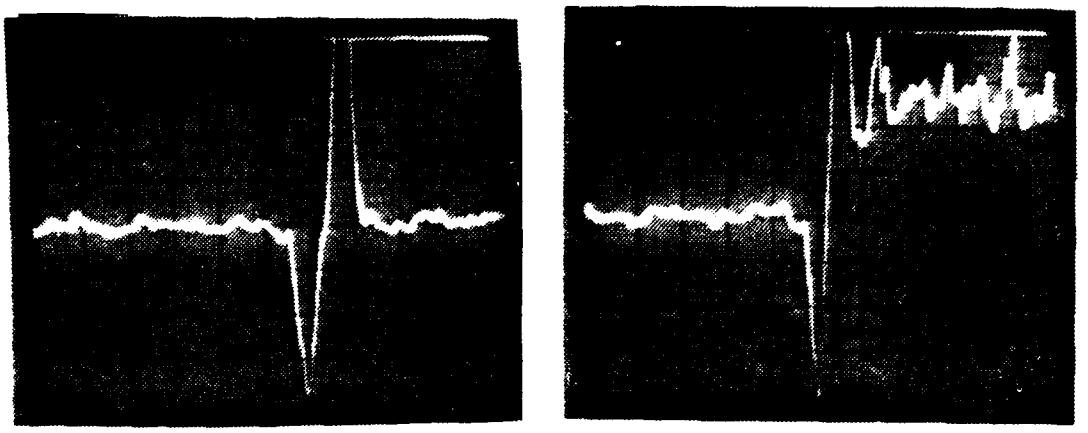
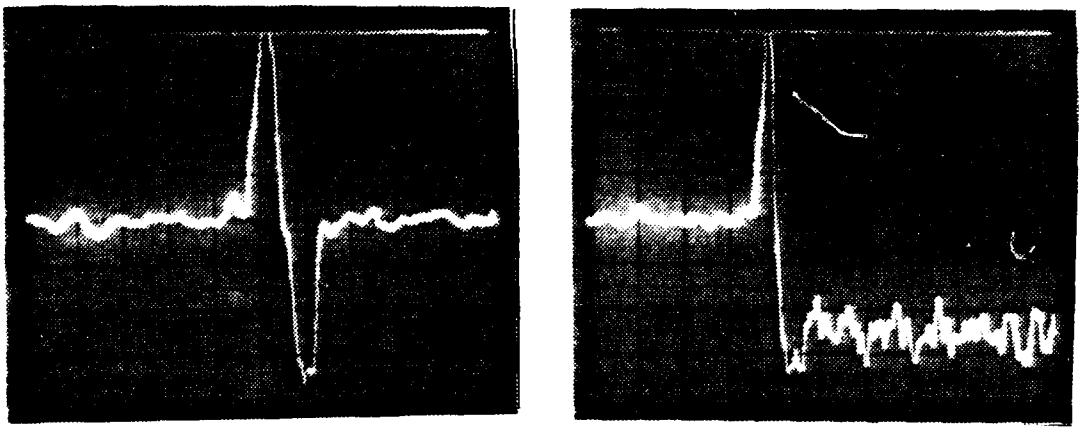


Figure 28. Illustration of Effects on ACF by Randomly Modulated Data Embedded in the Received Sequence, a) Input to ACF Rectification Circuit, and b) Output.



(a) (b)



(c) (d)

Figure 29. Error Voltage $v_e'(t)$ for DCDLL (with Data) for a) Case I ($f_\ell > f_r$) Open Loop, b) Case I Closed Loop, c) Case II ($f_r > f_\ell$) Open Loop, d) Case II Closed Loop, (Scales: Horizontal; 0.5 sec/div., Vertical; 0.2 V/div.), Storage: On.

b. Single-Channel Delay-Lock Loop (Synchronization Version)

In equation (11) we expressed the error voltage $v_e(t)$ that is generated by the dual-channel delay-lock discriminator as

$$\begin{aligned} v_e(t) &= [v_r(t) + n_r(t)][v_\ell(t + T_c) - v_\ell(t - T_c)] \\ &= v_i(t) \cdot v_{mm}(t). \end{aligned}$$

This equation suggests that we can realize a single channel (one multiplier) version of the delay-lock discriminator by first subtracting the two locally generated m-sequences to generate a three-level difference voltage $v_{mm}(t)$ and then multiply it by the input voltage $v_i(t)$. The SCDLL is illustrated in Figure 30 and a photograph of the three-level voltage $v_{mm}(t)$ is shown in Figure 31a. Because this sequence is created by subtracting two bipolar sequences (each of amplitude $\pm$ 1 volt) delayed by 2 chips it is in modified duobinary format [Ref. 5: p. 111]. The spectrum still has 255 discrete line components from 0 to 16 kHz as illustrated in Figure 30b, but its spectrum consists of lobes separated by 16 kHz and has no DC component. See Figure 31c. The final error signal $v_e'(t)$ produced by the SCDLL is theoretically the same as that generated by the DCDLL (synchronization version) and is essentially the same as that illustrated in Figure 26.

As noted earlier, the noise present on this error signal will limit the noise performance of the loop. Let us consider the noise that will be present on the error signal $v_e'(t)$ for the SCDLL. The locally generated three-level voltage $v_{mm}(t)$ will have constant amplitude values of $+2A_\ell$, $-2A_\ell$, and 0 volts each with probabilities 1/4, 1/4, and 1/2, respectively. Therefore the average noise value of $v_e'(t)$ is once again zero and the average noise power is $4A_\ell^2\overline{n_r^2(t)}$. Now the signal component of $v_e'(t)$ has average power $4A_\ell^2A_r^2$ so the SNR at the output of the loop filter has not improved, in theory. It should be noted, however, that

if there is any gain and/or delay mismatch between the early and late channels within the DCDLL, then the $+2A_\ell n_r(t)$ and $-2A_\ell n_r(t)$ terms, each occurring with probability 1/4, may not on the average cancel exactly. The SCDLL does not rely on the cancellation of these noise components.

It should be noted that if the received binary sequence is modulated (inverted) with data, then the SCDLL will not achieve lock, whereas the modified version of the DCDLL (synchronization and data version) can. So, the application of the SCDLL is limited to systems which are concerned only with accurate time/range information or systems which transmit preambles for clock synchronization.

3. Data Recovery System

The baseband received sequence plus noise, $v_r(t) + n_r(t)$, is applied to the punctual correlator while the locally generated sequence $v_\ell(t)$ is provided by the DCDLL as illustrated in Figure 32. The received sequence is despread by a correlation operation similar to the correlation performed in each channel of the DCDLL except an integrate and dump matched filter is used instead of just a LPF. This operation is called punctual correlation because the received sequence $v_r(t)$ is aligned (not retarded or advanced) with the locally generated punctual sequence $v_\ell(t)$. The output $v_4(t)$ of the punctual AVM is illustrated in Figure 33a.

As depicted in Figure 25, the early or late channel ACF will always peak at $\pm\tau_\Delta$ depending on the relative rates between the received sequence and the local sequences; thus the punctual correlator output will always peak directly between these two peaks or at zero delay between $v_m(t)$ and $v_\ell(t)$. As demonstrated earlier, positive and negative values of correlation will occur due to the random data inversion of the transmitted sequence $v_{m_c}(t)$. For a data pulse of duration $T_b = 15.94$ msec, the integrate and dump circuit will integrate over this bit time and will reach

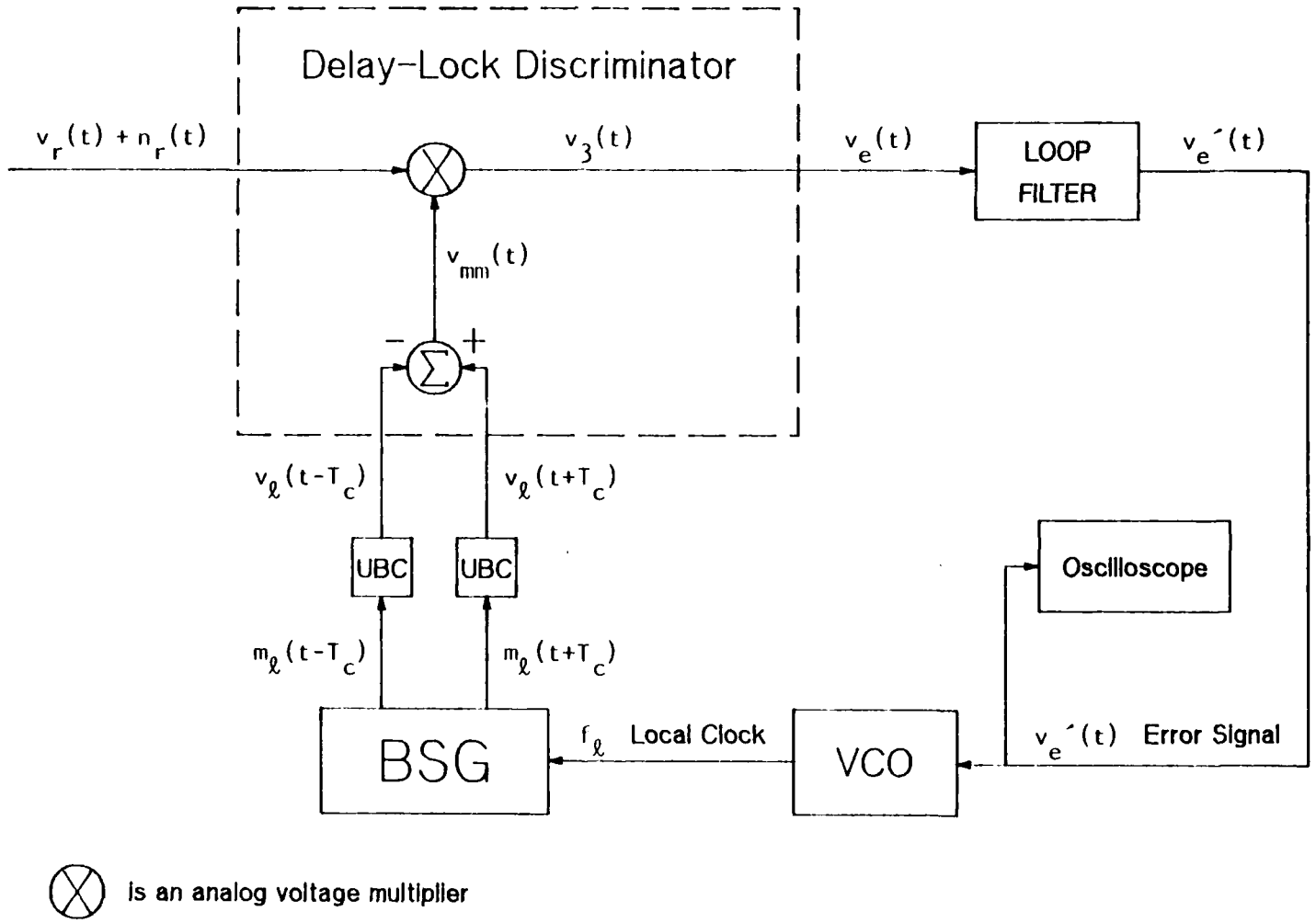
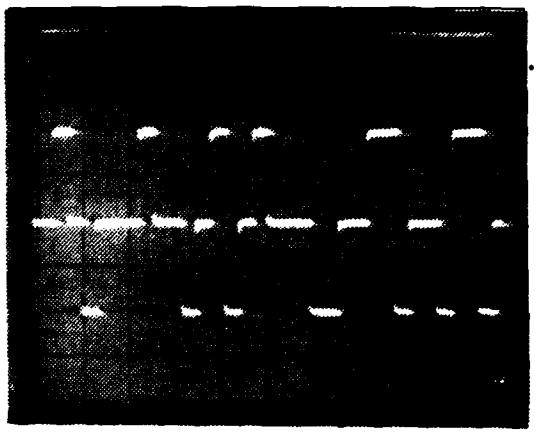
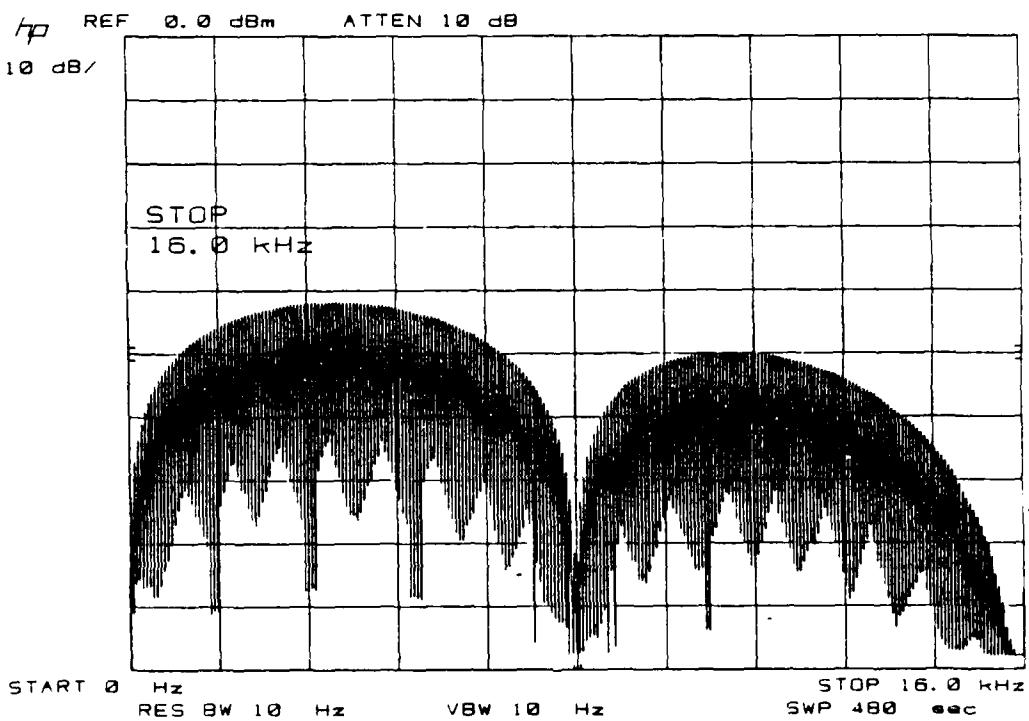


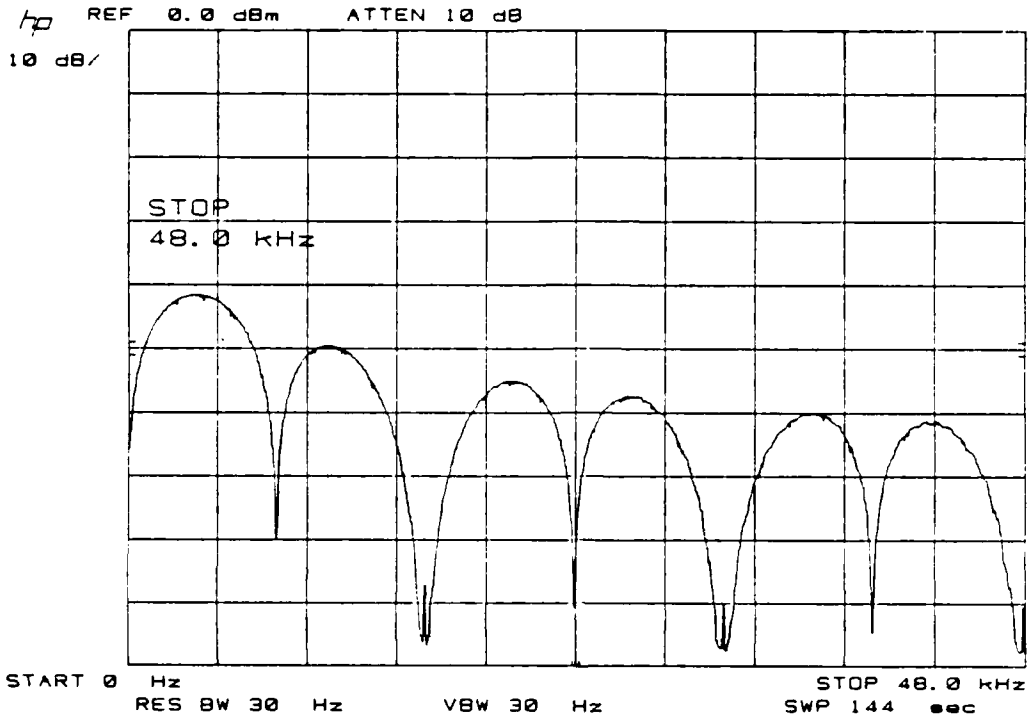
Figure 30. Single-Channel Delay-Lock Loop Block Diagram (Synchronization Version).



(a)


REF 0.0 dBm
ATTEN 10 dB
10 dB/
STOP
16.0 kHz
START 0 Hz
STOP 16.0 kHz
RES BW 10 Hz
VBW 10 Hz
SWP 480 sec

(b)



(c)

Figure 31. Representation of the Three-Level Sequence $v_{mm}(t)$ Used in the SCDLL. a) Time Domain (Scales: Horizontal: 2 msec/div. (X10), Vertical: 1 V /div.), b) Frequency Domain (0 to 16 kHz), c) Envelope of Frequency Domain (0 to 48 kHz).

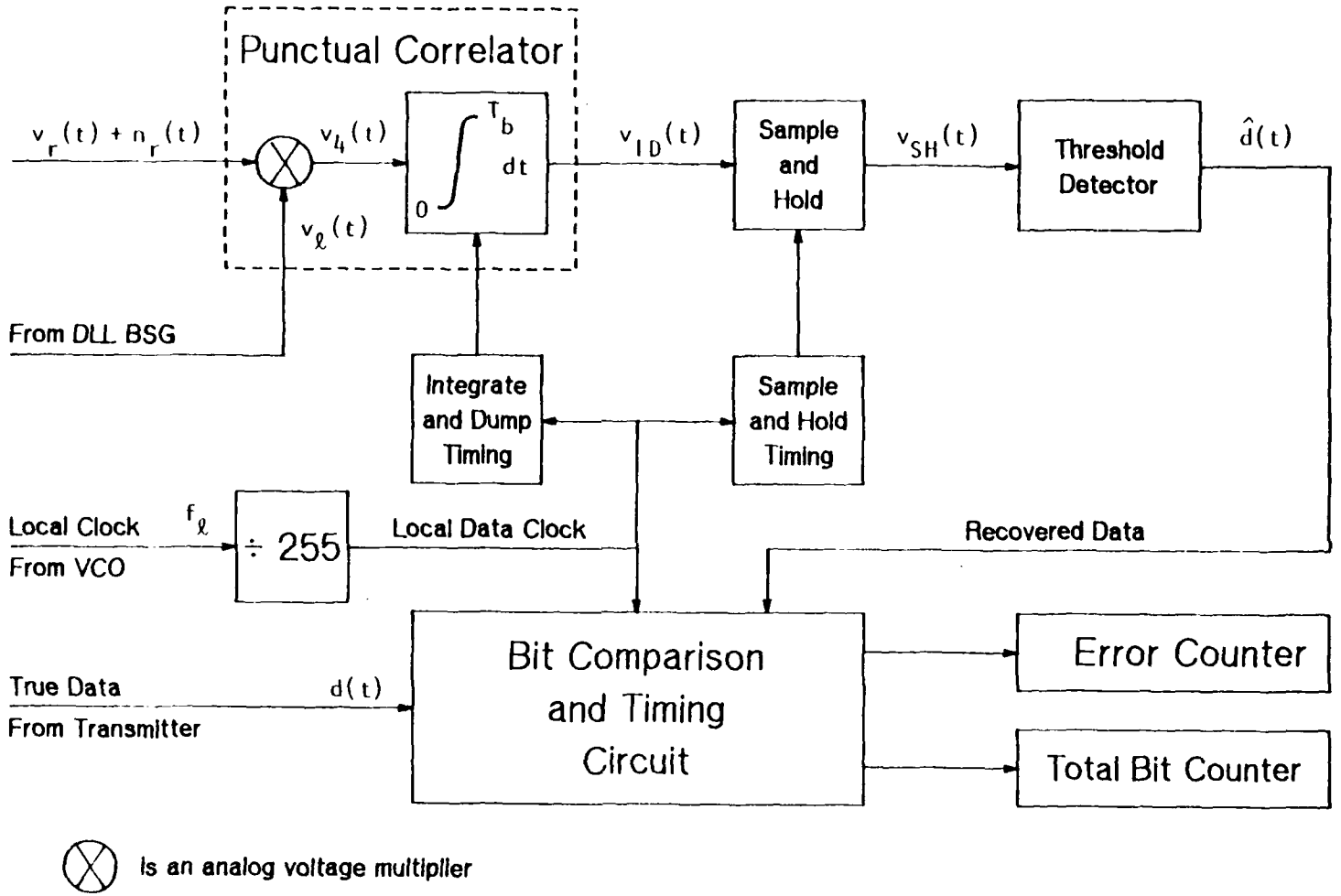


Figure 32. Punctual Correlator (Matched Filter), Data Bit Recovery and Timing General Block Diagram.

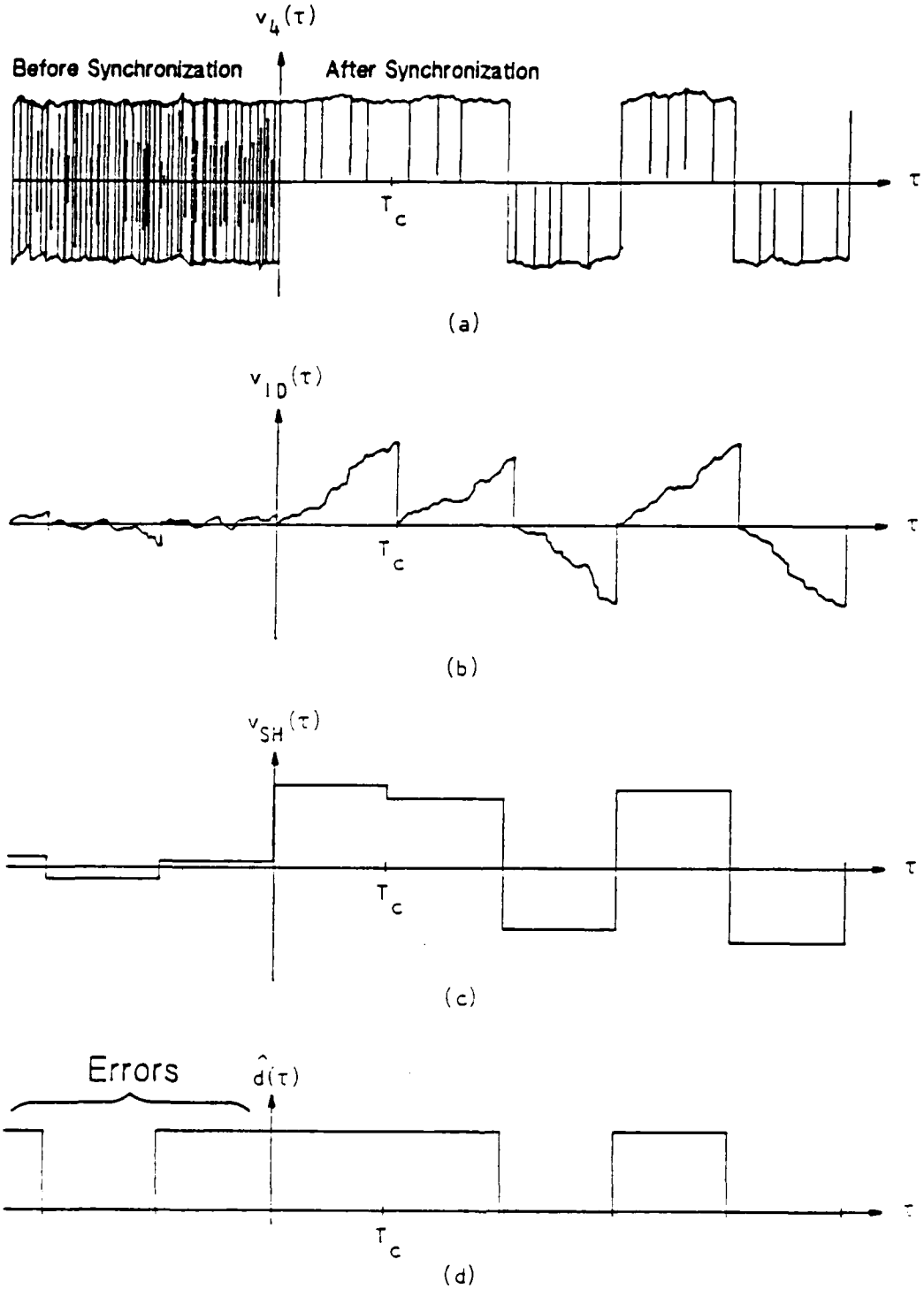


Figure 33. Illustration of Signal Outputs within the Data Recovery System of a) Analog Voltage Multiplier, b) Integrate and Dump, c) Sample and Hold, and d) Threshold Detector.

a maximum value at the end of the bit interval. At the end of this time, the output of the integrator $v_{\mathrm{ID}}(t)$ in Figure 33b is sampled just before the signal is dumped and held for one bit interval by the sample and hold circuit as shown in Figure 33c; Figure 34 illustrates the timing of this procedure. The varying amplitude bipolar bit stream $v_{\mathrm{SH}}(t)$ is then applied to a zero-crossing threshold detector to produce a unipolar estimate of the original pseudorandom data bit stream $\hat{d}(t)$ as shown in Figure 33d. The threshold of the detector is set equal to zero because Pr(data 1) = Pr(data 0) = 1/2 [Ref. 4: p. 326]. Figure 35 shows photographs of $v_4(t)$, $v_{\mathrm{ID}}(t)$, and $v_{\mathrm{SH}}(t)$ without noise and when SNR = -13 dB.

The recovered data $\hat{d}(t)$ is now compared with the original pseudorandom data bit stream $d(t)$. The timing is such that these bit streams are compared in the middle of the data bit interval ($T_b/2$) to avoid edge effects. See Figure 34. The outputs of the bit comparison and timing circuitry go to two separate counters as illustrated in Figure 31.

The ratio of the counts on each counter provides the measured BER = P_e. Because our system utilizes coherent BPSK modulation and matched filter data bit detection, an expression for probability of bit error is the same as for an optimum binary receiver. The derivation of the probability of error expression is well known and can be written for equal energy, equiprobable signals as

$$P_e = 1/2\mathrm{erfc}\left(\sqrt{E_b/N_o}\right) = 1/2\mathrm{erfc}\left(\sqrt{2\mathrm{SNR}}\right) \tag{12}$$

where erfc is the complementary error function [Ref. 5: pp. 402- 404].

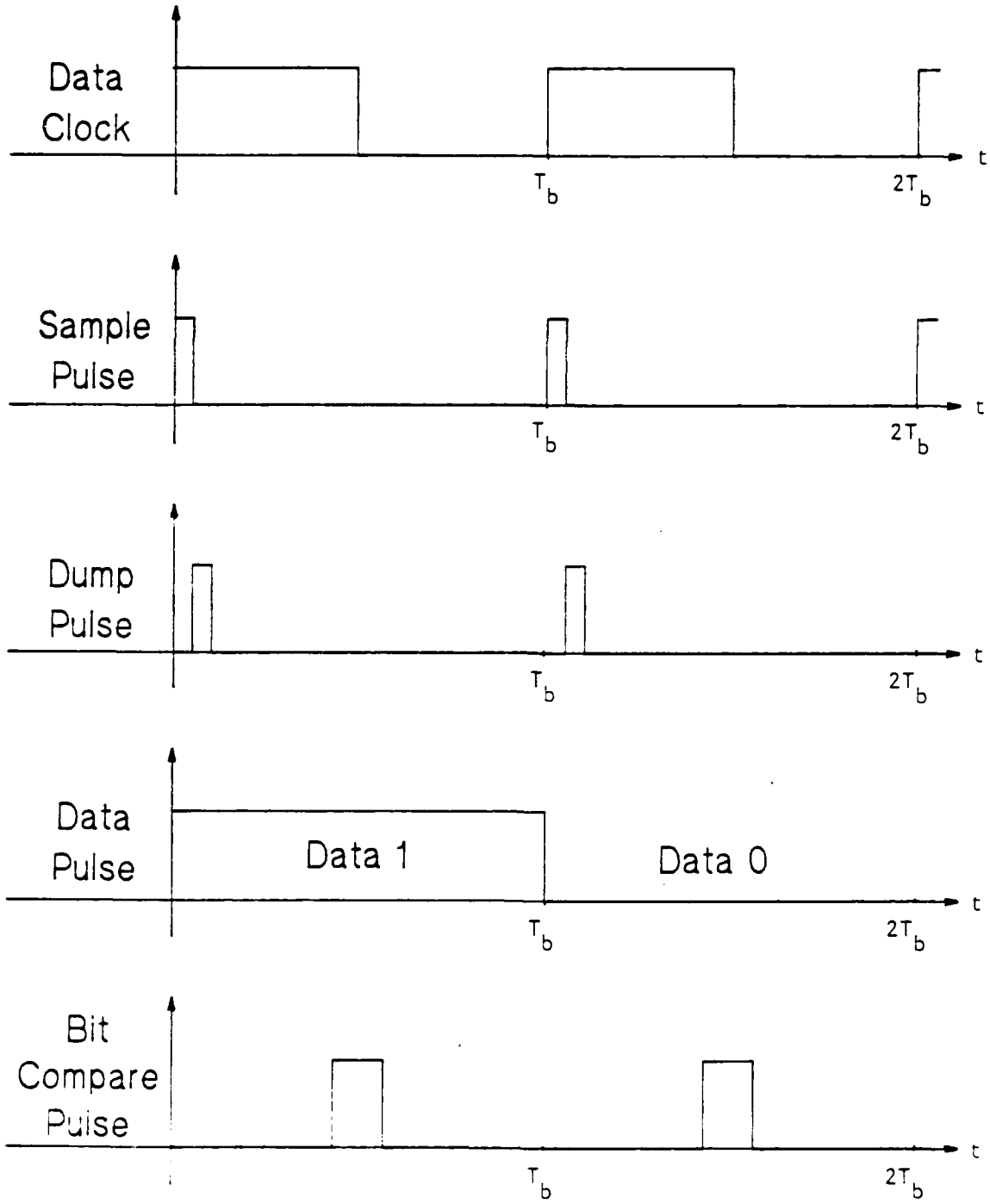


Figure 34. Timing Diagram Illustrating Sample, Dump, and Bit Compare Pulses.

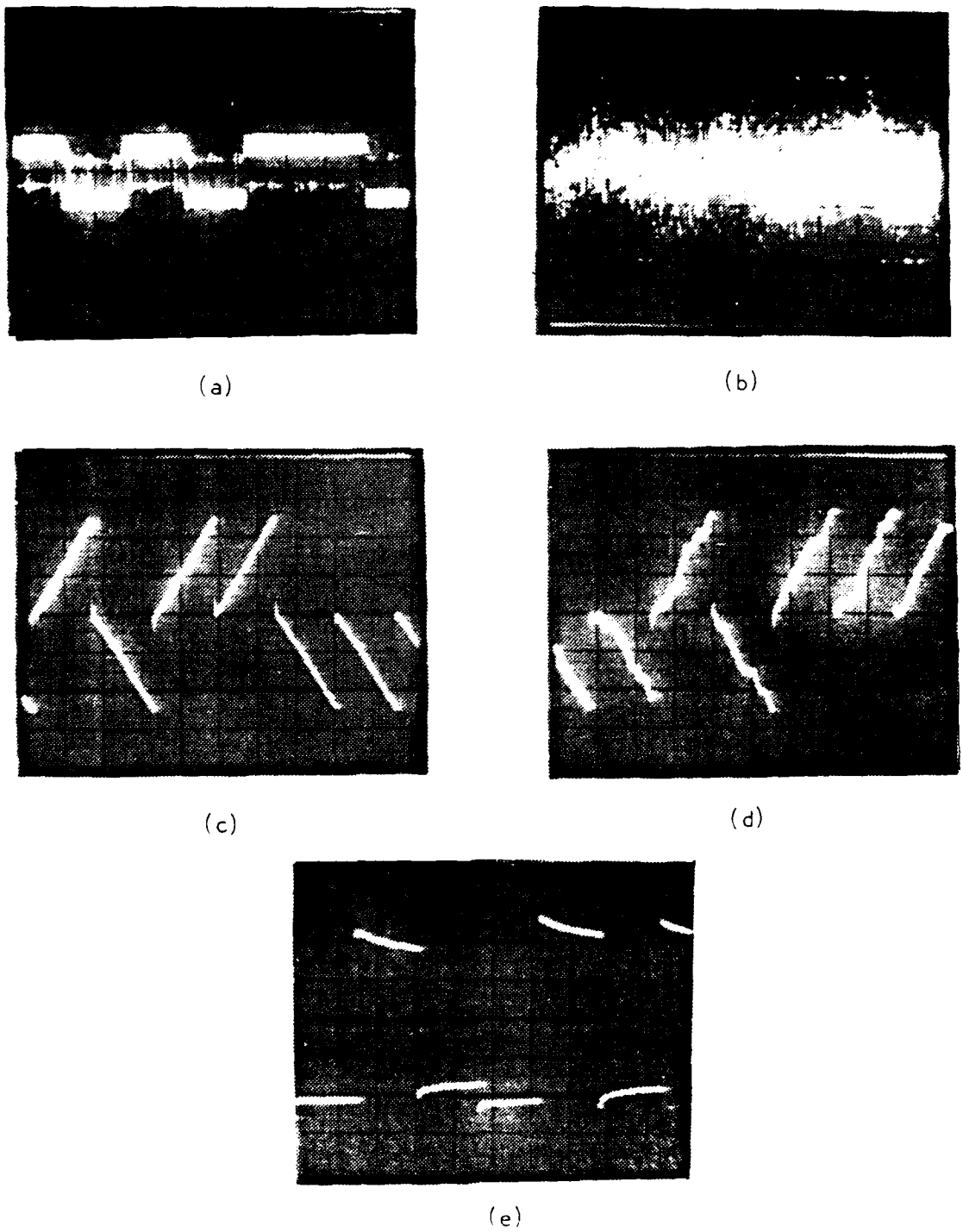


Figure 35. Time Domain Representation of a) Output of Punctual AVM $v_4(t)$ (no Noise), b) $v_4(t)$ (SNR = −13 dB), c) Output of the Integrate and Dump $v_{ID}(t)$ (no Noise), d) $v_{ID}(t)$ (SNR = −13 dB), e) Output of the Sample and Hold $v_{SH}(t)$ (SNR = −13 dB). (Scales: Horizontal: 10 msec/div., Vertical: 2 V/div.).

IV. DETAILED HARDWARE DESIGN, CONSTRUCTION, AND OPERATION

This chapter presents the design of the DS spread spectrum transmitter, channel, and receiver. Detailed circuit diagrams including component values, and circuit performance characteristics are provided. All diodes are model 1N914B; all resistor values are in kΩ; all capacitor values are in μF; all digital chip power supplies are 0, +5 volts, and all linear chip power supplies are ±15 volts unless otherwise specified. Off-the-shelf components are used throughout.

A. TRANSMITTER SUBSYSTEM

1. Binary Sequence Generator Circuit

Generation of the unipolar m-sequence $m(t)$ is accomplished by using a TTL clock (Wavetek Model 145 Function Generator), an 8-bit serial in, parallel out shift register (74164), 3 XNOR gates (3/4 74135) and an 8-input NAND (7430) gate. Figure 35 illustrates the BSG with feedback [8,4,3,2] from the Q_H, Q_D, Q_C, and Q_B taps, respectively. The 7430 is needed to prevent the FSR from staying in the all 1's state. Should for some reason the all 1's state occur, all other timing circuits, as well as the BSG, must be cleared (divide-by-255 and data register).

2. Divide-by-255 Circuit

The divide-by-255 circuit detailed in Figure 36 utilizes two 4-bit binary counters (54161). When the first counter (C1) reaches a divide by $2^4 = 16$ state, it enables the second counter (C2) to reach a $2^8 = 256$ count. This all 1's state is then detected by the 7430 8-input NAND gate. The NAND gate then loads the counters with the state 0000 0001. Thus, the all 0's state is avoided which produces

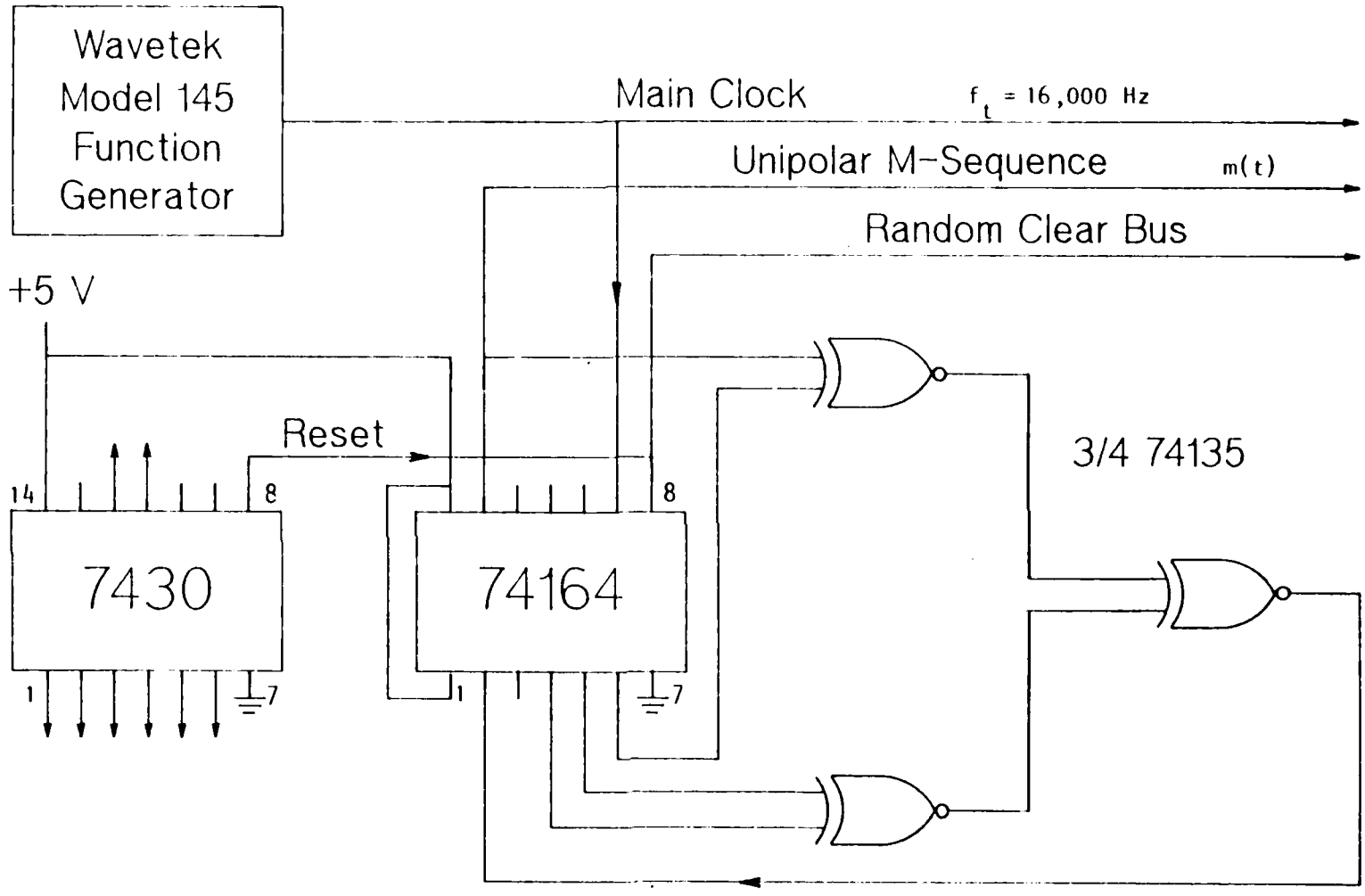


Figure 35. 8-Bit Maximal Length Binary Sequence Generator with Feedback Connections [8,4,3,2] Used for Spreading.

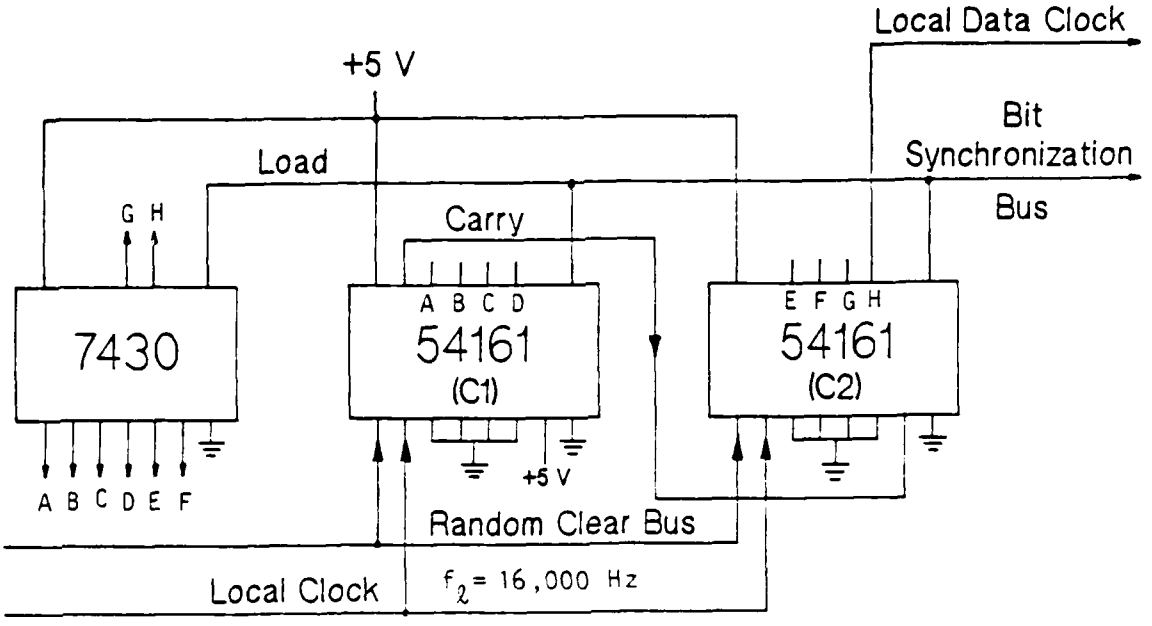


Figure 36. Divide-by-255 Counter Circuit.

a divide-by-255 count. The output is a TTL compatible data clock which is applied to the data generator.

3. Data Generator Circuit

Figure 37 illustrates the data generator circuit which is the same design as the BSG except the clock is provided by the divide-by-255 circuit and the feedback taps [8,5,3,1] are taken from Q_H, Q_E, Q_C, and Q_A respectively. The data bits are taken from stage 6 (Q_F). Delayed bits are used by the bit error measurement circuitry which are taken from stage 8. This 2 bit delay is necessary because the sample and hold introduces a 1 bit delay and a flip flop in the receiver creates another 1 bit delay; the data bit recovery circuitry is presented in Section 6. b.

4. Carrier Modulation Circuit

Prior to carrier modulation, the unipolar m-sequence $m(t)$ and the unipolar data bit stream $d(t)$ are combined by an XNOR (1/4 74135) as shown in Figure

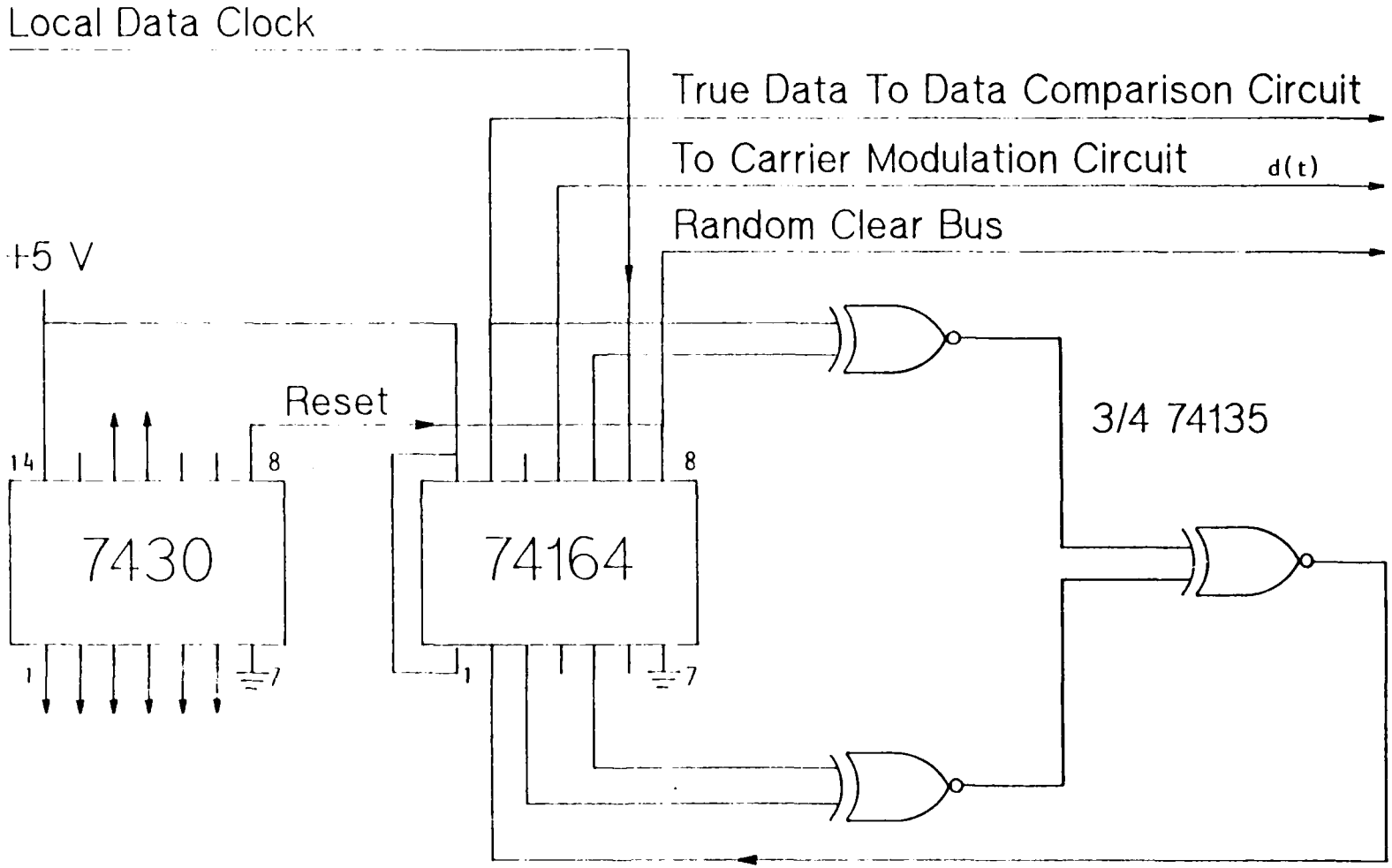


Figure 37. 8 Bit Maximal Length Binary Sequence Generator with Feedback Connections [8,5,3,1] Used to Generate Data Bits.

38 to produce the composite unipolar sequence $m_c(t)$. The sequence is then fed through 1/4 MC1488 which converts the unipolar voltage to bipolar having values $\pm$ 5.8 volts as shown in Chapter III, Figure 8. (The MC1488 is a line driver used for RS-233C communications.)

Carrier modulation is achieved by applying the composite sequence $v_{m_c}(t)$ to the X_1 input of the AD534J AVM while the other input (Y_1) has the carrier term applied. The carrier $c(t)$ is provided by a Fluke 6060A/AN Synthesized Signal Generator. The AVM as used has a voltage transfer characteristic expressed as

$$s(t) + n(t) = \left[\frac{(X_1)(Y_1)}{\mathrm{SF}}\right] + Z_2$$

where, SF = scale factor = 10 for this AVM. Z_2 is the externally applied noise voltage as explained in the next section.

B. CHANNEL SUBSYSTEM

Figure 38 illustrates the hardware implementation of the channel subsystem. An Elgencco 603A WGN Generator produces WGN up to 500 kHz which is filtered by a Murata Erie ceramic BPF. The filter is housed in an enclosed metal box with a 1500 Ω matching network. The measured filter transfer function is shown in Figure 39. The bandlimited noise is applied to a HP 465A Amplifier to produce $n(t)$. As inferred earlier, the noise $n(t)$ is added to the signal using the AD534J so that

$$s(t) + n(t) = \left[\frac{v_{m_c}(t) \cdot c(t)}{10}\right] + n(t)$$

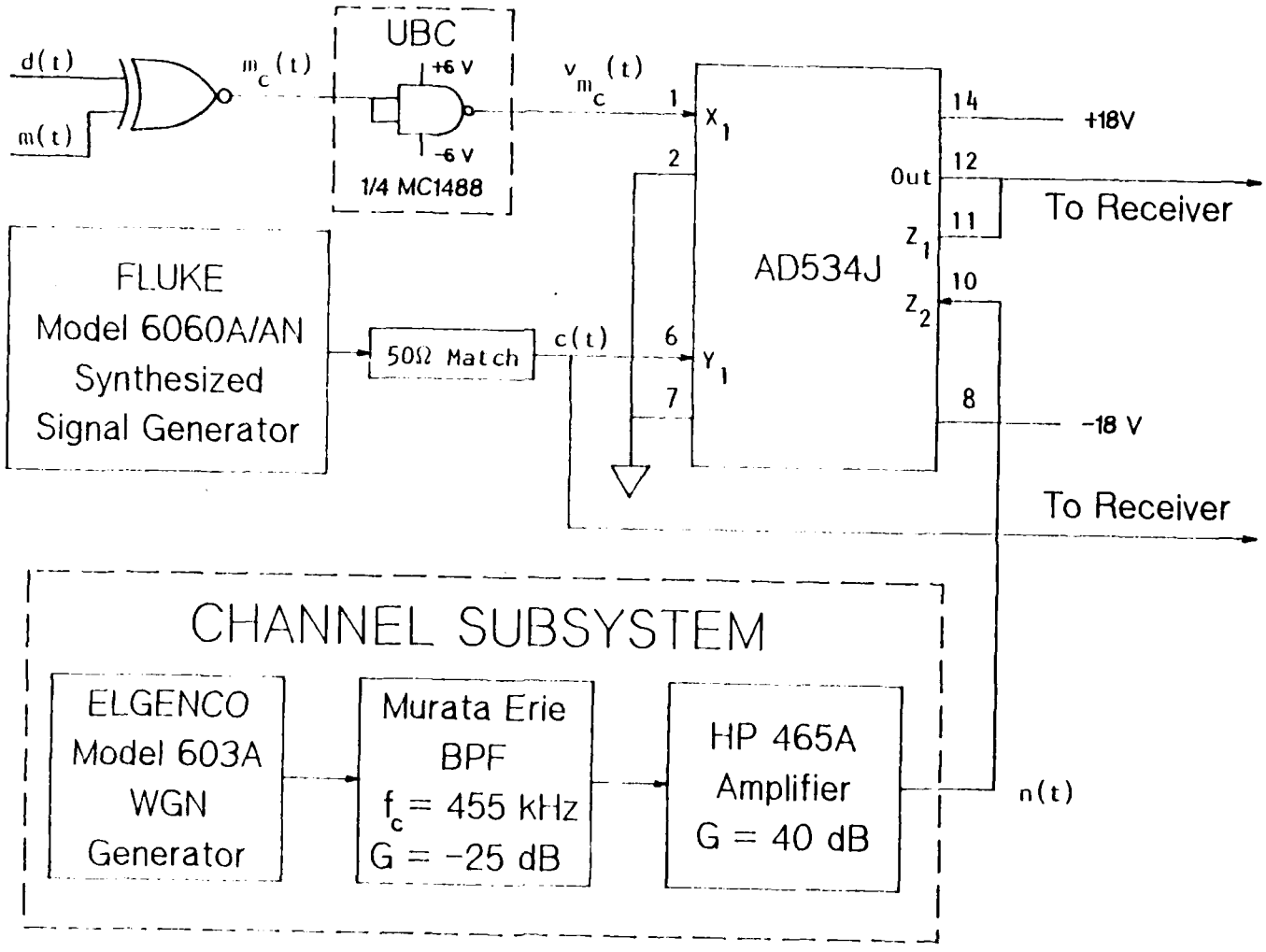


Figure 38. Composite Sequence Generation, Carrier Modulation, and Noise Circuit.

C. RECEIVING SUBSYSTEM

1. Carrier Bandpass Filter

The signal applied to the receiver $s(t)+n(t)$ is filtered by another Murata Erie wideband BPF to produce the received signal $r(t)$ which is applied to the demodulator as shown in Figure 40. The filter transfer function is shown in Figure 39. This filter represents the IF amplifier of a typical superheterodyne receiver. At the output of this filter (input to the receiver demodulator) a HP 3400A True rms Voltmeter measures the power of $r(t)$. The SNR in dB is calculated as

$$\text{SNR} = 10\log\left[\frac{(S)^2}{[(P_T)^2-(S)^2]}\right] \tag{13}$$

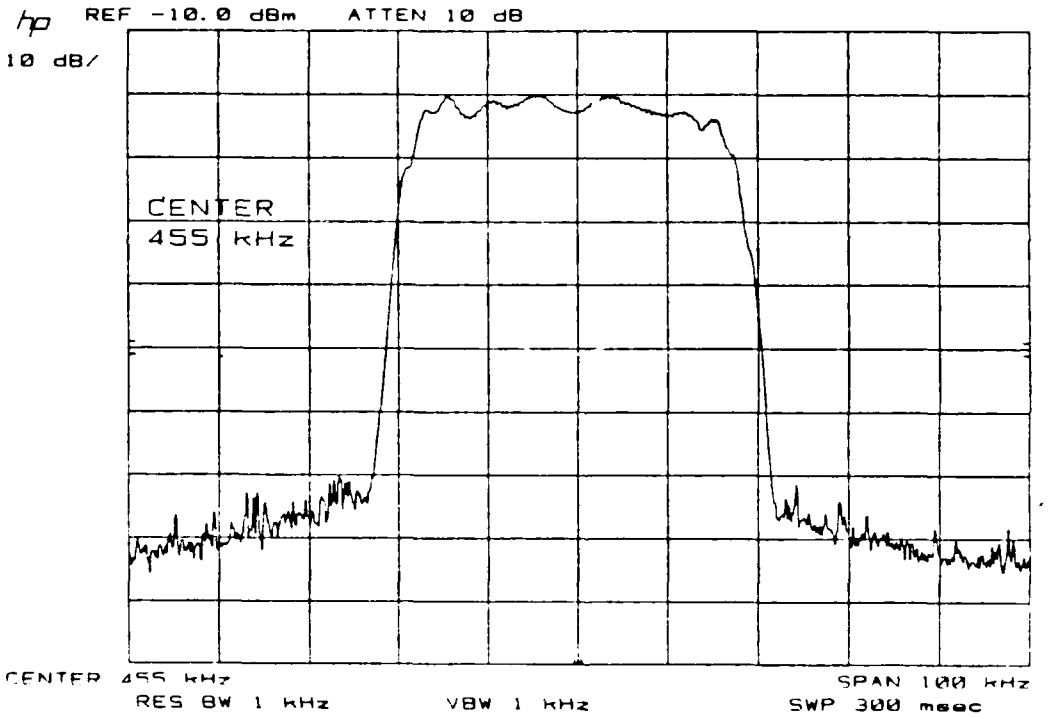


Figure 39. Measured Transfer Function of Murata Erie Wideband Bandpass Filter.

where

S = rms value of the signal voltage

P_T = rms value of the total voltage (signal plus noise).

2. Carrier Demodulation Circuit

The received signal $r(t)$ is demodulated, converted from a bandpass signal to a baseband signal, by applying it to the X_1 input to a AD534J AVM and multiplying it by a coherent carrier as shown in Figure 40. The coherent carrier for demodulation is obtained from the transmitter circuit and applied to the Y_1 input of the demodulator. From equation (8) the output of the demodulator is

$$v_b(t) = \frac{K}{2}\Big[v_{m_c}(t) + v_{m_c}(t)\cos 4\pi f_o t + n_r(t) + n_r(t)\cos 4\pi f_o t - n_s(t)\sin 4\pi f_o t\Big]$$

where the scale factor of 10 has been absorbed into the K term.

3. Lowpass Filter Circuit

A filter/amplifier is used to amplify the baseband signal and remove the 455 and 910 kHz terms as illustrated in Figure 41. The filter uses a biquad design with five 2nd order filters. Figure 42 illustrates the measured transfer function of this filter which has a 3 dB cutoff frequency f_{3dB} of 22 kHz, in-band ripple less than 0.4 dB (from 0 to 16 kHz), and gain of 30 dB. The baseband transfer function was measured on a HP 3580A Spectrum Analyzer.

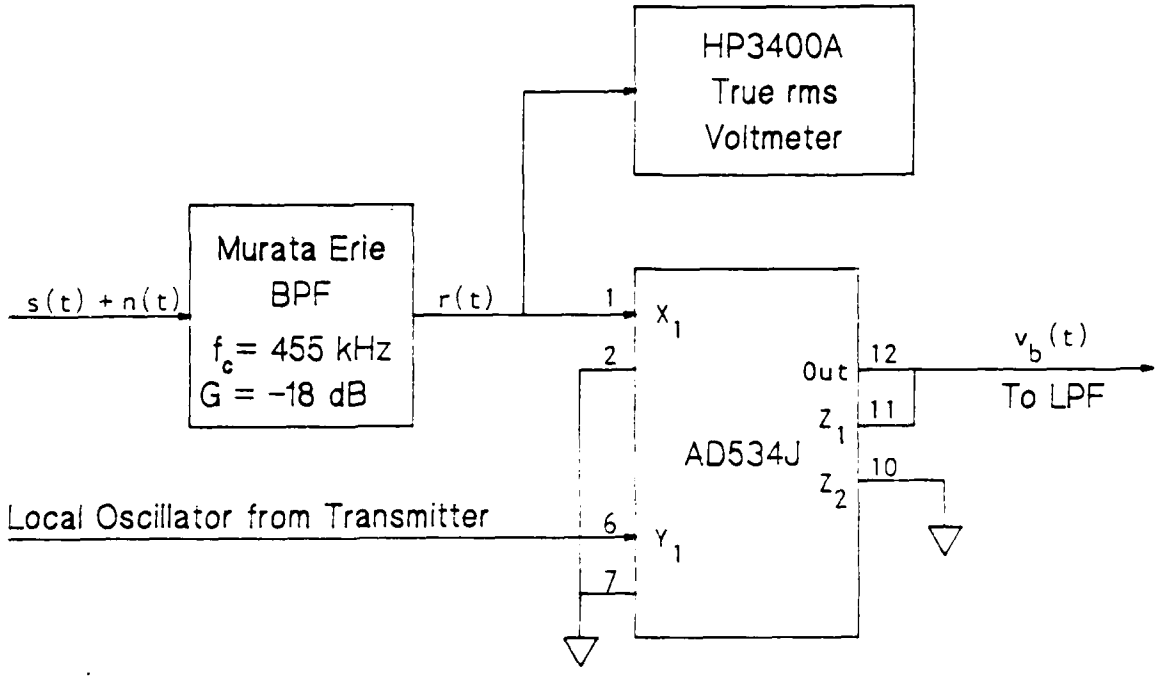


Figure 40. Receiver Wideband BPF and Coherent Carrier Demodulation Circuit.

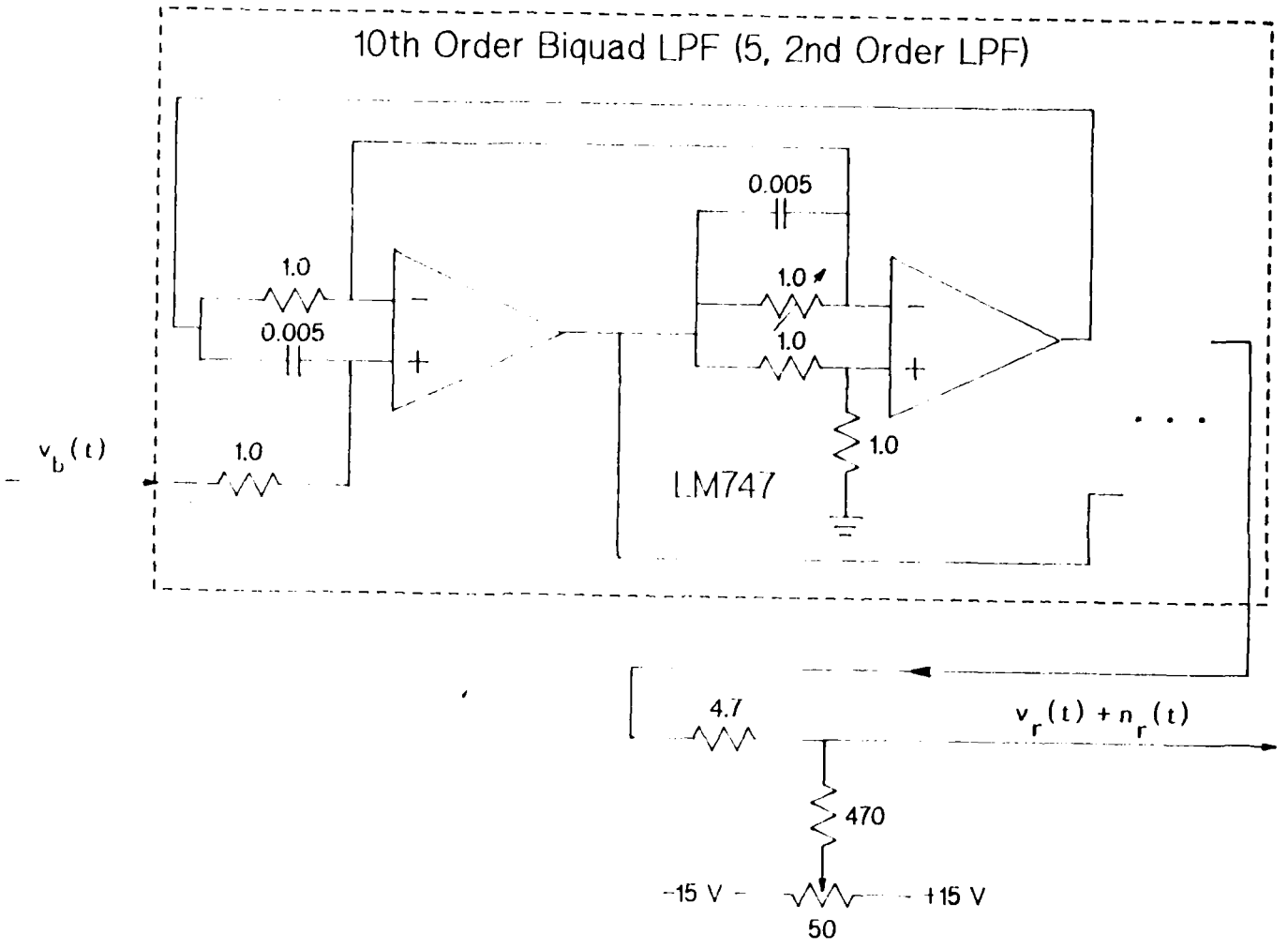


Figure 41. Lowpass Filter After Carrier Demodulation.

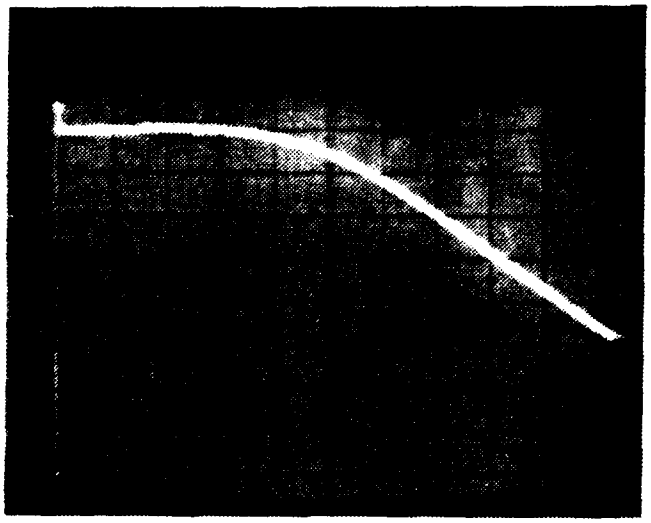
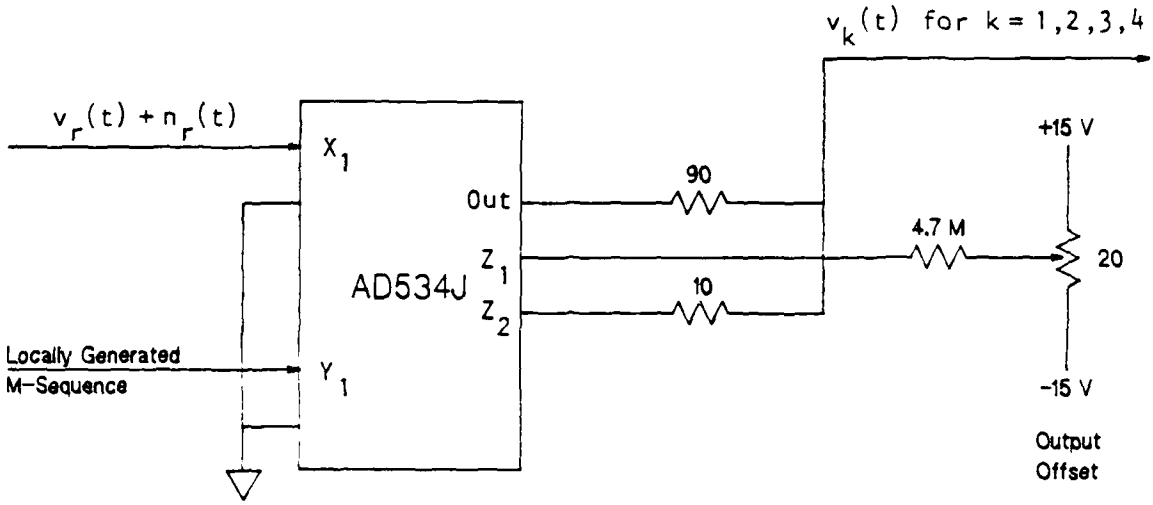


Figure 42. Measured Transfer Function of the LPF Used After the Carrier Demodulator, (Scales: Horizontal; 5 kHz/ div., Vertical; 10 dB/div., Resolution BW; 30 Hz, Calibration; −50 dB (middle of screen)).

4. Dual-Channel Delay-Lock Loop Circuitry

a. No Data Transmitted (Synchronization Version)

(1) Analog Voltage Muitiplication. Figure 43 illustrates the AVM circuit that is used in each channel of the DCDLL. (These are also used for the other channels as well.) This AVM is an AD534J with a scale factor of 1; this helps to reduce the noise produced by the AD534J. The output offset is used to add a small DC value such that the $-1/L$ correlation value and output offset variations of the early and late AVM components can be adjusted to zero volts.



$v_\ell(t + T_c)$	produces	$v_1(t)$,	(Early, DCDLL)
$v_\ell(t - T_c)$	produces	$v_2(t)$,	(Late, DCDLL)
$v_\ell(t)$	produces	$v_3(t)$,	(Punctual, DCDLL)
$v_{mm}(t)$	produces	$v_4(t)$,	(Early−Late, SCDLL)

Figure 43. Analog Voltage Multiplier Circuit Used in Each Channel (Early, Late, and Punctual) of the Receiver.

(2) Differential Amplifier. The differential amplifier used for the DCDLL is an LM741 operational amplifier (op-amp) and produces unity gain. This circuit is shown in Figure 44 and, from equation (10), produces

$$v_e(t) = v_1(t) - v_2(t).$$

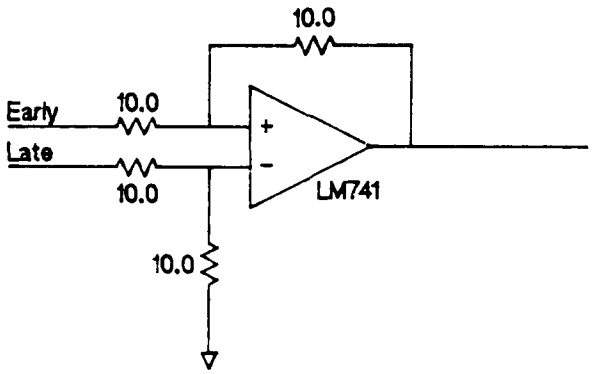


Figure 44. Differential Amplifier used in Dual-Channel Delay-Lock Loop.

(3) Loop Filter and Error Voltage Adjustment Circuitry. The error signal $v_e(t)$ is filtered by the loop filter to reduce the BW of the loop to approximately 10 Hz. This cutoff frequency determines the relative clock difference for which the loop can obtain lock. The filter is a 12th order Chebyshev design with designed ripple of 0.1 dB and unity gain [Ref. 7: pp. 260-265] and is shown in Figure 45. Figure 46 illustrates the measured transfer function of this loop filter using the HP 3580A Spectrum Analyzer.

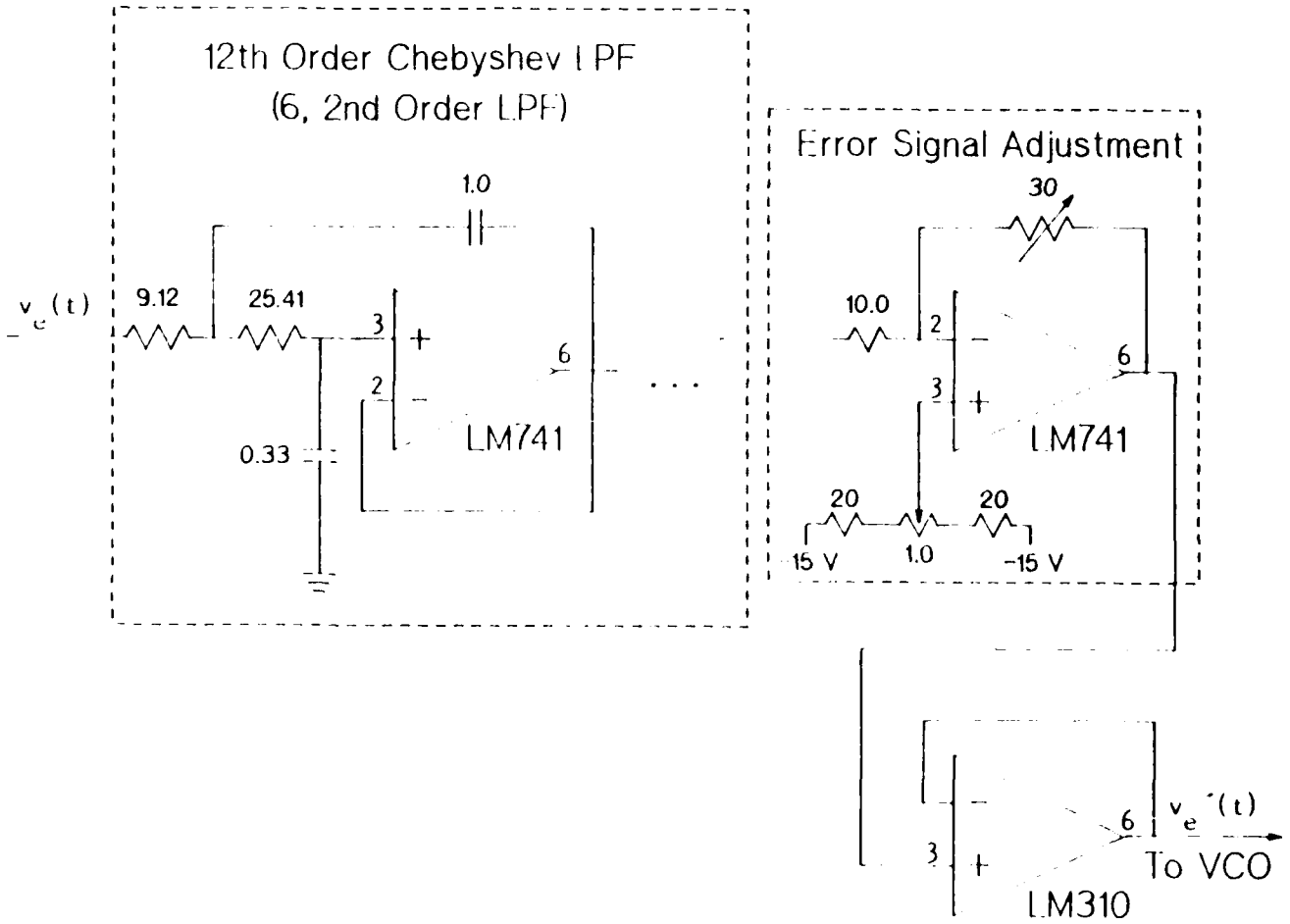


Figure 45. Loop Lowpass Filter and Voltage Adjustment Circuitry to Produce Error Voltage $v_e'(t)$ for the VCO.

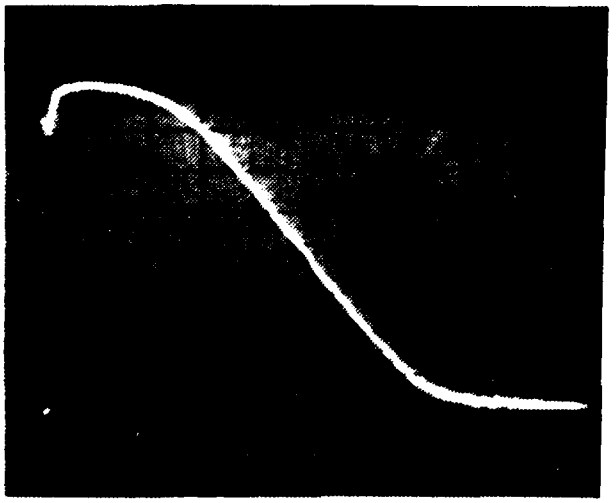


Figure 46. Measured Transfer Function of Loop LPF. (Scales: Horizontal: 5 Hz/div., Vertical: 10 dB. Resolution BW: 1 Hz).

As illustrated in Figure 45, the output of the loop filter is amplified by an inverting LM741 op-amp, biased for a zero offset, and buffered by an LM310 op-amp to produce the filtered error voltage $v_e'(t)$.

(4) Voltage Controlled Oscillator Circuit. Preliminary designs of the DLL incorporated commercially available single package VCO integrated circuits (IC). However, most commercially available VCO chips work over a wide range of frequency and are very sensitive to input voltage. These properties are not desired in this application. Thus, a stable VCO was designed to provide a small frequency change of ± 10 Hz about a rest frequency of 16.000 Hz via a relatively large input voltage. Figure 47 illustrates the VCO that was designed to have these properties. The VCO has to adjust its frequency up or down based on a negative or positive value of the error voltage $v_e'(t)$. This error voltage is inverted by an LM741 op-amp, buffered by an LM310 to produce $v_e'(t)^-$. The two inputs to an LM741 integrating op-amp $v_e'(t)^+$ and $v_e'(t)^-$ produce a sawtooth wave at the output of the

LM741 integrating op-amp. The feedback resistor and capacitor on the negative input to the integrator determine the rest frequency of the VCO. The pair of 1.0 kΩ resistors on the output reduce the value of the output and provide a reference sawtooth voltage fed back to the input. The ratio of the input resistor values (380 kΩ) to that of output resistors (1.0 kΩ) control the sensitivity of the VCO. The bipodal sawtooth wave is then applied to a 1/4 MC1489 which converts the bipodal signal to a unipolar TTL compatible clock. This clock is then applied to the local BSG and local divide-by-255 counter. (The MC1489 is a line receiver used in RS-232C communications.) Figure 48 illustrates the operating characteristic of this VCO.

(5) Despreading Binary Sequence Generator. The BSG used in the DLL for despreading via correlation operations is illustrated in Figure 49. It is identical in design to that used in the transmitter (Figure 35) except the clock at $f_\ell = 16,000 \pm 10$ Hz is supplied by the VCO. The unipolar outputs from stages 6, 7, and 8 ($m_\ell(t+T_c)$, $m_\ell(t)$, and $m_\ell(t-T_c)$, respectively) are converted to bipolar by 3/4 MC1488 to produce $v_\ell(t+T_c), v_\ell(t)$, and $v_\ell(t-T_c)$ which go to the early, punctual (if used), and late channels.

b. Operation with Data (Synchronization and Data Version)

The circuits that are added to the DCDLL (synchronization version) to enable it to obtain lock when the received sequence has random data inversions are considered here.

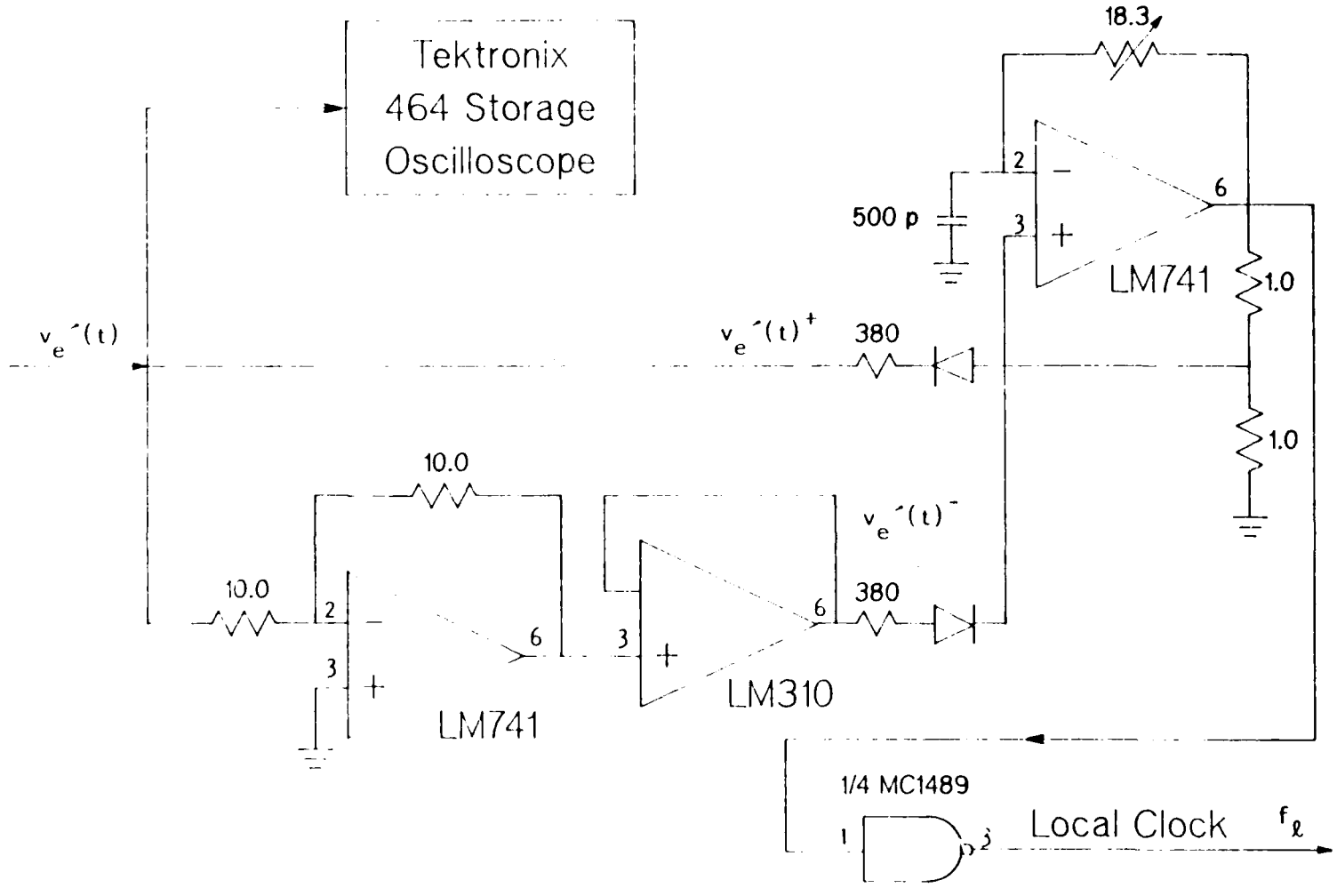


Figure 47. Voltage Controlled Oscillator Circuit.

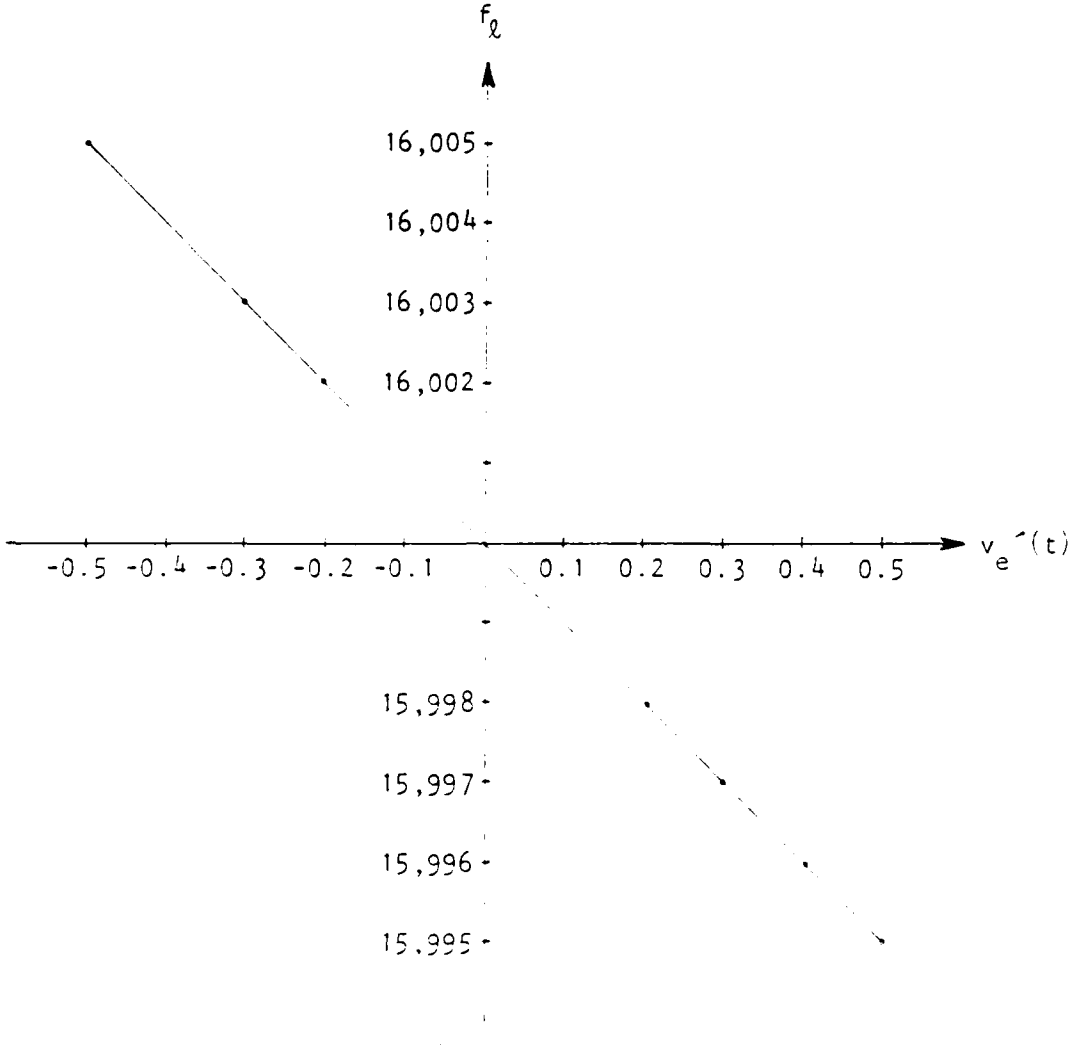


Figure 48. VCO Operating Characteristics.

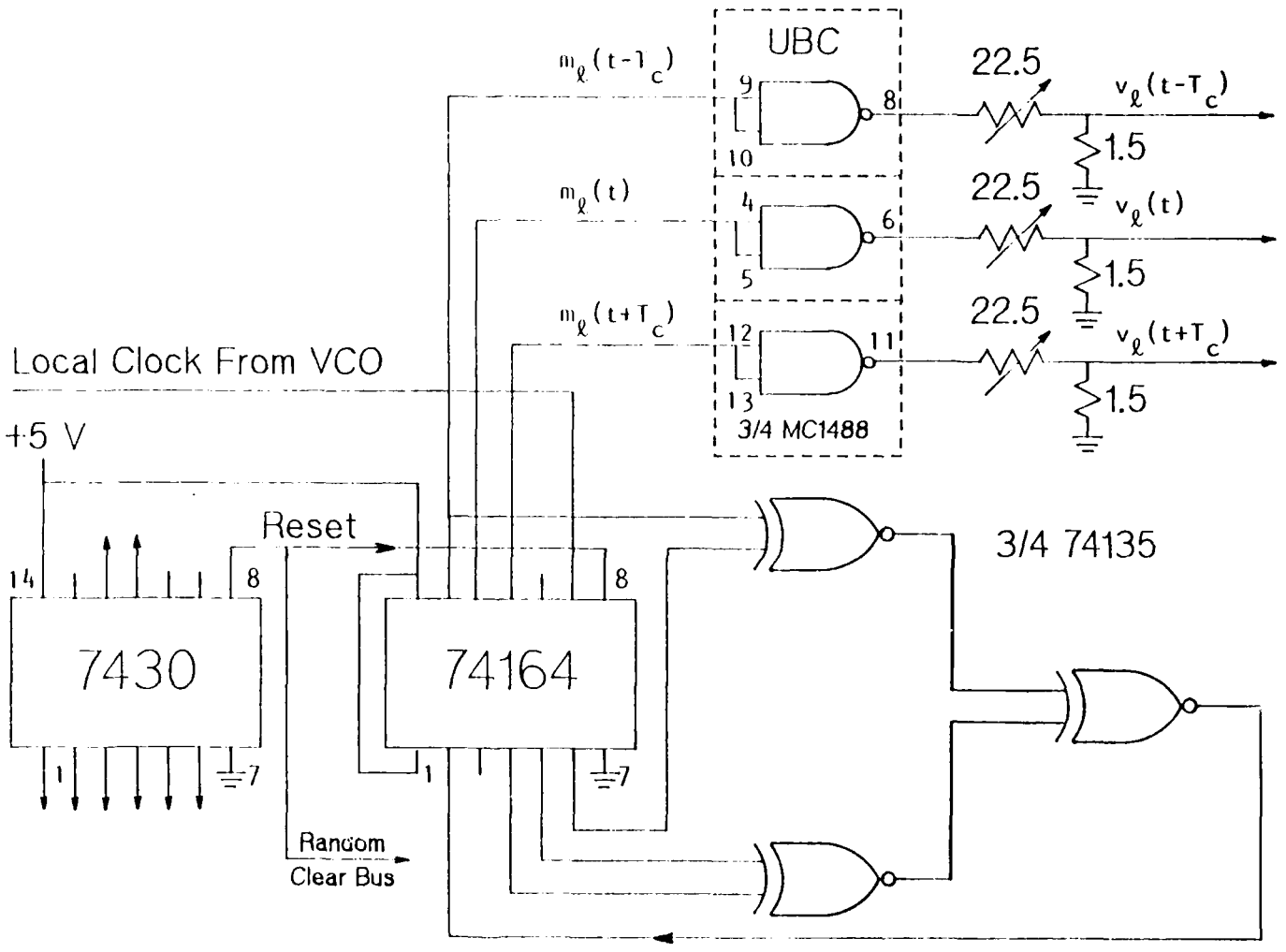


Figure 49. 8-Bit Maximal Length Binary Sequence Generator with [8,4,3,2] Connections for Despreading within Delay-Lock Loop.

(1) Integrating Data Lowpass Filter and ACF Rectification Circuit. The correlating LPF and rectification circuits added to each channel in the DCDLL are shown in Figure 50. The LPF is basically the same in design as that used for the loop filter. Four 2nd order filters produce an 8th order Chebyshev response. The filter was designed to have $f_{3dB} = 62.7$ Hz to pass the data transitions completely; however, the actual $f_{3dB} \approx 50$ Hz. The measured transfer function of this data LPF is illustrated in Figure 51. Since $f_{3dB} \approx 50$ Hz < 62.7 Hz, the one string of eight 0 bits is attenuated more than the other transitions.

The circuit used to rectify the output of the data LPF is an amplifier-coupled full-wave rectifier [Ref. 8: pp. 159-160] as shown in Figure 50. This circuit has unity gain and provides the absolute value of the input. Figure 52a illustrates the positive and negative voltage input. The output is shown in Figure 52b. With the diodes in the feedback paths of the circuit, the turn-on threshold of each diode (0.7 volts) is divided by the open loop gain of each op-amp (1/2 of LM747) and reduces the turn-on threshold of the circuit to approximately 0 volts; this is often referred to as a "superdiode".

5. Single-Channel Delay-Lock Loop Circuitry

The SCDLL utilizes the same components as the DCDLL (synchronization version) less one AVM (Figure 43) and the differential amplifier in Figure 44 and uses the three-level sequence $v_{mm}(t)$ for correlation with the received signal $v_r(t) + n_r(t)$. Generation of $v_{mm}(t)$ is accomplished by the circuit shown in Figure 53. The early and late locally generated bipolar m-sequences are buffered (LM310) and then subtracted by a high-speed differential amplifier (LF356) to produce $v_{mm}(t)$.

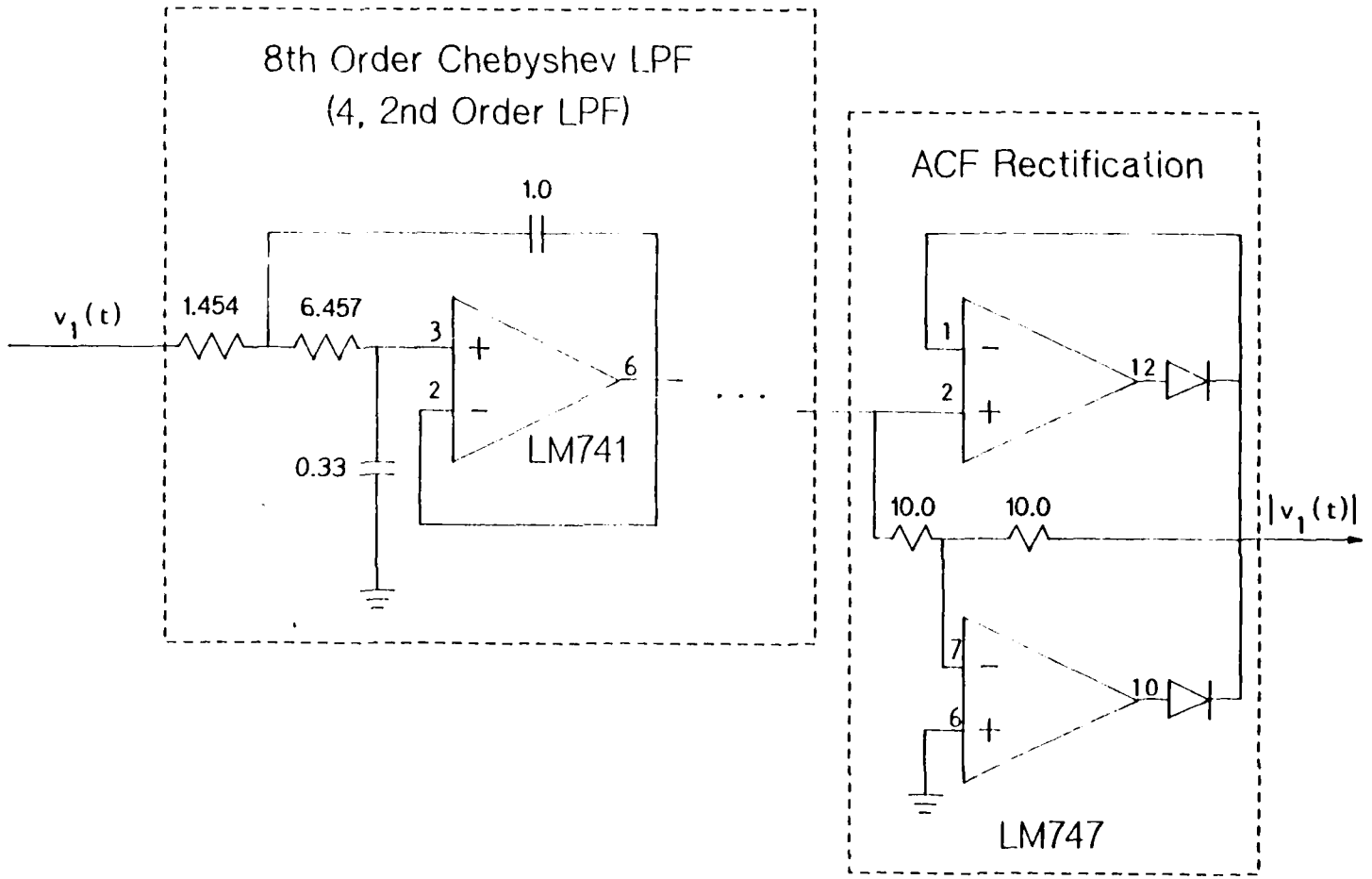


Figure 50. Integrating Data Lowpass Filter and Autocorrelation Function Rectification Circuitry.

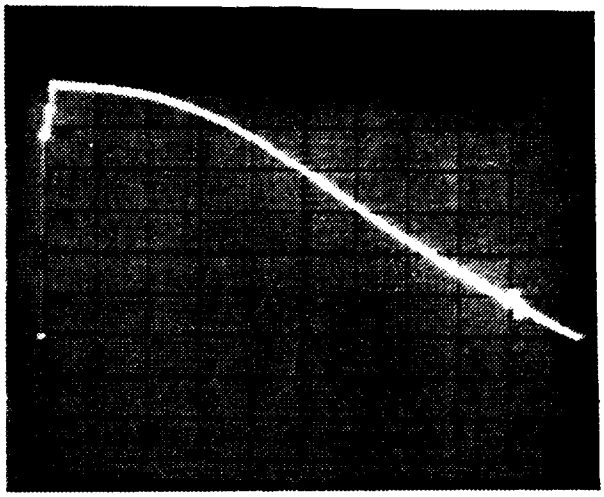
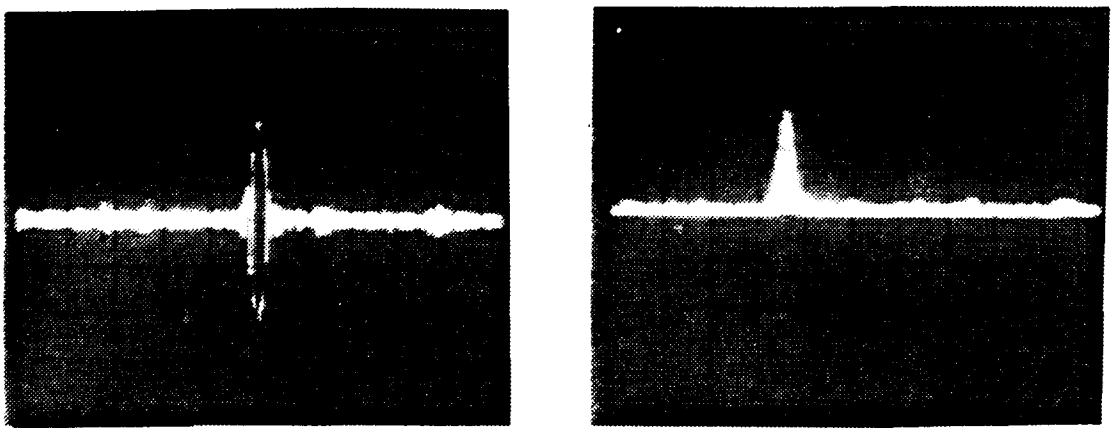


Figure 51. Measured Data LPF Transfer Function Used in DCDLL Operation with Data, (Scales: Horizontal; 20 Hz/div., Vertical; 10 dB/div., Resolution BW; 3 Hz).



(a) (b)

Figure 52. ACF Rectification Circuit, a) Input, and b) Output, (Scales: Horizontal 0.5 sec/div., Vertical; 0.5 V/div.), Storage: On.

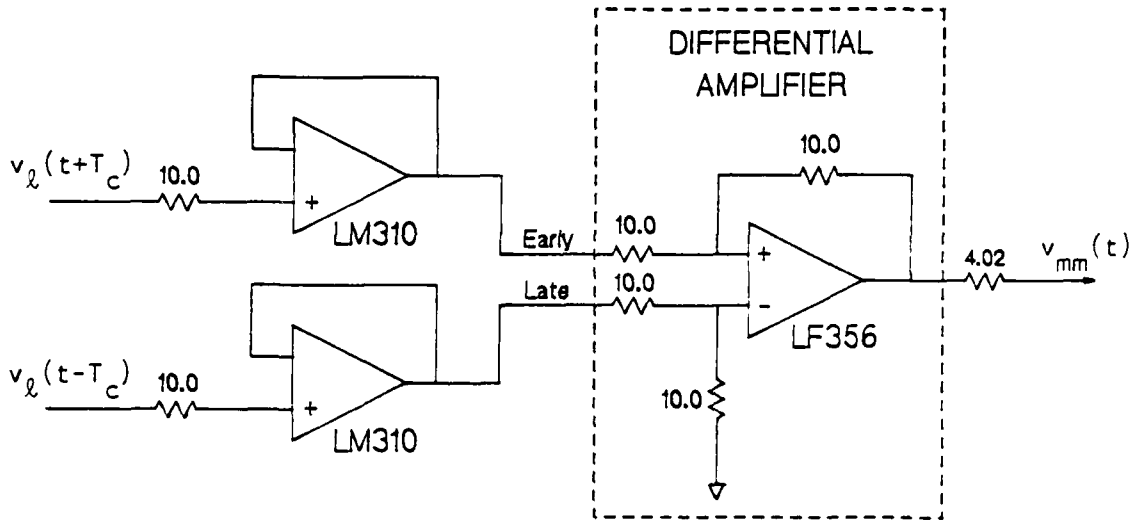


Figure 53. Generation of the Three-Level Sequence for the Single-Channel Delay-Lock Loop.

6. Data Recovery Circuitry

a. Punctual Correlator

(1) Analog Voltage Multiplier. The received signal $v_r(t) + n_r(t)$ is first multiplied by the locally generated punctual sequence $v_\ell(t)$ by an AD534J AVM shown as Figure 43. This multiplication acts to despread the received sequence and produce $v_4(t)$ illustrated in Figure 31. This is where the processing gain of the system is realized.

(2) Integrate and Dump Matched Filter Circuit. Figure 54 shows the integrate and dump circuit that is used. An LM741 op-amp is used and the capacitor in the feedback path is chosen to produce a maximum value at the end of the bit interval of T_b seconds. The switch in the feedback path acts to dump or discharge the capacitor value at the end of the bit interval after the output has been sampled. An MC14501 Multiplexer IC was used for the switch and was wired

such that when it receives a high-level dump pulse, it will short the output of the integrator to ground.

b. Sample and Hold, and Bipolar-to-Unipolar Circuit

The output of the integrator $v_{ID}(t)$ is applied to a LF398 Sample and Hold IC (Figure 54). The LF398 receives a sample pulse and samples $v_{ID}(t)$ just before the integrator is dumped to zero volts and then held for T_b sec to produce $v_{SH}(t)$.

The bipolar output of the sample and hold IC is fed through a LM311 zero crossing detector and configured such that the output is unipolar. This output is applied to a flip flop (1-bit quantizer) (one stage of a 74164 shift register is used) and then inverted by an 1/6 7404 digital inverter to produce the recovered bit stream $\hat{d}(t)$.

c. Divide-by-255 Circuit

This circuit used in the data recovery system is identical in design to that found in Figure 36, but it receives its clock from the VCO. The output of the receiver divide-by-255 circuit provides bit timing for the dump and sample times as well as for bit comparison circuitry. It should be noted that the load line of the transmitter divide-by-255 counter is tied to the load line of the receiver divide-by-255 counter; this ensures bit synchronization and is normally accomplished by a bit synchronization loop. This was not performed because the scope of this research effort was limited to the spread spectrum aspects of the system.

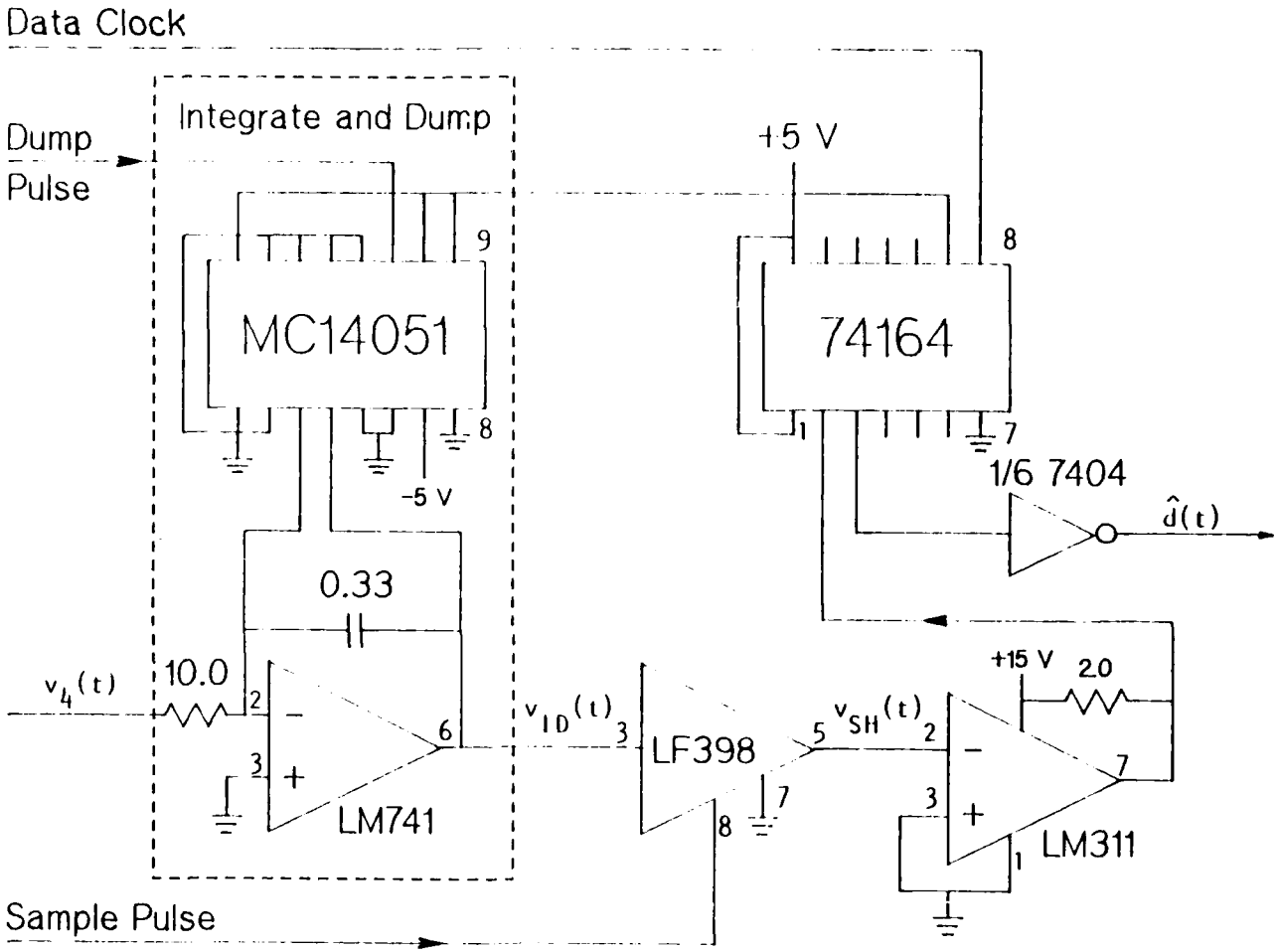


Figure 54. Integrate and Dump Matched Filter Used in the Punctual Correlator with Sample and Hold, and Threshold Detector to Produce $\hat{d}(t)$.

d. Dump and Sample Timing Circuit

This circuit, as shown in Figure 55, takes the data clock and generates two relatively narrow pulses each of approximate duration 0.33 msec. This is accomplished by using two 74121 one shots in series.

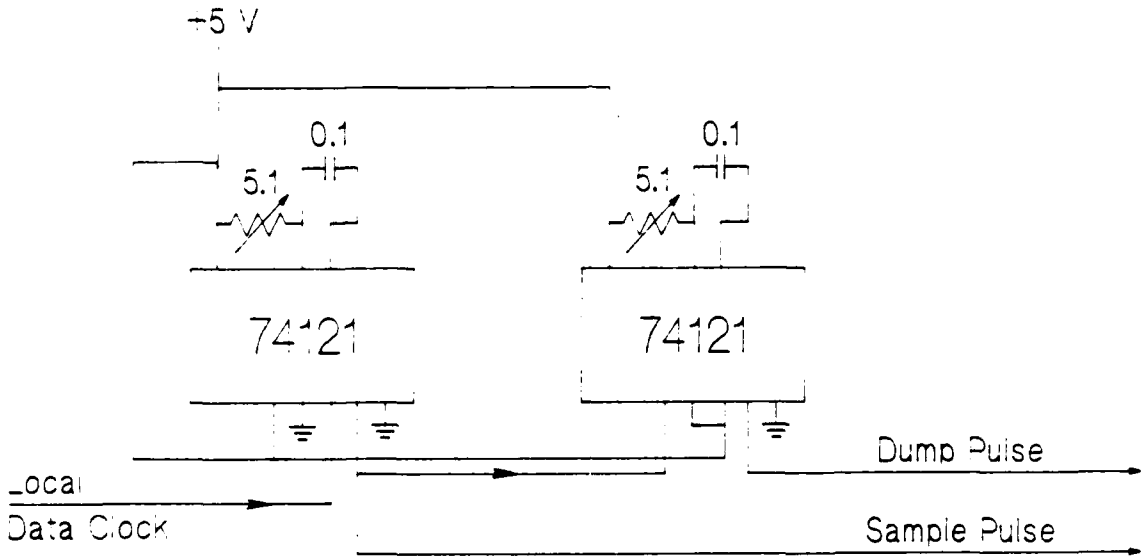


Figure 55. Sample and Dump Timing Pulse Generation Circuit.

7. Probability of Bit Error Measurement Circuit

Figure 56 illustrates the circuit that measures the BER. The circuit takes the local data clock from the divide-by-255 counter and produces a data compare pulse of approximate duration 2.5 msec in the middle of the bit interval, as illustrated earlier in Figure 33. Generation of this bit compare pulse is accomplished by using two 74121 one shots in series. This pulse is applied simultaneously to two AND gates (each 1/4 7408) so that $\hat{d}(t)$ and $d(t)$ are applied at the 2 input pins of an XOR gate (1/4 7486) at the bit compare time. See Figure 56. Thus,

if these two inputs are different, the output will go high; and if the dual- in-line package (DIP) switch is closed, an error will be registered on one of the HP 5300A Measurement System counters. The other HP 5300A counter measures total bit count so the ratio of the counts on these two counters is the BER $= P_e$.

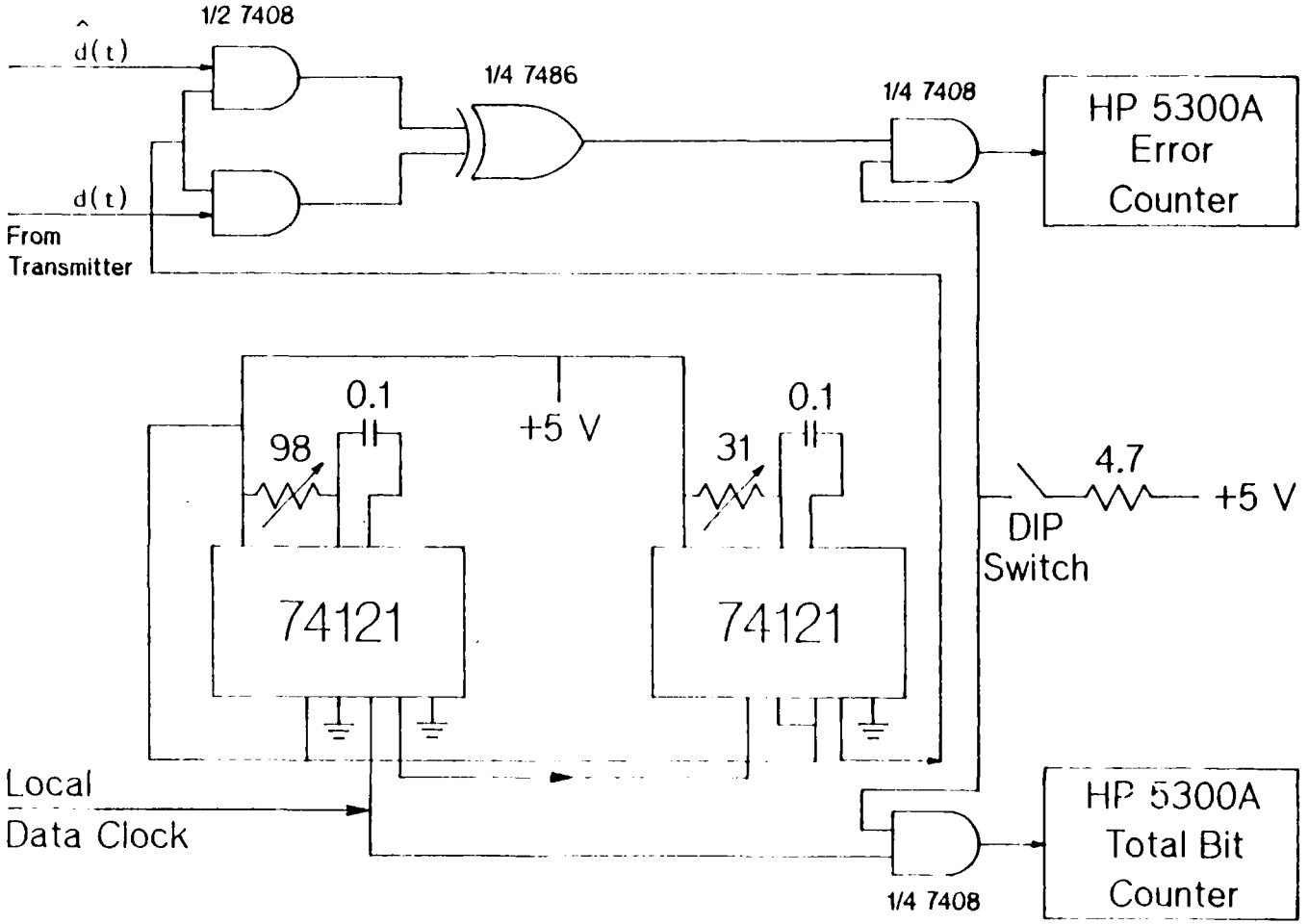


Figure 56. Data Comparison Circuit to Obtain Probability of Bit Error Measurement.

V. METHOD OF TEST

All laboratory tests were performed within an Ace Shielded Room at the Naval Postgraduate School, Monterey, CA. Data were taken to measure two subjects of interest: 1) the noise performance of the SCDLL as compared with the DCDLL with no data being transmitted, and 2) the noise performance of the DS spread spectrum system while transmitting data using the DCDLL.

A. LOSS OF LOCK PERFORMANCE TESTS

For these tests, the switch in Figure 5 was placed in the A volts position thus disabling data modulation. The amplitude of the CW signal from the Fluke 6060 A/AN Synthesized Function Generator (acting as the carrier oscillator) was set to provide for the desired signal power level of $S = (0.15)^2$ watts. The final error voltage $v'_e(t)$ was then adjusted to have a ± 0.8 volts swing where $f_\Delta = \pm 5$ Hz as illustrated in Figure 26. A total of four tests were performed at each of four offset frequencies of the transmitter clock (f_r = 16,000 Hz for all of these tests) and the receiver local clock. The VCO local clock rate was f_ℓ = 15,994, 15,997, 16,003, and 16,006 Hz (before lock) which corresponds to VCO input voltages of $-0.6, -0.3, +0.3$, or $+0.6$ volts (after lock). Thus, f_Δ equals $-6, -3, +3$, or $+6$ Hz respectively. These four test conditions are illustrated in Figure 57. Each test consists of ten subtests. For each subtest, the loop obtained lock to maintain the proper offset voltage at the VCO input. This error signal was monitored on a Tektronix 464 Storage Oscilloscope. Noise was then added to the signal manually by increasing the power out of the Elgencco 603A WGN Generator. When the constant DC term in the noisy error voltage disappeared, loss of lock was declared.

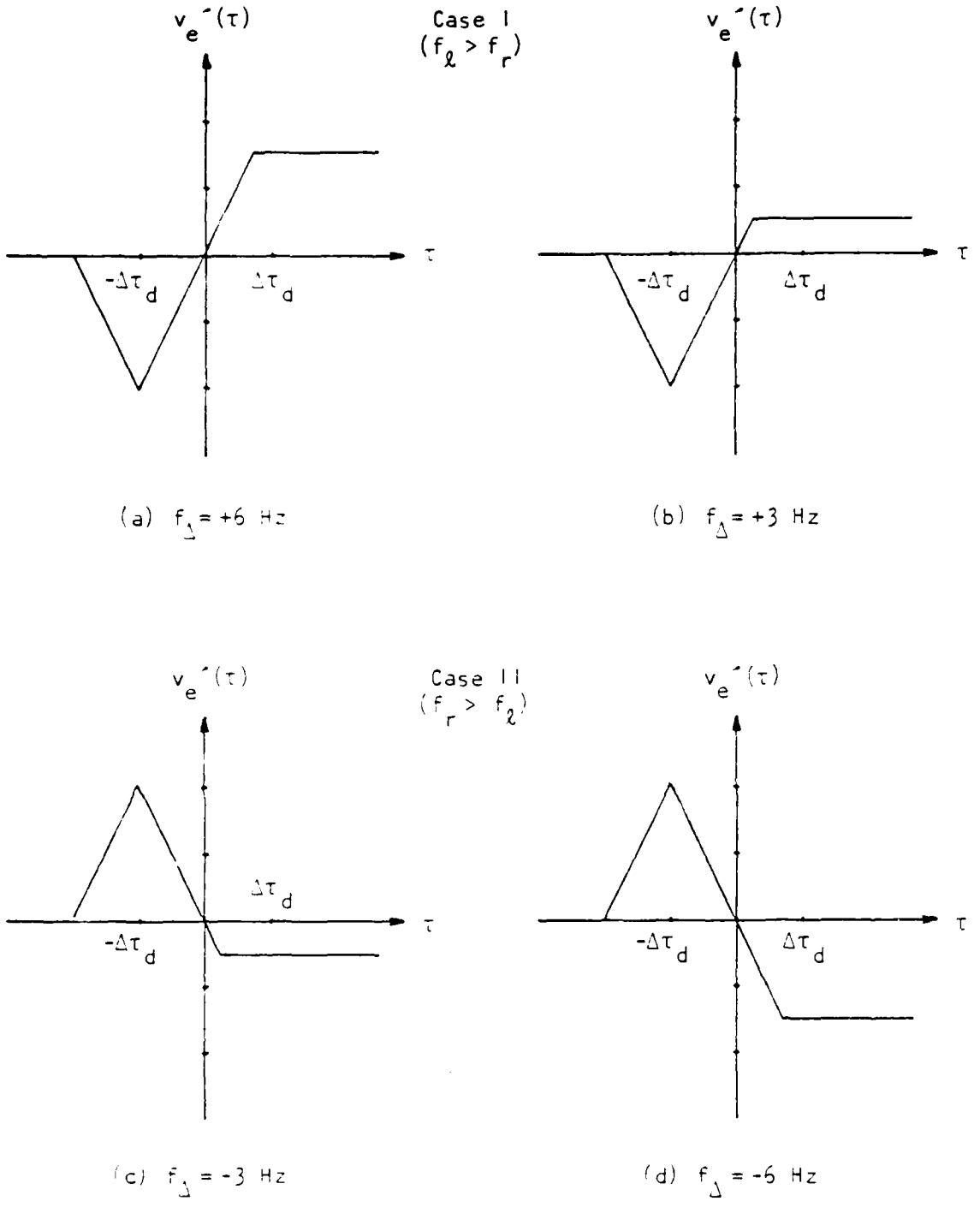


Figure 57. Illustration of the Error Voltage $v_e'(t)$ Test Conditions for the Loss of Lock Tests with $f_r = 16.000$ Hz and, a) $f_\ell = 16.006$ Hz, b) $f_\ell = 16.003$ Hz, c) $f_\ell = 15.997$ Hz, and d) $f_\ell = 15.994$ Hz before lock.

The total signal power P_T was obtained by squaring the HP 3400A True rms Voltmeter reading at the input to the carrier demodulator (Figure 15). For each of the ten subtests, values of P_T which caused loop lock were then averaged to produce $\overline{P_T}$. The final performance for a test is then given by

$$\text{SNR} = 10 \log \left[\frac{(0.15)^2}{[(\overline{P_T})^2 - (0.15)^2]} \right] \text{dB}.$$

This series of tests were performed for the DCDLL and then repeated for the SCDLL. Each DLL was configured as illustrated in Figure 21 and 30, respectively.

B. PROBABILITY OF BIT ERROR PERFORMANCE TESTS

The switch in Figure 5 is placed in the $d(t)$ position allowing data modulation, and the DCDLL was used as configured in Figure 27. The amplitude of the CW signal was set to provide a constant signal power of $S = (0.3)^2$. The final error voltage $v_e'(t)$ was adjusted to provide a ± 0.8 volts swing with $f_\Delta = \pm 5$ Hz as illustrated in Figure 29. For these tests the loop obtained lock and the input VCO offset voltage was adjusted to zero volts; thus, $f_r = f_\ell = 16,000$ Hz. The noise power was then fixed to produce values of constant SNR $= -16, -15, -14$, or -13 dB. A test was performed by clearing both the HP 5300A counter (Figure 54) and enabling the DIP switch which began the test. A test was completed when a total error count of 100, 100, 5, or 3 was reached on the error counter at the respective SNR. The P_e for a test was obtained by dividing the total error count by the total bit count. A final P_e was obtained by averaging two P_e values at a given SNR level. Thus four final P_e values are obtained at the four different values of SNR for the DCDLL.

VI. RESULTS AND DISCUSSION

A. LOSS OF LOCK PERFORMANCE TEST RESULTS

The recovered value of signal power was $S = (0.15)^2$ watts (at the input to the demodulator) which was less than that for the probability of error performance tests. This was necessary to achieve the very small values of SNR required for loss of loop lock. The smallest SNR that was obtainable was −25.86 dB. This was dictated by the power supply of the noise summing amplifier (the AD534J AVM of the transmitter as illustrated in Figure 43). Table I lists the averaged data that was collected on the DCDLL and SCDLL (with no data being transmitted). At the relatively "slow" clock passing rate of ±3 Hz (Figure 57b and 57c), the DLL

TABLE I
AVERAGED LOSS OF LOCK PERFORMANCE DATA

SNR \ f_Δ	+ 6	+ 3	− 3	− 6
Dual Channel	−22.68	−24.56	−25.86	
Single Channel	−23.18	−25.16	[illegible]	

under test operates closer to its optimum [illegible]

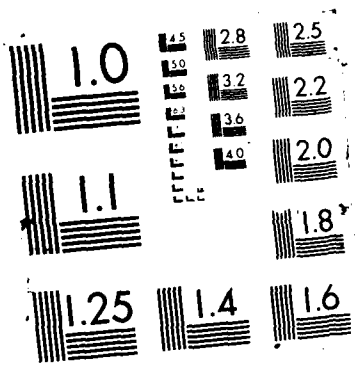
performs better than at an offset of ±6 Hz [illegible]

performed so well that the [illegible]

(SNR = −25.86 dB and [illegible]

AD-A186 280 MEASURED NOISE PERFORMANCE OF A DIRECT-SEQUENCE SPREAD-SPECTRUM SYSTEM AN..(U) NAVAL POSTGRADUATE SCHOOL MONTEREY CA C G BARTONE SEP 87 2/2

UNCLASSIFIED F/G 25/2 NL


1.0
1.1
1.25
1.4
1.6
1.8
2.0
2.2
2.5
2.8
3.2
3.6
4.0
4.5
5.0
5.6

20 sec to 1 min.). It was observed that both loops performed slightly better at negative offset values of frequency than positive offset values. This is attributed to the VCO operating characteristics and its noise performance. From the data collected and presented in Table I, it is clearly evident that the SCDLL performs slightly better than the DCDLL. These data indicate that the SCDLL will maintain lock with up to 0.64 dB more noise power at the input to the receiver (prior to demodulation). This improvement in performance is attributed to the fact that the SCDLL does not rely on the cancellation of the noise components of $v_1(t)$ and $v_2(t)$ as in the dual-channel system. In the DCDLL the noise components of $v_1(t)$ and $v_2(t)$ may not exactly cancel due to gain and delay mismatch of the two channels.

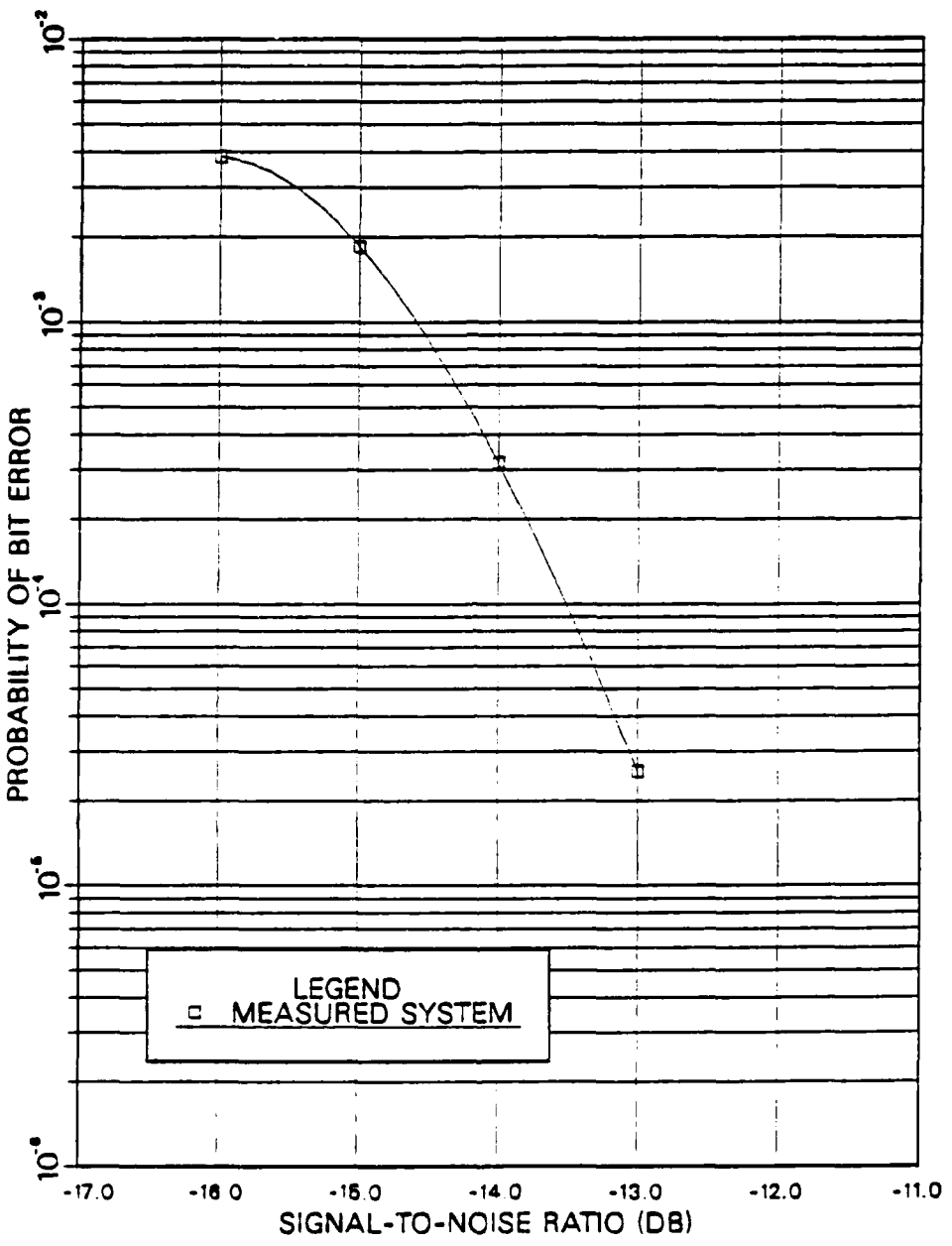
B. PROBABILITY OF ERROR PERFORMANCE TEST RESULTS

The signal power was set to $S = (0.3)^2$ watts so the loop gain was decreased by approximately 1/2 to produce ± 0.8 volts variation of $v_e'(t)$ (Figure 29) before lock. Then, with data modulation occurring in the transmitter, the loop obtained lock. The VCO was then adjusted such that $v_e'(t)$ after lock was approximately 0 volts. This adjustment to zero volts ensured that bit errors resulting when noise was added were due to carrier demodulation and not by the DCDLL itself.

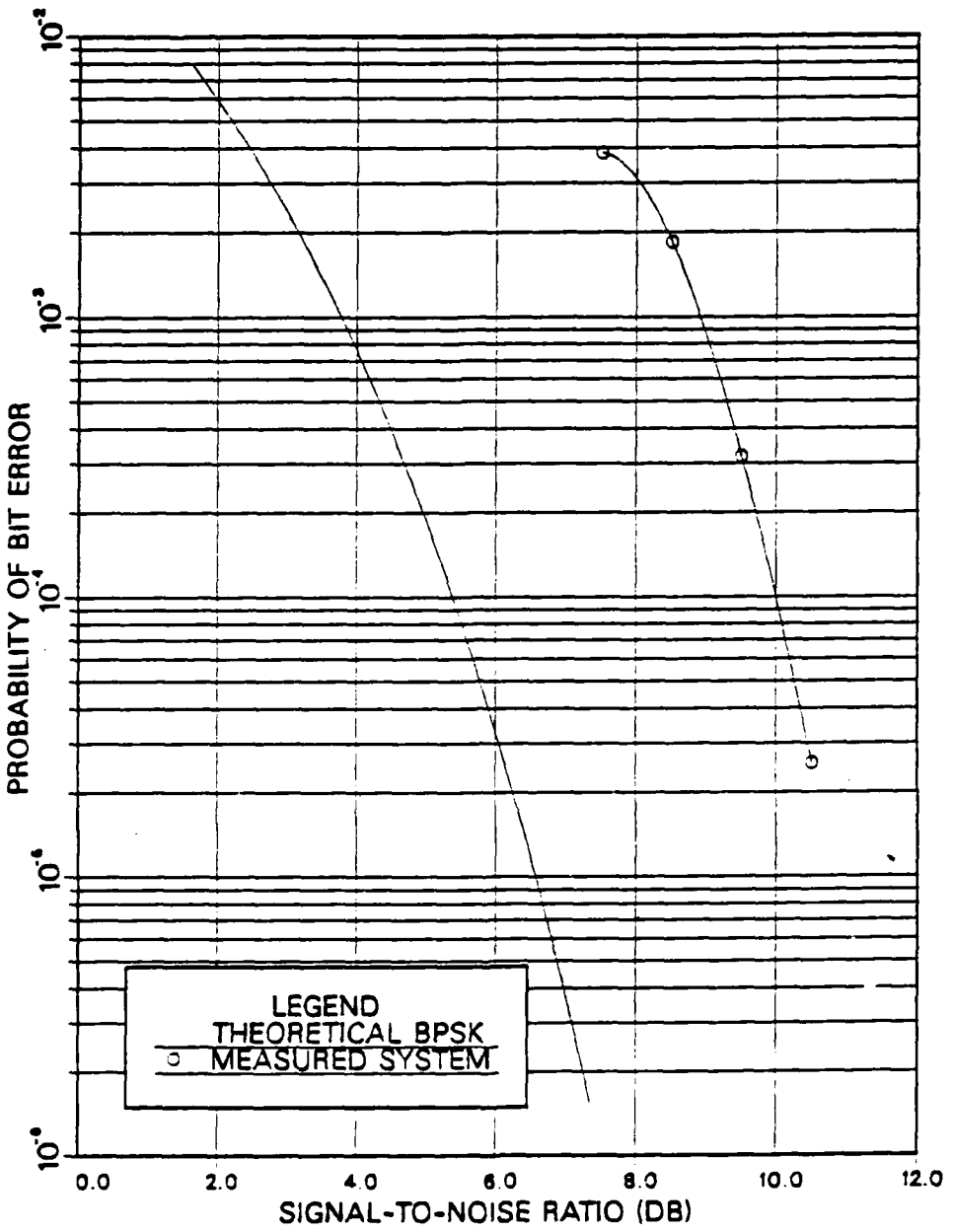
The VCO short term (0 to 7 min.) stability (± 1 Hz) was very good; however, its long term stability (i.e., 7 to 40 min.) was less than desired. Thus, in an attempt to keep the VCO operating point around its optimum point of ± 0 volts, the number of errors before test completion was varied. At low SNR (SNR = -16 dB), errors occurred fairly frequently so a test was completed with 100 errors. Figure 58a illustrates the final P_e at the four values of SNR used in the data collection. To compare these data with the theoretical BER of BPSK the curve of Figure 58a is translated by the amount of processing gain of the DS spread spectrum system.

Figure 58b plots Figure 58a translated by 23.51 dB, the theoretical value of PG. Note the theoretical BPSK curve in Figure 58b is for input SNR and is 3 dB to the left of a "typical" E_b/N_o curve. This is because $E_b/N_o = 2$ SNR. See equation 12. Thus we see that the system PG is approximately 5 dB less than predicted. This 5 dB loss is attributed to some errors being introduced by the DCDLL itself (VCO drift), non-ideal filtering, gain and delay mismatch of each channel within the DCDLL, and non-ideal components. However the majority of this 5 dB loss is attributed to the phase delay and "non-coherent" demodulation of the carrier. As the signal $s(t)$ passes through the IF BPF (Figure 15) a 2.2 μsec phase delay is introduced. Recall the carrier oscillator term used for demodulation was taken from the transmitter directly with no compensating phase delay. This results in a 45.86° relative phase delay between the received signal $r(t)$ and $c(t)$ at the demodulator. Thus, the amplitude of $v_b(t)$ is reduced by cos 45.87° = 0.696 and the SNR is reduced by $(0.696)^2$ which is 3.15 dB.[3] A typical system would implement a Costas or squaring loop to perform coherent carrier recovery and would derive its carrier term from $r(t)$. Thus this 3.14 dB loss may be reduced somewhat by the implementation of a coherent carrier recovery loop. Despite this 5 dB loss the system still performs quite well and will recover data with an approximate $P_e = 1 \times 10^{-5}$ at a SNR = −13 dB thus providing for an approximate PG = 18.5 dB. At the data rate of 62.5 bps this implies one error an average every 25.56 min. This may be optimistic, however, because VCO drift may create more errors.

[3] After the tests and data collecting described in this report were completed, an attempt was made to compensate for the phase shift of the IF BPF. Time constraints prevented collecting additional reliable data because various portions of the circuit had to be redone to achieve prior performance.


PROBABILITY OF ERROR PERFORMANCE
PROBABILITY OF BIT ERROR
10⁻²
10⁻³
10⁻⁴
10⁻⁵
10⁻⁶
LEGEND
MEASURED SYSTEM
-17.0
-16.0
-15.0
-14.0
-13.0
-12.0
-11.0
SIGNAL-TO-NOISE RATIO (DB)

(a)



(b)

Figure 58. Probability of Bit Error Curves for the DCDLL System, a) Measured Performance, b) Performance of Theoretical BPSK, and System Performance less Predicted Processing Gain.

VII. CONCLUSIONS AND RECOMMENDATIONS

A. CONCLUSIONS

A DS spread spectrum system wad designed, constructed, and tested in this research. A spreading factor of 255 is employed. This system can be used to transmit low rate digital data reliably at values of SNR much less than unity and can be implemented by a conventional AM radio system.

A single-channel delay-lock loop was built and tested. A dual- channel delay-lock loop was also built and tested and used in the despreading operation. Apart from hardware simplicity, the SCDLL provides, in practice, a noise performance advantage relative to the DCDLL; however, its application is limited to systems which are concerned only with accurate time/range information or systems which transmit preambles for clock synchronization.

B. RECOMMENDATIONS

It is recommended that this DS spread spectrum system be considered by the Department of Defense to be implemented in AM radio systems to provide a low data rate AJ/interference rejection capability.

Further design, construction, and testing should be performed to provide coherent carrier recovery, bit synchronization, and RF carrier circuitry.

Further development should be performed on the VCO to increase its stability to bring the measured performance closer to that predicted by theory.

LIST OF REFERENCES

1. Ziemer, Rodger E., and Pererson, Roger L., Digital Communications and Spread Spectrum Systems, Macmillan Publishing Company, 1985.

2. Dixon, Robert C., Spread Spectrum Systems, 2d ed., John Wiley & Sons, Inc., 1984.

3. Couch, Leon W., Digital and Analog Communication Systems, Macmillan Publishing Company, 1983.

4. Thomas, John B., Statistical Communications Theory, John Wiley & Sons, Inc., 1969.

5. Peebles, Peyton Z., Digital Communications, Prentice-Hall, Inc., 1987.

6. Shanmugam, K. Sam, Digital and Analog Communication Systems John Wiley & Sons, Inc., 1979.

7. Young, Thomas, Linear Integrated Circuits, John Wiley & Sons, Inc., 1981.

8. Sedra, Adel S., and Smith, Kenneth Carless, Microelectronic Circuits, Holt, Rinehart, and Winston, CBS College Publishing, 1982.

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