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February, 1981 MRDC41070.2QR

LSI/VLSI ION IMPLANTED GaAs IC PROCESSING

Quarterly Technical Report No. 1

For period 07/25/80 through 10/31/80

Contract No. F49620-80-C-0101

Project No. 3384-4
Rockwell International/Microelectronics and
Research Development Center
Thousand Oaks, CA 91360

Sponsored by:

Advanced Research Projects Agency (DOD)
ARPA Order No. 3384-4

Monitored by AFOSR under Contract F49620-80-C-0101

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REPORT DOCUMENTATION PAGE

READ INSTRUCTIONS BEFORE COMPLETING FORM

1. REPORT NUMBER

2. GOVT ACCESSION NO. A186522

3. RECIPIENT'S CATALOG NUMBER

4. TITLE (and Subtitle)
LSI/VLSI ION IMPLANTED GaAs IC PROCESSING

5. TYPE OF REPORT & PERIOD COVERED
Quarterly Technical Report
07/25/80 through 10/31/80

6. PERFORMING ORG. REPORT NUMBER

7. AUTHOR(s)
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8. CONTRACT OR GRANT NUMBER(s)
F49620-80-C-0101

9. PERFORMING ORGANIZATION NAME AND ADDRESS
ROCKWELL INTERNATIONAL/Microelectronics Research and Development Center
1049 Camino dos Rios
Thousand Oaks, CA 91360

10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS
ARPA Order No. 3384-4

11. CONTROLLING OFFICE NAME AND ADDRESS
Advanced Research Projects Agency (DoD)
1400 Wilson Boulevard
Arlington, VA 22209

12. REPORT DATE
February 1981

13. NUMBER OF PAGES
76

14. MONITORING AGENCY NAME & ADDRESS (if different from Controlling Office)
Air Force Office of Scientific Research
Bolling Air Force Base
Washington, DC 20332

15. SECURITY CLASS. (of this report)
UNCLASSIFIED

15a. DECLASSIFICATION/DOWNGRADING SCHEDULE

16. DISTRIBUTION STATEMENT (of this Report)
Approved for public release; distribution unlimited

17. DISTRIBUTION STATEMENT (of the abstract entered in Block 20, if different from Report)
This research was sponsored by the Advanced Research Projects Agency (DoD)
ARPA Order No. 3384-4

18. SUPPLEMENTARY NOTES

19. KEY WORDS (Continue on reverse side if necessary and identify by block number)

Semi-insulating	High Speed Logic
Ion Implantation	GaAs
IC	FET
Integrated Circuits	MESFET

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)
This report covers the first quarter of a program aimed at fully realizing the potential of GaAs for digital integrated circuits employing depletion mode MESFETs. The highlight of this first quarter is the successful operation of the 8 x 8 bit parallel multiplier having 1008 gates, fabricated from mask AR5 of a previous ARPA program. This result completes the demonstration of the feasibility of high-speed low-power LSI (> 1000 gates) GaAs digital integrated circuits. The multiply time of this circuit 5.2 ns, exceeds by far the performance of currently available multipliers.

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Other highlights of this first quarter are the successful fabrication and operation of circuits on substrate wafers grown by the liquid encapsulated Czochralski (LEC) technique, the material which is today capable of producing the large diameter wafers required by this program. Investigation of circuit reliability has begun. While successful operation at 125°C for a moderate period of time (140 hrs.) was demonstrated, degradation observed at temperatures above 200°C has been traced to ohmic contact reliability. Intensive studies of the ohmic contact metalization scheme being used today are underway and alternative metalization schemes are under consideration. Promising results from radiation hardness experiments have been obtained. The demonstration circuits to be incorporated in the first mask set have been identified, and their design and layout has begun.

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FOREWORD

The research covered in this report is carried out in a team effort having the Rockwell International Microelectronics Research and Development Center as the prime contractor with two universities and a crystal manufacturer as subcontractors. The effort is sponsored by the Defense Sciences Office of the Defense Advanced Research Projects Agency. The contract is monitored by the Air Force Office of Scientific Research. The Rockwell program manager is Fred H. Eisen. The principal investigators for each organization are:

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TECHNICAL SUMMARY

This report covers the first quarter of a program on LSI/VLSI ion implanted planar GaAs integrated circuit processing. The goal of this program is to realize the full potential of GaAs digital integrated circuits employing depletion mode MESFETs. The highlight of the first quarter is the successful operation of the 8 × 8 bit parallel multiplier (1008 gates) fabricated from mask set AR5 of a previous ARPA sponsored program. In addition to the fabrication and evaluation of 8 × 8 multipliers, processing wafers on liquid encapsulated Czochralski (LEC) material has shown excellent material uniformity. Reliability studies have begun, focused mainly on the reliability of ohmic contacts. Demonstration circuits for the first mask set of this program AR6, have been selected, and design of these circuits is in progress. Radiation hardness tests have been carried out with promising results.

Semi-Insulating Substrate Material and Ion Implantation

Evaluation of horizontal Bridgman grown semi-insulating GaAs substrates from several vendors has been carried out, with emphasis on the uniformity of pinch-off voltage attainable. Comparisons are drawn with the liquid encapsulated Czochralski material grown at Rockwell, which today appears to offer the most promising behavior in terms of uniformity. Gettering experiments and recoil implantation studies are under way and refined data on Cr redistribution after encapsulation and anneal have been obtained.

LEC Material Uniformity

One lot of AR4 and two lots of AR5 wafers were fabricated on LEC material (Cr-doped and undoped). With these 3 lots, 12 wafers have been fabricated on LEC material altogether. All these wafers exhibited excellent uniformity of dc device parameters. The lowest wafer standard deviation of FET pinch-off voltage was 41 mV, and it was observed on 2 wafers from 2 different lots. This value is very close to the best value ever observed, 35 mV. The highest standard deviation of pinch-off voltage for these 12 wafers was only 73 mV, which is still a low value, very suitable for device utilization. No appreciable difference was observed between undoped and Cr-doped material. Although a data base of 3 lots is small, the indication that the LEC material has potential for good uniformity is unmistakable. Good performance and good yield (15%) of 5 × 5 bit multipliers on the AR4 LEC wafer was also observed. Since the LEC material has relatively high dislocation density, the yield obtained for 5 × 5 multipliers on high dislocation density LEC material suggests that dislocations in critical gate areas (FET gates or diodes) do not cause circuit failure.

Reliability

While fabrication of AR5 wafers has proceeded, the investigation of device and circuit reliability and its dependence on the Schottky and ohmic metallizations have begun. Thermal stabilities of several different Schottky metals have been compared. It was verified that Ti/Au Schottky barriers could be further stabilized by adding a layer of Pt between the Ti and Au.

Therefore, Ti/Pt/Au has been implemented as the standard Schottky metallization. Devices and circuits were aged at different temperatures. Below 150°C, no significant degradation of device characteristics was observed after aging for up to 1000 hours without bias, and up to 140 hours under bias (time limited by equipment constraints). While 150°C appears to be a "safe" temperature, the devices started to degrade appreciably when aged above 200°C. The degradation was traced to deterioration of the ohmic contacts. After 5 hours at 250°C, the specific contact resistance of Au/Ge/Pt degraded from the 10^{-6} Ω cm^2 range to over 10^{-4} Ω cm^2. Several ohmic metal designs are currently under examination. Preliminary results using AuGe/Ni are very encouraging.

8 × 8 Bit Parallel Multiplier Tests

Tests of the 1008 gates 8 × 8 multiplier were conducted on the first lot of AR5 wafers. One of the circuits was found to be completely functional, including all input and output latches. More AR5 wafers (including the ones on LEC materials) will be tested soon. The highest speed of operation for the 8 × 8 multiplier (determined in the feedback loop oscillation mode) corresponds to an average propagation delay of 150 ps for a multiply time of 5.3 ns. The total power dissipation under these conditions was 2.08 W.

Radiation Hardness Experiments

Since early total dose experiments on packaged ÷8 circuits had been conducted without bias during irradiation, a new experiment was carried out at

RADC/ESE, Hanscom. A packaged ÷8 circuit was irradiated to a total dose of 2×10^7 rads while under bias. No appreciable change in operating characteristics was observed. The device was also tested under pulsed radiation, and the length of time during which device operation was upset was measured. For a pulse width of 20 ns, a 1.1×10^8 rads pulse caused a upset lasting 2 μs. This length of time increased with dose rate, reaching 40 ms for 2×10^{10} rad/s. Although very encouraging, these figures represent upper limits because in this preliminary experiment, the bias conditions were imposed by battery voltages. Lower upset durations are expected from tests in which the integrated circuits are biased favorably.*

AR6 Design

Two demonstration circuits have been selected for the first mask set (AR6). The first of these, an 8 × 8 parallel multiplier implemented with SD^2FL multiple level logic gates, was discussd in the technical proposal. This circuit will be assembled with adder cells providing 1 τ_d sum and carry delays. These faster adder circuits will provide the 16 bit product in roughly 2 ns as compared to the 5.3 ns observed on the earlier SDFL version AR5. The second circuit, a programmable code generator, was recommended by RADC/ESE as a demonstration circuit with important system applications. Both 7 bit and 8 bit generators will be included on the same chip so that a 2^{15} bit

*While this report was in press, a new measurement carried out under optimized bias conditions showed much shorter upset times. The new data will be presented in the next report.

Gold code can be created. Multiple level logic will be used in the shift register to provide maximum clock frequencies in the 1.5 to 2 GHz region. Design efforts have been initiated during the first quarter. These activities include circuit design, simulation of critical data paths, and preliminary IC layout. Simulation and layout will be completed, and digitizing of the IC layouts will begin during the next quarter.

1.0 INTRODUCTION

This report covers the first quarter of a program on LSI/VLSI Ion Implanted Planar GaAs IC Processing. As suggested by the title, the main objective of this program is to realize the full potential of GaAs digital integrated circuits by expanding and improving the fabrication and material techniques. The principal goal is to improve material and processing capabilities so that large wafers (over 2 in. diameter) can be processed in order to satisfy anticipated needs for high-speed low-power GaAs digital VLSI integrated circuits. In parallel with increasing circuit complexity and wafer size, the program is also directed toward a full investigation of circuit reliability and toward the development of processing techniques capable of attaining the highest reliability. Circuit design advancements are also planned, with the introduction and implementation of a new circuit approach, SD^2FL, which represents an expansion of the SDFL circuits to multi-level logic. Three subcontractors, the California Institute of Technology, North Carolina State University, and Crystal Specialties, Inc. are contributing to the program with their expertise in ion beam techniques, device modeling, and crystal growth, respectively.

The highlight of the first quarter of this program is the successful operation of the 8 × 8 bit parallel multiplier having 1008 gates, fabricated from mask set AR5 of a previous ARPA program.[1] This result completes the demonstration of the feasibility of high-speed low-power LSI (> 1000 gates) GaAs digital integrated circuits. The multiply time of this circuit 5.2 ns, exceeds by far the performance of currently available multipliers.

Other highlights of this first quarter are the successful fabrication and operation of circuits on substrate wafers grown by the liquid encapsulated Czochralski (LEC) technique, the material which is today capable of producing the large diameter wafers required by this program. Investigation of circuit reliability has begun. While successful operation at 125°C for a moderate period of time (140 hs) was demonstrated, degradation observed at temperatures

above 200°C has been traced to ohmic contact reliability. Intensive studies of the ohmic contact metallization scheme being used today are under way and alternative metallization schemes are under consideration. Promising results from radiation hardness experiments have been obtained. The demonstration circuits to be incorporated in the first mask set have been identified, and their design and layout has begun.

2.0 SEMI-INSULATING GaAs SUBSTRATES AND ION IMPLANTATION

This section describes research activities concerning the semi-insulating GaAs materials used as integrated circuit substrates, including their growth, characterization and use in the ion implantation process.

2.1 Bridgman Material

Although integrated circuit fabrication has been carried out with LEC grown material on an experimental basis, Bridgman-grown Cr-doped GaAs ingots continue (as in the previous ARPA program) to provide a major fraction of the substrates processed.[1] The principal supplier is Crystal Specialties, Inc., which acts as a subcontractor. In order to insure proper results in the IC fabrication process, qualification, testing and preselection of ingots continue to be required. The selection is based on (a) absence of thermal conversion during Si_3N_4 capped anneals, and (b) proper carrier density profiles obtained from representative Se implants. During this quarter 7 ingots grown by Crystal Specialties were tested. Of these, 4 proved to be qualified for ion-implantation, representing a qualification yield of 57%, in approximate agreement with the previously observed long term yield.[1] Also tested during this quarter were 2 ingots from Mitsubishi-Monsanto and one from Sumitomo, none of which qualified.

A portion of the semi-insulating ingots grown by Crystal Specialties are currently supplied as rectangular slices with dimensions approximately 1.5 × 2 in. grown in boats with square cross-section (rather than the customary semi-cylindrical cross-section). This technique, pioneered by Crystal Specialties, represents a significant advance towards the development of GaAs slices of large dimensions and standard shape (rectangular rather than round) as well as standard size obtainable using boat growth techniques.

The uniformity of substrate characteristics for the rectangular slice is an important question. It has previously been determined that the

uniformity of pinch-off voltage obtained from the Rockwell implantation process is influenced by the particular substrate used.[1] The substrate characteristics are nonuniform principally because of spatial variations in the concentration of Cr and residual impurities due to segregation effects during crystal growth. The square wafers were tested for pinch-off voltage uniformity and compared with the D shaped wafers. Our results to date indicate that the uniformity is different, but appears to be strongly ingot dependent.

The substrate uniformity may be gauged by the standard deviation σ_V of pinch-off-voltage among the test FETs fabricated across typical wafers. These test FETs are part of the process monitor test areas included on all mask sets, and are automatically tested for each wafer processed. The standard deviations obtained correspond to the variations in doping encountered for the Se implanted channel layer, over wafers of a standard size (24.5 mm × 24.5 mm). Measured values of σ_V are shown in Table 2.1-1 for both a highly uniform square ingot (ingot A) as well as for a square ingot of poor uniformity (ingot B). Values obtained for a representative D shaped ingot are shown for comparison. These results indicate that (a) the uniformity of pinch-off voltage is more strongly dominated by the substrate than the process, (b) the degree of uniformity achievable can be very high; (c) the results are ingot dependent in a way that is not currently understood. The pattern corresponding to the variations in pinch-off voltage is readily apparent in Fig. 2.1-1, which illustrates the depletion voltages measured by the C-V technique on a highly nonuniform wafer implanted with Se. A uniform gradient of depletion voltage is observed. The magnitude of the gradient observed correlates very well with the measured standard deviation of FET pinch-off voltage on processed wafers. If a linear variation depletion voltage of total edge to edge magnitude ΔV_T were observed along one of the wafer axes, it would induce a standard deviation $\sigma_V = \Delta V_T/2\sqrt{3}$.

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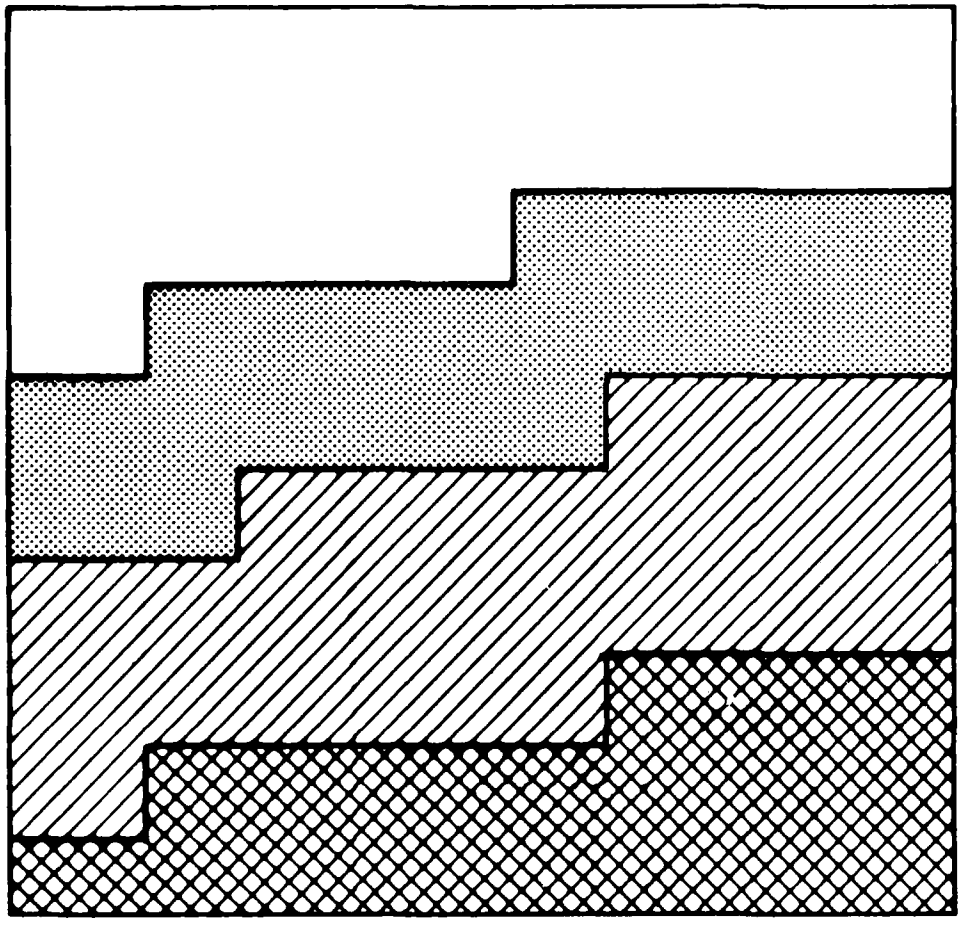

2.1-1 Measured distribution of depletion voltage over a Se implanted wafer obtained from a Crystal Specialties square ingot exhibiting poor uniformity. The sample dimensions are 1 in. × 1 in.

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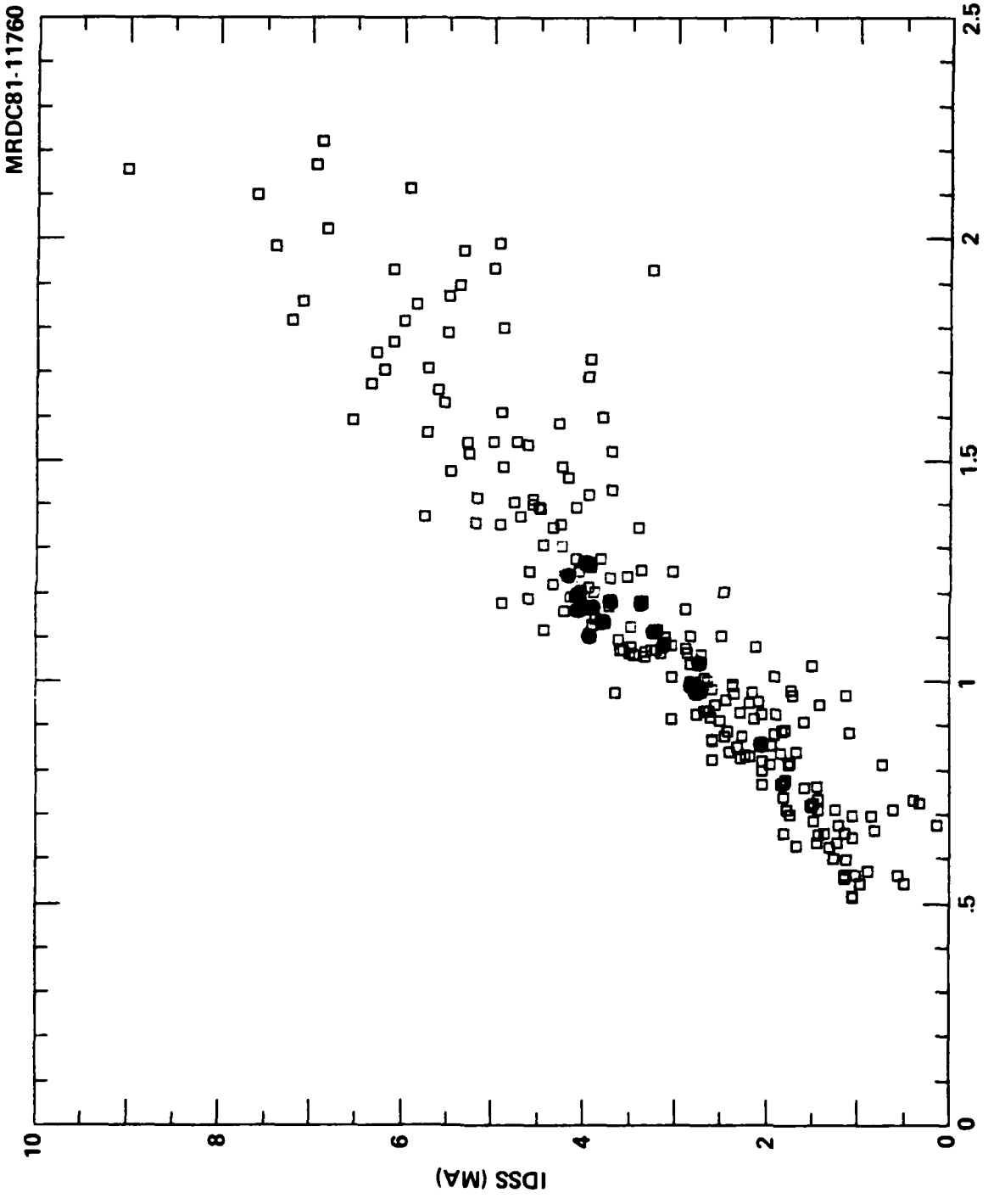
Table 2.1-1

Standard Deviations of Pinchoff Voltages Measured Across Processed Wafers from Representative Bridgman Ingots

Ingot	Shape	Quality	Standard Deviations (mV)
(A) E122	Square	Uniform	45, 62, 60, 63, 64, 130
(B) XS4570	Square	Non-uniform	165, 118, 151, 231, 320, 121, 149
(C) XS4572	D	Typical	86, 52, 103, 80, 126, 180, 200, 154, 203, 73, 93

2.2 LEC Material

Significant progress has been made at Rockwell Microelectronics Research and Development Center in the growth of GaAs ingots by the Liquid Encapsulated Czochralski technique. This effort is currently being conducted under IR&D funding. Large (2 in. and 3 in. diameter) ingots of semi-insulating GaAs have been produced, both with and without the intentional addition of Cr as a compensating impurity. A number of integrated circuit lots were processed with LEC material. DC characterization of test circuits on the process monitor areas distributed across the wafers has been completed for 3 lots fabricated under this program. The results confirm the observation made previously that the LEC substrates exhibit excellent uniformity. Table 2.2-1 illustrates the average values and standard deviations of FET pinch-off voltages obtained for the wafers of the lots. The standard deviations - as low as 41 mV - are among the lowest ever observed (the lowest attained to date is 34 mV). It is noteworthy that these results have been obtained both for ingots that were Cr doped and ingots that were grown undoped. In both cases the test FETs displayed a proper value of saturation current, in keeping with results observed using Bridgman-grown Cr-doped substrates. The similarity of current levels is shown in Fig. 2.2-1, in which measured values of saturation current (averaged over all the FETs on a wafer) are plotted vs pinch-off voltage (also averaged over the wafer) for a large number of Bridgman grown wafers obtained over a long period of time.



2.2-1 Saturation current vs pinch-off voltage for FETs fabricated on different substrates. Each point represents the average of 72 devices distributed across an entire processed wafer. The dark

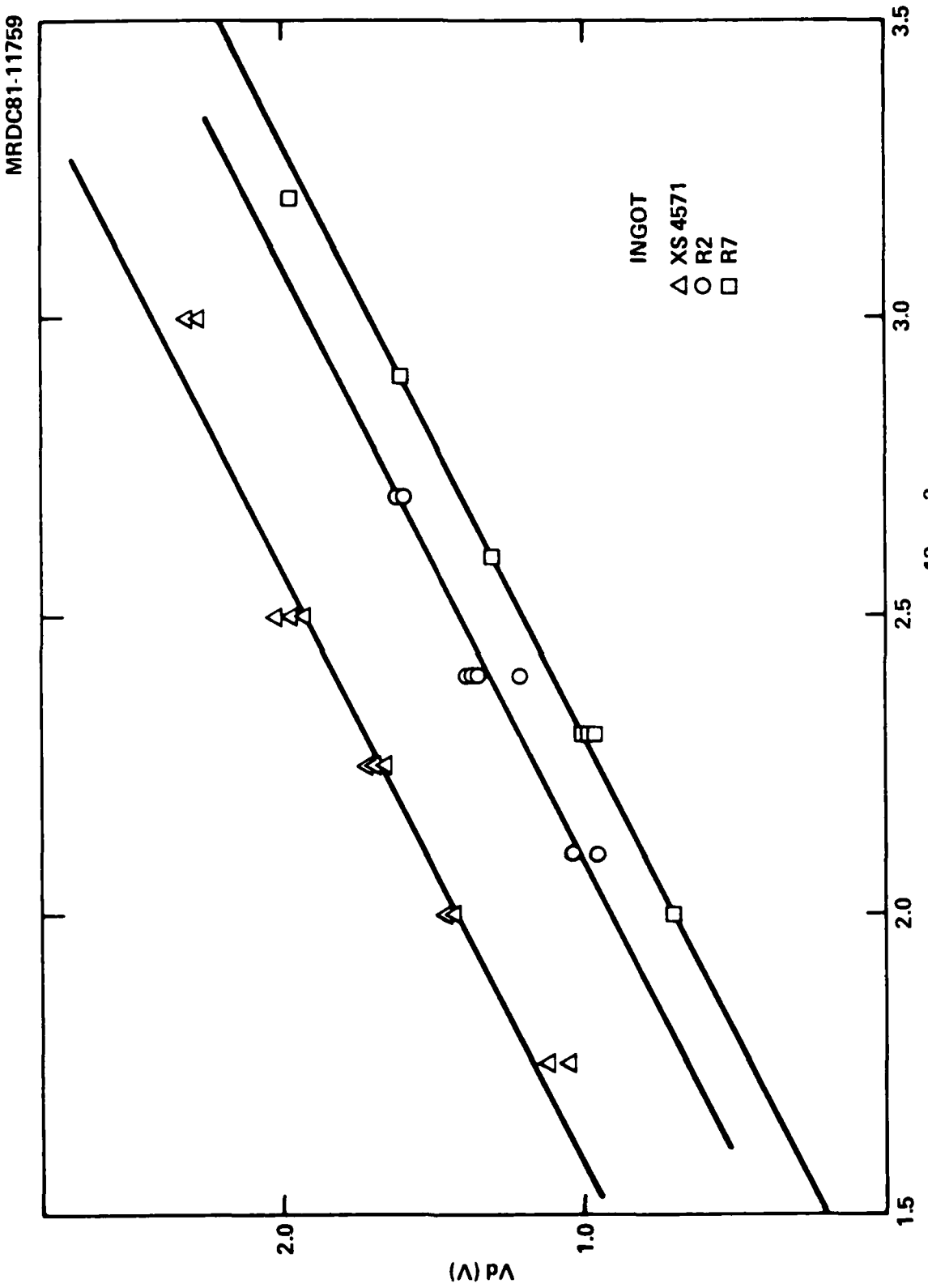
Shown for comparison are the wafer average values of saturation current with the LEC substrates.

Table 2.2-1

Mean and Standard Deviation of FET Pinchoff Voltage Measured on Wafers Processed with LEC Substrates

Lot	Ingot	$\bar{V}$ (V)	σ_V (mV)
AR4-8	R4 (Cr doped)	1.08	48
		1.12	69
		0.99	56
		1.18	73
AR5-6	R5 (Cr doped)	0.99	62
		1.26	41
		1.18	64
AR5-8	R2 (undoped)	1.04	66
		1.18	47
		1.13	42
		0.85	41

It was previously reported that the carrier density obtained with low dose Se implants was higher in the Bridgman grown substrates than in the LEC substrates. As a consequence, it is typically necessary to use a slightly higher implant dose in order to achieve a desired value of pinch-off voltage with the LEC substrates. It is of interest to determine the reason for this difference. One possible explanation is that a smaller fraction of the implanted donors may be electrically active in the LEC substrates. This hypothesis is effectively ruled out, however, by the data shown in Fig. 2.2-2, where the depletion voltage V_d that resulted for a series of Se implants is plotted vs implant dose for two LEC ingots and a representative Bridgman



2.2-2 Measured depletion voltage as a function of Se implant fluence for several substrates. The data indicate constant Se activation but variable contributions of residual donors or compensating centers for the substrates.

ingot. The values of V_d scale linearly with dose, with the same slope (~ 1 $V/10^{12}$ cm^{-2}) for all the materials. This is the result expected for comparable activation of the Se in all the substates. The offset in V_d is produced by a constant (dose independent) component of $N_{dr} - N_{ar}$ (where N_{dr} and N_{ar} are residual donor and acceptor concentrations) which differs among the substrates. The presence of a component N_{dr} due to residual Si in the Bridgman grown ingots has been previously discussed.[1] There may also be a slight net acceptor component N_{ar} in the LEC material, although further work is needed for its characterization.

2.3 Ion Implantation Research

Research was done in a number of areas of interest for the ion implantation process in GaAs. These topics include gettering, recoil implantation, Cr redistribution, and deep level spectroscopy studies.

(a) Gettering. The removal of substrate impurites by gettering processes in Si is well known. Recently the efficacy of gettering in GaAs has also been demonstrated, using implantation induced damage[2] and mechanically induced damage.[3] Of the two techniques, the mechanical damage appears to be the most stable.[3] An experiment has begun in collaboration with Dr. T. Magee of ARACOR, who has carried out pioneering work on gettering in GaAs. In the experiment currently under way, backside mechanical damage will be produced on a variety of wafers, including Bridgman high Cr wafers, Bridgman moderate Cr wafers, and LEC (undoped) wafers. For a number of substrates, the damage and

subsequent gettering anneal will be carried out prior to wafer polishing. On others, the backside damage will be carried out after polishing and the wafers will be processed in the standard fashion, relying on the standard post-implant anneal to accomplish the gettering. Ungettered control wafers will be simultaneously processed. The effects of gettering will be assessed with C-V measurements and Hall measurements on Se implanted FET channel layers.

(b) Recoil Implantation. Further measurements were made using the SIMS technique to ascertain the density of Si atoms that are recoil-implanted into GaAs substrates when Se ions are implanted through thin Si_3N_4 layers. Results previously obtained[1] suggested that the concentration and distribution of the Si atoms were very similar to the results predicted by L. Cristel and J. Gibbons of Stanford University,[4] although the measured density was lower by a factor of 2-2.5. The more recent measurements have reduced this discrepancy; they indicate a measured density low by a factor of about 1.6. Since this is close to the estimated accuracy of the measurement techniques, the results are consistent with complete agreement of theory and experiment. The slightly lower measured value earlier results were probably affected by slight etching of the GaAs surface during the removal of the encapsulant.

(c) Cr Redistribution. Detailed studies have been carried out of the profiles of Cr obtained after annealing Si_3N_4 encapsulated GaAs substrates. The Cr outdiffusion has previously been shown to have a significant role in thermal conversion phenomena as well as in determining the carrier

density profiles observed for low dose donor implants.[1,5] The Cr diffusion characteristics are also of interest in terms of understanding the behavior of impurities and native defects in GaAs during capped anneals. The studies have shown the following: (a) the profile shapes differ somewhat from the error function expected from simple diffusion. The effective diffusion coefficient (as obtained from an approximate Boltzmann-Matano analysis) is higher by ~ x2 in the first 0.5 μm than in the bulk. (b) The profiles do not scale precisely according to the square root of diffusion time. (c) The effective diffusion coefficients vary by as much as a factor of 3 among different GaAs substrates. (d) There is no significant effect of encapsulant thickness (or thus encapsulant stress) on the profile shape, for Si_3N_4 thickness in the range 500-1000 Å. (e) There is anomalous very rapid diffusion of Cr during the Si_3N_4 deposition process. The observed features of the Cr diffusion suggests the participation of native defects in the diffusion process. Efforts to model the process are under way.

(d) Deep Level Studies. Studies of electron traps in Bridgman-grown GaAs and of the changes in their concentration and distribution as a result of encapsulation with Si_3N_4, annealing and ion implantation have been carried out in collaboration with Prof. K. Wang of UCLA. The effort at Rockwell is funded under an IR&D program, and results are summarized here because of their relevance to this program. Among the results are the following: (a) In Crystal Specialties as-grown undoped substrates (which are lightly n-type) a number of electron traps are present in concentrations above 10^{14} cm^{-3}; the principal

ones are EL2 (with E_{act} = 0.83 eV, concentration 5-10 × 10^{15} cm^{-3}), EL3 (E_{act} ≈ 0.59 eV, density 1-5 × 10^{15} cm^{-3}) and EL6 (E_{act} ~ 0.35 eV, density 3-8 × 10^{15} cm^{-3}). These traps are well known in the literature but their chemical nature is undetermined.[6] (b) Several traps are introduced during the Si_3N_4 deposition process (in concentrations of ~ 10^{14} cm^{-3}) presumably due to damage of the GaAs surface during the initial phases of sputtering. (c) All the traps, both grown-in and introduced later, anneal out with subsequent thermal treatment. Several characteristic temperatures (annealing stages) appear to be present. The EL2 trap (E_{act} = 0.83 eV) anneals out at the highest temperature (~ 850°C). As the traps annealed out their distribution changes reflecting outdiffusion from the bulk, and pile up at the surface. As a result of an 850°C 30 min Si_3N_4 capped anneal the GaAs region at depths between about 0.1 and 1.0 μm is virtually free of electron traps. (d) Samples implanted with Se ions tend to show slightly higher densities of the EL2 trap, with peak concentration at approximately the depth of the implant damage (~ 0.03 μm). Se implants carried out before or after capping give essentially the same results (although a small concentration of traps at E_{act} ≈ 0.32 eV is visible only in the latter samples).

3.0 CIRCUIT FABRICATION

While planning for the fabrication of large (> 2 in.) wafers is under way, progress is reported here in two areas of circuit fabrication. The first one (Section 3.1) corresponds to the successful fabrication of wafers on liquid encapsulated Czochralski (LEC) substrate materials. The importance of this work stems from the need to fully evaluate, as quickly as possible and on real circuits the LEC material capable of providing the large wafers required by this program. The second area of circuit fabrication addressed in this report is reliability. Work identifying the ohmic contacts as the limiting factor of the reliability achieved today is presented in Section 3.2.

3.1 Fabrication of Circuits on LEC Wafers

While characterization of LEC semi-insulating GaAs has been carried out rather extensively and has been reported previously[1,7] (see also Section 2.2), this section covers the results of integrated circuit (IC) fabrication on LEC substrates.

One lot of LEC wafers was fabricated using a mask set AR4 of the previous ARPA program, and two lots were fabricated using mask set AR5 of the same program.[1] This represents a total of 12 wafers fabricated on LEC substrates. The fabrication of these wafers proceeded very normally. No departure from the behavior of the Bridgman material has been observed and no special fabrication procedures were required, with the exception of the

slightly different implant dose needed by the LEC material, discussed in Section 2.2.

The uniformity of FET pinch-off voltage observed was exceptionally good, however. The pinch-off voltages of test FETs exhibited standard deviations σ_{Vp} which ranged between 41 mV and 73 mV (see Section 2.2 for details). These values are very good. The lowest σ_{Vp} ever observed is 34 mV. Not only the standard deviations were in general quite low, but they were low for all the wafers. This observation is very encouraging since high uniformity will be required when large wafers are processed.

The FET and diode characteristics were virtually identical to those of devices fabricated on Bridgman material. The 5 × 5 bit parallel multiplier circuits were evaluated on one of the wafers from mask set AR4. The performance of these circuits was found to be as good as that of multipliers previously tested on Bridgman substrate wafers (190 ps/gate propagation delay, 134 fJ power delay product).[1] The yield of fully operational circuits was also high, 15%. An interesting observation is that the dislocation density of the LEC substrate determined by etch pit count was 20,000 cm^{-2}. If the critical device areas of the SDFL gates (FET gates and diodes) in the multiplier are added up, the probability of finding a dislocation in one of such critical areas turns out to be high ~ 90%. If such dislocations were capable of causing circuit failures, the yield of 5 × 5 multipliers would be 0. Therefore, this is the first supporting evidence to the idea that dislocations under FET gates or diodes do not necessarily cause circuit failure.[8]

In summary the results obtained from LEC substrates are encouraging. More of this material will be used in the near future so that the data base on device and circuit performance will be expanded.

3.2 Metallization Reliability

One of the major factors for achieving good and reliable GaAs integrated circuits is to have a good Schottky and ohmic metallization system. Unlike Si integrated circuits where high quality poly-silicon and metal silicides are easily formed, GaAs integrated circuits depend strictly on metals to form Schottky or ohmic contacts. Although much work on various metallization systems has been done in the past, a clear understanding of the GaAs-metallurgical interaction leading to a standard recipe for the industry to follow is still yet to be established. Also, the reliability of the metallization systems and its impact on the device performance of GaAs ICs is not fully understood. During the final phase of the previous ARPA process development program,[1] the processing techniques had been fully determined and the processes stabilized to a level of maturity that allowed us to begin to evaluate the reliability of the fabricated ICs. During this initial reporting period of the current program extensive reliability studies have been started, with the initial results reported here.

The initial goals of the reliability work were to establish the reliability status of our devices and metal systems, and to find out what the degradation mechanisms were, and to initiate corrective actions. Accelerating

aging techniques with thermal stress have been initially used for this study with further work on ICs aged under bias conditions planned.

As a starting point, 9-stage 10 μm NOR gate ring oscillators were chosen for the circuit reliability test. These circuits were fabricated using AuGe/Pt ohmic contacts and Ti/Au Schottky barrier metallization. The circuits were tested under bias at 125°C, the upper limit of the mil spec range, in air ambient. No degradation in operating frequency and power dissipation were observed up to 140 hours of continuous operation (time limited by equipment constraints). Characteristics of FETs and diodes after thermal aging were also measured using our automatic probing system.[1] Table 3.2-1 shows the results obtained from one of our standard IC wafers which was cut into two halves with one section thermally aged at 240°C and the other section heated at 150°C. Both heat treatments were done in air ambient. The characteristics of FETs and logic diodes were measured at different stages of the heat treatment using the standard T2 test patterns which are uniformly distributed on the wafers.[1] Each number on the table is the average representing the average values and standard deviations of the measured parameters for 36 devices. At 150°C no degradation was observed on the FETs even after 1000 hours of heat treatment. The average values of V_p, I_{dss}, and R_{on} remained nearly constant during this test. The series resistance of the diodes remained the same after 500 hours but increased slightly after 1000 hours. This is probably an indication of the onset of ohmic contact degradation. At 240°C the degradation of the FETs and the diodes can be clearly seen even after only few hours of heat treatment. It is interesting to note that although the current (I_{dss}) and the

Table 3.2-1 Characteristics of FETs (50 μm wide) and Diodes After Aging.

MRDC81-11564

		BEFORE HEATING	240°C 2 HOURS	240°C 4 HOURS
FET	V_p (V)	1.036 ± .1	.9827±.102	1.009 ±.0984
	I_{DSS} (MA)	3.024 ± .411	2.469 ± .436	2.415 ± .445
	Ron (Ω)	204.9 ± 35	256.8 ± 48.5	276.7 ± 51.9
DIODE	Rs (Ω)	697.3 ± 105	1243 ± 388	1434 ± 481

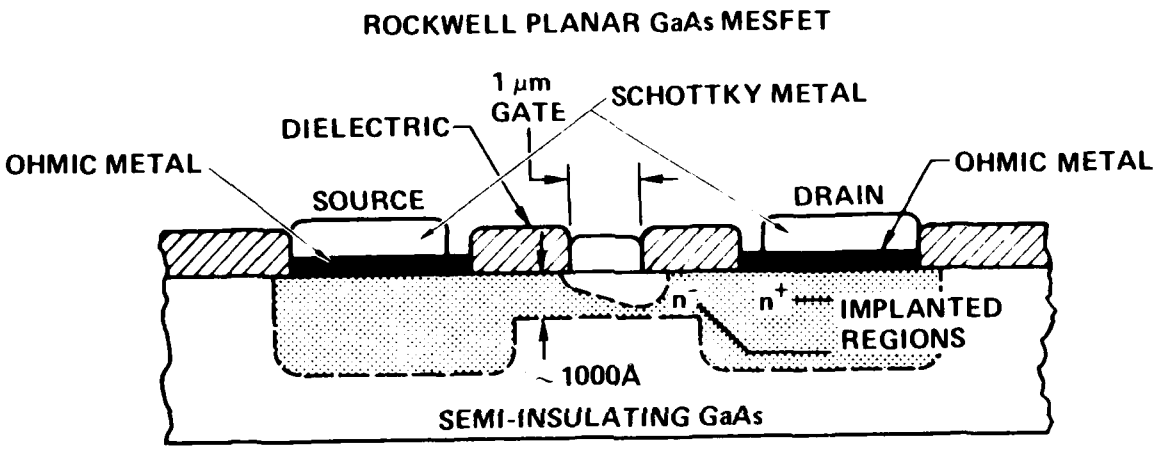
		BEFORE HEATING	150°C 124 HOURS	150°C 335 HOURS	150°C 502 HOURS	150°C 983 HOURS
FET	Vp (V)	.9988 ± .0501	1.011 ± .0576	1.007 ± .0794	1.02 ±.0614	1.05 ± .0622
	I_{DSS} (MA)	2.991 ± .233	2.833 ± .386	2.908 ± .262	2.99 ± .263	3.088 ± .33
	Ron (Ω)	203.7 ± 31.9	209.9 ± 52.2	197.8 ± 20.2	190.8 ± 16	190.1 ± 18.1
DIODE	Rs (Ω)	675.8 ± 110	680.9 ± 105	701.9 ± 109	679.5 ± 107	732.9 ± 138

resistances (R_{on} and R_s) have degraded, the pinch-off voltage (V_p) remains stable. This suggests that the TiAu Schottky barrier is much more reliable than the ohmic contacts, and the major reason for the device degradation is deterioration of ohmic contacts.

Ohmic contact reliability studies were conducted on test structures similar to the cross section of the metallization system for our standard FETs shown in Fig. 3.2-1. The ohmic contacts in the source and drain area consist of two layers of metals. The first layer is the alloyed ohmic metal, AuGe/Pt; the second layer is Ti/Au, which is the same metal used for the Schottky barrier gates.

In order to obtain direct measurement of the ohmic contact resistance an improved TLM test structure which utilizes several ohmic gaps with different gap lengths was included in AR5 mask set (designed and fabricated on the previous program).[1] This specific contact resistance (γ_c) structure is repeated so that a statistical sample size of 72 can be obtained from each wafer. The contact resistance of several wafers was monitored at frequent intervals during thermal aging tests, and these results were correlated with the device and circuit performance data.

The conclusion reached is that AuGe/Pt by itself forms excellent ohmic contact with GaAs, exhibited by low contact resistance and good morphology. Table 3.2-2 shows the specific contact resistance of AuGe/Pt contacts at different stages of aging at 250°C up to 300 hours. Little or no degradation was observed.



3.2-1 Cross section of the standard depletion mode GaAs MESFET used in SDFL logic.

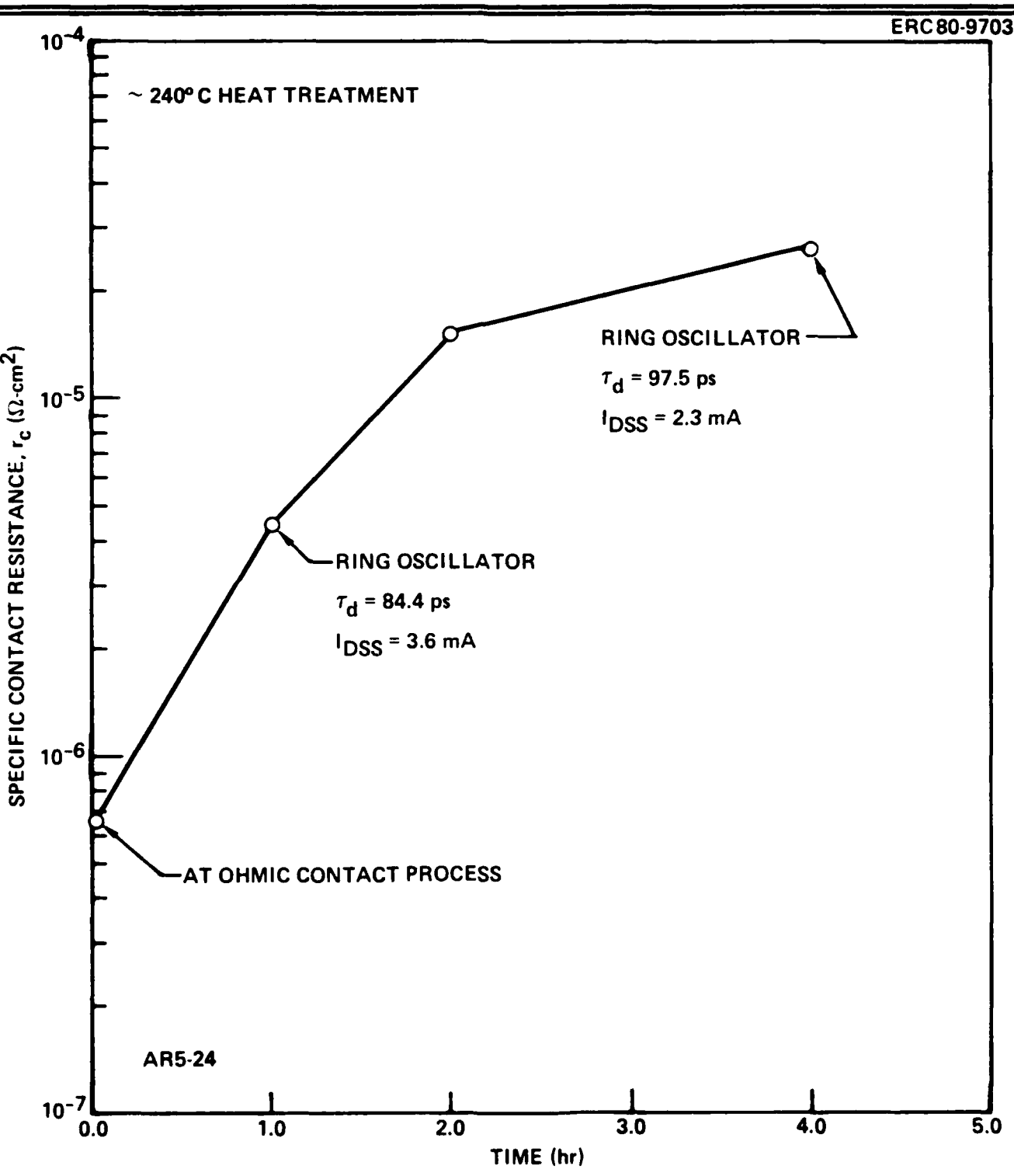
Table 3.2-2 Specific Contact Resistance ($\Omega\,cm^2$) of AuGe/Pt Ohmic Contacts (without Schottky overlay) Heat Treated at 250° C.

AS ALLOYED	2 HOURS	10 HOURS	50 HOURS	150 HOURS	300 HOURS
4×10^{-6}	7.3×10^{-6}	7.7×10^{-6}	5.6×10^{-6}	4.6×10^{-6}	4.9×10^{-6}

The effect of varying the doping concentration (over a limited range) on the contact resistance has also been studied. The dose of n^+ sulfur implant was varied over a range of sheet resistance from 250 Ω/□ up to 750 Ω/□. (Our typical sheet resistance is ~ 500 Ω/□). Table 3.2-3 shows the specific contact resistance and their reliability data corresponding to 4 different doses. It is clear from the data that γ_c is independent of the sheet resistance over this range and it is stable to 240°C.

It is important to note the reliability data of the ohmic contacts presented in Table 3.2-3 are obtained from AuGe/Pt contacts without Schottky metal overlay. When AuGe/Pt is covered by Schottky metal, a step necessary for circuit inter-connection, the contacts start to degrade very rapidly. Fig. 3.2-2 shows the thermal aging behavior of the contact rtesistance for contacts with a Ti/Au overlay. In only several hours of aging at 240°C, the specific contact resistance increased from high 10^{-7} Ω-cm^2 to more than 10^{-5} Ω-cm^2. Device degradation is also apparent from the decrease in the average I_{dss} of 50 μm FETs and the increase in propagation delay time measured from ring oscillators. Several other Schottky overlay metals such as Ti/Pt/Auand TiW/Au have been tried, but the thermal degradation results were similar indicating that Ti/Au overlay is not the problem, and the AuGe/Pt contact system itself must be suspected.

Experiments using more reliable ohmic contact metal schemes have been planned and are currently in progress. Preliminary results obtained from AuGe/Ni contacts look very encouraging. This system shows very good thermal stability with or without Schottky overlay. More complete reliability data of this contact will be available in the next report.



3.2-2 Reliability of AuGe/Pt ohmic contact with Schottky metal overlay.

Table 3.2-3 Thermal Reliability of AuGe/Pt Contacts* vs Sulfur Implant Dose.

DOSE \ TIME	AS ALLOYED	240°C, 1 HR	4 HR	16 HR	64 HR
SULFUR 1.7×10^{13} cm^{-2}	$\bar{r}_c = 1.6 \times 10^{-6}$ Ω-cm^2 $\bar{\rho}_s = 263$ Ω/□	1.3×10^{-6} 261	1.2×10^{-6} 260	1.3×10^{-6} 260	1.3×10^{-6} 262
1.3×10^{13}	1.9×10^{-6} 309	1.4×10^{-6} 306	1.2×10^{-6} 307	1.3×10^{-6} 304	1.3×10^{-6} 306
→ 9×10^{12}	1.4×10^{-6} 493	1.2×10^{-6} 492	0.9×10^{-6} 508	1.1×10^{-6} 508	1.2×10^{-6} 504
5×10^{12}	2.1×10^{-6} 763	1.4×10^{-6} 754	1.2×10^{-6} 762	1.7×10^{-6} 740	1.8×10^{-6} 763

*NO OVERLAY METAL

As mentioned earlier the Schottky metal in our process is more reliable than the ohmic contacts. In order to observe degradation, higher thermal aging temperatures were required. Samples with various Schottky metals were aged at several different temperatures and different time intervals. The Schottky barriers were characterized by I-V measurements; the ideality factor (n) and the Schottky barrier height (ϕ_B) were determined using the thermionic-emission model. Table 3.2-4 shows a comparison between Au, Pt/Au, Ti/Au and Ti/Pt/Au. Above 400°C all of these metal systems started to degrade. The degradation of Au is evident even at 320°C. The other three retained good diode characteristics at 320°C for two hours of aging. However, the barrier height of Pt/Au decreased, and the barrier height of Ti/Au increased.

This behavior can be explained by the diffusion of Au through the thin Pt and Ti layers. As Au reaches the GaAs surface the Schottky barriers no longer behave like Ti or Pt barriers but like Au barriers, Au having a barrier higher than Ti and lower than Pt. The data indicate that the Ti/Pt/Au Schottky barrier is more stable than Ti/Au and Pt/Au when heat treated at 320°C. Since the Pt layer is sandwiched between Au and Ti, it acts as an Au diffusion barrier preventing Au from reaching the GaAs surface. In order to study the effectiveness of the Pt barrier, Ti/Pt/Au Schottky diodes were fabricated with different thicknesses of Pt and aged at 240°C and 320°C. The electrical results are shown in Table 3.2-5. The thicker the Pt layer is, the more stable the barrier height, although the difference is not very significant. However when the Pt layer is thicker, the Schottky metal processing

Table 3.2-4 Comparison of Schottky Barrier Between Au, Pt/Au, Ti/Au and Ti/Pt/Au.

SCHOTTKY METAL	AS DEPOSITED	320° C 2 HRS	400° C 2 HRS	500° C 2 HRS
Au 1500Å	η = 1.01 ϕ_B = 0.873 eV	1.21 0.682	1.18 0.688	BAD DIODE
Pt/Au 300/1000Å	1.03 0.962	1.06 0.908	2.18 0.75	BAD DIODE
Ti/Au 300/1000Å	1.02 0.777	1.04 0.878	1.2 0.796	BAD DIODE
Ti/Pt/Au 300/300/1000Å	1.032 0.775	1.033 0.776	SCATTERED DATA	BAD DIODE

η (IDEALITY FACTOR)

ϕ_B (BARRIER HEIGHT)

Table 3.2-5 The Effect of the Pt Layer on the Reliability of Ti/Pt/Au Schottky Barriers

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SCHOTTKY METAL	AS DEPOSITED	240° C		320° C	
		25 HR	125 HR	2 HR	8 HR
Ti/Au 300/2700Å	η = 1.07 ϕ_B = 0.774	1.08 0.811	1.174 0.844	1.12 0.856	1.4 0.787
Ti/Pt/Au 300/300/2400Å	1.03 0.762	1.06 0.79	1.05 0.793	1.07 0.799	1.06 0.813
Ti/Pt/Au 300/600/2100Å	1.05 0.777	1.07 0.78	1.04 0.787	1.08 0.79	1.15 0.78
Ti/Pt/Au 300/900/1800Å	1.06 0.744	1.08 0.785	1.12 0.781	1.09 0.782	1.06 0.794

η (IDEALITY FACTOR)

ϕ_B (BARRIER HEIGHT)

step is more difficult because of the stress induced by the high density Pt film and the heat generated during evaporation. Based on these experiments, Ti/Pt/Au with thicknesses of 300 Å/300 Å/2400 Å was recently incorporated into our GaAs IC process replacing the simple Ti/Au used previously. Futher experiments addressing the process yield trade-offs associated with increasing one or both of the Ti and Pt metal thicknesses will be conducted.

4.0 CIRCUIT EVALUATION

This section contains a discussion of the results from testing the 8 × 8 bit parallel multiplier showing successful operation of the circuit. Although this circuit was described in the final report of the previous program,[1] where partial operation was reported, a full description of the circuit and the tests performed is included in Sec. 4.1 for completeness. Encouraging results from radiation hardness experiments on frequency dividers are presented in Sec. 4.2.

4.1 8 × 8 Bit Parallel Multiplier Evaluation

A particularly attractive candidate for a representative combinatorial logic circuit is a parallel multiplier, since multiplication frequently represents a bottleneck in signal processing and computer systems. Typical sizes for a high-speed parallel multiplier would be 8 x 8 bits or 16 x 16 bits, with larger products formed of combinations of these. A straight parallel multiplier, N x N bits, without carry lookahead and not using more complex (e.g., Wallace tree) approaches, requires N(N-2) full adders and N half adders in its implementation, and requires a total of (N-1) sum delays plus (N-1) carry delays to obtain the product.

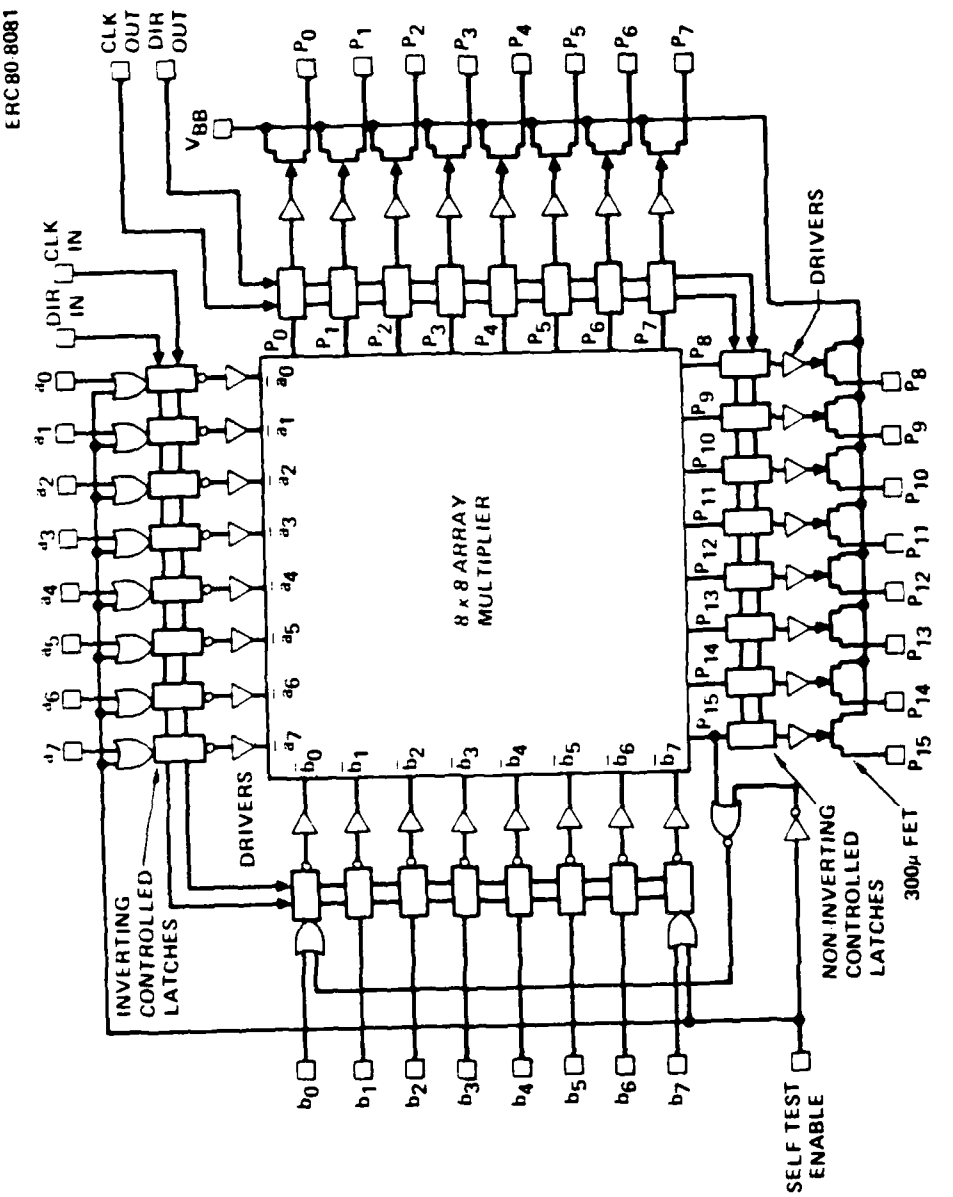
An 8 x 8 multiplier was designed as a 1000 gate demonstration circuit in the last phase of a previous ARPA GaAs IC program.[1] The circuit forms the 16 bit product of two 8 bit input numbers. The multiplication is done in paralley by a proper combination of 48 full adders and 8 half adders, and the

input and output words can be latched, or the input can be entered directly under external control. Control of the latching, as well as the clocking, is separate for input and output. An externally activated feedback self test connection is included, similar to the one on the 3 x 3 and 5 x 5 multipliers. A block diagram is shown in Fig. 4.1-1.

The outputs of the array go through non-inverting controlled latches, to drivers, and then to output FETs. The non-inverting controlled latch is essentially a D flip-flop with a bypass capability to allow for asynchronous testing. When the direct control line is a one, or high, the input is routed to the output through two gates. When the direct control line is low, the input becomes latched under control of the clock, in normal D flip-flop fashion. The inverting controlled latch is just a modification of the non-inverting one.

The inputs to the 8 × 8 array are introduced through the 16 inverting controlled latches and complementary drivers. The drivers are required to drive the considerable capacitance of the array; by implementing them in complementary form, dc power is minimized. The latch outputs drive bit lines which drive NOR gates used to form partial products $\overline{a}_j + \overline{b}_k = a_j \cdot b_k$. These latches can also be bypassed to allow for asynchronous testing.

The self-test feedback circuit is activated by holding the enable line high. This applies logic "1" to all a_j lines and to b_7. It also applies the complement of output bit P_{15} to b_0. This connection is unstable, as can be seen from the multiplication:



4.1-1 Block diagram of the 8 x 8 parallel multiplier. Self test feedback path is shown on this figure.

$$
\begin{array}{r}
A = 1\ 1\ 1\ 1\ 1\ 1\ 1\ 1 \\
B = 1\ 0\ 0\ 0\ 0\ 0\ 0\ b_0 \\
\hline
b_0 b_0 b_0 b_0 b_0 b_0 b_0 b_0 \\
1\ 1\ 1\ 1\ 1\ 1\ 1 \\
\hline
b_0 \bar{b}_0 \bar{b}_0 \bar{b}_0 \bar{b}_0 \bar{b}_0 \bar{b}_0 \bar{b}_0 b_0 b_0 b_0 b_0 b_0 b_0 b_0 b_0
\end{array}
$$

Changing bit b_0 (from 1 to 0 or 0 to 1) involves the longest delay path through the multiplier array, as can be seen from Fig. 4.1-1. Since the delay to a sum output for an SDFL NOR implemented adder is $3\tau_d$ and for a carry is $2\tau_d$, the delay to the most significant product bit (P_{15}) is 6 sums and 8 carries for a total of $34\tau_d$. Adding the control and latch gates, the self test mode causes the multiplier to self oscillate with half-period of $\sim 40\tau_d$.

Operation is therefore possible in three modes; with inputs and outputs unlatched (straight parallel multiplier); with inputs and/or outputs latched and independently clocked; and in an oscillatory self test mode. The 8 x 8 multiplier clearly represents an LSI chip. The array multiplier has 688 gates and the latches add 256 for 944. Including driver and control gates, the total is 1008. The complete 8 × 8 parallel multiplier circuit was placed in a 2.7 mm × 2.25 mm chip area including bonding pads. A photograph of a multiplier chip is shown in Fig. 4.1-2.

The 1008 gate, 8 × 8 multiplier circuit has been evaluated at wafer probe for logic functionality of all sections of the circuit and for high speed performance. A MACSYM II (Analog Devices) automatic data acquisition system has been used in conjunction with an Electroglas wafer probe station to

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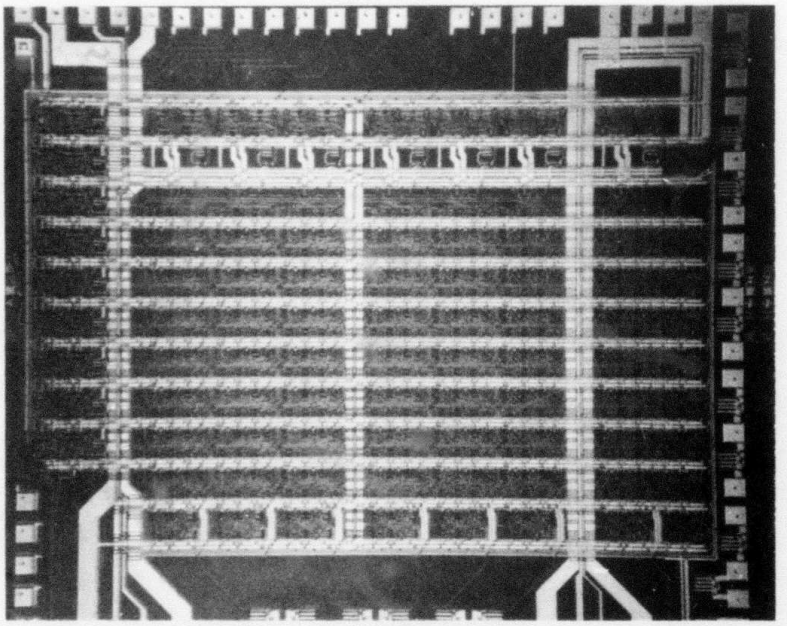
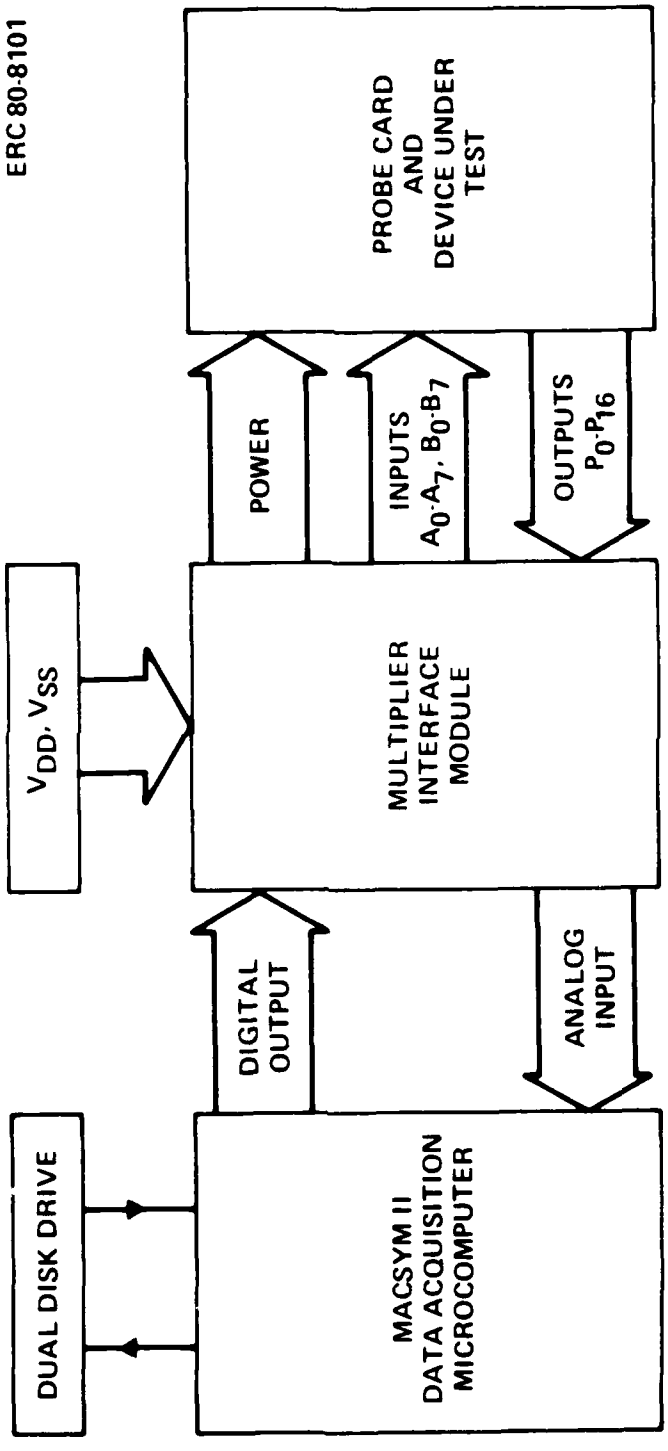


Fig. 4.1-2 Photomicrograph of an 8 x 8 multiplier chip. The chip including bonding pads covers a 2.7 mm x 2.25 mm area.

perform the automatic testing of the multiplier.[1] The data acquisition system contains a 16-bit microcomputer with a dual storage and digital as well as analog I/O capability. Software and hardware were developed so that the performance of the multiplier chip could be evaluated for all 64 possible input combinations.[1] Figure 4.1-3 shows a block diagram of the test setup using the MACSYM II system. All product outputs are monitored and stored on disk by the MACSYM. The output voltage levels are decoded into logic states and compared with the results of the calculated binary multiplications for the specific input states. If the results do not match, error codes are generated.[1]

On the wafers evaluated during the reporting period, one totally functional multiplier chip has been identified with many others operating with all but one or two gates performing correctly. Figure 4.1-4 shows the performance of the 8 × 8 multiplier in an unlatched (asynchronous) ripple test where the product 255 × 128 is being performed with a pulse applied to the b_0 input. The output product bits P_0 to P_{15} are shown to have the proper relationship to the b_0 input in this figure. Power dissipation ranged from 0.62 to 2.2 W total for the pinch-off voltage range (V_p = -0.9 to - 1.6 V) evaluated to date.

Figure 4.1-5 depicts the performance of the multiplier circuits operating synchronously with input latch control. A b_0 data input was derived from the clock waveform by a TTL frequency divider such that the data edge transitions were no longer coincident with all of the falling clock edges. This makes the DFF latch functionality evident by comparing the product output



4.1-3 Block diagram of the automatic test setup using the MACSYM II data acquisition system.

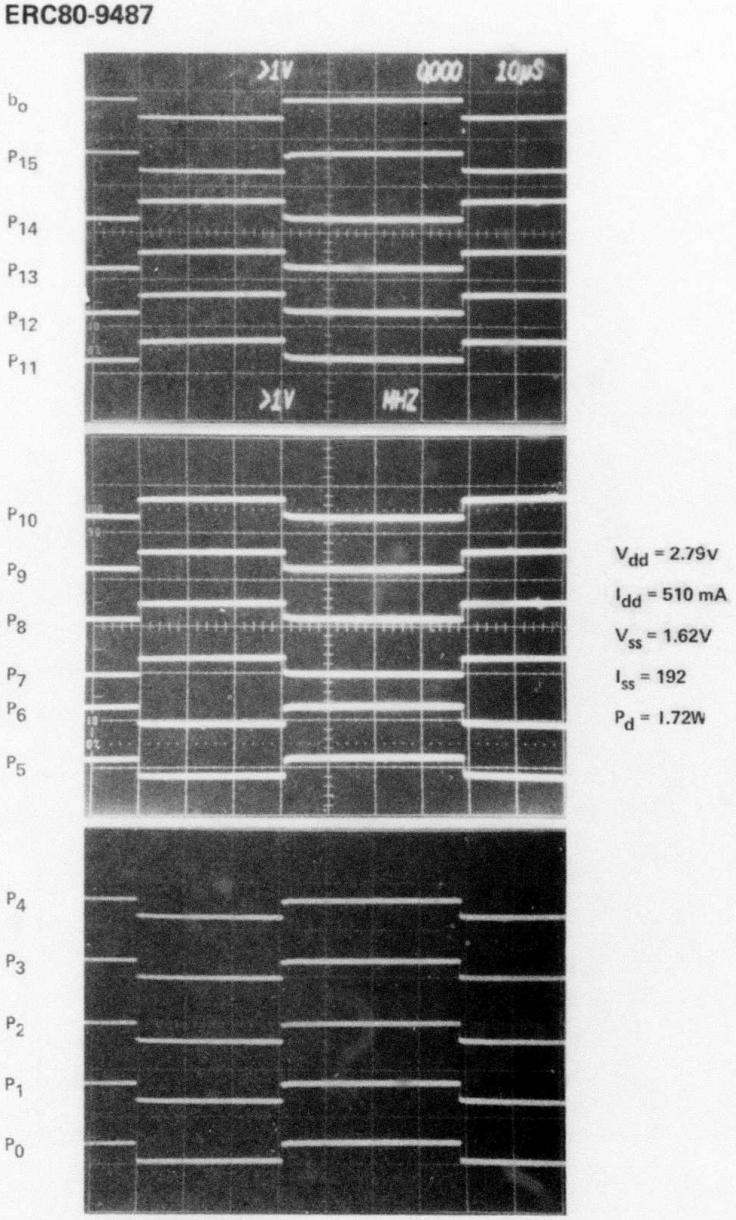


Fig. 4.1-4 Ripple (asynchronous) test of 8 x 8 multiplier with pulse input at b_0.

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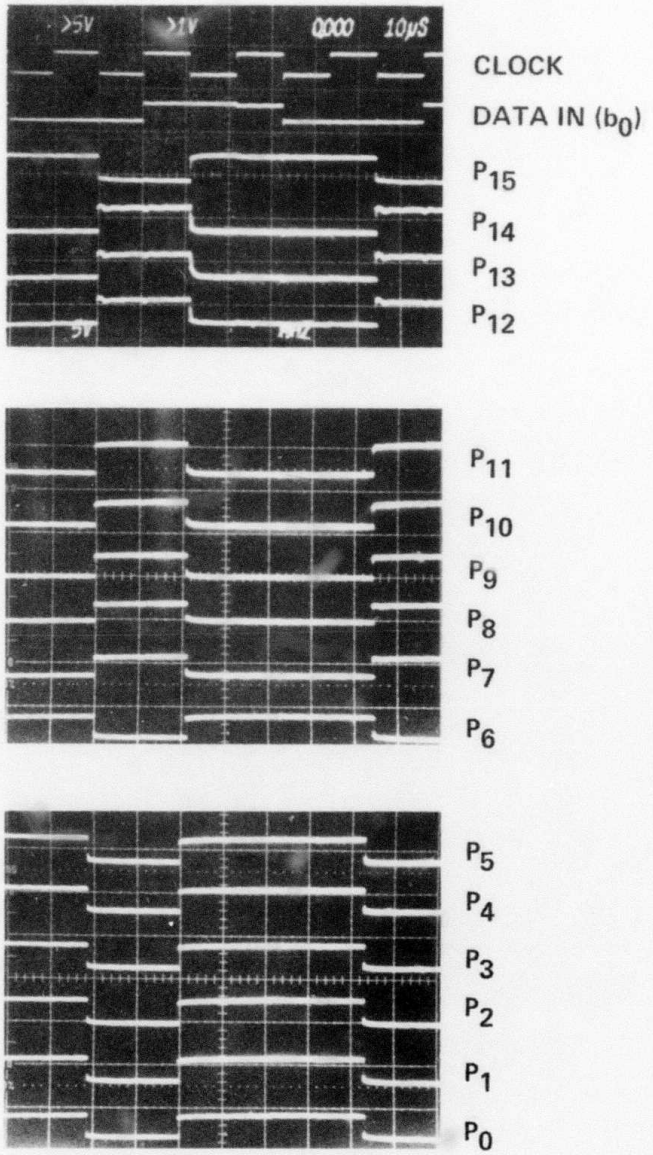

255 x 128

$$
\begin{array}{r}
 & & & & & & & & 1\ 1\ 1\ 1\ 1\ 1\ 1\ 1 \\
\times & 1 & 0 & 0 & 0 & 0 & 0 & 0 & b_0 \\
\hline
 & & & & & & & & b_0\ b_0\ b_0\ b_0\ b_0\ b_0\ b_0\ b_0 \\
+ & 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 \\
\hline
 & b_0 & \bar{b}_0 & b_0 & \bar{b}_0 & b_0 & \bar{b}_0 & b_0 & \bar{b}_0\ b_0\ \bar{b}_0\ b_0\ \bar{b}_0\ b_0\ \bar{b}_0\ b_0\ \bar{b}_0
\end{array}
$$

Fig. 4.1-5 Performance of 8 x 8 multiplier when data input is controlled by the input latches. Note that the output transitions are now synchronous with the falling clock edge.

transitions with the clock and data inputs. The output latches performed in a completely analogous manner.

High speed performance evaluation was carried out using the on-chip feedback path. The latches were operated with the direct control line high (logic "1") so that the multiplier would operate asynchronously. Figure 4.1-6 illustrates the oscillatory output waveform resulting from this test. The oscillation frequency observed in this case was 83.1 MHz which corresponds to a propagation delay per gate of 150 ps ($f = 1/80\ \tau_d$). Total power dissipation of this chip was 2.08 W or about 2 mW/gate. This would result in a full 16 bit product being performed in only 5.2 ns, a significant achievement. It is also important to note that speed was not compromised on the multiplier circuits by scaling up to the 1000 gate LSI level of complexity. In fact, the 8 × 8 multiplier average gate delays were less than those observed on the 75 gate 3 × 3 MSI multiplier, probably a consequence of improved design and simulation capability.

4.2 Radiation Hardness Assessment

During the first quarter of this program, GaAs Schottky diode FET logic integrated circuits were evaluated for total dose and dose rate sensitivity. Three stage ripple D Flip-Flop divider circuits (divide by 8) were selected for radiation testing because they are of MSI complexity (25 gates), are easily evaluated, and most importantly, they represent real sequential logic circuits with typical fanouts of 2 to 3 in their D FF latches. This latter condition is important to assure relevant test results, because noise

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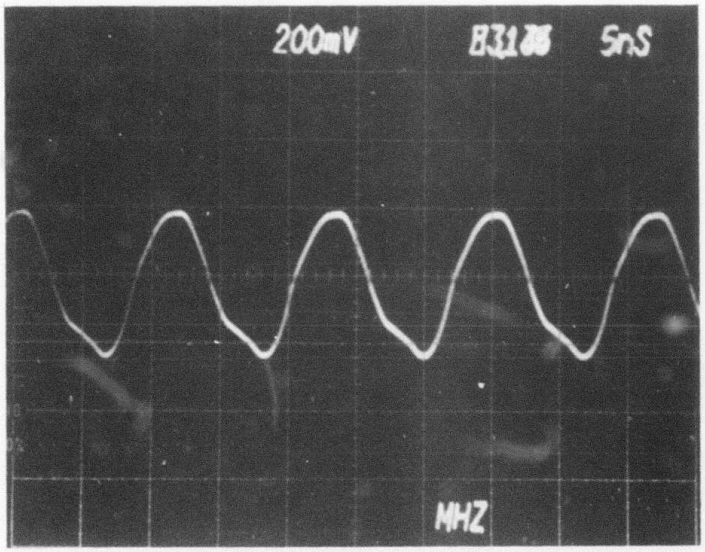

V_{dd} = 2.72V	f = 83.1 MHz	τ_d = 150 ps
V_{ss} = -2.03V	P_d = 2.08W	$P_d\tau_d$ = 310 fJ

Fig. 4.1-6 Performance of 8 x 8 multiplier when evaluated for high speed operation. The on-chip feedback path was enabled and the latches disabled to perform this measurement.

margins and therefore logic upset levels are sensitive to fanout. Quite different results might be obtained on F.O. = 1 ring oscillator inverters and on D Flip-Flops, even on the same wafers.

The SDFL divide by 8 circuits were packaged in 16 pin flatpacks. Correct operation was observed at clock frequencies up to 1.35 GHz on these particular samples, at a total power dissipation of about 100 mW. An electrically shielded test fixture in which the circuit under test was powered by batteries to minimize possible pulse EMI problems was prepared. The divide-by 8 output was monitored remotely during the test. A 250 MHz signal was provided as a clock input.

Total dose measurements under active, biased device operation were made to verify that degradation of device performance would not be induced by irradiation of a functioning logic circuit. Previous total dose measurements had been carried out on unbiased devices with up to 50 MRad of Co^{60} gamma radiation exposure being applied without noticeable change in device performance.[1] A Co^{60} source at the RADC Radiation Test Facility, Hanscom AFB, MA was used to carry out these tests.

As expected, no change in device performance was detectable up to a total dose of 2×10^7 Rad. The packaged divider circuit continued to function exactly as before irradiation. In the future, the test will be continued up to a total dose of 5×10^7 Rad.

The device was also tested under pulsed ionizing radiation using the Flash x-ray source at RADC. This source provided a 20 ns pulse of 1.4 meV

x-rays. The sample under test was biased at fixed voltage levels of V_{DD} = 3.75 V and V_{SS} = -2.5 V using batteries as a dc supply. Dose rates between 1 × 10^8 and 2 × 10^{10} Rad/s were applied. The dose rate was monitored with a silicon PIN diode, and total dose by thermoluminescent dosimeters.

The measured response of the divider circuit to the FXR pulse is summarized in Table 4.2-1. As can be seen from the data, circuit recovery times from 2 μm to 40 ms were observed. Although very encouraging, these figures represent upper limits in recovery time because of the fixed bias levels used in this preliminary experiment. Recovery time is expected to be very dependent on operating voltage. Shorter times are expected from a new experiment in which variable voltage supplies will be used to optimize bias conditions.*

Table 4.2-1

Transient Upset Response of the Three Stage Ripple Divider Circuit

Dose Rate (rad/s)	Total Dose per pulse (rad)	Recovery Time
1.1 × 10^8	2.2	2.0 μsec
4.9 × 10^8	9.8	5.5
2 × 10^9	40	14 msec
2 × 10^{10}	400	40 msec

*While this report was in press, a new measurement carried out under optimized bias conditions showed much shorter upset times. The new data will be presented in the next report.

5.0 CIRCUIT DESIGN - MASK SET AR6

In the following sections, the selection of two demonstration circuits for the first mask set, AR6, will be presented. Since both circuits employ multiple level logic gates (OR/NAND and AND/NOR), a discussion of the design of these gates will also be included.

5.1 Demonstration Circuits

The demonstration circuits selected for mask set AR6 represent important potential application areas for GaAs high speed, large scale logic. They also explore the potential density, speed and power advantages of multiple-level Schottky diode FET logic gates. For the first of these two circuits, the 8 × 8 multiplier of AR5[1] will be redesigned using two-level logic gates in the adder array. A block schematic diagram of the 8 × 8 multipliers was shown in Fig. 4.1-1, and a schematic drawing of the adder array is shown in Fig. 5.1-1.

The redesigned multiplier will provide a suitable vehicle for evaluation of the potential speed enhancement made possible by two-level diode logic gates (SD^2FL). The SD^2FL gates will allow a full adder cell to be realized yielding a 1 τ_d sum and 1 τ_d carry delay. This can reduce the worst-case delay time through the full adder array from 35 τ_d for the AR5, NOR-implemented version to 14 τ_d for the projected AR6 SD^2FL version. This could yield a significant speed improvement if the basic gate propagation delay is comparable to or only slightly longer than the SDFL NOR gate. Power and area considerations can also be assessed for this new logic gate approach. A

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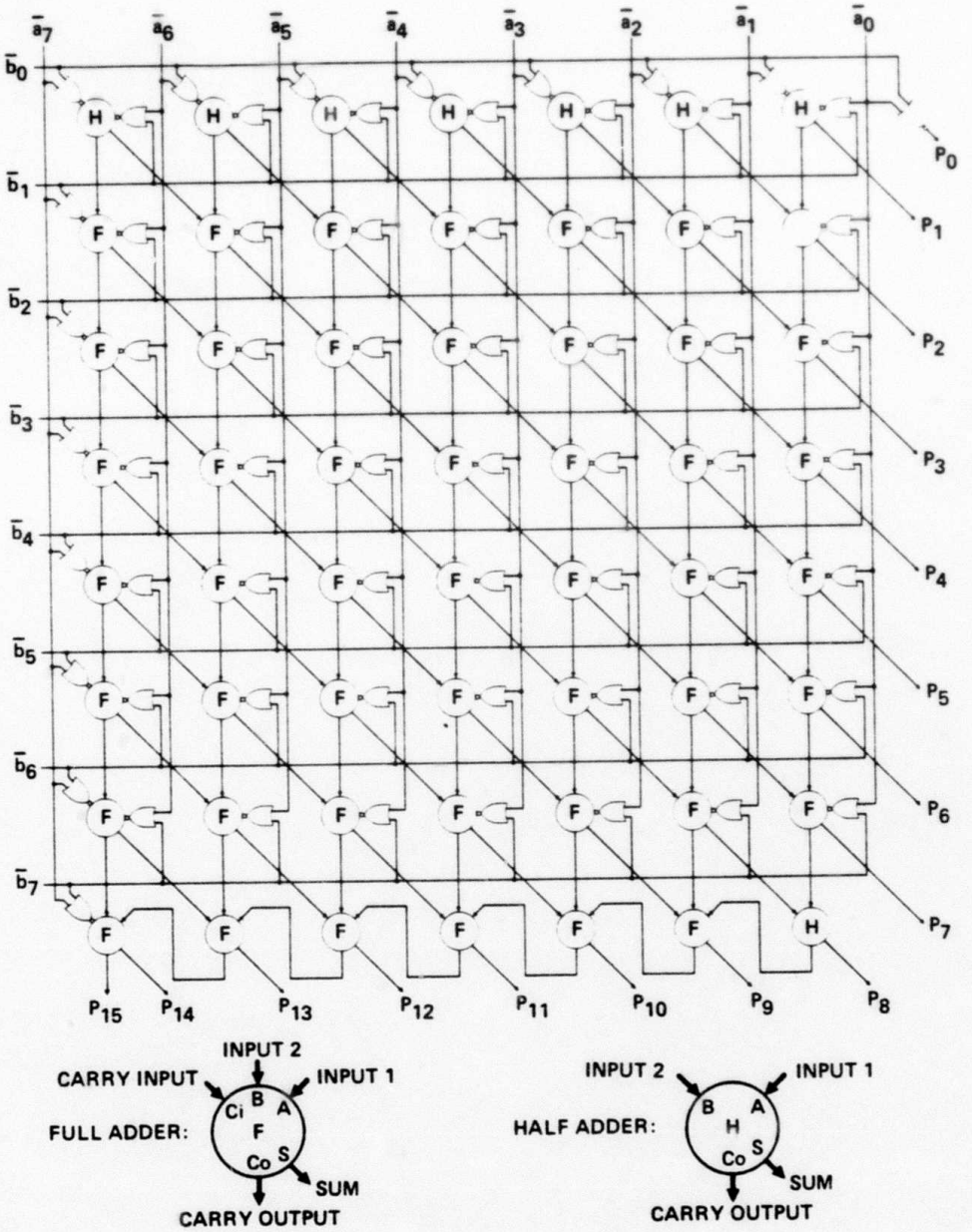
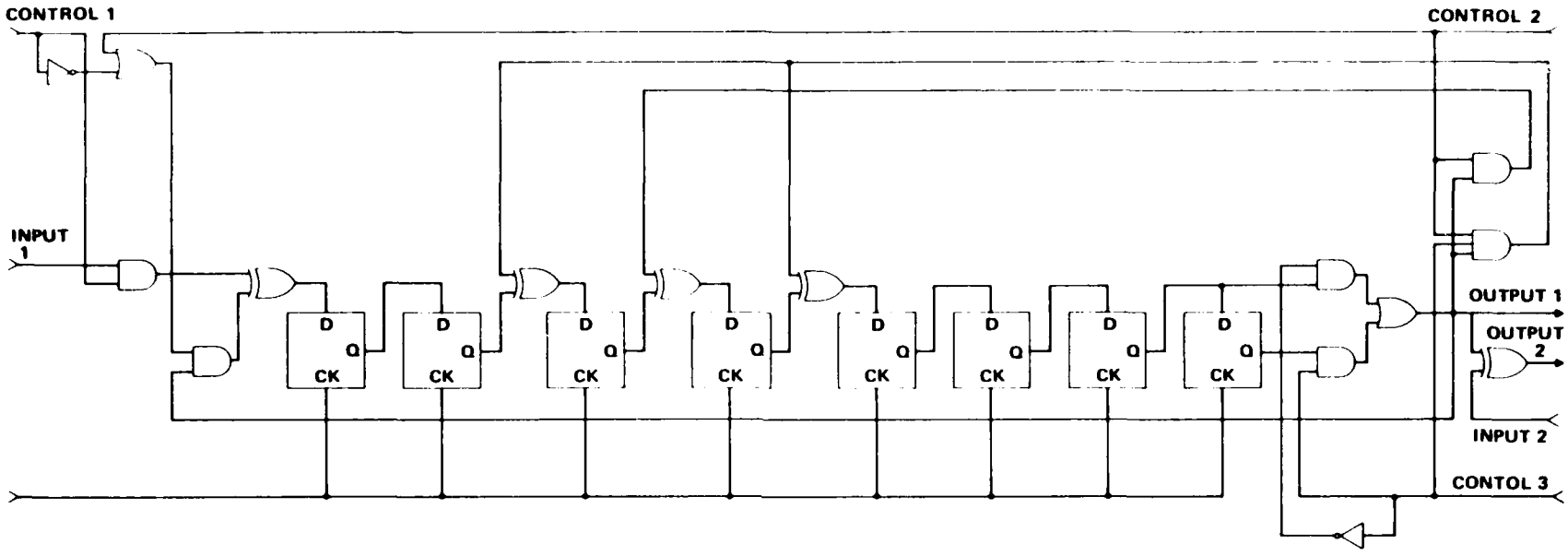


5.1-1 Circuit diagram of 8 × 8 parallel multiplier array.

discussion of this SD^2FL two-level logic gate and SDFL two and three level logic gates can be found in Section 5.2.

The second demonstration circuit, a programmable linear feedback shift register (LFSR) was recommended by RADC/ESE because of important potential system applications. This circuit produces a binary sequence of length 2^m-1, where m is the number of stages. There are 2^m-1 possible initial loading conditions where each loading results in a distinct output sequence. Binary linear feedback shift registers can also be used to perform polynominal division, where all polynominals have coefficients that are either one or zero. When a linear feedback shift register (LFSR) is used for division, its feedback connection polynominal is defined as the divisor polynominal. To perform division, the registers in the LFSR should be cleared to zero. Then the polynominal to be divided is fed sequentially into the input of the LFSR with the most significant coefficient first. The quotient polynominal appears at the output of the LFSR as the input polynominal is being divided. After the input polynominal has been entered into the LFSR, the remainder polynominal or residue is left in the shift register stages.

Figure 5.1-2 shows the logic circuit for a transposed direct-form realization of a programmable eight-stage LFSR. This LFSR can be used to generate m-sequences or to perform polynominal division. The circuit contains three control lines that provide for eight distinct modes of operation as shown in Fig. 5.1-2. The LFSR is electronically reconfigurable in order to generate two distinct m-sequences. In one mode of m-sequence operation, the LFSR is seven stages long and its connection polynominal is $X^7 = X^3 + 1$. This



CONTROL 1	CONTROL 2	CONTROL 3	FUNCTIONS	COMMENTS
1	0	0	LOAD LENGTH 7 REGISTER	7 STAGE DELAY LANE
1	0	1	LOAD LENGTH 8 REGISTER	8 STAGE DELAY LANE
0	1	0	GENERATE PN SEQUENCE,	127 LENGTH
0	1	1	GENERATE PN SEQUENCE,	255 LENGTH
1	1	0	DIVIDE BY P7(X)	$P9(X) = 1 + X^3 + X^7$
1	1	1	DIVIDE BY P8(X)	$P8(X) = 1 + X^2 + X^3 + X^4 + X^7$
0	0	0	READ RESIDUE, LENGTH 7	RECIRCULATING MEMORY
0	0	1	READ RESIDUE, LENGTH 8	

5.1-2 Logic circuit for the direct form realization of a programmable eight stage linear feedback shift register (LFSR).

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configuration will generate an m-sequence of length 127. In a second mode of m-sequence operation, the LFSR is eight stages long and its connection polynominal is $X^8 = X^4 + X^3 + X^2 + 1$. This configuratiuon generates an m-sequence of length 255. For the generation of m-sequences, the registers in the LFSR should be cleared to zero and then initialized by sequential input data. The programmable LFSR can perform divisions using different divisor polynominals. In one division mode, the LFSR divides by $1 + X^3 + X^7$, and in the other mode it divides by $1 + X^2 + X^3 + X^4 + X^3$. After either division, the LFSR can be reconfigured into a recirculating memory, and the polynominal residues can be read cyclically.

Two m-sequence generators whose shift register lengths are relatively prime and whose connection polynominals are different can be used to construct a gold-code generator. To produce a gold-code sequence, the output of two synchronized LFSR's are added module-2. An Exclusive-OR gate can be used for this function. By using any programmable LFSR's, it is possible to generate a gold-code sequence. If one LFSR is programmed as length 7 while the other is programmed as length 8, the resulting gold-code sequence will have a period of $(2^7-1)(2^8-1) \approx 2^{15}$.

During the next quarter, final design and layout will be carried out on the circuit described above. Optimum choices of logic gates, register cell architecture, diode requirements and feedback elements will be established by use of simulation and circuit modeling tools.

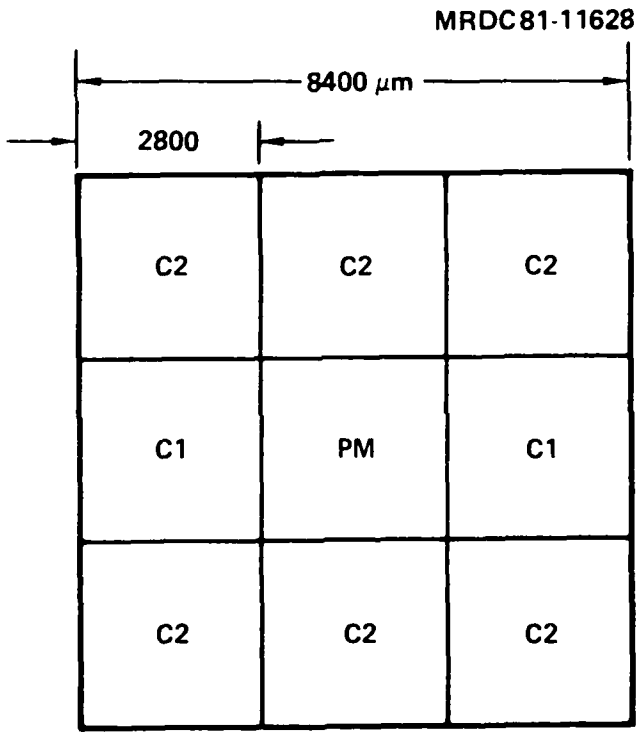
Mask set AR6 will follow the format utilized in previous mask sets AR4 and AR5[1] with a 3 × 3 reticle composition encompasing an 8.4 mm × 8.4 mm area on the wafers. A drawing of a tentative composition of AR6 is shown in Fig. 5.1-3. Three reticles, PM, C1 and C2 will be required to accommodate the two main demonstration circuits and the necessary process monitoring/circuit development test structures.

5.2 Multiple Level Logic Circuits

A logic gate circuit design must be capable of extension to two or more levels of logic per gate delay in order to realize the highest speed, and to minimize chip area and power dissipation for a given IC logic technology (a logic level consists of one (N)AND or (N)OR operation of arbitrary width). Multilevel gate implementations allow complex logic operations to be achieved in slightly over one basic logic gate propagation delay (τ_d) rather than two or three delays as would be the case for single level NOR or NAND implementations. They also dissipate less power and require less wafer area than single level circuit implementations.

SDFL Multiple Level Logic Gate Design and Performance

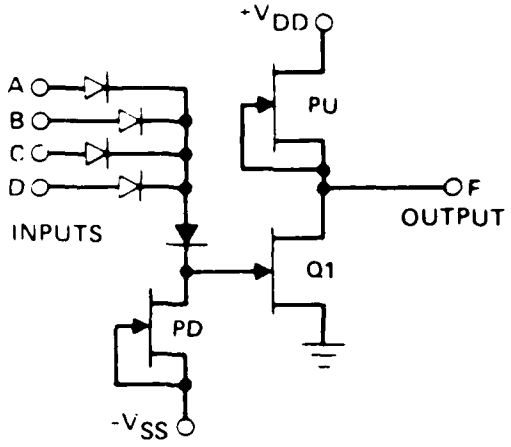
The use of combinations of series (NAND) or parallel (NOR) FET configurations to achieve two-level logic functions is common. VanTuyl, et al.[9] demonstrated depletion-mode GaAs MESFET buffered-FET logic (BFL) NAND/NOR (or NAND/WIRED-AND) gates, with up to two NAND input terms (series or dual-gate FETs) and up to two of these NAND functions "drain dotted" together,



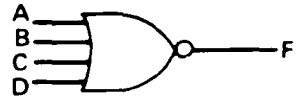
5.1-3 Composition of a reticle for mask set AR6 showing the PM, C1, and C2 chips.

having propagation delays as low as τ_d = 110 ps. Four of these gates were utilized to implement a fast ($f_c \sim 1/(2\tau_d)$) complementary-clocked ÷2 frequency divider[9] stage which gave toggle frequencies up to 4.5 GHz, for $\tau_d \sim 111$ ps effective gate delays, at a $P_D \sim 40$ mW/gate power level. Here, the advantage of a two-level gate is clear, since the fastest NOR-gate implemented complementary-clocked divider circuit uses 8 gates and has a maximum speed of $f_c = 1/4\tau_d$. In SDFL, more easily used, single-clocked T-connected D-flip flops using 6 NOR gates were fabricated, achieving maximum toggle frequencies of f_c = 1.9 GHz at P_D = 2.5 mW/gate, which corresponds to τ_d = 110 ps ($f_c = 1/4.85\tau_d$ in this configuration).[10] Hence, while the SDFL NOR gates gave the same propagation delays as the BFL gates (and at much lower power levels), the architecture of the NAND/NOR dividers allowed much higher toggle frequencies to be reached.

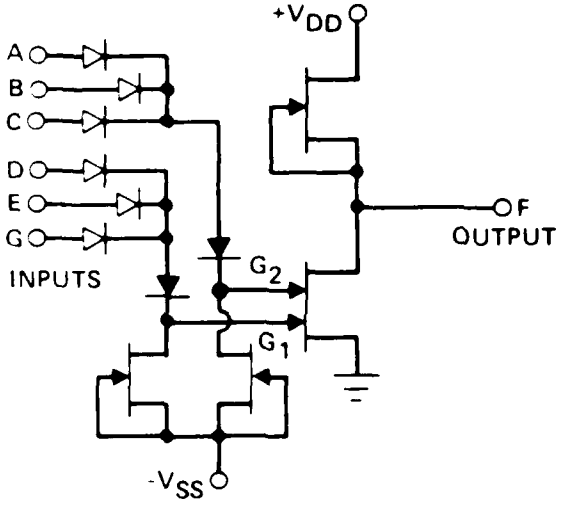
Multi-level logic gate configurations may indeed be realized in SDFL[11] with up to 3-level gates with many (10 - 20) inputs not being restricted to 4-input 2-level gates as in BFL. In the previously-published SDFL work,[10] the FET logic function utilized was principally the inverter, so that, with the diode-OR, a NOR gate function was realized (Fig. 5.2-1a). On the other hand, by using such diode-OR clusters on each gate of a dual gate FET (or series-FET connection), an OR/NAND 2-level gate is achieved (Fig. 5.2-1b), This gate is the complement of the 2-level NAND/NOR gate realized in BFL, except that the number of first level terms in the SDFL version is no longer restricted to two. The resulting OR/NAND function $F = \overline{(A+B+C)(D+E+G)}$ can be used to reduce considerably the propagation delay per equivalent gate by performing a two-



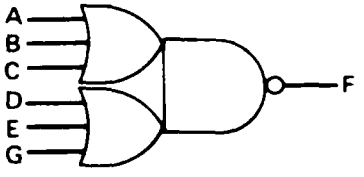
$$F = \overline{A + B + C + D}$$



a) SDFL NOR GATE

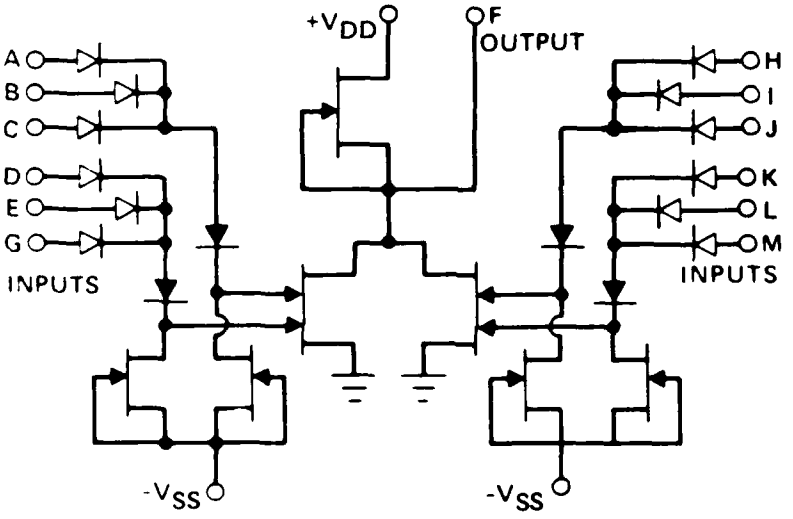


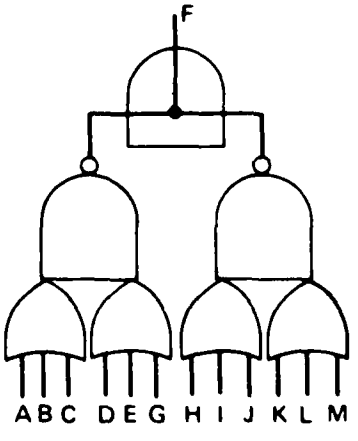
$$F = \overline{(A + B + C) \cdot (D + E + G)}$$



b) SDFL OR/NAND GATE

$$F = \overline{[(A + B + C) \cdot (D + E + G)] + [(H + I + J) \cdot (K + L + M)]}$$





c) SDFL OR/NAND/WIRED-AND GATE

5.2-1 Comparison of 1-, 2-, and 3-level SDFL gate configurations.

level operation in approximately one NOR gate delay. Power dissipation is only slightly above that of a NOR delay gate (one added pull-down) and the area is also only slightly greater.

A three-level (OR/NAND/WIRED-AND) gate can also be constructed by the use of "drain-dotting" or sharing of a common pull-up by two OR/NAND gates. An example of this gate is shown in Fig. 5.2-1c. Again, the number of OR inputs is arbitrary. Here, the three-level logic function $F = \overline{[(A+B+C)\ (D+E+G)] + [(H+I+J)\ (K+L+M)]}$ is performed by this gate in substantially the same propagation delay time required by a single NOR gate. Power dissipation is again only slightly above that of a single level (NOR) gate, and the area would be about twice that of a NOR gate.

These multilevel gates can provide large equivalent gate counts depending on the application. An equivalent gate count can be defined by the minimum number of NOR gates required to implement a particular Boolean function. For example, an Exclusive OR function which would be implemented (from complementary inputs) with three NOR gates can be realized by only one OR/NAND gate. In this case, the equivalent gate count of the OR/NAND gate is 3. The three-level gate can provide gate counts as high as 7 in certain applications. That is, one OR/NAND/WIRED-AND gate can replace seven NOR gates in some types of logic circuit applications.

Circuits have been fabricated, using our planar 1 μm gate length GaAs IC process, with both 2-level OR/NAND (Fig 5.2-1b) and 3-level OR/NAND/WIRED-AND (Fig. 5.2-1c) SDFL gates. The SEM pictures in Fig. 5.2-2, for example,

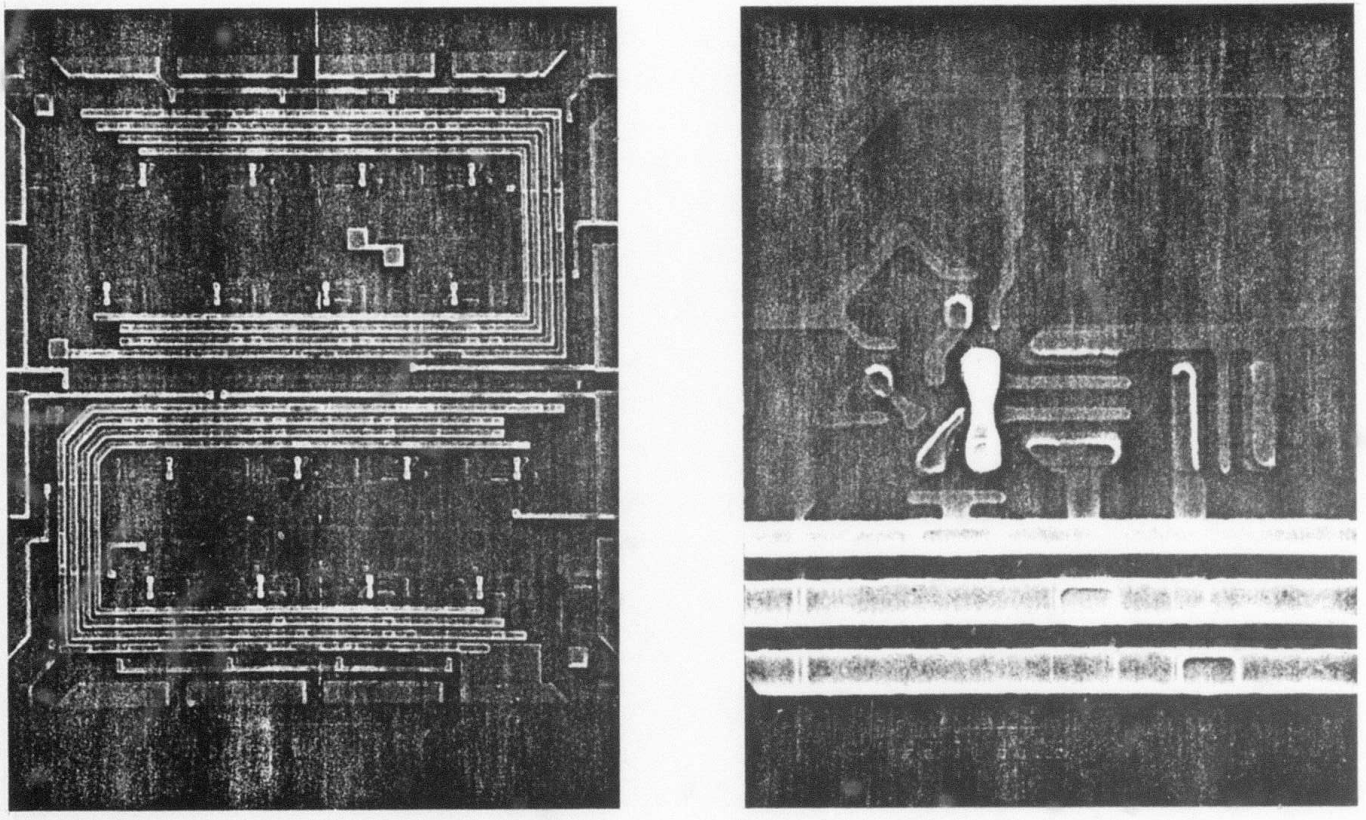


Fig. 5.2-2 SEM picture of 7-stage SDFL OR/NAND (2 level) gate ring oscillators. The upper ring oscillator in the left picture allows propagation through G_2 only (e.g., inputs A, B or C in Fig. 5.2-1b), while the lower ring oscillator allows propagation through G_1, G_2 or both gates simultaneously. Photo on right shows one gate from this lower ring oscillator.

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show a subchip (320 μm x 320 μm inside pads) containing two 7-stage OR/NAND ring oscillators and a detail of one of the gates. The gate area (about 30 μm x 45 μm) is only about 30% larger than a standard SDFL NOR gate of the same 10 μm FET width. Figure 5.2-3 shows the static transfer characteristics of one of these SDFL OR/NAND gates, both in standard and intensity modulated (2-dimensional) display formats. These show that the proper NAND function is being realized between logic diode inputs attached to FET gate 2 (G2; A, B, or C in Fig. 3.6-1b) and inputs to FET gate 1 (G1;D, E, or G in Fig. 3.6-1b). The + 180 mV shift of threshold voltage on FET gate 2 inputs is due to the I_dR_{on} voltage drop across the G1 effective FET.

The lower 7-stage ring oscillator in Fig. 5.2-2 allows for operation in three modes of signal propagation: through G2 only with fanout of 1 (FO=1) and fanin of 4 (FI=4), through G1 only (FO=1, FI=4) or simultaneously through both G2 and G1 (FI=2, FO=4). Evaluation of these ring oscillators has been carried out, and the results for 5 μm and 10 μm OR/NAND ring oscillators operated in each of the three propagation modes is shown in Table 5.2-1.

SDFL OR-NAND GATE OPERATION

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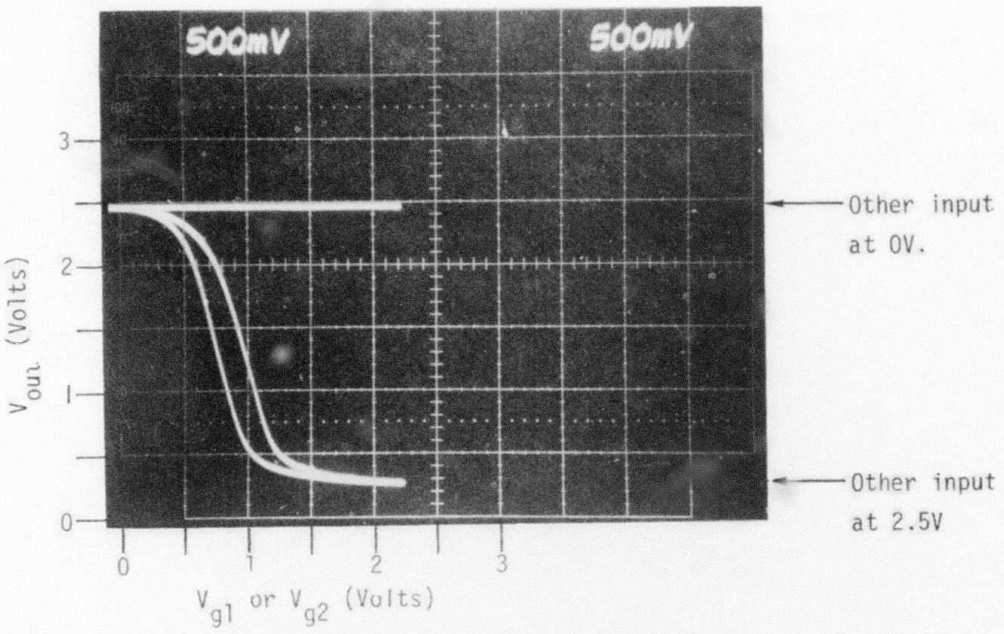


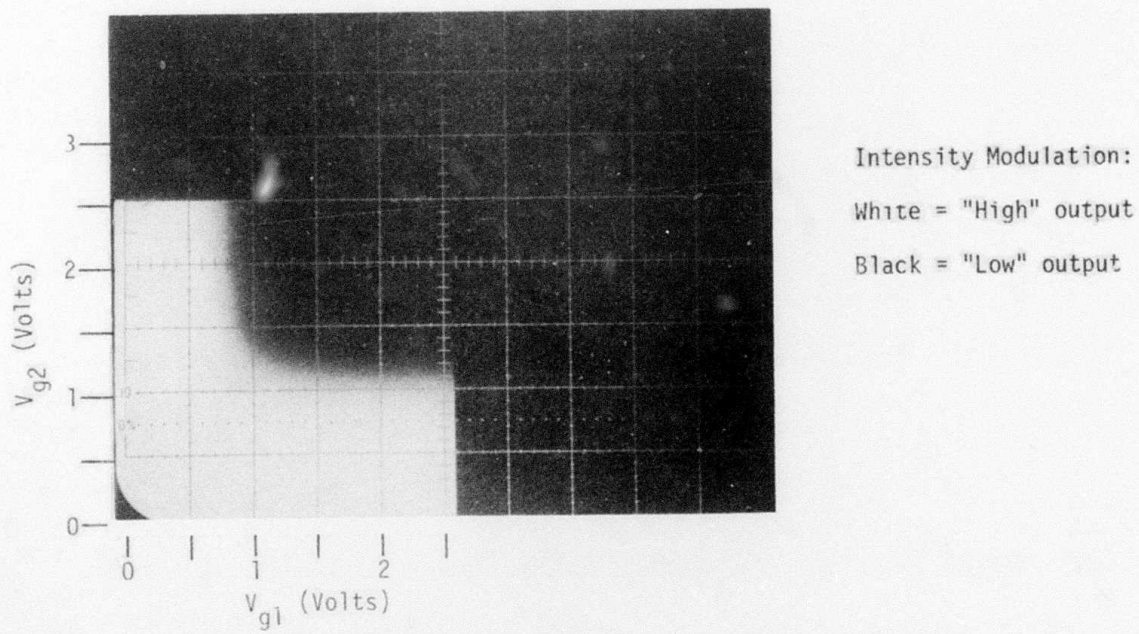


Fig. 5.2-3 Static transfer characteristics for SDFL OR/NAND gates. V_{g1} refers to the logic gate input voltage at D, E or G in Fig. 5.2-1b, while V_{g2} refers to inputs attached to the second FET gate, A, B or C in Fig. 5.2-1b.

Table 5.2-1

SDFL OR/NAND Ring Oscillator Evaluation

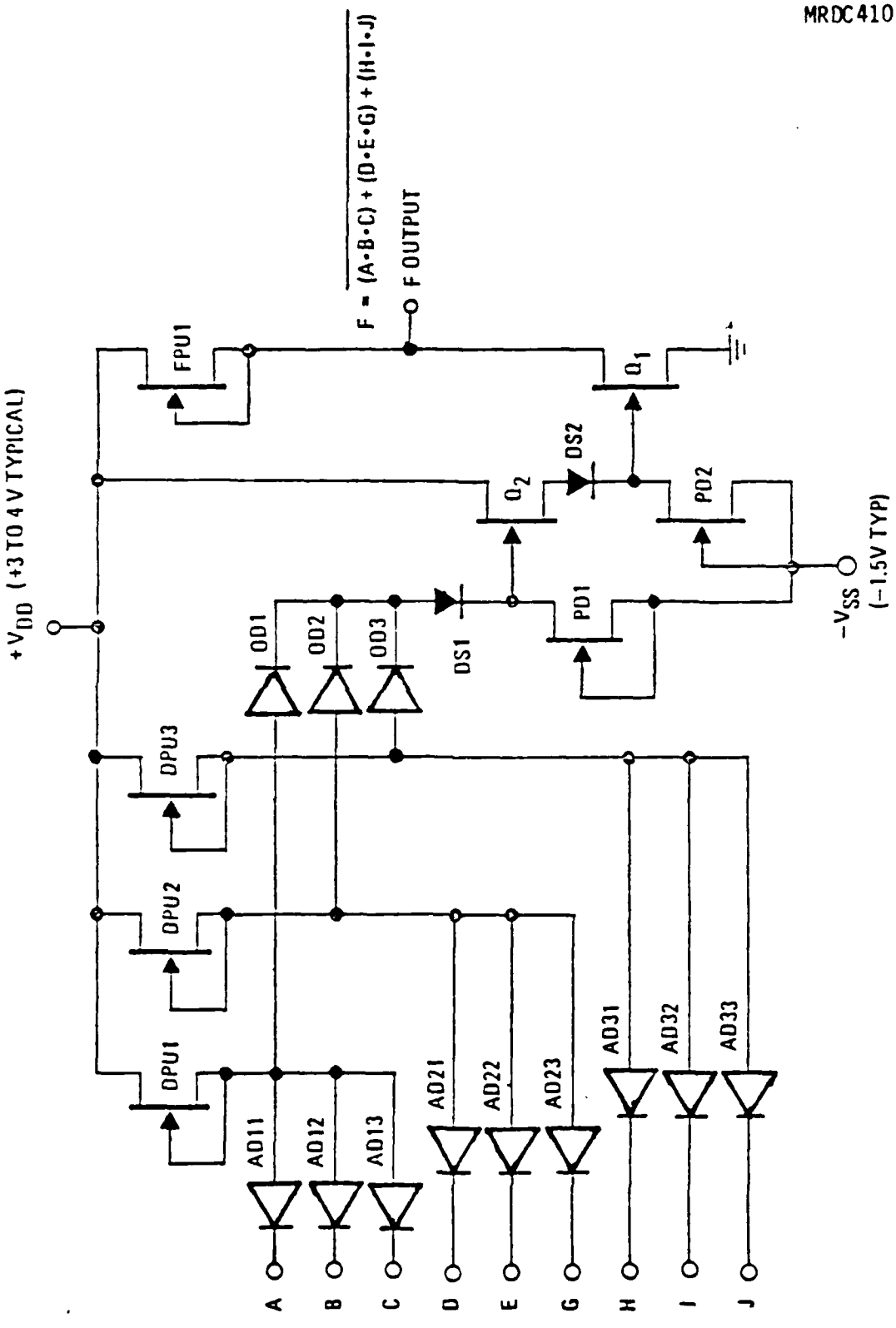
	Mode(FO)	f_{osc} (MHz)	Power Dissipation	τ_d (ps)	$P_D\tau_d$ (fJ)
W=5 μm	G_1 (1)	405	475 μW	176	84
7 Stage	G_2 (1)	410	542	174	94
OR/NAND RO	G_1+G_2 (2)	348	456	205	94
W=10 μm	G_1 (1)	640	1.8 mW	112	201
7 Stage	G_2 (1)	680	1.7	105	180
OR/NAND RO	G_1+G_2 (2)	550	1.67	130	217

The key to the performance of these SDFL circuits is the extremely low capacitance (C_j ~ 2 fF), high conductance planar GaAs Schottky barrier switching diodes (R_s as low as 270 Ω for a cutoff frequency of $f_c = 1/(2\pi R_s C_j)$ ~ 300 GHz). Because the diode speed is so far above the f_τ ~ 15 GHz current gain-bandwidth products of the L_g = 1 μm depletion-mode MESFETs, the gates have large diode-OR fanins with little degradation in switching speed. On the other hand, in FET logic, parasitics such as gate capacitance and "on" resistance severely limit the fanins (either in series-FET NANDing or drain dotting) usable if high speeds are to be maintained. In fact, the 10 μm OR/NAND gate RO data described above is somewhat slower than the best 10 μm NOR gate RO performance (105 ps as opposed to 62 ps) even though only a fanin of two is utilized at the first (NAND) level. However, a large net increase in circuit speed and reduction in area can be achieved by the proper use of two-level logic gates rather than single level (NOR) gates.

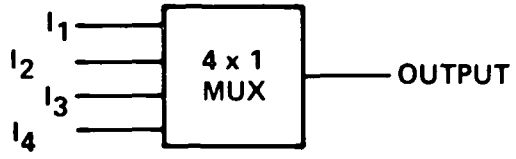
SD^2FL Gate Design

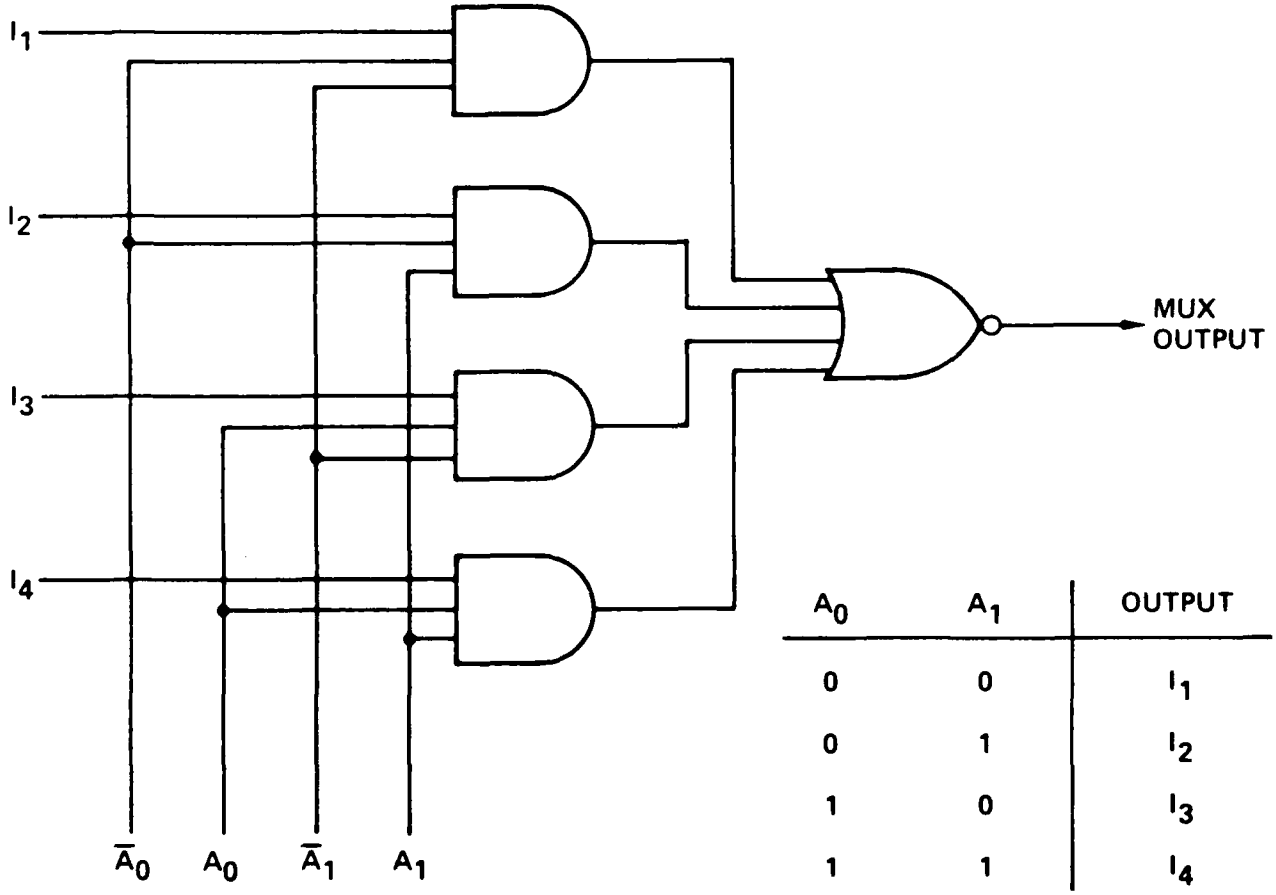
The multi-level logic gate approach described above allows major saving of chip area and power dissipation, and also increased circuit speed (fewer gate delays). In general, however, the numbers of terms which can be practically "NAND'ed" with series FETs is limited (due to parasitic gate capacitances and FET "ON" resistances) to 2 or perhaps 3 without substantial performance degradation. Similar restrictions apply to the "drain dot" -wired AND of the three level OR/NAND/WIRED-AND gate. To avoid this fanin restriction of multi-level logic gates, the extra fast logic element available in the GaAs Schottky diode can be utilized to perform two levels of logic operations rather than just one level. Figure 5.2-4 illustrates the use of 2 levels of diode logic with the basic SDFL gate structure. Clusters of diodes (AD_{xx}) with their cathodes connected to inputs and their anodes connected in common to a pull up (DPU_x) form the first level of positive - AND function (i.e., if any input is "low" the common anode must be low). The anode output of these AND clusters are combined to form an "OR" diode cluster (OD_x) and the common cathodes of this diode cluster are connected to the FET (Q_1) gate and its pull down current source, PD1, through two voltage level shift diodes (SD1, SD2) such as would be needed in a regular SDFL gate.

Figure 5.2-5 illustrates how this type of simple 2-level diode logic (SD^2FL) gate could be utilized in a typical application. With two levels of logic (AND - OR) and unlimited width (as compared to the FET NAND or "drain dot" which is typically limited to 2 or 3 terms), most desired logic functions can be directly obtained from their full min-term expansion in only one gate



5.2-4 Circuit diagram of simple SD^2FL logic gate.





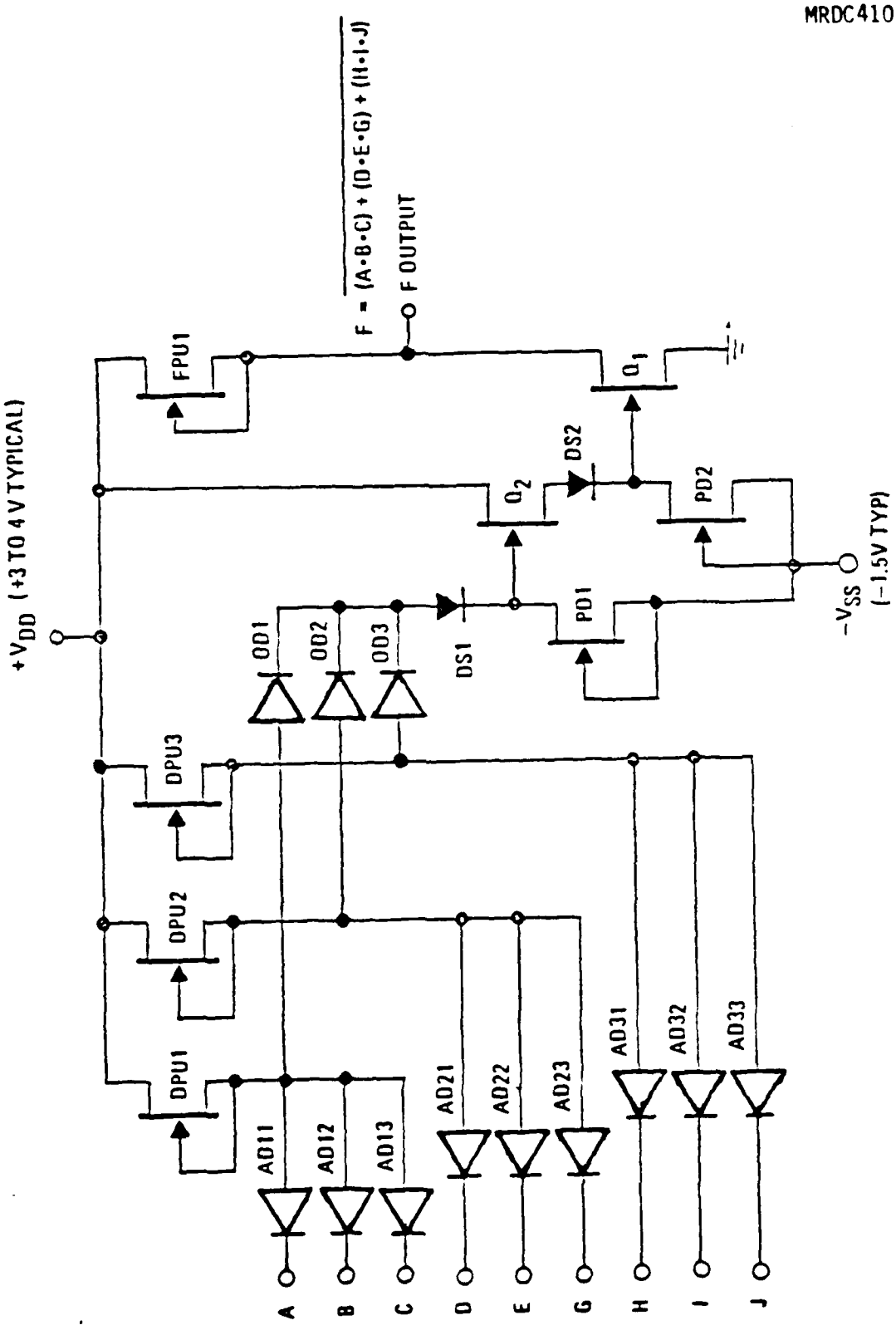
A_0	A_1	OUTPUT
0	0	I_1
0	1	I_2
1	0	I_3
1	1	I_4

5.2-5 Logic diagram of 4 to 1 multiplexer realized with a single SD^2FL.

delay. In the 4 to 1 multiplexer example of Fig. 5.2-5, it only takes one SD^2FL logic gate and one gate delay to generate this function which would require five SDFL NOR gates and two NOR gate delays to realize in single level logic. The SD^2FL gate in this example, therefore, has an equivalent gate count of 5.

Unfortunately, in the simple SD^2FL version of Fig. 5.2-4, the speed advantage will be lost because of the unfavorable ratio between the pull down size (W_{PD}) and the width of FET (W_Q) which must handle all of the diode pull up currents. With a fan out of 6, a ratio of $W_Q/W_{PD} = 20$ is required. This 20 to 1 ratio would lead to gate delays up to 4 times worse than an SDFL NOR gate in which the W_Q/W_{PD} ratio is usually kept at 5:1. Figure 5.2-6 shows an improved version of the 2 level diode logic gate which would allow an implementation of complex circuits without gross speed loss due to fan out drive problems. The key to this improved SD^2FL circuit speed is the inclusion of the source follower driver stage (Q_2 - PD_2) to provide current gain from the small logic diode current levels up to the substantial gate drive currents required for the high speed switching of Q_1. With the sacrifice of slightly increasing the power dissipation and complexity (due to the addition of the source follower driver), the gate delay time of the modified SD^2FL gate should be nearly as fast as the SDFL NOR gate.

The extension of this SD^2FL approach to an even higher level of logic function can be easily achieved. Note that if Q_1 is a dual gate FET and if the input and same source follower structure is used for each gate, a 3 level gate AND/OR/NAND gate will be obtained. Similarly, if another such 3 level

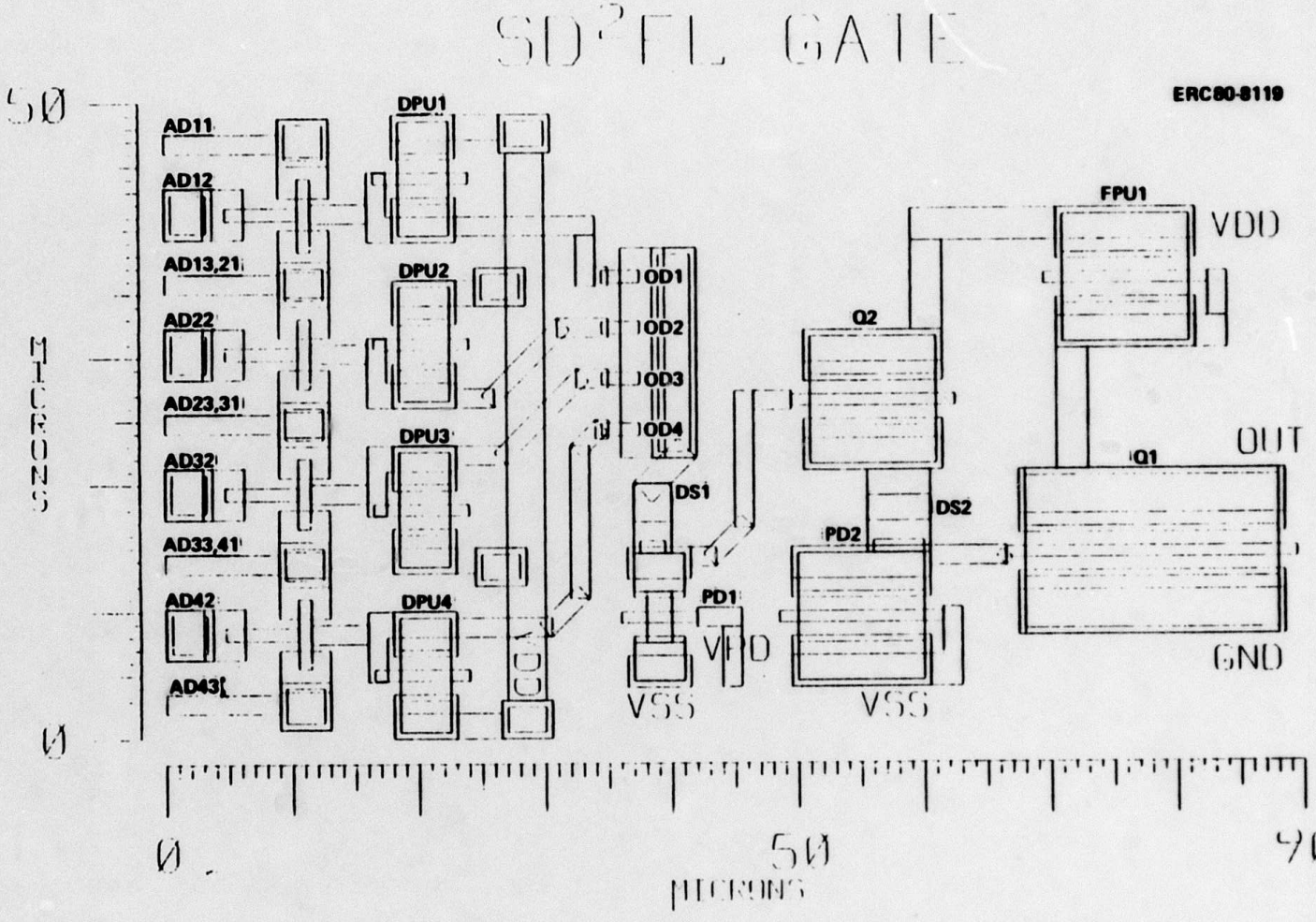


5.2-6 Improved version of 2-level SD^2FL diode logic gate.

gate were connected with their outputs sharing a common pull up, a 4 level AND/OR/NAND/WIRED-AND would be obtained.

A layout drawing of a typical SD^2FL 2-level AND/NOR logic gate is shown in Fig. 5.2-7. This is similar to a gate which might be used for the 4 to 1 multiplexer of Fig. 5.2-5 and would thus have an equivalent gate count of 5. The total area required by this gate, exclusive of intrconnects, is less than 4500 μm^2, representing an area per equivalent gate of only 900 μm^2.

The circuit simulation program, SPICE 2, has been used to evaluate the potential performance of SD^2FL gates. Parasitic capacitances were calculated for typical layouts and included in the simulation. A 3 stage ring oscillator (FI=4, FO=1) was modeled for the 20 μm SD^2FL gate of Fig. 5.2-7 with only one input cluster being OR-ed and inverted. A propagation delay of 107 ps was calculated as shown in Fig. 5.2-8. This is only slightly slower than the propagation delay simulation result obtained by modeling a 10 μm NOR gate ring oscillator (FI=2, FO=1; τ_d = 84 ps).



5.2-7 Layout drawing of a 20 μm SD^2FL AND/OR logic gate. e.

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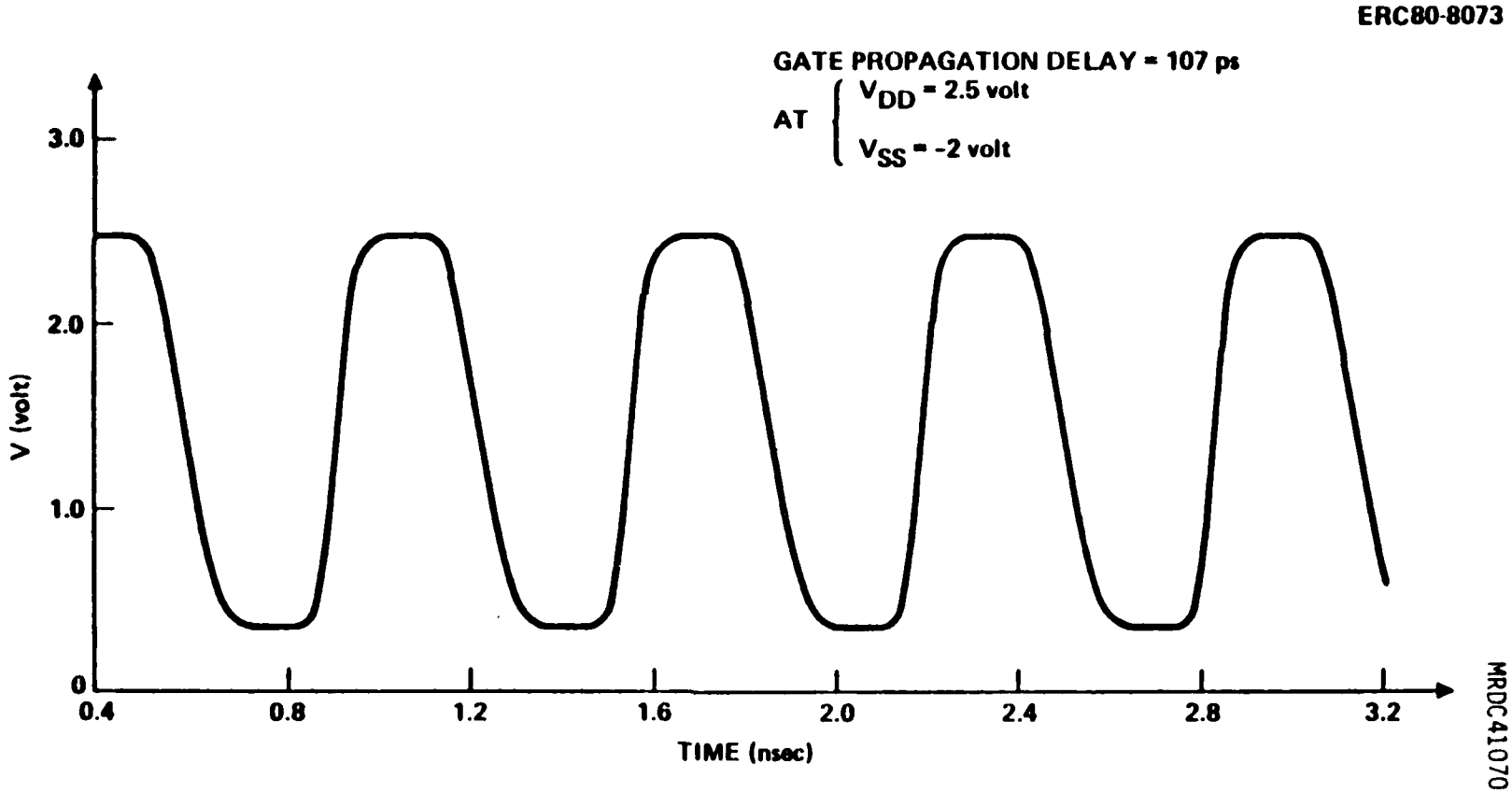
SIMULATION OUTPUT OF 3 STAGE RING OSCILLATOR WITH SD^{2}FL GATES



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5.2-8 Circuit simulation output of a 3-stage 20 μm SD^{2}FL ring oscillator (FO=1). This was calculated for V_{DD} = 2.5 V and V_{SS} = -2.0 V. A propagation delay of 107 ps/gate is predicted.

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