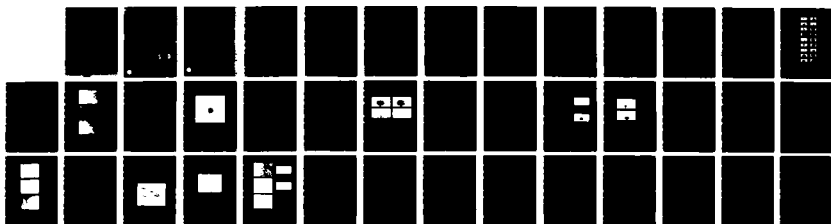


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DEVELOPMENT OF VLSI OPTICAL DATA LINK

Quarterly Technical Status Reports #1 and #2
For the Periods September 1 to November 30, 1986
and December 1, 1986 to February 28, 1987

Contract No. DAAL01-86-C-0023
Department of the Army
Electronics Technology and Device Laboratory
Fort Monmouth, New Jersey 07703

P. G. McMullin
Crystal & Device Technology Research

R. L. Messham
Microelectronic Device Research

September 18, 1987

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The deposition of GaAs epilayers onto the silicon epilayer of an SOS wafer has proven to be a relatively robust process, insensitive to variations in substrate orientation, cleaning, preconditioning, growth rate and temperature, and composition of the deposited layer. Deposition onto sapphire substrates has not yet given GaAs epilayers of high quality. The best approach for obtaining device-quality GaAs appears to be through utilization of the silicon epilayer as the base for the GaAs deposition. Experiments will be carried out to improve the quality of GaAs layers deposited directly onto sapphire. <i>Keyword include:</i>					
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1. INTRODUCTION

The major objective of this program is to show the feasibility of VLSI optical data links with GaAs optical components fabricated on a common sapphire substrate with silicon signal-processing integrated circuits. The first goal of the program requires improvement of the quality of GaAs epilayers deposited onto sapphire or SOS substrates. Indeed, this is an essential requirement for successful completion of the fabrication of optical devices. An investigation has been started to identify the critical factors that determine the quality of epilayers deposited by the MOCVD method. The factors to be considered are:

- Substrate
- Cleaning Procedures
- In-Situ Pretreatment
- Growth of Nucleation Layer
- Growth Rate
- Temperature of Growth
- Composition of Nucleation and Final Layer
- Multilayer Structure

The factors are each considered, and the range of variation explored experimentally is presented.

1.1 SUBSTRATES

The program calls for integration of function between SOS VLSI circuits and GaAs optical components. This constrains the substrate to the surfaces available from SOS. The SOS sapphire substrate is a single crystal of $1\bar{1}02$ surface plane orientation. Many samples of this kind have been included in the study, either as whole two-inch wafers or as

1 cm square pieces. GaAs may also be deposited onto the surface of the silicon epilayer of the SOS wafer. Most of the work so far has centered on silicon epilayers of SOS samples, since the early runs indicated this was a favorable case. For comparison, standard silicon wafers have been included in some runs, as well as basal-plane-oriented sapphire samples. Recently, the best GaAs/Si layers reported in the literature have been made with tilted Si substrates. This is not a practical variation for SOS wafers, since it would call for a new specification of the SOS material and would raise questions about the processing characteristics for VLSI circuits. The customary specification for SOS wafers allows a two-degree misorientation away from the nominal $1\bar{1}02$ plane. An attempt has been made to correlate the orientation of a set of SOS wafers, determined by x-ray, with the layer quality. Also, a tilted silicon substrate has been included among the MOCVD runs.

1.2 CLEANING PROCEDURES

The substrate surface must be extremely clean for deposition of low defect density epilayers. An experiment has been performed to evaluate the effect of surface cleaning on epilayer quality. A set of six substrates, three each of SOS and bare sapphire, were placed together in the reactor for MOCVD deposition of GaAs. The substrates were given either a minimal clean, stringent clean, or partial etch before the run. The epilayer appearance and quality were correlated to the cleaning procedure and the run conditions.

1.3 IN-SITU PRETREATMENT

The condition of the substrate surface at the start of deposition can be affected by the procedures carried out while the sample is in the chamber. Every MOCVD run begins with a bake cycle at 300°C in flowing hydrogen to ensure that all moisture is removed before the growth cycle. After this, several different methods of preparing the substrate have been used. A high-temperature prebake in hydrogen, intended to allow desorption of the last traces of native oxide from the

surface of silicon samples, has also been applied to sapphire samples. Prebaking at a temperature above the deposition temperature, in flowing arsine, saturates the substrate surface with arsenic as the initial condition for deposition. This method has been used for silicon and sapphire surfaces. The converse preparation condition, saturation with gallium or aluminum, has been used for sapphire substrates. Aluminum is a constituent of sapphire, and gallium is a chemical equivalent to aluminum, allowing the possibility that this pretreatment will produce an active surface for the initial deposition.

1.4 GROWTH OF NUCLEATION LAYER

The condition of the initially deposited layer is obviously critical, since the surface of this layer comprises the substrate for the subsequently deposited material. The program has included a comparison of deposition under constant conditions throughout the layer growth, with multiple-step depositions taking place at different temperatures and rates. One method which has given some excellent results involves the deposition of a thin nucleation layer at a low temperature, 420°C. Because of the low temperature, the layer is amorphous as deposited. The layer thickness has been varied from 20 to 50 nm in thickness. The growth is then interrupted while the temperature is raised. During this interval, the nucleation layer recrystallizes on the substrate by a solid phase process. In theory, this should be a more uniform and controllable process than the island growth and coalescence that occurs in higher temperature layer growth. Finally, the layer thickness is built up by continuation of the deposition at the higher temperature. This procedure has been applied for SOS and sapphire substrates with several variations of the temperature of the final layer deposition and layer thickness.

1.5 GROWTH RATE

A number of depositions have been carried out at constant temperature, particularly with sapphire substrates. In such runs, the

growth rate is an important parameter. The growth rate has been varied by changing the flow rate of the trimethyl gallium source gas. A slower growth rate is intended to favor a smoother surface morphology by providing more time for surface diffusion. Also, the growth rate has been varied during a run to separate the effects of the initial and final growth rates.

1.6 TEMPERATURE OF GROWTH

Normally the MOCVD process has a wide window for temperatures at which GaAs may be deposited. The quality of the epilayer will vary in several important respects with the deposition temperature. The native defect concentrations depend on temperature; this is evident as a change in the conductivity type and the carrier concentration, depending on temperature, as well as the ratio of the III-V constituents in the process gas. The surface morphology tends to be somewhat worse at higher deposition temperatures. Due to differential thermal contraction, the stress in the deposited layer will be greater when a higher deposition temperature is used. The temperature range from 600 to 775°C has been investigated for the deposition of the final layer.

1.7 COMPOSITION OF THE NUCLEATION AND FINAL LAYER

In the MOCVD reactor as presently configured, an additional degree of freedom is available in the fractional content of AlAs present in the deposited layer. This has been explored by growing nominally 30 percent and 70 percent AlAs layers, using other deposition parameters that had proved favorable for GaAs.

1.8 MULTILAYER STRUCTURE

There is some indication that a repetitive sequence of layers, alternating in composition between GaAs and AlGaAs, can reduce the epilayer defect density by confining threading dislocations in the interfaces. This effect should be stronger for alternating layers of GaAs and InGaAs, where the lattice mismatch is greater and the layers

are more highly stressed. At the present, an In source is not available, and the experiments have been limited to AlGaAs multilayers. Samples with thin multilayer regions near the interface with the substrate have been grown and are being characterized.

This completes the overview of the range of experimentation in the optimization of the epilayer deposition. In the next section, more detailed information is given about the experimental procedures. Measurement data and characterization results are presented, and conclusions are drawn. Many of the experiments have not yet been completed; later reports will review the results as they become available.

2. RESULTS AND DISCUSSION

2.1 COMPARISON OF SOS AND SAPPHIRE SUBSTRATES

In a series of nine MOCVD runs, samples of SOS substrates and sapphire substrates were placed in the reactor together to ensure identical deposition conditions. The samples were 1 cm square pieces scribed and cracked from larger samples. The SOS samples were taken from SOS wafers purchased from Union Carbide, with a 500 nm thick silicon epilayer. The sapphire substrates were cut from 1102 oriented sapphire substrates purchased from Union Carbide, supplied with the proprietary surface polish to make them ready for silicon epitaxial deposition. These wafers were considered to represent ordinary commercial material.

The samples were cleaned by various methods intended to range from casual to rigorous, as explained in the next section. The MOCVD run conditions also covered a wide range of conditions. After the MOCVD deposition was completed, the samples were examined visually, inspected and photographed using a Nomarski differential interference contrast microscope, and submitted for electron diffraction (RHEED) characterization.

Although diverse preparation and run conditions were involved, a consistent result was obtained. Figure 1 shows a compilation of RHEED patterns from samples in the series of runs. It can be easily seen that the SOS samples typically exhibit a regular pattern of spots, with no rings or ring arcs evident. Such patterns indicate a single-crystal orientation of all material on the surface within the diameter of the electron beam, which is about 50 μm . In contrast, the RHEED patterns from sapphire substrates vary from rings to irregular spot patterns,

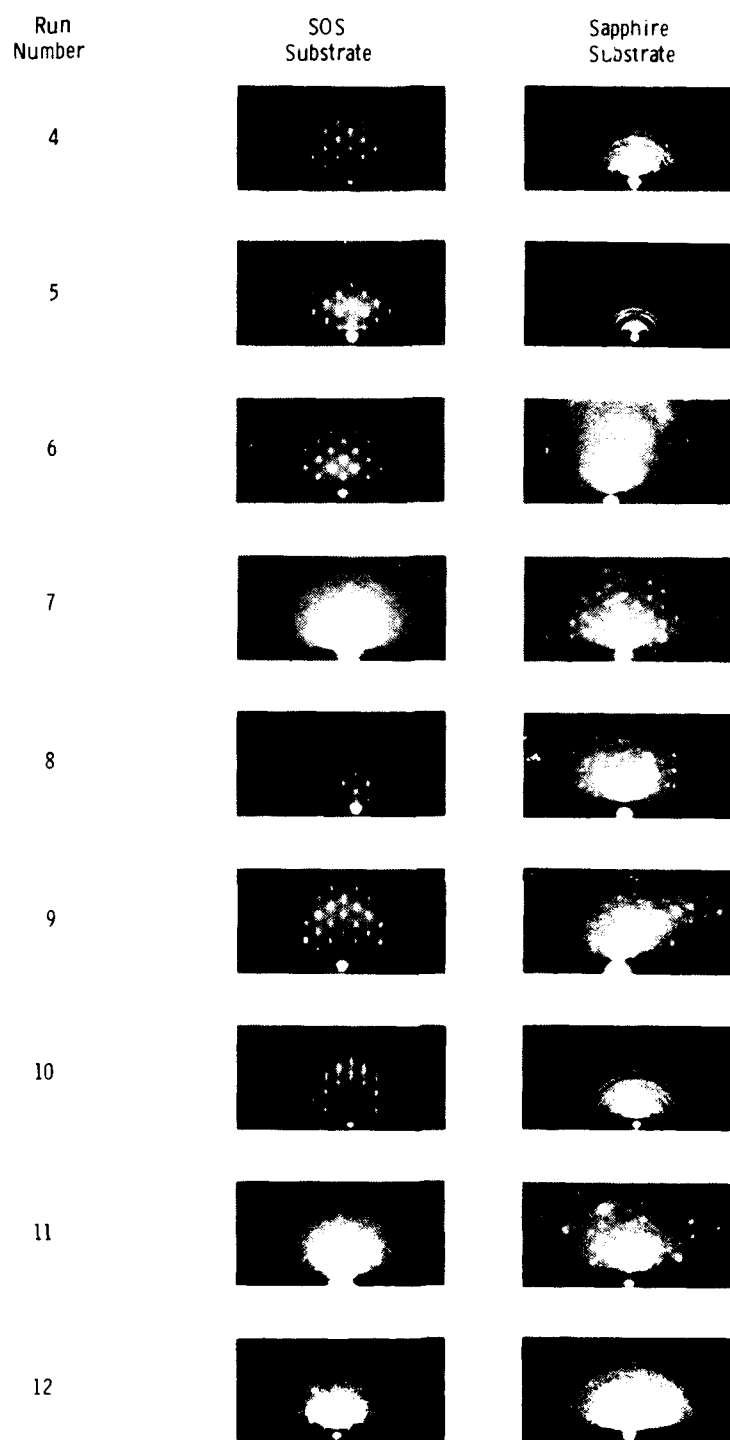


Figure 1. RHEED patterns from SOS and sapphire samples in a series of nine MOCVD runs.

indicating either fine-grain polycrystalline material, or large-grain poly with an odd surface orientation. The conclusion is that epitaxial deposition is relatively easy to obtain for GaAs films being grown on the silicon surface of an SOS wafer, but relatively more difficult to obtain on the $1\bar{1}02$ sapphire surface. With this preliminary result, the next series of runs was directed to SOS wafers and wafer sections, and silicon substrates, in order to pursue the most promising approach.

2.2 COMPARISON OF SOS AND SILICON SUBSTRATES

An experiment was initiated to compare GaAs layers grown under the same preparation conditions on SOS, (100) silicon, and tilted (100) silicon substrates. The samples were all two-inch wafers. The SOS wafer was purchased from Union Carbide. The (100) silicon wafer was a p-type Cz sample of 10 ohm-cm resistivity, purchased from Wacker. The tilted (100) silicon sample, purchased from Virginia Semiconductor, has a surface plane orientation specified as four degrees off from 100 toward 110. The samples were cleaned by the same procedure, and the MOCVD runs were identical and consecutive. The cleaning was comprised of an RCA type treatment, with an HF dip immediately before insertion into the MOCVD reactor. The MOCVD run began with a hydrogen prebake at 800°C, followed by growth of a nucleation layer at 420°C. The sample temperature was ramped up to 600°C, and the final layer thickness of 1.5 μm was reached in a single step.

The surfaces of all three samples are shiny, but nonuniform. There are scattered spots and gray areas near the edges of all three samples. The surface of the SOS sample has a very light cloud, in visual appearance, while the tilted silicon sample has a slightly stronger cloud. The (100) sample also shows a very light cloud extending inward to the center from a gray patch near the edge. Photomicrographs of the surfaces, shown in Figure 2, indicate a light surface texture, along with a scattering of defects that appear to be pits. The density of defects is comparable on the SOS and tilted



Si (100)



Tilted
Si (100)



SOS

50 μ m

Figure 2. Optical micrographs of GaAs epilayer surfaces on three different substrates.

silicon samples, and lower on the (100) silicon sample. At this point, the quality of all three samples seems comparable. More detailed characterization and comparison is planned.

2.3 ORIENTATION OF SAPPHIRE SUBSTRATES

Although it is not practical to plan an experiment with tilted sapphire substrates, there is a range of orientations to be expected within the standard specification of SOS wafers. Accordingly, by checking the orientation of some wafers, the epilayer characteristics can be back correlated to the surface plane orientation. Several SOS wafers, with GaAs epilayers deposited by MOCVD on the surface, have been checked by x-ray diffraction. An example of the result for one wafer is shown in Figure 3. The wafer was placed on a goniometer mount, and a laser setup was used to ensure that the surface of the wafer was normal to the incident x-ray beam. The slight shifting of the Laue backscattered spot pattern indicates that the substrate surface plane is tilted about 1.9 degrees from the just $1\bar{1}02$ orientation. Further characterization and correlation with the epilayer quality is still under way.

2.4 SUBSTRATE CLEANING

Proper cleaning of the substrate surface is expected to be an important factor affecting epilayer quality. An experiment was conducted to observe the effect of cleaning. In this procedure, a series of MOCVD runs was carried out with similar sets of substrates. Each run contained six samples, 1 cm square in size, arranged within the two-inch space available in the MOCVD reactor. Three of the samples had silicon epilayers, while three of them were bare sapphire substrates. One each of the SOS and sapphire samples was given a minimal cleaning by rinsing in solvents. One each of the SOS and sapphire samples was given a stringent cleaning, starting with the solvent rinse, followed by immersion in hot $\text{HCl}:\text{H}_2\text{O}_2:\text{H}_2\text{O}$, followed by immersion in hot $\text{NH}_4\text{OH}:\text{H}_2\text{O}_2:\text{H}_2\text{O}$, and completed by rinsing in DI water. This procedure

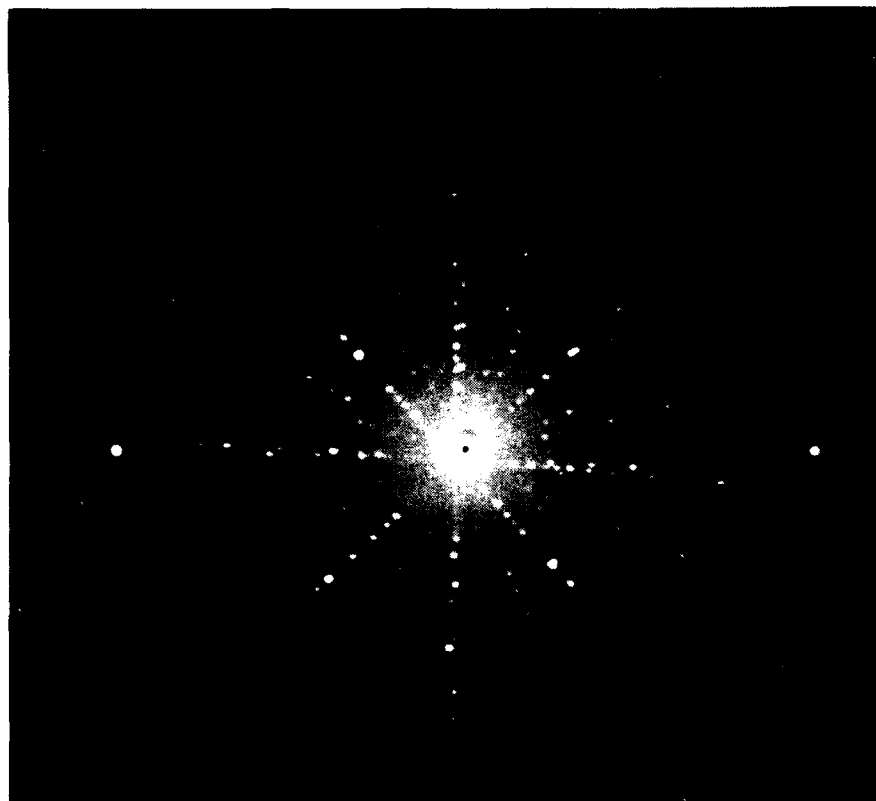


Figure 3. Laue backscattering pattern from GaAs epilayer on SOS substrate.

has been used successfully for cleaning samples prior to gate oxidation. The third SOS sample was prepared by etching about 100 nm of the silicon epilayer away, using $\text{HNO}_3\text{:H}_2\text{O:HF}$ in 20:20:1 proportions. Similarly, the third sapphire sample was prepared by using the same etchant to completely remove the silicon epilayer from an SOS sample.

The MOCVD run parameters covered a wide range of conditions. After each run, the samples were evaluated by visual inspection, followed by Nomarski microscope examination. Selected samples were submitted for RHEED characterization.

The results may be summarized according to the type of substrate. The sapphire samples were typically gray in appearance, and some of them had a dull matte surface. Generally, the sapphire samples that received the stringent clean, or were stripped SOS samples, had a better surface appearance. The best samples, having a gray surface with a shiny background, and RHEED patterns without rings, were stripped substrates. Further consideration of surface cleaning will be required for sapphire samples, as none of the samples in this sequence had good GaAs epilayers.

The SOS samples in this sequence showed a clear difference according to cleaning method. The casual clean samples all had gray surfaces. Some of the stringent clean samples had shiny surfaces, depending on the MOCVD run conditions. The partial strip samples also had shiny surfaces. RHEED patterns from the shiny samples had well-defined spot patterns with no ring or ring arcs, indicating GaAs epilayers had been grown. The partial strip method gave a slightly higher yield of good epilayers, but the stringent clean procedure is also acceptable.

2.5 IN-SITU PRETREATMENT

The objective of the pretreatment is to create a surface condition which allows the most perfect initial growth of the deposited layer. To this end, methods for the removal of the last traces of dirt or contamination from the surface are important. Also, methods that

alter the chemical condition of the surface for more complete and uniform initial deposition are included.

In an early experiment, the effect of a prebake in hydrogen at 800°C before deposition was evaluated by comparison with MOCVD runs in which the hydrogen prebake was omitted. On SOS substrates, the RHEED patterns showed epilayer growth in both cases, but the surface was shinier and the defect density was lower for the sample that received the hydrogen prebake. The improvement is attributed to removal of the last traces of surface oxide, providing a cleaner, more uniform silicon surface for the initiation of growth on the sample that had the prebake. For sapphire samples, the hydrogen prebake had no observable effect. Due to the favorable result with silicon surface treatment, the hydrogen prebake at 800°C was adopted as the standard pretreatment for SOS and silicon substrates.

Pretreatment of sapphire substrates with exposure to trimethyl gallium (TMG) was tried on two occasions. The first run procedure included the normal drying cycle at 300°C in hydrogen, followed by ramping to 600°C and exposure to TMG for one minute before the arsine flow was turned on. The growth then proceeded normally at 600°C for 18.5 minutes for a target GaAs layer thickness of 1.5 μm . The comparison run included the drying cycle, temperature ramping to 620° and a six-minute prebake in arsine, then growth of a 1.5 μm thick layer. RHEED patterns from the two runs are shown in Figure 4. The TMG sample shows a clear primary spot pattern, with many extra spots as well as rings being present. This material is polycrystalline, with a strong tendency for the grains to select a fixed orientation with respect to the substrate. The comparison sample has a stronger primary spot pattern, fewer extra spots, and only traces of ring arcs. Neither of these samples represents a good-quality GaAs epilayer, but the RHEED patterns indicate that the TMG pretreated sample is not as good as the comparison sample.

A second experiment was carried out, with a two-inch sapphire substrate being heated to 650°C in hydrogen and held for 20 minutes,

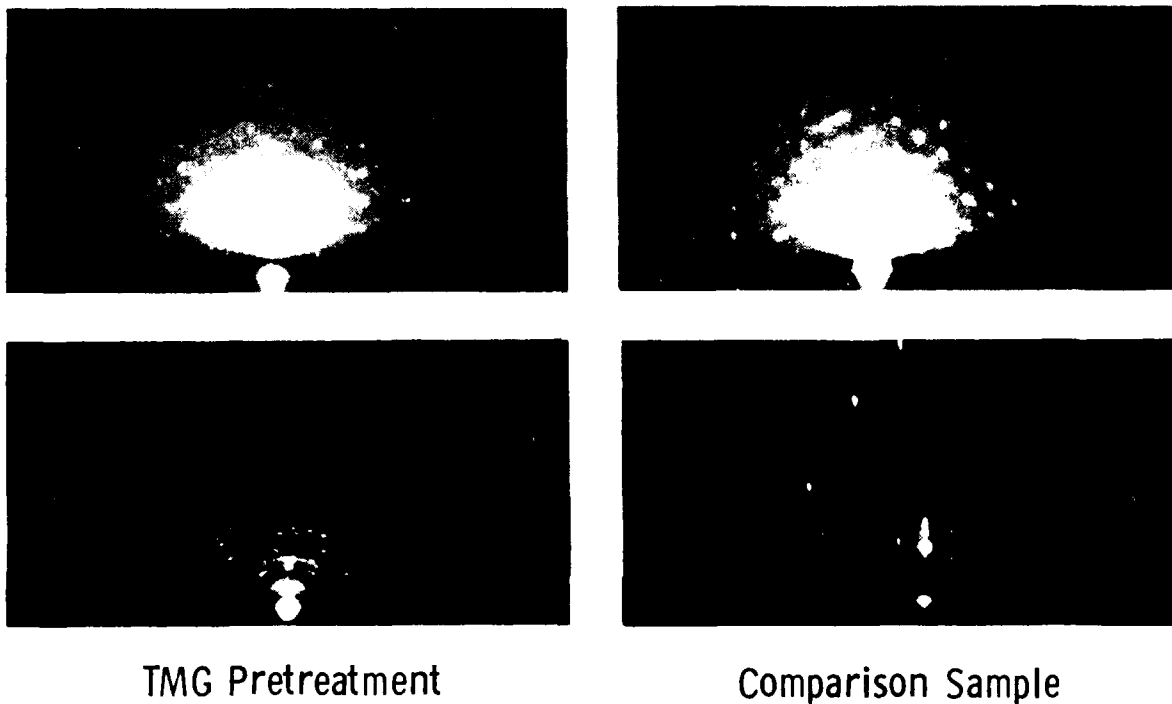


Figure 4. RHEED patterns from sapphire samples showing the effect of TMG pretreatment.

then exposed to TMG for two minutes before the arsine flow was turned on. A 1.5 μm thick GaAs layer was deposited. The comparison wafer was prebaked in arsine at 750°C for six minutes, then the temperature was lowered to 650°C, and the TMG flow was turned on to grow a 1.5 μm thick GaAs layer. In visual appearance, the wafers were clearly different. The TMG wafer is dull gray in color, with only a trace of background shine, while the comparison wafer is shiny with a gray cloud. The RHEED patterns from the wafers are shown in Figure 4. Once again, the TMG treated wafer has scattered spots and rings, indicating polycrystalline structure with a small grain size and little tendency toward orientation with respect to the substrate. The comparison wafer has a strong spot pattern with no rings, clearly showing a better crystal structure.

Surface pretreatment with trimethyl aluminum (TMA) was also studied. A sapphire wafer was heated to 700°C in hydrogen and exposed to TMA flow for two minutes. Layer deposition was initiated by turning on TMG and arsine flow for 1.5 minutes, after which the TMA flow was shut off, and a 1.5 μm thick GaAs layer was deposited. The deposited layer thus has a thin AlGaAs layer at the substrate interface, with a thick GaAs layer on top. The surface of this sample was dull gray in appearance, and micrographs showed a rough and grainy texture. This was judged to be an unsatisfactory result, and no RHEED plates were made.

2.6 GROWTH OF NUCLEATION LAYER

The method of growth in two steps with deposition of a nucleation layer was investigated for SOS and sapphire substrates. For SOS samples, the surface was given a stringent clean or partial etch, and a final HF dip immediately before insertion into the MOCVD reactor. The first deposition took place at 420°C to a layer thickness of 20 to 50 nm. The temperature was ramped up to 600 or 620°C, and the final layer thickness was attained in a single deposition step at that temperature. In some cases, a separate anneal step was inserted by holding the sample at 600°C for 20 minutes in flowing arsine before starting the final growth step. In most cases, the temperature ramp

from 420 to 600°C, which itself takes about 20 minutes, was considered to provide an adequate anneal for the nucleation layer. Such samples were compared to SOS substrates with GaAs epilayers grown at constant temperature by single-step procedures.

The results of this comparison are shown in Figure 5. The comparison sample has a GaAs layer grown in a single step at 600°C in a procedure similar to that used for GaAs epitaxy onto GaAs substrates. The RHEED patterns for both samples show clear spot patterns and no trace of rings, indicating good epilayer quality. There is some tendency toward streaking of the spots along a vertical axis, indicating a relatively smooth surface. The surfaces are shown in the optical micrographs in the same Figure. The nucleation layer sample has a flatter surface and smaller defects than the single-step sample, although the defect density is high in both samples. In visual inspection, the nucleation layer sample has a shiny surface, while the other sample has a gray, cloudy surface appearance. Because of the better surface morphology obtained using the nucleation layer procedure, the major sequence of MOCVD runs was aimed at optimizing the two-step run conditions for best surface morphology. Single-step growth procedures also provide good crystalline epilayers and will be investigated as time and resources permit.

Sapphire substrates were included in 11 runs involving nucleation layers, either as whole wafers or as smaller samples included with other substrates. RHEED plates are available for six of these runs. The RHEED patterns exhibit rings with no spots in evidence, for all $1\bar{1}02$ sapphire samples. Only one sapphire substrate of 0001 orientation showed a pattern of spots, and in that case the pattern was irregular, indicating polycrystalline material. This result is borne out in a run that included only the nucleation layer growth and the anneal at 620°C, leaving only a 50 nm surface layer of GaAs. The $1\bar{1}02$ sapphire sample from this run showed only rings in the RHEED, as shown in Figure 6, while an SOS sample from the same run showed a well-defined spot pattern with no rings. The remaining sapphire samples, for which

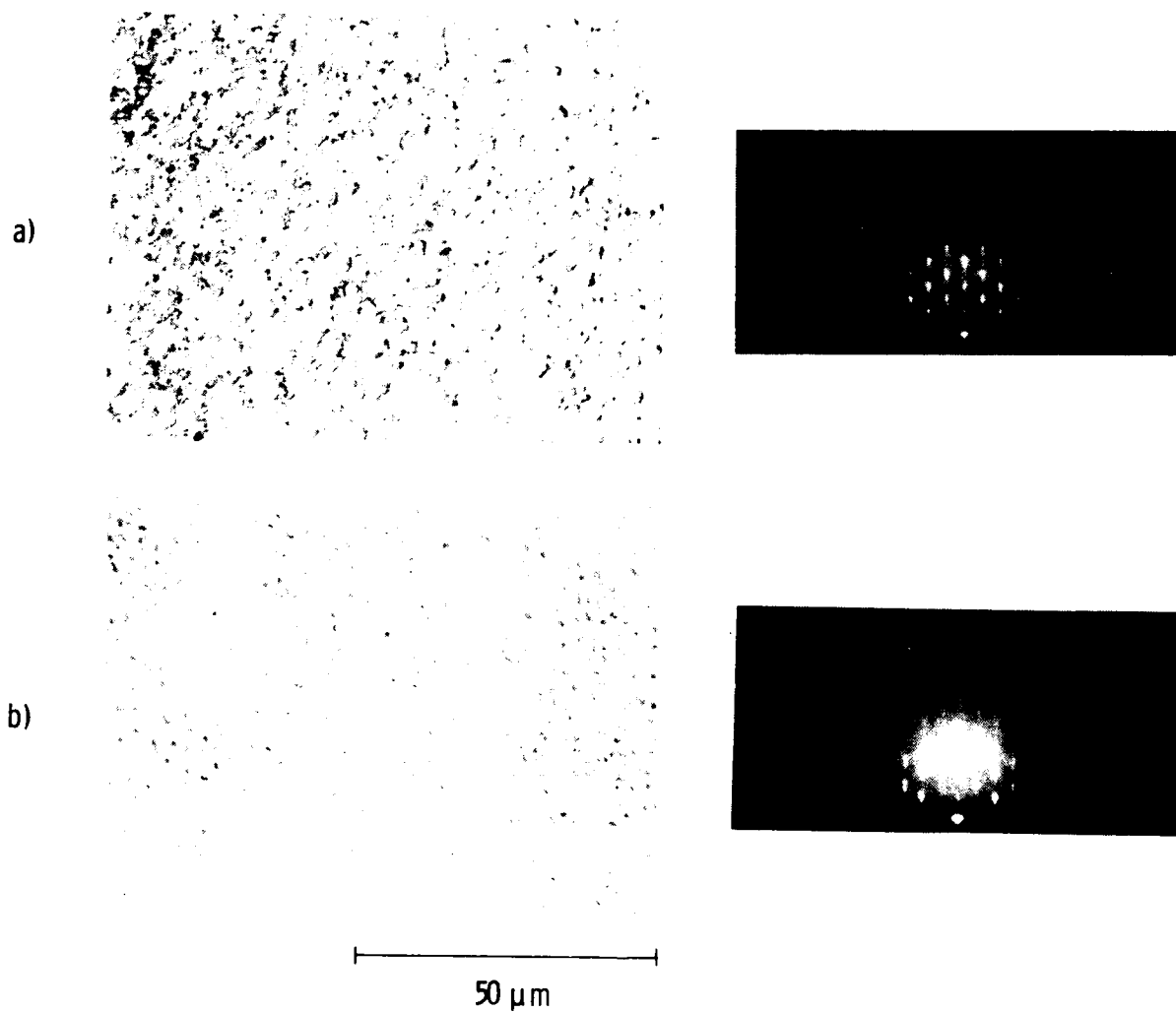


Figure 5. Comparison of the surface appearance and RHEED patterns of GaAs epilayers grown in a single step (a), and by the two-step nucleation layer process (b).



SOS
Substrate



Sapphire
Substrate

Figure 6. RHEED patterns from thin GaAs layers grown using the nucleation layer deposition and anneal steps of the three-step process.

RHEED plates have not been taken, have rough surfaces as viewed in the microscope. The UVS haze scans show high haze levels and no peaks that would indicate crystalline texture. All of the evidence is consistent with the result that only fine-grain polycrystalline GaAs has been obtained in all attempts to use the nucleation layer method on sapphire substrates. Accordingly, the major sequence of MOCVD runs on sapphire substrates has been directed toward investigating single-step procedures.

2.7 GROWTH RATE

The influence of the deposition rate was investigated in two experiments. The first experiment included SOS and sapphire substrates, with deposition at a constant temperature of 620°C. For the reference sample, a 1.5 μm thick layer was grown at the standard rate of 1.4 nm/second. Initial deposition was lower by a factor of ten on the second sample, for the first 50 nm, and then the standard rate was resumed by increasing the flow rate of TMG. A third sample had the initial growth rate increased by a factor of four to grow the first 50 nm layer, followed by deposition of 1.5 μm of GaAs at the standard rate. The variation in growth rate thus affects only the first layer to grow.

The SOS samples all had reasonably good RHEED patterns. The sample with slow first growth had weak subsidiary spots near the strong spots of the principal RHEED pattern, showing a high density of coherent crystal defects such as twins. The other two samples had good RHEED spots with some tendency toward streaking in the vertical direction, as expected for a relatively smooth surface. Visual inspection shows that the slow first growth sample is gray in appearance due to a rough surface, while the other samples are shiny with a gray cloud. The sample with the fast initial growth has some very shiny regions. It is concluded that a fast initial deposition may have advantages, but that uniformity may be harder to achieve. The quality of the GaAs layer was not as good as that obtained from the two-step process, with the nucleation layer grown at a lower temperature.

Sapphire samples were also included in the growth rate study. The slow growth procedure resulted in incomplete surface coverage in two of three sapphire samples in the run. Slow initial growth thus seems to interfere with nucleation during the subsequent standard rate deposition during the same run. This could be due to surface modification, or possibly due to improper cleaning of the sample for this run. Comparing the RHEED patterns for the sapphire samples, it is seen that the reference sample has extra spots and rings, indicating polycrystalline material with a tendency to orient on the substrate. The slow initial growth sample has a strong spot pattern with no rings, but the pattern is irregular, possibly due to an unusual orientation of the GaAs layer. The fast first-growth sample has extra spots but no rings, showing oriented large-grain poly GaAs. The initial growth rates are clearly important for the sapphire substrates, but proper control will require further experiments.

Rate variation was combined with the two-step process in experiments on whole SOS wafers. Nucleation layers about 50 nm thick were deposited on each of two wafers at 420°C. The temperature was raised to 750°C, and a final layer about 1.5 μm thick was deposited. On the reference wafer, the standard rate of 1.4 nm/second was used, while the growth rate was reduced to 0.3 nm/second for the second wafer. The wafers are nearly identical in appearance, although the slow-growth wafer has a number of shiny regions near the rim that are absent on the reference wafer. The UVS haze traces for the wafers are also nearly identical, showing four peaks and a moderate haze level. Evidently, the growth rate is not a major factor governing the layer quality under the conditions specified.

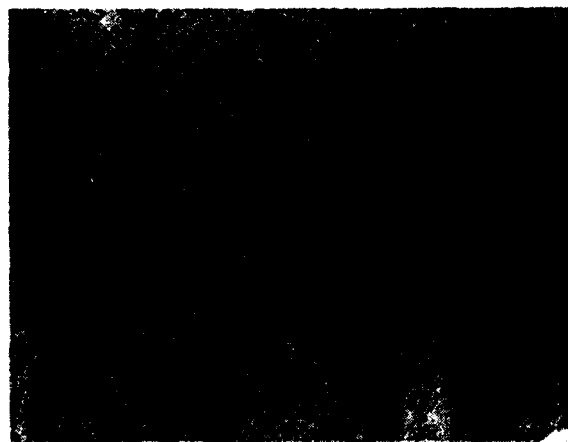
This experiment was repeated with a reduced final layer thickness, to investigate the evolution of the GaAs layer characteristics during the growth. Again, the two-step process was used, with the nucleation layer being deposited at 420°C. The final layer deposition temperature was 750°C, and the target thickness was 300 nm. The growth rate for the reference wafer was 1.4 nm/ second, and the

intended growth rate for the second wafer was 0.3 nm/second. In visual appearance, the slow-growth wafer is much shinier, but this is mainly due to a difference in the layer thickness between the wafers. The wafers were masked with wax and etched to the silicon layer to provide edges for the measurement of the GaAs layer thickness. The reference wafer had a 360 nm thick layer, while the slow-growth wafer had a 280 nm thick layer. The discrepancy may be due to an incorrect calibration of growth rate for a given TMG flow rate. Comparison by UVS haze scattering showed that the reference wafer has a much higher haze, with four peaks evident, while the slow-growth wafer had moderate haze with two peaks. This result shows that the growth rate seems to be important during the early growth of the layer. This is apparently inconsistent with the result for the 1.5 μm layers described above. Further study will be required to resolve this matter.

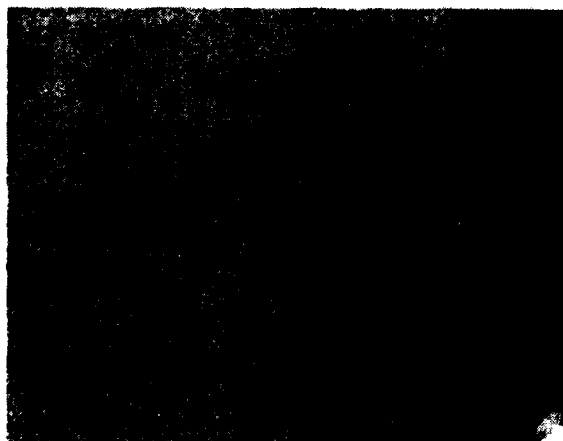
2.8 TEMPERATURE OF GROWTH

Having adopted the two-step process as the most promising approach for GaAs deposition onto the silicon epilayer of SOS wafers, the temperature of the final layer growth remains to be optimized. A sequence of MOCVD runs was planned to cover a range of temperatures and to determine which yielded the best GaAs layer. Intact two-inch SOS wafers were used to provide information on the uniformity of the deposition. The wafers were cleaned using the partial etch procedure, with a final HF dip immediately before loading into the MOCVD reactor. The high-temperature prebake at 800°C in hydrogen was employed for all runs in this sequence. The samples were cooled to 420°C for the nucleation layer deposition to a thickness of 50 nm, the temperature was ramped up to the final layer deposition temperature, and deposition was started at the standard rate of 1.4 nm/second with no separate anneal period. Layers were grown to thickness targets of 300 nm and 1.5 μm to provide data on the evolution of the layer structure.

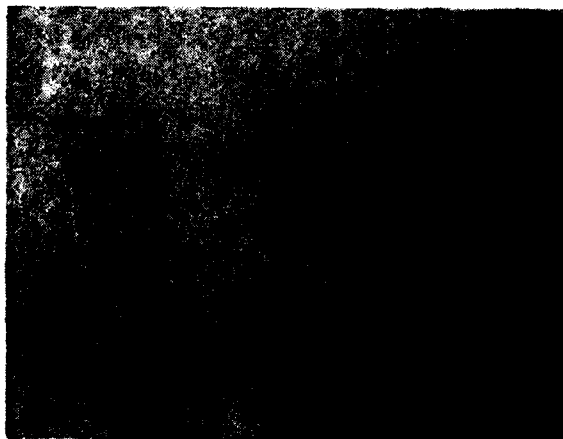
A comparison of the surfaces of three wafers with 300 nm thick layers grown at 600, 650, and 700°C is shown in Figure 7. The GaAs



700°C



650°C



600°C

50 μ m

Figure 7. Optical micrographs of 300 nm thick GaAs epilayers grown at different temperatures on SOS substrates.

layer surfaces are shiny; high magnification shows that the fields are flat but with a varying density of defects that appear to be small pits. The defect density is highest for the 700°C growth, and lowest for the 600°C growth. RHEED patterns from the 650°C wafer show a clear spot pattern with a tendency toward vertical streaking and no sign of rings or extra spots. The UVS haze levels are 3063, 1257, and 269 for the 700, 650, and 600°C wafers, respectively. All of the evidence is consistent in pointing to the lowest temperature of deposition for the final layer as yielding the best quality, at the target thickness of 300 nm.

Thicker layers, more appropriate for device applications, were grown by the two-step process by extending the final growth cycle to reach a target thickness of 1.5 μm . The surface of a wafer with final growth temperature 650°C is shown in Figure 8. The optical micrograph shows a light texturing of the surface, with an appreciable density of pits present as well. The SEM micrograph clearly shows that the pits tend to have faceted surfaces. The density of defects is lower for this thicker layer than in the thinner layers shown in Figure 7. A GaAs epilayer grown at 600°C to a thickness of 1.5 μm is shown in Figure 9. The surface field is very flat with a minimum of texturing. Small pits ranging from about 0.5 to 2 μm in diameter are present at a density of about $8.5 \times 10^5/\text{cm}^2$. This defect density is comparable to that observed in GaAs layers deposited directly onto silicon substrates. The UVS haze level from this sample is 60, lower than most SOS wafers that have been examined.

Sapphire substrates were used for a similar sequence of runs at different temperatures. Since it was previously observed that the two-step process was not successful for bare sapphire substrates, all of the runs in this sequence were carried out at a single temperature. The samples were cleaned, inserted into the MOCVD reactor, dried at 300°C in hydrogen, prebaked for six minutes in arsine at 750°C, and then ramped to the growth temperature. The layer deposition then proceeded without interruption to the final layer thickness of 1.5 μm . Figure 10

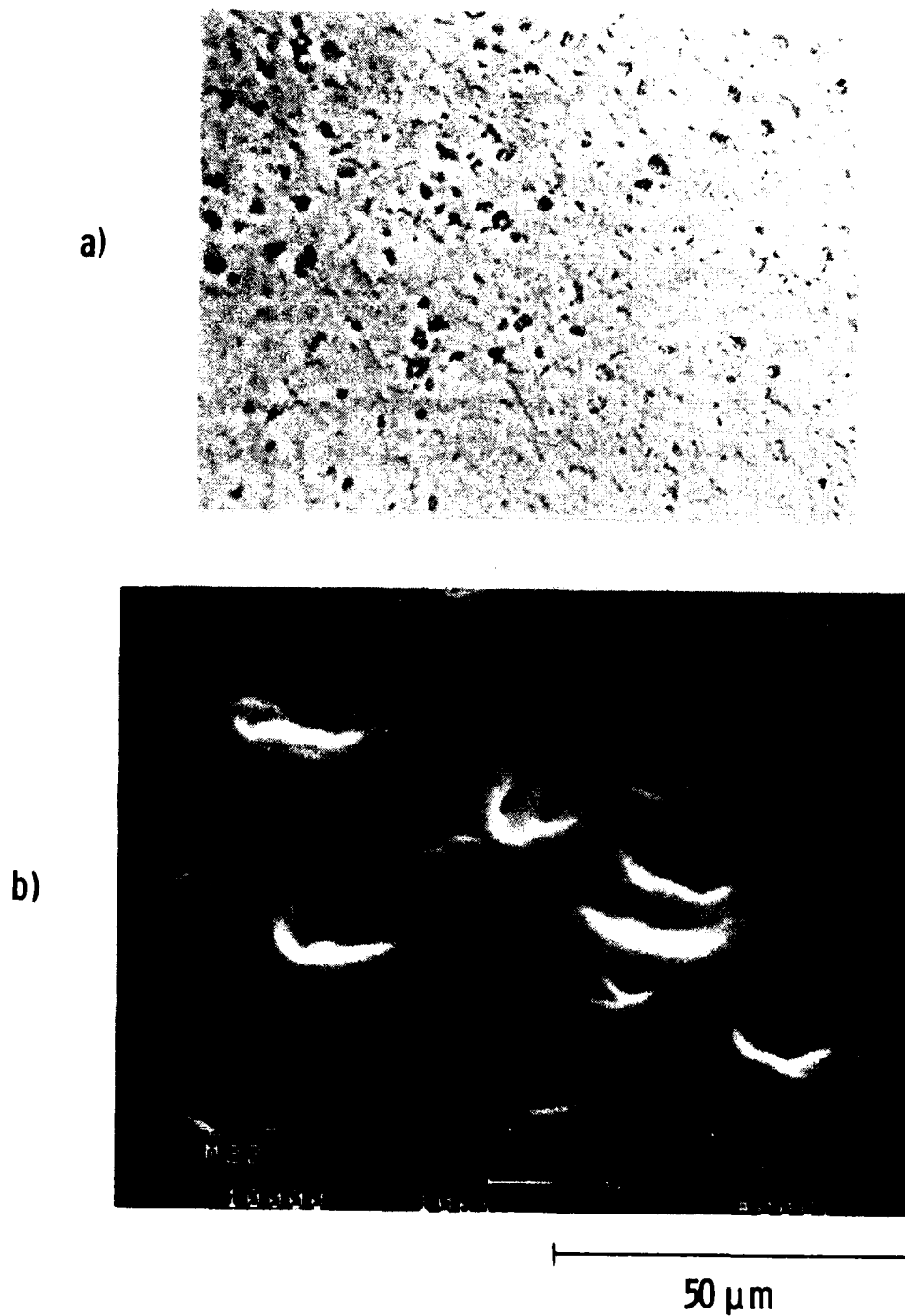


Figure 8. Optical (a) and SEM (b) micrographs of the surface of a 1.5 μ m thick GaAs epilayer deposited at 650°C onto an SOS substrate.

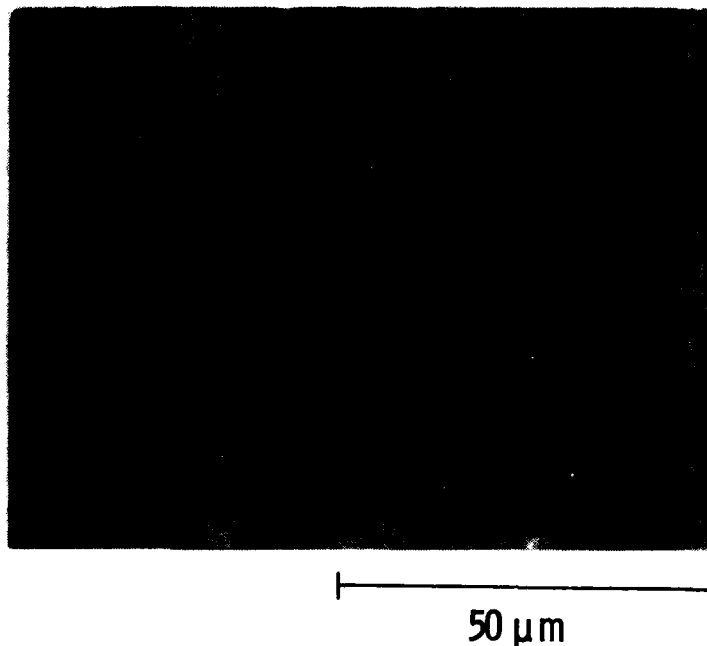


Figure 9. Optical micrograph of the surface of a 1.5 μm thick GaAs epilayer grown at 600°C onto an SOS substrate.

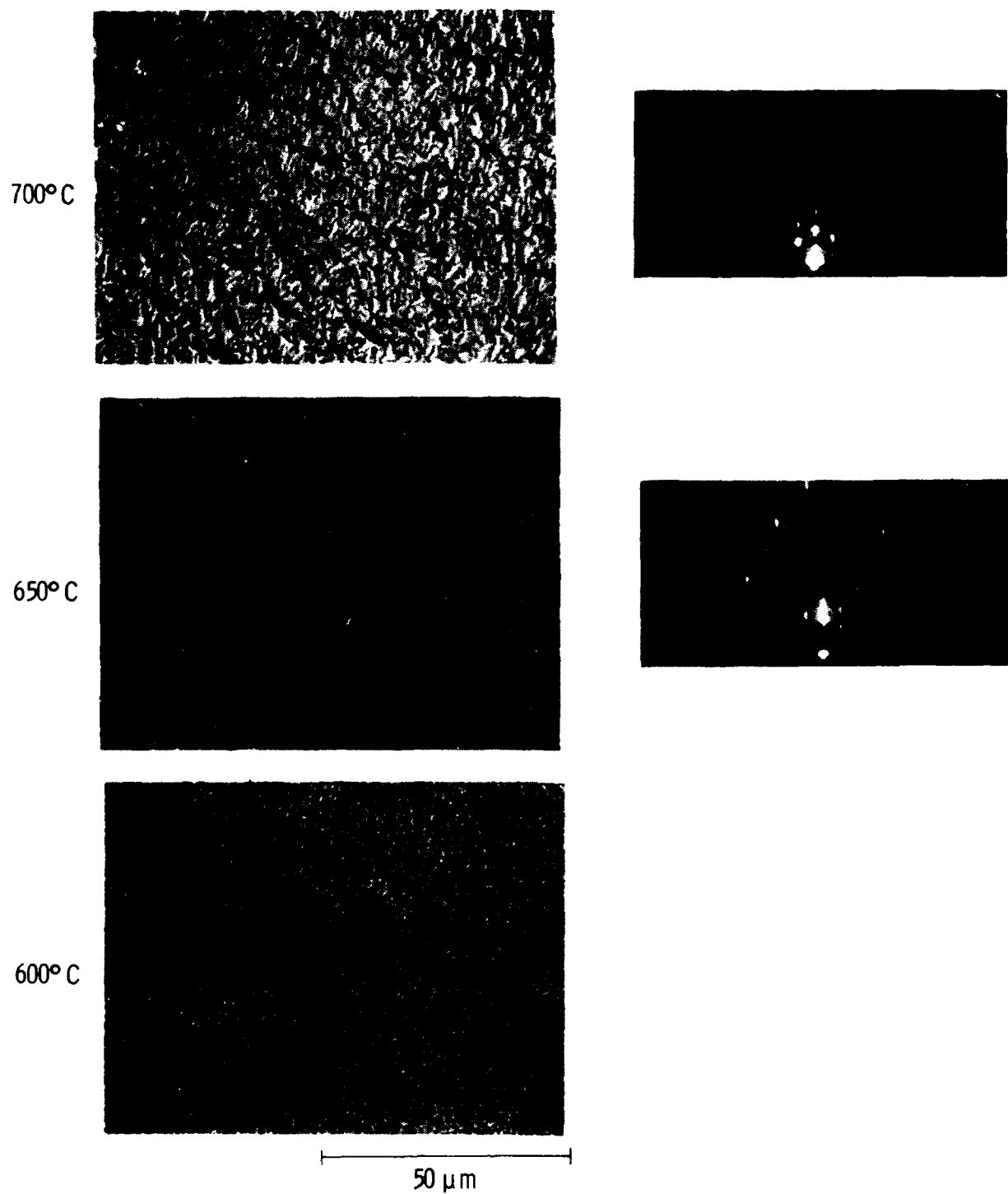


Figure 10. Comparison of the surface appearance and the RHEED patterns of 1.5 μm thick GaAs epilayers grown at different temperatures onto 1102 sapphire substrates.

summarizes the results for depositions at 600, 650, and 700°C. The surfaces of all three wafers show a strong texture that is clearly crystallographic. The RHEED pattern for the 650°C sample has a strong spot pattern with a very weak trace of rings, indicating highly oriented material. The RHEED pattern for the 700°C sample exhibits rings as well as a strong spot pattern. (No RHEED patterns are available at this time for the 600°C sample.) In appearance, the 650 and 700°C samples are shiny with a gray cloud, the cloud being heavier for the 700°C sample. The 600°C sample is nonuniform, with regions that are shiny along with gray spots and streaks. It appears that this sample was not properly cleaned. The UVS haze data for these wafers are shown in Figure 11. The traces are irregular, showing strong peaks that do not conform to either two- or four-fold symmetry. The texture, RHEED patterns, and UVS haze strongly indicate that the GaAs layer orientation deviates substantially from the (100) plane that is universally observed on silicon and SOS substrates. A more detailed analysis of this material is still under way.

2.9 COMPOSITION OF NUCLEATION AND FINAL LAYER

An aluminum source is available on the MOCVD machine which has been utilized to investigate the effect of layer composition on epilayer quality, primarily for sapphire substrates. By modulating the ratio of trimethyl gallium (TMG) and trimethyl aluminum (TMA), deposited layers of nominal 30 percent and 70 percent AlAs have been grown. The aluminum-rich layers have been employed in single-step deposition processes, two-step processes, and as thin "nucleation" layers under GaAs depositions. The surface texture of the AlGaAs layers compares favorably with the GaAs layers on sapphire substrates. At the present time, there is little more detailed information available about these samples.

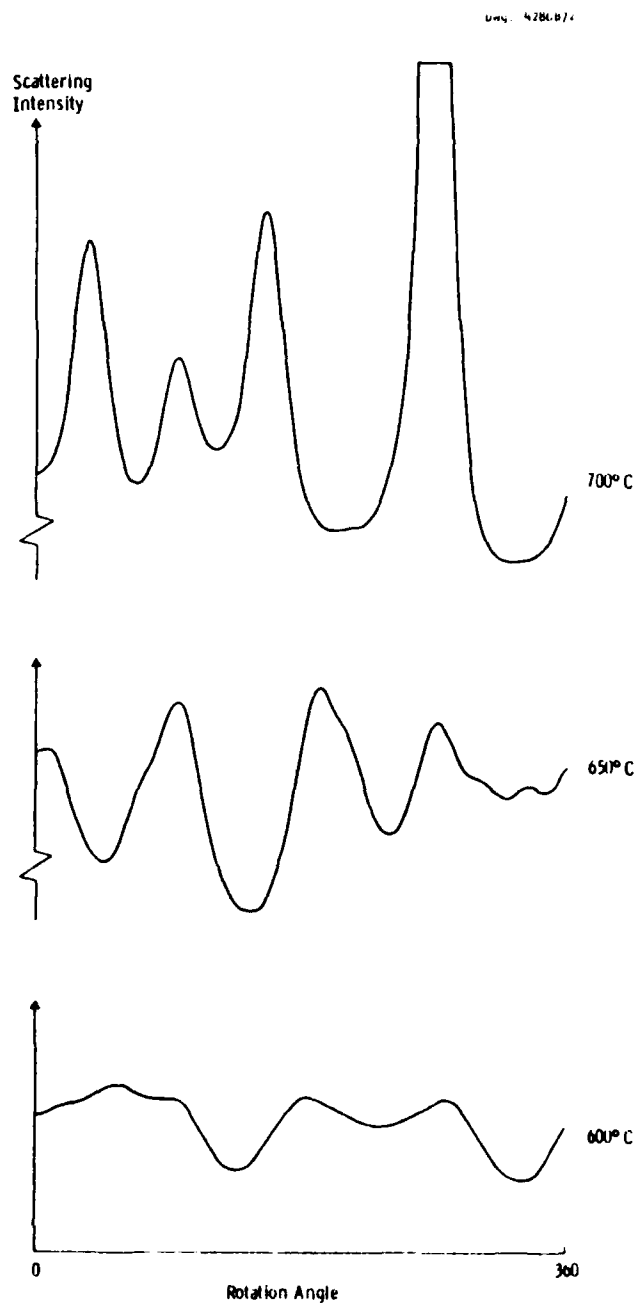


Figure 11. UVS haze traces from 1.5 μm thick GaAs epilayers grown onto 1102 sapphire substrates at different temperatures.

2.10 MULTILAYER STRUCTURE

A sample has been produced to evaluate the potential of multilayer structures to reduce the surface defect density. The SOS substrate was cleaned, inserted into the MOCVD reactor, prebaked in hydrogen at 800°C, and cooled to 420°C. The nucleation layer was grown to a thickness of 50 nm, the temperature was raised to 600°C, and a GaAs layer was deposited to a thickness of 40 nm. Then, an alternating sequence of ten layers each of GaAs and $\text{Al}_{0.2}\text{Ga}_{0.8}\text{As}$ was deposited, each layer with a target thickness of 20 nm. The growth was interrupted for ten seconds at each interlayer transition. Finally, a GaAs layer 1.5 μm thick was grown at the standard rate of 1.4 nm/second. The surface of the sample was lightly textured, with pits ranging up to 2 μm in diameter. The density of defects is about $5 \times 10^5/\text{cm}^2$. This represents a reduction in defect density compared to the solid GaAs layer seen in Figure 9. A further reduction by some orders of magnitude would be desirable for device-quality material. Further characterization of this sample is under way.

3. CONCLUSIONS

At this point in the program, several conclusions can be stated regarding the preliminary findings and the most promising directions for further work.

The deposition of GaAs epilayers onto the silicon epilayer of an SOS wafer has proven to be a relatively robust process, insensitive to variations in substrate orientation, cleaning, preconditioning, growth rate and temperature, and composition of the deposited layer. The optimum MOCVD process, based on the present data, requires partial etching of the silicon epilayer, a high-temperature hydrogen prebake, deposition of a thin nucleation layer at low temperature, and growth of the final layer at a temperature of 600°C. Using this method, good (100) GaAs epilayers have been grown on two-inch SOS wafers. The surfaces are shiny, uniform over the wafer area, low in UVS haze compared to SOS wafers, and of good crystal quality according to the RHEED patterns.

Deposition onto sapphire substrates has not yet given GaAs epilayers of high quality. Although the RHEED patterns indicate that well-oriented material can be obtained for certain deposition conditions, the GaAs surface tends to be highly textured and unsuitable for device fabrication.

The best approach for obtaining device-quality GaAs appears to be through utilization of the silicon epilayer as the base for the GaAs deposition. Accordingly, the major emphasis will be placed on the thorough characterization of the structural and electrical properties of GaAs/Si/sapphire samples. The key issue of the defect density in the surface region of the GaAs layer will be addressed by using cross-section TEM to determine the nature, density, and distribution of

crystallographic defects. The electrical quality will be assessed by fabricating test structures for Hall-effect mobility measurements. The MOCVD deposition conditions and the structure of the deposited layer will be further optimized.

At the same time, experiments will be carried out to improve the quality of GaAs layers deposited directly onto sapphire. The nature of the early growth will be studied by depositing very thin layers under different conditions, to identify methods for obtaining smoother, more uniform layers of the principal (100) or (111) orientations.

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