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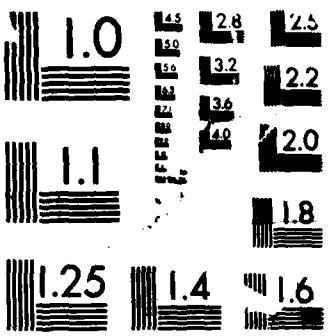

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This research program investigates the effect of extreme submicron spatial modulation of the electrostatic potential on the transport in a two-dimensional electron gas (2DEG) in silicon and in III-V compound semiconductor devices. The test vehicle is the so-called grating-gate FET (GGFET). When made to move in a direction perpendicular to the potential modulation, i.e., perpendicular to the grating gate, electrons experience a surface superlattice (SSL) effect. When moving along the potential modulation electrons are restricted to only one degree of freedom, and thus constitute a quasi-one-dimensional (Q1D) system. Our major achievements in the past year include:

In silicon we have fabricated, with high yield, grating gate transistors and measured their current voltage characteristics at liquid helium temperatures. The device mobility at 4 K is about 15000 cm^2/Vs, possibly the highest reported for MOSFETs fabricated using e-beam or x-ray lithographies.

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In III-V compounds we have built our first working GGHEMT devices in GaAs-GaAlAs MBE layers grown at MIT. The device characteristics are good at room and liquid nitrogen temperatures and will be measured at helium temperatures as soon as fixtures for overcoming persistent photoconductivity effects are completed.

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STUDY OF QUANTUM MECHANICAL EFFECTS IN DEEP SUBMICRON, GRATING-GATE FIELD EFFECT TRANSISTORS

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This research program investigates the effect of extreme submicron spatial modulation of the electrostatic potential on the transport of 2-D electrons in silicon and in III-V heterojunction semiconductor devices. The test vehicle is the so-called grating-gate FET (GGFET). When electrons are made to move in a direction perpendicular to the potential modulation, i.e., perpendicular to the grating gate, they experience a surface superlattice (SSL) effect. When moving along the potential modulation electrons are restricted to only one degree of freedom and thus constitute a quasi-one-dimensional (Q1D) system.

As a result of the past year's effort we now have working devices in both silicon and III-V compounds. To date we have focused our efforts both on the measurement of those devices at low temperatures and on improvements of the fabrication technology. Our progress is described below.

A. Silicon GGFETs

Our efforts over the past year have focused on fabricating and characterizing surface superlattice (SSL) and quasi-one-dimensional (Q1D) grating gate field effect transistors (GGFET). The first working devices were completed in June 1987. Device yield is good due to the processing improvements described below. We have also achieved our goal of building very high mobility MOSFETs despite prolonged exposure to x-rays during fabrication. We anneal x-ray damage in vacuum at 950 ^{o}C without deterioration of the gate wires due to either oxidization or growth of large grains. Our experiments last year in the metallurgy of various refractory metal combinations was crucial to the development of this technology. The inversion layer electron mobility for our devices was measured to be about 1000 cm^2/Vsec at room temperature and 15000 cm^2/Vsec at 4.2 K. These devices are possibly the highest mobility

MOSFETs made using either e-beam or x-ray lithography. High electron mobility is needed to obtain the long elastic and inelastic diffusion lengths necessary to observe features in conductivity due to the wave nature of the electrons.

The silicon GGFET's dual-stacked gate MOS structure is very advantageous for experiments involving both the SSL and Q1D GGFET. In the case of the SSL, the dual gate allows independent control of the average electron density in the inversion layer and of the strength of the periodic modulation. In Q1D devices the dual gate allows the formation of inversion strips between gate wires. This permits easy control of the inversion layer width. The feature distinguishing the Q1D GGFET is its relative insensitivity to the reproducible but sample specific fluctuations characteristic of other MOSFETs built to study electronic conduction in single narrow inversion layers. The signal-to-"noise" ratio should increase as one over the square root of the number of incoherent regions in the device. The primary feature which distinguishes the SSL GGFET from other superlattices, such as those fabricated using molecular beam epitaxy, is that both the strength of the periodic modulation and the Fermi level can be controlled independently. In sharp contrast to systems attempting to emulate static crystal properties, the SSL GGFET functions as a voltage controlled crystal.

We search for a weak modulation in the GGFET conductance at low drain-to-source voltages. A lock-in amplifier allows high signal-to-noise measurement, either of the conductance or of the transconductance. In our direct measurements of transconductance we observe reproducible structure on planar as well as GGFET devices, which we believe to be the so-called "universal" conductance fluctuations of Lee and Stone. They are unavoidable in any metallic system with a finite mean free path. Any desired features in conductance, such as those from one-dimensional sub-bands or electron back diffraction from a periodic potential, must be larger than the characteristic size of the natural conductance fluctuation background to be observed.

A strong modulation of the silicon inversion layer requires strong control of the device current from both gates. Two deficiencies in the first devices we have completed are (1) the grating appears to have wide lines and narrow spaces, and (2) the top gate is relatively far away from the inversion layer (2000 Å). Thus the top gate does not have as strong a control as in the earlier devices of Warren. We understand this as a competition of fringing fields in the region between grating wires. While continuing measurements of our current devices, we are fabricating new GGFETs with small wire widths and upper dielectric thickness of 500 Å.

In the past year we have also come to better understand the criterion for observing a weak modulation in conductivity from one-dimensional confinement or an impressed periodic potential. Destruction of electron wave effects comes from averaging the conductivity over each incoherent region of the sample. If the inelastic length is long compared to the sample size, the conductivity or density of states does not have to be averaged over a width in

energy $\hbar/\tau$, where τ is the elastic mean free time. The subtle point here is that inelastic processes give rise to a broadening whose width is determined by the elastic mean free time. The broadening is called elastic, yet depends on the existence of inelastic processes.

At low enough temperatures, the inelastic length can be almost arbitrarily long. If the inelastic length can be made comparable to the sample size, any fundamental objections about observing features in conductivity resulting from energy states spaced less than $\hbar/\tau$ apart are removed. Additional elastic impurity scatterers in the superlattice transistor may simply give rise to localized states in the energy gap, similar to the doping of a semiconductor crystal. In the one-dimensional transistor, elastic impurity scatterers will simply shift the sub-band positions in energy but will not broaden them.

The device processing improvements we developed last year are responsible for our high device yield and electron mobility. These improvements include (1) adopting the local oxidation of silicon (LOCOS) device isolation process as opposed to the previous planar device process; (2) developing a deep-UV lithography system to expose PMMA, thus allowing simultaneous formation of the grating gate contacts and of the grating by a single electron beam evaporation of the refractory metal; (3) finding a capping material which prevents oxidation of refractory metal grating lines during high temperature vacuum anneal. Improvements (1) and (2) eliminated the shorting between grating gate and substrate, (1) by placing the grating gate contacts over a thick field oxide, and (2) by making the grating gate contact a reliable etch stop. Improvement (3) accounts for our high device mobility. These process improvements are described in detail in last year's report.

In addition to the above process technology for the SSL and Q1D GGFETs, we have explored improvements in our lithography techniques. Using a scanning electron beam lithography tool at IBM's T. J. Watson Research Center, we fabricated x-ray masks containing a variety of x-ray patterns, some with linewidths as fine as 500 Å. We replicated these x-ray masks at MIT with high fidelity. In the future we should be able to work with a variety of new device patterns, assuming continued access to an e-beam system. In order to use x-ray masks written using electron beams in our silicon device work, we must still solve the problem of x-ray mask coarse alignment. In parallel, we are investigating the feasibility of using the MIT focused ion beam system for doing lithography work.

We have also demonstrated a new achromatic holography technique for generating gratings of 1000 Å (i.e., 500 Å linewidth). This is half the spatial frequency of our current gratings. Such ultra-fine gratings should greatly enhance the quantum effects we are investigating in both the SSL and Q1D GGFET.

We believe ourselves to be in a position to perform unique experiments in the basic physics of electron transport in macroscopic phase coherent quantum systems. The ultra high mobility and high yield of our initial device fabrication efforts demonstrate the soundness of our GGFET fabrication techniques. We have learned much about the device configuration required for adequate electrostatic control of the silicon inversion layer. We believe that, in our next fabrication run of devices, the electrostatic control will be adequate to observe electron back diffraction from the superlattice as well as one-dimensional sub-bands. We expect to complete our next devices in one to two months. In this same time frame we will also fabricate grid gate devices. The grid gate devices will enhance our chances of observing a modulation in the SSL GGFET conductance.

B. III-V GGFETs

In our work over the past year on the grating gate high electron mobility transistors (GG-HEMT), our efforts were centered around the simulation of the device in the semiclassical regime and on settling on a tenable fabrication procedure. This year we have succeeded in finishing the fabrication of our first GG-HEMTs. The first set of devices are being bonded and packaged for cryogenic temperature measurements.

Early on we ran into the following problems: (1) insufficient material (since we could not grow our own material); (2) poor ohmic contacts betwen source and drain; and (3) lack of diagnostic features in the original mask design.

We were able to solve the first problem by getting one of us (K.I.) trained on the MBE machine available at MIT. With our own fully qualified user, we have been able to grow enough material to work with during the last six months.

The second and third problems were solved by redesigning our fabrication process and mask design. The original procedure involved evaporating the ohmic contact metals (Au/Ge) over the entire wafer. The source and drain pads were defined by a set of etching steps and then alloyed. The resulting surface morphology of the pads was very rough and the contacts behaved in most cases either Schottky-like or were very resistive. We also observed a high leakage current between devices even after a deep mesa etch. Both problems were related to the alloying of Au with Ga and the deep diffusion of Au into the layers. After a separate experiment, we found that the optimum metalization, resulting in both a very smooth surface morphology and a low contact resistivity, has to include a bottom, thin Ni layer (50 Å), a multilayer of Au and Ge capped with Ni and Au. The optimum sintering temperature and time were found to be 450 ^{o}C and 2 minutes, respectively.

Since the presence of the bottom Ni layer was not compatible with our etching process, we had to redesign our fabrication procedure and mask design. Instead of using etching to define our source-drain pads, we now lift off the desired metals. Also, we added diagnostic structures to allow us to determine quantitatively our contact resistance and to test the quality of our Schottky contacts. With this new procedure reproducible low resistance ohmic contacts have been obtained, and the measured leakage current between devices after mesa isolation is maintained in the nA range.

A set of GG-HEMTs has been completed. They have exhibited good transistor behavior at room temperature. Typical values for a 20 μm-channel device are 35 mS/mm transconductance and 0.2 mS/mm output conductance. The threshold voltage varied from -0.1 V on the continuous gate devices to -0.25 V on the grating gate devices. The grown layers had a sheet carrier concentration of 5.0×10^{11} cm^{-2} and a mobility of 7300 cm^2/Vsec and of 70000 cm^2/Vsec at room temperature and 77 K, respectively.

A second and third set of devices are nearing completion. Besides the GG-HEMTs they also comprise quasi-one-dimensional lines defined by x-ray lithography followed by wet etching, and grid gate devices defined by a double x-ray exposure and Ti liftoff. The grid gate has the potential of preventing the carriers from lateral scattering, which should lead to a more pronounced superlattice effect.

After finishing the second and third set of devices we will devote our efforts to low-temperature measurements. More device sets will be then fabricated under the guidance of our evaluation of the present sets. A recent acquisition of two Indium-free mounting blocks for the MBE should facilitate the growth of 2" HEMT layers and our device productivity in the near future.

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