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RELIABILITY ANALYSES OF A SURFACE MOUNTED PACKAGE USING FINITE ELEMENT SIMULATION

Gretchen A. Bivens and William J. Bocchi

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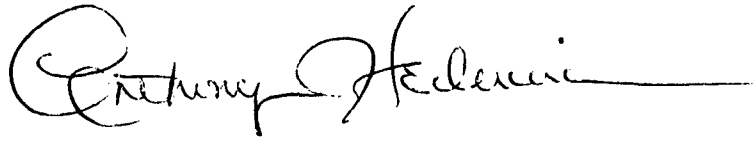
APPROVED: 

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The objective of this study was to evaluate a surface mounted leadless chip carrier to determine if it had met the critical requirements of proper heat dissipation, acceptable thermal stress levels and a minimum temperature rise in the die. Two finite element models were utilized. The first model represented the package/board assembly. This model was used to simulate the effects various die sizes, heat producing areas, and voids in the die attach and thermal undercoat on the package thermal resistance. The second model represented a leadless solder connection. The output temperature solutions from the package/board model were then used as input conditions for this solder connection model. Thermal stress simulations were performed on both models to determine if any of the stress values were too high. The results of these simulations were then compared to determine the correlation between changes in the package thermal resistance and stresses in the solder connection.

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PREFACE

The purpose of this effort was to analyze the reliability of a surface mounted device using an advanced thermal analysis technique. The finite element program NISA (Numerically Integrated Elements for Systems Analysis) was utilized. The authors were trained in the use of NISA by the developers of the program, EMRC (Engineering Mechanics Research Corp.).

The authors wish to thank Mr. Eugene Blackburn for his technical assistance, and Mr. Douglas Holzhauer and Mr. James Collins for their assistance in the formulation of the finite element models.

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1.0 INTRODUCTION

The thermal environment that electronic equipment is subjected to and its ability to dissipate heat have a significant effect on the equipment's reliability. Leadless Chip Carriers (LCC) are a packaging concept that is being incorporated in a number of military applications, and Rome Air Development Center (RADC) is concerned with the reliability of such surface mounted devices. A mechanical engineering evaluation team has reviewed a Leadless Ceramic Chip Carrier (LCCC) surface mounted onto a Printed Circuit Board (PCB) to determine if it has met the critical requirements of proper heat dissipation, acceptable thermal stress levels, and minimum temperature rise in the die. Approximately half of this study concentrated on analyzing the overall package/board system and the other half concentrated on analyzing the thermal stresses in the solder connection between the package and the board. Solder connections in surface-mounted devices must perform mechanical support and transfer electrical signals, thus making them an extremely critical component.

We found that under ideal conditions, this surface mounted package/board system has good heat dissipation resulting in a low thermal resistance. However, the heat flow pattern and the expansion resulting from these temperature changes caused high stress levels in the solder connections. These finite element simulations indicate that a low θ_{JC} does not necessarily equate to a highly reliable package. The high coefficient of thermal expansion of the thermal plane connected to the bottom surface of the ceramic board forced the board to expand more than the ceramic package directly above it. This uneven expansion of the surfaces directly above and below the solder connection caused high shear and normal stresses in the solder. Experimental thermal cycling has shown that solder cracks occur at the same locations as predicted by the finite element simulations.

2.0 FINITE ELEMENT ANALYSIS

In order to evaluate this surface mounted package, several computer aided analyses were performed using the finite element program Numerically Integrated Elements for System Analysis (NISA). NISA was developed by the

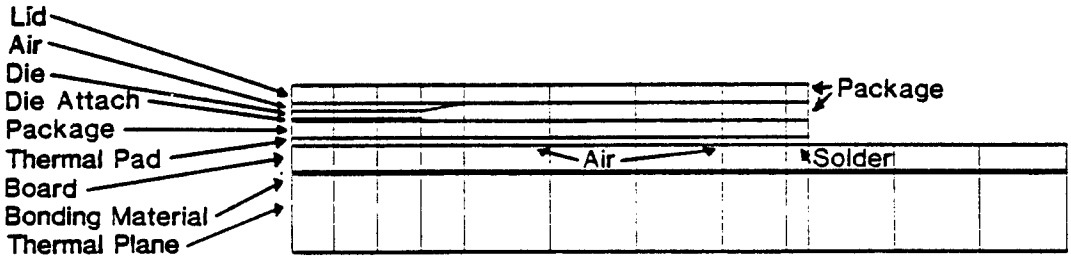
Engineering Mechanics Research Corporation, Troy MI. This program can be used to perform a wide range of analyses, including static stress, dynamic, buckling and heat transfer. In this study, we utilized NISA's static stress and heat transfer modules to simulate the response of the package/board to various physical factors and thermal environments. The data needed to execute NISA is typed into an input data file. The format for this data file is outlined in the NISA manuals. The engineer must create these data files, define the appropriate parameters, and interpret the results in the form of both numerical and graphical output.

2.1 PACKAGE/BOARD MODEL

The main model used in this study simulated an LCCC surface mounted on a ceramic board and aluminum thermal plane. The LCCC was 1.2 square inches with 84 solder connections. Due to the symmetry conditions along the "x" and "z" axes, only one-quarter of the package/board system was modeled. The package/board model is shown in Figure 1. In order to simulate the entire package/board system, heat flow and thermal expansion were prohibited along the inner (cut) surfaces in the direction perpendicular to the plane of symmetry. The outer surfaces assume no convection, conduction, or radiation to the surrounding air.

Due to the relative size of certain components, such as the wire connections between the die and the package and the negligible effect these components had on the analyses, these package components were not modeled. The materials that were modeled are also identified in Figure 1 and are as follows: the die, die attach, air surrounding the die, package, thermal pad beneath the center of the package, air gaps in between the package and the board, solder connections between the package and the board, board, bonding material between the board and the thermal plane, and thermal plane. The following is a list of the thermal conductivities used in this analysis:

PACKAGE/BOARD MODEL



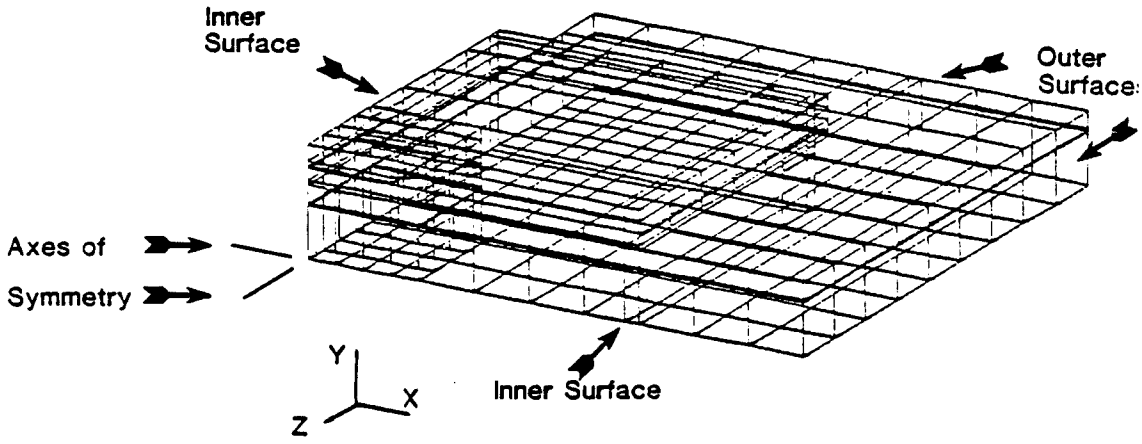


FIGURE 1

	Conductivity (W/in^{o}C)
Die	2.66
Die Attach	8.00
Air	0.00081
Package	0.77
Thermal Pad	1.28
Solder	1.28
Board	0.77
Bonding Material	0.013
Thermal Plane	4.09

2.2 SOLDER CONNECTION MODEL

In the package/board model, the solder connections (also referred to as solder bumps) were modeled as a strip of solder material. This strip was an accurate representation of the solder for the heat transfer analyses, but did not sufficiently indicate the thermal stress throughout the individual solder bumps. Therefore, a finite element model of an individual solder bump was created. This model is shown in Figure 2. The entire model consists of solder elements. The solder properties applied in this study were that of a tin-lead solder. Comparing this finite element solder bump model to the LCC in Figure 3, the solder connection model closely resembles a solder connection located on a typical LCC.

3.0 THERMAL RESISTANCE

The thermal resistance of an electronic package is the relative temperature rise in relation to the heat produced by the circuit. In order to determine the thermal resistance of the circuit, the circuit is powered up until it reaches steady state, that is, the thermal state where the temperature remains constant. The thermal resistance of the package, θ_{JC}, is then determined by taking the difference between the highest temperature on the die and the highest temperature at the bottom of the package and dividing this value by the power supplied to the die. The overall resistance of the package/board is determined by taking the difference between

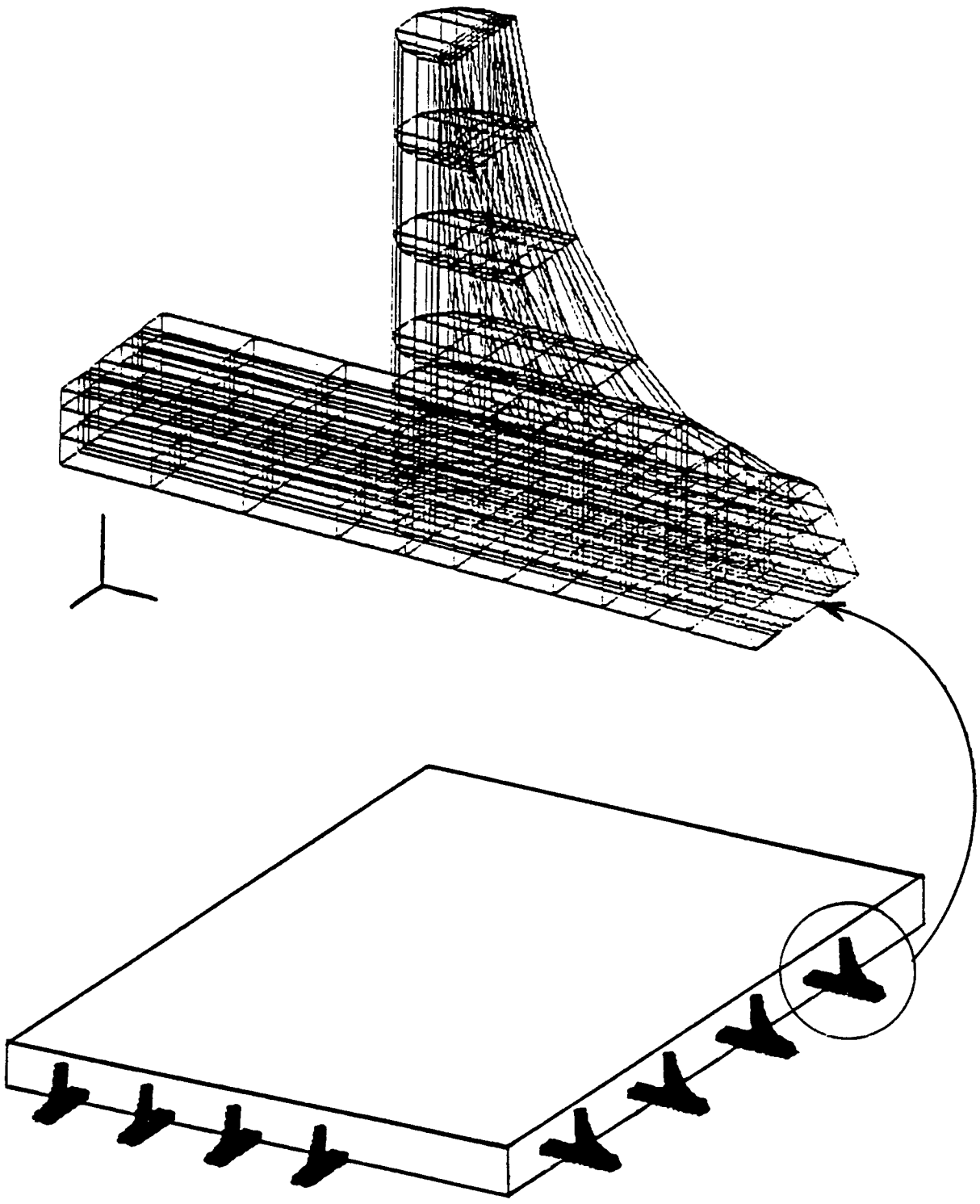


FIGURE 2

SOLDER CONNECTION MODEL

LEADLESS CHIP CARRIER

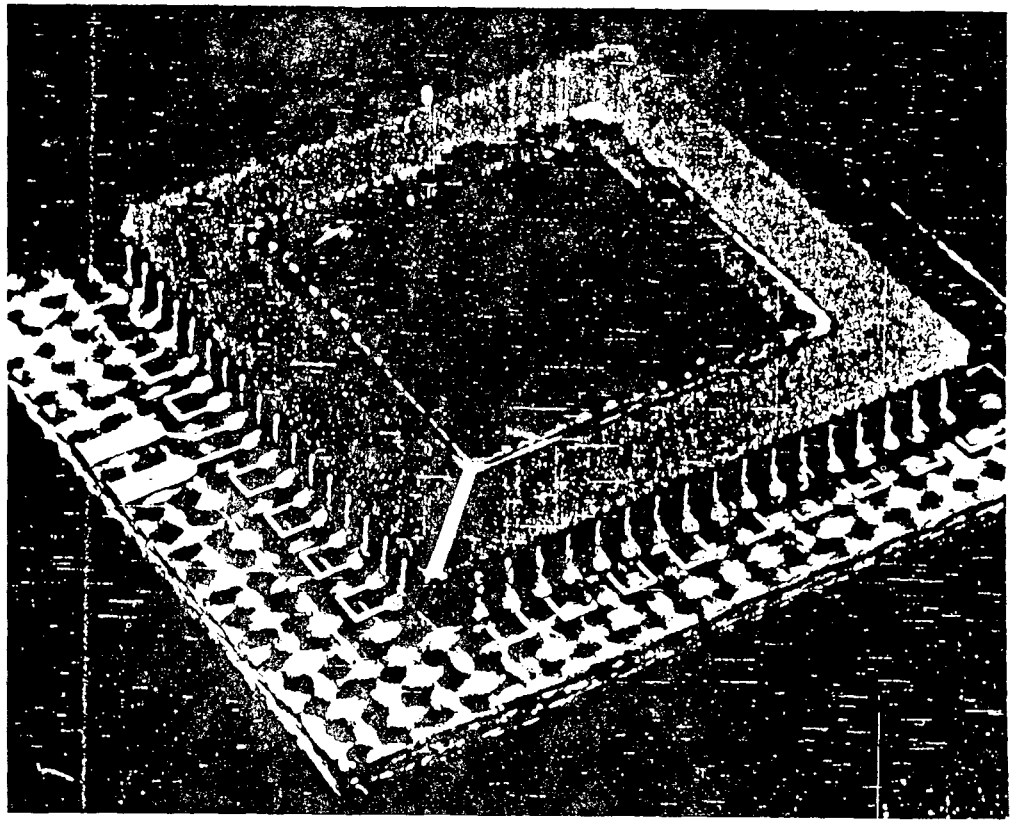


FIGURE 3

the highest temperature on the die and the heat sink temperature (ambient) and dividing this value by the power supplied to the die.

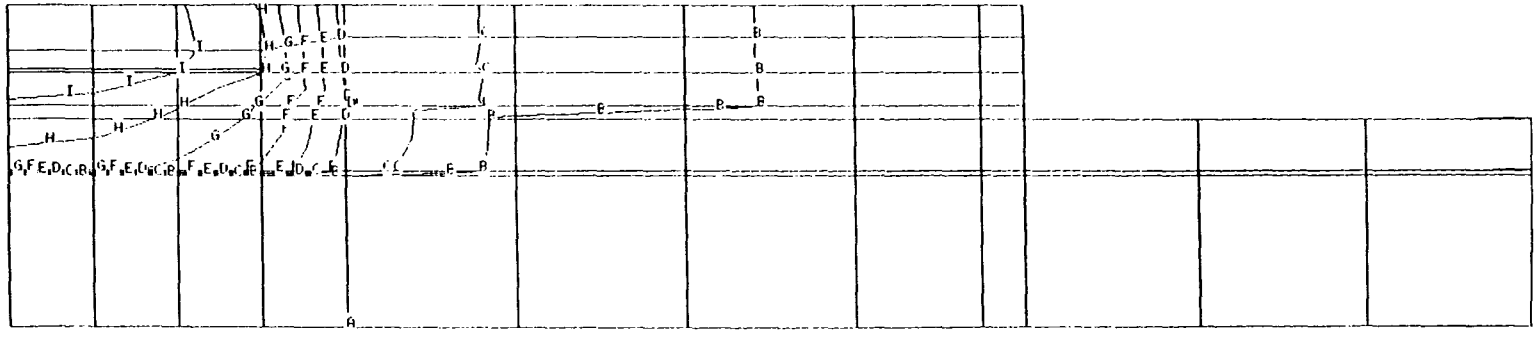
A steady state analysis was performed on the package/board finite element model. The circuit (die) had a total of 2 Watts (W) evenly distributed across its surface. The system had an initial temperature of $90^{o}C$ and the bottom of the thermal plane was held at a constant temperature of $90^{o}C$. Under ideal conditions, the maximum temperature rise in the die was $3.72^{o}C$. This simulation resulted in a θ_{JC} of $.245^{o}C/W$. The thermal contour diagram for this simulation is displayed in Figure 4. When the constant temperature heat sink was moved from the bottom of the thermal plane to the side of the thermal plane, the maximum temperature rise became $5.02^{o}C$ and the package resistance, θ_{JC}, became $.235^{o}C/W$. The thermal resistance was then tabulated for several different conditions. These conditions consisted of varying the die size, varying the heat producing areas on the die, creating voids in the die attach and varying the size of the thermal pad located beneath the package. In the majority of the simulations, the hottest point on the die was located at the center of the die. The hottest point on the die changed when the environmental conditions caused a change in the heat flow.

3.1 VARYING DIE SIZE

The size of integrated circuits (dies) varies from application to application. For a given package size, the effect on thermal resistance for various die sizes was determined. The die and the die attach located directly beneath it were modeled with dimensions of .3" x .3" and were represented by nine elements. These elements are displayed in Figure 5. Another simulation was made where the die and die attach were reduced from nine elements to four elements. This meant changing the material index of elements 22, 25, 48, 50, and 62 in the die (conductivity = $2.66W/in.^{o}C$) and elements 21, 24, 47, 49, and 61 in the die attach (conductivity = $8.00W/in.^{o}C$) from that of their respective materials to that of air (conductivity = $.00081W/in.^{o}C$). In order to keep the overall power input into the die at

THERMAL CONTOURS OF STEADY STATE ANALYSIS

Legend	
A	90.00
B	90.41
C	90.82
D	91.24
E	91.65
F	92.06
G	92.48
H	92.89
I	93.30
J	93.72



SURFACE MOUNTED LEADLESS CHIP CARRIER

FIGURE 4

ONE-QUARTER VIEWS OF DIE AND DIE ATTACH

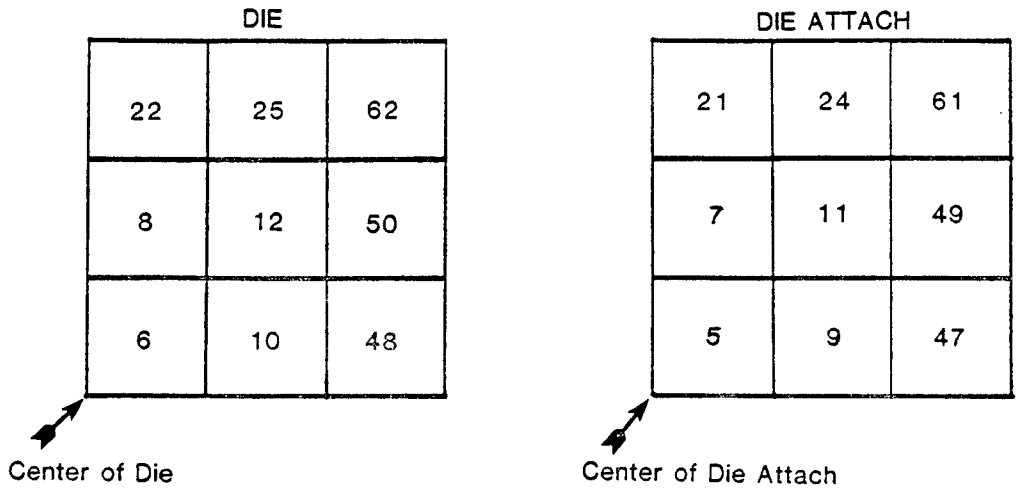


FIGURE 5

HEAT DISTRIBUTION IN DIE

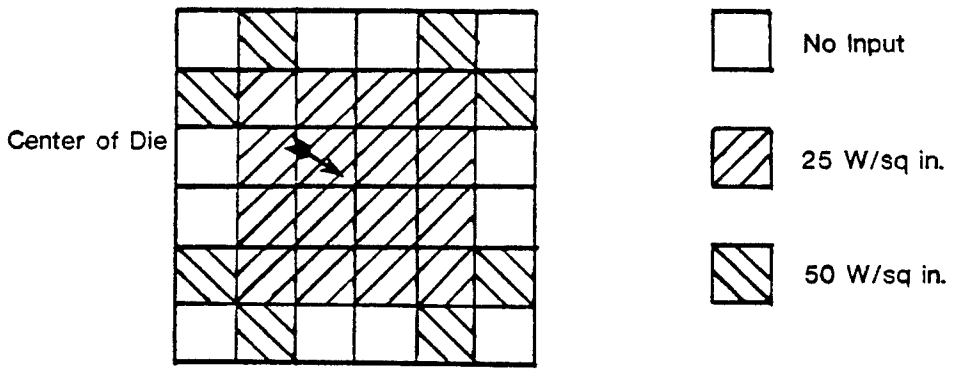


FIGURE 6

2W, the flux supplied to the die was altered from 22.2 (W/sq in.) to 50.0 (W/sq in.), thus taking into account the change in area. The results are as follows:

No. of Element	Area (Sq in.)	Overall Resistance	Highest Die Temperature
9	.09	$1.86^{o}C/W$	$93.72^{o}C$
4	.04	$2.91^{o}C/W$	$95.82^{o}C$

These results show a 56 percent increase in thermal resistance for a 56 percent reduction in die area.

3.2 VARYING DIE HEAT PRODUCING AREAS

In a typical integrated circuit, the heat is not produced uniformally throughout the surface of the die. The finite element model made it possible to vary the locations of heat production within the die in order to assess the effect on thermal resistance. Therefore, the material properties of the die and die attach were returned to their original values but the heat producing area of the die remained in the four centermost elements. The results of this simulation showed the overall resistance to be $2.53^{o}C/W$ and the highest die temperature to be $95.05^{o}C$. The heat producing areas on the die were altered again to the pattern shown in Figure 6. As shown in the figure, some of the elements had 25W/sq in. applied, some had 50W/sq in. applied, and some had no power flux input. The results of this simulation run showed the overall resistance to be $1.91^{o}C/W$ and the highest die temperature to be $93.82^{o}C$.

3.3 VOIDS IN THE DIE ATTACH

Voids at various locations within a packaged integrated circuit often occur during fabrication. Therefore, it is important to determine the extent to which voiding is permissible. Six additional analyses which simulated voids in the die attach were made. The voids varied in size and number. The results of these simulations are as follows:

No. of Voids	Area Per Void	Total Void Area	Highest Die Temp.	Thermal Resis. of Package	Overall Resistance
0	---	---	93.72°C	.245°C/W	1.86°C/W
4	.005"	.02"	93.76°C	.245°C/W	1.88°C/W
2	.010"	.02"	94.41°C	.530°C/W	2.21°C/W
2	.015"	.03"	94.43°C	.530°C/W	2.22°C/W
4	.010"	.04"	96.47°C	1.370°C/W	3.24°C/W
2	.020"	.04"	96.38°C	1.360°C/W	3.19°C/W
1	.040"	.04"	96.22°C	1.665°C/W	3.11°C/W

This table shows that minor voiding (i.e., 25 percent) in the die attach has very little effect on the thermal resistance of the package and on the overall thermal resistance, however, major voiding (i.e., 50 percent) in the die attach has a significant effect in these areas. Smaller voids that were distributed over a large area resulted in a lower resistance than the summation of the smaller voids concentrated in one area.

3.4 VARYING THERMAL PAD SIZE

The presence of a thermal pad or coating and its size is a design variable that requires assessment. The necessity of a thermal coating and its size can be determined through finite element simulations. Finally, the effect that the thermal pad size has on the overall resistance of the package was evaluated through a series of simulations. The thermal pad was represented by 16 elements in the one quarter view and had the dimensions of .4" X .4". This model is displayed in Figure 7. As the thermal pad decreased in size, it remained centered at the center of the package. The thermal pad size was reduced by changing the material index of certain thermal pad elements from that of solder (conductivity = 1.28°C/W) to that of air (conductivity = .0081°C/W). The results of these simulations are as follows:

ONE-QUARTER VIEW OF THE THERMAL PAD

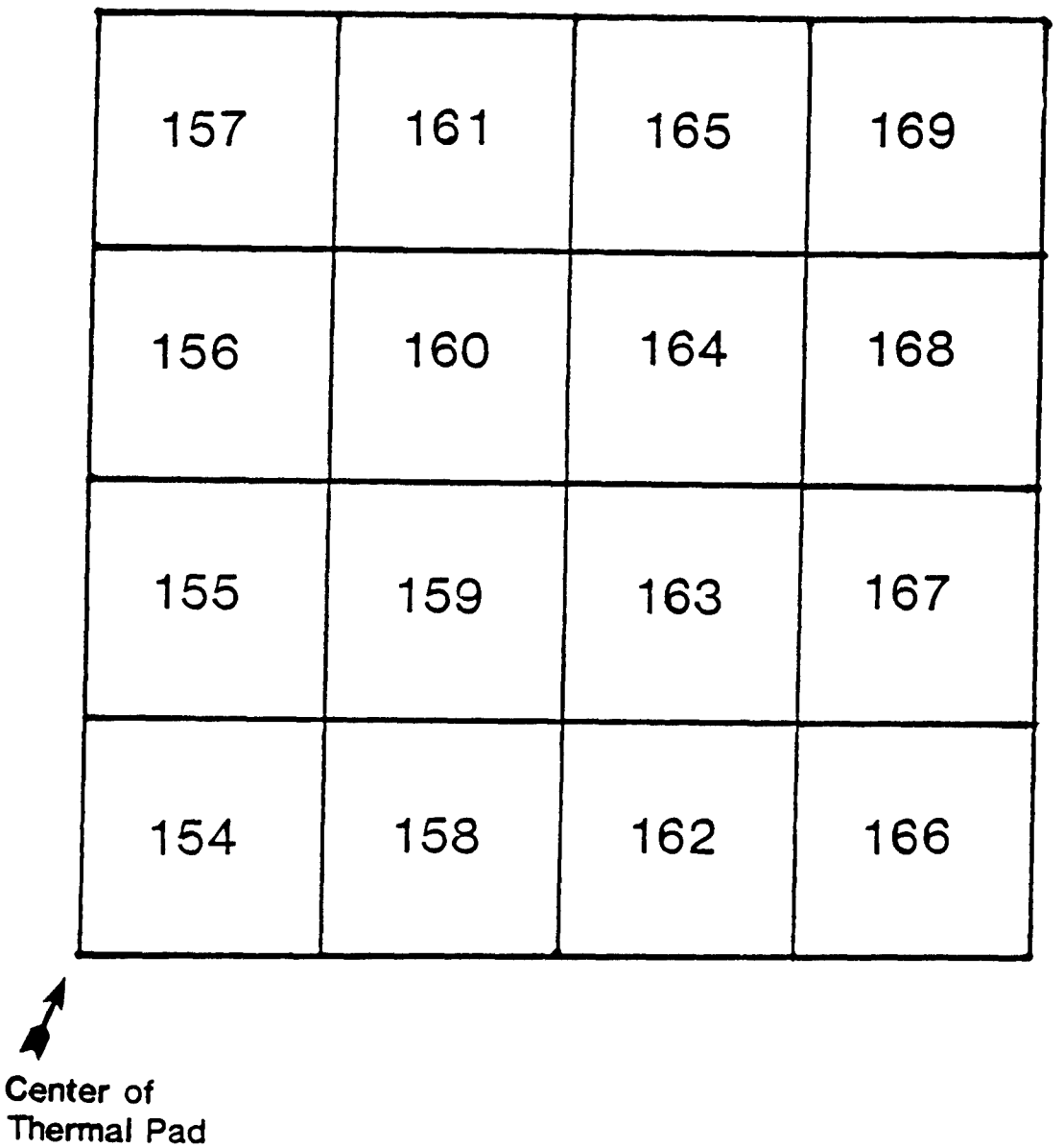


FIGURE 7

No. of Thermal Pad Elements	Highest Die Temperature	Package Resistance	Overall Resistance
16	93.72°C	.245°C/W	1.86°C/W
9	93.94°C	.250°C/W	1.97°C/W
4	94.86°C	.262°C/W	2.43°C/W
1	97.35°C	.613°C/W	3.68°C/W
0	107.62°C	.087°C/W	8.61°C/W

The thermal resistance increased in value as long as a thermal pad was there. This was expected. As soon as the pad was totally replaced by a layer of air, the air acted as an insulator and a large temperature build-up occurred in the package. This explains the sudden drop in package resistance between one and zero thermal pad element size. A graph of the thermal pad area and the overall thermal resistance is displayed in Figure 8.

4.0 TRANSIENT THERMAL ANALYSIS

The steady state analysis simulates the system's thermal state which is constant with time. A transient analysis simulates changes in the system's thermal state in relation to time. A transient analysis was simulated in order to determine at what time interval the maximum temperature difference and the maximum thermal gradients occurred. In order to simulate a transient thermal analysis, a time step must be calculated and supplied to the NISA data file. This time step defines the time interval between calculations. After every time interval, NISA will determine a new temperature distribution throughout the package. The time step is calculated by appropriate parametric evaluations using the device's physical and material characteristics. The time step value that was used in this study was .01535 seconds. After 100 iterations, the die had reached 99 percent of its steady state temperature rise.

One hundred time steps were used in this analysis. The temperature values at the center of the die (Node 10) and at the center of the bottom of the package (Node 1) were taken for each time step and plotted on a graph to determine which time step has the maximum temperature difference and

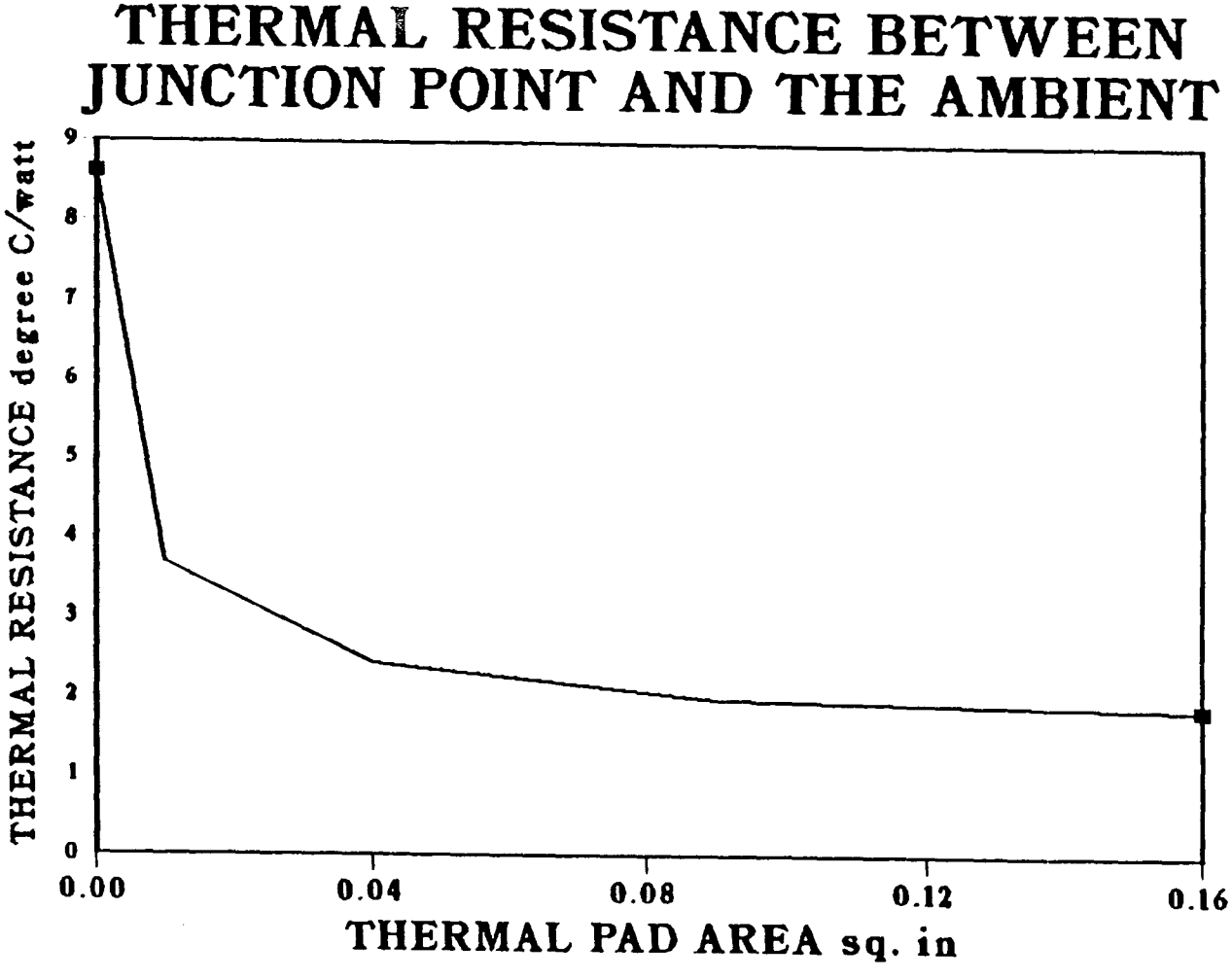

THERMAL RESISTANCE BETWEEN JUNCTION POINT AND THE AMBIENT
THERMAL RESISTANCE degree C/watt
9
8
7
6
5
4
3
2
1
0
0.00
0.04
0.08
0.12
0.16
THERMAL PAD AREA sq. in

FIGURE 8

therefore, the maximum θ_{JC}. These values were graphed twice. The first graph shows the relationship between temperature and time (Figure 9) and the second graph shows the relationship between the temperature and the log of the time (Figure 10). The results of these simulations showed that the largest thermal gradients, and therefore the maximum thermal stresses, would occur at steady state.

5.0 PACKAGE/BOARD THERMAL STRESS ANALYSIS

A series of thermal stress analyses were performed on the package/board model. These analyses are based on a state of zero stress when the device is at $90^{o}C$. All stress results do not consider the residual stresses that exist prior to circuit powerup. These residual stresses are caused by the manufacturing process, prior thermal cycling, creep, oxidation, etc. During operation, the temperature of the package/board rises and causes the materials to expand in a non-uniform manner. This non-uniform expansion causes thermal stresses. To perform these thermal stress analyses, the output temperature solutions from the steady state simulations are used as inputs to the stress analysis. The change in thermal state along with appropriate material properties determine the thermal stresses. All positive stress values indicate material that is in tension and all negative stress values indicate material that is in compression.

5.1 EFFECTS OF VOIDS ON THE PACKAGE/BOARD STRESSES

In order to assess how voids in the die attach and in the thermal pad would affect the thermal stress of the package, three thermal stress analyses were made. One analysis considered the original package/board model, the second considered minor voiding in the die attach and the thermal pad, and the third considered major voiding in the die attach and the thermal pad. A diagram of the void location and size is shown in Figure 11. The majority of the highest stress values occurred in the ceramic material between the die attach and the thermal pad. The following table shows exactly what the relative maximum stresses were in all three simulations. The bar graph in Figure 12 displays the relative magnitude of these maximum

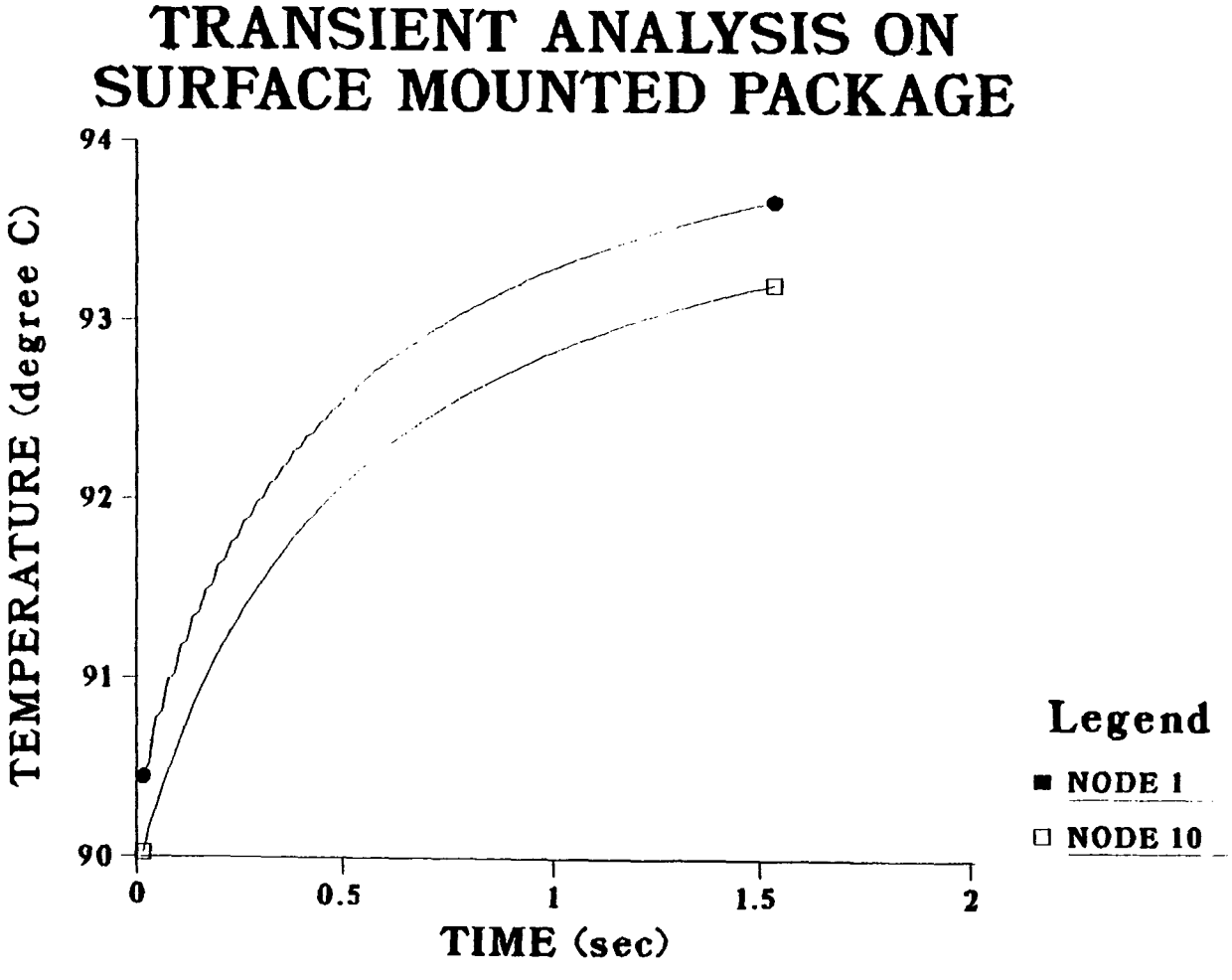

TRANSIENT ANALYSIS ON
SURFACE MOUNTED PACKAGE
TEMPERATURE (degree C)
94
93
92
91
90
0
0.5
1
1.5
2
TIME (sec)
Legend
NODE 1
NODE 10

FIGURE 9

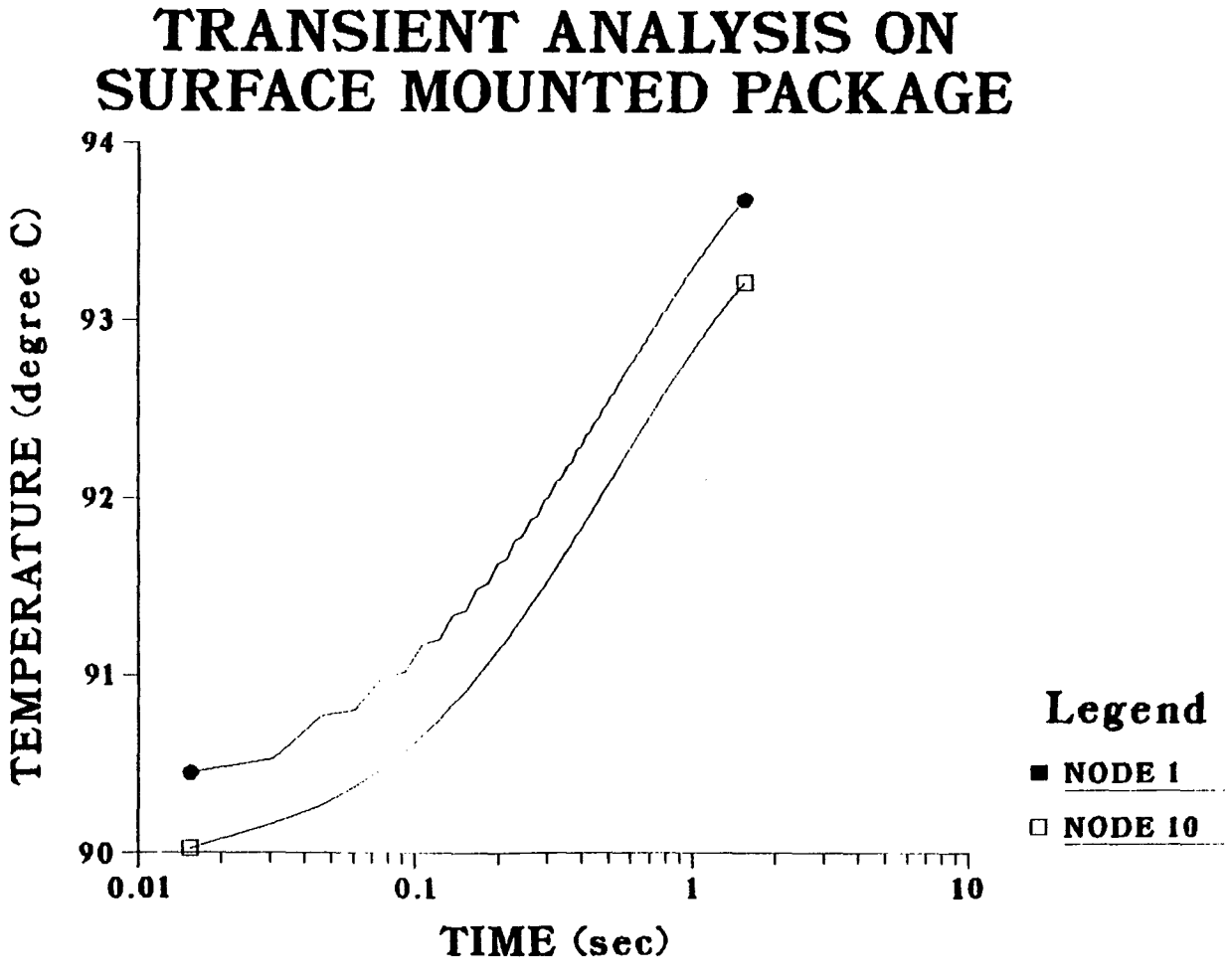
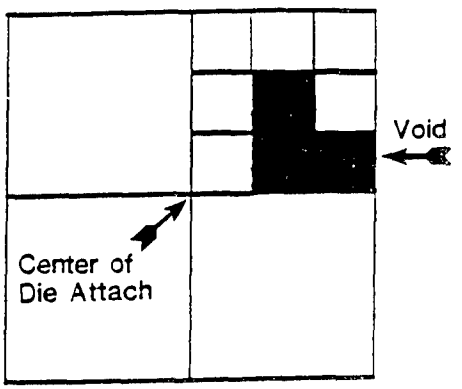
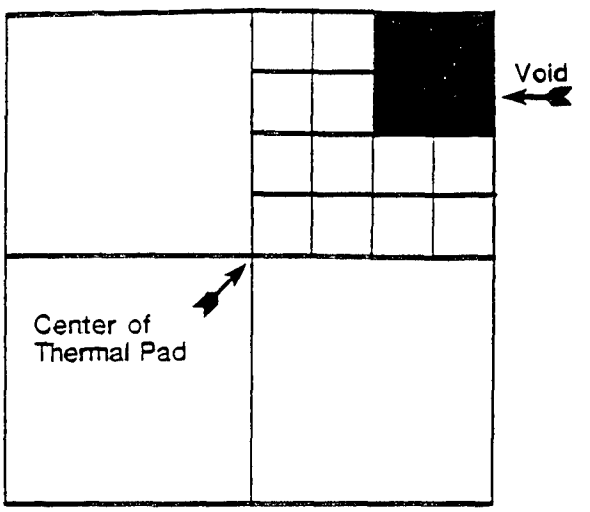

TRANSIENT ANALYSIS ON
SURFACE MOUNTED PACKAGE
TEMPERATURE (degree C)
94
93
92
91
90
0.01
0.1
1
10
TIME (sec)
Legend
NODE 1
NODE 10

FIGURE 10

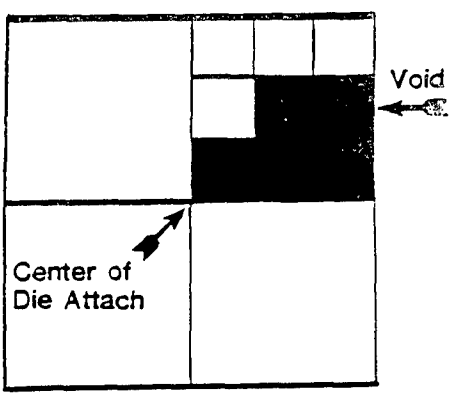
VOIDING IN THE DIE ATTACH AND THERMAL PAD

MINOR VOIDING





MAJOR VOIDING



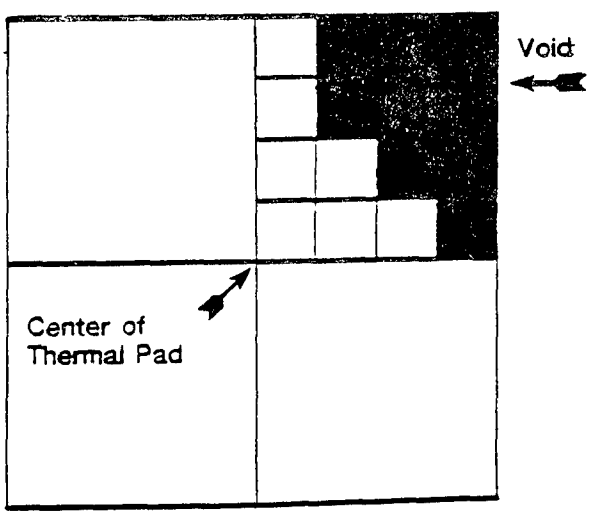


FIGURE 11

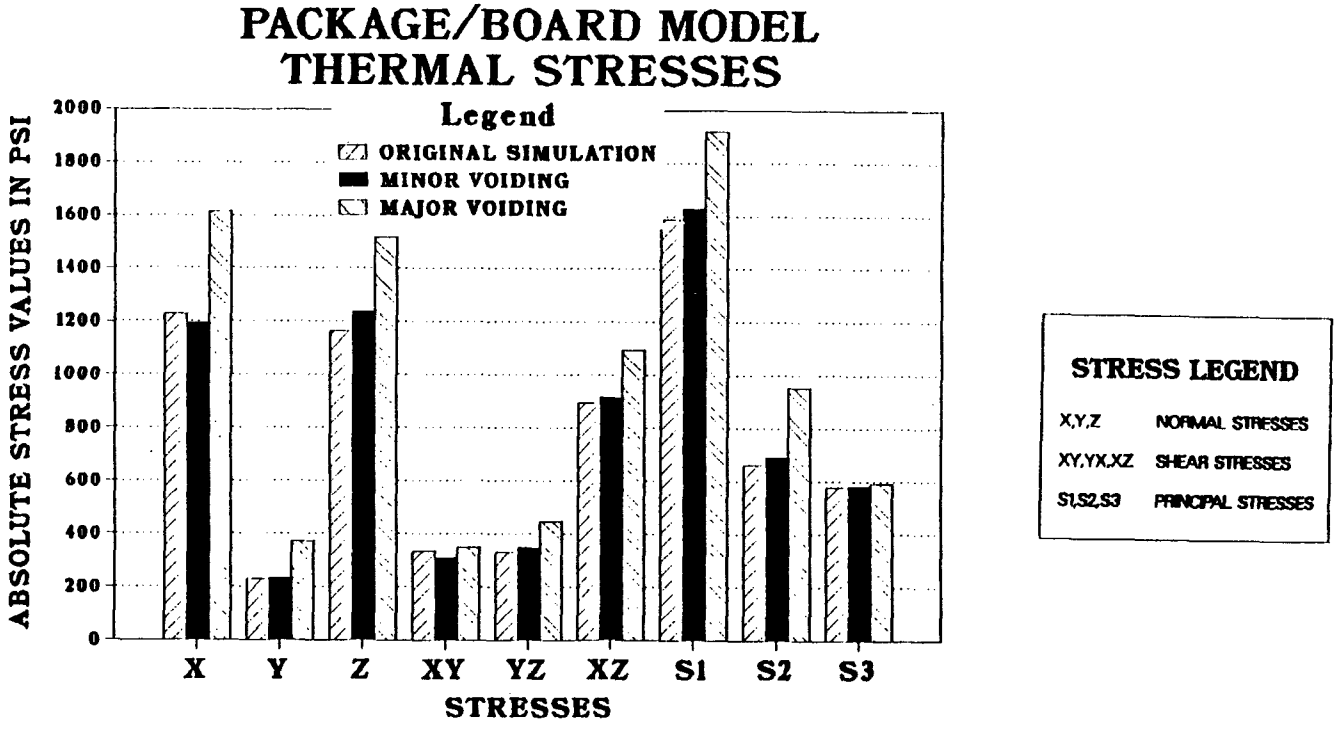

PACKAGE/BOARD MODEL
THERMAL STRESSES
Legend
ORIGINAL SIMULATION
MINOR VOIDING
MAJOR VOIDING
ABSOLUTE STRESS VALUES IN PSI
2000
1800
1600
1400
1200
1000
800
600
400
200
0
X
Y
Z
XY
YZ
XZ
S1
S2
S3
STRESSES
STRESS LEGEND
X,Y,Z NORMAL STRESSES
XY,YX,XZ SHEAR STRESSES
S1,S2,S3 PRINCIPAL STRESSES

FIGURE 12

stresses. All listed values in the table below apply to the ceramic package with exceptions as noted. All stress values are in pounds per square inch (psi).

	Original Simulation	Minor Voiding	Major Voiding
Normal stresses			
x direction	-1229	-1194	-1613
y direction	- 229	- 235	- 372 (die attach)
z direction	-1165	-1239	-1519
Shear stresses			
xy direction	337	308	348
yz direction	331	348	449
xz direction	897	918	1095
Principal stresses			
S1	-1588	-1628	-1921
S2	- 662 (bond)	- 692 (bond)	- 954 (die attach)
S3	581 (board)	584 (board)	593 (board)
Tresca Max Shear	902	919	1097
Von Mises Equiv	1631	1664	1989
Octahedral Shear	769	784	938

The ceramic material has a compressive strength of 340,000 - 400,000 psi and a tensile strength of 25,000 psi. The values here are well below these failure points.

6.0 SOLDER CONNECTION THERMAL STRESS ANALYSES

A finite element model that closely resembles a typical solder connection was generated. This solder connection model is necessary to show a general stress distribution and to locate specific areas of high stress. As shown in Figure 13, this model contacts the package along two of its surfaces and the board along its upper surface. The output deflections from the package/board stress analysis along these three surfaces were used as input deflections for the solder connection model. The remaining surfaces were unconstrained. One set of input deflections came from the

SOLDER CONNECTION CONTACTING SURFACES

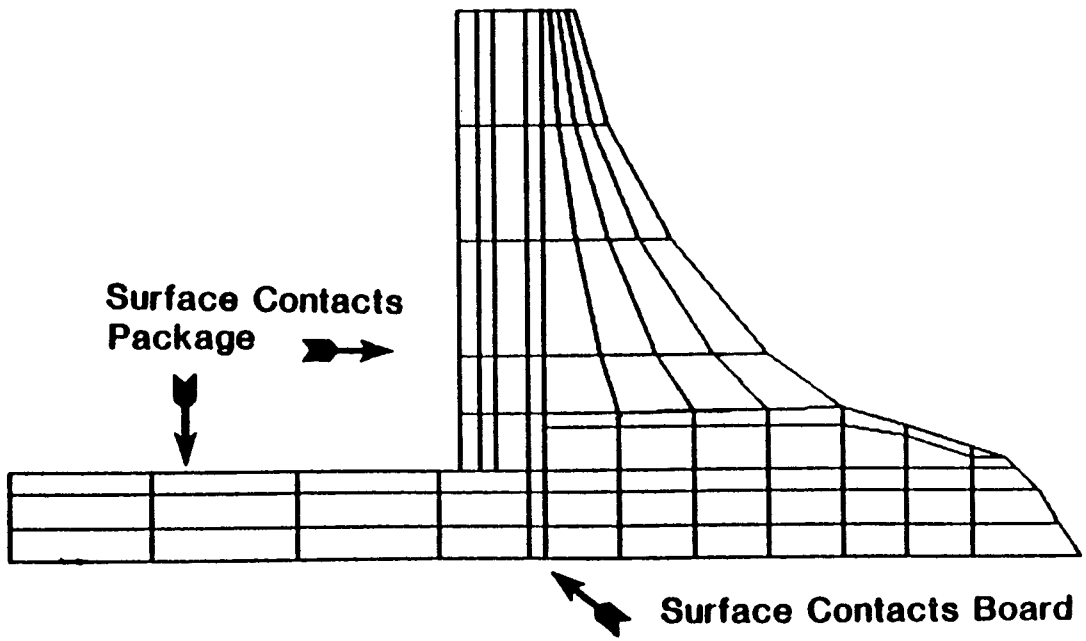


FIGURE 13

mid-side of the package and a second set of input deflections came from the corner of the package. These two simulations were compared and the results are listed below and shown in bar graph form in Figure 14.

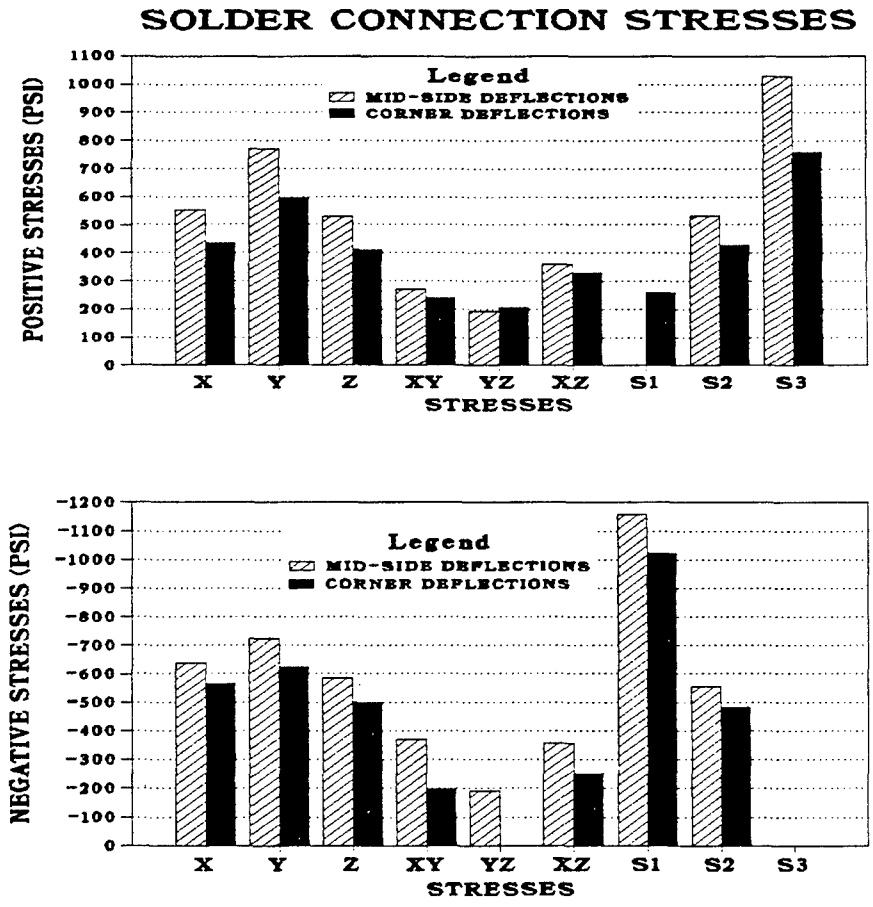
	Mid-side Deflection Analysis		Corner Deflection Analysis	
Normal stresses				
x direction	- 637	551	- 566	433
y direction	- 724	769	- 626	597
z direction	- 596	528	- 500	412
Shear stresses				
xy direction		370		239
yz direction		191		206
xz direction		359		329
Principal stresses				
S1	-1160	**	-1024	259
S2	- 557	533	- 483	429
S3	*	1029	*	760
Tresca Max Shear	*	465	*	420
Von Mises Equiv	*	817	*	737
Octahedral Shear	*	385	*	347

Note: The above values were taken from a list of 50 highest (absolute) output values.

**There were no positive values listed in the top 50.

*There were no negative values listed in the top 50.

These results show that deflections from the mid-side of the package produce the highest stresses in the solder connection. Therefore, output deflections from the mid-side of the package/board model will be used as inputs for the additional solder connection analyses.



STRESS LEGEND	
X,Y,Z	NORMAL STRESSES
XY,YX,XZ	SHEAR STRESSES
S1,S2,S3	PRINCIPAL STRESSES

FIGURE 14

6.1 EFFECTS OF VOIDS ON THE SOLDER CONNECTION STRESSES

The finite element simulation of a surface mounted device without any voids showed the existence of large shear and normal stresses in the solder connection between the package and the board. These stresses are due to the fact that the aluminum heat sink within the board causes a large relative deflection between the ceramic package and the ceramic board. However, voiding in the die attach and thermal pad results in a higher temperature within the package; thus, reducing this relative deflection. The following table lists the maximum stresses within the solder connection model. Graphs of these values are shown on Figures 15 & 16. All stress values are in psi.

	Original Simulation		Minor Voiding		Major Voiding	
Normal stresses						
x direction	- 637	551	- 602	551	- 435	554
y direction	- 724	769	- 685	770	- 494	781
z direction	- 586	528	- 561	528	- 397	534
Shear stresses						
xy direction		370		357		316
yz direction		191		166		183
xz direction		359		323		242
Principal stresses						
S1	-1160	---	-1024	297	- 787	354
S2	- 557	533	- 526	533	- 379	540
S3		1029		1018		995
Tresca Max Shear		465		423		333
Von Mises Equiv		817		745		589
Octahedral Shear		385		351		278

NOTE: Only the maximum absolute shear stresses are listed above.

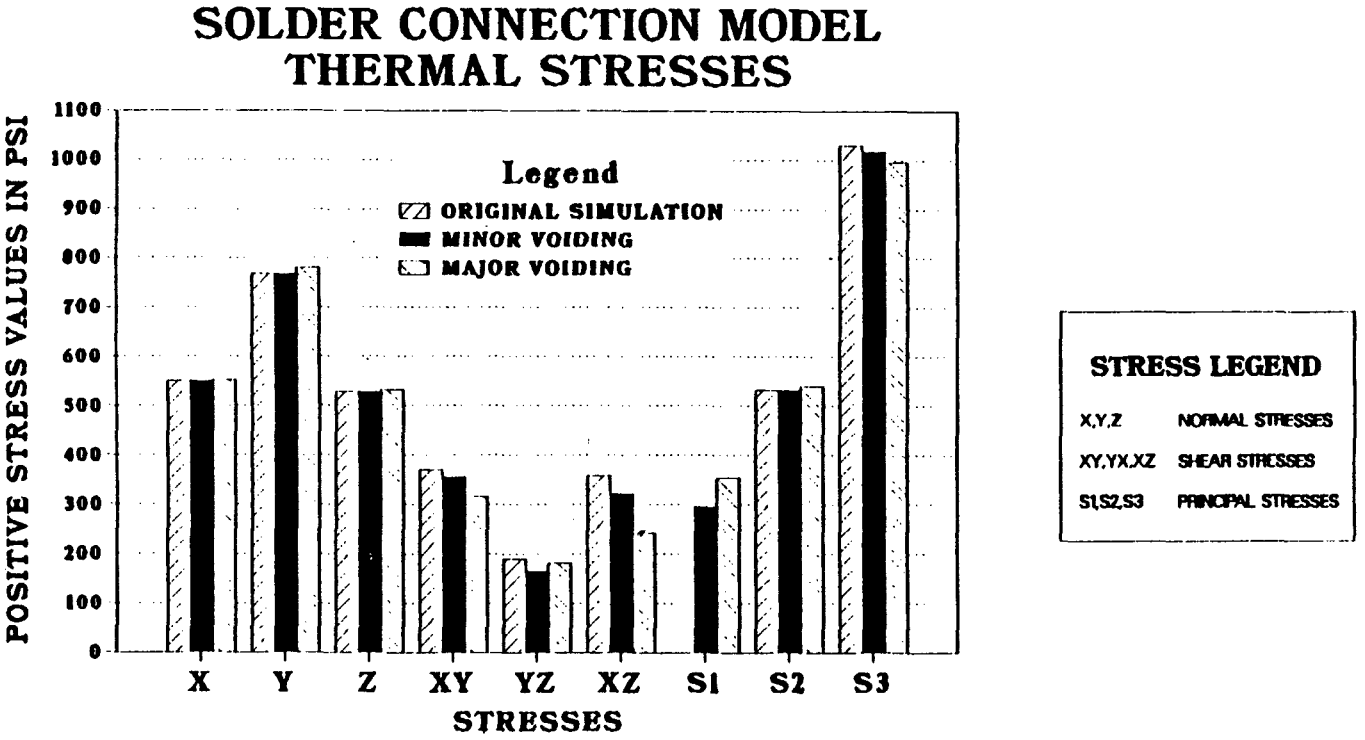

SOLDER CONNECTION MODEL
THERMAL STRESSES
POSITIVE STRESS VALUES IN PSI
1100
1000
900
800
700
600
500
400
300
200
100
0
Legend
ORIGINAL SIMULATION
MINOR VOIDING
MAJOR VOIDING
X
Y
Z
XY
YZ
XZ
S1
S2
S3
STRESSES
STRESS LEGEND
X,Y,Z NORMAL STRESSES
XY,YX,XZ SHEAR STRESSES
S1,S2,S3 PRINCIPAL STRESSES

FIGURE 15

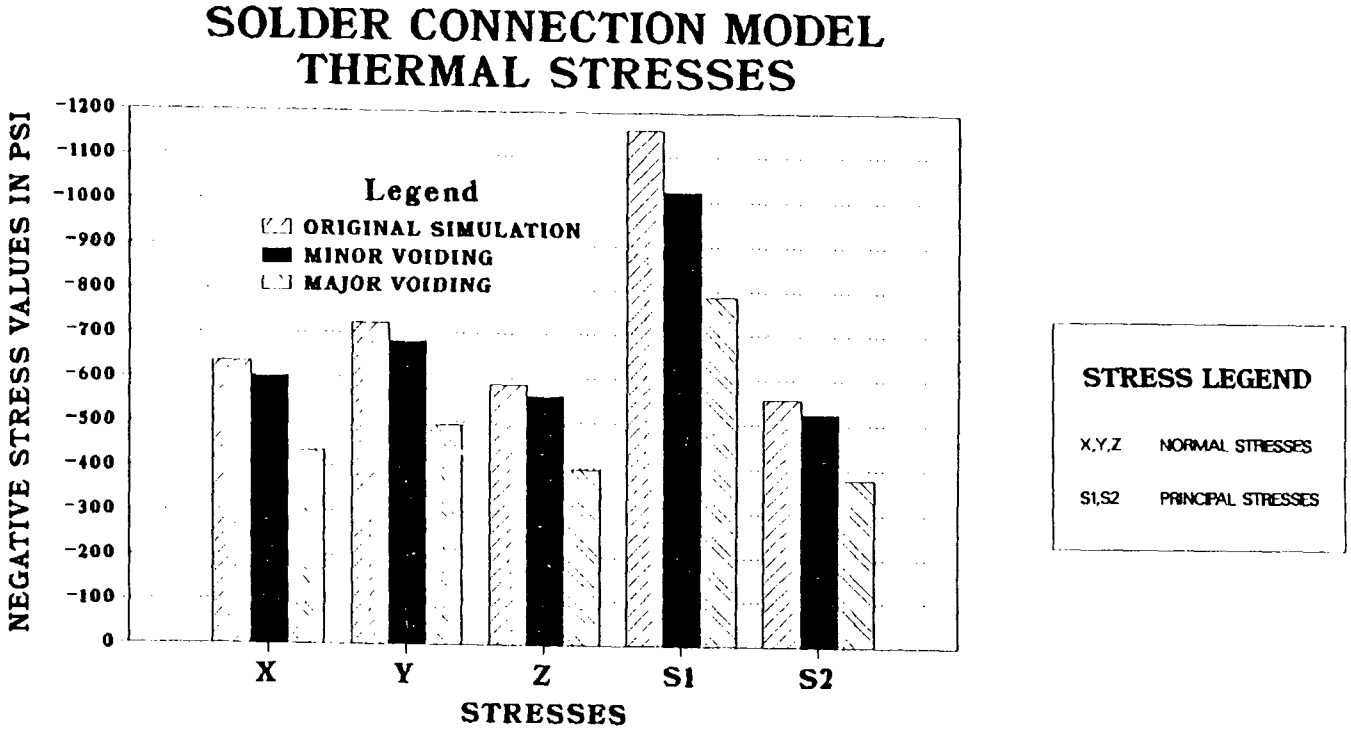

SOLDER CONNECTION MODEL
THERMAL STRESSES
NEGATIVE STRESS VALUES IN PSI
-1200
-1100
-1000
-900
-800
-700
-600
-500
-400
-300
-200
-100
0
Legend
ORIGINAL SIMULATION
MINOR VOIDING
MAJOR VOIDING
X
Y
Z
S1
S2
STRESSES
STRESS LEGEND
X,Y,Z NORMAL STRESSES
S1,S2 PRINCIPAL STRESSES

FIGURE 16

6.2 EFFECT OF HEAT SINK LOCATION ON THE SOLDER CONNECTION THERMAL STRESS VALUES

An important design parameter is the location of the heat sink in relation to tne heat generation area. A finite element simulation of the physical device makes it possible to assess the thermal results when the heat sink is located somewhat remotely from the chip instead of directly beneath it. Two physical configurations were modeled. One configuration considered the 90^{o}C heat sink along the bottom of the thermal plane. This allows a nearly vertical heat conduction path. A second configuration considered the 90^{o}C heat sink along the edge of the thermal plane. This configuration causes the heat to conduct from the center of the package/board to the edge of the board; thus, causing a larger horizontal thermal expansion in the board/thermal plane. The results of the solder connection simulations are shown in Figure 17.

6.3 THE STRESS DISTRIBUTION WITHIN AN INDIVIDUAL SOLDER CONNECTION

There were two localized areas of stress concentrations within a solder connection. The first area is shown in Figure 18 and is where the maximum positive normal stresses are occurring. These tensile stresses indicate that a separation between the package and the solder pad could occur. If the package separated from the solder pad, tensile stresses would propagate until they reached the critical area where most solder failures are known to occur (shown in Figure 18b). In order to confirm this hypothesis, another solder connection simulation was made. A finite element simulation of the package separating from the board was accomplished by modeling a free surface between the two appropriate surfaces. This thermal stress analysis did indeed show the maximum positive stresses to have propagated to the area identified in Figure 18b. Maximum tensile stress values for element 51 (Figure 18a) are listed below. All stress values are in psi:

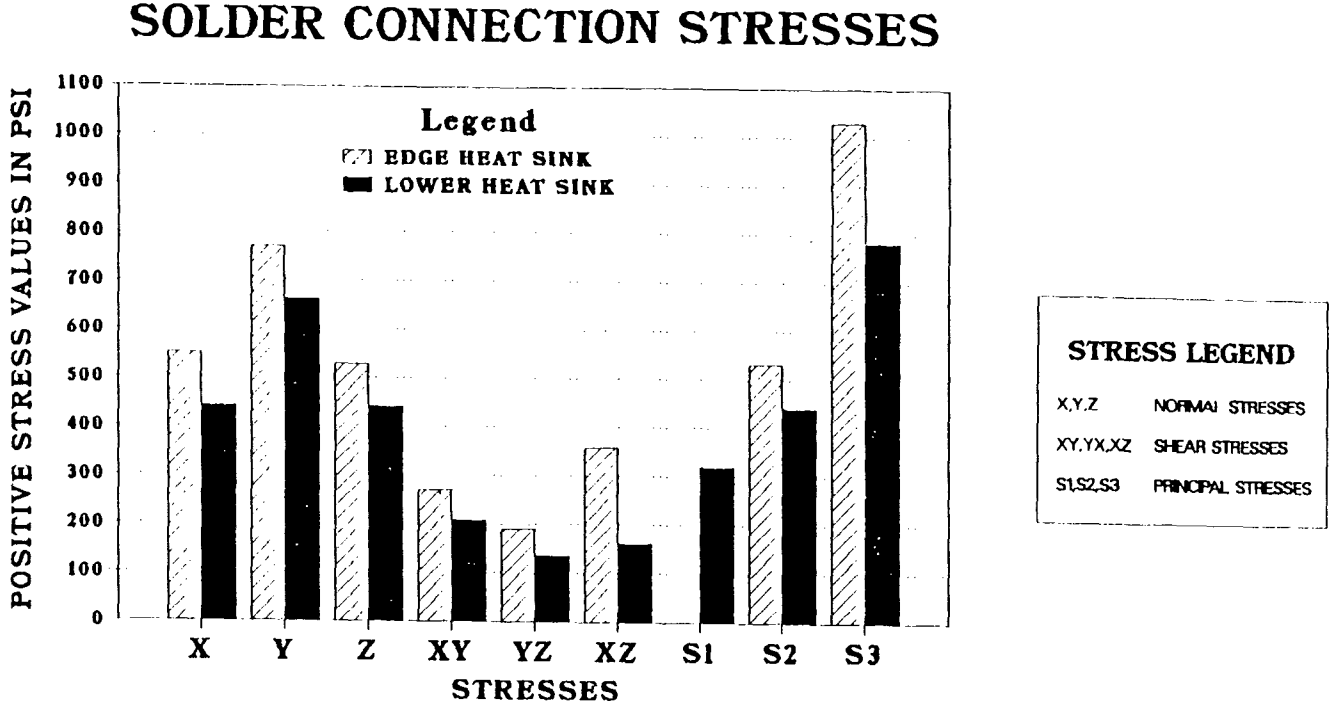

SOLDER CONNECTION STRESSES
POSITIVE STRESS VALUES IN PSI
1100
1000
900
800
700
600
500
400
300
200
100
0
Legend
EDGE HEAT SINK
LOWER HEAT SINK
X
Y
Z
XY
YZ
XZ
S1
S2
S3
STRESSES
STRESS LEGEND
X,Y,Z NORMAL STRESSES
XY,YX,XZ SHEAR STRESSES
S1,S2,S3 PRINCIPAL STRESSES

FIGURE 17

MAXIMUM SOLDER CONNECTION STRESSES

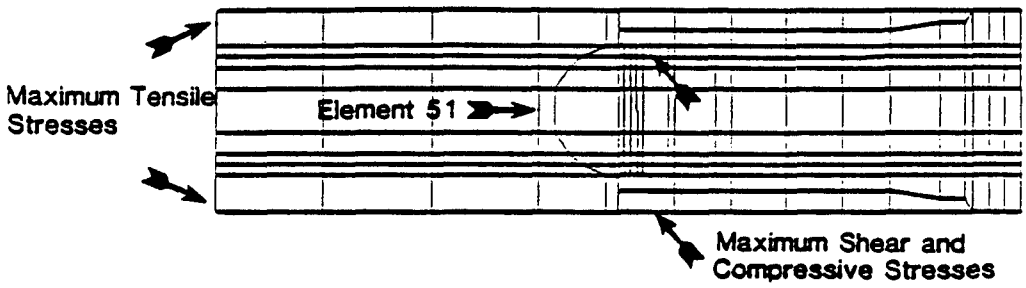


FIGURE 18a

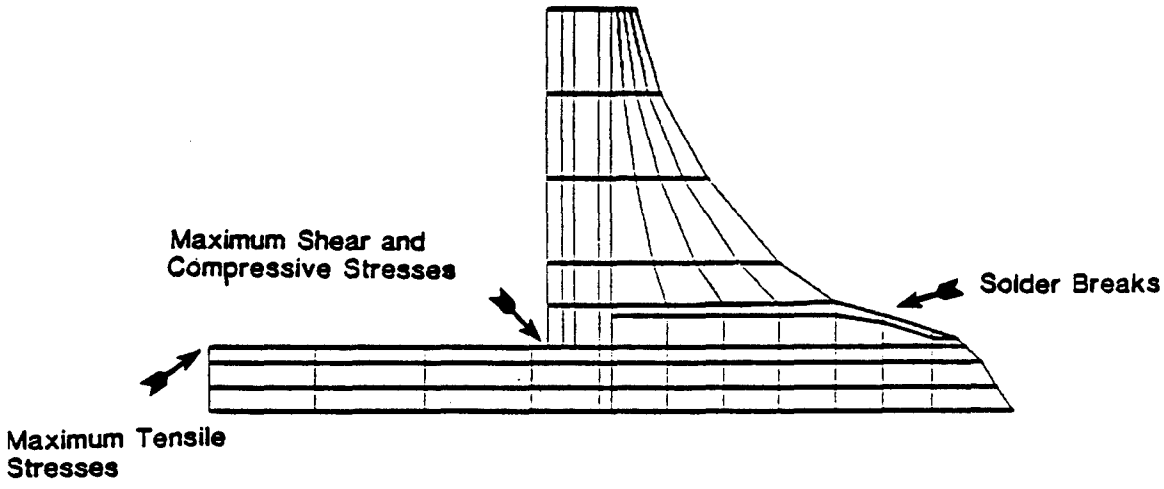


FIGURE 18b

	Original Simulation	Package Lifting Simulation
Tensile Stresses		
x direction	288	466
y direction	338	555
z direction	250	409

The second area of concern is where the maximum negative normal stress (-724psi) and the maximum positive shear stresses (370psi) occurred (Figures 18a&b). This area of high concentration of stresses, shear and compressive, is located where most solder connection failures occur. Once again, as voiding was simulated in the die attach and thermal pad, these shear and compressive stresses decreased. The stress distribution pattern remained consistent throughout all of the solder connection simulations.

7.0 SUMMARY

NISA finite element analyses of a powered integrated circuit in an LCCC package were made. These simulations allowed the thermal response of all the materials used in the chip/package/board to be predicted. These thermal responses included both temperature and thermal stresses. Transient and steady-state conditions were simulated. The finite element simulations made it possible to see how various physical factors affect maximum chip temperatures, chip to heat sink thermal resistance and maximum material stresses. The physical factors that were investigated were: voiding in the die attach and the thermal pad located beneath the package, varying the die size and heat producing areas and varying the thermal pad size. The results of the simulations show the following:

(1) Die size has a very significant effect on its temperature rise.

(2) Varying the die heat producing areas had a significant effect when the power was concentrated in the center of the die but had very little effect when minor variations were made across the die.

(3) Large voids in the die attach had a significant effect on the thermal resistance. The thermal resistance for the package was higher for voids concentrated in one area than for equivalent area voiding distributed over a large area.

(4) As the thermal coating underneath the package decreased in size, the thermal resistance increased at an accelerated rate.

(5) The maximum temperature difference, thermal resistance, thermal contours and thermal stresses occur at steady state conditions.

(6) The highest thermal stresses occurred in the ceramic package. However, the stresses were within the strength capability of the ceramic.

(7) Large shear and normal thermal stresses were found in the solder connection between the package and the board due to the expansion of the aluminum heat sink. The fatigue strength of the solder is on the order of 500 to 1,000 psi. These solder connections displayed tensile stresses of 724 psi and shear stress of 359 psi.

(8) The area of high shear and tensile stress in the solder connection model occurred in the same region as the majority of solder connection breaks during thermal cycling tests.

(9) These finite element simulations indicate that small temperature differences throughout a packaged device do not necessarily equate to a highly reliable surface mounted package.

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