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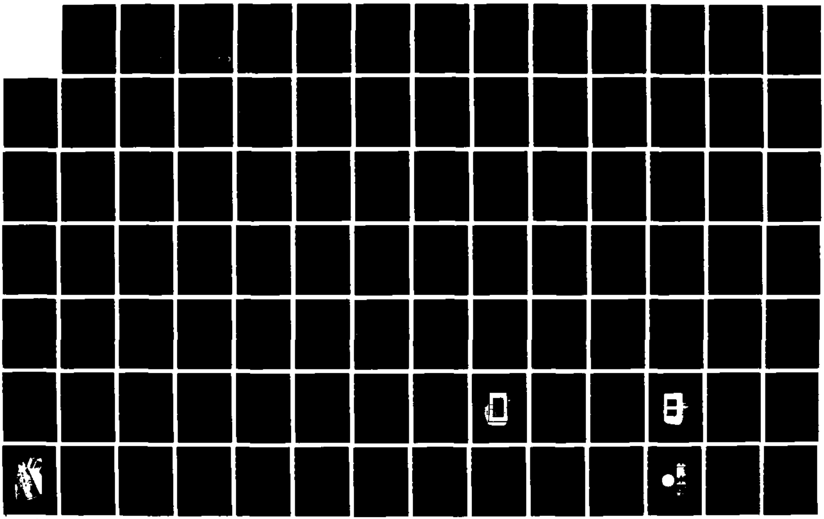

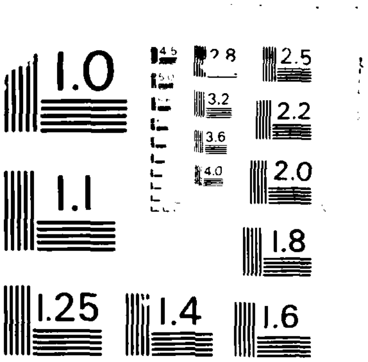

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EXAMINATION OF TEMPERATURE EFFECTS ON GATE-TO-DRAIN AVALANCHE BREAKDOWN IN GaAs MESFETs BY MEASURING LIGHT EMISSION UNDER RF DRIVE

THESIS

Roger E. Robb
Captain, USAF

AFIT/GE/ENG/87D-73

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THESIS

Presented to the Faculty of the School of Engineering
of the Air Force Institute of Technology
Air University
In Partial Fulfillment of the
Requirements for the Degree of
Master of Science in Electrical Engineering

Roger E. Robb, B.S.
Captain, USAF

December 1987

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Abstract

This investigation examines temperature effects on avalanche breakdown in GaAs MESFETs to determine if this failure mechanism is accelerated by high temperature life tests. The specific objective is to assess whether the accelerated life test evaluations performed on a GaAs MESFET planned for use in future Defense Satellite Communications System (DSCS) spacecraft have adequately addressed the reliability issues concerning the gate-to-drain avalanche breakdown failure mechanism. This objective was accomplished by adapting an existing analytical model for temperature effects, and using it to predict the variation in avalanche multiplication activity with temperature. To verify this model, it was used to calculate the associated changes in light emissions over temperature which were experimentally validated on one device of the type planned for use by the DSCS program. Once validated, these models were used to evaluate the adequacy of the accelerated temperature life tests. The results of this evaluation indicate that the avalanche breakdown failure mechanism is decelerated with temperature, and therefore, the effects of avalanche breakdown on the reliability of GaAs MESFETs cannot be determined by accelerated temperature life testing.

EXAMINATION OF TEMPERATURE EFFECTS ON GATE-TO-DRAIN AVALANCHE BREAKDOWN IN GaAs MESFETs BY MEASURING LIGHT EMISSION UNDER RF DRIVE

I. Introduction

Background

Power GaAs metal-semiconductor field-effect transistors (MESFETs) are being considered as replacements for Traveling Wave Tube Amplifiers (TWTAs) in various spacecraft applications. One of the advantages of the GaAs MESFET is that the reliability of a given device design should be predictable from accelerated life testing. A major concern in spacecraft applications of TWTAs is the reliability associated with long term operation in a vacuum (25). Since there are no known test techniques to accelerate the effects of a vacuum environment on TWTAs, real time life testing is required (25). Because the design life of a typical spacecraft presently ranges from five to ten years, these life tests become impractical from both a time and cost perspective.

Before GaAs MESFETs are used in satellites and other high reliability systems, their reliability must be demonstrated through testing. Several reliability studies utilizing accelerated temperature life testing have been conducted with various GaAs MESFETs, and these studies have concluded that they are very reliable devices (5:395; 6:151; 7:321; 8:SEC IV). But, these reliability conclusions were based on assumptions about the device's failure mechanisms and the respective activation energies (5:397; 6:151; 7:321; 8:SEC IV). The key assumption in all of these studies is that all failure mechanisms are accelerated in the same way with respect to temperature (5:595; 6:151; 7:327; 8:SEC IV). Therefore, the mean-time-to-failure (MTTF) determined at high temperatures can be projected to lower, normal operating temperatures. In fact, the overall reliability of a device is determined by a set of different failure mechanisms. Under any particular condition, any one of these, or a subset of these failure mechanisms could be dominant, limiting the operational life of the device. It has been empirically shown that the rate of thermally accelerated processes should increase with temperature according to the Arrhenius relation (1:204). However, it may not be valid to assume all GaAs MESFET failure mechanisms are accelerated with temperature in this way, since the physical processes of all of the different failure mechanisms have not been determined. Moreover, even if all of the failure mechanisms are accelerated with temperature according to the Arrhenius relation, the degree of acceleration could be different for some of the failure mechanisms. If this were true, a failure mechanism that is dominant at conventional operating temperatures could be masked at accelerated life test temperatures by another failure mechanism which was significantly enhanced with temperature. To correctly extrapolate the reliability of a device from accelerated temperature life test data, the same failure mechanisms must be causing device failure at both the elevated life test temperatures and normal operating temperatures (1:203). Since GaAs MESFETs are fairly new in comparison to the desired operational life times of up to 10 years, there is very little practical long term reliability information at normal operating temperatures. Therefore, to verify the validity of extrapolating the accelerated temperature life test results to normal operating temperatures, each of the failure mechanisms not causing failure at the elevated temperatures needs to be identified and examined separately to determine if it effects the overall reliability at normal operating temperatures.

As a specific application of GaAs MESFETs, the Defense Satellite Communications System (DSCS) program office is developing a prototype, 10 watt, X-band solid state amplifier (SSA) utilizing GaAs MESFETs (8:SEC II). Two types of GaAs MESFET devices are being used in this amplifier design, the NEC NE 868898 and the Fujitsu, Ltd FLM 7177-5SHL (8:SEC I). The NEC MESFET is rated at approximately 33 dBm saturated output power and is used in the SSA as a driver amplifier operated at 31 dBm maximum output power in its linear gain region (8:SEC II). The Fujitsu MESFET is used in the SSA as a saturated output stage with a design output power of 37.2 dBm (8:SEC II).

General Electric (GE), the prime Air Force contractor for DSCS-III and manufacturer of the SSA, performed accelerated temperature life testing under rf drive on these devices and have reported their results (8). This testing was performed on 12 of each device type (8:SEC II). Although the report concluded that the devices are very reliable, on the order of 10^6-10^7 hours MTTF (8:SEC IV), questions still exist on the conclusiveness of the life testing. In this study, only five of the NEC devices and two of the Fujitsu devices were tested to the failure criteria (8:SEC IV). Most of the time-to-failure data was extrapolated from the device's degradation curves (8:SEC IV). With such a limited number of devices taken to failure, concerns over the validity of the MTTF calculations at test temperatures were raised. To gain increased confidence in the reliability of these devices, the Jet Propulsion Laboratory (JPL) was requested to perform further accelerated life testing under rf drive. These tests would take all devices under test to failure, and they are still in progress. In addition, similar to the other reliability studies of GaAs MESFETs, the GE study, as well as the JPL study, assume that all failure mechanisms are accelerated according to the Arrhenius relation, and that the same failure mechanisms that are dominant at test temperatures are also dominant at normal operating temperatures. The concern regarding the validity of projecting the MTTF at normal operating temperatures from either the GE or JPL life tests is whether these assumptions are correct. Since long term operational reliability data is not available on these devices to determine prominent failure mechanisms, each failure mechanism must be identified and examined separately to determine if accelerated temperature life testing has adequately addressed its contribution to overall reliability. If the selected failure mechanism is not accelerated by temperature as quickly as those causing failure at test temperatures, then it could detrimentally effect the MTTF of the device under normal operations. It is important to understand that if the failure mechanism under investigation was not adequately tested by accelerated temperature life testing, it only means that its contribution to the overall reliability of the device under normal operations is not known. Potentially, it could have no effect on the overall reliability. However, if the failure mechanism has not been adequately addressed by accelerated temperature life testing, its effect on the overall reliability of the device needs to be addressed by other methods. These methods could include theoretical analysis, tests accelerating this failure mechanism by conditions other than temperature, or long term life tests under normal operating conditions (1:203; 26:159-160, 440-441).

A key failure mechanism in GaAs MESFETs is gate-to-drain avalanche breakdown. Gate-to-drain avalanche breakdown in combination with forward gate conduction is the power saturation mechanism in GaAs MESFETs (11:962). Therefore, if a GaAs MESFET is operating near its saturation level, the combination of dc bias and the rf voltage swing will induce gate-to-drain avalanche breakdown (2:20). Since many applications of GaAs MESFETs are as saturated power amplifiers, this failure mechanism will be constantly exercised in normal operation. One of the measurable indications of avalanche breakdown in a GaAs MESFET under normal operating conditions is light emission (4:572). The light emitted by a GaAs MESFET under rf drive is caused by the transient, high-reverse bias due to the combination of dc and rf levels, causing avalanche breakdown at the drain-side edge of the gate (2:20; 11:962-963). Based on this relationship, measuring the light emissions of a given device will partially check the validity of the assumption that all failure mechanisms are accelerated equally with temperature. These measurements, taken over a temperature range from normal operating temperatures to accelerated life test temperatures while the device is under rf drive, will indicate the variation in the amount of avalanche multiplication occurring at different temperatures. Comparing these variations to the temperature acceleration for all failure mechanisms used in the GE life test, should clarify the validity of the assumption that all failure mechanisms are accelerated equally with temperature.

Objective

The overall objective of this investigation is to determine if the reliability studies concerned with the Fujitsu FLM 7177-5 GaAs MESFET proposed for use in the DSCS III satellite have adequately accounted for the gate-to-drain avalanche breakdown failure mechanism. This overall objective can be accomplished by evaluating the results of a set of specific goals:

1. By adapting an existing analytical model (11) for temperature effects (12) and considering the specific device parameters of the Fujitsu GaAs MESFET, it will be possible to predict the variation of gate-to-drain avalanche multiplication with respect to temperature.

2. Using the predicted variation in avalanche multiplication, it will be possible to predict the associated changes in the intensity of the emitted light.

3. Devise a test configuration capable of making measurements of light emissions, rf power levels, and dc bias values at temperatures ranging from normal operating temperatures to accelerated life test temperatures.

4. Using this instrumentation scheme, it will be possible to experimentally verify the predicted variations in emitted light intensities. This

will validate the model of avalanche multiplication variation with temperature.

5. Lastly, this model will be used as a partial evaluation of the assumption made in the reliability studies that all failure mechanisms, including avalanche multiplication, are accelerated equally with temperature.

Scope and Assumptions

The analytical model used in this investigation is a two-dimensional model. As such, it can be used to predict avalanche multiplication at one, minutely thin slice of the MESFET channel. It does not predict the fluctuation of avalanche multiplication along the width of the gate, and therefore, when used as a basis to predict the intensity of light emissions, it can only predict the relative variation with temperature assuming the entire gate width is in avalanche breakdown. However, since only the relative, not absolute, variation with temperature is needed to determine the validity of accelerated temperature life test assumptions, this analytical model was considered adequate. Even though the assumption of uniform light emission along the width of the gate was used in developing the theoretical prediction of light emission presented in Chapter II, much better correlation with the test results was achieved using the fundamentals of a model to predict the number of microplasmas occurring in the device. This model is discussed along with the test results in Chapter IV. In addition, the analytical model is based on a planar device. The Fujitsu 7177-5 device is a recessed gate design (18). But, some of the effects of recessing the gate tend to increase the breakdown voltage while others decrease it (11:968). Therefore, since these effects are quite difficult to model, and only relative changes with respect to temperature are necessary for the purposes of this investigation, the planar model was considered adequate (11:968).

Since the photomultiplier tube has demonstrated adequate sensitivity to measure the light emissions of lidded devices, it is assumed that all the measurements in this experiment can be made through the device lid. If the transmittance characteristics are relatively constant, the presence of the lid should not corrupt the results by effecting the total amount of detectable light differently under varying test conditions. The device's lid is constructed of alumina (Al_2O_3) (18). Based on empirical transmittance data above 1 μm and absorbtion data below 1 μm, alumina has relatively constant transmittance characteristics over the entire near infra-red spectrum (0.720 - 1.400 μm) (28). This assessment assumes that scattering, cause by material pore sizes near the wavelength of the incident illumination, is not significant in this frequency range (28).

Only one Fujitsu GaAs MESFET will be tested. Since this test device was one of the devices used in the General

Electric accelerated temperature life test program, it has already exhibited degradation in output power capability. However, it is assumed that since this thesis project is only making relative measurements between parameters under different test conditions (temperature, bias level, etc.), that the relationships between measured parameters on this device will be representative of undegraded devices. Inherent in this assumption is that the output power degrades linearly with respect to the other device parameters. Then, the relative measurements of this degraded device will be representative of a new device.

Experimental Approach

The experiment was conducted by installing the test device in an instrumented rf amplifier circuit. Figure 1.1 is a schematic of the experimental arrangement. This configuration facilitates the measurement of all the basic operating parameters: gate-to-source voltage (V_{GS}), gate-to-source current (I_{GS}), drain-to-source voltage (V_{DS}), drain-to-source current (I_{DS}), rf input power (P_{IN}), and rf output power (P_{OUT}). In addition, the test arrangement monitors the light output of the device, which is measured by a photomultiplier tube. The actual test device is mounted in a specially fabricated test fixture. The test fixture is constructed to provide thermal isolation, temperature control and monitoring, and a light tight mounting flange for the photomultiplier tube. The gate and

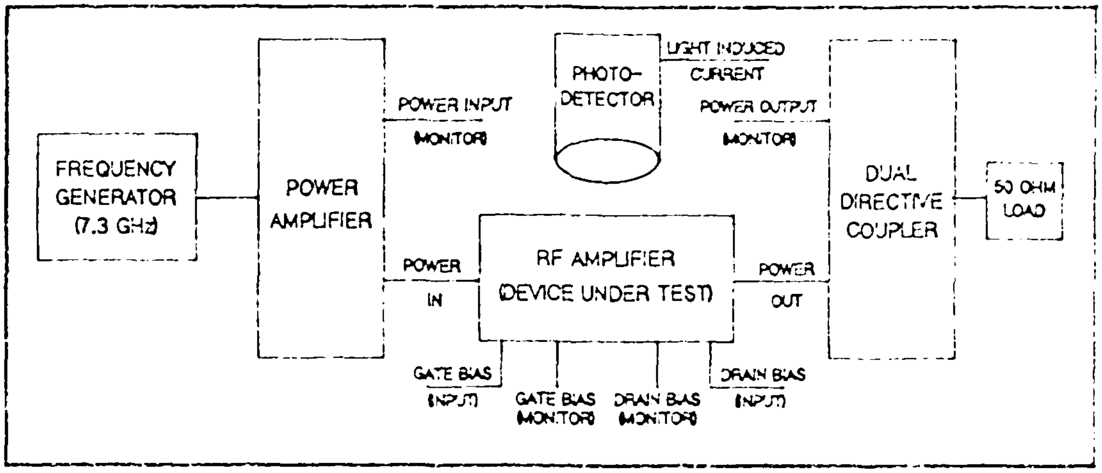


Figure 1.1. Experimental arrangement used to measure light emissions, input and output power, and dc bias levels.

drain are connected to twin-sleeve tuners to allow the device to be tuned for maximum output. The power amplifier is a TWTA with P_{IN} monitored through the test port of a dual-directional coupler, which is connected to the output of the TWTA. A similar configuration is used to monitor P_{OUT} using a dual-directional coupler. Both P_{IN} and P_{OUT} are measured by digital power meters. The photomultiplier tube is used with a precision ammeter to measure light induced current (I_{LE}).

Sequence of Presentation

Chapter II provides background information on accelerated life testing and avalanche breakdown in GaAs MESFETs. It describes the theoretical development associated with the relative variation of avalanche multiplication and light emission with temperature. It also provides background information on gate-to-drain avalanche breakdown in GaAs MESFETs. Specifically, it describes the theory of reliability testing as applied to semiconductor devices. This discussion addresses accelerated life testing and the Arrhenius relation. The concepts of failure mechanisms and their associated activation energies is also included. Next, a description of pertinent reliability tests accomplished with GaAs power MESFETs, and the specific tests that have been accomplished on the Fujitsu device are discussed. In addition, Chapter II describes the adaptation of an existing analytical model to predict the relative variation of avalanche multiplication with respect to temperature. Finally, building on the results of this model, it describes the generation of a theoretical prediction for the relative variation of the intensity of light emissions with respect to temperature.

The remaining chapters describe the experiment and presents the results, conclusions and recommendations. Chapter III describes the experimental instrumentation configuration and test procedures used to gather the data to verify the theoretical predictions of Chapter II. Chapter IV evaluates the test arrangement and compares the experimental results with those predicted in Chapter II. Chapter V reports the findings that can be concluded from this experiment. In addition, it makes recommendations for future testing to gain additional understanding and confidence in the reliability of these GaAs MESFETs.

II. Background

This chapter provides background information on accelerated life testing, avalanche breakdown in GaAs MESFETs, and light emission from GaAs MESFETs. The fundamentals and application of accelerated life testing to GaAs MESFETs is explained in some detail to emphasize the concern that the reliability predictions made from accelerated temperature life tests of GaAs MESFETs may not include the effects of all failure mechanisms. In addition, avalanche breakdown is discussed because it is a key failure mechanism and is continuously active in many applications. An existing model of gate-to-drain avalanche breakdown in GaAs MESFETs is presented and adapted for predicting the breakdown voltage with respect to temperature for the device under test. Lastly, to provide for experimental verification of this model, the fundamentals of light emission from GaAs MESFETs are discussed, and prediction of light emission variations with respect to temperature based on the avalanche breakdown model is made for the device under test.

Accelerated Life Testing

Fundamentals. One of the advantages of using solid-state devices in place of TWTAs in high reliability systems is that a solid-state device's reliability can be predicted from accelerated life testing. Accelerated life testing is most easily described as accelerated stress testing and is applicable to many different components. It is a test method where an equivalent amount of stress associated with long-term normal operations is applied to the device in a much shorter time period. In addition, since the failure rate of the device increases while under these higher stress levels, a much smaller lot size of devices can be evaluated to provide statistically meaningful data. Therefore, accelerated life tests are recognized as a very practical method of testing for reliability assurance (1:203). Any of the stress types (for example: shock, vibration, thermal) acting on the device during normal operations can be accelerated in life testing. The initial task is to find the stress type causing the predominant number of failures in normal operations. In many cases this stress type is obvious from either the device application or routine failure analysis; however, in some instances, where it is difficult to determine if failures are being induced by just shock, vibration, or thermal stress alone, it may be necessary to perform multiple accelerated tests, with each of the different stress types, to determine overall reliability. Once the type of stress being applied to the device is determined, the goal of the test is to accelerate the associated failure mechanism in a way that maintains a fixed relationship between test results and the expected failure rate in normal use. The primary requirement is that the same failure mechanism(s) dominates the cause of failures relative to all of the stress levels, including normal operating levels and accelerated levels (1:203). The other requirement is that the physical failure mechanism(s) needs to be understood sufficiently to assure the proper extrapolation of failure rates to lower stress levels. "An important implication is that a test which is established to accelerate a particular failure will only provide information about that mechanism, or those which are similarly accelerated. It will not tell anything about mechanisms that are not accelerated by that stress but which may still be important in the application." (1:203).

Application to Semiconductors. Accelerated life testing is a very useful tool in determining the reliability of semiconductor devices. An obvious important stress in semiconductors is temperature. Consequently, accelerated temperature life testing is frequently used to evaluate semiconductor devices. It is an empirically observed phenomenon regarding thermally accelerated processes, that the rate of the process is dependent upon temperature according to the Arrhenius relation (1:204):

$$R = R_O \text{ EXP } (-E_A/kT_k) \qquad (2.1)$$

where

R = the reaction rate
R_o = a constant
E_A = activation energy
k = Boltzmann's constant
T_k = absolute temperature.

The failure rate associated with a failure mechanism that is accelerated by temperature is related to the mechanism's increased reaction rate and, therefore, should also follow the Arrhenius relation (1:204). The Arrhenius relation provides the fixed relationship, discussed in the previous section, for extrapolating failure rates to lower stress levels. However, this extrapolation will only be correct if the same failure mode(s) dominating at normal operating temperatures also dominate at the accelerated test temperatures, and the associated failure mechanism(s) of these mode(s) do in fact follow the Arrhenius relation. A failure mode describes how the device fails as a result of a failure mechanism. If the two criteria above are satisfied, then a mean-time-to-failure (MTTF) can be predicted for normal operating temperatures by experimentally establishing a MTTF at two different accelerated temperatures. In order to extrapolate the failure rates to lower operating temperatures, and thus to predict the MTTF at any given operating temperature, a curve of MTTF versus 1/T is drawn. Since the failure rates follow the Arrhenius relation, the shape of the curve (linear on a semi-log scale) is defined and the two experimental test points define the slope of the line (a function of the activation energy). Figure 2.1 is an example of such a plot.

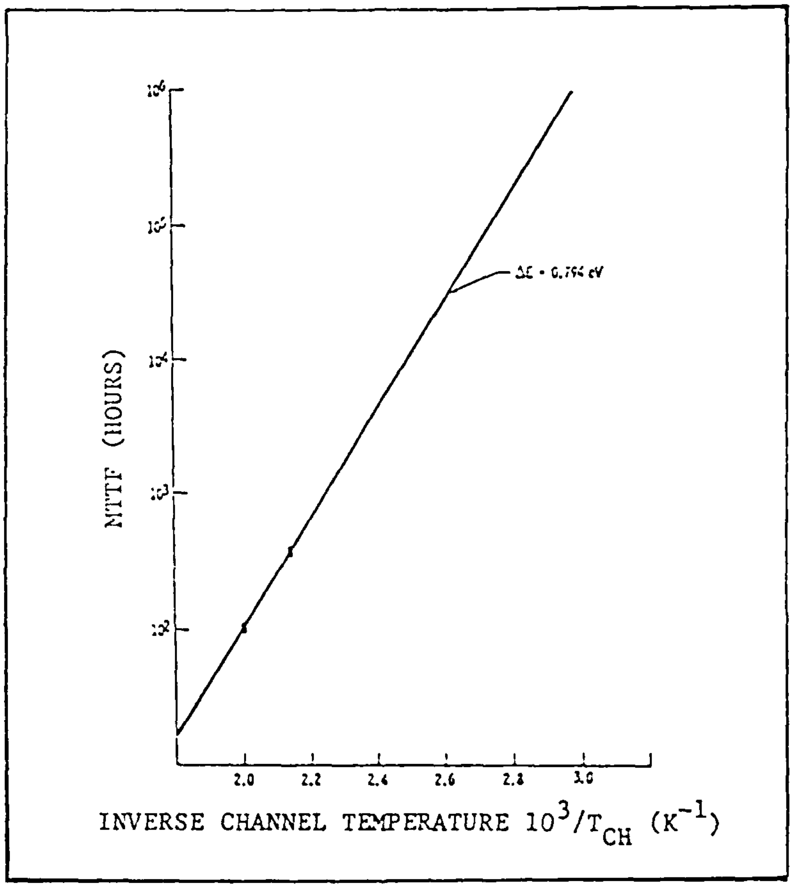


Figure 2.1. Example MTTF versus channel temperature graph (29:16).

Application to GaAs MESFETs. The accelerated temperature life testing techniques described above have been applied to GaAs MESFETs. Many tests have been accomplished with numerous GaAs MESFET designs, and the reports conclude they are very reliable devices (5:395;

6:151; 7:321; 8:SEC IV). However, these conclusions were based on assumptions about the failure mechanism(s) to permit the extrapolation of MTTFs at normal operating temperatures. The failure mechanisms causing failure at high temperatures were assumed to be the same ones that would cause failure at normal temperatures (5:395; 6:151; 7:321; 8:SEC IV). The failure mechanisms were assumed to be accelerated according to the Arrhenius relation and, therefore, could be extrapolated to normal temperatures. Neither of these assumptions were verified. In fact, without long-term normal operating temperature data, it cannot be determined with absolute certainty which failure mechanism(s) will be the predominant cause of failure at normal operating temperatures. Therefore, to verify the validity of extrapolating the accelerated temperature life test results to normal operating temperatures, each of the failure mechanisms not causing failure at the elevated temperatures needs to be identified and examined separately to determine if it effects the overall reliability at normal operating temperatures.

Fujitsu GaAs MESFET Testing. As a specific example, the Fujitsu FLM 7177-5 device used in this experiment was life tested by General Electric (8). A total of 12 devices were tested. However, three of the devices were catastrophically damaged by the test apparatus. Of the remaining nine devices, six were tested at 195 °C and the other three at 225 °C. A gradual degradation failure criteria was established. In a properly designed and fabricated GaAs MESFET, catastrophic failure is not the major factor in determining the useful lifetime of the device; the major factor is gradual degradation (14:5,6). This gradual degradation eventually reduces the power output to the point where it will no longer satisfy the minimum circuit requirements. "It is quite common to perform a reliability analysis on life test results of power GaAs FETs assuming an arbitrary failure definition such as a 1.0 dB decrease in output power." (14:5). The failure criteria established for the FLM 7177-5 used in the SSA was a 1.0 dB degradation in output power. This gradual degradation in output power was verified as the major failure mode, since it occurred prior to any catastrophic failure mechanism or any other performance degradation. The test was performed for 6000 hours of operation. During this time, only two devices, one at each test temperature, exceeded the 1.0 dB degradation failure criteria. Time to failure data was extrapolated for the other devices from their degradation curves. The conclusion of this life test was that the FLM 7177-5 was highly reliable with a projected MTTF of 2.4×10^6 hours at a T_{CH} of 125 °C. Figure 2.2 shows the Arrhenius plot for this life test. Consistent with Figure 2.1, the experimental data in Figure 2.2 represents the mean-time-to-failure of all of the

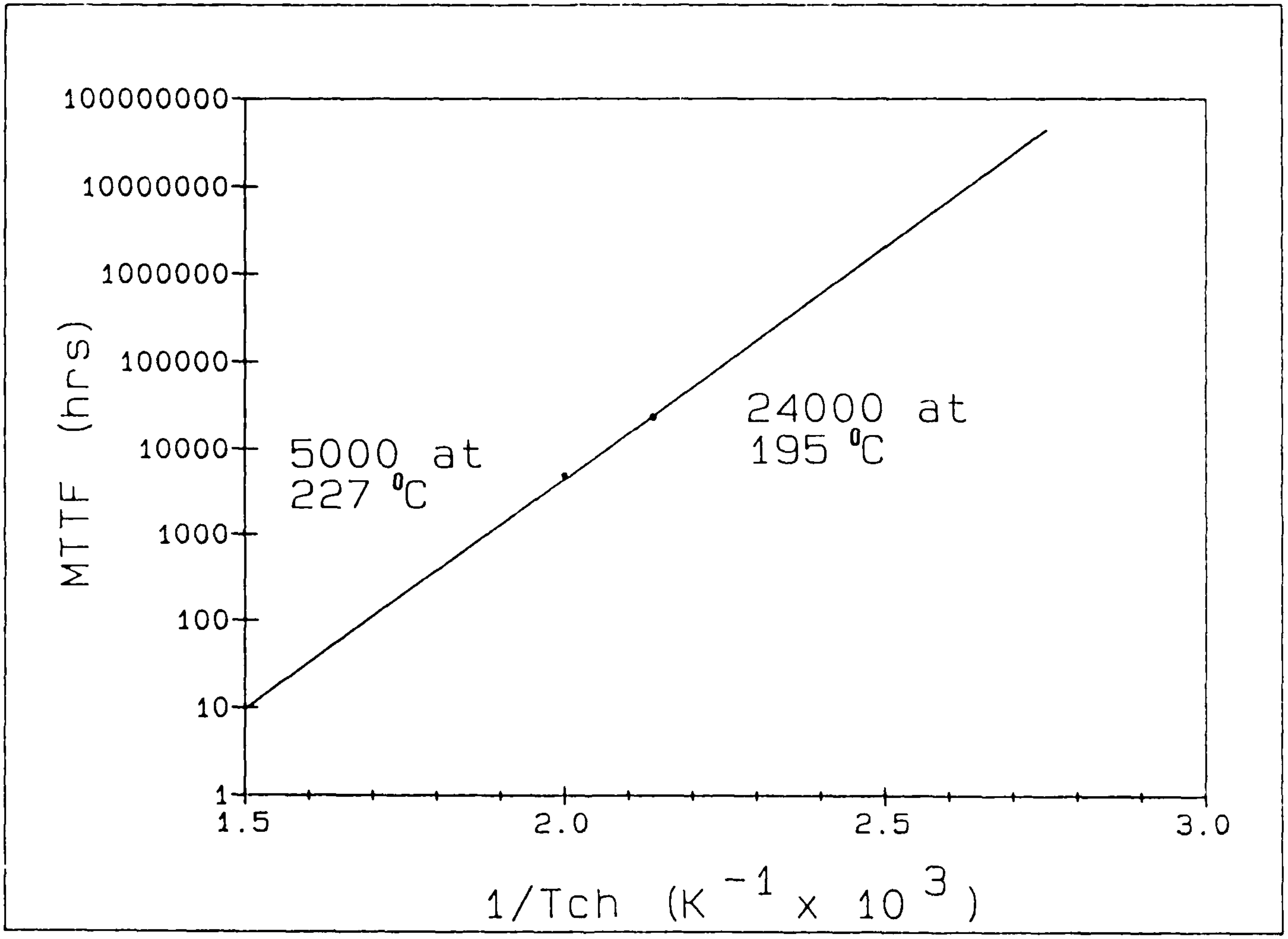


Figure 2.2. Arrhenius plot of life test data for the FLM 7177-5 GaAs MESFET (8:SEC V,14).

devices tested in the GE life test at that temperature. An additional conclusion of the life test program was that the results supported other test results on similar devices that projected MTTFs in the 10^6 - 10^7 range.

Concerns. Many concerns could be expressed over the conclusions from life tests on GaAs MESFETs. Specifically, with respect to the FLM 7177-5 testing, there could be concerns regarding the statistical significance of the size of the sample lots or the method of extrapolating the device's MTTFs. However, one concern that is applicable to all the life tests is whether failure mechanisms prevalent under long term, normal rf operations may not be prevalent at high test temperatures. The overall reliability of a device is determined by a set of different failure mechanisms. Under any particular condition, any one of these or a subset of these failure mechanisms could be dominant, limiting the lifetime of the device by causing device failure. Although it has been empirically shown that the rate of thermally accelerated processes should increase with temperature according to the Arrhenius relation (1:204), it may not be valid to assume all GaAs MESFET failure mechanisms are accelerated with temperature since a physical description of all the different failure mechanisms have not been determined. Moreover, even if all of the failure mechanisms are accelerated with temperature according to the Arrhenius relation, the degree of acceleration could be different for some of the failure mechanisms. If this were true, a failure mechanism that is dominant at operating temperatures could be masked at accelerated life test temperatures by another failure mechanism which was accelerated much faster with temperature. To correctly extrapolate the reliability of a device from accelerated temperature life test data, the same failure mechanisms must be causing device failure at both the elevated life test temperatures and normal operating temperatures (1:203). Since GaAs MESFETs are fairly new in comparison to the desired lifetimes of up to 10 years, there is very little practical long term reliability information at normal operating temperatures. Therefore, to verify the validity of extrapolating the accelerated temperature life test results to normal operating temperatures, each of the failure mechanisms not causing failure at the elevated temperatures needs to be identified and examined separately to determine if it effects the overall reliability at normal operating temperatures. This concern is reinforced by the preliminary results of the concurrent JPL accelerated temperature life test. In the JPL test, the control device (operated under the same rf drive as the test devices, but at normal temperatures) is presently exhibiting more degradation than the test devices (15). If this data is valid, then some failure mechanism is dominating gradual power degradation at normal temperatures and is decreasing with temperature. This investigation will examine one of the FLM 7177-5 MESFET failure mechanisms to verify, for this failure mechanism only, the assumption made in the GE life test that all failure mechanisms follow the Arrhenius relation. The failure mechanism chosen is the gate-to-drain avalanche breakdown, since it is present whenever the device is operated in saturation. The FLM 7177-5 is used in the SSA design as a saturated output stage (3:SEC II), and therefore, is constantly exercising the gate-to-drain breakdown mechanism. The validity of the GE assumption for gate-to-drain avalanche breakdown is determined by developing a theoretical model for the variation of the gate-to-drain breakdown voltage (V_B) with temperature. Since gate-to-drain breakdown only occurs when the combination of dc bias and rf voltage swing exceeds V_B, the output of the model is used in predicting the variation of the percentage of time the device is in breakdown with respect to temperature. These results are verified by experimental measurement of the light emissions caused by the breakdown in one FLM 7177-5 device. Once verified, the results are compared to the acceleration curve used to extrapolate failure rates at normal operating temperatures.

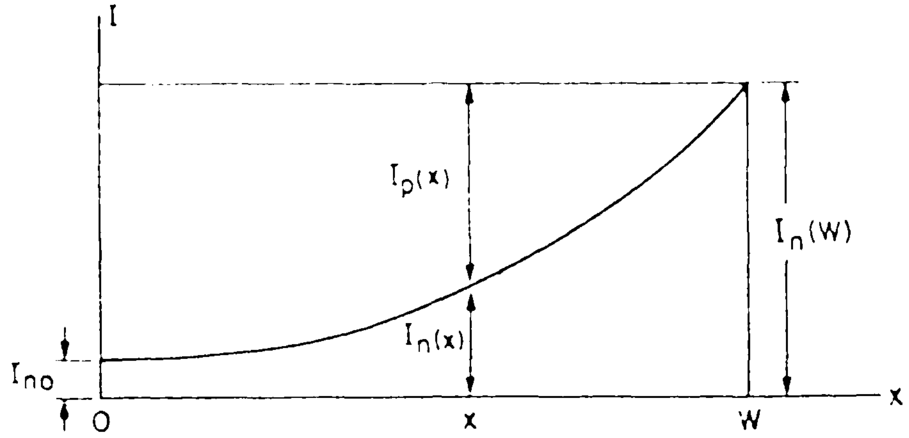


Figure 2.3. Depletion region in a p-n junction with multiplication of an incident current (16:102).

Avalanche Multiplication

Background. If a large electric field is applied to a semiconductor, the carriers may gain enough kinetic energy that when they collide with the lattice they will break a bond. By breaking a bond, or ionizing a valence electron from the valence band to the conduction band, an electron-hole pair is generated. In turn, the free carriers of the electron-hole pair are accelerated by the high field and can, on collision with the lattice, generate other electron-hole pairs. The process of generating an electron-hole pair from a carrier collision with the lattice is called impact ionization (16:102). In addition, because many of these free electron-hole pair carriers collide and generate additional electron-hole pairs, this process is known as avalanche multiplication (16:102). In the case of a p^+-n, one-sided abrupt junction shown in Figure 2.3, if the electric field in the depletion region is high enough to initiate impact ionization, the electron current I_n will increase with distance through the depletion region. If the edges of the depletion region are defined as 0 and W, with x (distance) increasing from 0 to W, then (16:102):

$$I_n(W) = M_n I_n(0) \tag{2.2}$$

where

$I_n(0)$ = the electron current entering the depletion region at x=0
$I_n(W)$ = the electron current exiting the depletion region at x=W
M_n = the avalanche or multiplication factor.

A similar equation can be written for the increase in hole current from x = W to x = 0 . By examining the incremental electron current, and assuming that the electron and hole ionization coefficients are equal, Sze (16) shows that:

$$1 - \frac{1}{M_n} = \int_0^W \alpha[E(x)]\, dx \tag{2.3}$$

where

$\alpha = \alpha_p = \alpha_n$ = the ionization coefficient (cm^{-1})
E(x) = the electric field as a function of distance (x) (V/cm).

Since the avalanche breakdown voltage is defined as the voltage where M_n approaches infinity (16:103), the breakdown condition is given by:

$$\int_0^W \alpha[E(x)]\, dx = 1 . \qquad (2.4)$$

Because the ionization coefficient is highly dependent on the electric field, a critical field and therefore, a critical voltage (V_B) for avalanche breakdown can be calculated.

Gate-to-Drain Breakdown in GaAs MESFETs. To understand gate-to-drain breakdown in GaAs MESFETs, one must understand the operation of these devices under large-signal conditions. Typical state-of-the-art devices exhibit output power saturation at input powers considerably below power levels causing catastrophic failures. Figures 2.4a and 2.4b show the output power and gate current of a typical X-band power FET as a function of input power for two gate-to-source bias (V_{GS}) levels. Frensley (11) concludes that the power saturation mechanisms are associated with two competing gate current producing processes. The first process, gate-to-drain breakdown, causes the negative gate current. The second process, forward gate conduction, causes the positive gate current. Both of these processes are produced by the combination of the dc bias and rf voltage swing. In addition, the processes occur in different portions of the rf voltage cycle. Gate-to-drain breakdown occurs when the peak rf voltage combined with the dc bias voltages exceeds

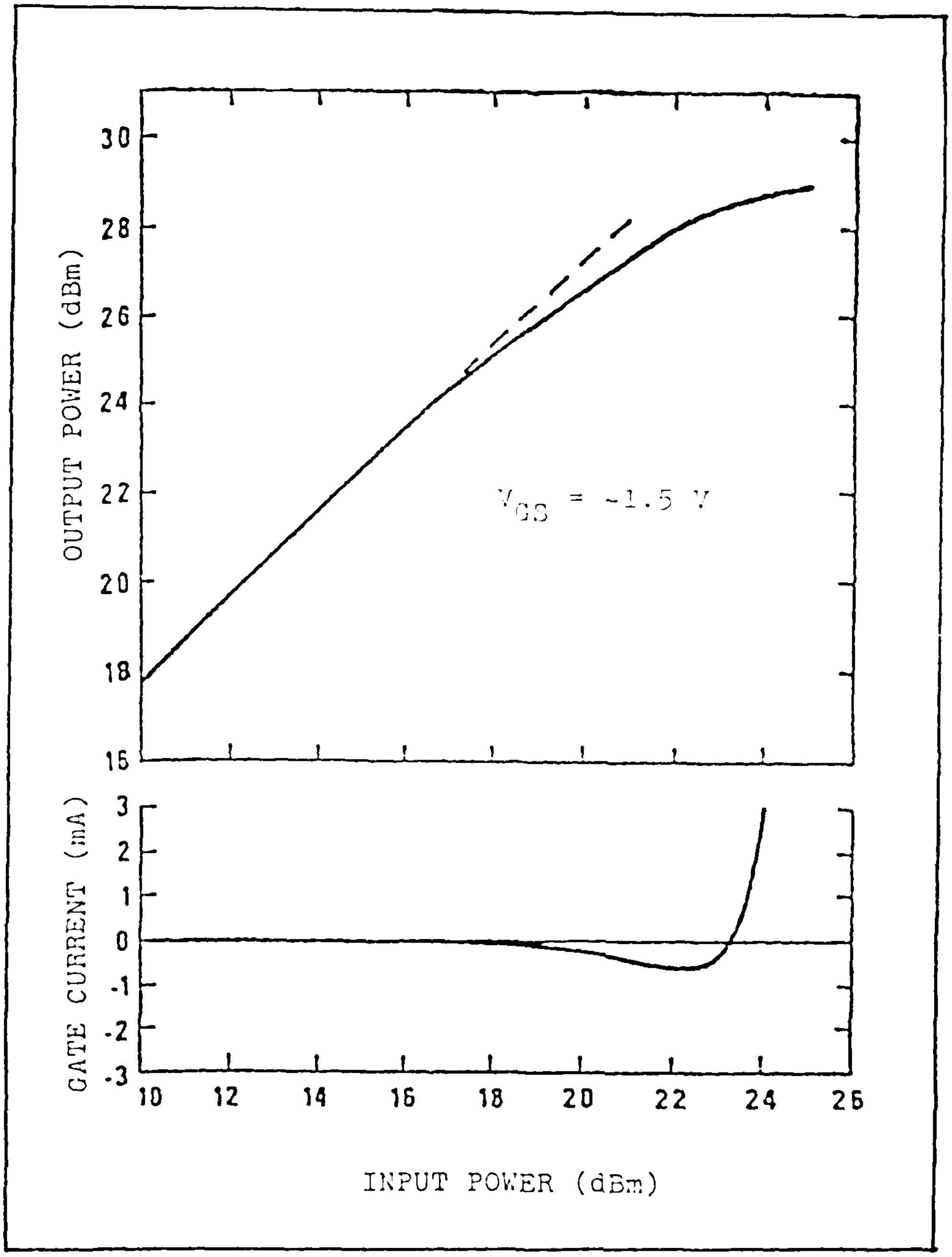


Figure 2.4a. Output power characteristic of a 1.2-mm gate width GaAs MESFET at 10 GHz with the gate biased at -1.5 V. The lower plot of gate current as a function of input microwave power shows evidence of both forward and reverse conduction (11:963).

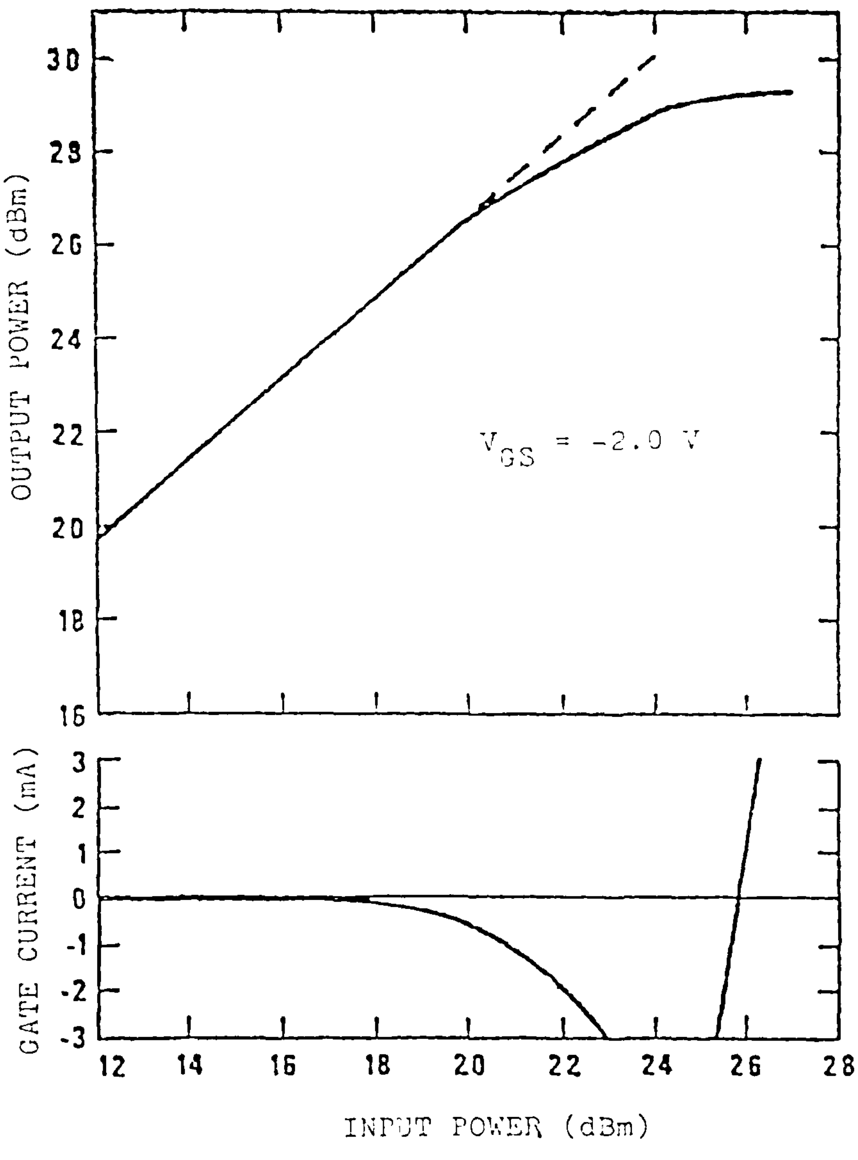


Figure 2.4b. Output power characteristic of a 1.2-mm gate width GaAs MESFET at 10 GHz with the gate biased at -2.0 V. Gate current shows much more pronounced reverse conduction than in Figure 2.4a (11:963).

the breakdown voltage of the device. In contrast, forward gate conduction occurs when the rf voltage is at a minimum, which when combined with the dc bias voltages reduces the instantaneous drain voltage to the point where the gate is forward biased. As a result, it might be anticipated that since the average gate current is the sum of both phenomenon, it will change dramatically if the V_{GS} bias point is changed. Indeed, comparing Figures 2.4a and 2.4b reveals that lowering V_{GS} from -1.5 V to -2.0 V dramatically changes the gate current. In particular the gate current becomes negative sooner, and the magnitude of the negative current increases prior to the forward current dominating the curve. Both of these processes are present in a saturated GaAs MESFET. Even if the average saturation gate current is positive, an instantaneous negative current component associated with gate-to-drain breakdown is present. Another way of visualizing the large-signal operation of a power GaAs FET is by using a load line diagram. Figure 2.5 depicts the drain characteristic curves associated with an ideal GaAs MESFET. A maximum-power load line is superimposed on the curve. From this curve, it is observed that the gate-to-drain breakdown phenomenon occurs at high drain voltage and low drain current corresponding to the region of Figure 2.5 labeled 'A'. Lastly, the interaction of the dc bias and the rf

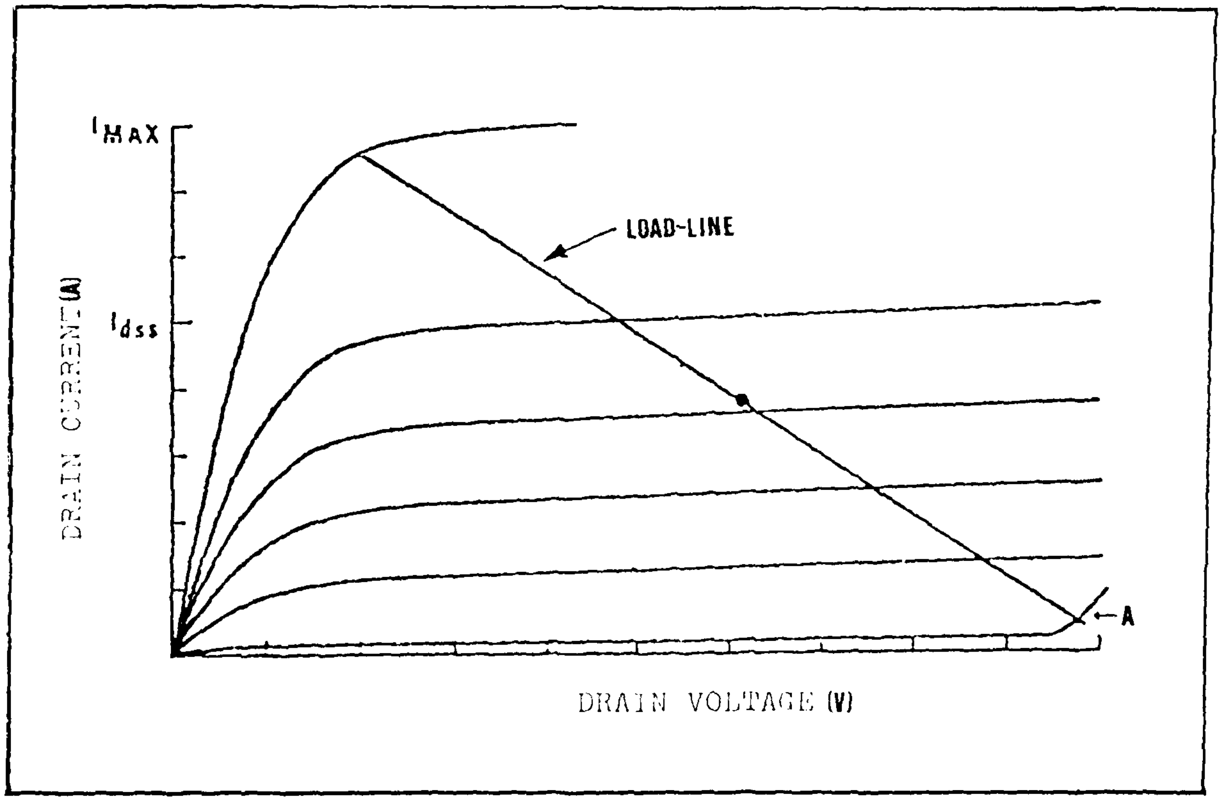


Figure 2.5. Drain characteristics of an idealized GaAs *MESFET with* a maximum-power load-line superimposed. *Under large-signal operation,* devices swing from the high-current, low-voltage region to the low-current, high-voltage region indicated by 'A' (11:963).

voltage causing the gate-to-drain breakdown can be depicted with respect to the output rf signal. Figure 2.6 shows the output of an ideal GaAs MESFET amplifying a perfect sine wave signal. The rf output, v(t), is offset by the dc bias, V_{DS}. Gate-to-drain breakdown would occur in a non-ideal device when the potential between the gate and drain equals or exceeds V_B, that is $[v(t) + V_{DS} - V_{GS}] \geq V_B$. Therefore, in Figure 2.6 a non-ideal device would be in breakdown between θ_1 and θ_2, which corresponds to the region labeled 'A' on the load line of Figure 2.5. From Figure 2.6, the amount of time the device is in avalanche breakdown per rf cycle is $(t_2 - t_1)$, where $\theta_2 = \omega t_2$ and $\theta_1 = \omega t_1$. Therefore, under continuous rf operation, the percentage of time the device is in avalanche breakdown (T_B) is:

$$T_B = (\omega t_2 - \omega t_1)/2\pi \ . \tag{2.4}$$

Since

$$\omega t_1 = \arcsin\,[(V_B + V_{GS})/(V_M + V_{DS})] \tag{2.5}$$

and

$$\omega t_1 = \pi - \omega t_2 \tag{2.6}$$

then

$$T_B = \{\, \pi - 2\arcsin\,[(V_B + V_{GS})/(V_M + V_{DS})]\}/2\pi \ . \tag{2.7}$$

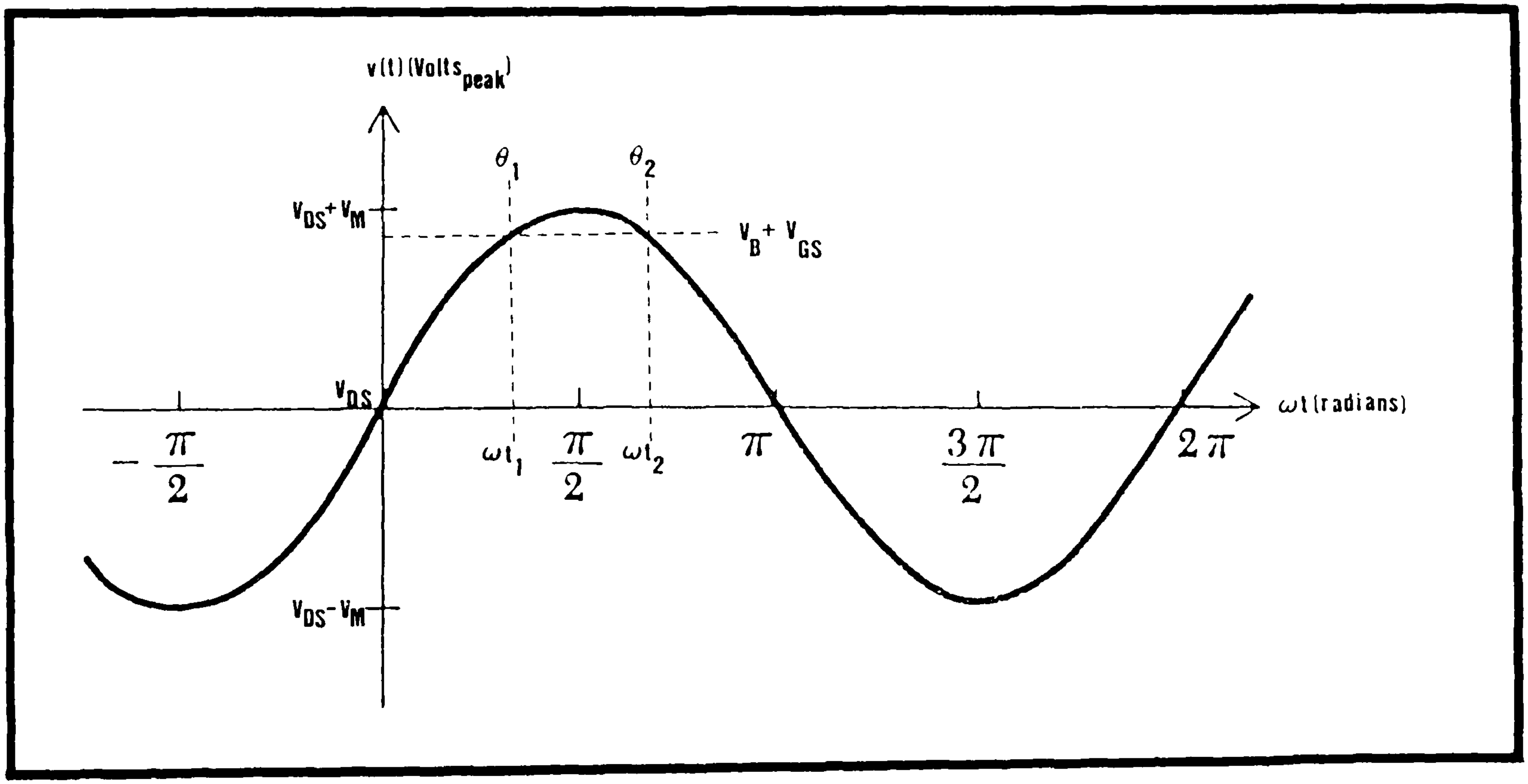


Figure 2.6. Output of an ideal GaAs MESFET under large-signal operation. The rf signal is a perfect sine wave. The portion of the signal between θ_1 and θ_2 would drive a non-ideal MESFET into gate-to-drain avalanche breakdown. This portion of the signal corresponds to the region of the load-line in Figure 2.5 indicated by 'A'.

If avalanche breakdown is the dominant failure mechanism, the MTTF of the device is related to the total amount of time the device is in avalanche breakdown. Since T_B is the percentage of time the device is in avalanche breakdown, the MTTF is inversely proportional to T_B. Therefore, any accelerated life testing should increase T_B and correspondingly accelerate the avalanche breakdown failure mechanism. To determine if accelerated temperature life testing is increasing T_B, Equation 2.7 can be calculated at several test temperatures. However, a method for determining V_B at these temperatures is required. The next section will show how an existing two-dimensional analytical model can be adapted for calculating V_B at different temperatures.

Adaptation of a Two-Dimensional Analytical Model. Frensley (11) has developed a two-dimensional analytical model to determine the breakdown voltage (V_B) as a function of several device parameters. Figure 2.7a shows the geometry of the analytical model for a MESFET at breakdown. The model permits the calculation of V_B by relating the electric field at the gate edge to the drain voltage. As shown in Figure 2.7a, the model is based upon a planar device with a rectangular depletion layer of depth 'a'; the active channel's length 'b' is measured from the gate edge to the boundary of the depletion layer. However, the Fujitsu FLM 7177-5 is composed of a pair of internally

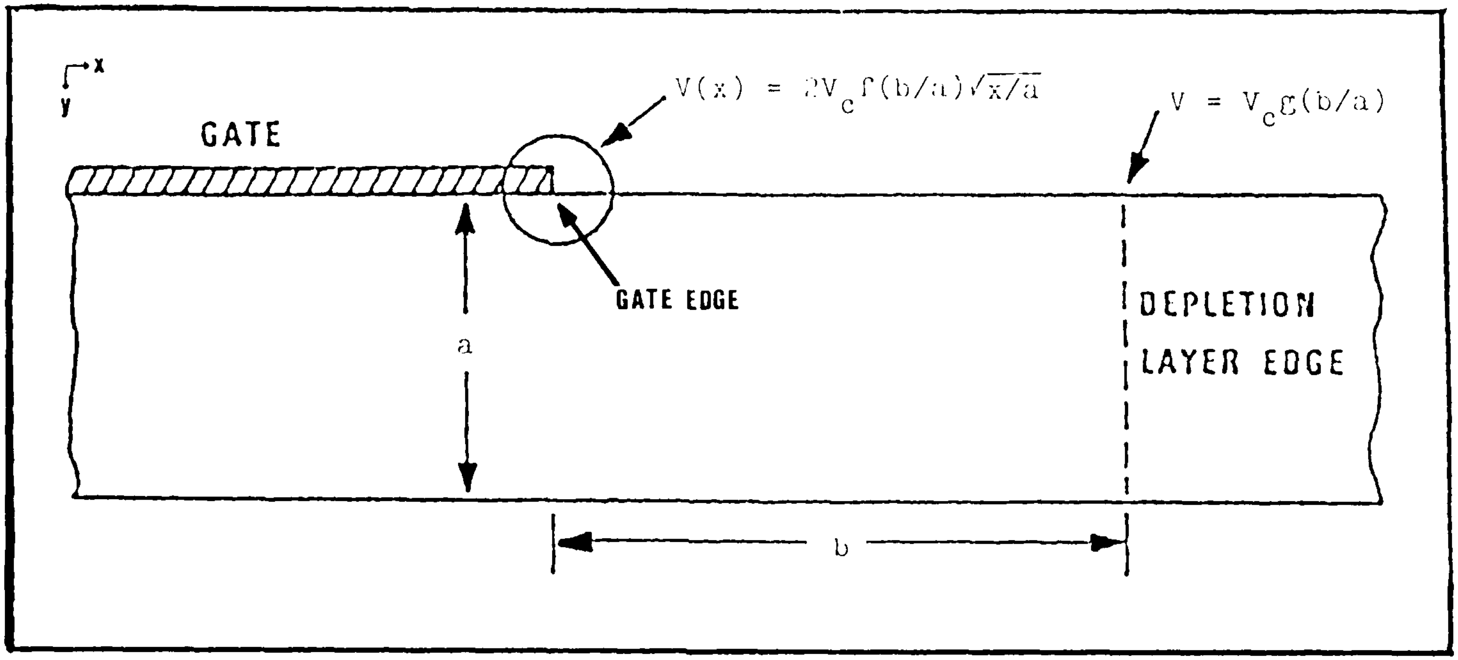


Figure 2.7a. Geometry associated with the analytic model for a planar MESFET at breakdown (11:966).

matched recessed-gate MESFETs. Figure 2.7b depicts the recessed gate geometry of the FLM 7177-5. Recessed-gate MESFETs, of course, will have a different breakdown voltage compared to planar devices. It is noted that the effects on breakdown voltage caused by recessing the gate are quite difficult to model, and of the two major effects, one tends to increase breakdown voltage while the others decrease it (11:968). The first of these effects is that recessing the gate causes the electric field [E(x)] to decrease more rapidly with distance (x) from the gate edge (11:968). This effect increases the breakdown voltage. The second effect results from the increased depth of the depletion region in the non-recessed portion of the device (11:968). Since the depth of the non-recessed portion of the depletion region is larger, the length of the depletion region (b) containing an equivalent total charge as the same area in the planar device will decrease (11:698). Since (as shown below) the breakdown voltage decreases as the ratio of b/a decreases, for the same active channel depth (a) this effect decreases the breakdown voltage (11:698). Therefore, for the purposes of this investigation, when the relative changes with respect to temperature are more important than the absolute value of the breakdown voltage, the planar model will be used, and the active channel depth (a) will be defined as the depth under the gate metallization as shown in Figure 2.7b.

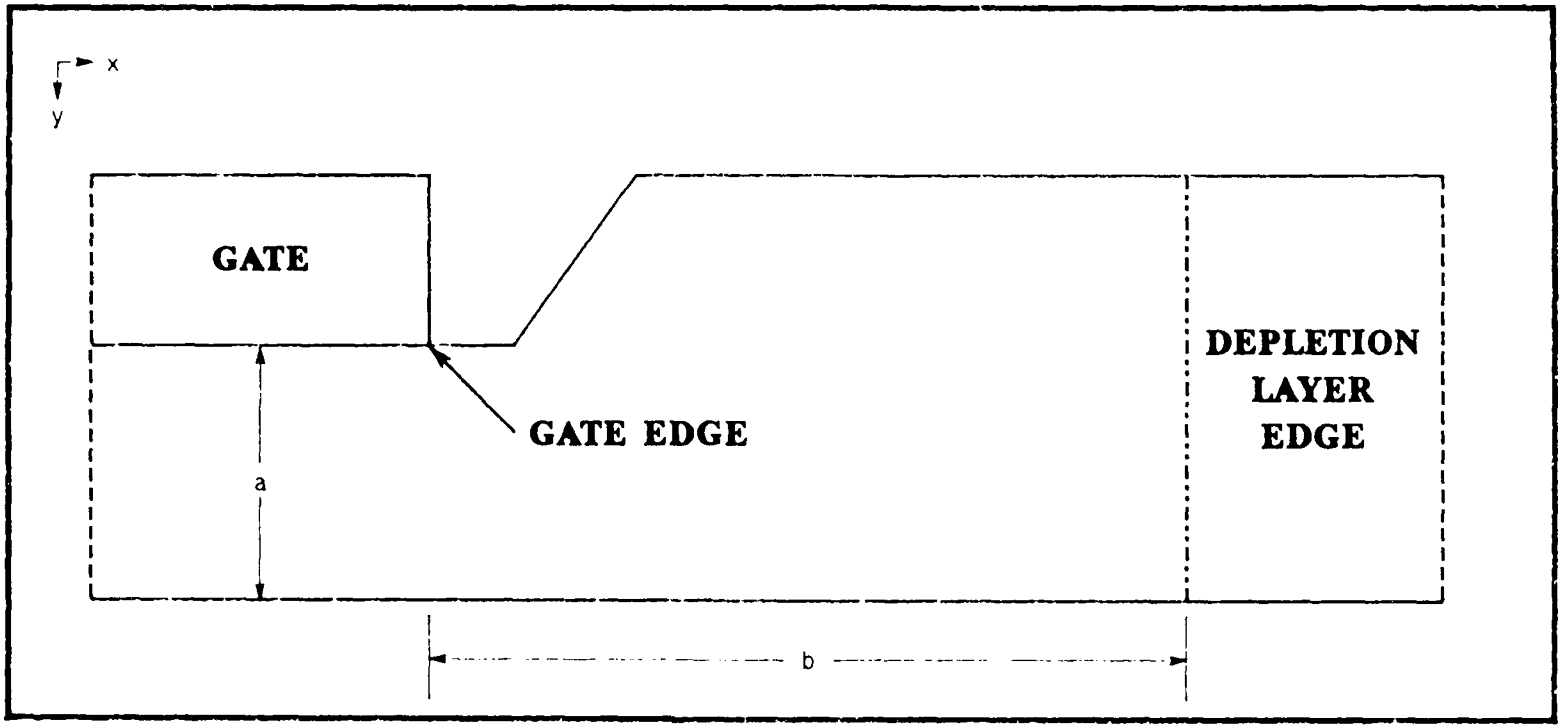


Figure 2.7b. Recessed gate geometry of the Fujitsu FLM 7177-5. The definition of active channel depth (a) and depletion layer length (b) for the analytic model is shown.

Frensley's model predicts voltages as a function of geometry, and a constant voltage (V_C) determined by device parameters. Equation 2.8 specifies the definition of V_C:

$$V_C = \frac{qa}{2\epsilon_S} \int_0^a N(y)\,dy \tag{2.8}$$

where

q = electron charge (1.60218×10^{-19} C)
a = active channel depth
ϵ_S = semiconductor permittivity (13.1 times the permittivity of free space) (17:350)
$N(y)$ = doping profile in active channel.

Note that for a uniformly doped structure, V_C is simply the pinchoff voltage which includes the built-in potential. Frensley (11) also shows that the drain voltage (V_{DS}) is:

$$V_{DS} = V_C g(b/a) \tag{2.9}$$

and the voltage along the surface near the gate edge is:

$$V(x) = 2V_C f(b/a)\sqrt{x/a} \tag{2.10}$$

where $f(b/a)$ and $g(b/a)$ are functions of the depletion-layer aspect ratio, and are shown in Figure 2.8. Therefore, V_{DS} at breakdown can be calculated once the depletion-layer aspect ratio at avalanche breakdown is determined. From Equation 2.10, Frensley (11) states that the electric field near the gate is:

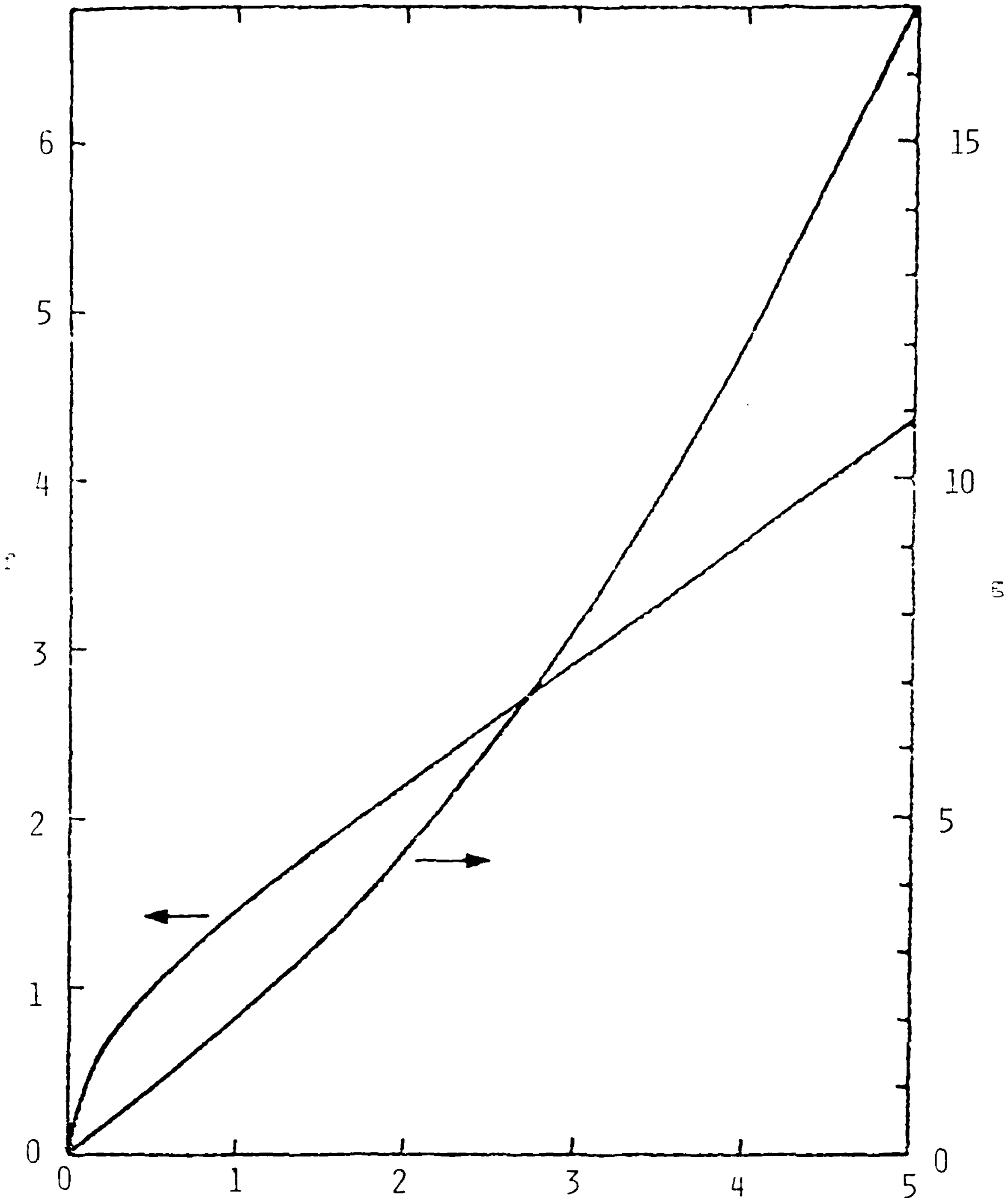


Figure 2.8. Values of f and g as a function of the depletion-layer aspect ratio b/a. f describes the magnitude of the singularity of the gate edge. g is related to the potential of the edge of the depletion layer (which equals the drain voltage) (11:967).

$$E(x) = -\frac{V_C f(b/a)}{\sqrt{ax}} . \qquad (2.11)$$

Once the electric field is defined, the ionization coefficient (α) can be determined as a function of the electric field. Therefore, the ionization integral (Equation 2.4) can be solved for the breakdown condition if the value of f(b/a) is known. Frensley (11) has performed these calculations; however, his relationship of the ionization coefficient to the electric field was not temperature dependent. In this research, a temperature dependent relationship is essential to show the changes of V_B with respect to life test temperatures. A temperature dependent form of the ionization coefficient has been developed by Crowell and Sze (12). They start with Baraff's generalized theory for all semiconductors which relates the ionization coefficient (α) to the electric field (E) using three parameters: ϵ_r, the Raman optical phonon energy; ϵ_i, the ionization energy; and λ_o, the carrier mean free path for optical phonon generation (12:242). The most appropriate ionization energy is one and one-half times the bandgap (12:242). The remaining parameters of Baraff's theory are modified. First, the average energy lost per collision ($<\epsilon_r>$) is substituted for the Raman optical phonon energy (ϵ_r). Secondly, a carrier mean free path for optical phonon generation that includes the effects of both optical phonon absorption as well as generation (λ) was substituted for λ_o. The calculation associated with these parameters is shown in Equation 2.12 (12:242):

$$\frac{\langle \epsilon_r \rangle}{\epsilon_r} = \tanh\,(\epsilon_r/2kT) = \frac{\lambda}{\lambda_o} \qquad (2.12)$$

where

ϵ_r = optical phonon energy (5.6×10^{-21} J for GaAs) (17:851)
k = Boltzmann's constant (J/^{o}K)
T = temperature (^{o}K)
λ_o = phonon mean free path (5.8×10^{-9} m for GaAs) (17:851).

With these refinements Crowell and Sze show that the ionization coefficient predicted by Baraff's theory can be approximated by:

$$\alpha = \frac{1}{\lambda}\,\mathrm{EXP}\left[\begin{array}{l}(11.5r^2 - 1.17r + 3.9 \times 10^{-4})z^2 \\ +(46r^2 - 11.9r + 1.75 \times 10^{-2})z \\ -757r^2 + 75.5r - 1.92\end{array}\right] \qquad (2.13)$$

where

$r = \langle \epsilon_r \rangle / \epsilon_i$
$z = \epsilon_i / qE\lambda$.

The errors in fitting Baraff's curves with this approximation are within ± 2% over the range of $0.01 < r < 0.06$ and $5 < z < 16$ (12:244). For GaAs the parameter 'r' decreases with temperature from 0.010 at 300 ^{o}K to 0.006 at 600 ^{o}K. These values are slightly out of the range that the accuracy of Equation 2.13 was verified for.

However, in examining Figure 2.9, which are the Baraff curves, it is easy to see that even though the curves diverge more as r decreases, they are still well-behaved. Since Equation 2.13 approximates the curves within ± 2% over a large range of 'r' values, its accuracy should still be sufficient over the range in question. With respect to the z-parameter, which is inversely proportional to the electric field, it is obvious in looking at Equation 2.11 that as x approaches 0 at the gate edge, E(x) approaches infinity, and therefore, z approaches 0. In practice, the electric field approaches infinity only in an idealized geometry with a perfectly sharp gate edge (11:966). If a more reasonable gate geometry with a radius of curvature of 100 Å is assumed, then an upper bound on the electric field of approximately 1.2×10^6 V/cm is established. Since the electric flux lines now radiate radially from the rounded gate edge, no singularity exists (22:172-177). In addition, since the flux lines are radial they can be viewed as emanating from the center of curvature, and Equation 2.11 can still be used to approximate the electric field but with the gate edge at $x = 100$ Å instead of $x = 0$. Under this assumption of gate curvature, $z > 5$ for all subsequent calculations of breakdown voltage. Finally, to establish an upper bound for the z-parameter, it is observed in Figure 2.9 that at higher r-values, α (since λ

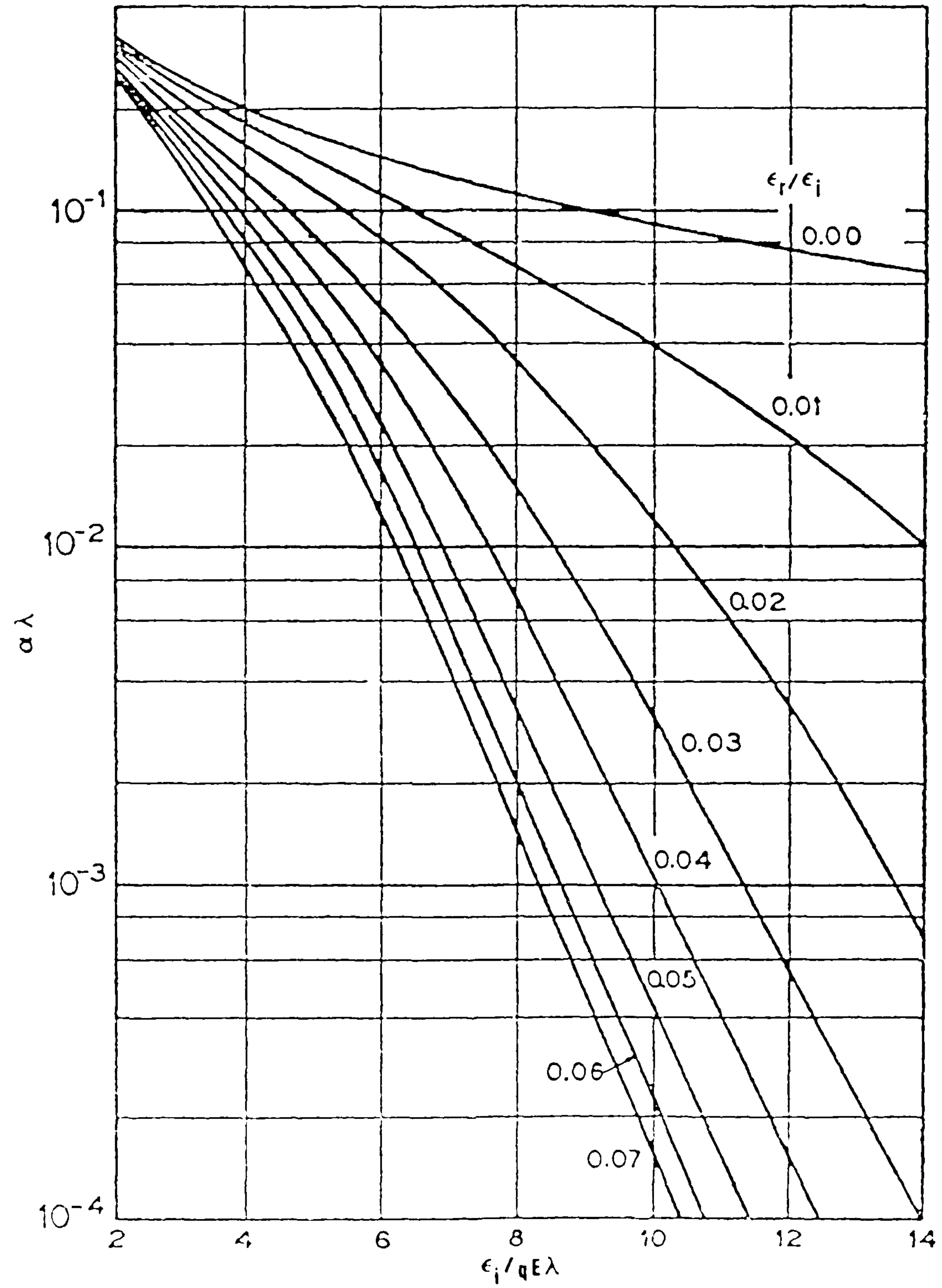
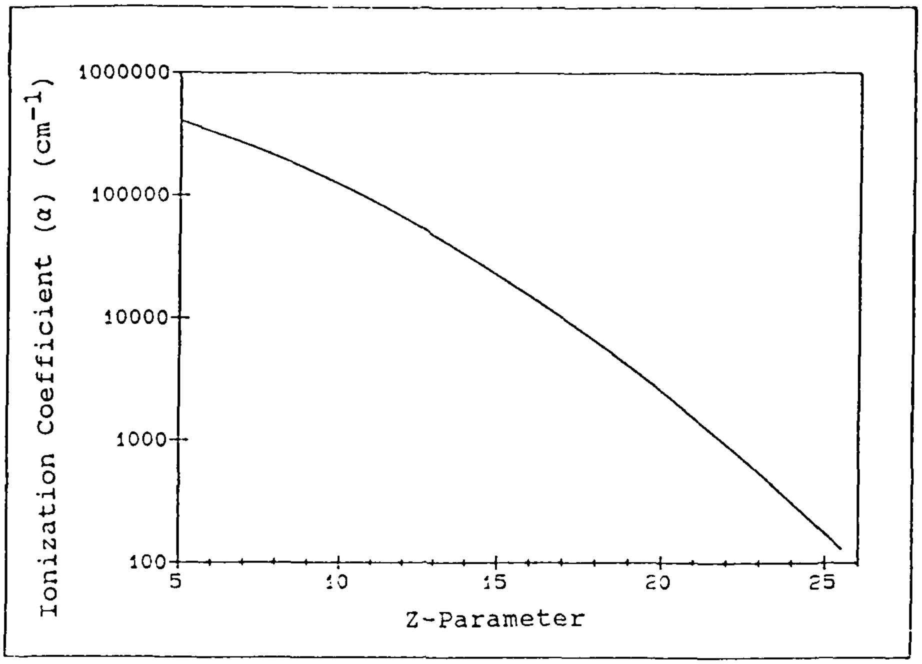


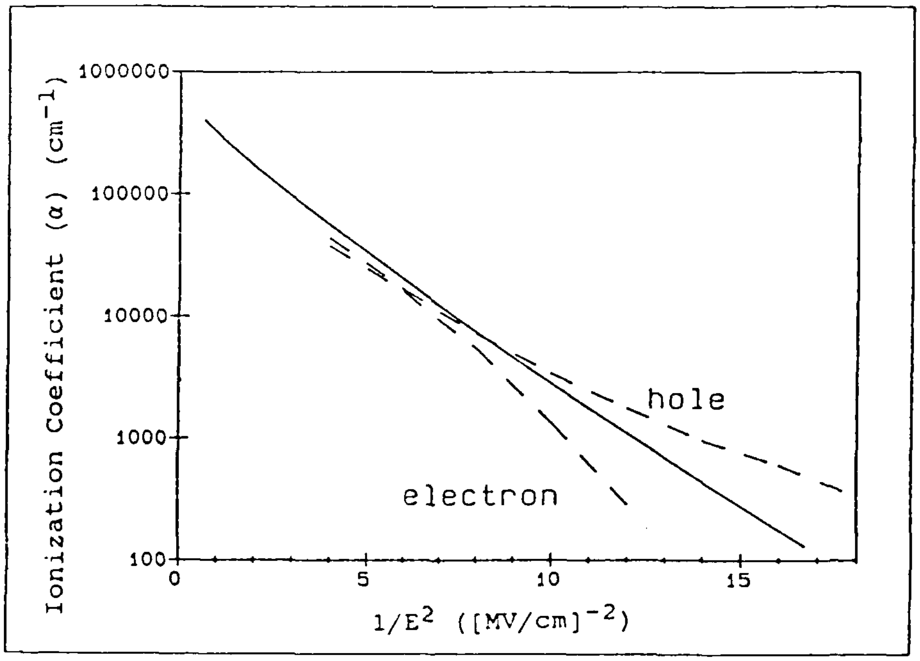
Figure 2.9. Baraff curves showing dependence of $\alpha\lambda$ on the z-parameter ($\epsilon_i/qE\lambda$) for various values of the r-parameter (ϵ_r/ϵ_i) (13:2513).

is a constant at any given temperature) varies over several orders of magnitude within a very small range of the z-parameter. Therefore, when integrating α to determine breakdown, only a small range of 'z' needs to be included. However, at small values of 'r', α varies much more slowly with respect to 'z', and a larger range of 'z' must be included in the integration to determine breakdown. At r = 0.010, as shown in Figure 10a, 'z' must be allowed to vary up to 24 to achieve the same (slightly over three orders of magnitude) variation in α which is characteristic of Figure 2.9 at higher values of 'r'. Since the accuracy of Equation 2.13 was not verified at these high values of 'z', some justification for utilizing this equation is required. Figure 10b shows published ionization coefficients for both holes and electrons in GaAs with Equation 2.13, for the same parameters as Figure 10a, superimposed over the data (23:1551). Since, for this research, the differences between the electron and hole ionization coefficients are neglected, Equation 2.13 is to represent an overall ionization coefficient. With this in mind, Figure 10b shows that Equation 2.13 correlates well with the published data at the higher values of 'z'. Substituting Equation 2.11 into Equation 2.13 yields the following ionization coefficient equation:

$$\alpha = 1/\lambda \ \mathrm{EXP}(K_1 x + K_2 \sqrt{x} + K_3) \qquad (2.14)$$



(a)



(b)

Figure 2.10. (a) Ionization coefficient (α), calculated from Equation 2.13 for GaAs at 300 °K, plotted against the z-parameter. (b) The same calculated ionization coefficient data compared to published ionization rates for GaAs (23:1551).

where

$$K_1 = \frac{a\epsilon_i^2}{\lambda^2 q^2 V_c^2 f^2(b/a)} \left[\frac{11.5<\epsilon_r>^2}{\epsilon_i^2} - \frac{1.17<\epsilon_r>}{\epsilon_i} + 3.9 \times 10^{-4} \right]$$

$$K_2 = \frac{\sqrt{a}\ \epsilon_i}{\lambda q V_c f(b/a)} \left[\frac{46<\epsilon_r>^2}{\epsilon_i^2} - \frac{11.9<\epsilon_r>}{\epsilon_i} + 1.75 \times 10^{-2} \right]$$

$$K_3 = -\frac{757<\epsilon_r>^2}{\epsilon_i^2} + \frac{75.5<\epsilon_r>}{\epsilon_i} - 1.92 \quad .$$

Substituting Equation 2.14 into Equation 2.4 yields the following ionization integral:

$$1/\lambda \ \mathrm{EXP}(K_3) \int_{10^{-3}}^{\infty} \mathrm{EXP}(K_1 x + K_2\sqrt{x}\,)\ dx = 1 \ . \qquad (2.15)$$

The lower limit of integration is changed from 0 to 100 Å to incorporate the effects of gate curvature. In addition, to include the entire depletion layer which has an undefined length, the upper limit of integration is change to infinity. This is possible because the ionization coefficient decreases dramatically with distance from the gate edge. Therefore, integration of its value beyond the depletion layer edge will not significantly effect the solution. Equation 2.15 can be solved for the value of f(b/a). Once f(b/a) is known, the value of g(b/a) can be determined from (11:967):

$$g(b/a) \approx 0.89 f^2(b/a) + 0.11 f(b/a) \ . \qquad (2.16)$$

Once g(b/a) is known, the breakdown voltage (V_B), which is the same as V_{DS} with zero gate bias, is determined by Equation 2.9.

Theoretical Prediction of the Variation of Avalanche Breakdown Activity with Temperature. With a model to predict V_B , a theoretical prediction of T_B (the percentage of time the device is in avalanche breakdown) can be made for the device under test at different temperatures and operating conditions. First, the device parameters of the MESFET under test are used to determine V_C. For the Fujitsu 7177-5, the active-channel depth (a) is 0.12 μ, and the doping profile in the channel is uniform with a concentration of 1.5 X 10^{17} cm^{-3} (18). From Equation 2.8, V_C for the test device equals 1.49 V. Secondly, the breakdown voltage can be determined from Equation 2.9 with the value of g(b/a) at breakdown. Iteratively solving Equation 2.15 by numerical methods for f(b/a) at breakdown, and using Equation 2.16 to determine the corresponding value of g(b/a), the theoretical breakdown voltage of the device under test over temperature was calculated. The results are shown in Figure 2.11. Next, V_M (the maximum rf drain voltage swing) must be related to an easily measurable test parameter. The simplest and most convenient measure of device rf output is the output power (P_{OUT}). P_{OUT} can be related to the rf voltage swing by the equation $P_{OUT} = 10 \text{ Log}_{10} (V_{OUT}^2/2R)$, where V_{OUT} is the

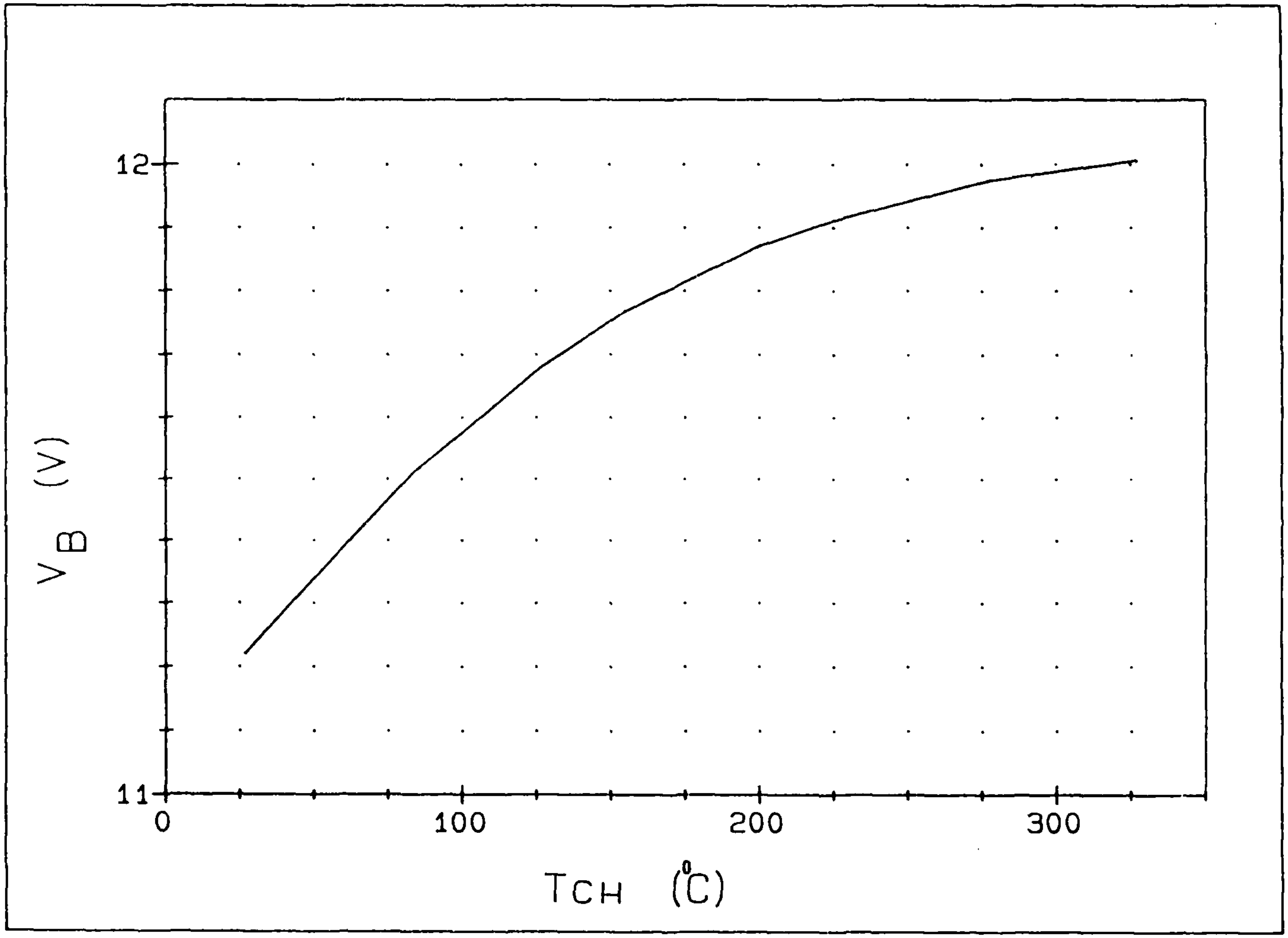


Figure 2.11. Calculated breakdown voltage (V_B) of the FLM 7177-5 versus channel temperature (T_{CH}).

peak voltage and R is the resistance driven by the device. For the standard test arrangement used in this experiment, R is assumed to be 50 ohms and represents an ideal transmission line. However, this situation exists at the output of the Fujitsu 7177-5, which is a internally matched pair of Fujitsu FLC 301 GaAs MESFETs (8:SEC II). Assuming the matching circuit has no power loss and is perfectly matched to the two internal FETs, then each of the FETs is supplying one half of the output power. Since a decrease of 3 dB represents a loss of one half of the power, $[10\text{Log}_{10} (V_{OUT}^2/2R) - 3] = 10\text{Log}_{10} (V_M^2/2R_M)$, where V_M is the rf voltage swing at the drain of one of the devices and R_M is the input resistance of the matching circuit. Solving for V_M yields: $V_M = [(V_{OUT}^2 R_M)/2R]^{-1/2}$. Observing that $V_{OUT}^2/2R$ is the output power (in watts) as shown above, V_M can be related to P_{OUT} by the equation: $V_M = \{R_M[10{*}{*}(P_{OUT}/10)]\}^{-1/2}$. Since the FLM 7177-5 is assumed to be perfectly internally matched, R_M is the same as the output resistance of one of the FLC 301s. The output resistance of one of the FETs in the FLM 7177-5, derived from the basic model parameters supplied by the vendor, is 6.8 ohms (19; 20). These model parameters are shown in Table 2.1. This resistance is calculated at ambient temperature, however, since the matching circuit is a completely passive network consisting of wires and metallization patterns, the temperature effects on R_M were

TABLE 2.1

FLC 301 GaAs MESFET BASIC MODEL PARAMETERS (19)

PARAMETER	VALUE
Magnitude of Transconductance at DC	0.680 S
Time Delay Associated with Transconductance	5.5 ps
Gate-to-Source Capacitance	9.2 pF
Channel Resistance	0.5 Ω
Drain-to-Gate Capacitance	0.48 pF
Drain-to-Source Capacitance	1.52 pF
Drain-to-Source Resistance	18.75 Ω
Series Gate Resistance	0.125 Ω
Series Gate Inductance	0.07 nH
Series Drain Resistance	0.3 Ω
Series Drain Inductance	0.07 nH
Series Source Resistance	0.3 Ω
Series Source Inductance	0.05 nH

considered negligible (20). Since this experiment is accomplished by controlling P_{IN} and $P_{OUT} = P_{IN} + GAIN$, by substituting into the above equation V_M can be related to P_{IN} by:

$$V_M = \sqrt{\{R_M[10**(P_{IN}+GAIN)/10]\}} \quad . \qquad (2.17)$$

Finally, the bias voltages, V_{GS} and V_{DS}, are test parameters directly controlled. Therefore, with the experimental measurement of the device gain with known values of P_{IN}, V_{GS}, V_{DS}, and T_{CH}, a theoretical prediction of T_B can be made using Equation 2.7. Unfortunately, this prediction can not be directly verified by measurement. However, two measurable parameters associated with the amount of time the device is in avalanche breakdown are the reverse gate current and light emission. Since the device's gate current in saturation is a combination of forward gate conduction and reverse gate current due to avalanche breakdown, it is difficult to isolate the component of gate current associated with avalanche breakdown. For this reason, light emission was chosen as a means to verify the theoretical prediction of the amount of time the device operates in avalanche breakdown.

Light Emission

Background. Under thermal-equilibrium conditions, the product of the electron and hole concentrations in any semiconductor must remain constant (21:142). While the thermal generation of electron-hole pairs is continually occurring, their recombination occurs at the same rate. This recombination process must release energy. The amount and type of energy released during recombination depends on the type of transition the electron makes to recombine with a hole in the band structure of the semiconductor. Figure 2.12 shows the basic classes of transitions that are possible in a semiconductor. The type 1 transitions (Figure 2.12) are called interband transitions because the electron drops from the conduction band to the valence band. There are two modes of interband transitions. The intrinsic mode transition releases energy corresponding very closely to the bandgap energy. The other higher-energy transition involves hot carriers. One source of hot carriers is avalanche multiplication. The type 2 transitions involve chemical impurities or physical defects with energy states located within the bandgap. There are four modes of these transitions; conduction band to acceptor, donor to valence band, donor to acceptor, and deep level transitions. Lastly, the type 3 transitions are intraband transitions involving hot carriers. These transition modes indicate the amount of energy released during the recombination process. The type of energy released is based on the fundamental band structure of the semiconductor. The band structures can be separated into two classes; indirect gap and direct gap semiconductors.

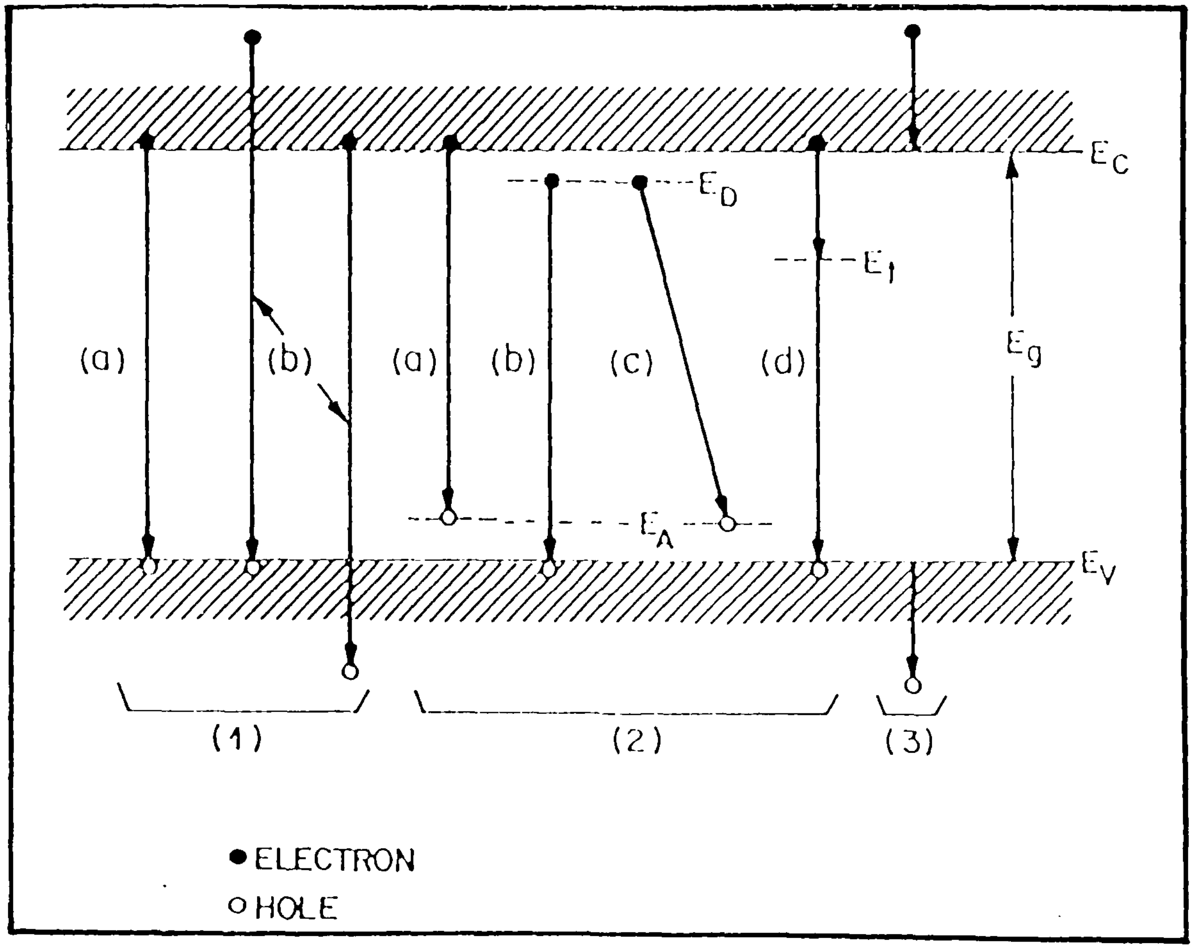


Figure 2.12. Basic transitions in a semiconductor. Type 1 transitions are interband transitions, either (a) intrinsic, with energy close to E_g or (b) higher-energy, hot carrier transitions. Type 2 transitions involve chemical impurities or defects and use this intermediate energy level in several modes of recombination. Type 3 transitions are intraband transitions involving hot carriers (17:684).

An indirect gap semiconductor is one in which the minimum energy bandgap (E_g) between the conduction and valance band is not at the same wave vector (21:144-145). Therefore, for an electron to make the minimum energy transition between bands, it would have to change momentum. This class of transitions are called indirect transitions and must involve collisions with the atoms of the crystal, transferring lattice vibrational energy or phonons.

Direct gap semiconductors have their minimum bandgap at the same wave vector and, therefore, can release the recombination energy without any momentum change (21:144-146). This direct transition may result solely in the release of a photon with energy equivalent to the energy change of the transition. As stated earlier, these generation-recombination transitions are occurring continuously but proceed at a net rate to maintain a constant number of carriers. If the carrier generation rate is increased above the thermal rate, then the recombination rate will correspondingly increase in an attempt to maintain the product of hole and electron concentrations constant. A portion of these recombination events will result in a photon that will be emitted rather than being reabsorbed by the semiconductor.

Light Emission from GaAs MESFETs. Applying this general background to GaAs MESFETs, it is convenient to show a relationship between light emission and avalanche breakdown. First, GaAs is a direct gap semiconductor which favors interband recombinations, and most of the energy is released as photons (21:143,146). Secondly, the avalanche multiplication processes, as discussed earlier, is a prodigious source of electron-hole pairs. These electron-hole pairs greatly disturb the equilibrium carrier concentration and promote large recombination rates. Without trying to determine the exact relationship, it is convenient to observe that the recombination rate and, therefore, the rate of photon emission is proportional to the carrier generation rate (17:685). Relating this information to the idealized GaAs MESFET signal shown in Figure 2.6, the overall average carrier generation rate is the number of carriers generated during avalanche breakdown divided by the period of the signal. The number of carriers generated during avalanche breakdown (N_B) can be expressed as the average carrier-concentration generation rate during breakdown (G_B) multiplied by the amount of time the device is in breakdown:

$$N_B = G_B\ T_B\ (1/freq)\ . \qquad (2.18)$$

Thus the overall average carrier-concentration generation rate, G, is then $N_B/(1/freq)$ or:

$$G = G_B\ T_B\ . \qquad (2.19)$$

The overall photon emission rate, or light current induced in the photomultiplier tube (I_{LE}), is proportional to G. Since, a theoretical model for determining T_B at different temperatures has already been shown, only G_B, the average generation rate during breakdown, needs to be determined to predict variations in light emissions with temperature.

Prediction of Light Emission Variations with Temperature. As shown above, the amount of light emitted is proportional to the product of the average generation rate of carriers during avalanche breakdown (G_B), and the percentage of time the device is in avalanche breakdown (T_B). A model to predict T_B has already been developed in a previous section (Gate-to-Drain Breakdown in GaAs MESFETs). This section will discuss a theoretical model for the variation of light emission with temperature by first developing a model for the change of the average carrier-concentration generation rate with temperature. Since the carrier-concentration generation rate from impact ionization is very large compared to thermal generation, only the avalanche induced carrier-concentration generation rate needs to be considered. The carrier-concentration generation rate from impact ionization is given by (17:45):

$$G_B = \alpha_n n v_n + \alpha_p p v_p \qquad (2.20)$$

where

α_n = the electron ionization coefficient (cm^{-1})
α_p = the hole ionization coefficient (cm^{-1})

n = the electron concentration (cm^{-3})
p = the hole concentration (cm^{-3})
v_n = the electron drift velocity (cm/s)
v_p = the hole drift velocity (cm/s) .

Equation 2.20 can be reduced using some common simplifying assumptions. The first of these is the previous assumption that the electron and hole ionization coefficients are equal. The second is that at the extremely high fields associated with avalanche breakdown the carrier drift velocities approximate their saturation velocity. The last assumption is that at high doping levels the carrier concentration can be represented by the doping level. Using these assumptions, Equation 2.20 reduces to:

$$G_B = \bar{\alpha} v_s N \tag{2.21}$$

where

$\bar{\alpha}$ = the average ionization coefficient in the breakdown region (cm^{-1})
v_s = the saturation velocity (cm/s)
N = the doping concentration (cm^{-3}) .

The saturation velocity for GaAs is approximately 6×10^6 cm/s at 300 ^{o}K and varies as the inverse of temperature (17:45-46). Therefore, the only unknown factor for calculating G_B is the average ionization coefficient in the breakdown region. To determine the average ionization coefficient, the avalanche breakdown region can be analyzed in the same way as the avalanche region of an IMPATT diode. The avalanche breakdown condition, as shown in Equation 2.4, is given by integrating the ionization coefficient over the entire depletion region. However, since the ionization coefficient is extremely dependent on the electric field, and the electric field, as defined by Equation 2.11, decreases dramatically with distance from the gate edge, the ionization region is highly localized in the area at the gate's edge. The avalanche region can be defined as the region from the gate's edge to a distance x_A, where x_A is the width of the avalanche region. The value of x_A is determined by iteratively calculating (17:573):

$$\int_{10^{-8}}^{x_A} \alpha \, dx = 0.95 \ . \tag{2.22}$$

For a GaAs MESFET, the ionization coefficient at breakdown is defined by Equation 2.14 calculated at the breakdown value of f(b/a). Once x_A is determined, an average ionization coefficient in the avalanche region can be defined as the constant value of α required to satisfy Equation 2.22. This average value is valid at the condition of breakdown (when the ionization integral equals unity). For the dc case, the ionization integral can never exceed unity and, therefore, the equation is valid whenever the device is in breakdown. However, the ionization integral may exceed unity with an rf signal applied to the device. Therefore, any rapidly varying electric field in excess of the critical field required for breakdown will increase the average ionization coefficient in the avalanche region. To account for this effect, an average f(b/a) during avalanche breakdown can be used to derive an ionization coefficient using Equation 2.14. The average value of this ionization coefficient in the avalanche region (from the gate's edge to x_A as defined above) is the average ionization coefficient used in Equation 2.21. Since the value of the function f(b/a) is related to the drain voltage, the average value of f(b/a) during breakdown can be calculated from the average drain voltage during breakdown using Equations 2.9 and 2.16. Lastly, x_A varies with changes in temperature since α is temperature dependent. To include this effect in the prediction of light emissions, the carrier-concentration generation rate is multiplied by the avalanche-region width. This result yields Equation 2.23 as the theoretical prediction of light emissions:

$$I_{LE} = C_1 G_B x_A T_B \tag{2.23}$$

where

I_{LE} = light induced photomultiplier current (nA)
C_1 = constant of proportionality -- empirically determined (nA-s-cm^2)
G_B = average carrier-concentration generation rate in breakdown (cm^{-3}-s^{-1})
T_B = percentage of time in breakdown
x_A = width of the avalanche region (cm) .

Summary

The first portion of this chapter described the theory of reliability testing as applied to semiconductor devices, and specifically, GaAs MESFETs. This discussion addressed the assumptions inherent in extrapolating accelerated temperature life test data to normal operating temperatures. The critical assumptions are that all failure mechanisms are accelerated by temperature according to the Arrhenius relationship, and that the same failure mechanism(s) is the dominant cause of failures spanning the whole range of temperatures. These assumptions have not been validated for GaAs MESFETs in general, or for the specific Fujitsu FLM 7177-5 being tested. Since avalanche breakdown occurs any time, a GaAs MESFET is operating in saturation, it is of particular interest to validate these assumptions for that failure mechanism. The second section of this chapter developed a theoretical method to predict the variation of avalanche breakdown activity with respect to temperature in a GaAs MESFET. This model predicts from basic device and test parameters the percentage of time the device is in avalanche breakdown during large-signal sine wave operation. This model will be used to check the assumption, for avalanche breakdown only, that all failure mechanisms are accelerated by temperature according to the Arrhenius relationship. Since the percentage of time that a GaAs MESFET is in avalanche breakdown is not directly measurable, the final section of this chapter derived a corresponding model to predict the variance in the amount of light emissions as a function of temperature. This analysis provides a quantitative method for experimentally verifying the variations in avalanche breakdown activity. Chapter III will describe the experimental configuration and procedures used to control and measure the basic parameters necessary to predict avalanche breakdown activity and verify the predictions with light emission measurements.

III. Experimental Design

Introduction

To validate the theoretical model of avalanche multiplication variation with temperature, experimental measurements of light emissions from the device at various temperatures and operating parameters was required. First, a test configuration with the capability of making these light emission measurements was necessary. The test configuration must be able to monitor the light emissions while controlling the rf input power (P_{IN}), dc bias voltage levels (V_{DS} and V_{GS}), and baseplate temperature of the device (T_{BP}). In addition, the rf output power (P_{OUT}) and bias current levels (I_{DS} and I_{GS}) must be measured. The output power level is necessary to calculate the device gain which is used in Equation 2.17 to determine the maximum rf drain voltage swing. Also, the device power transfer curve (P_{OUT} versus P_{IN}) is a desirable indication of general device performance during testing. The bias current levels are used in conjunction with the bias voltage levels and the rf input and output power levels to determine the total power dissipation of the device. This power dissipation is required to translate the baseplate temperature (T_{BP}) into channel temperature (T_{CH}) for comparison to the theoretical predictions. The process of calculating T_{CH} from T_{BP} will be described in Chapter IV.

The second requisite in collecting the required data is a comprehensive experimental test program based on the validation objective. This chapter describes the experimental equipment configuration and test program used to collect the data necessary to validate the theory presented in Chapter II.

Equipment Configuration

General. The laboratory equipment configuration to facilitate the required measurements over the temperature range of interest had to incorporate a thermally isolated device test fixture. This isolation was necessary to allow accurate (within ± 2 °C) temperature control of the device under test, while permitting the remainder of the instruments to be operated at normal laboratory conditions. The instrumental test configuration was designed to control P_{IN}, V_{DS}, and V_{GS}, while accurately measuring P_{OUT}, I_{DS}, I_{GS}, T_{BP} and light emissions. The light emissions were monitored by recording the light induced current (I_{LE}) on a photomultiplier tube. This arrangement also provides an rf tuning capability on both the input and output of the device to assure consistent and maximum power transfer.

High-Temperature Test Fixture. The high-temperature test fixture (HTTF) provides a thermally isolated, temperature controlled and light-tight environment for the device under test. The fixture is a metal enclosure approximately

9.5" W X 3.0" H X 6.0" D. Figure 3.1 shows the inside of the enclosure which contains three major assemblies:

1. The temperature controlled and thermally isolated mounting block.
2. The rf input and output circuitry.
3. The heat sink assembly.

Also considered part of the HTTF is the temperature controller hardware exterior to the enclosure itself.

The temperature controlled and thermally isolated mounting block is the heart of the HTTF. Its design and the design of the rf circuitry are based on the designs used by JPL, for their accelerated temperature life tests. The copper mounting block, item A in Figure 3.1, provides a small mounting surface for the device under test in the center of the HTTF enclosure. The remainder of the copper extends downward into the enclosure where a 75W heater and thermocouple (TC1) are mounted. This heater and TC1 are connected through the enclosure with penetration pins at location B in Figure 3.1. Connection to external hardware is used to control the temperature of the block and, therefore, the device's baseplate temperature (T_{BP}). Since, there are thermal gradients across the mounting block during device operation, a second thermocouple (TC2) is mounted on the upper surface of the device's baseplate to directly measure T_{BP}.

The rf circuitry, shown in Figure 3.1, consists of two polytetrafluoroethylene laminate (OAK 602) boards with

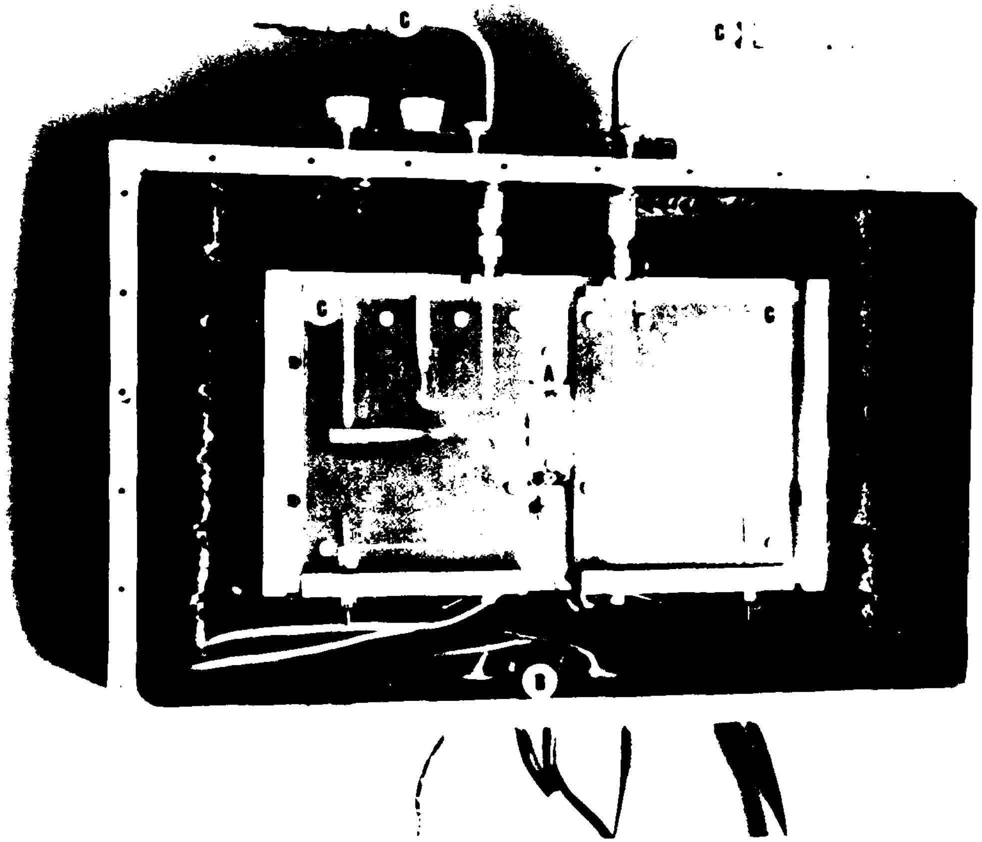


Figure 3.1. Photograph of the inside of the high-temperature test fixture. Highlighted in the photograph are the: A. top of the copper mounting block with the device under test. B. penetration pins for heater control circuitry. C. rf circuitry including the gate and drain circuit boards and their corresponding semi-rigid coax cables.

50 ohm aluminum metallization paths from the device's gate and drain leads to openings in the back of the HTTF enclosure. At this point, the metallization paths are connected to semi-rigid coax leads which are approximately 4" long. The circuit boards are attached to brass holders in the fixture with the ground plane of the boards electrically connected to the respective holders. These holders are mounted in the fixture such that they can accommodate different device package sizes. By sliding the boards closer together, the fixture can accommodate smaller packages, and by moving them farther a part, larger packages can be evaluated. The board and its holder's only contact with the high temperature mounting block is the device itself. The edge of the circuit board and holder intimately contacts the edge of the device package, such that the holder, and, therefore, the board's ground plane, contacts the device's baseplate (source). To minimize thermal conduction from the device to the board and holder assembly, a one-square inch section of the holder surrounding the device's area of contact was fabricated from stainless steel (type 303). The stainless steel is much less thermally conductive than brass. Assuming that the thermal conductivity of these materials is linear in the range of temperature from ambient to the highest baseplate (T_{BP}) test temperature of 163 °C, stainless steel has a thermal conductivity of 8.08 Btu/h/ft^2/°F/ft

compared to brass which has a thermal conductivity of 61.0 Btu/h/ft^2/^{o}F/ft (24:SEC 4,60-61). In addition, the actual contact area to the device was limited to a 0.010 square inch tab on the stainless steel insert. The only other thermal contact with the high temperature block is, of course, the gate and drain leads. However, these leads are connected with gold ribbons which, because of their small size, do not provide a very large thermal conduction path.

The heat sink assembly was a required modification. When the HTTF was first used, with the heat dissipated from the device, the lowest controllable T_{BP} was approximately 110 ^{o}C. Therefore, to accomplish measurements in the normal operating temperature range of the device, a method to selectively heat sink the mounting block was required. The method chosen was spring loaded copper rods. The heat sink assembly consists of three spring loaded 7/32" diameter copper rods mounted on the bottom of the HTTF enclosure. Figure 3.2, a bottom view of the HTTF, shows the tab on the external end of each rod. These tabs, as shown in Figure 3.2, can be positioned to maintain an air gap between the tip of the rods and the mounting block, leaving the mounting block thermally isolated. Alternatively, the tabs can be turned, allowing the rods to press with the force of the springs against the bottom of

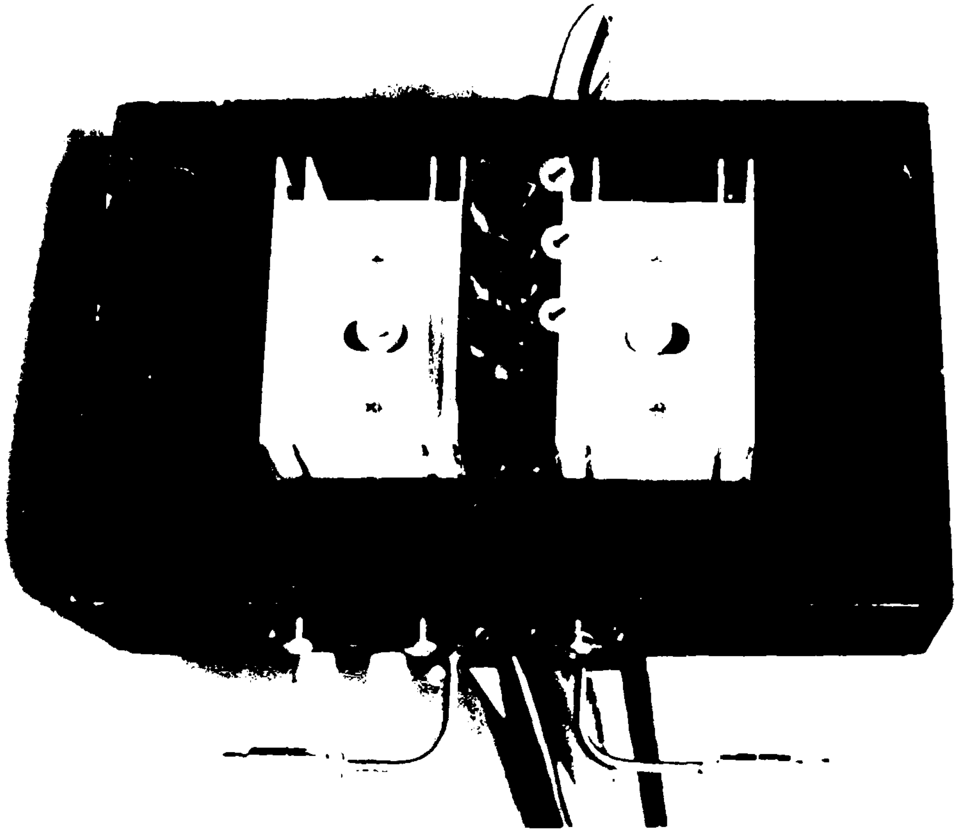


Figure 3.2. Photograph of the bottom of the high-temperature test fixture. Highlighted are the three external tabs of the heat sink assembly. They are shown in the thermally isolated position. Turning the tabs vertically provides a heat sink by allowing the tabs to drop into the slot, and thereby permit the internal copper rods to contact the mounting block.

the mounting block. With the mounting block heat sinked to the HTTF enclosure, the block temperature can be controlled to approximately 45 °C, which is well within even the most restrictive device operating range of -24 °C to +61 °C (30:6-7).

The temperature controller hardware consists of an Omega Engineering Inc. temperature controller and a General Radio Company variac. The temperature controller is a single unit that monitors TC1 relative to a variable set point, and closes a relay which connects 120 VAC to the 75 W heater when TC1 falls below the set point. Since TC1 and the heater are not mounted in exactly the same spot in the block, there is thermal lag. The heater will put more heat than necessary into the system because TC1 has not yet reached the set point due to the time needed for thermal diffusion through the block. This effect exhibits itself as a temperature overshoot of approximately 10 °C. To help minimize this temperature fluctuation, a variac was put in line between the controller and the heater. This allows the voltage to the heater and, therefore, the wattage of the heater to be selectable. When operating at lower temperatures, this enhancement limits the heater wattage and hence, the overshoot. At higher temperatures, a larger wattage setting can be selected to counteract the increasing thermal dissipation from the block.

Instrumental Test Configuration. The instrumental test configuration was designed to control P_{IN}, V_{DS}, and V_{GS} while accurately measuring P_{OUT}, I_{DS}, I_{GS}, I_{LE}, and T_{BP}. The arrangement also provides an rf tuning capability on both the input and output of the device to assure consistent and maximum power transfer. Figure 3.3 is a picture of the test arrangement, while Figure 3.4 schematically depicts the test configuration. This section will describe this arrangement from the perspective of three functional parts:

1. dc bias control, dc bias measurement, and T_{BP} measurement.
2. rf control and measurement.
3. I_{LE} measurement.

The dc bias control, dc bias measurement, and T_{BP} measurement portion of the instrumental configuration performs three functions. First, it controls V_{DS} and V_{GS}. Second, it measures I_{DS} and I_{GS}. Third, it measures T_{BP}. A critical element of this portion of the instrumental configuration is the FET Power Supply. The Aerospace Corporation designed the FET power supply. The supply provides adjustable V_{DS} and V_{GS} sources while featuring automatic adjustable cut-off limits for over-voltage and over-current conditions. The unit digitally displays the values of V_{DS}, V_{GS}, I_{DS}, and I_{GS}. The current values are read directly from these displays. However, with the line losses between the supply and the bias networks, where the

Figure 3.3. Photograph of the instrumental test configuration. Major elements are: A. FET power supply. B. digital thermometer. C. signal-source. D. variable attenuators. E. Travelling Wave Tube Amplifier. F. dual directional couplers. G. tuners. H. high-temperature test fixture. I. photomultiplier tube. J. photomultiplier tube power supply. K. micro volt-ammeter.

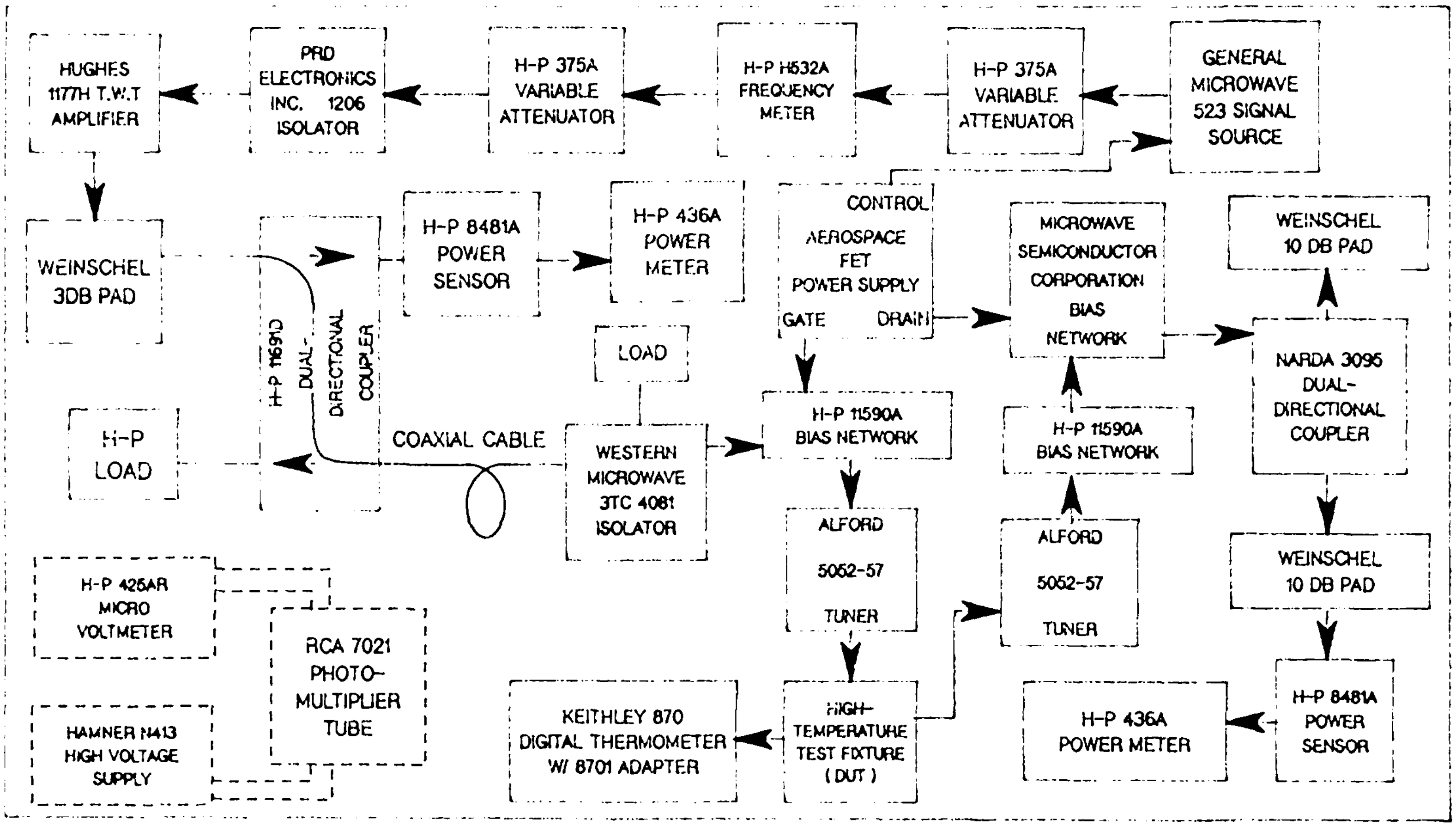


Figure 3.4. Schematic of the instrumental test configuration.

bias voltages are combined with the rf signal and applied to the device, the voltage values displayed on the supply are higher than those actually applied to the device. Therefore, voltmeters are attached to both Hewlett-Packard bias networks to monitor the actual values of V_{DS} and V_{GS}. Because I_{DS} is approximately 1.5 A for this device, the Hewlett-Packard bias network is not adequate to supply the drain bias, but is used to measure V_{DS}. To apply the drain bias, a specially designed Microwave Semiconductor Corporation high-current bias network is used. Lastly, T_{BP} is directly measured using a Keithly digital thermometer from TC2 in the HTTF.

The rf control and measurement portion of the instrumental configuration is most easily explained by following the signal path through the arrangement. The General Microwave signal-source (Figure 3.4) provides the 7.30 GHz test signal. The external control port on the signal-source was connected to the FET power supply control output. In this way, if for any reason the power supply was disabled, the rf signal generator would also turn off. The rf signal then passes through two Hewlett-Packard variable attenuators, a Hewlett-Packard frequency meter, and a PRD Electronics, Inc. isolator. The variable attenuators were used to adjust the P_{IN} levels utilized in the tests. The rf signal is then amplified, using a Hughes Travelling Wave Tube Amplifier, and routed through a

Weinschel 3 dB pad to a Hewlett-Packard dual-directional coupler which provides two outputs. One output goes to a Hewlett-Packard power sensor and Hewlett-Packard power meter that is used to measure the power at this point in the circuitry. A calibration factor is used to adjust this measured value to reflect the actual input power delivered to the device. How this calibration factor was determined will be explained later in this section. The other output of the coupler is the signal path to the HTTF and the device under test. This signal is passed through a Western Microwave isolator to assure there is no interaction between the measured source and the Alford tuner which is used to assure maximum power transfer into the HTTF. However, prior to the Alford tuner is the Hewlett-Packard bias network where the gate bias is applied to the device under test. After the tuner, the signal passes into the HTTF's semi-rigid coax gate line and passes through the HTTF and the device under test (DUT), and comes out through the semi-rigid coax drain line. Another Alford tuner was used at this point to assure maximum power transfer out of the HTTF. Next, the signal passes through both the Hewlett-Packard bias network and the Microwave Semiconductor Corporation high-current bias network. The Hewlett-Packard bias network is used to monitor the drain bias while the Microwave Semiconductor Corporation high-current bias network applies the drain bias. After the bias networks, the signal is injected into the Narda coupler. One of the two outputs of this coupler is routed through a Weinschel 10 dB pad to a port that was used for an optional connection to a spectrum analyzer (not shown in Figure 3.4), which was used to examine the output to assure the device was not in oscillation. The other output of the Narda coupler was routed to a Weinschel 10 dB pad and then to a Hewlett-Packard power sensor and a Hewlett-Packard power meter. A calibration factor was used to adjust this measured value to reflect the output power at the device.

The calibration factors for adjusting the input and output power measurements to reflect the actual power at the device were measured before the device was mounted in the HTTF. Both the input and output powers are monitored by meters at the respective dual-directional couplers. Therefore, changes (adjustments or unit replacements) to the instrumental arrangement external to the signal path between the two dual-directional couplers do not effect the power measurement accuracy of the test configuration. Figure 3.5 shows a schematic of the calibrated portion of the test configuration (from the input dual-directional coupler to the output dual-directional coupler). Once this test configuration was established it was not disturbed during the data collection. The calibration factors are the offsets in relative attenuation between the signal path

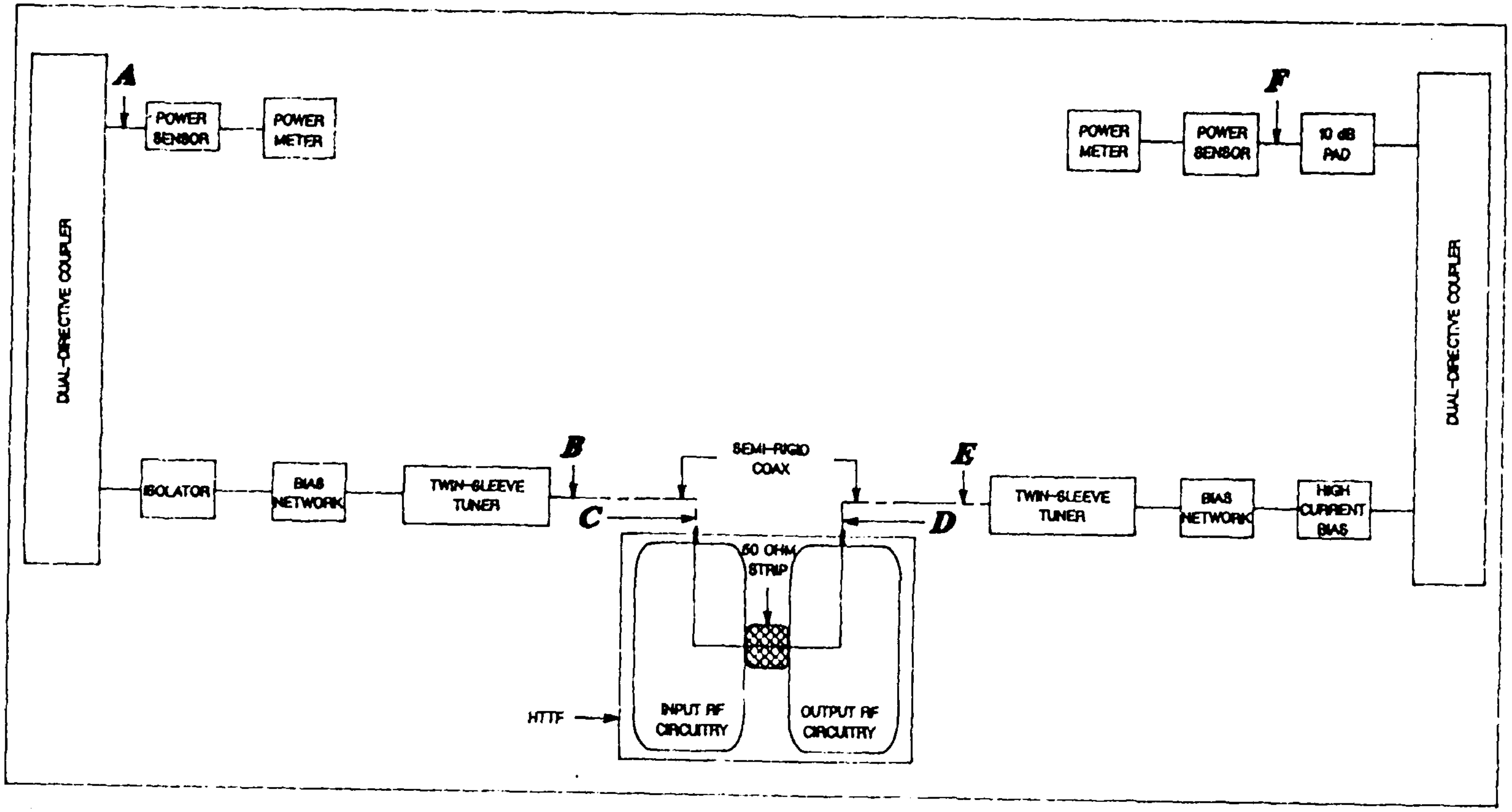


Figure 3.5. Schematic of the calibrated portion of the instrumental test configuration.

to the power sensor measuring input or output power and the device. Three significant contributions to these factors were measured. Referring to Figure 3.5 these contributions were: the HTTF rf circuitry losses between the device and the connection to the semi-rigid coax (C-D, 1/2 for the input circuitry and 1/2 for the output circuitry); the semi-rigid coax loss (B-C and D-E); and the offset in power of the test arrangement between the power sensor and the connection point to the semi-rigid coax (A-B and E-F). The rf circuitry and coax losses were measured using a Hewlett-Packard model 8620C sweep oscillator in conjunction with a Precision Microwave Inc. model 1038 scaler analyzer, which measures delta dB from an established reference level with respect to the actual measured value. The oscillator was set to sweep from 6.00 GHz to 8.00 GHz and all the test cables were calibrated to establish the reference level. All of the losses were recorded at the test frequency of 7.30 GHz. With a 50 ohm strip installed in the HTTF instead of a device, the total losses of the HTTF, including the input and output semi-rigid coax leads were measured (B-E in Figure 3.5). Next the losses of both coax leads, coupled end-to-end, were measured. By subtracting the losses in the leads from those of the total HTTF, the loss associated with the rf circuitry was determined to be 1.70 dB (C-D in Figure 3.5). At this point, it was assumed that the losses in the rf circuitry were uniformly distributed between the input and output circuitry. This was necessary, since individual measurements could not be made, to allow the losses to be allocated between the input and output circuitry. Therefore, the rf input circuitry loss or the rf output circuitry loss equaled 0.85 dB. Finally, each of the semi-rigid coax leads were measured separately to determine their losses. The input coax loss was 0.15 dB (B-C in Figure 3.5). The output coax loss was 0.05 dB (D-E in Figure 3.5). To measure the difference in relative attenuation between the path to the input power sensor and the connection to the input semi-rigid coax, the output power meter was connected to the output of the gate tuner (at point B in Figure 3.5) in place of the input's semi-rigid coax. Therefore, this power meter would read the input power to the HTTF. It was assumed, since the device under test would be tuned for maximum output power, that the connection between the test configuration and the HTTF would, therefore, be tuned for maximum power transfer. Hence, to make the relative attenuation measurements, the gate tuner was tuned for maximum power transfer to the output power meter. The value of this offset was 17.50 dB (A-B in Figure 3.5). To measure the attenuation in the path to the output power sensor from the output's semi-rigid coax, the two tuners were coupled together, end-to-end, at this same interface. Examining Figure 3.5, this was accomplished by connecting point B to point E.

Since the input's relative attenuation factor was already known, the power level at this interface relative to the drain tuner (the normal interface to the output semi-rigid coax) could be calculated. Then by tuning both tuners for maximum power transfer, the output power attenuation factor was determined to be 11.25 dB (E-F in Figure 3.5). With these measurements the input calibration factor was 16.50 dB, and the corresponding output calibration factor was 12.15 dB. Table 3.1 presents the individual components of these factors. Each of these calibration measurements were performed once; no attempt was made to collect a statistical average calibration factor to account for variations in connector losses associated with reconnecting the test configuration after calibration. However, the objective of this research is to measure variations in device parameters at different input powers and temperatures. Since the calibrated portion of the test configuration was not disturbed during data collection, any small variations in connector losses became a bias for all measurements and did not effect the measured variation in power levels. These instrumental test configuration calibration factors were used to convert all measured rf power readings to power levels at the device itself. The Hewlett-Packard power sensors and meters have a self-calibration mode which was used prior to each days testing. These instruments have a drift specification of -50 dBm/h

TABLE 3.1

CALIBRATION FACTORS

SEGMENT	P_{IN} FACTOR (dB)	P_{OUT} FACTOR (dB)
Input Offset (A-B)	17.50	
Output Offset (E-F)		(11.25)
Input Semi-Rigid Coax Loss (B-C)	(0.15)	
Output Semi-Rigid Coax Loss (D-E)		(0.05)
HTTF RF Circuitry Loss (C-D, split between input and output)	(0.85)	(0.85)
Total	16.50	(12.15)

NOTE:

ALPHABETIC SEGMENT DESIGNATORS REFER TO FIGURE 3.5

P_{IN} = METER READING + CALIBRATION FACTOR

P_{OUT} = METER READING - CALIBRATION FACTOR after warm-up (31:SEC 1,2). Since these instruments are left on continuously, the 24 h warm-up period was met for all testing and drift was considered insignificant at the power levels recorded. Lastly, care was taken to assure the instruments were configured properly including the correct meter calibration factor settings for the sensors that were used.

The light induced current (I_{LE}) measurement portion of the instrumental test configuration consists of a photomultiplier tube, a power supply for this tube, and a precision ammeter to measure the tube's output current (I_{LE}). These electrical components are shown in Figure 3.4. The photomultiplier tube utilized was an RCA-7102 which is a 10-stage tube intended for use in the visible to near infrared spectrum. The tube, mounted in a special fixture, attaches to a flange on the top cover of the HTTF. This flange opens into the HTTF enclosure directly over the device under test. Once the photomultiplier tube's fixture is attached to the HTTF the entire assembly is light tight. The power supply for the photomultiplier tube was set at 1200 V. The output of the tube was measured with a Hewlett-Packard dc micro volt-ammeter which has the capability of resolving pico-amperes. Figure 3.6 is a photograph of two FLM 7177-5 MESFETs (the same design as the device under test). One of the devices is shown intact, with the package lid in place. The other device

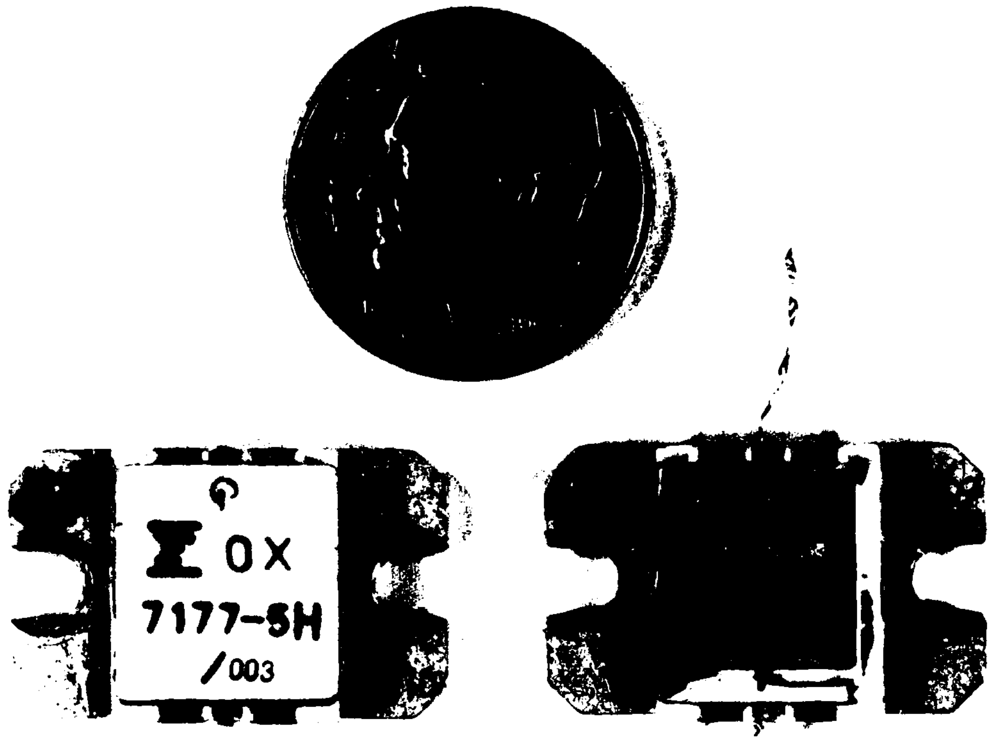


Figure 3.6. Photograph of two Fujitsu FLM 7177-5 GaAs MESFETS. The device on the left is an operational device of the same design as the device under test. The device on the right was destructively delidded to show internal layout.

was destructively de-lidded to display the internal construction of the device. Figure 3.7 depicts the optical collection path from the device under test to the photomultiplier tube. A portion of the light emitted by the two FLC 301 MESFET chips impinges on the package lid. The package lid is constructed of alumina (aluminum oxide- - Al_2O_3) (18). Based on empirical transmittance data above 1 μm and absorbtion data below 1 μm, alumina has relatively constant transmittance characteristics over the entire near infra-red spectrum (0.720 - 1.400 μm) (28). This assessment assumes that scattering, cause by material pore sizes near the wave-length of the incident illumination, is not significant in this frequency range (28). Referring to Figure 2.12, the intrinsic, interband transitions may release photons with energies near the bandgap energy (E_g). For GaAs, E_g is 1.42 eV at room temperature and varies with temperature according to: $E_g(T) = 1.52 - [(5.4 \times 10^{-4}) \times T^2/(T + 204)]$ (16:13). The frequency associated with these intrinsic energy photons is derived from: $\nu = E_g/h$ where ν is the frequency of the light emitted and h is Planck's constant (21:53). Figure 3.8 presents the spectral transmittance characteristics of aluminum oxide. The wavelength range of intrinsic emissions from GaAs at 85 ^{o}C to 225 ^{o}C is also shown in Figure 3.8. This is the range of channel temperatures employed in this research; the calculation of these channel temperatures from the experimental baseplate

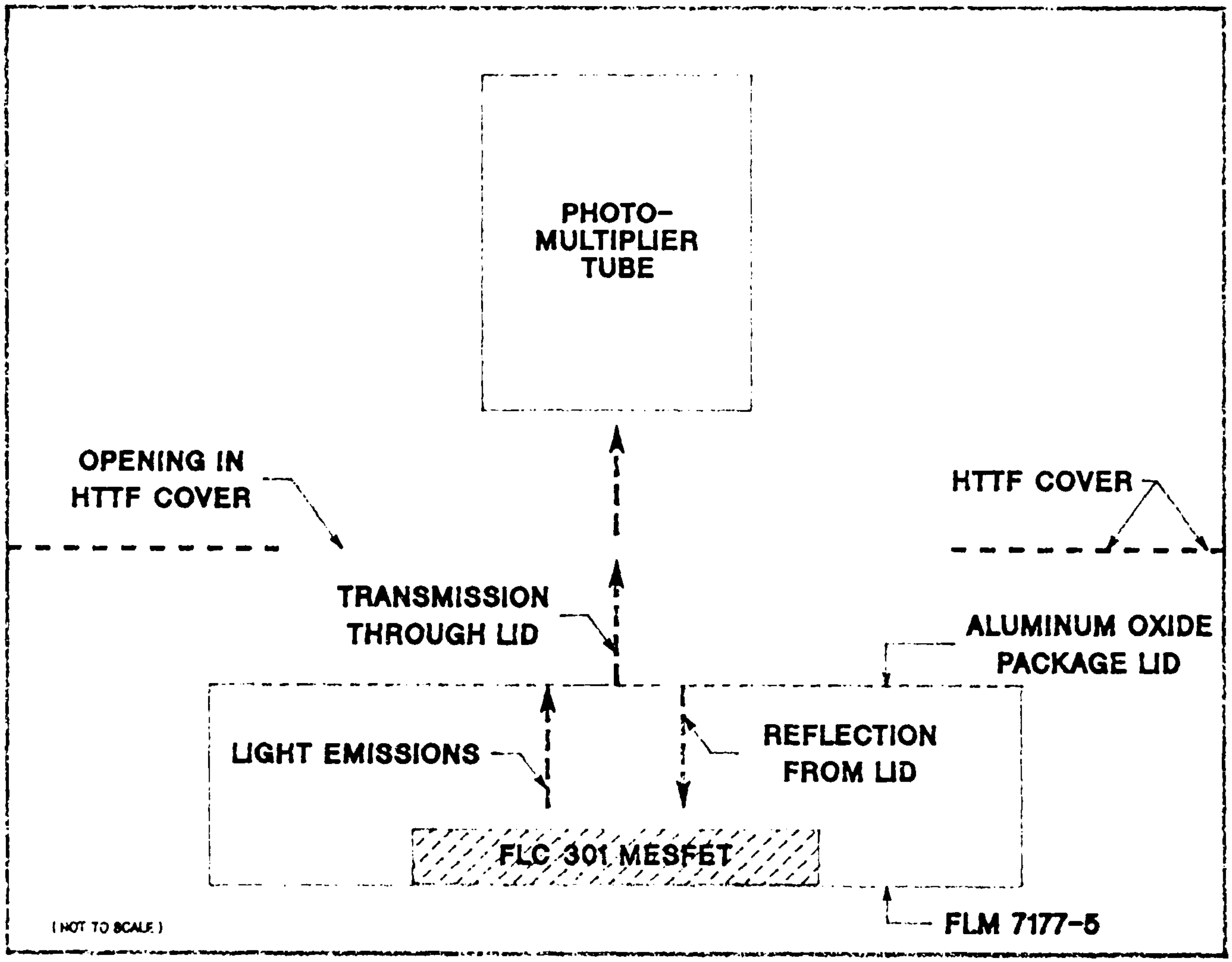
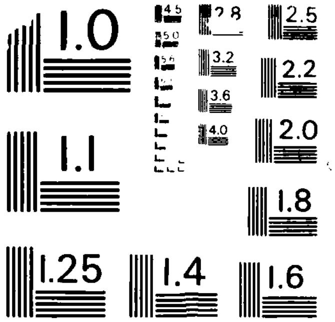


Figure 3.7. Diagram of the optical collection path.

AD-A189 634 EXAMINATION OF TEMPERATURE EFFECTS ON GATE-TO-DRAIN 2/2
AVALANCHE BREAKDOWN I..(U) AIR FORCE INST OF TECH
WRIGHT-PATTERSON AFB OH SCHOOL OF ENGI.. R E ROBB
UNCLASSIFIED DEC 87 AFIT/GE/ENG/87D-73 F/G 9/1 NL



MICROCOPY RESOLUTION TEST CHART
NATIONAL BUREAU OF STANDARDS-1963-A

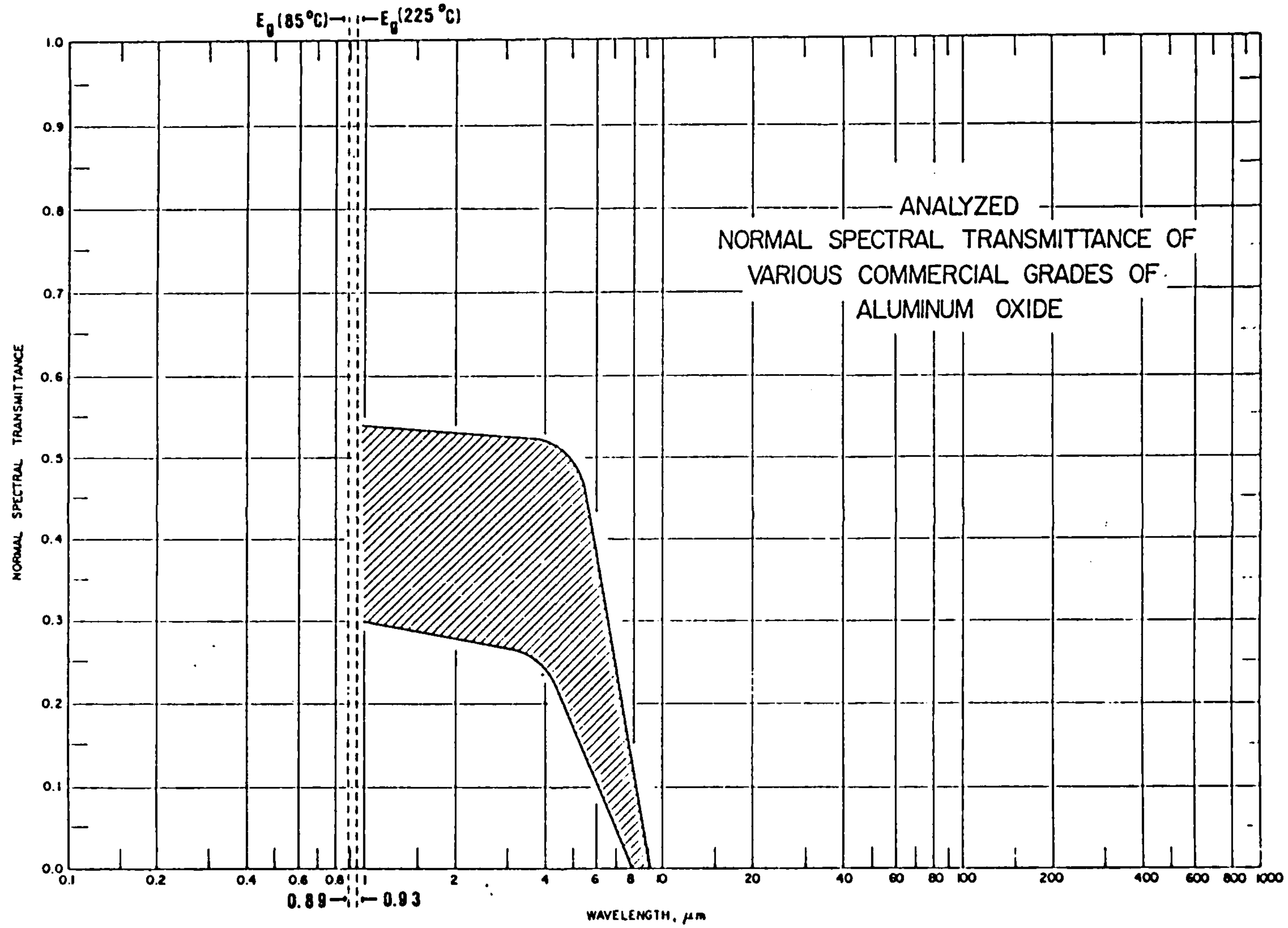


Figure 3.8. Analyzed normal spectral transmittance of various commercial grades of aluminum oxide (27:170).

temperatures will be explained in Chapter IV. The transmittance of each of the various grades of aluminum oxide is relatively constant from 1 to 4 μm; the shading in Figure 3.8 predominantly represents variations between different commercial samples (27:170-173). However, the intrinsic wavelength of light emitted from GaAs is shorter in wavelength (higher in frequency and energy) than 1 μm. In addition, the higher-energy, hot carrier transitions (Figure 2.12) emit even shorter wavelength light. This was confirmed by observations of visible light emissions from GaAs MESFETs (2:20). (Note that the visible spectrum is from 0.380 to 0.720 μm) (32:SEC 9,3). Even though the aluminum oxide lid is observably opaque its transmittance characteristics can be assumed to remain relatively constant through out the near infra-red band (to wavelengths as short as 0.720 μm) (28). This range of constant transmittance covers a large portion of the potential light emission wavelengths (carrier energies associated with recombination) and, therefore, was considered acceptable for this research. Figure 3.9 shows the spectral response of the photomultiplier tube with the intrinsic emissions wavelength range superimposed (32). The response of the photomultiplier tube was also considered adequate for this research. Since only relative measurements were of interest, no attempt was made to calibrate this system to determine absolute levels

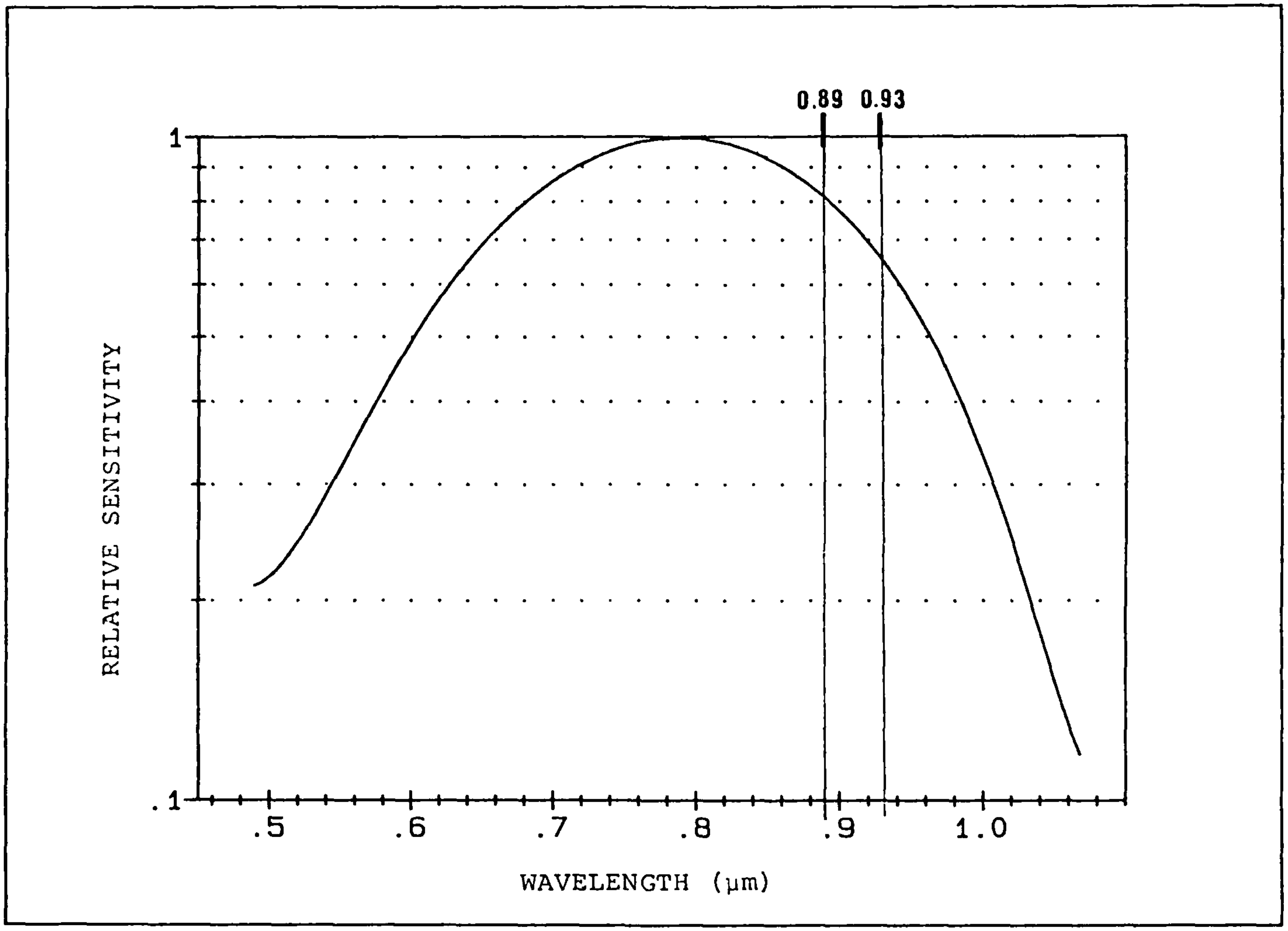


Figure 3.9. Spectral response of the photomultiplier tube (32).

of light emissions. In addition, a constant light source was not available to calibrate the photomultiplier tube's drift with respect to time and temperature. However, the dark current of the system or the I_{LE} reading with no light emissions provided a near constant signal. Since at very low rf drive levels the device does not emit significant quantities of light, measuring I_{LE} at a low rf drive level at the beginning of each test provided an appraisal of the consistency of the I_{LE} measurement arrangement. Over the testing period, the light current measured at the particular device temperatures used for the individual test runs and with a P_{IN} of 8.50 dBm varied from a minimum of 0.094 nA to a maximum of 0.118 nA. Even though some of these variations were probably due to changes in device temperature, the magnitude of the variations were so small in comparison to the experimental data used for determining trends between test temperatures, that no effort was made to compensate for these variations.

Experimental Test Program

Objectives. The overall objective of this project is to determine if the reliability studies on the Fujitsu FLM 7177-5 GaAs MESFET proposed for use on the DSCS III satellite have adequately accounted for the gate-to-drain avalanche breakdown failure mechanism. The objective section of Chapter I divided this overall objective into five specific goals. Of these, goals three and four are experimentally related. The third goal was to devise a test configuration capable of making measurements of light emissions, rf power levels, and dc bias values at temperatures ranging from normal operating temperatures to accelerated life test temperatures. The previous portions of this chapter have described the test configuration developed to accomplish this goal. To evaluate how well this test configuration satisfied this goal was the first experimental objective. A test program to identify deficiencies in the test configuration which may effect the validity of the results or are areas for future improvement was deemed necessary. The fourth goal from Chapter I was to use this instrumental configuration and experimentally verify the predicted variations in emitted light intensities, and thereby, validate the model of avalanche multiplication variation with temperature. Therefore, the second experimental objective is to collect the necessary test data to verify the theoretically predicted variations in emitted light intensities.

<u>Procedures</u>. This experimental test procedure section will describe the tests accomplished to satisfy the two experimental objectives discussed above and the procedures used. These tests were conducted on one Fujitsu FLM 7177-5H MESFET (S/N 7254) with nominal dc biases of -1.15 V (V_{GS}) and 8.50 V (V_{DS}). These bias parameters were verified or readjusted at each test point to correct for

any variations. This same MESFET (S/N 7254) was used in the GE life test as were all available devices (8). During the GE life test, this device was operated for 6000 hours at 195 °C and, as a result, suffered a 0.9 dB degradation in gain (8:SEC V,10). However, since this project is only making relative measurements between parameters, it is assumed the relationships between these parameters for this device are representative of new devices. In addition, all the measurements in this experiment were made through the device's lid. It is assumed that the lid attenuated total detectable light emissions consistently in all test conditions.

To satisfy the first experimental objective of evaluating the test configuration, the performance of the test device can be compared to the final performance of the device in the GE life test. The final power capability of this device in the GE test had an output of 35.5 dBm with an input of 30.0 dBm under similar dc bias conditions and ambient temperature (8:SEC V,10). Therefore, the first test requirement was to conduct this same measurement to verify repeatability. To satisfy this objective at the lowest controllable test temperature (45 °C) P_{OUT} at a P_{IN} of 30.0 dBm was measured. In addition, the power transfer curve of the device over a wide range of input powers was used to provide an indication of consistent measurements. Therefore, at each test temperature, approximately 25 experimental test points were made at different P_{IN} values ranging from well within the linear region to approximately 32.5 dBm where the device is saturated. The 32.5 dBm value was chosen because it was the P_{IN} value used in the JPL life test (9:Appendix I,5).

To satisfy the second test objective, experimental verification of the predicted variations in light emissions were measured at several different temperatures and input power levels. These measurements included not only the light current (I_{LE}) and input power (P_{IN}), but also P_{OUT}, I_{GS}, and I_{DS} were required to calculate gain and power dissipation. The gain is required to calculate the rf voltage swing at the drain which is correspondingly necessary to predict light emissions, and the power dissipation is necessary to calculate T_{CH} for comparison with the theory. The four test temperatures of T_{BP} were 45, 110, 145, and 168 ^{o}C. The 45 ^{o}C test temperature was the lowest controllable baseplate temperature. The 145 and 168 ^{o}C test temperatures were chosen since, when converted to channel temperatures, they roughly match the accelerated test temperatures of 195 ^{o}C and 225 ^{o}C used in the GE life test or the 190 ^{o}C and 225 ^{o}C used in the JPL life test (8:SEC IV; 9:Appendix I,5). The calculation of these channel temperatures from the experimental baseplate temperatures will be explained in Chapter IV. Three different P_{IN} settings were chosen at 3 dB increments to demonstrate validity of the model over a range of input powers. These settings were 25.5, 28.5, and 31.5 dBm, and were chosen to span a range of P_{IN} values corresponding to the top of the linear region to well within (greater than 1 dB compression) the saturation region. Figure 3.10 is a power transfer (gain) curve of a typical travelling wave tube amplifier (TWTA) with a dashed line indicating the extension of the linear response of the TWTA. The point where the actual response of the TWTA diverges from this dashed line separates the linear region from the saturation region. The amount of compression is determined by the difference between the actual response curve and the continuation of the linear response line at a given input power. Since the first experimental objective dictated the collection of approximately 25 test points, including this range of values, the only additional requirements were to assure these particular P_{IN} values were chosen, and that the additional measurements of I_{GS} and I_{DS} were made. To standardize all of the measurements, the bias current values and light emission level were collected for all data points.

Summary

This chapter described the experimental configuration and program used to collect the information necessary to validate the model of avalanche multiplication variation with temperature. The test configuration was discussed in

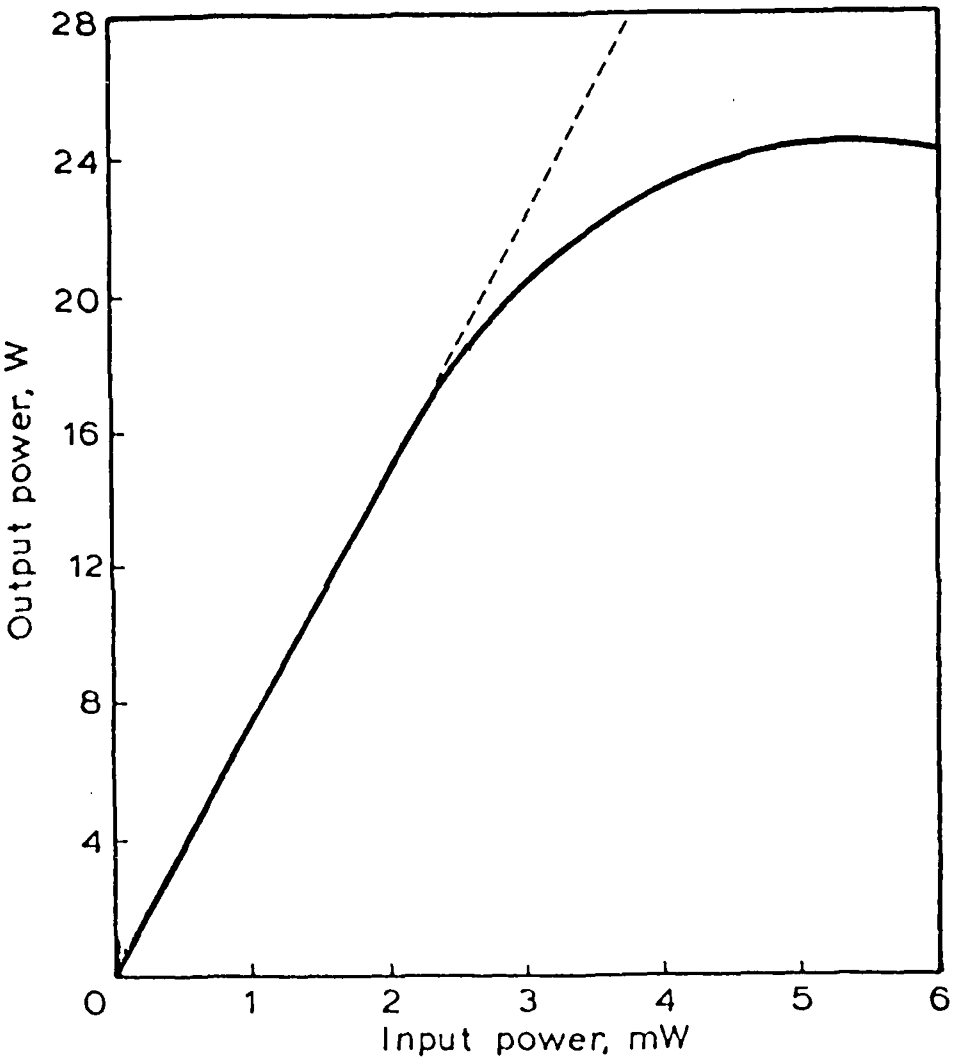


Figure 3.10. Power transfer (gain) curve of a typical Travelling Wave Tube Amplifier (33:SEC 34,19).

detail to show how it could control the necessary reference parameters of P_{IN}, V_{DS}, V_{GS}, and T_{BP}. In addition, this chapter described how this configuration could measure P_{OUT}, I_{DS}, I_{GS}, and I_{LE}. P_{OUT} is necessary to compute the device's gain which is required to determine the device's drain rf voltage swing. The dc bias currents are needed, along with P_{IN} and P_{OUT}, to determine the total power dissipated by the device. The power dissipation is used to convert T_{BP} into T_{CH} for comparison to the theoretical model. Lastly, I_{LE} is a measure of light emissions which is the parameter predicted by the theory of Chapter II. The experimental program described in this chapter developed the procedures for collecting the necessary data to validate this theory. The next chapter will present the results of performing these experiments.

IV. Results and Discussion

Introduction

This chapter presents the experimental results and formulates several associated observations. The two specific objectives of the experimental test program, presented in Chapter III, were to:

1. Evaluate how well the test configuration developed in Chapter III satisfies the requirements of making measurements of light emissions, rf power levels, and dc bias values at temperatures ranging from normal operating temperatures to accelerated life test temperatures.

2. Collect the necessary test data so that verification of the theoretically predicted variations in emitted light intensities could be tested.

This chapter will present the test results relating to both of these experimental objectives. In addition, observations based on these results will be discussed.

Evaluation of the Test Configuration

Operational. Two aspects of the test configuration caused difficulty in efficiently collecting data. The first of these is P_{IN} jitter. This jitter made it very difficult to make accurate measurements at high rf drive levels. The second of these is the T_{BP} control range. Later portions of this chapter will show that I_{LE} is temperature dependent. During the testing it was noted that variations of several degrees Celsius under conditions of high light emissions can significantly change the measured value. To procedurally compensate for the temperature fluctuations of the HTTF, care was taken to record data at roughly the same temperature. However, this was time consuming since only one, or at the most two, data points could be taken per temperature cycle.

P_{IN} jitter is rapid fluctuations of the rf power level about the desired P_{IN} value. Also, in some cases, these fluctuations are accompanied by shifts in the set value of P_{IN}. This jitter only exhibits itself at high rf drive levels (above 30 dBm), and in many cases is intermittent enough to allow accurate measurements. However, if data collection was attempted during these fluctuations they would force a real time interpretation of the P_{IN} value and, therefore, reduce the accuracy of the measurement. Compounding this problem is the fact that many correlated measurements must be made at that P_{IN} value, and the time needed to record these values is much longer than the stable time period of P_{IN} when it is fluctuating. Therefore, the operator must determine how each of these parameters is varying with the P_{IN} fluctuations and record the values at a corresponding point during the variations. This is both potentially inaccurate and very time consuming. Fortunately, since this only happens at high rf drive and intermittently, enough data points were collected without jitter to obtain the data necessary to satisfy the experimental objectives. However, it is quite frustrating and worthy of some corrective effort if continued measurements are made with this instrumental configuration. One attempt was made during this experiment to fix the problem. Since an isolator was incorporated prior to the input tuner in the test arrangement, it was concluded the problem was in the instrumental configuration somewhere in the rf signal path from the signal source through the input dual-directional coupler. Because there was an observable change in helix current, the most likely cause was considered to be the Hughes TWTA. Consequently, this unit was replaced with an identical model. This apparently cured the problem for a short period of time, but eventually the jitter returned, although not as frequently.

The T_{BP} control range is the temperature range that T_{BP} spans throughout the HTTF temperature control cycle. It is a function of the temperature controller, the variac selected heater power, and the HTTF design. Typical variations were approximately $\pm$ 5.5 °C. Changing the variac setting, which changes the heater wattage, could reduce this slightly to $\pm$ 4.5 °C. Ideally, if a heater wattage equal to the heat dissipation from the block is selected, the heater will be constantly on and keep the temperature stable. With this experimental arrangement, however, this is impossible to achieve. It would be extremely time consuming to experimentally establish this variac setting. Also, since the amount of heat flowing into the block from the device changes with P_{IN} (power added efficiency changes), the variac setting would have to be adjusted for every data point. In addition, with the heater power set at a low value to counteract dissipation from the block, if the block temperature does rise enough to trip the controller off, the block would cool down quickly and the heater, when turned back on, would take a very long time to bring the block temperature to the control point. Therefore, for these experiments, the variac was set somewhat higher. This higher setting did permit some overshoot; however, the higher setting was necessary to minimize the temperature deviations below the control point when the controller tripped off. This behavior contributed to the larger than desired temperature control range of approximately ± 5 °C. Procedurally, setting the control point such that the desired T_{BP} was at the high end of the control range provided more consistent temperatures for data collection. Since the temperature variations slowed after the heater turned off, and before heat dissipation started to rapidly cool the block, a period of relatively stable temperature existed. This time period was long enough to make one or possibly, by quickly changing P_{IN}, two measurements. However, since the temperature cycles were several minutes in length, taking data only during one portion of each cycle was a time consuming procedure.

Accuracy and Consistency. As described in Chapter III, the accuracy of the test configuration and its consistency needed to be experimentally verified. Comparing the performance of the test device in this experimental arrangement to the performance of the same device in the GE test configuration provided an indication of accuracy. Since this device (FLM 7177-5, S/N 7254) was used in the GE life test, its final performance in that test should match the performance in this experiment. The final power capability of this device in the GE test was 35.5 dBm at ambient temperature with an input of 30.0 dBm and similar dc bias conditions (8:SEC V,10; Appendix,7). With this experimental arrangement the corresponding output level is approximately 35.8 dBm. This indicates a small, but acceptable, variance in test configurations, which could be attributed to experimental variations. Secondly, consistency can be ascertained from plots of the power transfer curves. Power transfer curves demonstrate how the device is performing. Consistent measurements taken on a properly operating device should reduce to a standard power transfer curve (linear at lower powers and saturating at higher powers) that is smooth in appearance. Significant scattering of the data points about the least-squares curve would indicate inconsistency in the test configuration or device. Figures 4.1 through 4.4 show the least-squares power transfer curves (with the experimental test points displayed) for the device under test at the four test temperatures. These curves demonstrate consistent data collection from the experimental configuration.

Experimental Results

The second experimental objective was to collect data to test the validity of the theoretically predicted variations in emitted light intensities. This section presents the test data collected to satisfy this objective and discusses some observations based on this data. This data includes not only the light current (I_{LE}) and input power (P_{IN}), but also I_{DS}, I_{GS}, and P_{OUT} required to calculate power dissipation and gain. The power dissipation is necessary to calculate the channel temperature (T_{CH}). T_{CH} is required to permit comparison of the experimental results to the theoretical predictions. The gain is required to calculate the rf voltage swing at the drain, which is necessary to theoretically predict the amount of light emitted. The remainder of this section will describe the calculation of T_{CH}, compare the test data to the theoretically predicted levels, and discuss some observations based on this comparison.

Channel Temperature Calculation.

The channel temperature of the device is calculated from the thermal resistance of the device, the power dissipation of the

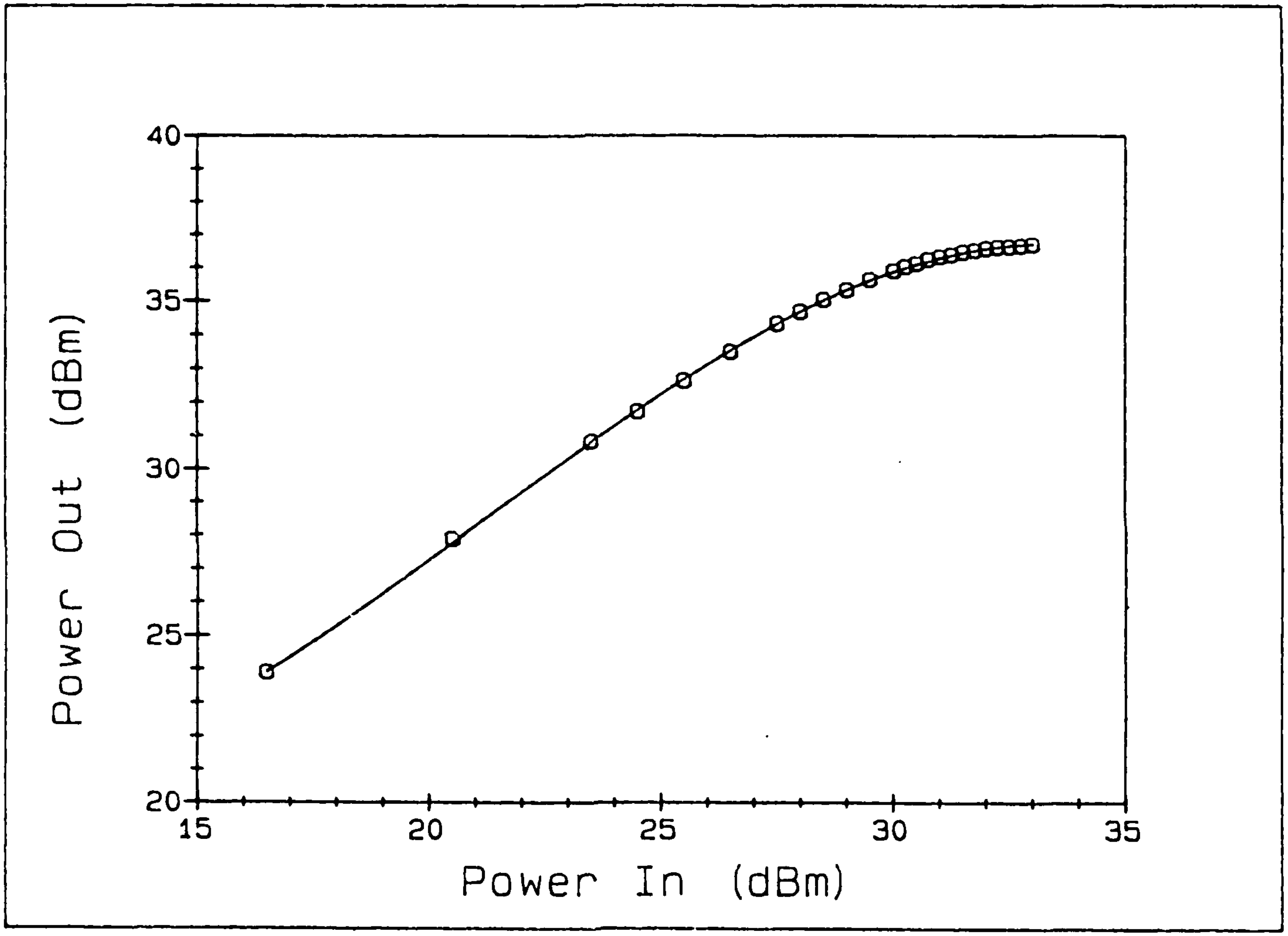


Figure 4.1. Least-squares power transfer curve at a channel temperature of 85 ^{o}C. The minimal scattering of the experimental data points indicates the consistency of the test configuration.

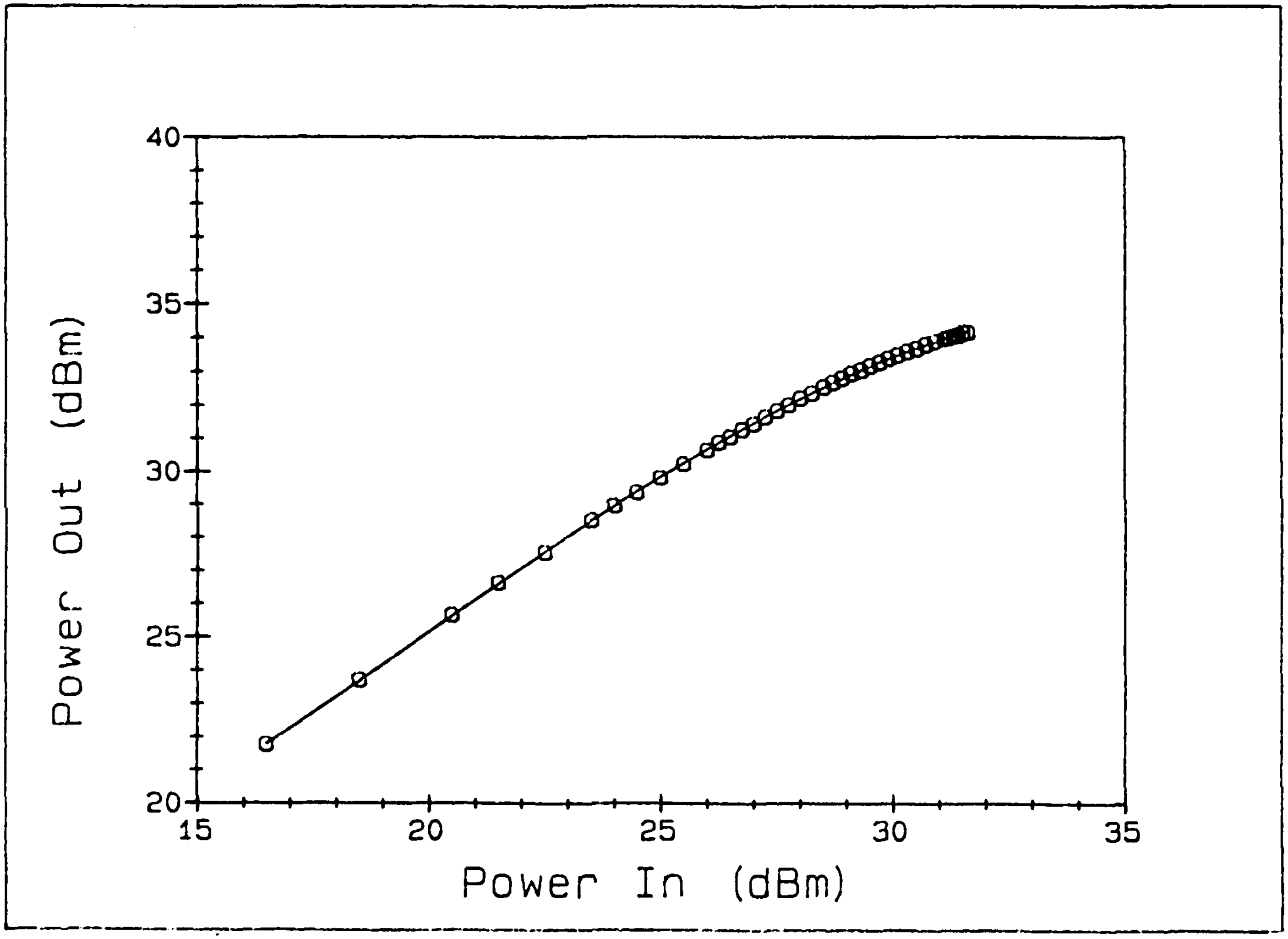


Figure 4.2. Least-squares power transfer curve at a channel temperature of 155 ^{o}C. The minimal scattering of the experimental data points indicates the consistency of the test configuration.

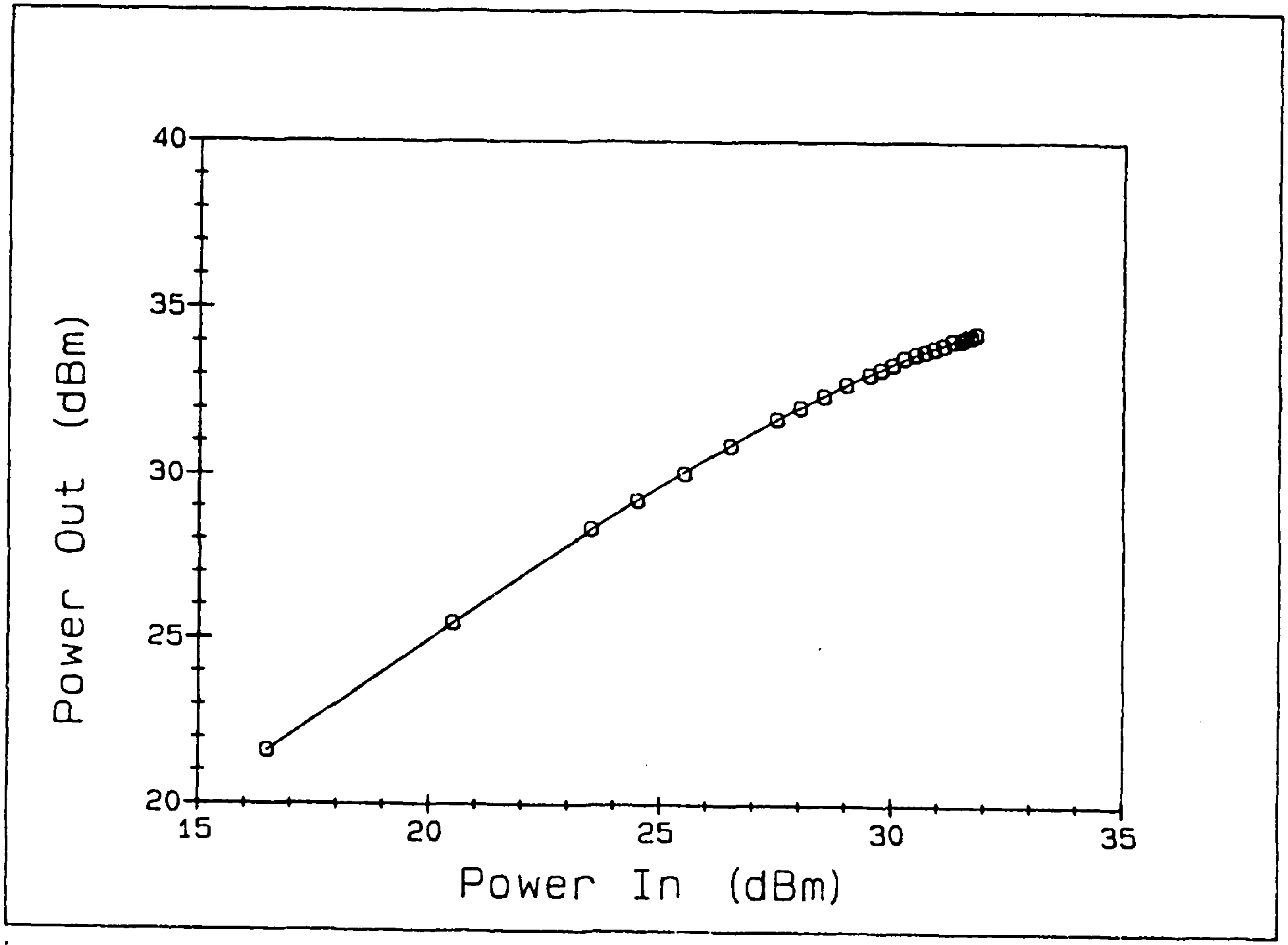


Figure 4.3. Least-squares power transfer curve at a channel temperature of 195 °C. The minimal scattering of the experimental data points indicates the consistency of the test configuration.

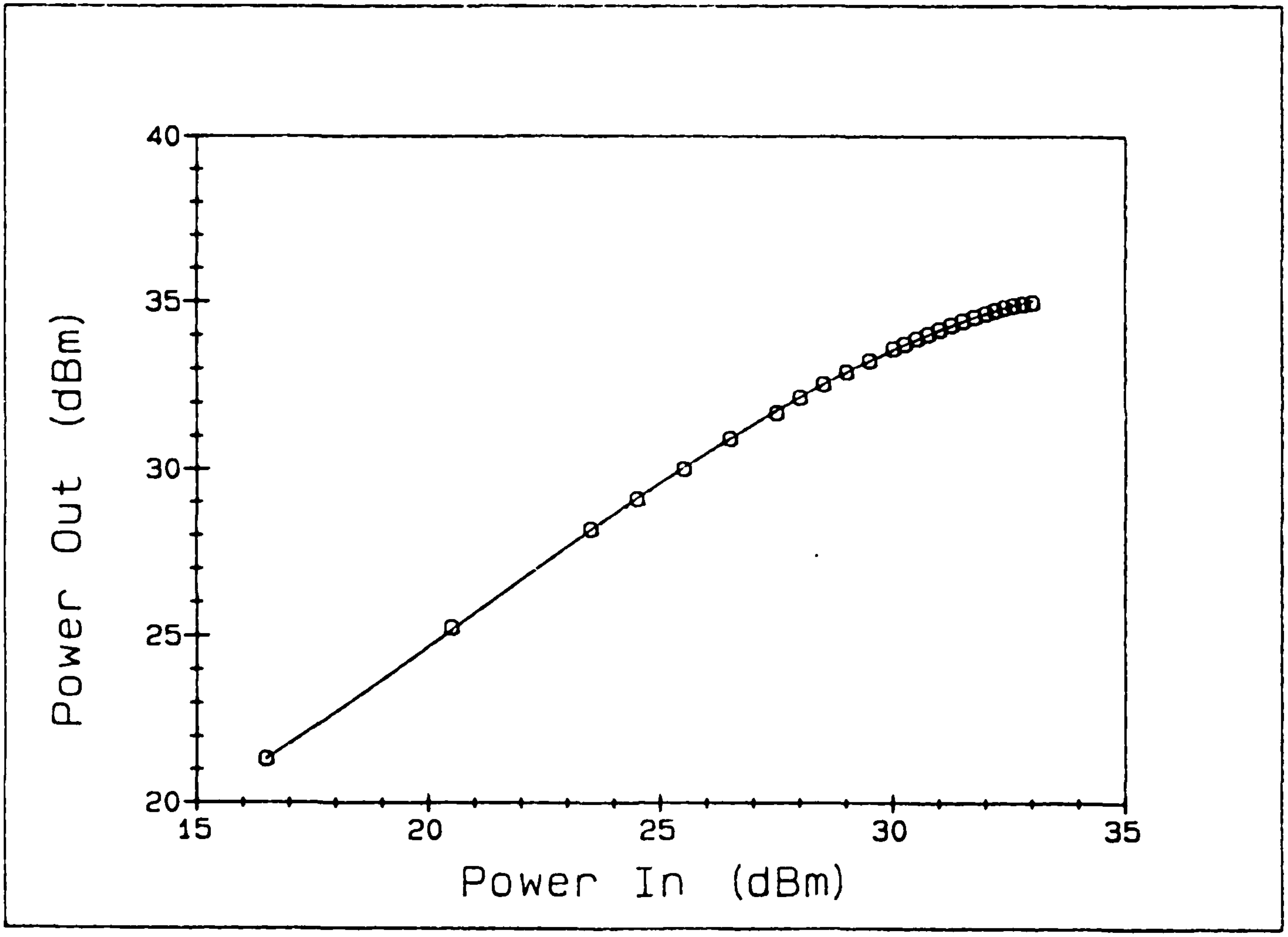


Figure 4.4. Least-squares power transfer curve at a channel temperature of 225 ^{o}C. The minimal scattering of the experimental data points indicates the consistency of the test configuration.

device, and the baseplate temperature of the device. The thermal resistance was determined from the JPL measurements (9:Appendix II). These were heat pulse measurements made on Fujitsu 7177-5 FETs. From these measurements, JPL determined that at a channel temperature of 190 ^{o}C, the average thermal resistance was 4.5 ^{o}C/W with a standard deviation of 0.47 (9:Appendix II,4). They also discerned that thermal resistance varied linearly with respect to temperature with a gradient of 1.01 when plotted on a log-log scale (9:Appendix II,4-6). Therefore, at a given channel temperature, the average thermal resistance can be calculated by Equation 4.1. This equation is the point-slope formula for a straight line on a log-log scale, and it can be expressed as:

$$R_{CC}(T_{CH}) = 10**\{N\ [LOG(T_{CH}+273)-LOG(190+273)] + LOG[R_{CC}(190)]\} \quad (4.1)$$

where

$R_{CC}(T_{CH})$ = thermal resistance at T_{CH} (^{o}C/W)
N = exponent representing the slope of thermal resistance to channel temperature on a log-log scale .

From the JPL measurements, $R_{CC}(190) = 4.5$ ^{o}C/W and $N = 1.01$, therefore:

$$R_{CC}(T_{CH}) = 10**\{1.01\ [LOG(T_{CH}+273)-LOG(463)] + LOG(4.5)\}. \quad (4.2)$$

However, this assumes that T_{CH} is known. As stated above, channel temperature is a function of T_{BP}, R_{CC} and P_{DS} which is the power the device dissipates (9:Appendix II):

$$T_{CH} = R_{CC}(T_{CH})\ P_{DS} + T_{BP}\,. \tag{4.3}$$

From Equation 4.2 and 4.3, R_{CC} values can be calculated for each T_{BP} control point if P_{DS} is known. At this point P_{DS} was assumed to be 12.75 W. This was derived assuming the major contributor of P_{DS} was the drain bias. The drain bias power with $V_{DS} = 8.50$ V and typically $I_{DS} = 1.50$ A is orders of magnitude larger than the gate bias power with $V_{GS} = -1.15$ V and $|I_{GS}| < 20.0$ mA . In addition, since the R_{CC} calculation is rather insensitive to the choice of P_{DS}, it was not considered necessary to include the effects of P_{IN} and P_{OUT} in this initial prediction of P_{DS}. One watt difference in P_{DS} varies R_{CC} by less than 0.1 ^{o}C/W. This variation is small compared to the standard deviation of 0.47 ^{o}C/W derived by JPL (9,Appendix II:4). Assuming 12.75 W, Table 4.2 shows the R_{CC} values at each T_{BP} control point. These R_{CC} values were used to calculate T_{CH} at each test point using the actual device P_{DS}, including rf power, at that point. The channel temperature for all of the data points was calculated using Equation 4.3, where R_{CC} is taken from Table 4.1 and P_{DS} was calculated from the power conservation equation:

$$P_{DS} = P_{DC} + P_{IN} - P_{OUT} \tag{4.4}$$

where

$$P_{DC} = \text{total dc power (W)} = V_{DS}I_{DS} + V_{GS}I_{GS} \ .$$

TABLE 4.1

THERMAL RESISTANCE VALUES

BASEPLATE TEMPERATURE (T_{BP}) (^{o}C)	THERMAL RESISTANCE (R_{CC}) ($^{o}C/W$)
45.0	3.52
110.0	4.24
145.0	4.64
168.0	4.84

The channel temperature was calculated for each test point, and the complete experimental results are presented in tabular form in Appendix A.

<u>Comparison of Test Data with the Theoretical Predictions</u>. To validate the theoretical model, the predicted light emissions at the four different test temperatures was compared to the experimental measurements. This comparison was accomplished for each temperature at the three input power settings: 25.5, 28.5, and 31.5 dBm. This section summarizes the calculations (from Chapter II) used to make the theoretical predictions of light emission. Next, a comparison of the predictions to the experimental data will be presented graphically.

Chapter II described the theoretical development of a light emissions prediction, or more precisely, a prediction of the carrier generation rate which is proportional to light emissions. This prediction is based on the Frensley (11) model of gate-to-drain avalanche breakdown which was modified using a temperature dependent equation for α, the ionization coefficient, developed by Crowell and Sze (12). From this V_B, the breakdown voltage, for the device under test was calculated and presented in Figure 2.11. Once the breakdown voltage is calculated, the percentage of time the device is in avalanche breakdown, T_B, for an ideal sinusoidal wave was determined using Equation 2.7. The peak voltage swing at the drain is derived from the input power and gain using Equation 2.17. Next, the average carrier generation rate during breakdown was calculated using Equation 2.21. Finally, the theoretical prediction of I_{LE} was calculated from Equation 2.23 which is repeated here for convenience:

$$I_{LE} = C_1 G_B x_A T_B \tag{2.23}$$

where

I_{LE} = light induced photomultiplier current (nA)
C_1 = constant of proportionality -- empirically determined (nA-s-cm^2)
G_B = average carrier-concentration generation rate in breakdown (cm^{-3}-s^{-1})
T_B = percentage of time in breakdown
x_A = width of the avalanche region (cm) .

The theoretical predictions derived from Equation 2.23 are compared to the experimental results in Figure 4.5. For the purposes of this comparison, the constant of proportionality was $C_1 = 10^{-20}$ nA-s-cm .

Discussion. Figure 4.5 indicates poor correlation between the theoretical predictions and the experimental results. Although the theoretical lines do exhibit a negative gradient, it is not nearly as steep as that associated with the corresponding behavior of the experimental data. In addition, the theoretical predictions do not show the widely varying magnitudes that the experimental data exhibit. In an attempt to obtain better correlation, the assumptions used in developing the theoretical prediction were reexamined. The assumption of uniform light emission over the width of the gate was readdressed since changes in the extent of the gate's width that emanates light could account for wide variations in the intensity of light emissions. If the light emissions are not generated uniformly along the gate width, then they are generated by localized microplasmas (17:772). Logan, Chynowelth, and Cohen (10) quantitatively examined microplasmas in GaAs p-n junctions and determined that the number of microplasmas increase exponentially with bias voltage (10:2521-2522). Since the gate-to-drain voltage is the average ac drain voltage plus the difference between the drain bias voltage and the gate bias voltage, then:

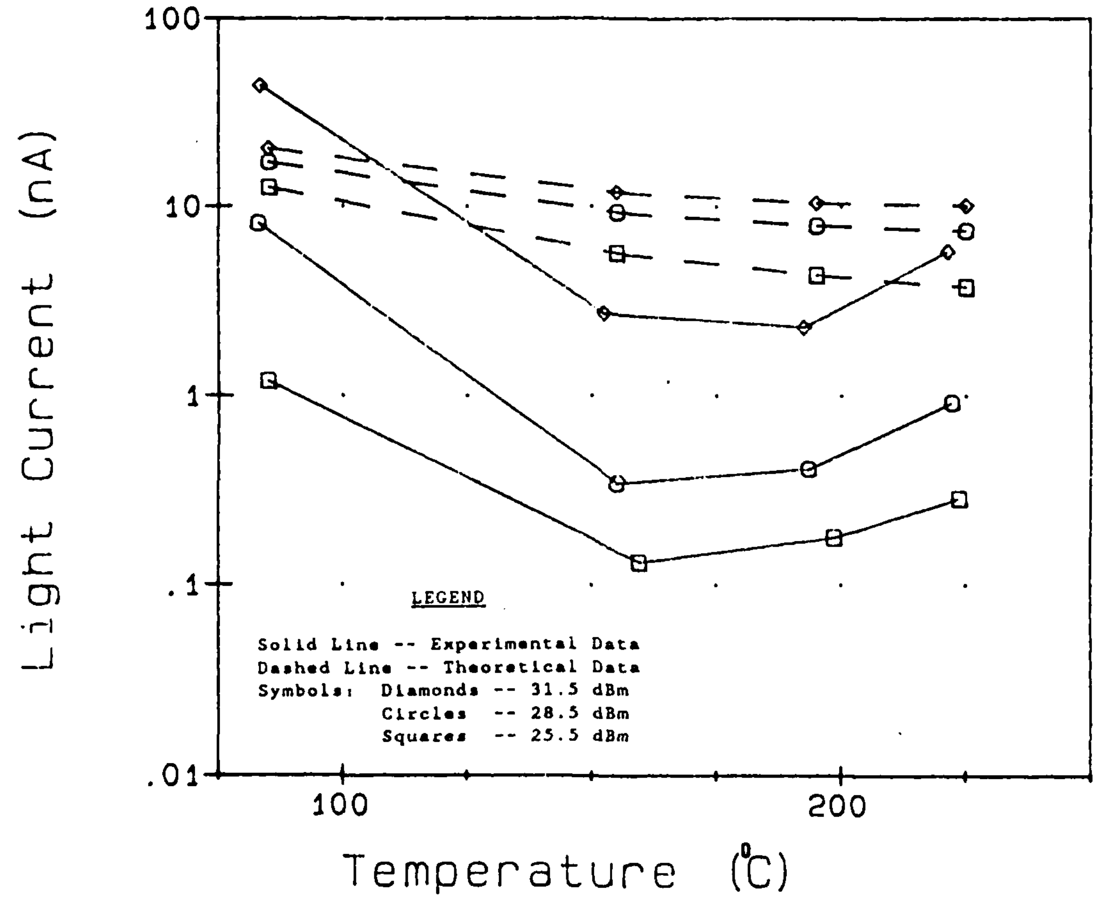


Figure 4.5. Comparison of experimental results with the theoretical prediction of light emissions at three different input power levels.

$$\text{Number of Microplasmas} = \text{EXP}\ [C_2(\bar{v}_B + V_{DS} - V_{GS})] \quad (4.5)$$

where

C_2 = microplasma generation constant (V^{-1})
$\bar{v}_B$ = average ac drain voltage in breakdown (V)
V_{DS} = drain bias voltage (V)
V_{GS} = gate bias voltage (V) .

In addition, some of the junctions tested indicated that each of the microplasmas were of equal intensity (10:2522). Equation 2.23 is the theoretical prediction of light induced current assuming the entire gate width is in avalanche breakdown. If small localized microplasmas are occurring along the gate, the light induced current of each of the microplasmas should be related to the size of the microplasma in relation to the entire gate width. Therefore, the amount of light induced current caused by each microplasma is proportional to Equation 2.23. Assuming an equal intensity for each microplasma, the amount of light induced current caused by each microplasma is:

$$I_{LE} \text{ per Microplasma} = C_3 G_B x_A T_B \quad (4.6)$$

where

I_{LE} = light induced photomultiplier current (nA)
C_3 = constant of proportionality (nA-s-cm^2)
G_B = average carrier-concentration generation rate in breakdown (cm^{-3}-s^{-1})
x_A = width of the avalanche region (cm)
T_B = percentage of time in breakdown .

Therefore, accounting for microplasma formation, the total amount of light induce current is:

$$I_{LE} = C_3 G_B x_A T_B \, EXP[C_2(\bar{v}_B + V_{DS} - V_{GS})] \qquad (4.7)$$

where

I_{LE} = light induced photomultiplier current (nA)
C_3 = constant of proportionality -- empirically determined (nA-s-cm^2)
G_B = average carrier generation rate in breakdown (cm^{-3}-s^{-1})
T_B = percentage of time in breakdown
x_A = width of the avalanche region (cm)
C_2 = microplasma generation constant -- empirically determined (V^{-1})
$\bar{v}_B$ = average ac drain voltage in breakdown (V)
V_{DS} = drain bias voltage (V)
V_{GS} = gate bias voltage (V) .

Figure 4.6 compares the modified theoretical predictions derived from Equation 4.7 to the experimental results. For the purposes of this comparison, the constants were C_2 = 2.1 V^{-1} and C_3 = 10^{-33} nA-s-cm^2 . The C_2 constant was chosen to provide the best match in slope to the initial [I_{LE}(85 °C) to I_{LE}(155 °C)] portion of the P_{IN} = 31.5 dBm experimental curve of Figure 4.6. The chose of C_2 = 2.1 V^{-1} was made by graphical observation; however, the slopes of the theoretical and experimental curves were verified to match within 3 %. Since the experimental configuration was not calibrated for absolute light measurements, the C_3 constant of proportionality was arbitrarily chosen for graphical comparison. Figure 4.6 indicates good correlation between the modified theoretical predictions and the experimental results. The ambient temperature light current points are very well matched. This shows agreement between the modified theory and test

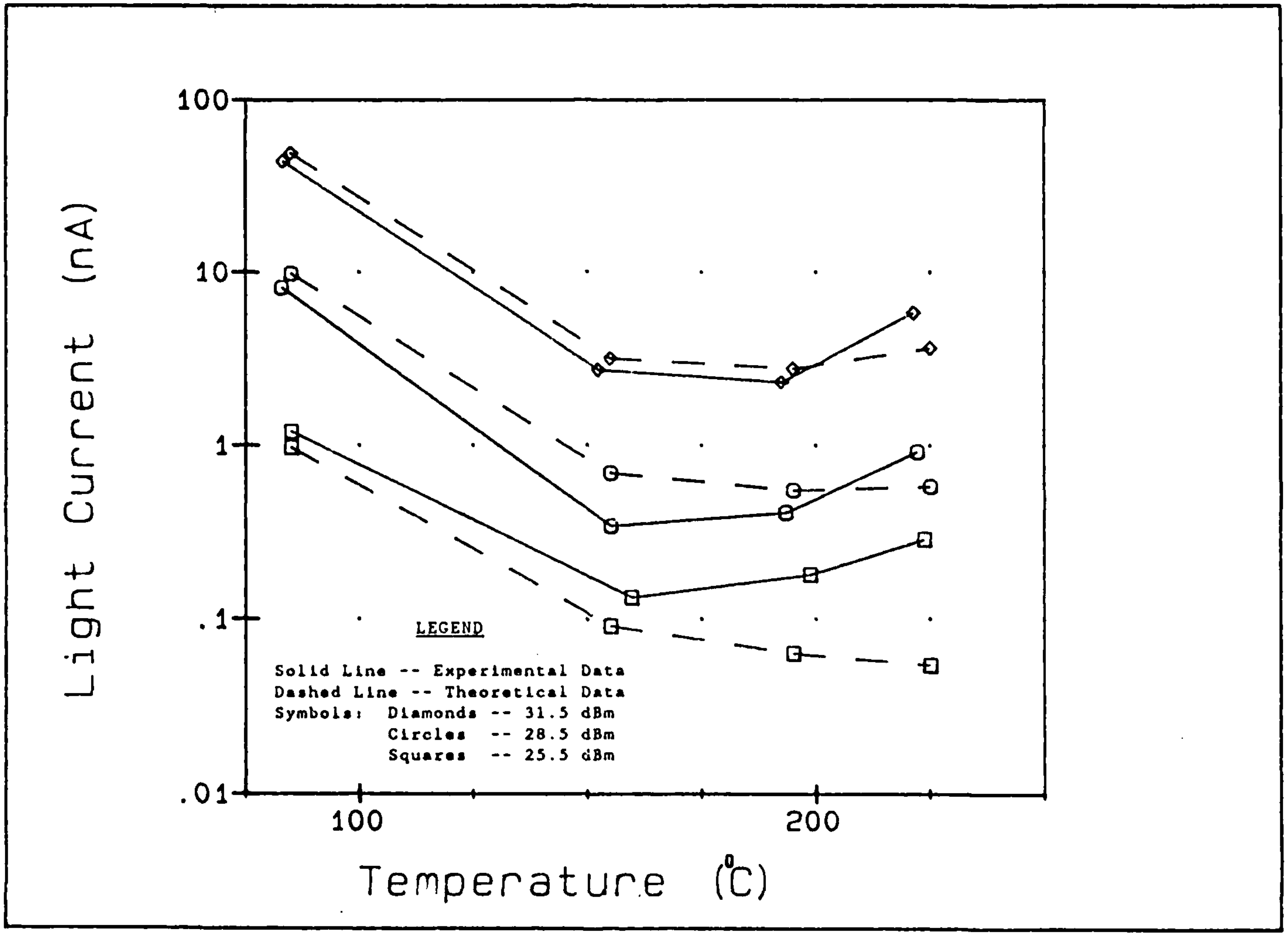


Figure 4.6. Comparison of experimental results with the modified theoretical prediction of light emissions at three different input power levels.

data on the variation of light emissions with changes in input power. The initial roll-off of light emissions with temperature is also modeled very well by the modified theory. Of course, for the P_{IN} = 31.5 dBm case, the theoretical and experimental lines were made parallel by the choice of the microplasma generation constant (C_2). However, with this constant defined, theory and experiment correlate well for the other two input power settings. Lastly, the theoretical predictions correlate to the experimental data at the higher temperatures. The best correlation is at the highest input power setting and gets progressively worse as the input power decreases. The experimental light emissions increase more sharply at higher temperatures than theoretically predicted. In fact, at the lower power setting, theory predicts a continued decrease in light emissions with temperature. This divergence between theory and test data at higher temperatures could be caused by a light producing mechanism (other than avalanche multiplication) which exhibits itself at high temperatures. Since avalanche multiplication generates more light emissions at higher input power settings, the correlation between theory and test would be best at the highest input power. As the input power is lowered, the amount of light emissions from avalanche multiplication would decrease, and the light emitted from the other mechanism would become more prominent, causing a greater divergence between theory and test. However, the correlation between the theoretical predictions and experimental data is considered sufficient to verify the use of the modified theory for the purposes of this study.

Summary

This chapter evaluated the test configuration, presented the experimental results, and discussed the significance of these results. The test configuration was evaluated from an operational perspective and for accuracy and consistency. Operationally, two difficulties with the test configuration were discussed. These two difficulties were P_{IN} jitter and the T_{BP} control range. Neither of these difficulties were critical in collecting the necessary experimental data for this study. However, both hindered efficient data collection, and if any future testing with this configuration is attempted, they should be rectified. The accuracy of the test configuration was checked by comparing a power measurement using this configuration to one made on the same MESFET in the GE test configuration. The consistency of the configuration was demonstrated by presenting the power transfer curves of the device at all four test temperatures. Next, the experimental results were presented. The calculation of the channel temperature of the device under test was accomplished to permit comparison of the experimental data to the theory. Next, the experimental results were graphically compared to the theoretical predictions. Lastly, discussions of this comparison indicated that the theory developed in Chapter II did not correlate well with the experimental results. However, if the light emissions were considered to be generated from microplasmas rather than uniformly across the entire gate width, good correlation was demonstrated. Therefore, this chapter verified the modified theoretical model of light emission. In addition, by verifying this theory, it validated the model of avalanche multiplication variation with temperature upon which the theoretical prediction of light emission was based. This model of avalanche multiplication variation with temperature will be used in Chapter V to evaluate the assumption, made in the reliability studies of the Fujitsu FLM 7177-5 MESFET, that all failure mechanisms, including avalanche multiplication, are accelerated equally with temperature.

V. Conclusions and Recommendations

Introduction

The overall objective of this investigation was to determine if the reliability studies on the Fujitsu FLM 7177-5 GaAs MESFET, proposed for use in the DSCS III satellite, have adequately accounted for the gate-to-drain avalanche breakdown failure mechanism. Chapter I addressed this overall objective by partitioning the analysis into a set of five specific goals. This introductory section will capsulize the issues impacting these goals. The remaining portion will culminate the investigation, present findings associated with the overall objective, and provide recommendations for future effort.

To summarize the presentation, this section reviews the specific goals outlined in Chapter I and how they were satisfied by this investigation. The specific goals were:

1. By adapting an existing analytical model (11) for temperature effects (12) and the specific parameters of the Fujitsu GaAs MESFET, predict the variation of gate-to-drain avalanche multiplication with respect to temperature.

2. Using the predicted variation in avalanche multiplication, predict the associated changes in the intensity of emitted light.

3. Devise a test configuration capable of making measurements of light emissions, rf power levels, and bias values at temperatures spanning normal operating temperatures to accelerated life test temperatures.

4. Using this instrumentation scheme, experimentally verify the predicted variations in emitted light intensities. This will validate the model of avalanche multiplication variation with temperature.

5. Lastly, this model will be used as a partial evaluation of the assumption made in the reliability studies that all failure mechanisms, including avalanche multiplication, are accelerated equally with temperature.

Chapter II developed the model of avalanche multiplication variation with temperature. This model calculated the percentage of time the device was in avalanche breakdown (T_B) as a function of temperature, bias settings, input power level, and gain. Chapter II developed a model to predict the amount of light emitted by the device at different temperatures and input power levels. This model was later modified in Chapter IV to enhance the correlation with the experimental data. Chapter III described the equipment configuration used to make the measurements necessary to verify the predicted variations in light intensities. In addition, the chapter also explained the experimental test program used to collect the data. Chapter IV evaluated the test configuration and presented the experimental results. The discussion of the experimental results (Chapter IV) concluded that the modified theoretical model of the variation of light emissions with temperature and input power sufficiently matched the experimental data to validate the model of avalanche multiplication variation with temperature.

Therefore, of the specific goals outlined, the first four have been satisfied. The fifth goal of evaluating the assumption that all failure mechanisms, including avalanche multiplication, are accelerated equally with temperature is addressed in the next section.

Conclusions

The General Electric Corporation performed an accelerated temperature life test on the Fujitsu FLM 7177-5 MESFET, and concluded it was a very reliable device with a MTTF of 10^6-10^7 hours (8:SEC IV). However, this study was conducted under the assumption that the dominant failure mechanisms are accelerated according to the Arrhenius relation, and that the same failure mechanisms causing failure at elevated life test temperatures will cause failures at normal operating temperatures (8:SEC IV). These are common assumptions used in other accelerated life tests to permit the extrapolation of high temperature test data to normal operating temperatures (5:395; 6:151; 7:321). However, with little understanding of the failure mechanisms present in a GaAs MESFET under high rf drive, the validity of these assumptions is not obvious. The overall reliability of a device is determined by a set of different failure mechanisms. For a particular operating condition, any one of these, or a subset of these failure mechanisms, could be dominant, and thus limit the operational life of the device. If one of these failure mechanisms is accelerated more slowly with temperature, then its effect on the reliability of the device at normal operating temperatures would not be evident from accelerated temperature life testing. This is a result of the fact that at higher life test temperatures, the effect of this failure mechanism would be masked by failure mechanisms that were accelerated much faster with temperature. Therefore, to verify the validity of extrapolating the accelerated temperature life test results to normal operating temperatures, each of the failure mechanisms not causing failure at the elevated temperatures needs to be identified and examined separately. To determine if accelerated temperature life testing has adequately addressed the contribution of a particular failure mechanism, its physical acceleration with temperature can be compared to the acceleration used to extrapolate the reliability at normal operating temperatures. If the physical acceleration with temperature of this failure mechanism is slower than the acceleration used for extrapolation, then its contribution to reliability was not adequately addressed.

The overall objective of this investigation was to determine if the reliability studies on the Fujitsu FLM 7177-5 GaAs MESFET have adequately accounted for the gate-to-drain avalanche breakdown failure mechanism. The General Electric Corporation life test referenced above, and the concurrent Jet Propulsion Laboratory tests have assumed all failure mechanisms were accelerated equally to allow extrapolation of test data. To evaluate if these tests adequately address avalanche multiplication, the validated model of avalanche multiplication variation with temperature can be compared to the acceleration used to extrapolate the life test data. If the model for avalanche multiplication shows a slower acceleration, then its contribution to the overall reliability of the device at normal operating temperatures was not adequately addressed in determining the life test predictions.

The model of avalanche multiplication variation with temperature computes the percentage of time the device is in avalanche breakdown. Assuming avalanche multiplication was the dominant failure mechanism, the failure point of the device is related to the total amount of time the device is in avalanche breakdown. The percentage of time the device is in breakdown (T_B) can be used to determine how this total time changes with temperature. For example, if $T_B = 10\ \%$ at normal operating temperatures and the device fails after 10^4 hours of operation, the device would have been in breakdown for 10^3 hours. If the temperature of the device increases and T_B increases the avalanche multiplication, then this failure mechanism will be accelerated and the device will fail after less operating time. The amount of this acceleration compared to the acceleration curve used in the General Electric Corporation life test will determine if the avalanche multiplication failure mechanism was adequately accounted for in the MTTF predictions. Figure 5.1 shows the change in T_B with temperature from the validated model of avalanche multiplication. This graph demonstrates that T_B is actually lower at accelerated life test temperatures than at normal operating temperatures. Therefore, the avalanche multiplication failure mechanism is decelerated with respect to increasing temperature. However, this analysis assumes that degradation of device performance occurs at the same rate during all periods of avalanche breakdown. Under this assumption, one hour of operation in avalanche breakdown at 85 ^{o}C and an input power of 31.5 dBm would cause the same degradation as one hour of operation in breakdown at 225 ^{o}C and an input power of 25.5 dBm. This may be a good first order assumption, but, as shown in Chapter II, the average ionization coefficient during breakdown varies with temperature and input power. This change in the average ionization coefficient during breakdown causes a change in the total number of impact ionizations occurring. In addition, as shown in Chapter IV, the number of microplasmas also varies with temperature and input power. Assuming failures associated with avalanche multiplication are a function of the cumulative number of impact ionizations that have occurred in the

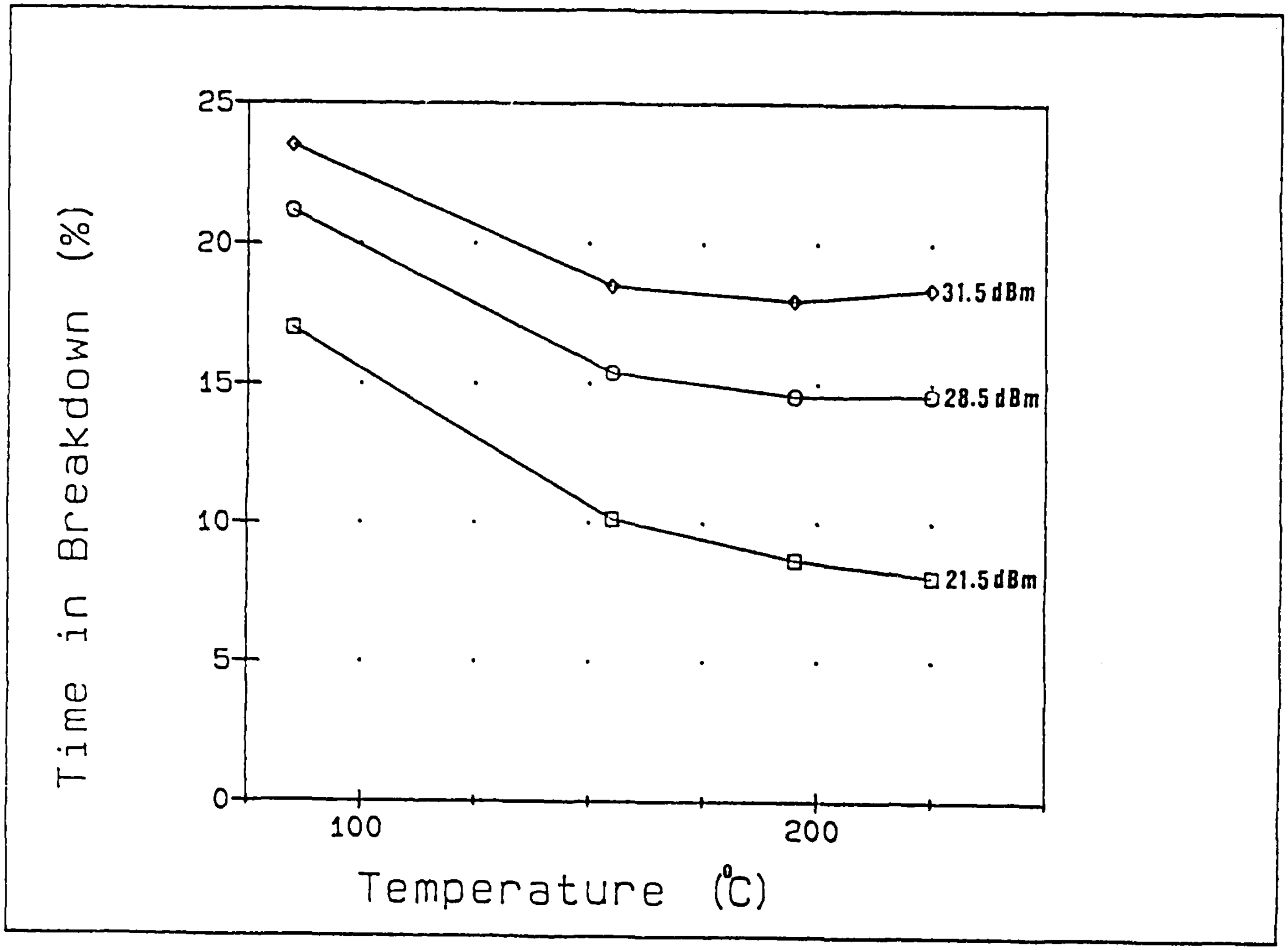


Figure 5.1. Variation in the percentage of time the device is in avalanche breakdown with respect to temperature at three input power settings.

device, then the MTTF is inversely proportional to the number of ionization events. Chapter IV developed the modified theory for predicting light emissions based on this impact ionization (carrier-concentration generation) rate. The predicted light emission was a constant of proportionality times this rate. Therefore, the variation, with respect to temperature and input power, in the rate of impact ionizations will follow the same theoretical curves shown in Figure 4.6. This behavior also indicates a deceleration of avalanche multiplication activity with increasing temperature. With this evidence, it is clear that no accelerated temperature life test can adequately account for avalanche multiplication since the increased temperature used to accelerate other failure mechanisms, reduces the effect of avalanche breakdown.

Recommendations

The recommendations for future efforts stemming from this research is presented in three catagories. First, a recommended improvement to the experimental configuration is proposed. Second, potential refinements to the analytical model used in this research are presented. Lastly, since accelerated temperature life testing does not adequately account for gate-to-drain avalanche breakdown, alternate approaches to determining the impact on reliability of avalanche breakdown are discussed.

Experimental Configuration Improvement. If future experiments are made with this arrangement, an improvement needs to be made to the temperature control system. As discussed earlier (Chapter IV), the temperature fluctuations of the experimental configuration were approximately ± 5 ^{o}C. However, setting the control point such that the desired device baseplate temperature was at the high end of the control range provided more consistent temperatures for data collection. Because the temperature variations slowed after the heater turned off, and before heat dissipation started to rapidly cool the block, a period of relatively stable temperature existed. This time period was long enough to make one or possibly two measurements. However, since the temperature cycles were several minutes in length, taking data only during one portion of each cycle was a time consuming procedure. One possible improvement would be to provide a constant heater current which would be selectable to provide just slightly less heat than the block's dissipation, and a second higher selectable heater current controlled by a faster controller which has a tighter control zone. In addition, a larger mounting block should be used. With the increased mass of the mounting block, temperature fluctuations would be reduced. The constant heater current would offset the rapid cooling, and the higher current would be selected to minimize overshoot. The faster controller would also limit overshoot by tripping off more quickly. The limiting factor, of course, is the thermal lag in the controller feedback thermocouple. However, with this proposed configuration a much narrower control range, within the ± 2 °C desired range, should be possible.

Analytical Model Refinement. The analytical model used in this research was adequate for relative comparison of avalanche breakdown activity at different temperatures. But, a more accurate model of avalanche breakdown as a function of device parameters would be valuable. It would not only aid in device design, but also in determining the effects of avalanche breakdown on device reliability. The present model assumes a planar device. The effects on avalanche breakdown of recessing the gate are complex and difficult to model (11:968). However, recessing the gate is a prevalent design technique for GaAs MESFETs and understanding the effects of recessing the gate on avalanche breakdown would be very beneficial. A first step in better understanding these effects is to refine the avalanche breakdown model to be more representative of the actual avalanche activity in the Fujitsu FLM 7177-5 test device used in this research. It is suggested that the experimental configuration used in this research be employed in making measurements of avalanche breakdown activity of the device under varying dc and temperature conditions. Since these measurements would be conducted under dc conditions, reverse gate current could be used as an indication of breakdown activity. In addition, concurrent collection of light emission data would help correlate the two indicators (reverse gate current and light emission) of breakdown activity. For these measurements, a method for non-destructively removing the device's lid must be utilized. Removing the lid and calibrating the photo-multiplier tube would allow absolute measurements of light intensity for comparison to reverse gate current. Once refined to best represent this new data, the model can be compared to test results from other device designs to determine if it is applicable to MESFETs in general. However, even if it is only representative of the Fujitsu FLM 7177-5, it still may be useful in analyzing the effects of avalanche breakdown on the reliability of the device.

Device Reliability. It is important to understand that even though avalanche multiplication was not adequately tested by the General Electric Corporation or Jet Propulsion Laboratory accelerated life test programs, it may not detrimentally effect reliability. The fact that this particular failure mechanism was not tested only means its contribution is unknown. It might have no significant effect on reliability since other failure mechanisms may dominate reliability at all temperatures. However, its effect on reliability should be addressed. Of course, this could be done with long term life tests under normal operating conditions to determine the prevalent failure mechanisms. But, this would require many years of testing. Another possible method of addressing the reliability impact of avalanche breakdown is by analysis. For example, it may be possible to develop a physical-failure model of the avalanche breakdown process in the device. Once the physical-failure model exists it can be compared by analysis to the avalanche breakdown process in similar devices. The GaAs Schottky-barrier IMPATT diode which operates at large reverse avalanche breakdown currents is a device similar to the GaAs MESFET with much longer field operating experience. With an accurate physical-failure model, an analysis, by comparison to the IMPATT diode, of the reliability impact of avalanche breakdown on the overall reliability of the Fujitsu FLM 7177-5 may be possible. A first step in developing this accurate physical-failure model is the additional testing suggested above. Lastly, a possible method would be to test the devices by accelerating avalanche multiplication through changes in parameters other than temperature. If a stress type is identified to controllably accelerate avalanche breakdown, this would provide the highest degree of confidence in the results because it would be based on test data of the actual device concerned. Since avalanche breakdown is dependent on voltage, accelerated voltage life testing is recommended. However, if this method is used, care must be taken to assure that increased voltages, and the resulting increased currents, do not accelerate other failure mechanisms at a higher rate than avalanche multiplication. Regardless of what method is chosen, the effects on MTTF predictions of avalanche multiplication should be addressed prior to incorporating these GaAs MESFETs into high reliability applications such as satellite systems.

Appendix A. Test Data

This appendix contains tabular listings of the experimental data collected during this investigation. Tables A.1 through A.4 display the data collected at the baseplate temperature set points of 45, 110, 145, and 168 °C respectively. This data was collected at the standard bias values of $V_{GS} = -1.15$ V and $V_{DS} = 8.50$ V . Tables A.5 through A.8 list similar data collected at bias voltages of $V_{GS} = -1.15$ V and $V_{DS} = 9.00$ V . Lastly, Tables A.9 through A.12 list similar data collected at bias voltages of $V_{GS} = -1.20$ V and $V_{DS} = 8.50$ V . These last two sets of data at different bias voltages were not analyzed in this thesis; however, they were collected with the same test configuration and are included for those readers who may be interested in examining bias effects on light emission. Included in all of these tables is the power added efficiency at each data point. This efficiency was calculated using the following equation (20):

$$EFF = 100\ [P_{OUT}/P_{DC}\ (1 - 1/GAIN)] \qquad (A.1)$$

where

EFF = power added efficiency (%)
P_{OUT} = output power (W)
P_{DC} = total dc power to the device (W)
$GAIN$ = rf power gain of the device (W) .

TABLE A.1

EXPERIMENTAL RESULTS AT STANDARD BIASES AND A CONTROL TEMPERATURE OF 45 °C

DRAIN VOLTAGE = 8.50 V GATE VOLTAGE = - 1.15 V

THERMAL RESISTANCE = 3.52 °C/W

GATE CURRENT (mA)	DRAIN CURRENT (A)	DC POWER (W)	GAIN (dB)	EFF (%)	INPUT POWER (dBm)	OUTPUT POWER (dBm)	BASE TEMP (°C)	CHANNEL TEMP (°C)	LIGHT CURRENT (mA)
0.02	1.48	12.58	7.45	0.26	8.50	15.95	44.3	89.0	0.064
0.01	1.49	12.67	7.40	1.58	16.50	23.90	44.6	88.5	0.111
- 0.02	1.50	12.75	7.39	3.94	20.00	27.39	44.4	87.5	0.132
- 0.15	1.51	12.83	7.32	7.67	23.50	30.62	44.1	85.9	0.324
- 0.26	1.52	12.92	7.23	9.35	24.50	31.73	45.8	87.0	0.512
- 0.50	1.53	13.00	7.15	11.43	25.50	32.65	44.5	85.0	1.20
- 0.90	1.54	13.09	7.01	13.73	26.50	33.51	45.3	85.0	1.91
- 1.80	1.56	13.26	6.83	16.20	27.50	34.33	44.9	84.0	4.01
- 2.42	1.57	13.34	6.68	17.29	28.00	34.68	46.3	85.1	5.41
- 3.36	1.58	13.43	6.54	18.50	28.50	35.04	44.6	83.1	8.10
- 4.91	1.60	13.59	6.33	19.25	29.00	35.33	44.9	83.5	11.5
- 6.13	1.62	13.76	6.14	20.11	29.50	35.64	45.5	84.2	15.6
- 8.17	1.63	13.85	5.90	20.58	30.00	35.90	44.3	82.9	20.8
- 9.37	1.64	13.93	5.78	21.17	30.25	36.03	45.5	84.1	23.8
-10.7	1.64	13.93	5.63	21.39	30.50	36.13	45.1	85.2	27.7
-12.0	1.65	14.01	5.50	21.61	30.75	36.25	45.7	84.4	32.2
-13.1	1.66	14.09	5.34	21.61	31.00	36.34	44.0	82.9	36.0
-13.9	1.65	14.01	5.15	21.64	31.25	36.40	45.7	84.3	39.7
-14.2	1.66	14.09	4.98	21.53	31.50	36.48	44.5	83.4	44.0
-13.1	1.65	14.01	4.78	21.42	31.75	36.53	45.1	83.8	48.2
-10.5	1.65	14.01	4.59	21.23	32.00	36.59	45.6	84.5	51.3
- 6.31	1.65	14.02	4.38	20.86	32.25	36.63	44.3	83.4	56.0
- 0.45	1.64	13.94	4.14	20.34	32.50	36.64	44.9	84.0	59.2
6.40	1.64	13.95	3.92	19.90	32.75	36.67	46.0	85.4	61.5
17.4	1.65	14.05	3.71	19.17	33.00	36.71	44.7	84.7	63.0

TABLE A.2

EXPERIMENTAL RESULTS AT STANDARD BIASES AND A CONTROL TEMPERATURE OF 110 °C

DRAIN VOLTAGE = 8.50 V GATE VOLTAGE = - 1.15 V

THERMAL RESISTANCE = 4.24 °C/W

GATE CURRENT (mA)	DRAIN CURRENT (A)	DC POWER (W)	GAIN (dB)	EFF (%)	INPUT POWER (dBm)	OUTPUT POWER (dBm)	BASE TEMP (°C)	CHANNEL TEMP (°C)	LIGHT CURRENT (nA)
- 0.09	1.50	12.75	5.31	0.13	8.50	13.81	111.4	165.4	0.086
- 0.09	1.50	12.75	5.29	0.42	13.50	18.79	110.4	164.2	0.087
- 0.08	1.50	12.75	5.27	0.83	16.50	21.77	109.1	162.7	0.089
- 0.09	1.50	12.75	5.21	1.29	18.50	23.71	111.6	165.0	0.092
- 0.09	1.49	12.67	5.15	2.01	20.50	25.65	110.6	163.2	0.095
- 0.09	1.49	12.67	5.13	2.52	21.50	26.63	109.5	161.8	0.097
- 0.09	1.49	12.67	5.04	3.08	22.50	27.54	111.2	163.2	0.105
- 0.10	1.48	12.58	5.00	3.85	23.50	28.50	109.3	160.6	0.110
- 0.11	1.48	12.58	4.95	4.25	24.00	28.95	108.5	159.6	0.112
- 0.12	1.48	12.58	4.86	4.62	24.50	29.36	110.8	161.7	0.118
- 0.12	1.47	12.50	4.81	5.13	25.00	29.81	109.2	159.5	0.122
- 0.14	1.47	12.50	4.73	5.60	25.50	30.23	109.6	159.6	0.132
- 0.15	1.46	12.41	4.65	6.15	26.00	30.65	109.8	159.2	0.142
- 0.17	1.46	12.41	4.63	6.47	26.25	30.88	108.1	157.3	0.150
- 0.19	1.45	12.33	4.55	6.71	26.50	31.05	109.9	158.7	0.158
- 0.19	1.45	12.33	4.52	7.03	26.75	31.27	107.8	156.4	0.168
- 0.21	1.45	12.33	4.44	7.24	27.00	31.44	110.1	158.6	0.180
- 0.22	1.45	12.33	4.40	7.56	27.25	31.65	108.3	156.6	0.192
- 0.25	1.44	12.24	4.33	7.86	27.50	31.83	109.8	157.6	0.213
- 0.25	1.44	12.24	4.26	8.11	27.75	32.01	109.4	157.1	0.239
- 0.30	1.44	12.24	4.21	8.43	28.00	32.21	107.5	155.0	0.265
- 0.33	1.43	12.16	4.11	8.67	28.25	32.36	109.9	157.0	0.295
- 0.36	1.43	12.16	4.04	8.94	28.50	32.54	108.2	155.1	0.340
- 0.41	1.43	12.16	3.98	9.15	28.70	32.68	108.5	155.3	0.385
- 0.44	1.43	12.16	3.91	9.33	28.90	32.81	108.6	155.3	0.420
- 0.49	1.43	12.16	3.85	9.54	29.10	32.95	108.0	154.6	0.475
- 0.54	1.43	12.16	3.74	9.56	29.30	33.04	109.6	156.2	0.535
- 0.58	1.43	12.16	3.67	9.74	29.50	33.17	107.8	154.3	0.618
- 0.63	1.42	12.07	3.57	9.86	29.70	33.27	109.6	155.7	0.695
- 0.68	1.42	12.07	3.49	9.99	29.90	33.39	107.9	154.0	0.800
- 0.72	1.42	12.07	3.39	10.03	30.10	33.49	109.3	155.3	0.925
- 0.73	1.42	12.07	3.30	10.10	30.30	33.60	107.7	153.7	1.12
- 0.69	1.41	11.99	3.18	10.11	30.50	33.68	109.5	155.2	1.24

TABLE A.2

(Continued from Previous Page)

GATE CURRENT (mA)	DRAIN CURRENT (A)	DC POWER (W)	GAIN (dB)	EFF (%)	INPUT POWER (dBm)	OUTPUT POWER (dBm)	BASE TEMP (°C)	CHANNEL TEMP (°C)	LIGHT CURRENT (mA)
- 0.63	1.41	11.99	3.10	10.21	30.70	33.80	109.4	155.0	1.50
- 0.36	1.41	11.99	3.00	10.22	30.90	33.90	108.1	153.7	1.68
0.02	1.40	11.90	2.88	10.19	31.10	33.98	108.0	153.3	1.95
0.45	1.40	11.90	2.81	10.08	31.20	34.01	109.3	154.7	2.12
0.80	1.40	11.90	2.76	10.07	31.30	34.06	107.1	152.5	2.28
1.30	1.40	11.90	2.67	9.85	31.40	34.07	109.4	154.9	2.50
1.80	1.40	11.90	2.64	9.93	31.50	34.14	107.0	152.4	2.72
2.70	1.39	11.81	2.56	9.83	31.60	34.16	109.3	154.5	2.78

TABLE A.3

EXPERIMENTAL RESULTS AT STANDARD BIASES AND A CONTROL TEMPERATURE OF 145 °C

DRAIN VOLTAGE = 8.50 V GATE VOLTAGE = - 1.15 V

THERMAL RESISTANCE = 4.64 °C/W

GATE CURRENT (mA)	DRAIN CURRENT (A)	DC POWER (W)	GAIN (dB)	EFF (%)	INPUT POWER (dBm)	OUTPUT POWER (dBm)	BASE TEMP (°C)	CHANNEL TEMP (°C)	LIGHT CURRENT (mA)
- 0.48	1.51	12.84	5.17	0.13	8.50	13.67	147.5	207.0	0.113
- 0.42	1.50	12.75	5.11	0.79	16.50	21.61	144.9	203.6	0.119
- 0.47	1.50	12.75	4.96	1.88	20.50	25.46	146.7	204.8	0.131
- 0.47	1.48	12.58	4.83	3.63	23.50	28.33	147.9	204.2	0.149
- 0.47	1.46	12.41	4.71	4.45	24.50	29.21	149.0	204.0	0.162
- 0.47	1.45	12.33	4.54	5.31	25.50	30.04	144.5	198.7	0.178
- 0.54	1.44	12.24	4.40	6.40	26.50	30.90	147.4	200.6	0.212
- 0.58	1.42	12.07	4.20	7.59	27.50	31.70	142.3	194.1	0.273
- 0.68	1.41	11.99	4.06	8.14	28.00	32.06	147.1	198.2	0.335
- 0.71	1.40	11.90	3.91	8.69	28.50	32.41	143.0	193.4	0.405
- 0.82	1.39	11.82	3.76	9.26	29.00	32.76	146.5	196.3	0.520
- 0.94	1.33	11.73	3.56	9.65	29.50	33.06	144.5	193.7	0.658
- 1.02	1.38	11.73	3.46	9.80	29.75	33.21	146.5	195.6	0.755
- 1.07	1.38	11.73	3.35	9.91	30.00	33.35	144.0	193.0	0.890
- 1.12	1.37	11.65	3.30	10.35	30.25	33.55	145.0	193.4	1.05
- 1.06	1.37	11.65	3.17	10.36	30.50	33.67	141.7	190.1	1.25
- 0.97	1.36	11.56	3.04	10.30	30.70	33.74	144.5	192.6	1.41
- 0.78	1.36	11.56	2.94	10.30	30.90	33.84	146.3	194.4	1.57
- 0.36	1.35	11.48	2.84	10.36	31.10	33.94	143.4	191.1	1.82
0.40	1.35	11.47	2.78	10.54	31.30	34.08	144.8	192.4	2.05
1.75	1.34	11.39	2.60	10.17	31.50	34.10	145.0	192.5	2.30
2.30	1.34	11.39	2.59	10.35	31.60	34.19	145.0	192.4	2.45
3.00	1.34	11.39	2.50	10.11	31.70	34.20	144.6	192.1	2.60
4.10	1.34	11.39	2.48	10.24	31.80	34.28	145.0	192.4	2.82

TABLE A.4

EXPERIMENTAL RESULTS AT STANDARD BIASES AND A CONTROL TEMPERATURE OF 168 °C

DRAIN VOLTAGE = 8.50 V GATE VOLTAGE = - 1.15 V

THERMAL RESISTANCE = 4.84 °C/W

GATE CURRENT (mA)	DRAIN CURRENT (A)	DC POWER (W)	GAIN (dB)	EFF (%)	INPUT POWER (dBm)	OUTPUT POWER (dBm)	BASE TEMP (°C)	CHANNEL TEMP (°C)	LIGHT CURRENT (mA)
- 0.83	1.54	13.09	4.85	0.11	8.50	13.35	165.0	228.3	0.118
- 0.86	1.54	13.09	4.82	0.69	16.50	21.32	165.3	228.2	0.128
- 0.90	1.53	13.01	4.75	1.71	20.50	25.25	164.5	226.4	0.149
- 0.98	1.52	12.92	4.67	3.35	23.50	28.17	165.2	225.6	0.196
- 1.00	1.51	12.84	4.59	4.12	24.50	29.09	164.5	224.1	0.229
- 1.09	1.51	12.84	4.51	5.64	25.50	30.01	164.7	223.7	0.284
- 1.20	1.50	12.75	4.42	6.19	26.50	30.92	163.0	220.9	0.393
- 1.46	1.49	12.67	4.20	7.24	27.50	31.70	167.7	224.6	0.562
- 1.59	1.48	12.58	4.11	8.02	28.00	32.15	166.9	222.9	0.720
- 1.74	1.47	12.50	4.05	8.73	28.50	32.55	167.0	222.2	0.920
- 2.00	1.46	12.41	3.91	9.35	29.00	32.91	168.0	222.5	1.23
2.29	1.45	12.33	3.75	9.91	29.50	33.25	168.0	221.8	1.65
- 2.64	1.44	12.24	3.60	10.54	30.00	33.60	168.0	221.0	2.16
- 2.89	1.43	12.16	3.49	10.75	30.25	33.74	169.0	221.5	2.50
- 3.07	1.43	12.16	3.40	10.96	30.50	33.90	169.0	221.4	2.92
- 3.34	1.42	12.07	3.28	11.10	30.75	34.03	170.0	221.9	3.65
- 3.46	1.42	12.07	3.17	11.21	31.00	34.17	170.0	221.9	4.22
- 3.51	1.41	11.99	3.05	11.33	31.25	34.30	170.0	221.5	4.95
- 3.25	1.41	11.99	2.93	11.35	31.50	34.43	170.0	221.4	5.75
- 2.68	1.40	11.90	2.79	11.33	31.75	34.54	170.0	221.1	6.75
- 1.54	1.39	11.82	2.65	11.28	32.00	34.65	171.0	221.7	7.82
- 0.11	1.39	11.82	2.54	11.16	32.20	34.74	171.0	221.8	9.12
2.25	1.38	11.73	2.42	11.65	32.40	34.82	171.0	221.5	10.8
4.60	1.38	11.72	2.28	10.72	32.60	34.88	171.0	221.7	11.9
8.00	1.37	11.64	2.13	10.37	32.80	34.93	172.0	222.5	13.2
13.6	1.37	11.63	1.97	9.85	33.00	34.97	173.0	223.7	14.2

TABLE A.5

EXPERIMENTAL RESULTS AT AN INCREASED DRAIN BIAS AND A CONTROL TEMPERATURE OF 45 °C

DRAIN VOLTAGE = 9.00 V GATE VOLTAGE = - 1.15 V

THERMAL RESISTANCE = 3.52 °C/W

GATE CURRENT (mA)	DRAIN CURRENT (A)	DC POWER (W)	GAIN (dB)	EFF (%)	INPUT POWER (dBm)	OUTPUT POWER (dBm)	BASE TEMP (°C)	CHANNEL TEMP (°C)	LIGHT CURRENT (nA)
0.01	1.50	13.50	7.30	0.23	8.50	15.80	46.6	94.0	0.111
0.00	1.50	13.50	7.32	1.45	16.50	23.82	45.8	92.6	0.125
- 0.02	1.51	13.59	7.30	5.61	20.50	27.80	45.5	91.6	0.169
- 0.15	1.53	13.77	7.24	6.99	23.00	30.24	45.2	90.3	0.350
- 0.26	1.53	13.77	7.19	8.57	24.50	31.69	44.9	89.2	0.578
- 0.48	1.54	13.86	7.10	10.57	25.50	32.60	44.6	88.2	1.05
- 0.91	1.56	14.04	6.96	12.42	26.50	33.46	44.3	87.5	1.95
- 1.84	1.57	14.13	6.78	14.[illegible]	27.50	34.28	44.1	86.4	4.22
- 2.52	1.58	14.22	6.62	15.94	28.00	34.62	46.5	88.6	5.75
- 3.14	1.60	14.40	6.49	17.[illegible]	28.50	34.99	45.0	87.1	8.45
- 4.86	1.61	14.49	6.33	18.57	29.00	35.33	44.3	86.1	12.2
- 6.45	1.63	14.66	6.12	[illegible]	29.50	35.62	46.2	88.1	16.1
- 8.54	1.65	14.84	5.88	19.[illegible]	30.00	35.88	45.2	87.3	21.8
- 9.78	1.65	14.93	5.78	[illegible]	30.25	36.03	44.1	86.3	25.0
-11.3	1.66	14.93	5.61	19.[illegible]	30.50	36.11	45.5	87.4	28.1
-12.7	1.67	15.02	5.48	20.40	30.75	36.23	46.0	88.3	34.0
-14.1	1.67	15.01	5.34	[illegible]	31.00	36.34	44.9	87.0	38.0
-16.9	1.67	15.01	5.18	20.[illegible]	31.25	36.43	44.4	86.5	42.2
-15.2	1.67	15.01	4.98	20.11	31.50	36.48	45.6	87.8	46.2
-14.8	1.67	15.01	4.81	20.20	31.75	36.56	44.7	86.9	50.3
-13.0	1.67	15.02	4.60	19.85	32.00	36.60	46.0	88.3	54.0
-10.0	1.67	15.02	4.40	19.61	32.25	36.65	45.0	87.5	59.5
- 3.80	1.68	15.12	4.20	19.13	32.50	36.70	44.4	87.4	64.0
2.30	1.67	15.03	3.97	[illegible]	32.75	36.72	44.2	87.2	68.3
8.40	1.66	14.95	3.74	18.[illegible]	33.00	36.74	45.0	88.0	[illegible]

TABLE A.6

EXPERIMENTAL RESULTS AT AN INCREASED DRAIN BIAS AND A CONTROL TEMPERATURE OF 110 °C

DRAIN VOLTAGE = 9.00 V GATE VOLTAGE = - 1.15 V

THERMAL RESISTANCE = 4.24 °C/W

GATE CURRENT (mA)	DRAIN CURRENT (A)	DC POWER (W)	GAIN (dB)	EFF (%)	INPUT POWER (dBm)	OUTPUT POWER (dBm)	BASE TEMP (°C)	CHANNEL TEMP (°C)	LIGHT CURRENT (mA)
- 0.13	1.52	13.68	5.19	0.12	8.50	13.69	113.3	171.2	0.112
- 0.13	1.51	13.59	5.13	0.30	12.50	17.63	113.2	170.7	0.112
- 0.13	1.51	13.59	5.05	1.15	18.50	23.55	113.0	170.0	0.118
- 0.13	1.51	13.59	5.00	1.79	20.50	25.50	112.8	169.4	0.122
- 0.14	1.50	13.50	4.89	2.74	22.50	27.39	113.4	169.1	0.129
- 0.15	1.50	13.50	4.81	3.36	23.50	28.31	113.0	168.3	0.135
- 0.16	1.49	13.41	4.72	4.13	24.50	29.22	112.4	166.9	0.142
- 0.18	1.48	13.32	4.60	5.02	25.50	30.10	111.8	165.4	0.158
- 0.22	1.47	13.23	4.45	6.03	26.50	30.95	110.5	163.2	0.187
- 0.24	1.47	13.23	4.34	6.50	27.00	31.34	109.7	162.1	0.208
- 0.28	1.46	13.14	4.26	7.13	27.50	31.76	109.0	160.7	0.244
- 0.36	1.45	13.05	4.10	7.59	28.00	32.10	111.5	162.6	0.298
- 0.40	1.45	13.05	3.96	8.08	28.50	32.46	110.7	161.6	0.375
- 0.52	1.44	12.96	3.79	8.54	29.00	32.79	109.0	159.3	0.505
- 0.66	1.44	12.96	3.60	8.88	29.50	33.10	108.7	158.8	0.682
- 0.71	1.44	12.96	3.47	8.81	29.70	33.17	110.6	160.7	0.770
- 0.78	1.44	12.96	3.41	8.99	29.90	33.31	108.5	158.5	0.885
- 0.81	1.43	12.87	3.31	9.09	30.10	33.41	110.7	160.3	1.03
- 0.71	1.44	12.96	3.24	9.17	30.30	33.54	108.5	158.4	1.15
- 0.90	1.43	12.87	3.15	9.29	30.50	33.65	108.7	158.2	1.46
- 0.40	1.43	12.87	2.83	9.20	31.10	33.93	109.0	158.6	2.25
1.40	1.42	12.78	2.62	9.15	31.50	34.12	110.0	159.2	3.00
2.80	1.40	12.60	2.46	9.05	31.75	34.21	107.9	156.5	3.80
5.28	1.40	12.59	2.31	8.64	32.00	34.31	109.8	158.5	4.60
10.65	1.39	12.50	2.14	8.55	32.25	34.39	109.0	157.5	5.20

TABLE A.7

EXPERIMENTAL RESULTS AT AN INCREASED DRAIN BIAS AND A CONTROL TEMPERATURE OF 145 °C

DRAIN VOLTAGE = 9.00 V GATE VOLTAGE = - 1.15 V

THERMAL RESISTANCE = 4.64 °C/W

GATE CURRENT (mA)	DRAIN CURRENT (A)	DC POWER (W)	GAIN (dB)	EFF (%)	INPUT POWER (dBm)	OUTPUT POWER (dBm)	BASE TEMP (°C)	CHANNEL TEMP (°C)	LIGHT CURRENT (nA)
- 0.47	1.53	13.77	4.92	0.11	8.50	13.42	143.0	206.8	0.142
- 0.50	1.53	13.77	4.35	0.56	16.50	20.85	143.6	207.1	0.158
- 0.52	1.52	13.68	4.49	1.49	20.50	24.99	143.1	205.6	0.179
- 0.60	1.51	13.59	4.52	3.02	23.50	28.02	144.0	205.2	0.276
- 0.66	1.50	13.50	4.97	4.47	24.50	29.47	144.5	204.3	0.330
- 0.73	1.50	13.50	4.51	4.80	25.50	30.01	145.0	204.6	0.362
- 0.85	1.48	13.32	4.50	6.10	26.50	31.00	145.4	203.4	0.476
- 1.07	1.47	13.23	4.45	7.59	27.50	31.95	146.5	203.2	0.704
- 1.24	1.47	13.23	4.35	8.21	28.00	32.35	147.5	203.9	0.824
- 1.45	1.46	13.14	4.22	8.85	28.50	32.72	148.5	204.1	1.14
- 1.71	1.46	13.14	4.04	9.28	29.00	33.04	150.0	205.3	1.45
- 2.00	1.45	13.05	3.93	10.05	29.50	33.43	148.4	202.9	1.92
- 2.45	1.45	13.05	3.75	10.51	30.00	33.75	149.0	203.2	2.62
- 2.72	1.45	13.05	3.65	10.69	30.25	33.90	149.0	203.1	3.25
- 3.07	1.44	12.96	3.56	10.99	30.50	34.06	150.0	203.5	3.87
- 3.42	1.44	12.96	3.46	11.17	30.75	34.21	150.0	203.4	4.65
- 3.80	1.43	12.87	3.34	11.32	31.00	34.34	150.0	203.0	5.65
- 4.04	1.43	12.87	3.21	11.33	31.25	34.46	150.0	203.0	6.62
- 4.13	1.43	12.87	3.08	11.33	31.50	34.58	150.0	203.0	7.72
- 4.05	1.43	12.87	2.96	11.35	31.75	34.71	150.0	203.0	10.2
- 3.35	1.42	12.78	2.81	11.28	32.00	34.81	150.0	202.6	11.4
- 2.20	1.42	12.78	2.69	11.14	32.20	34.89	150.0	202.7	13.2
0.15	1.41	12.69	2.55	10.94	32.40	34.95	151.5	203.9	14.7
2.20	1.41	12.69	2.43	10.75	32.60	35.03	151.0	203.5	16.2
7.33	1.41	12.68	2.27	10.32	32.80	35.07	151.5	204.3	17.5
10.7	1.41	12.68	2.13	9.96	33.00	35.13	151.0	204.0	19.2

TABLE A.8

EXPERIMENTAL RESULTS AT AN INCREASED DRAIN BIAS AND A CONTROL TEMPERATURE OF 168 °C

DRAIN VOLTAGE = 9.00 V GATE VOLTAGE = - 1.15 V

THERMAL RESISTANCE = 4.84 °C/W

GATE CURRENT (mA)	DRAIN CURRENT (A)	DC POWER (W)	GAIN (dB)	EFF (%)	INPUT POWER (dBm)	OUTPUT POWER (dBm)	BASE TEMP (°C)	CHANNEL TEMP (°C)	LIGHT CURRENT (nA)
- 1.11	1.55	13.95	4.76	0.10	8.50	13.26	165.0	232.5	0.182
- 1.08	1.54	13.86	4.72	0.63	16.50	21.22	165.0	231.7	0.196
- 1.12	1.54	13.86	4.71	1.58	20.50	25.21	165.0	231.0	0.231
- 1.26	1.53	13.77	4.60	3.06	23.50	28.10	167.0	231.6	0.323
- 1.36	1.52	13.68	4.51	3.76	24.50	29.01	168.0	231.7	0.382
- 1.44	1.51	13.59	4.44	4.65	25.50	29.94	168.0	230.7	0.473
- 1.61	1.50	13.50	4.31	5.62	26.50	30.81	169.0	230.7	0.610
- 1.89	1.49	13.41	4.18	6.78	27.50	31.68	170.0	230.5	0.870
- 2.03	1.48	13.32	4.08	7.38	28.00	32.08	170.0	229.7	1.12
- 2.30	1.48	13.32	3.96	7.91	28.50	32.46	171.0	230.4	1.38
- 2.62	1.47	13.23	3.83	8.50	29.00	32.83	172.0	230.6	1.73
- 2.99	1.46	13.14	3.68	9.04	29.50	33.18	171.0	228.9	2.32
- 3.40	1.45	13.05	3.54	9.65	30.00	33.54	170.0	227.1	3.26
- 3.69	1.44	12.96	3.46	9.95	30.25	33.71	170.0	226.5	3.75
- 4.01	1.44	12.96	3.37	10.15	30.50	33.87	170.0	226.4	4.30
- 4.33	1.43	12.87	3.27	10.37	30.75	34.02	170.0	225.9	5.02
- 4.66	1.43	12.88	3.16	10.46	31.00	34.16	170.0	225.8	5.83
- 4.94	1.42	12.79	3.04	10.57	31.25	34.29	171.0	226.3	6.82
- 4.93	1.42	12.79	2.93	10.64	31.50	34.43	171.0	226.3	8.02
- 4.65	1.41	12.70	2.80	10.67	31.75	34.55	171.0	225.9	9.22
- 3.84	1.41	12.69	2.67	10.60	32.00	34.67	171.0	225.9	11.2
- 2.66	1.40	12.60	2.56	10.57	32.20	34.76	171.0	225.5	12.8
- 1.60	1.40	12.60	2.43	10.34	32.40	34.83	172.0	226.7	14.2
0.70	1.39	12.51	2.30	10.16	32.60	34.90	172.0	226.4	15.0
5.00	1.38	12.41	2.15	9.83	32.80	34.95	173.0	227.2	17.2
8.70	1.38	12.41	2.02	9.52	33.00	35.02	173.0	227.3	19.2

TABLE A.9

EXPERIMENTAL RESULTS AT A DECREASED GATE BIAS AND A CONTROL TEMPERATURE OF 45 °C

DRAIN VOLTAGE = 8.50 V GATE VOLTAGE = - 1.20 V

THERMAL RESISTANCE = 3.52 °C/W

GATE CURRENT (mA)	DRAIN CURRENT (A)	DC POWER (W)	GAIN (dB)	EFF (%)	INPUT POWER (dBm)	OUTPUT POWER (dBm)	BASE TEMP (°C)	CHANNEL TEMP (°C)	LIGHT CURRENT (nA)
0.01	1.43	12.16	7.46	0.27	8.50	15.96	45.0	87.7	0.083
0.00	1.43	12.16	7.40	1.65	16.50	23.90	44.5	86.6	0.096
- 0.04	1.44	12.24	7.35	4.06	20.50	27.85	45.7	87.0	0.161
- 0.21	1.46	12.41	7.28	7.84	23.50	30.78	45.5	85.8	0.475
- 0.38	1.47	12.49	7.23	9.66	24.50	31.73	44.8	84.5	0.750
- 0.66	1.48	12.58	7.13	11.75	25.50	32.63	45.4	84.5	1.42
- 1.25	1.50	12.75	7.01	14.10	26.50	33.51	44.5	83.0	2.71
- 2.26	1.52	12.92	6.77	16.34	27.50	34.27	44.6	82.6	5.30
- 3.18	1.54	13.09	6.72	17.83	28.00	34.72	44.4	82.2	7.70
- 4.22	1.55	13.17	6.51	18.69	28.50	35.01	45.2	82.9	10.5
- 5.55	1.57	13.34	6.34	19.68	29.00	35.34	45.5	83.2	13.6
- 7.24	1.58	13.42	6.10	20.41	29.50	35.60	46.4	84.0	17.2
- 9.28	1.61	13.67	5.90	21.14	30.00	35.90	44.5	82.5	23.3
-10.6	1.61	13.67	5.74	21.30	30.25	35.99	46.4	84.3	25.8
-11.9	1.62	13.76	5.61	21.53	30.50	36.11	44.7	82.7	32.0
-13.2	1.63	13.84	5.49	21.81	30.75	36.24	44.6	82.7	34.2
-14.5	1.63	13.84	5.32	21.87	31.00	36.32	46.4	84.5	37.0
-15.6	1.63	13.84	5.12	21.69	31.25	36.37	46.4	84.5	41.0
-16.0	1.63	13.84	4.97	21.85	31.50	36.47	44.7	82.8	46.5
-15.8	1.63	13.84	5.13	24.42	31.75	36.88	46.3	83.1	48.2
-14.5	1.63	13.84	4.57	21.35	32.00	36.57	44.5	82.8	53.5
-12.1	1.63	13.84	4.35	20.90	32.25	36.60	45.5	85.0	58.0
- 7.50	1.63	13.85	4.15	20.55	32.50	36.65	45.2	83.9	62.5
- 1.00	1.63	13.85	3.92	19.93	32.75	36.67	46.3	85.3	66.2
6.70	1.62	13.78	3.68	19.31	33.00	36.68	44.5	83.6	71.0

TABLE A.10

EXPERIMENTAL RESULTS AT A DECREASED GATE BIAS AND A CONTROL TEMPERATURE OF 110 °C

DRAIN VOLTAGE = 8.50 V GATE VOLTAGE = - 1.20 V

THERMAL RESISTANCE = 4.24 °C/W

GATE CURRENT (mA)	DRAIN CURRENT (A)	DC POWER (W)	GAIN (dB)	EFF (%)	INPUT POWER (dBm)	OUTPUT POWER (dBm)	BASE TEMP (°C)	CHANNEL TEMP (°C)	LIGHT CURRENT (nA)
- 0.09	1.45	12.32	6.70	0.21	8.50	15.20	110.9	163.0	0.103
- 0.10	1.45	12.32	6.81	1.38	16.50	23.31	109.0	160.5	0.112
- 0.13	1.44	12.24	6.65	3.32	20.50	27.15	110.0	160.2	0.141
- 0.22	1.44	12.24	6.62	6.57	23.50	30.12	108.3	156.8	0.224
- 0.30	1.43	12.15	6.51	8.06	24.50	31.01	109.6	157.0	0.320
- 0.42	1.43	12.15	6.30	9.53	25.50	31.80	109.8	156.4	0.442
- 0.68	1.42	12.07	6.22	11.80	26.50	32.72	108.4	153.5	0.782
- 1.07	1.41	11.98	5.89	13.52	27.50	33.39	109.7	153.6	1.38
- 1.40	1.41	11.98	5.76	14.57	28.00	33.76	108.3	151.7	1.91
- 1.85	1.41	11.98	5.60	15.54	28.50	34.10	109.3	152.2	2.80
- 2.54	1.41	11.98	5.42	16.46	29.00	34.42	109.0	151.4	4.10
- 3.55	1.41	11.98	5.23	17.36	29.50	34.73	108.8	150.8	6.08
- 4.70	1.42	12.06	5.02	18.04	30.00	35.02	108.5	150.4	8.50
- 5.20	1.42	12.06	4.87	18.17	30.25	35.12	108.5	150.4	10.3
- 6.20	1.42	12.06	4.77	18.60	30.50	35.27	108.0	149.6	12.0
- 7.07	1.42	12.06	4.62	18.70	30.75	35.37	109.3	150.9	14.8
- 7.89	1.42	12.06	4.49	18.91	31.00	35.49	109.4	150.9	17.2
- 8.22	1.42	12.06	4.34	18.93	31.25	35.59	108.3	149.7	19.4
- 7.92	1.42	12.06	4.18	18.95	31.50	35.68	109.3	150.7	22.8
- 6.67	1.42	12.06	4.02	18.90	31.75	35.77	108.3	149.8	25.8
- 4.23	1.41	11.98	3.82	18.65	32.00	35.82	109.1	150.4	30.0
0.50	1.42	12.07	3.63	18.17	32.25	35.88	107.5	149.4	32.5
5.00	1.41	11.99	3.42	17.76	32.50	35.92	109.0	150.8	34.5
13.5	1.40	11.92	3.20	17.22	32.75	35.95	109.7	151.5	37.5

TABLE A.11

EXPERIMENTAL RESULTS AT A DECREASED GATE BIAS AND A CONTROL TEMPERATURE OF 145 °C

DRAIN VOLTAGE = 8.50 V GATE VOLTAGE = - 1.20 V

THERMAL RESISTANCE = 4.64 °C/W

GATE CURRENT (mA)	DRAIN CURRENT (A)	DC POWER (W)	GAIN (dB)	EFF (%)	INPUT POWER (dBm)	OUTPUT POWER (dBm)	BASE TEMP (°C)	CHANNEL TEMP (°C)	LIGHT CURRENT (nA)
- 0.38	1.47	12.49	6.06	0.17	8.50	14.56	143.8	201.7	0.134
- 0.42	1.46	12.41	6.05	1.09	16.50	22.55	145.7	202.7	0.149
- 0.43	1.46	12.41	6.05	2.74	20.50	26.55	143.3	199.3	0.180
- 0.55	1.45	12.32	5.88	5.22	23.50	29.33	145.4	199.6	0.267
- 0.57	1.44	12.24	5.66	6.17	24.50	30.16	142.8	196.1	0.326
- 0.74	1.44	12.24	5.71	7.90	25.50	31.21	144.3	196.6	0.465
- 0.93	1.43	12.15	5.57	9.58	26.50	32.07	144.0	195.0	0.682
- 1.31	1.41	11.98	5.37	11.47	27.50	32.87	144.2	193.4	1.17
- 1.54	1.40	11.90	5.26	12.50	28.00	33.26	143.1	191.4	1.51
- 1.83	1.40	11.90	5.08	13.22	28.50	33.58	143.9	191.8	1.95
- 2.31	1.40	11.90	4.96	14.24	29.00	33.96	142.0	189.3	2.67
- 2.92	1.39	11.81	4.75	14.93	29.50	34.25	144.0	190.6	3.65
- 3.68	1.39	11.81	4.56	15.73	30.00	34.56	142.0	188.2	5.05
- 4.16	1.39	11.81	4.44	15.96	30.25	34.69	144.0	190.1	5.95
- 4.77	1.38	11.72	4.32	16.31	30.50	34.82	145.0	190.5	7.18
- 5.30	1.39	11.81	4.20	16.41	30.75	34.95	145.0	190.8	8.42
- 5.76	1.38	11.72	4.11	16.93	31.00	35.11	143.5	188.7	9.80
- 6.02	1.38	11.72	3.94	16.81	31.25	35.19	145.0	190.3	11.4
- 5.93	1.38	11.72	3.83	17.06	31.50	35.33	142.5	187.6	13.4
- 5.26	1.38	11.72	3.64	16.75	31.75	35.39	144.7	190.0	15.2
- 3.64	1.37	11.64	3.49	16.80	32.00	35.49	143.0	187.9	17.2
- 0.70	1.37	11.64	3.30	16.41	32.25	35.55	144.7	189.9	19.6
4.31	1.36	11.57	3.16	16.45	32.50	35.66	144.7	189.5	21.6
10.9	1.37	11.66	2.95	15.71	32.75	35.70	144.5	190.1	23.2
19.0	1.36	11.58	2.75	15.22	33.00	35.75	144.5	190.1	25.3

TABLE A.12

EXPERIMENTAL RESULTS AT A DECREASED GATE BIAS AND A CONTROL TEMPERATURE OF 168 °C

DRAIN VOLTAGE = 8.50 V GATE VOLTAGE = - 1.20 V

THERMAL RESISTANCE = 4.84 °C/W

GATE CURRENT (mA)	DRAIN CURRENT (A)	DC POWER (W)	GAIN (dB)	EFF (%)	INPUT POWER (dBm)	OUTPUT POWER (dBm)	BASE TEMP °C)	CHANNEL TEMP (°C)	LIGHT CURRENT (nA)
- 0.85	1.47	12.49	5.80	0.16	8.50	14.30	166.5	226.9	0.200
- 0.87	1.47	12.49	5.81	1.00	16.50	22.31	166.5	226.4	0.221
- 0.94	1.47	12.49	5.75	2.48	20.50	26.25	166.4	225.4	0.278
- 1.08	1.46	12.41	5.61	4.76	23.50	29.11	167.7	224.9	0.423
- 1.19	1.45	12.32	5.51	5.85	24.50	30.01	167.9	224.1	0.543
- 1.33	1.44	12.24	5.42	7.20	25.50	30.92	168.0	223.0	0.742
- 1.63	1.42	12.07	5.26	8.73	26.50	31.76	168.0	221.3	1.08
- 2.08	1.41	11.98	5.08	10.42	27.50	32.58	168.0	220.0	1.69
- 2.33	1.40	11.90	4.99	11.43	28.00	32.99	166.0	217.0	2.12
- 2.80	1.39	11.81	4.81	12.15	28.50	33.31	168.0	218.2	2.72
- 3.27	1.39	11.81	4.69	13.08	29.00	33.69	165.0	215.7	3.65
- 3.93	1.38	11.73	4.49	13.77	29.50	33.99	168.0	216.9	4.73
- 4.83	1.37	11.64	4.29	14.43	30.00	34.29	168.0	216.2	6.13
- 5.27	1.37	11.64	4.20	14.94	30.25	34.45	166.0	214.0	7.17
- 5.83	1.37	11.64	4.07	14.97	30.50	34.57	168.0	215.9	8.20
- 6.40	1.36	11.55	3.95	15.26	30.75	34.70	168.0	215.4	9.80
- 6.91	1.36	11.55	3.83	15.43	31.00	34.83	168.0	215.3	11.1
- 7.40	1.36	11.55	3.69	15.46	31.25	34.94	168.1	215.4	12.8
- 7.45	1.35	11.47	3.58	15.77	31.50	35.08	166.0	212.7	14.4
- 7.15	1.35	11.47	3.42	15.63	31.75	35.17	168.0	214.8	16.2
- 5.94	1.34	11.38	3.28	15.71	32.00	35.28	166.0	212.4	18.2
- 3.05	1.34	11.39	3.08	15.22	32.25	35.33	168.0	214.7	20.0
0.65	1.34	11.39	2.93	15.04	32.50	35.43	168.0	214.8	22.2
4.54	1.34	11.40	2.76	14.68	32.75	35.51	168.0	215.1	24.8
11.4	1.33	11.32	2.56	14.16	33.00	35.56	168.0	215.0	26.5

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This investigation examines temperature effects on avalanche breakdown in GaAs MESFETs to determine if this failure mechanism is accelerated by high temperature life tests. The specific objective is to assess whether the accelerated life test evaluations performed on a GaAs MESFET planned for use in future Defense Satellite Communications System (DSCS) spacecraft have adequately addressed the reliability issues concerning the gate-to-drain avalanche breakdown failure mechanism. This objective was accomplished by adapting an existing analytical model for temperature effects, and using it to predict the variation in avalanche multiplication activity with temperature. To verify this model, it was used to calculate the associated changes in light emissions over temperature which were experimentally validated on one device of the type planned for use by the DSCS program. Once validated, these models were used to evaluate the adequacy of the accelerated temperature life tests. The results of this evaluation indicate that the avalanche breakdown failure mechanism is decelerated with temperature, and therefore, the effects of avalanche breakdown on the reliability of GaAs MESFETs cannot be determined by accelerated temperature life testing.

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