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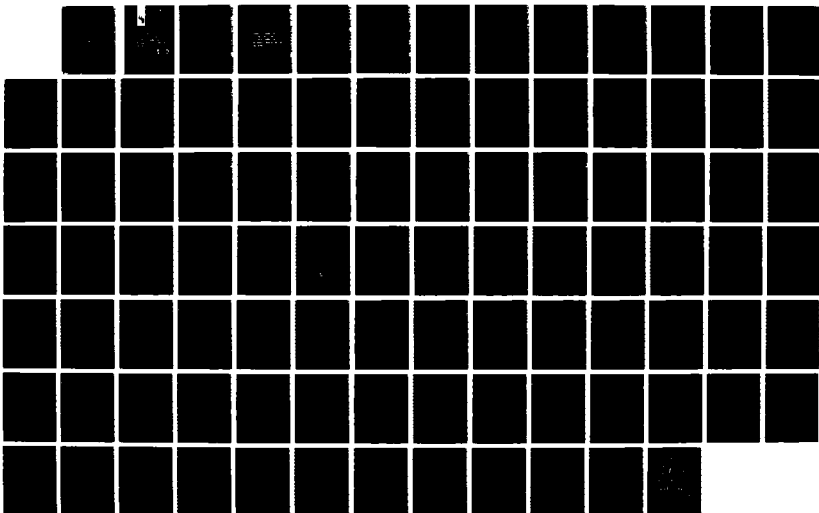
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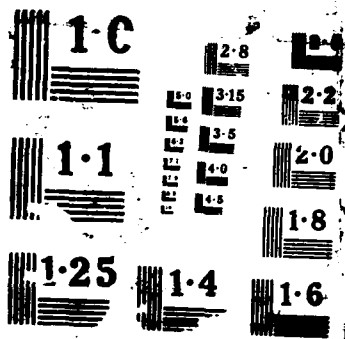
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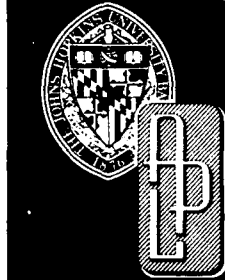


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Technical Memorandum

**ADVANCED PACKAGING FOR
VLSI/VHSIC APPLICATIONS:
ELECTRICAL, THERMAL, AND
MECHANICAL CONSIDERATIONS—AN
IR&D REPORT**

G. V. CLATTERBAUGH
H. K. CHARLES, JR.

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1. INTRODUCTION

The advancement of microelectronics toward more complex and faster device technologies has imposed upon the electronics packaging engineer the challenge of interconnecting any number of these devices together into an integrated hybrid microcircuit without serious degradation in the overall electrical performance of the system. The movement is toward devices that can operate at clock speeds in excess of 100 MHz. For example, present and future requirements for high speed digital signal processors for military and communications applications will require devices with rise times of 3 nsec or less and some as fast as 0.1 nsec (e.g., gallium arsenide). For subnanosecond rise and fall times, properly terminated transmission lines are a requirement. These higher clock speeds and faster rise times will require that propagation delays be minimized, resulting in a need for increased packing density, high conductivity, and low-capacity materials.

With the introduction of very large scale integrated circuits (VLSI), new packaging methods must be developed to meet all the requirements necessary for the efficient and reliable use of these complex device technologies. The increased circuit densities made possible through advanced VLSI semiconductor processing techniques demand that packaging methods be capable of supporting the high I/O and high power dissipation densities of these devices. VLSI devices can have between 1000 and 80,000 logic gates per chip. Three-dimensional multilayer surface mount technologies are essential for accommodating this high I/O requirement. Surface mount packages must be able to support the high I/O number and must possess enhancements for improving their heat transfer characteristics. The reduced feature size of VLSI devices has established the need for higher characteristic line impedance to offset the increase in output driver resistance. In addition, the larger physical size for both the semiconductor die and chip packages will require more rugged attachment materials able to withstand the increased mechanical stresses.

Electronic packaging requirements for the Department of Defense very high speed integrated circuits (VHSIC) program has put even more stringent demands on the electrical, thermal, and mechanical characteristics for device packaging. The primary goal of the VHSIC program is development of very high speed digital processing systems through utilization of advancements in high speed semiconductor device fabrication. Since all devices typically consume more power when

operating at high speeds, VHSIC packaging will require further improvements (over VLSI device packaging) in overall thermal management. The sensitivity of circuit design to the electrical parameters of the package (e.g., capacitance, inductance, resistance, and characteristic impedance) increases with higher frequency operation, introducing such transmission line effects as reflections, crosstalk, and propagation delays. The compatibility with transmission line and high-density interconnections will ultimately mark the necessary requirements for electronic packaging technologies of the future.

The intent of this report is to focus on the electrical characteristics of the most promising VLSI/VHSIC packaging concepts, with emphasis on high reliability applications. Initially, its focus is on the various packaging requirements essential for successfully integrating several VLSI/VHSIC device technologies into modern microcircuit systems. Since the devices themselves dictate the suitability of a particular packaging approach, some of the electrical characteristics of VLSI/VHSIC devices are discussed. The report then shifts its emphasis to the fundamental electrical characterization of device interconnects. Computer aided methods for calculating fundamental high-frequency circuit parameters such as capacitance, inductance, and characteristic impedance are presented. Additional numerical methods are presented for estimation of reflections and crosstalk in substrate wiring boards and device-package interconnections. Computer programs for the analysis of transmission line parameters, reflections, and crosstalk are provided in the appendixes. A brief summary of experimental techniques useful in determining transmission-line parameters (such as characteristic line impedance, line attenuation, phase delay, and insertion loss) is presented, followed by discussion of the most promising packaging concepts for integrating VLSI/VHSIC devices into modern electronic systems. This includes methods for chip-to-package attachment and interconnection, package-to-substrate lead attachment, and substrate wiring interconnects. The multilayer thick-film, ceramic-chip carrier assembly is described for use in high speed, high-circuit-density applications using techniques previously discussed. The report concludes with a discussion of new packaging methods that incorporate all of the fundamental characteristics necessary for integrating VLSI/VHSIC devices into a high speed, high reliability system.

2. VLSI/VHSIC INTERCONNECTS AND PACKAGING DESIGN CONSIDERATIONS

CHIP I/O REQUIREMENTS

The goal of many VLSI/VHSIC programs is to increase the I/O capability to more than 200 I/Os and ultimately to as many as 500. These high I/O counts are required to maximize the capability of the VLSI/VHSIC device. Often, the number of I/Os can be related empirically to the number of gates (or proportionately to the number of functions) via an exponential relationship known as Rent's Rule.¹ According to Rent's empirical relationship,

$$I/Os = a(gates)^b. \quad (1)$$

The exponent b (often referred to as Rent's exponent) is typically found to be close to 0.5;² however, as the functionality or performance of the device is increased, so too is the exponent. Estimates of the Rent's exponent are as high as 0.85 for some high performance computer designs.

For many logic systems the Rent's relationship is accurate and the exponent is close to 0.5 (square root law). One manufacturer³ has found that for logic chips a Rent's relationship with $a = 4.5$ and $b = 0.5$ is consistent with their findings. Assuming this to be the case, a logic chip with a thousand gates would require more than 100 I/Os. For memory chips that are typically addressed in a binary encoded format, doubling the memory can be accomplished by simply adding one additional address bit (logarithmic law). For example, a 256K memory chip can have as few as 20 I/Os. Other device functions also follow this logarithmic I/O law. For dual-processing functions the number of I/Os would follow a linear relationship. Whatever the relationship it is clear that clever designers can design around I/O limitations. However, if the bit-transfer rate is to be improved significantly, the number of I/Os must be increased.

At clock speeds in excess of 100 MHz, electrical performance becomes a critical factor in influencing chip I/O design. At these high frequencies crosstalk due to mutual coupling of adjacent conductors can become a serious concern. Mutual and self-inductance effects can be minimized with the proper use of power and ground distribution on the high speed device itself. This, however, increases the number of dedicated I/Os for power and ground connections, further intensifying the pin density problems.

One concern associated with high I/O devices is the increase in their physical dimensions. This will require that the differential thermal coefficients of expansion (TCE) between device and package be low. Thermal stress problems arise from large TCE differences and also from the increased amount of power dissipated by dense, high speed VLSI/VHSIC chips.

PACKAGE REQUIREMENTS

Packaging of semiconductor dies in discrete chip carrier packages has many advantages over mounting the devices directly on the substrates. These advantages include protection for the die itself and for the wire bonds, isolation from external moisture and contamination (hermeticity), and testability (pre- and post-burn-in). However, the driving force behind discrete device packaging is the ability to repair the circuit should the need arise. It is clear that an entire circuit board with chips mounted directly to the substrate could be packaged so as to offer protection and hermeticity. However, if such a subsystem should fail in the field, repairs would be difficult and expensive. Discrete packaging would preclude the necessity of subsystem packaging, permitting direct access to the failed device. Removal could be accomplished by removing only one device package and replacing it with another. Also, the ability to replace a single device or component at the manufacturing site reduces the number of subcircuits that must be discarded, subsequently reducing their net cost.

The requirements for discrete VLSI/VHSIC device packaging include: the ability to support high I/O counts; low thermal resistance to accommodate large power-dissipation densities; hermetically sealed packages to afford protection from external moisture and contamination; good electrical properties of the leads; a TCE approximately equal to that of the die; rugged mechanical and electrical connections to the substrate; and easy reparability. Other desirable characteristics would include placement and attachment amenable to automation, low package profile, and low package cost.

Of all these characteristics, meeting the high I/O number while satisfying approximately the other package criteria will present a most demanding challenge. For perimeter-leaded packages such as chip carrier packages, satisfying the modest goal of 200 I/Os would require 50 leads per side. For a 1-in.-square package, this would require that the pitch of the leads equal 20 mils.

SUBSTRATE INTERCONNECT REQUIREMENTS

Substrate interconnect wiring must meet even more stringent requirements than does discrete packaging. The interconnects are typically longer than package leads and thus will more significantly influence the transmission characteristics of high speed signals. Good thermal characteristics are essential when heat transfer is primarily by thermal conduction through the substrate medium. A good TCE match between package and substrate is generally favorable, especially when using surface-mount, leadless chip carriers and components. A low dielectric constant is essential for high speed transmission, low capacitance, and high characteristic impedance. It also facilitates the fabrication of fine-line, multilayer conductor geometries required by VLSI and VHSIC devices.

High circuit density compatible with high I/O capabilities is the primary requirement for successful implementation of VLSI and VHSIC device technologies. For VHSIC devices compatibility with such transmission line interconnects as striplines and microstriplines is essential. To achieve the necessary level of circuit wiring density will require the use of multilayer circuit boards. Combining the requirements for both high circuit density and transmission line interconnects compatible with the device I/O characteristics places certain restrictions on the dielectric constant for insulating materials in multilayered systems.

The characteristic line impedance requirements for interconnecting VHSIC devices may be different than for some VLSI devices. As the density of the circuitry in VLSI devices increases, the output impedances for these devices are likely to be significantly higher than for the VHSIC devices. The latter are currently being fabricated to drive 50- Ω transmission line interconnects. They will be much more sensitive to controlled impedance than the VLSI devices because of the higher speeds at which they will be expected to operate. The 50- Ω line impedance offers a compromise as to ease of fabrication, good crosstalk immunity, and high speed transmission. Fabricating 50- Ω lines in multilayered dielectric media depends on the dielectric constant, thickness of the insulating layers, and the conductor geometry. Also, the lower the dielectric constant, the faster a signal propagates and the longer is the interconnection before proper line termination becomes necessary. A longer unterminated length becomes desirable as the number of connections increases; as they increase, both the average length of signal lines and the number of lines requiring termination will also increase.

The stripline and microstrip lines are the most common multilayer transmission-line structures for high speed interconnects. The configurations are illustrated

in Fig. 1. Both possess well characterized transmission-line properties. The microstrip line is a higher impedance type of structure than is the stripline. For 50- Ω impedance lines the stripline requires a thicker insulation and lower dielectric constant than does the microstrip. This is because of the inherently higher capacitance and lower inductance for the stripline configuration.

A popular high speed interconnect for multilayered circuit boards is the dual stripline transmission line shown in Fig. 2. This structure provides good crosstalk immunity by shielding signal lines from overlapping parallel lines. The structure provides a similar impedance for board interconnections that must travel both horizontally and vertically. The dual stripline also does not require the larger number of ground plane structures that the more conventional stripline configuration requires. However, when tightly controlled impedance is necessary, the dual stripline is not as effective, owing to the effect that crossovers have on the characteristic line impedance. The dual stripline is still an effective multilevel structure for achieving dense wiring with good crosstalk immunity when tight impedance control is not absolutely essential.

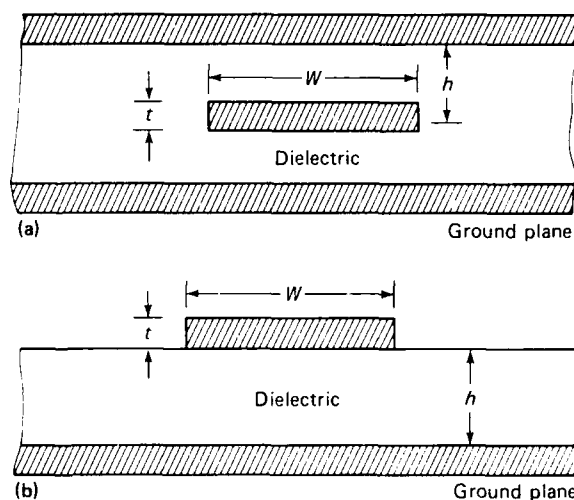


Figure 1 Stripline (a) and microstrip (b) configurations.

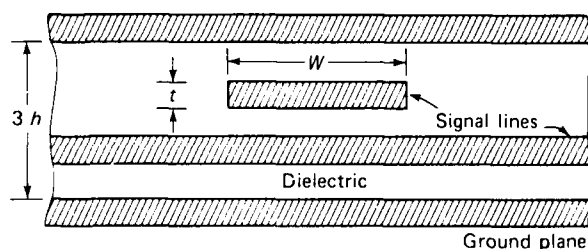


Figure 2 The dual stripline configuration.

CONNECTOR REQUIREMENTS

The substrate connectors of the VLSI/VHSIC era may have to accommodate I/O numbers ranging from 100 to 1000 depending on the application. The standard I/O configurations for the connector technology of today consist primarily of linear pin arrays spaced on 100-mil centers. Multiple linear arrays or pin grid-type connectors must be developed to accommodate both present and future needs. Perimeter-style connections (on all four circuit board edges) and even area connections may be required to maximize circuit board wiring densities (via Rent's Rule) and to accommodate I/O numbers greater than 1000. If hundreds or even thousands of pins are required, the pitch will have to be 50 mils or less, even when area arrays are used.

In addition, for testing and repairing these complex circuit systems, the connector pins must be able to withstand many connect and disconnect cycles. Manufacturing reliable connectors can be difficult because the pin pressures required to make reliable contacts can often result in wear, plastic flow, welding, and intermetallic formation. Also, zero insertion-force attachment of pin-style connectors is necessary when making connections involving large numbers of pins.

One of the primary concerns associated with the use of connectors is that they function electrically; that is, the connector should not add any significant resistance, capacitance, or inductance to the signal path. Inductive voltage spikes resulting from high frequency pulses is a primary source of crosstalk in connectors.⁴ In high frequency usage, the connector leads should be shielded transmission-line interconnections, with impedances matching those of the circuit board. Any unshielded portions of the connector should be as small physically as possible.

THERMAL CONSIDERATIONS

Heat dissipation in both complementary metal-oxide semiconductor (CMOS) and bipolar device technologies is increasing and will continue to do so as operating speeds are further increased. Although the quiescent power dissipation is zero for CMOS devices, while switching it is comparable to that for most bipolar technologies. This power is a function of both the operational frequency, the driver power-supply voltage, and the load capacitance. Increasing the performance of CMOS (i.e., the speed) requires that driver voltages be high. The high wiring densities for VLSI devices will always conspire to keep load capacitance high. Large CMOS gate-array devices commonly exhibit power dissipations greater than 2 W.

Emitter-coupled logic (ECL) circuits driving transmission-line interconnects must often utilize series resistance (approximately that of the line) at the source end (due to the low driver output impedance) and a termination resistance at the load end (to minimize reflections). For an ECL device with 200 I/Os driving 50- Ω matched transmission lines, the power per driver is about 15 to 25 mW. For 200 lines the chip could be expected to use as much as 5 W for driver power alone.

Additional difficulties will be encountered in making void-free bonds to large area dies. These difficulties are typical for most eutectic and solder attachment methods where voids can produce localized hot spots on the chip. Ideally, thermal resistances from the junction through this bond to the substrate should be less than 5 to 6 $^{\circ}\text{C}/\text{W}$.

In space electronic systems, for example, weight is usually an overriding consideration. Here, every portion of the electrical system must be maximized with respect to its contributions in the area of thermal management.

Thermal management may ultimately become the limiting factor in applications where conventional cooling methods are not practical and more exotic methods (such as heat pipes) may have to be investigated.

PROCESS REQUIREMENTS

Microelectronic design, manufacturing, materials development, and testing processes will have to undergo a major metamorphosis if the full impact of VLSI technology is to be realized. The effect of this increased activity will result initially in increased production, capital expenditure, design, and development costs. Presently, microelectronics packaging is lagging behind new device technologies, particularly in the areas of attachment, high performance wiring boards (i.e., dense multilayer circuit boards), surface mounting (necessary for high speed), and reliability testing and evaluation.

The most significant area requiring development is that involving high I/O chip packaging. With I/O estimates as high as 200 to 400, how can such traditional processes as wirebonding continue to function as reliable chip-to-package interconnects? Even if high-density wirebonding can be accommodated, nondestructive pull testing will become extremely difficult, and shorting as a result of wire slumping will always remain a potential hazard. Tape-automated bonding (TAB), which is a "gang bonding" process, may solve the problems of density and speed of bonding; however, testing TAB bonds by means of techniques akin to nondestructive pull testing is out of the question because of the Kapton polyimide film that supports the lead frame.

Surface-mount attachment of leaded, high-I/O-density chip packages will present another significant challenge to electronics packaging. Automatic handling, testing, placement, and attachment will require extreme care and sophisticated tooling and processes. I/Os will be small and fragile, with lead spacings of 20 mils or less.

The fabrication of dense multilayer circuitry that possesses controlled-impedance signal traces, ground and power planes, low-K dielectric constant, good thermal

conductivity, and a TCE compatible with surface mounting is still an illusive goal. Since low dielectric constant usually implies low thermal conductivity, methods for incorporating high-thermal-conductivity materials, either in the form of metal cores, bonded heat sinks, or other thermal conductivity enhancement features will have to be devised and further developed if we are adequately to make use of the excellent electrical properties of the low-K dielectric circuit board materials.

3. ELECTRICAL CHARACTERIZATION OF VLSI/VHSIC DEVICES

Evaluation of a suitable substrate wiring technology for a particular application of a high speed device depends on the the specific characteristics for the logic family that is to be interconnected. These characteristics include the input and output impedances, noise immunity, and the unloaded rise and fall times of the signals from the device output drivers. The popular logic families for moderate to high speed logic applications would include: high speed complementary metal oxide semiconductor (HCMOS) logic, transistor-transistor logic (e.g., ALSTTL and ASTTL), and emitter-coupled

logic (e.g., ECL 10K and ECL 100K). Typical electrical characteristics for these device technologies are listed in Table 1.

RISE AND FALL TIME

The unloaded rise time (t_r) and fall time (t_f) for device output drivers are important in determining the maximum unterminated length of a signal line before reflections and ringing need to be considered. The rise

Table 1—Typical SSI device characteristics for some popular high speed logic families

Device	Rise time (t_r) (typical), nsec	Quiescent output impedance, Ω		Dynamic impedance αR_0 , Ω		DC noise margins, v		Decoupling capacitance per gate, pF
		V_{OH}	V_{OL}	0 $\rightarrow$ 1	1 $\rightarrow$ 0	V_{OH}	V_{OL}	
HCMOS	7	On resistance of upper FET ≈ 60	On resistance of lower FET ≈ 50	≈ 120	≈ 120	28% of V_{CC}	18% of V_{CC}	750
ALSTTL	4	≈ 63	≈ 15	41	46	0.7	0.3	3000
ASTTL	2	≈ 40	≈ 6	22	32	0.5	0.3	4500
ECL (10K)	2	≈ 7	≈ 7	20	26	0.125	0.155	750
ECL (100K)	1	≈ 10	≈ 7	5		0.140	0.145	1500

and fall times are also useful for time-domain analysis of voltage crosstalk. The maximum unterminated length of a transmission line can be given through the relationship

$$l_c = (t_r \text{ or } t_f) / 2 T_d . \quad (2)$$

The time delay, T_d , can be modified to include the effects of bonding wire, package leads, etc. through the relation

$$T'_d = T_d \sqrt{1 + C_L / C_0} , \quad (3)$$

where C_0 and C_L are the isolated line and parasitic load capacitance, respectively.

The maximum sinusoidal frequency harmonics for a trapezoidal clock pulse can be estimated through the relation

$$f_{\max} = 0.35 / (t_r \text{ or } t_f) , \quad (4)$$

where t_r (or t_f) represents the rise time (or fall time) for the pulse. This approximate relationship only applies strictly to periodic pulses such as those found on clock lines and with duty cycles less than 50%. As the duty cycle is increased, the power in the DC and lower frequency signal components decreases and that in the higher frequency components increases.

DEVICE OUTPUT IMPEDANCE

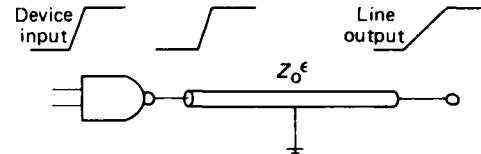
The device output impedance is important in determining the optimum signal line impedance for the unterminated line. For example, ringing—as a result of reflections in unterminated lines—can be eliminated by matching the driver source impedance to the line impedance. For most devices the output impedances for high-to-low and low-to-high transitions are typically different, and an exact match is impossible. However, a good compromise can usually be found. Generally, the higher the output impedance, the less capacitance that a source can drive for a given propagation delay. For short lines a relationship for the device (internal) and line (external) propagation delays, the propagation delay total t_p can often be represented by an equation of the form

$$t_p = t_{pi} + \alpha R_0 C_L , \quad (5)$$

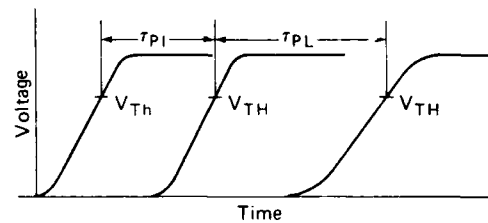
where t_{pi} is the internal delay, αR_0 is the dynamic output impedance (R_0 is the static output resistance), and C_L is the load capacitance. This approximate relationship is valid only when the rise and fall times are less than twice the line delay. Figure 3 illustrates the relationship between the total time delay and the internal and line (or load) delay.

In VLSI chips scaling will ultimately increase the driver output resistance for these devices.⁵ This increase in output resistance may limit the amount of capacitance that a device can drive before encountering excessive time delays. Implementation of low-K dielectric materials will be required for fabrication of suitable wiring boards that provide the low capacitance (and low inductance) environment required by these devices.

The most common output drivers currently being investigated for VHSIC devices include STTL, CMOS, LSTTL, and ECL. Of these driver circuits, STTL and LSTTL are the most popular. The average dynamic-output resistances (average for both high-to-low and low-to-high transitions) for STTL drivers are typically around 35 Ω , while those for LSTTL circuits are much higher, $\approx 125 \Omega$.



(a) Device and "loaded" characteristic line impedance Z_0 .



(b) Total delay equals the internal delay t_i plus the line/load delay t_L .

Figure 3 Estimating time delays for device interconnections.

4. ELECTRICAL CHARACTERIZATION OF HIGH SPEED DEVICE/SYSTEM INTERCONNECTIONS

PROPAGATION VELOCITY AND CHARACTERISTIC IMPEDANCE

All electromagnetic circuits involve the transmission of electromagnetic waves. These waves travel at finite speed with an associated wavelength that is typically much larger at low frequencies than the physical size of most electronic circuits. Thus, for low-frequency operation, the voltage (electric field) and the current (magnetic field) are relatively static, and the effects of wavelength and velocity of propagation are relatively unimportant. At low frequency, DC-circuit concepts using lumped elements can be derived by assuming stationary electric and magnetic fields. At higher frequencies where the wavelength is a significant fraction of the physical size of the circuit, this lumped-element approximation is no longer valid. For non-TEM modes existing at high frequencies, the concept of voltage and current in the DC-circuit sense becomes meaningless.

The relationship between the velocity of propagation and the wavelength for a pure sinusoidal wave is

$$\lambda = \frac{v_p}{f}, \quad (6)$$

where v_p is the velocity of propagation, λ is the wavelength, and f is the frequency. For quasi-TEM transmission the propagation velocity of the signal along a lossless transmission line of capacitance per unit length C and inductance per unit length L is

$$v_p = \frac{1}{\sqrt{LC}}. \quad (7)$$

For those situations where the largest significant wavelength for a digital pulse is less than or equal to twice the length of the signal line that it is propagating on, transmission-line analysis is required. Classical transmission-line analysis requires that the predominant mode of transmission be TEM (transverse electromagnetic). Fortunately, at most frequencies of interest (below 2 GHz), typical multilayer-circuit configurations cannot sustain low-order non-TEM modes (e.g., TM or TE), and thus quasi-TEM transmission-line techniques are usually valid.⁶

When a voltage signal propagates on a long transmission line, the load experienced by the signal is the characteristic impedance of the line. The characteristic impedance can be represented by the equation:

$$Z_0 = \sqrt{\frac{R + j\omega L}{G + j\omega C}}, \quad (8)$$

where

- Z_0 = characteristic impedance in Ω
- R = resistance in Ω/cm
- L = inductance in H/cm
- C = capacitance in F/cm
- G = conductance in S/cm
- ω = angular frequency in rad/sec .

At low frequencies, when $R \gg \omega L$ and $\omega C \gg G$, the characteristic impedance becomes

$$Z_0 = \sqrt{\frac{R}{j\omega C}}. \quad (9)$$

At high frequencies, when $R \ll \omega L$ and $\omega C \gg G$ (the lossless case), the characteristic impedance becomes

$$Z_0 = \sqrt{\frac{L}{C}}. \quad (10)$$

For this case the impedance is real and behaves like a pure resistance. However, since the line is lossless (no Joule heating effect) this impedance is not a true resistance.

Whenever the signal on a long transmission line, encounters a discontinuity in the characteristic impedance of the line, a portion of the transmitted wave is reflected back toward the source. The fraction of the wave reflected from the discontinuity is given by the relation

$$\rho_l = \frac{Z_l - Z_0}{Z_l + Z_0}, \quad (11)$$

where ρ_l is the reflection coefficient, Z_l represents the load impedance (or source impedance), and Z_0 is the

characteristic line impedance. These discontinuities can result from a change in either the line impedance or at the input of a device load or load circuit.

When interconnections become long or signal-line impedance is low, reflections must be considered. Reflections occur when device interconnections are not terminated in their characteristic impedance; they may lead to reduced noise margins, excessive delays, ringing, and overshoot. Generally, when the rise time of a device is less than 10 times the RC time constant of the loaded line, the simple lumped-element model for the interconnection must be replaced with a transmis-

sion-line model for an accurate estimation of time delays.

The transmission-line analysis for the n-line system requires an estimation of the transmission-line parameters of the system, which at high frequencies include the capacitance and inductance matrixes, the conductance matrix (for the high-loss dielectric case only), and the line resistance. In the following sections techniques for estimating these high-frequency circuit parameters and methods for simulating circuit performance are discussed.

5. ANALYTICAL TECHNIQUES FOR ESTIMATING FUNDAMENTAL ELECTRICAL PARAMETERS

CAPACITANCE CALCULATIONS

Calculating such electrical circuit parameters as the capacitance and inductance for multiconductor transmission lines is a formidable task. Prior to the introduction of high speed computers, only analytical formulations obtained by solving Laplace's equation for relatively simple and highly symmetrical conductor and ground plane geometries were available. Today there are many numerical techniques for calculating capacitance and inductance for arbitrarily shaped multiconductor transmission-line geometries.

Evaluation of the capacitance of an n-conductor system requires that the free charge distribution on each conductor be determined. The matrix element C_{ij} is defined as the ratio of the charge on the i th conductor to the potential on the j th conductor with all of the conductors at zero potential except the j th conductor. The elements of the capacitance matrix can be expressed through the relation

$$C_{ij} = \frac{Q_i}{V_j} \bigg|_{V_i=0, i \neq j, n} \quad (12)$$

There are three primary numerical ways to evaluate the capacitance of the n-conductor system: the boundary element method, the finite element method, and the finite difference method. Each of these techniques provides a means to estimate the free-charge distributions on conductor boundaries for an arbitrarily oriented n-conductor system.

Boundary Element Method

The boundary element technique⁷ is essentially a Green's function integral method that has the desirable property that only surface elements making up the conductor boundaries and dielectric interfaces need be considered in the analysis. The procedure for achieving a solution is based on the well known method of replacing all the conductor and dielectric surface layers with equivalent layers of unknown charge densities in free space.^{8,9} For this assumption the potential and the electric field can be expressed through the relations

$$\phi(r(j)) = \int \sigma_T(i) G(r(j)|r(i)) d^3 r(i) \quad (13)$$

and

$$E(r(j)) = -\nabla \phi(r(j)) \quad (14)$$

where the integration takes place over all conductor surfaces and dielectric-dielectric interfaces. $\phi(r(j))$ is the potential and $E(r(j))$ is the electric field. $(\sigma(i))_T$ represents the total charge density and $G(r(j)|r(i))$ is the free-space Green's function for the electrostatic problem. The total charge density consists of the bound charge density residing at dielectric-dielectric interfaces and the sum of the bound and free charge densities at the conductor-dielectric boundaries.

The boundary element method assumes that conductor surfaces can be divided into subelements, and impulse functions can be defined such that

$$f(r(i)) = 1, \text{ on the } i\text{th subelement} \quad (15)$$

$$= 0, \text{ elsewhere}$$

The total charge density can then be expressed as follows:

$$\sigma_T(i) = \sum_{i=1}^N \frac{q(i)}{\Delta l_i} f(r(i)), \quad (16)$$

where Δl_i is the contour of the i th subelement and $q(i)$ is the total charge on the i th subelement. Hence, the potential is given by the relation

$$V(r(j)) = \sum_{i=1}^N \sigma_T(i) \int_{\Delta l_i} G(r(j)|r(i)) dl_i \quad (17)$$

For the two-dimensional case the conductor surfaces and dielectric interfaces consist of arbitrarily small line elements, and the integral in Eq. 17 becomes a line integral. The free-space Green's function in two dimensions is given by the relation

$$G(r(j)|r(i)) = \frac{1}{2\pi\epsilon_0} \ln \frac{k}{|r(j) - r(i)|}, \quad (18)$$

where $r(j)$ is the field point and $r(i)$ is the source point, ϵ_0 is the free-space permittivity, and k is a constant. The constant, k , represents the potential that exists at infinity. It can be effectively eliminated by requiring that the total free and bound charge densities at conductor surfaces and dielectric interfaces be equal to zero.

For three-dimensional applications the subelements are surfaces; the three-dimensional free-space Green's function is used and is given by the relation

$$G(r(j)|r(i)) = \frac{1}{4\pi\epsilon_0 |r(j) - r(i)|}. \quad (19)$$

The total charge density at the conductor boundaries is given simply by the set of N_c conductor equations expressed by Eq. 17 assuming that the voltage on the conductor boundaries is known. The bound charge density at the dielectric interfaces can be determined through the application of the appropriate boundary conditions. The boundary conditions for the electric field at the dielectric-dielectric interfaces can be expressed through the following expressions:

$$D_1 \cdot \hat{n} = D_2 \cdot \hat{n}, \quad (20)$$

and

$$\epsilon_0 \epsilon_1(i) E_1(r(i)) \cdot \hat{n} = \epsilon_0 \epsilon_2(i) E_2(r(i)) \cdot \hat{n}, \quad (21)$$

where ϵ_1 and ϵ_2 are the relative permittivities, and $\hat{n}$ is the outward or normal unit vector at the interface. The electric field vectors $E_2(r(i))$ and $E_1(r(i))$ represent the components of the field in the positive and negative normal directions, respectively, at the interface.

At the interface the bound charge density for any subelement can be expressed through the polarization vectors P_1 and P_2 as

$$\sigma_b(i) = P_1(r(i)) \cdot \hat{n} - P_2(r(i)) \cdot \hat{n}. \quad (22)$$

Enforcing the boundary conditions at the interface, we obtain the relation

$$\sigma_b(i) = \left(\frac{\epsilon_1(i) - \epsilon_2(i)}{\epsilon_1(i)} \right) \epsilon_0 E_2(r(i)) \cdot \hat{n}, \quad (23)$$

where E_2 is the electric field at any subelement resulting from the total surface charge distribution at every other conductor boundary or dielectric interface subelement. The electric field at any subsection can then be expressed through the relation

$$E(r(j)) \cdot \hat{n} = - \sum_{\substack{i=1 \\ i \neq j}}^N \sigma_T(i) \int_{\Delta l_i} \nabla G(r(j)|r(i)) \cdot \hat{n} dl_i + \frac{\sigma_T(j)}{2\epsilon_0}. \quad (24)$$

Combining Eqs. 23 and 24, one obtains the set of N_d equations for the total charge density (i.e., bound charge density) at the dielectric-dielectric interfaces:

$$\sigma_T(i) \left(\frac{\epsilon_1(i) + \epsilon_2(i)}{2\epsilon_0} \right) - (\epsilon_1(i) - \epsilon_2(i)) \times \sum_{\substack{i=1 \\ i \neq j}}^N \sigma_T(i) \int \nabla G(r(j)|r(i)) \cdot \hat{n} dl_i = 0. \quad (25)$$

The equations for the total charge density for each subelement can then be calculated by prescribing the voltages on each of the conductor subelement sections for the N_c conductor equations and the set of N_d equations for each of the dielectric subelement sections. An additional equation is then included to eliminate the constant, K , for the two-dimensional case, which constrains the total bound and free charge over the entire domain of the problem to be equal to zero.

The free-charge density at each of the conductor subelements is then evaluated through the use of the boundary conditions at each of the conductor-dielectric interfaces; i.e.,

$$\sigma_f(j) = D_2(j) \cdot \hat{n}(j) - D_1(j) \cdot \hat{n}(j). \quad (26)$$

The dielectric constant in the region outside the conductor is simply that of the dielectric material surrounding that conductor, while the dielectric constant inside the conductor surface is simply that for free space.

For the infinitely thin conductor the boundary conditions for the discontinuity in the electric field across a surface dipole layer may be assumed. Using Eq. 26 and the relation

$$E(r(j)) \cdot \hat{n}(j) = \frac{\sigma_f(j)}{\epsilon_0} \quad (27)$$

for the discontinuity of the electric field through a surface dipole charge layer, the free charge density can be expressed through the relation

$$\sigma_f = \frac{\epsilon_1(j) + \epsilon_2(j)}{2} \sigma_T(j) - (\epsilon_2(j) - \epsilon_1(j)) \times \sum_{\substack{i=1 \\ i \neq j}}^N \sigma_T(i) \int \nabla G(r(j)|r(i)) \cdot \hat{n} dl_i. \quad (28)$$

Once the free-charge density on the conductor surfaces has been determined, elements of the capacitance matrix can be evaluated with the help of Eqs. 12 and 16.

Four computer programs have been written that incorporate the theory discussed here for the purpose of

performing capacitance and inductance calculations for arbitrarily complex two-dimensional multiconductor geometries. The four programs calculate (a) capacitance—finite ground plane, (b) capacitance—finite ground plane, (c) inductance—finite ground plane, and (d) inductance—finite ground plane. The program is written in Fortran for the IBM Personal Computer AT. The Fortran code is provided in Appendix A.

Finite Element Method

The finite-element method is a generalized technique for obtaining approximate solutions to a wide variety of boundary problems. The method involves the decomposition of a complex domain into simpler subdomains or finite elements, and use of a variational technique to obtain approximate solutions over a collection of finite elements.

The availability of a variational formulation for the electrostatic problem (Poisson's equation) guarantees a finite-element approach for obtaining the capacitance matrix elements for the n -conductor system. The variational formulation for the electrostatic problem is given through the relationship

$$F(\phi) = \int_v \left\{ \frac{1}{2} \left[\epsilon_x \left(\frac{\partial \phi}{\partial x} \right)^2 + \epsilon_y \left(\frac{\partial \phi}{\partial y} \right)^2 + \epsilon_z \left(\frac{\partial \phi}{\partial z} \right)^2 \right] - \rho \phi \right\} dv, \quad (29)$$

where ϕ is the electrostatic potential, ϵ is the dielectric constant, and ρ is the volume charge density. For situations where charges reside on the conductor surfaces, the volume charge density, ρ , is replaced with the surface charge density, σ , and that portion of the integral in Eq. 29 containing the charge density becomes a surface integral. $F(\phi)$ is referred to as the energy functional for the electrostatic problem. A functional is an integral in which the integrand contains functions and their derivatives. The variational approach seeks to minimize this energy functional with respect to the function ϕ . When the condition is satisfied, the functional is said to be "stationary" for the particular solution ϕ' that is found.

The solution procedure involves dividing a body into N elements and the functional into N functionals for each of the finite elements as follows:

$$F(\phi) = \sum_{e=1}^E F_e(\phi), \quad (30)$$

where the index e goes from 1 to the total number of finite elements (E) used in the calculation. A solution of the form

$$\phi(\mathbf{r}) = \sum_{j=1}^{Nodes} N_j \phi_j, \quad (31)$$

is assumed for each of the finite-element subdomains where j goes from 1 to the number of finite-element nodes. The nodes serve as demarcation points for the finite-element subdomains. The vector N_j is referred to as the shape function and the ϕ_j 's are referred to as the vectors of nodal values.

The electrostatic potential is considered a function of all the nodal potentials

$$F \equiv F(\phi_1, \phi_2, \dots, \phi_n). \quad (32)$$

The variation of $F(\phi)$ yields

$$\delta F \equiv \frac{\partial F}{\partial \phi_1} \delta \phi_1 + \frac{\partial F}{\partial \phi_2} \delta \phi_2 + \dots + \frac{\partial F}{\partial \phi_n} \delta \phi_n. \quad (33)$$

Since the ϕ_j 's are arbitrary,

$$\frac{\partial F}{\partial \phi_1} = 0, \frac{\partial F}{\partial \phi_2} = 0, \dots, \frac{\partial F}{\partial \phi_n} = 0. \quad (34)$$

Hence, we go from a global statement of the problem to a local one:

$$\frac{\partial F}{\partial \phi_i} = \frac{\partial \sum_{e=1}^E F_e}{\partial \phi_i} = \sum_{e=1}^E \frac{\partial F_e}{\partial \phi_i} = 0, \quad (35)$$

and the problem reduces to considering one element at a time.

For the electrostatic problem we consider the energy functional for the situation where we have charges residing on the conductor surfaces. The energy functional can be written as follows:

$$F_e(\phi_1, \dots, \phi_n) \equiv \int_v \frac{1}{2} \left[\epsilon_x \left(\frac{\partial}{\partial x} \sum_{j=1}^N N_j \phi_j \right)^2 + \epsilon_y \left(\frac{\partial}{\partial y} \sum_{j=1}^N N_j \phi_j \right)^2 + \epsilon_z \left(\frac{\partial}{\partial z} \sum_{j=1}^N N_j \phi_j \right)^2 \right] dv$$

$$- \oint_s \sigma \sum N_j \phi_j ds. \quad (36)$$

We differentiate to obtain

$$\begin{aligned} \frac{\partial F_e}{\partial \phi_i} &= \int_v \left[\epsilon_x \left(\frac{\partial}{\partial x} \sum_{j=1}^N N_j \phi_j \right) \frac{\partial N_j}{\partial x} \right. \\ &\quad + \epsilon_y \left(\frac{\partial}{\partial y} \sum_{j=1}^N N_j \phi_j \right) \frac{\partial N_j}{\partial y} \\ &\quad \left. + \epsilon_z \left(\frac{\partial}{\partial z} \sum_{j=1}^N N_j \phi_j \right) \frac{\partial N_j}{\partial z} \right] dv \\ &\quad - \oint_s \sigma N_j ds = 0. \end{aligned} \quad (37)$$

This expression can be simplified by interchanging the $\frac{\partial}{\partial x}$, $\sum_{j=1}^N$, and $\int_v$:

$$\begin{aligned} \frac{\partial F_e}{\partial \phi_i} &= \sum_{j=1}^N \left\{ \int_v \left[\epsilon_x \frac{\partial N_i}{\partial x} \frac{\partial N_j}{\partial x} + \epsilon_y \frac{\partial N_i}{\partial y} \frac{\partial N_j}{\partial y} \right. \right. \\ &\quad \left. \left. + \epsilon_z \frac{\partial N_i}{\partial z} \frac{\partial N_j}{\partial z} \right] dv - \oint_s \sigma N_j ds \right\} = 0. \end{aligned} \quad (38)$$

This expression can be written in matrix form as

$$\left\{ \frac{\partial F_e}{\partial \phi_i} \right\} = [K] \phi - \{P\} \equiv 0 \quad (39)$$

where

$$\begin{aligned} K_{ij} &= \int_v \left(\epsilon_x \frac{\partial N_i}{\partial x} \frac{\partial N_j}{\partial x} + \epsilon_y \frac{\partial N_i}{\partial y} \frac{\partial N_j}{\partial y} \right. \\ &\quad \left. + \epsilon_z \frac{\partial N_i}{\partial z} \frac{\partial N_j}{\partial z} \right) dv \text{ and } P_i = \oint_s \sigma N_i ds. \end{aligned}$$

The choice of basis vectors or shape functions is arbitrary, as there is no systematic way of constructing

reasonable basis functions for the approximate test function. Moreover, the quality of the approximate solution will vary depending on the choice for these basis functions. The basis or "shape" functions should be defined piecewise over the finite-element subdomains. Over these subdomains the functions are usually chosen to be very simple ones such as low-order polynomials. Another requirement for the shape functions is that they be smooth enough so that the integrals of Eq. 39 are finite over each finite element.

Fortunately, the specification of the shape functions and the solution algorithms for the solution of Poisson's equations is available in many standard finite-element codes. The codes are generally formulated to solve the steady-state heat equation; however, the analogy between the heat equation and the electrostatic problem permits the use of such codes to evaluate the capacitance matrix. Substituting potential, permittivity, and charge for temperature, thermal conductivity, and power, respectively, is all that is required to complete the analogy. To obtain a row of capacitance matrix elements, a reference ground is determined such that the potential (i.e., the temperature) is zero. All other conductors are required to reside at zero potential except the conductor of interest. These boundary conditions form a system of constraint equations from which the surface charge (i.e., the power) required to maintain all of the conductors at their prescribed potentials (temperatures) may be extracted.

The attractive features of the finite-element technique include the availability of pre- and post-processors for the rapid construction and analysis of two- and three-dimensional finite-element geometries, and the availability of analysis codes (such as NASTRAN) that are able to analyze complex conductor geometries and anisotropic dielectric materials.

INDUCTANCE CALCULATIONS

To obtain the inductance matrix $[L]$, the permittivities for all the dielectrics are replaced with the vacuum permittivity, and the capacitance matrix is recalculated for the identical conductor configuration. For quasi-TEM transmission lines the inductance per unit length is related to the capacitance per unit length by the relation

$$[L] = \frac{1}{c^2} [C_v]^{-1}, \quad (40)$$

where $[C_v]$ is the capacitance matrix with the dielectric replaced with vacuum and c is the speed of light in vacuum.

The self-inductance calculated in this manner represents the external or high-frequency inductance; it assumes that all or most of the current resides on the conductor surfaces. Also, this model assumes that the series resistance of the line is negligible and the thickness of the conductor trace is greater than several times the skin depth. Inductance calculations for thin transmission lines are discussed in Section 6, when discussing attenuation and dispersion effects.

CONDUCTANCE CALCULATIONS

The conductance matrix $[g_{ij}]$ for multiconductor transmission lines in a lossy dielectric medium can be estimated using a solution procedure similar to that used to estimate the capacitance matrix. The coupled, complex, time-harmonic transmission-line equations for the current and voltage are given as

$$\frac{d\hat{v}}{dz} = -j\omega [L] \hat{I}, \quad (41)$$

and

$$\frac{d\hat{I}}{dz} = -\{[G] + j\omega [C]\} \hat{v}, \quad (42)$$

where the complex permittivity can be expressed as

$$\hat{\epsilon} = \epsilon' - j\epsilon'' . \quad (43)$$

Equation 42 can be rewritten as

$$\frac{d\hat{I}}{dz} = -j\omega \left[[C] - j \frac{[G]}{\omega} \right] \hat{v} = -j\omega [\hat{C}], \quad (44)$$

where the complex matrix is

$$[\hat{C}] = [C] - j \frac{[G]}{\omega} . \quad (45)$$

Thus, from the above equation, using the imaginary part of the complex dielectric permittivity in place of the real permittivity to calculate the capacitance, as was discussed previously, and multiplying that result by $-\omega$, yields the conductance matrix in siemens per unit length.

6. CHARACTERIZATION OF NOISE IN DEVICE INTERCONNECTIONS

REFLECTION ANALYSIS

Classical transmission-line analysis is applicable for analyzing reflections in device interconnections, but it is difficult to accomplish because the input and output impedances for most devices are nonlinear. Two alternative methods for circumventing this problem are to assume that the source and load impedances are linear or to use a graphical technique known as the Bergeron method. For some device technologies, making the former assumption would lead to errors because of the high degree of nonlinearity of the input and output characteristics, especially for long lines. When the linear assumption is not reasonable, the graphical technique provides a suitable alternative.

The following section discusses analysis of the reflection from unterminated device interconnections using Bergeron diagrams. Here, reflections will be considered for the Series ALSTTL logic family.

Analysis of Reflections from Nonlinear Device Terminations

As an example of the Bergeron method¹⁰ for analyzing transmission-line reflections from nonlinear device terminations, the graphical technique is applied to the situation in which two Series ALSTTL nand gates are interconnected via a 10- Ω transmission line, as is depicted in Fig. 4. It is assumed that the circuit rise time is less than twice the line delay. To evaluate a logical 1-to-0 transition, a line of slope $-1/Z_0$ is drawn from the intersection of the input and output curves for the logical 1 condition. This line proceeds toward the intersection of the $-1/Z_0$ curve and the logical 0 output curve. At time t_0 , the voltage at the source, or driver, end is determined from the intersection of the $-1/Z_0$ line with the logical 0 output curve. The slope of the line then changes to $+1/Z_0$ and proceeds toward the logical 0 input curve; the voltage at the receiving end at t_1 (after one time delay) is determined from the intersection of the two curves. The slope of the line then reverts to $-1/Z_0$ and proceeds back toward the logical 0 output curve and so on. This procedure is continued until a logical 0 condition is reached.

The results for this example indicate that there are nine time delays before a guaranteed logical 0 condition ($V_{II} = 0.8$ V) appears at the gate input at the receiving end of the line. For a capacitive line or one with several capacitive loads, one time delay can be sig-

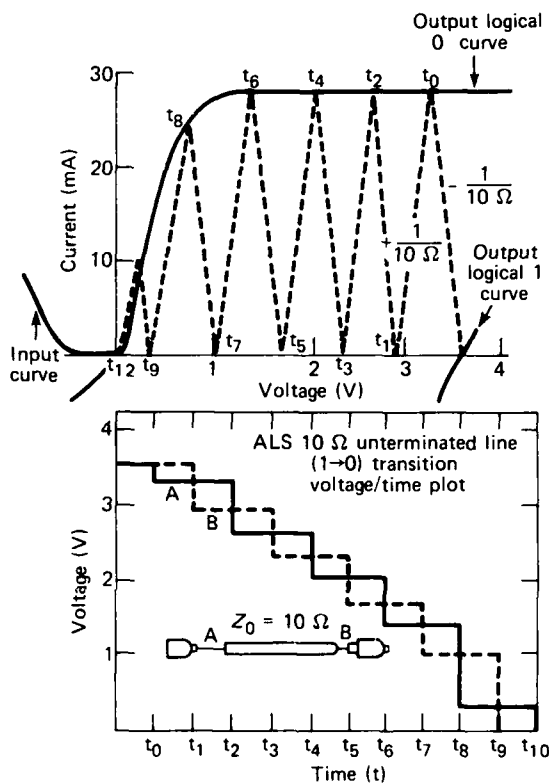


Figure 4 ALS 10- Ω unterminated line (1→0) transition (Bergeron diagram).

nificant for high speed operation. Clearly, the performance of the low-impedance interconnection is unacceptable for all but the shortest lines.

The same procedure is used to analyze a logical 0-to-1 transition with the same 10- Ω impedance interconnection. The situation is depicted in Fig. 5. For this case the $-1/Z_0$ line is drawn from the intersection of the input and the logical 0 output curves and proceeds toward the logical 1 input curve. The intersection of the $-1/Z_0$ curve and the logical 1 output curve represents the voltage at the driver end of the line at t_0 . The slope of the line changes, as before, to $+1/Z_0$ and proceeds from the intersection toward the logical 1 input curve. Once again, the voltage at the input to the gate after one time delay ($t = t_1$) is determined at the intersection of the two curves. The procedure is carried out as

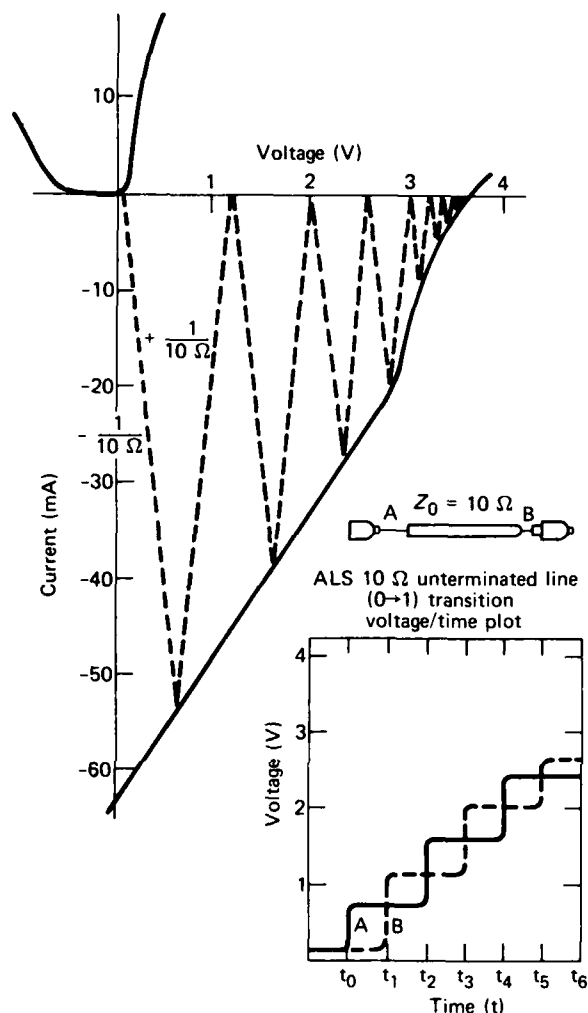


Figure 5 ALS 10- Ω unterminated line (0→1) transition (Bergeron diagram).

in the previous example until the logical 1 condition is reached.

The results for this case indicate that three time delays are required before a guaranteed logical 1 condition ($V_{IH} = 2.0$ V) is reached at the gate input with almost no noise margin. In addition, any gate having its inputs connected to the input of this transmission-line interconnection will be operating within its linear region and will be drawing excessive currents, thus aggravating ground and V_{CC} noise problems.

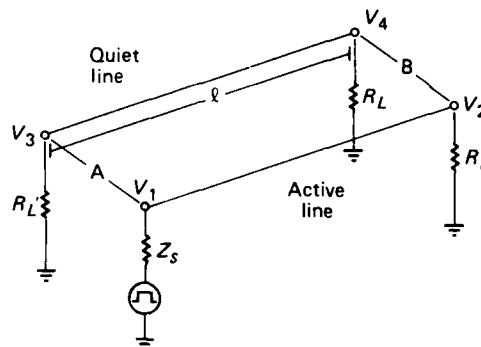
The usefulness of this technique for estimating time delays resulting from improper line impedance of transmission-line interconnects has been demonstrated. The method can be useful in determining which inter-

connection technologies are particularly suited to a device technology once the transmission-line properties of the interconnections have been characterized.

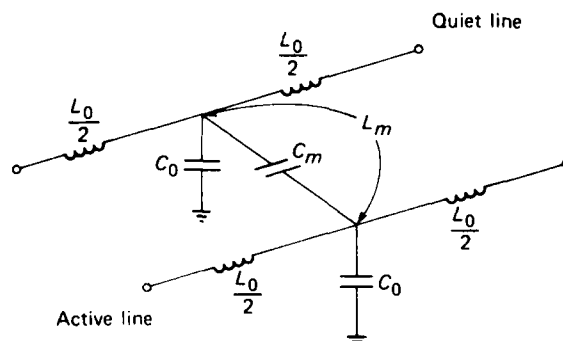
CROSSTALK ANALYSIS

Voltage crosstalk arises from the mutual capacitive (electric-field) and inductive (magnetic-field) coupling between adjacent conductors. When two lines are electrically coupled, the fields produced by changes in the currents and voltages on one line can induce currents and voltages on the other. As the switching time is decreased, the crosstalk is increased. In VLSI/VHSIC devices, the increased circuit densities and switching speeds inherent in them are making the task of controlling crosstalk increasingly difficult.

A convenient way to begin the discussion of crosstalk is to consider the two coupled lines shown in Fig. 6. For the present we neglect signal-line reflections by assuming that both lines are terminated in their characteristic impedances. Also, we assume that the voltage



(a) Parallel signal lines.



(b) Incremental circuit model for coupled lines.

Figure 6 Crosstalk circuit models for two coupled signal lines.

source is changing at the sending end of the active line while there is no voltage source on the quiet line. The coupling is assumed to result from a mutual capacitance, C_m , and a mutual inductance, L_m . As the signal generated at point A on the active line travels toward point B, a forward-traveling wave and a backward-traveling wave are generated on the quiet line. For this case both waves are eventually absorbed at the matched loads at both ends of the line. The voltage wave appearing at the near end of the quiet line is referred to as near-end or backward crosstalk. The voltage at the far end is referred to as far-end or forward crosstalk. Under these assumptions the forward voltage crosstalk in this case is given by the relation¹

$$V_f = \frac{l}{2v_p} \frac{dV_s}{dt} (C_m Z_2 - L_m/Z_1), \quad (46)$$

where l is the coupled length, v_p is the propagation velocity, dV_s/dt is the time rate of change of the voltage, and Z_1 and Z_2 are the characteristic impedances for the active and quiet lines, respectively. If both impedances are approximately equal, the relation becomes

$$V_f = \frac{l}{2v_p} \frac{dV_s}{dt} (C_m/C - L_m/L), \quad (47)$$

where C and L represent the self-capacitance and self-inductance of the coupled lines, respectively.

For the case of two coupled conductors immersed within a single dielectric medium (such as the case for the stripline), C_m/C equals L_m/L , and the forward crosstalk voltage is nearly zero. In most multilayer applications, this is nearly always true. For this particular case the forward crosstalk is negligible. As we will observe for more typical cases involving unterminated device interconnections, forward crosstalk cannot be neglected.

The amplitude of the backward traveling wave is given by the relation¹¹

$$V_b = \frac{1}{4} (L_m/Z_1 + C_m Z_2), \quad (48)$$

For the case where the coupled lines have approximately the same impedance, the backward voltage crosstalk is given as

$$V_b = \frac{1}{4} (L_m/L + C_m/C). \quad (49)$$

For very short lines, where twice the line delay is less than the rise-time of the signal, the above equation must be multiplied by the factor $2T_d/t_r$, yielding the relation

$$V_b = T_d/2t_r (L_m/L + C_m/C). \quad (50)$$

This is because the crosstalk fails to reach its maximum whenever the rise-time is less than twice the signal-delay time. Thus, one may observe that the backward crosstalk is independent of the rise-time except in the case where the risetime is much smaller than the delay time of the line.

Inspection of Eqs. 47 and 49 reveals that reducing both the mutual capacitance and inductance can significantly reduce voltage coupling. For the case where the active line is nearly terminated in its characteristic impedance, maximum coupling occurs when the near end of the quiet line is terminated in a high impedance (i.e., a device input) and the far end in a low impedance. This situation is approximately true for coupled device interconnections whose signals are propagating in opposite directions.¹² This situation is depicted in Fig. 7.

The above equations apply only in those cases where the lines are terminated in their characteristic impedances. In the next section a more general method is discussed for evaluating crosstalk between coupled transmission lines. It uses the method of normal modes and permits the use of arbitrary loads for both the source and terminal resistances.

Voltage Crosstalk For The N-Conductor System

As noted in the previous section for properly terminated transmission lines, near-end crosstalk is typically much greater than far-end crosstalk. However, when device interconnections are terminated in device loads (high-impedance loads), near-end and far-end crosstalk voltages differ only slightly. It is thus necessary to arrive at a more general and practical procedure for rep-

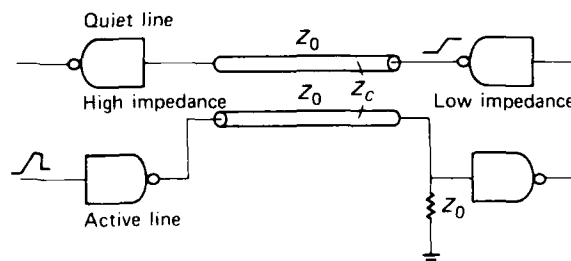


Figure 7 Maximum crosstalk coupling for an active line terminated in characteristic impedance Z_0 ; quiet line in logical 0 state.

representing device interconnections not terminated in matched loads.

The normal modes method,^{13,14} when applied to the multiconductor coupled transmission-line system, provides the most direct procedure for analyzing crosstalk. It is also a more general technique for analyzing coupled lines terminated at one or both ends in device loads. The voltages and currents for mutually N-coupled conductors can be expressed by the following N-coupled transmission-line equations:

$$\frac{\partial \hat{v}}{\partial z} = -[L] \frac{\partial \hat{i}}{\partial t}, \quad (51)$$

and

$$\frac{\partial \hat{i}}{\partial z} = -[C] \frac{\partial \hat{v}}{\partial t}, \quad (52)$$

where $[L]$ and $[C]$ are the inductance and capacitance matrixes, respectively. These equations are valid for the case of quasi-TEM transmission. At frequencies below 2 GHz, the mode of propagation along striplines and microstriplines is approximately TEM, so the following analysis should apply for most digital circuit applications.

Making the assumption of a time harmonic wave of the form $e^{j(\omega t - \beta z)}$, the voltages and currents in Eqs. 51 and 52 can be decoupled to yield

$$([L][C] - \lambda [I]) \hat{v} = 0, \quad (53)$$

and

$$([C][L] - \lambda [I]) \hat{i} = 0. \quad (54)$$

These equations represent a generalized eigenvalue and eigenvector problem whose method of solution is well known. The eigenvalues in this case represent the inverse of the square of the propagation velocities for each of the N-coupled modes. The solution of the eigenvector problem yields the matrix of eigenvectors $[M_v]$ for the voltages. Also, because the matrixes $[L]$ and $[C]$ are adjoint, the matrix of eigenvectors for the current $[M_i]$ can be determined from the relation

$$[M_i] = [[M_v]^T]^{-1}. \quad (55)$$

The coupled voltages and currents are related to the uncoupled voltages and currents through the relations

$$\hat{v} = [M_v] \hat{v}', \quad (56)$$

and

$$\hat{i} = [M_i] \hat{i}'. \quad (57)$$

From Eq. 51 the current and voltage eigenvectors are related via the relation

$$[M_v] = [\lambda]^{-1} [L] [M_i]. \quad (58)$$

Substituting $\hat{v} = [M_v] \hat{v}'$ and $\hat{i} = [M_i] \hat{i}'$ into the transmission line equations yields the set of N-uncoupled equations

$$\frac{\partial \hat{v}'}{\partial z} = -[L'] \frac{\partial \hat{i}'}{\partial t}, \quad (59)$$

and

$$\frac{\partial \hat{i}'}{\partial z} = -[C'] \frac{\partial \hat{v}'}{\partial t}, \quad (60)$$

where $[L']$ and $[C']$ are diagonal matrixes given by

$$[L'] = [M_v]^{-1} [L] [[M_v]^T]^{-1}, \quad (61)$$

and

$$[C'] = [M_v]^T [C] [M_v]. \quad (62)$$

The set of uncoupled transmission lines in Eqs. 59 and 60 can be solved using a circuit-analysis program such as SPICE,¹⁴ which will be discussed in detail in the section, "Analyzing Reflections and Crosstalk for the N-Conductor Transmission Line." An alternative computational approach¹⁵ that will be discussed here uses a method equivalent to the addition of successive reflections to the incident voltage at a source or to the transmitted pulse at the terminating load.

As before, let the matrix $[\lambda]$ be the diagonal matrix of eigenvalues and $[M_v]$ and $[M_i]$ be the corresponding voltage and current eigenvectors. The characteristic impedance matrix can be defined in terms of the current and voltage eigenvectors as

$$[M_v] = [Z_0] [M_i]. \quad (63)$$

Through the use of Eqs. 58 and 63, the impedance matrix $[Z_0]$ can be expressed by the relation

$$[Z_0] = [\lambda]^{-1} [L] . \quad (64)$$

The source end transmission and reflection coefficients can be found from the relations

$$[\tau_s] = [Z_0] \{ [R_s] + [Z_0] \}^{-1} , \quad (65)$$

and

$$[\rho_s] = \{ [R_s] - [Z_0] \} \{ [R_s] + [Z_0] \}^{-1} , \quad (66)$$

where $[R_s]$ is the source load matrix.

The load end reflection coefficient is given by the relation

$$[\rho_l] = \{ [R_l] - [Z_0] \} \{ [R_l] + [Z_0] \}^{-1} , \quad (67)$$

where $[R_l]$ is the load resistance matrix.

The modal transmission and reflection coefficients can be related to the modal voltages through the relations

$$[\tau'_s] = [m_v]^{-1} [T_s] , \quad (68)$$

$$[\rho'_s] = [M_v]^{-1} [\rho_s] [m_v] , \quad (69)$$

and

$$[\rho'_l] = [M_v]^{-1} [\rho_s] [M_v] . \quad (70)$$

The relationship between the actual voltage and the incident and reflected mode voltages can be expressed through the relationship

$$\hat{V} = [M_v] \{ \hat{V}'_{inc} + \hat{V}'_{ref} \} . \quad (71)$$

A computer program based on these results was written to evaluate the crosstalk between two coupled transmission lines. Since the coupling between an n -line system of equally spaced parallel conductors will yield only two modes of transmission,¹⁶ understanding the coupling in the two-line system can be quite useful for studying parallel bus structures. The nonlinear-device output impedances are simplified by using the dynamic output resistance for the active-line source impedance and the static output resistance for the quiet line. The model for this analysis is illustrated in Fig. 8. The computer crosstalk model was subsequently used to analyze various interconnect structures discussed in this report. The source code for this program is presented in Appendix B.

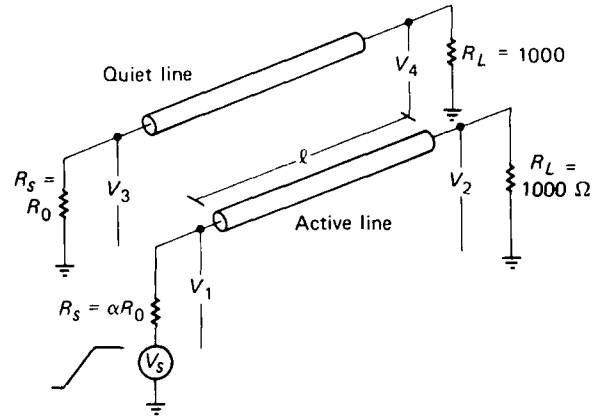


Figure 8 Model for crosstalk analysis of coupled two-line system.

ATTENUATION AND DISPERSION EFFECTS

In order to pass a complex signal along a transmission line without distortion, the attenuation and phase velocity for various frequency components must be constant with the frequency. In this case the signal will arrive at the end of the line somewhat attenuated but possessing the same characteristic form. Thus, for distortionless transmission the attenuation must be constant with frequency and the phase velocity must be constant (or equivalently, the phase constant must be proportional to the frequency).

Now in general, the propagation constant is given by the relationship

$$\gamma = \sqrt{(R + j\omega L)(G + j\omega C)} . \quad (72)$$

For the low loss condition (i.e., $R \ll \omega L$ and $G \ll \omega C$), the real and imaginary portions of the complex propagation constant can be approximated using the binomial expansion to yield

$$\alpha \approx \frac{R}{2} \sqrt{\frac{C}{L}} + \frac{G}{2} \sqrt{\frac{L}{C}} , \quad (73)$$

and

$$\beta \approx \omega \sqrt{LC} \quad (74)$$

where α is the attenuation constant and β is the phase constant. The first term in the attenuation constant is

that resulting from the resistive losses while the second represents that resulting from lossy dielectric insulator materials. The conductance is highly dependent on the frequency (see Eq. 45) but is typically small for most circuit board materials, compared to the resistive losses. Signal distortion (i.e., frequency dependence) resulting from resistive losses occurs as a result of the high frequency skin effect.

Skin Effect

Skin effect is important at high frequencies where current flow is essentially concentrated in a thin layer or skin near the surface of the conductor. A broader definition of skin effect indicates that it is a phenomenon that tends to concentrate currents on the surfaces of conductors closest to the field sources that produce them.¹⁷ This definition includes proximity effects resulting from currents (i.e., magnetic field) on nearby conductors. The two primary results of this phenomenon include an increase in the AC resistance of the conductor (that results from the reduced penetration of the current into the conductor) and a change in the inductance. The percentage of reduction in the inductance from the low frequency case to the ultra high frequency case is typically small. The resistance change from the DC case, however, is a monotonically increasing function of the frequency. In the past, resistive losses in signal lines were not a problem for conventional silicon device technologies and printed circuit boards, especially in digital applications. However, with the subnanosecond digital device technologies (e.g., gallium arsenide) and the reduction of signal-line traces to accommodate the increased circuit densities of VLSI/VHSIC devices, losses from skin resistance are receiving greater attention.

Numerous methods have been employed to calculate skin resistance, with varying degrees of success; typically, the TEM wave approximation is employed. This assumption restricts the current flow to the direction along the length of the conductor and reduces the vector equation to a scalar one, although the problem remains highly nonlinear. The nonlinear nature of the skin effect arises from the fact that the fields producing the current distribution are constantly being modified by the resulting changes in the current distribution. To circumvent this nonlinearity the driving field is usually approximated by a field obtained by solving the skin effect problem in the low frequency limit.

In the TEM approximation the electromagnetic field is independent of the z-direction, and the current density will exhibit a z-component only. In this case the magnetic field will have transversal components only,

and thus the vector potential will have a component in the z-direction only. For this situation the governing equation

$$\nabla \times \nabla \times \mathbf{A} = \mu \left(\mathbf{J} + \frac{\partial \mathbf{D}}{\partial t} \right), \quad (75)$$

and the Lorentz condition

$$\nabla \cdot \mathbf{A} = -\mu\epsilon \frac{\partial \phi}{\partial t}, \quad (76)$$

yield the inhomogeneous wave equation

$$\nabla^2 \mathbf{A} - \mu\epsilon \frac{\partial^2 \mathbf{A}}{\partial t^2} = -\mu \mathbf{J}. \quad (77)$$

In the analysis of static magnetic fields, this equation reduces to the Poisson equation,

$$\nabla^2 \mathbf{A} = -\mu \mathbf{J}. \quad (78)$$

A homogeneous wave equation, especially useful at lower frequencies, can be formulated by choosing the divergence of $\mathbf{A}$ judiciously:

$$\nabla \cdot \mathbf{A} = -\mu\sigma\phi - \mu\epsilon \frac{\partial \phi}{\partial t}. \quad (79)$$

This condition yields the homogeneous wave equation

$$\nabla^2 \mathbf{A} - \mu\sigma \frac{\partial \mathbf{A}}{\partial t} - \mu\epsilon \frac{\partial^2 \mathbf{A}}{\partial t^2} = 0. \quad (80)$$

First we consider the portion of the domain that lies inside the conductors. Because the current density is not explicit in this formulation, we need to make the assumption that the vector potential $\mathbf{A}$ can be divided into the sum of the corresponding static potential $\mathbf{A}_0$ and the time varying portion $\mathbf{A}'$,¹⁸

$$\mathbf{A} = \mathbf{A}_0 + \mathbf{A}'. \quad (81)$$

The static solution can be found by solving Eq. 78 for the static field problem.

In the case of sinusoidal time variation, the homogeneous wave equation can be cast in the following form:

$$\nabla^2 \mathbf{A}' + j\omega\mu\sigma \mathbf{A}' = \mu \mathbf{J}_0 + j\omega\mu\sigma \mathbf{A}_0. \quad (82)$$

For good conductors at frequencies below 2 GHz, the real term is typically small and can be neglected. However, because (a) the finite element method will be discussed with respect to obtaining approximate solutions to skin effect problems, and (b) the exclusion of the latter term in Eq. 81 offers no significant reduction in computational effort, the real term need not be discarded.

In Eq. 82, J_0 represents the known current distribution in the low-frequency limit. For simplicity we can rewrite this equation as

$$\nabla^2 A' + k^2 A' = S_0 \quad (83)$$

where

$$S_0 = \mu J_0 + j\omega\mu_0 A_0,$$

$$k = \sqrt{j\omega\mu\sigma}.$$

The complex current density S_0/μ is the sum of the current density and the eddy current density. This formulation, therefore, uses static current and vector potential as loads for approximating the time-varying vector potential in the TEM approximation.

Outside the conductors, assuming sinusoidal time variation, Eq. 80 takes the form

$$\nabla^2 A' + \mu\epsilon\omega^2 A' = -\mu\epsilon\omega^2 A_0. \quad (84)$$

Here we have neglected the complex term because the conductivity of the insulating medium is assumed to be quite small and thus may be neglected.

Finding approximate solutions to this problem can best be accomplished through the use of the finite element method. This method requires the existence of a variational formulation for Eq. 84. Unfortunately, the operator L ,

$$L = \nabla^2 + k^2 \quad (85)$$

for this equation is non-self-adjoint; i.e.,

$$\langle u, Lv \rangle \neq \langle Lu, v \rangle, \quad (86)$$

where u and v are any two vectors in the domain of L . Thus, a variational formulation for this problem in the classical sense does not exist.

Recently, several authors^{19,20} have proposed a method for solving the non-self-adjoint problem by introducing an auxiliary problem, i.e., the adjoint problem, as follows:

$$L^u u^u = S^u, \quad (87)$$

where L^u is the adjoint operator of L (in our case, the complex conjugate operator), u^u is the adjoint field, and S^u is the adjoint source function. We can choose the adjoint source function S_0^u to be equal to S_0 without any restrictions.

Using the method of weighted residuals, we can write the weak formulation of the non-self-adjoint problem as

$$\int_{\Omega} u^{u*} (\nabla^2 u + k^2 u - S_0) d\Omega + \int_{\Omega} (\nabla^2 u^u - k^2 u^u - S_0^u)^* u d\Omega = 0, \quad (88)$$

where we have used the adjoint or complex conjugate field for the test (or weight) function for the original problem and the non-self-adjoint field as the test function for the adjoint problem. It has been shown that the problem of solving for both u and u^u simultaneously is equivalent to determining the stationarity of both fields from Eq. 88.²¹ We can reformulate Eq. 88 in the symmetric form with the aid of Green's theorem. This results in the functional

$$F = -2 \int_{\Omega} \nabla u^{u*} \cdot \nabla u d\Omega + 2sk^2 \int_{\Omega} u^u u d\Omega - \int_{\omega} u^{u*} S_0 d\Omega - \int_{\omega} S_0^u u d\Omega. \quad (89)$$

Here we have assumed the natural homogeneous boundary conditions,

$$\frac{\partial A}{\partial n} = 0 \text{ (at symmetry lines)}, \quad (90)$$

and

$$A = 0 \text{ (along flux lines)} \quad (91)$$

on the external boundary.

Thus, we have arrived at a variational formulation consistent with the prescribed boundary conditions. The homogeneous Dirichlet boundary conditions, $A = 0$ apply at conductor interfaces or along magnetic field flux lines (where the normal component of the electric field vanishes) while the homogeneous Neumann boundary conditions, $\partial A / \partial n = 0$, can be applied along magnetic field symmetry lines or at iron surfaces.

Application of the appropriate boundary condition implies that some apriori knowledge of the magnetic field distribution can be assumed.

We can proceed with our formulation of the variational equation for the skin resistance by employing the Galerkin method. This method states that the best solution to the above weak variational formulation can be found by choosing the same expansion functions for both the weight function (adjoint field-original field) and that used to approximate the field variable (original field-adjoint field). We approximate u and u^a with the series expansion

$$u = \sum_{n=1}^N a_n \phi_n, \quad (92)$$

and

$$u^a = \sum_{n=1}^N a_n^a \phi_n^a, \quad (93)$$

where the expansion functions (ϕ_n) and (ϕ_n^a) are chosen to be equal (Galerkin's result) and should form a complete set of linearly independent functions. Also, the expansion functions must satisfy the boundary conditions for both the original and the adjoint operator equations. Moreover, the original and adjoint fields must be such that they satisfy the homogeneous Dirichlet conditions at the boundaries. The coefficients a_n and a_n^a are complex and can be adjusted for any set of linear expansion functions so that the boundary conditions may be satisfied.

Inserting Eqs. 92 and 93 into Eq. 91, we arrive at the variational statement (assuming homogeneous boundary conditions),

$$\begin{aligned} F = & -2 \int_{\Omega} \sum_i a_i^{a*} \nabla \phi_i^* \sum_j a_j \nabla \phi_j d\Omega \\ & + 2k^2 \int_{\Omega} \sum_i a_i^{a*} \phi_i^* \sum_j a_j \phi_j d\Omega - \int_{\Omega} \sum_i a_i^{a*} \\ & \phi_i d\Omega - \int_{\Omega} S_0 \sum_j a_j \phi_j d\Omega. \end{aligned} \quad (94)$$

Taking the first variations with respect to the coefficients a_k and a_k^a we get the following two decoupled equations:

$$\begin{aligned} \frac{\partial F}{\partial a_k^a} = & -2 \sum_j a_j \int_{\Omega} \nabla \phi_k^* \nabla \phi_j d\Omega \\ & + 2k^2 \sum_j a_j \int_{\Omega} \phi_k^* \phi_j d\Omega - \int_{\Omega} S_0 \phi_k d\Omega \equiv 0, \end{aligned} \quad (95)$$

and

$$\begin{aligned} \frac{\partial F}{\partial a_k} = & -2 \sum_i a_i^{a*} \int_{\Omega} \nabla \phi_i^* \nabla \phi_k d\Omega \\ & + 2k^2 \sum_i a_i^{a*} \int_{\Omega} \phi_i \phi_k d\Omega \\ & - \mu \int_{\Omega} S_0 \phi_k d\Omega \equiv 0. \end{aligned} \quad (96)$$

From these equations we can estimate the complex coefficients a_k and a_k^a (using complex matrix arithmetic, of course). The magnetic fields can then be determined once the magnetic vector potential A has been determined. The skin resistance is then given by the relation²²

$$R = \frac{R_m}{I_0 I_0^*} \oint \mathbf{H} \cdot \mathbf{H}^* dl. \quad (97)$$

The inductance can be estimated using the relation

$$L = \frac{\mu}{I_0 I_0^*} \oint \mathbf{H} \cdot \mathbf{H}^* dl. \quad (98)$$

The above analysis yields a straightforward implementation of the finite-element approach for solving the non-self-adjoint skin effect equation. The only additional requirement for implementing this method is the use of complex matrix arithmetic.

POWER AND GROUND NOISE

In high speed digital applications, maintaining low AC impedance and low DC resistance in power supply lines and ground returns is desirable for preserving device noise margins and switching speeds. The large current requirements for high density, high speed circuitry can cause shifts in ground potentials that can affect both low-state and high-state noise margins in TTL and ECL circuits. Inductance in power supply leads (V_{cc}) can

produce large switching transients, particularly in TTL circuits.

Noise generation stems from the rapid change in current demand when a device changes state. Additional current may be required for charging or discharging a large load capacitance. This transient current pulse propagating through the inductance of power supply leads can produce large voltage spikes.

Devices are generally more sensitive to voltage spikes on ground-return leads than on power-supply leads. Inductive voltage spikes generated on ground returns can produce undesirable noise transients that may be picked up by devices terminated nearby.

In most situations the resistive voltage drop can be lowered by using higher-conductivity conductor materials and larger ground-conductor crosssectional areas. The inductance of ground conductors is generally more difficult to control since it is primarily dependent upon the conductor geometry. Both the inductance and resistance of ground conductors can be decreased by increasing the width of printed conductor leads. For this reason solid conductor planes are generally used for more efficient distribution of power and ground. The self-inductance of these planes is also affected by their proximity to nearby conductors. Eddy currents can form in secondary conductors, inducing currents in the same direction as the primary currents. These induced currents then act to reduce the net fields between the conductors, thereby effectively reducing the inductance of the current-carrying conductor. Thus, bringing power and ground planes closer will favorably increase power supply decoupling while significantly reducing the inductance of power- and ground-return leads.

Power and ground planes may be either a continuous conductor sheet or a perforated conductor sheet. Solid ground planes often pose a manufacturing problem in fabricating multilayer circuit boards when the adhesion between insulator and conductor materials is relatively poor. In these cases the perforated or grid plane is used in place of the continuous conductor plane. Gridded ground planes are also used when it is necessary to reduce the capacitive coupling of signal lines to ground. This is particularly useful for multilayer thick-film circuits where the dielectric constant of the insulator is particularly high. Ground and power planes should be arranged in the multilayer stack in such a way as to conform to either a microstrip or, preferably, a stripline configuration. Ground and power planes are also used in high speed multilayer packages to provide transmission line leads for signals, to help reduce crosstalk, and to provide EMI (electromagnetic interference) shielding, in addition to efficient power and ground distribution.

SPICE CIRCUIT SIMULATION FOR MODELING PERFORMANCE OF HIGH SPEED DEVICE INTERCONNECTIONS

We have previously presented methods for estimating circuit parameters and transmission line characteristics. Now, the next logical step in the evaluation of circuit performance is to simulate the high speed signal transmission using a network analysis program such as SPICE (Simulation Program for Integrated Circuit Evaluation). We will now illustrate the use of SPICE for analyzing crosstalk, reflections, delay, and dispersion, using appropriate circuit modeling techniques.

Distributed Line Analysis

At high frequencies when simple, lumped, element models are not appropriate for analyzing signal line transmission, distributed element modeling of the transmission line may be required.

For lossless, or nearly lossless, transmission lines, analysis is handled most conveniently with a simple SPICE transmission line element. In this case all of the pertinent circuit parameters are included in the element definition statement (i.e., characteristic line impedance and propagation constant) and the transmission line behaves like a simple delay element with a prescribed amount of attenuation.

For lossy transmission lines the characteristic impedance is complex, and the analysis of signal line transmission can be more easily accommodated through the use of distributed circuit elements. In Fig. 9 a differential section of a transmission line is depicted, including all of the pertinent signal line parameters as we have previously discussed. This differential section of a lossy transmission line is adequate to represent a signal whose highest significant wavelength is at least 10 times greater than the length of the distributed section. Obviously, simulations using distributed circuit analysis techniques will become increasingly more complex at ultra-high frequencies. However, this representation should be adequate for most digital signal applications.

As an example, the case of reflections for a clock pulse generated from a device with an output impedance of approximately $40\ \Omega$, interconnected to the input of a high-impedance device through a lossy, low impedance section of transmission line, is examined. The situation is illustrated in Fig. 10. This example was chosen to approximate a situation where a 40 MHz shift register on a wire wrap board was used to generate a clock pulse on a ceramic digital circuit board using Series ALS TTL devices. Some of the clock lines on the ceramic board were exceedingly long (≈ 8 in.) and the capacitance per unit length was quite high (≈ 23 pF/in.). This was be-

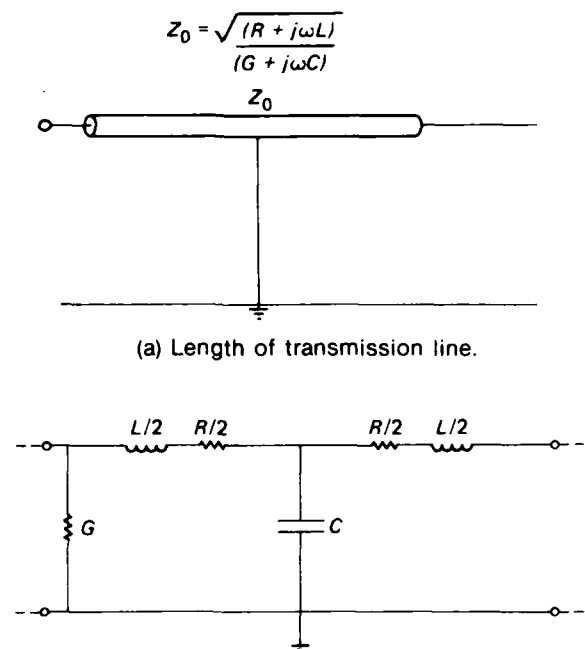


Figure 9 Transmission line (a) and incremental circuit model (b) for a section of transmission line.

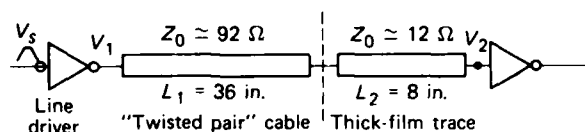
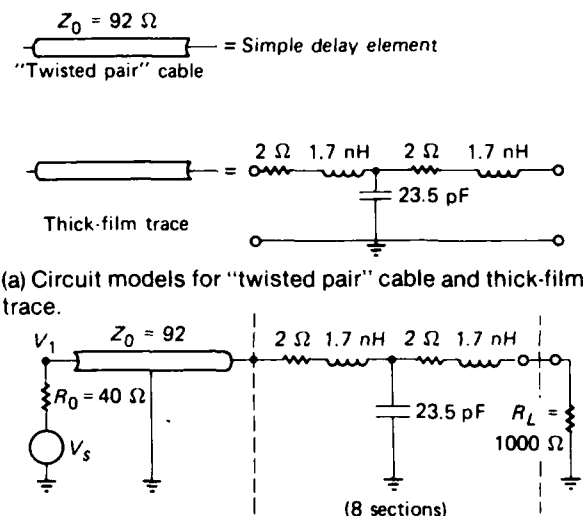


Figure 10 Interconnection model for SPICE simulation.

cause of the close proximity of these lines to the underlying ground plane and the high K for the dielectric material. In addition, the conductor lines were fabricated from a high resistivity conductor material. In testing the board it was discovered that the low impedance clock line was degrading the performance of the system. To overcome this difficulty the clock speed had to be reduced to overcome the effects of high capacitive loading.

The circuit parameters for the multilayer thick-film circuit used for this simulation were obtained using methods discussed previously. These parameters were then incorporated into a distributed SPICE model for the device interconnections (Fig. 11). The device output impedance was modeled with a resistor that was equivalent to the average dynamic output resistance for the device driving the line. The input impedance was modeled using a nominal 1000- Ω resistance. The SPICE



(b) SPICE circuit model for interconnection of Fig. 10.

Figure 11 SPICE model for the circuit of Fig. 10.

input file for this analysis is depicted in Table 2. The results of the analysis, compared with the measured voltage at the receiving end of the line, are shown in Fig. 12 for a 4-nsec input ramp pulse. The figure illustrates the equivalent features for both the simulated and measured clock signals.

A second analysis was performed in which the ground plane was isolated from the clock by adding more layers of dielectric between the signal line and the ground plane and by using a higher conductivity conductor material. These results, shown in Fig. 13, indicate the vast improvement in switching characteristics for this particular situation.

This example, which requires first an estimate of the circuit parameters (using methods discussed previously) and then a relatively simple SPICE analysis, illustrates the usefulness of simulation methods. These techniques are particularly useful for determining the suitability of various interconnection schemes for VLSI and VHSIC device technologies.

Analyzing Reflections and Crosstalk for the N-Conductor Transmission Line

Once the capacitance and inductance matrix of the system have been determined, reflections and crosstalk for the lossless n -conductor transmission lines can be analyzed using a multipurpose circuit analysis program such as SPICE. The analysis involves considering a 2n-port model for the device interconnections that consist of linear dependent sources (current and voltage) and transmission lines. The model is similar to that discussed

Table 2
A representative SPICE model for the device interconnection shown in Fig. 11b.

```
' description: distributed circuit
dim
    freq hz
    lng in
    ang rad
    res oh
    ind h
    cap f
ckt
    tlinp_t1 1 2 2=92 1=4 k=3.0 a=.05 f=100e+6 ' twisted pair cable
    ind_l01 2 3 1=25.2e-9 ' connector inductance
    res_r01 3 4 r=8 ' beginning of distributed transmission line
    cap_c01 4 0 c=21e-12
    ind_l02 4 5 1=3.32e-9
    res_r02 5 6 r=8
    cap_c02 6 0 c=21e-12
    ind_l03 6 7 1=3.32e-9
    res_r03 7 8 r=8
    cap_c03 8 0 c=21e-12
    ind_l04 8 9 1=3.32e-9
    res_r04 9 10 r=8
    cap_c04 10 0 c=21e-12
    ind_l05 10 11 1=3.32e-9
    res_r05 11 12 r=8
    cap_c05 12 0 c=21e-12
    ind_l06 12 13 1=3.32e-9
    res_r06 13 14 r=8
    cap_c06 14 0 c=21e-12
    ind_l07 14 15 1=3.32e-9
    res_r07 15 16 r=8
    cap_c07 16 0 c=21e-12 ' end of distributed transmission line
    res_rl 16 0 r=10000 ' load resistance
    def2p 1 16 line ' 2-port network "line"
source
    line ivs_v1 20 0 tran=pulse(0 4 0 4e-9 4e-9 71e-9 100e-9)
    line res_rs 20 1 r=42 ' device dynamic output resistance
control
    line tran .8e-10 170e-9 0 .8e-10
spiceout
    line tran v(20) v(16)
```

in Refs. 13 and 14 and can be derived from the method of normal modes.

The method of normal modes for the lossless transmission line was discussed in the Section, "Voltage Crosstalk for the N-Conductor System." Here, the diagonalized inductance $[L']$ and capacitance $[C']$ matrices were introduced, which then resulted in a set of decoupled transmission line equations. A normal-mode characteristic impedance and propagation velocity for the k th uncoupled line can be given by the following relationships:

$$Z_k = \sqrt{\frac{L'_k}{C'_k}}, \quad (99)$$

and

$$u_{pk} = \frac{1}{\sqrt{\lambda_k}}, \quad (100)$$

where L'_k and C'_k are the mode equivalent inductance and capacitance, respectively, and λ_k is the k th eigenvalue of Eq. 53.

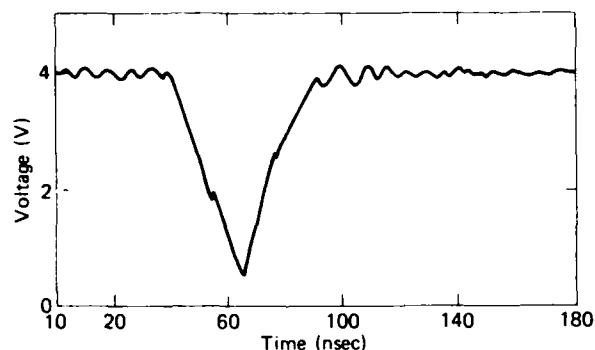
The normal mode currents and voltages can be represented in terms of the uncoupled voltages by means

of the matrix transformation equation as

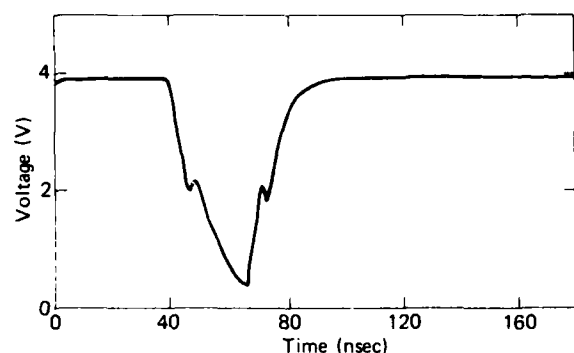
$$\hat{v} = [M_v] \hat{v}', \quad (101)$$

where $[M_v]$ is the matrix of eigenvectors for the eigenvalue problem given by Eq. 53. The uncoupled transmission lines from Eqs. 59 and 60 lead to the equivalent circuit model for the two-line system, as shown in Fig. 14.

The corresponding SPICE 4-port model for the two-line circuit is shown in Table 3. The input parameters for the model include the propagation velocity for each normal mode (v_k), the normal mode characteristic impedances (Z_k), the eigenvector matrix elements $[M_{ij}]$, and the coupled line length. The nonlinear dynamic source and load impedance for the interconnected devices can be either modeled using the static or dynamic output resistances as discussed in the section, "Electrical Characterization of VLSI/VHSIC Devices," or approximated more closely with the use of SPICE's capability to model a nonlinear resistor. The effect of a nonlinear source resistor on the source input voltage can be modeled by using a SPICE current-controlled voltage-source element.



(a) Measured voltage at V_2 at input of hex inverter (see Fig. 10).



(b) Predicted voltage at V_2 using SPICE simulation.

Figure 12 Measured (a) and simulated (b) waveforms for a low-impedance thick-film circuit trace.

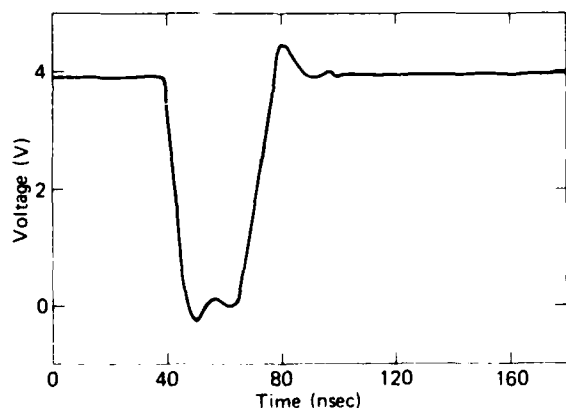
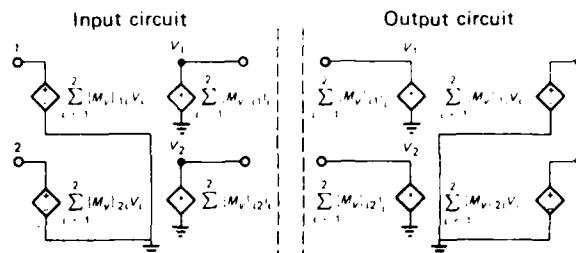
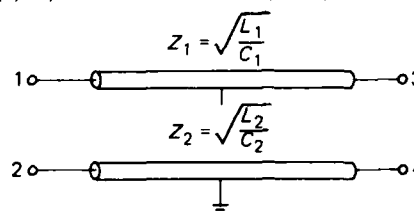


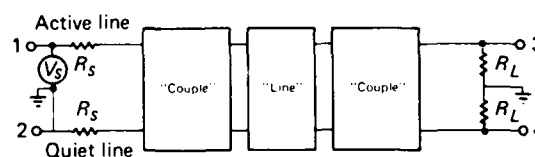
Figure 13 SPICE predicted waveform for the interconnection in Fig. 10 with high-impedance ($\approx 40\Omega$), low-resistance, thick-film trace.



(a) 4-port subcircuit "couple" (see Table 3).



(b) 4-port subcircuit "line" (see Table 3).



(c) 4-port circuit "net" (see Table 3).

Figure 14 SPICE 4-port equivalent circuit for two coupled transmission lines.

Analyzing Dispersion in Periodic Signals

In circumstances where the signal lines are particularly lossy, it is of interest to estimate the degree to which the pulse will be distorted. The most straightforward approach to estimating the shape of the distorted pulse is by means of a Fourier decomposition of the input pulse. Once the input pulse has been decomposed into its constituent components, each frequency component can in turn be passed through a SPICE transmission line with an attenuation constant and phase constant consistent with that particular frequency. At the end of the line, each of the individual frequency components can then be summed to yield the distorted waveform.

The dispersion model for the analysis is depicted in Fig. 15, and the SPICE circuit file is shown in Table 4. In Fig. 16 the undistorted input Fourier waveform (seven harmonics included), the unattenuated output (V_{out}), and the attenuated waveforms are illustrated. They correspond to the input and output waveforms for the transmission line example discussed in the section, "Distributed Transmission Line Analysis." The input pulse was a 40-MHz trapezoidal pulse with a

Table 3
A representative SPICE model code for the coupled two-line system.

```
dim
freq hz
ang rad
cvt
; circuit "couple" which separates the input signals into modes
;
; independent voltage source line 1
vsrc_v1n 10 2 dc=0
; independent voltage source line 2
vsrc_v1l 9 11 dc=0
; voltage controlled voltage source
vsrc_v12 11 9 10 2 .50541
; voltage controlled voltage source
vsrc_v13 11 9 10 2 .77351
; current controlled current source
vsrc_v14 11 9 10 2 .50541
; current controlled current source
vsrc_v15 11 9 10 2 .77351
; voltage controlled voltage source
vsrc_v16 12 9 10 2 .66721
; voltage controlled voltage source
vsrc_v17 12 9 10 2 .67781
; current controlled current source
vsrc_v18 12 9 10 2 .86291
; current controlled current source
vsrc_v19 12 9 10 2 .67781
; define 4-port subcircuit named couple
def4p 1 2 3 4 couple

; transmission line delay circuit "line"
;
; These resistances are required by
; SPICE when independent current
; sources are used since these
; sources have no internal resistance.
res_r1 1 0 r=100000000
res_r2 2 0 r=100000000
res_r3 4 0 r=100000000
; delay line 1
tlin_t1 1 3 .5e-9 .4e-9 en.525 f=100e6
; delay line 2
tlin_t2 2 4 .5e-9 .4e-9 en.112 f=100e6
; define four port network called "line"
couple_c1 1 2 3 4 line
; Separate signal into normal modes
line_c1 2 5 6 7 0
; Delay each mode appropriately
couple_c2 2 4 7 8
; Recombine signals again

; define circuit "net" with load and source resistances
;
; add load resistance to output line 1
res_r11 1 0 r=500
; add load resistance to output line 2
res_r12 4 0 r=500
; add source resistance to input line 1
res_rs2 2 0 r=50
; arbitrary transmission line attached
; to the input
tlin_t3 20 1 .5e-9 en.565 f=100e6
; define 4-port circuit "net"
def4p 1 2 3 4 net

source
net v1 v1 21 0 trimpulse(0 5 0 2e-9 2e-9 4e-9 25e-9) ; voltage source
out res_rs 21 20 r=50 ; source resistance of voltage source
control
net tran 12e-9 40e-9 0 12e-9
spice=it
net tran v(1) v(2) v(3) v(4) v(20)
```

4-nsec rise and fall time. The assumption in this analysis was the use of a lossy (resistive line, i.e., Pt-Au thick-film ink with a sheet resistivity of approximately 40 m Ω per square), low-impedance (12 Ω) thick-film transmission line for the clock pulse (see Fig. 10). The point of this analysis was to observe the effect of a high-resistivity conductor trace on the attenuation at frequencies of interest for thick-film applications.

Comparison of the output waveforms in Fig. 16 indicates that the effect of voltage attenuation is relatively minor when compared to the poor rise- and fall-time characteristics for a low-impedance line. Dispersion effects, however, would become more pronounced as pulse rise and fall times approach the subnanosecond regime.

MODELING PACKAGE INTERCONNECTIONS

For circuit rise and fall times well into the subnanosecond regime, components of the device-to-package in-

terconnects (such as wire bonds, solder joints, package leads, pins, etc.) may introduce transmission line effects that could ultimately limit the useful frequency of a particular package style. For very-high-speed applications, modeling the effects of package leads is essential for determining the suitability of various package types.

In this section several package styles are modeled and then subsequently analysed, using methods discussed in previous sections, to obtain electrical circuit parameters for package leads. The high frequency performance is then evaluated using the TOUCHSTONE microwave software package to obtain a predetermined cutoff frequency in the forward gain transfer function (S_{21} scattering parameter). This cutoff point is somewhat arbitrary, as the amount of losses that can be tolerated depends on the application. However, it is useful to establish some cutoff frequency for comparing various package styles. In the subsequent analysis the cutoff frequency will correspond to only those insertion losses not involving either resistive or dielectric losses. Methods and techniques used for evaluating, design-

Table 4
SPICE model for dispersion in a periodic signal.

```
' circuit filename: dispersion
' description: General example of dispersion
' date/author: 9/16/86/quv
dim
    freq hz
    lng in
    att rad
circuit
    tlinp t1 20 40 2 12 1e8 1e8.7 a=0.0 1e100e+0 'attenuation "a" and
    tlinp t2 21 41 2 12 1e8 1e8.7 a=0.05 1e100e+0 'the effective dielectric
    tlinp t3 22 42 2 12 1e8 1e8.7 a=0.1 1e100e+0 'constant "k" vary with
    tlinp t4 23 43 2 12 1e8 1e8.7 a=0.158 1e100e+0 'frequency
    tlinp t5 24 44 2 12 1e8 1e8.7 a=0.162 1e100e+0
    tlinp t6 25 45 2 12 1e8 1e8.7 a=0.12 1e100e+0
    tlinp t7 26 46 2 12 1e8 1e8.7 a=0.125 1e100e+0
    tlinp t8 27 47 2 12 1e8 1e8.7 a=0.200 1e100e+0
    res rt1 20 10 0 r=40 'source resistance
    res rt2 21 11 0 r=40
    res rt3 22 12 0 r=40
    res rt4 23 13 0 r=40
    res rt5 24 14 0 r=40
    res rt6 25 15 0 r=40
    res rt7 26 16 0 r=40
    res rt8 27 17 0 r=40
    slpa_e1 50 51 [40 0 1] 'voltage controlled voltage sources sum
    slpa_e2 51 52 [41 0 1] 'the contribution from all of the higher
    slpa_e3 52 53 [42 0 1] 'frequency components
    slpa_e4 53 54 [43 0 1]
    slpa_e5 54 55 [44 0 1]
    slpa_e6 55 56 [45 0 1]
    slpa_e7 56 57 [46 0 1]
    slpa_e8 57 0 [47 0 1]
    res rl1 40 0 r=1000 'load resistances
    res rl2 41 0 r=1000
    res rl3 42 0 r=1000
    res rl4 43 0 r=1000
    res rl5 44 0 r=1000
    res rl6 45 0 r=1000
    res rl7 46 0 r=1000
    res rl8 47 0 r=1000
    res rl 50 0 r=1000
    def9p 10 11 12 13 14 15 16 17 50 line
    source 'DC and harmonic voltage sources
    line vvs_v1 10 0 dc=2.0
    line vvs_v2 11 0 transsin(0 2.538 2e+7 0 0 .08058)
    line vvs_v3 12 0 transsin(0 .0232 6e+7 0 0 .2462)
    line vvs_v4 13 0 transsin(0 .4697 1e+8 0 0 .7967)
    line vvs_v5 14 0 transsin(0 .2138 1.4e+8 0 0 .5304)
    line vvs_v6 15 0 transsin(0 .2259 1.8e+8 0 0 .6460)
    line vvs_v7 16 0 transsin(0 .1702 2.2e+8 0 0 .7446)
    line vvs_v8 17 0 transsin(0 .1325 2.6e+8 0 0 .8280)

control
    line tran .2e 9 100e-9 0 .9e-10
spiceout
    line tran v(50)
```

ing, or specifying standard and custom VLSI and VHSIC packages will be discussed and results presented for several package styles.

68-Pin JEDEC-Type A Leadless Ceramic Chip Carrier

In Fig. 17 the signal path for a typical chip carrier lead is shown schematically. For the 68-pin LCCC we have chosen to represent the interconnection with six independent transmission line segments as depicted in Fig. 18. Each of the individual segments can be modeled approximately using the two-dimensional boundary element techniques discussed previously. More accurate representations would require three-dimensional capacitance and inductance calculations. At the frequencies encountered in high speed digital ap-

plications, the time and expense of carrying out these more complex calculations are usually not warranted. Once we have characterized the transmission line parameters for each of the individual segments, a touchstone file can be written that uses these values as data input for an s-parameter evaluation. Frequencies over the range of interest can be swept, and the forward gain parameter, s_{12} can be calculated as a function of frequency.

In Fig. 19 the forward gain plot is shown for a corner pin of a 68-pin LCCC (with wirebonds) terminated in 50- Ω impedance. The plot shows that the -3-dB point is beyond 9 GHz for the standard chip carrier package (with no integrated ground planes); however, there is significant degradation just above 4 GHz. The

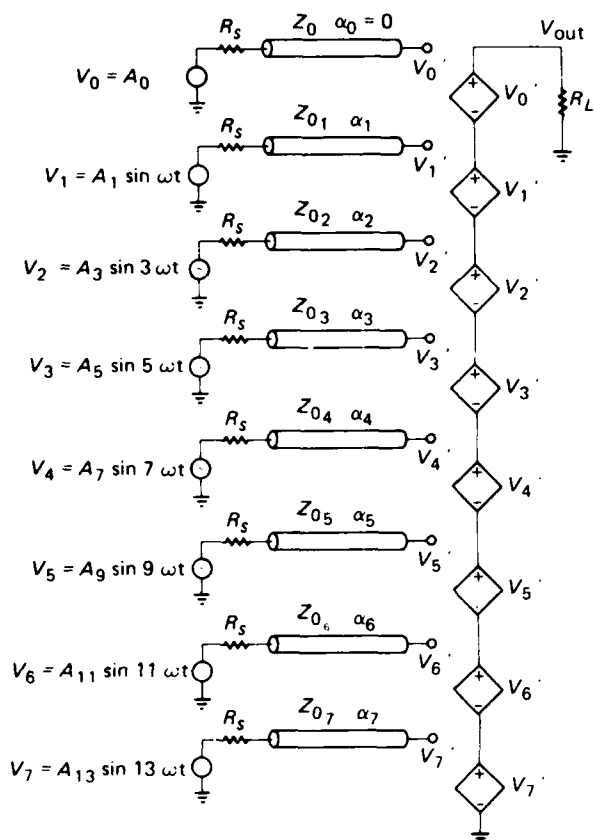


Figure 15 Dispersion model for lossy transmission lines or device interconnections.

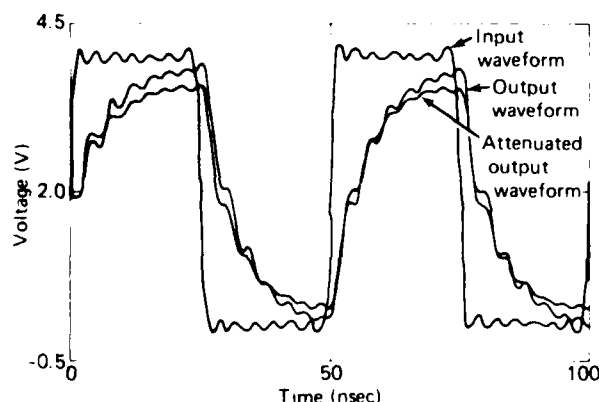


Figure 16 Effect of high resistivity conductors on signal attenuation for the example illustrated in Fig. 10.

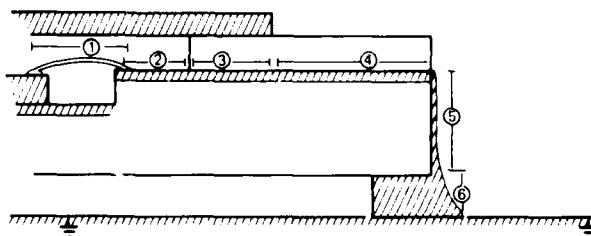


Figure 17 Signal path for a representative chip carrier lead.

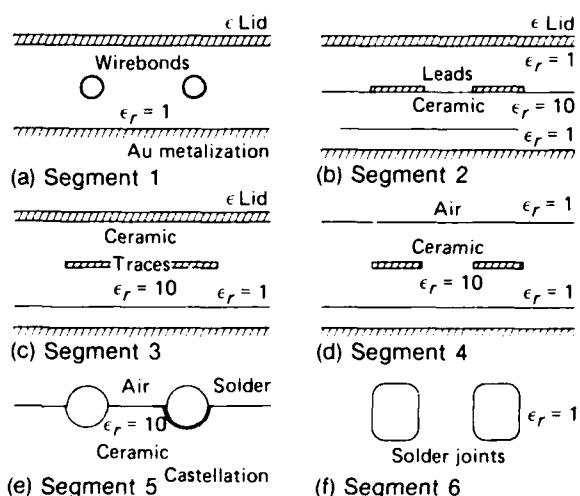


Figure 18 Chip carrier package leads represented by a series of transmission line segments.

same calculation was repeated, with the wirebonds replaced with a 50-Ω microstrip TAB bond (two-layer tape with one layer reserved for a ground plane). With this adjustment the plot shown in Fig. 20 indicates no significant insertion losses below 9 GHz. Of course, in this figure the -3-dB point has been extended well beyond the validity of the model (no accounting for skin or coupling losses). Thus, the primary factor influencing the insertion losses are the package wirebonds. It is important to note, however, that non-transmission-line TAB bonds, isolated from ground, would suffer much of the same nondissipative losses that wirebonds exhibit. TAB performance should outperform wirebonds only at much higher frequencies where skin-effect losses tend to predominate.

68-Lead Pin Grid Array Package

Standard cofired ceramic pin grid array (PGA) packages closely resemble the cofired ceramic leadless chip

carrier except that the PGA has brazed pins. These brazed pins are responsible for much of the difference in performance between the chip carrier and pin-grid array. In Fig. 21 the forward gain is plotted for the case where the substrate lead ties into the pin at the bottom portion of the pin. For this case we see that the performances of the LCCC and the PGA are nearly equal. However, when the pin is connected to the signal trace near the braise location, the performance differs by quite

a significant margin. This configuration results in an unterminated stub condition as shown in Fig. 22. The forward gain plot for this case indicates that the -3 -dB point occurs at about 3.5 GHz, while significant losses are already occurring at 2.5 GHz; these calculations assume a pin length of 0.15 in. Performance can be improved with the use of a $50\text{-}\Omega$ TAB and by reducing the length of unterminated stubs.

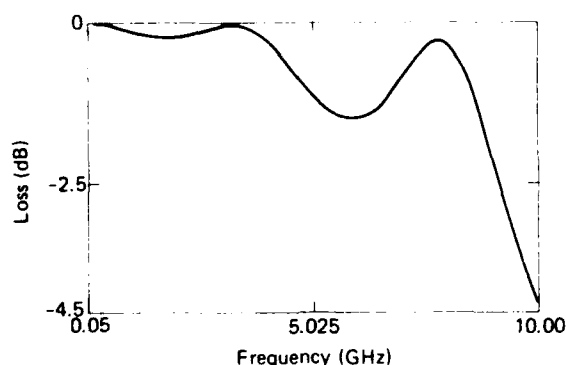


Figure 19 Forward gain (S_{21} scattering parameter) as a function of frequency for the corner lead of 68-pin leadless chip carrier.

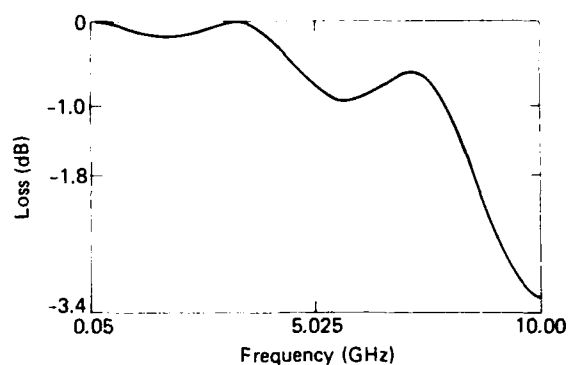


Figure 21 Forward gain (S_{21}) for a 68-lead pin grid array package connected in a no-stub configuration.

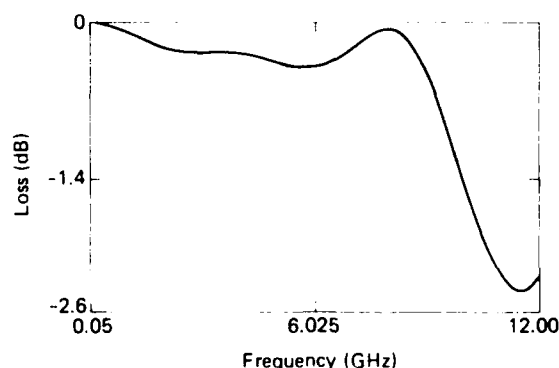


Figure 20 Forward gain (S_{21} scattering parameter) as a function of frequency for the corner lead of a 68-pin chip carrier with wirebonds replaced with $50\text{-}\Omega$ TAB bonds.

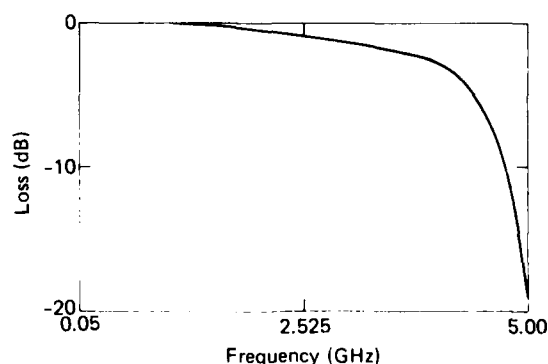


Figure 22 Forward gain (S_{21}) as a function of frequency for a 68-lead pin grid array corner lead with unterminated stub.

7. EXPERIMENTAL METHODS FOR CHARACTERIZING DEVICE AND PACKAGE INTERCONNECTIONS

NETWORK ANALYZER TECHNIQUES

Measurement of Transmission Line Parameters

The s -parameter method can be a useful technique for determining the dissipative losses in high speed transmission line structures.²³ For a lossy line with characteristic impedance Z_0 between a source with internal impedance Z_0 and a termination impedance Z_0 , the scattering matrix may be defined as

$$S = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} = \begin{bmatrix} 0 & \alpha e^{-\tau j\omega} \\ \alpha e^{-\tau j\omega} & 0 \end{bmatrix}, \quad (102)$$

where τ is the time delay and $j\omega$ is the frequency variable, and $-20 \log_{10} \alpha$ is the total attenuation for a length l of transmission line.

For the same line terminated at both the source and load ends in a $50\text{-}\Omega$ impedance (as is the case for most s -parameter test setups), the new scattering parameters s_{11} and s_{21} can be rewritten as

$$S_{11} = \frac{\rho_1 + S_{11} + \rho_1 \rho_2 S_{22} + \rho_2 \Delta S}{1 + \rho_1 S_{11} + \rho_2 S_{22} + \rho_1 \rho_2 \Delta S}, \quad (103)$$

$$S_{21} = \frac{S_{21} \sqrt{(1 - \rho_1^2)(1 - \rho_2^2)}}{1 + \rho_1 S_{11} + \rho_2 S_{22} + \rho_1 \rho_2 \Delta S}, \quad (104)$$

where $\Delta S = s_{11}s_{22} - s_{12}s_{21}$ and $\rho_1 = \rho_2 = \rho = \frac{Z_0 - 50}{Z_0 + 50}$.

Thus, from Eqs. 102, 103, and 104, we can derive the following relations:

$$S_{11} = \frac{\rho (1 - \alpha^2 e^{-2\tau j\omega})}{1 - \rho^2 \alpha^2 e^{-2\tau j\omega}}, \quad (105)$$

and

$$S_{21} = \frac{\alpha e^{\tau j\omega} (1 - \rho^2)}{1 - \rho^2 \alpha^2 e^{-2\tau j\omega}}. \quad (106)$$

With $p = j\omega$ and $\rho^2 = |\rho|^2$,

$$|S_{11}|^2 = \frac{\rho^2 |1 - \alpha^2 e^{-j2\omega\tau}|^2}{|1 - \rho^2 \alpha^2 e^{-j2\omega\tau}|^2}, \quad (107)$$

and

$$|S_{21}|^2 = \frac{\alpha^2 |1 - \rho^2|^2}{|1 - \rho^2 \alpha^2 e^{-j2\omega\tau}|^2}. \quad (108)$$

When $e^{j2\omega\tau} = 1$, i.e., when the frequency ω is a multiple of one-half the wavelength of the line, Eqs. 107 and 108 become

$$|S_{11}|^2 = \frac{\rho^2 (1 - \alpha^2)^2}{(1 - \rho^2 \alpha^2)^2}, \quad (109)$$

and

$$|S_{21}|^2 = \frac{\alpha^2 (1 - \rho^2)^2}{(1 - \rho^2 \alpha^2)^2}. \quad (110)$$

The half-wavelength frequencies can best be determined by measuring the transmission maxima in swept frequency measurements of the line.

Equations 109 and 110 can be solved simultaneously for the unknowns, ρ and α , resulting in the following two quadratic equations:

$$\alpha^2 + \alpha \left(\frac{|S_{11}|^2 - |S_{21}|^2 - 1}{|S_{21}|} \right) + 1 = 0, \quad (111)$$

and

$$|\rho|^2 + |\rho| \left(\frac{|S_{21}|^2 - |S_{11}|^2 - 1}{|S_{11}|} \right) + 1 = 0. \quad (112)$$

Thus, both ρ (and thus the characteristic impedance) and α can be determined assuming that both S_{11} and S_{21} can be measured. This method becomes impractical for measuring characteristic line impedances whose values are close to that for the source and load impedances. This is a result of difficulty in accurately determining the half-wavelength intervals of the line.

Insertion Loss Techniques For Package Analysis.

This method involves the use of a network analyzer and an s -parameter test setup. The parameter S_{12} is scanned over a range of frequencies, and the gain response can be determined as a function of the frequency. This method is identical to that described in the section, "Modeling Package Interconnections." Assuming that the frequency can be related to the rise time of the circuit via the relationship given in Eq. 4, then the package can be qualified for any given device technology. Both dielectric and resistive losses, as well as the losses due to impedance mismatch can be determined using this method.

TIME DOMAIN REFLECTOMETER MEASUREMENTS

The TDR method for measuring the amount of the transmitted signal that is reflected back from a load em-

plays a step generator and an oscilloscope in a "closed loop radar" system. The operation consists of generating a voltage step function along a transmission line that is to be studied. Both the incident and reflected waves are monitored on an oscilloscope at a particular point along the line. The voltage input step is not a true step but has a very short rise time (approximately 30 psec). This short pulse is generated by a tunnel diode having a source impedance of 50 Ω .

The TDR method is an effective technique for estimating the characteristic impedance of an unknown transmission line. It is also useful for analyzing line discontinuities and can reveal much about the position and type (capacitive, inductive, or resistive) of each discontinuity.

8. ELECTRICAL CHARACTERIZATION OF VLSI/VHSIC PACKAGING TECHNOLOGIES

Integrating VLSI/VHSIC devices into a high-performance electronic system requires careful attention to the electrical, thermal, mechanical, and environmental constraints at all levels of integration (package, substrate, and system). The electrical requirements may include some or all of the following characteristics: specific or controlled impedance interconnects (transmission lines), high propagation velocity, high circuit density, low crosstalk, power supply decoupling, and distributed power and ground planes. Thermal considerations are required to insure proper functioning of the electronic circuit as well as the integrity of both mechanical and electrical interconnections resulting from solid state diffusion and thermally induced stress. Mechanical considerations include TCE matching to reduce thermal stress related effects, selecting low-weight and high-strength materials with resistance to corrosion and fa-

tigue, and protection of devices and bonded lead wires. Environmental factors such as temperature and temperature range, humidity, vibration, radiation, and contamination may affect all of the aforementioned electrical, thermal and mechanical considerations when choosing an appropriate packaging scheme. Simply stated, the optimal integrated packaging scheme must possess the following characteristics:

1. Nearly lossless signal propagation without significant time delay,
2. High-density transmission line interconnects,
3. Noise free environment,
4. Thermal shunt from device to ambient,
5. Matched TCE at critical electrical and mechanical interconnections,
6. Hermetic device packaging,
7. Required mechanical support,

8. Lightweight assembly,
9. Reliability.

Unfortunately, a packaging scheme optimized for all of the above criteria is either nonexistent, currently unavailable, or prohibitively expensive. Practical electronic packaging represents an evaluation process that consists of finding compromises between such factors as high performance, cost, availability, and the amount of time that can be invested in a particular design (turn-around time). In many ground-based high speed electronic systems such as those found in high speed digital computers, size, weight, power consumption, and external cooling requirements are of little concern where computational speed is of primary interest. In applications where limited power availability, weight restrictions, external cooling limitations, and cost are of primary concern, operational speed requirements may have to be relaxed to accommodate system requirements.

The primary intention of this section is to introduce the most promising electronic packaging technologies for VLSI and VHSIC applications. Emphasis will be on directing the APL effort toward those packaging approaches that can accommodate the high speed, high-circuit-density requirements for future VLSI and VHSIC programs and to assist circuit designers in choosing viable packaging alternatives.

CHIP ATTACHMENT AND INTERCONNECTION—LEVEL 1 INTERCONNECTS

Chip mounting and interconnection requirements for VLSI and VHSIC applications are becoming critical as both the size of the devices and the number of I/O pads increase. In this section several of the popular chip mounting and interconnection techniques are discussed.

Die Attach

Separated integrated circuit dies may be attached to packages or substrates by four primary techniques: eutectic die bonding, soldering, epoxy (or other organic adhesive) attach, and glass bonding.

Eutectic die bonding uses a bimetallic alloy of gold-tin or aluminum-germanium in which the stoichiometric ratios of the constituent elements are selected to have a single melting point, i.e., the eutectic point of the binary alloy. For an alloy of 94 weight % gold and 6 weight % silicon, the eutectic temperature is 370°C. The source of gold in the alloy (assuming that one wants to attach a silicon die to a gold metallized package or substrate) can be the package plating on a metal pack-

age, the thick-film conductor ink on a ceramic package, gold metallization on the backside of the silicon die, or actual eutectic alloy preforms placed between the chip and the substrate. The eutectic is formed by heating the die and the package slightly above 370°C and then mechanically scrubbing the die into the underlying metal surface. This scrubbing action breaks down any thin oxide layers present as well as minimizing the formation of voids under the chip. Other common alloys for die attach include: gold-tin (80 weight % gold, with a melting temperature of 280°C), gold-tin (10 weight % gold, with a melting temperature of 217°C), and aluminum-germanium (45 weight % aluminum, with a melting temperature of 423°C).

Eutectic die attach forms a rigid bond between the die and the substrate because of the high modulus of elasticity of the eutectic alloys. This rigid bond can cause large thermal stresses in the silicon die when attached to high-TCE substrate materials. This problem is exacerbated when attaching the larger VLSI devices. The larger die size can also result in increased void formation caused by the difficulty of applying uniform pressure over the larger die area when scrubbing.

Solder attach refers to the use of soft-lead-based solder alloys (i.e., tin-lead system) for die attach. In this technique both the die and the substrate are pretinned with the solder compound. The components are then fluxed, placed together, and the solder reflowed. Following reflow the flux must be removed by a vigorous cleaning process. Sometimes an additional solder preform is used to provide a larger volume of solder than can be "loaded" on the die during the "tinning" operation. The tin-lead solders are those primarily used for die attach. Of these, the high-lead-content varieties are the most popular (e.g., 95 weight % lead) and have been investigated because of the relatively ductile nature of the die attach and have facilitated somewhat the attachment of large chips to some high-TCE materials.

The problems associated with the use of these solders include susceptibility to void formation (from trapped flux volatiles underneath the die), and crack formation resulting from thermal fatigue. For the case of the high-lead-content solders, crack propagation is assisted by the rapid formation of oxides within cracks already present after soldering. Oxidation of cracks, which occurs quite rapidly in the lead-rich phases of the solder, prevents partial rewelding during the compressive stages of the fatigue cycle. This oxidation has been observed in atmospheres of low-oxygen partial pressures. The voids present after soldering can also serve as crack nucleation sites for future crack propagation.

Adhesive die attach refers to the use of epoxy, or other organic adhesive resins such as polyimide, to attach

dies to packages and/or substrates. Unmodified, epoxies are dielectric in nature and therefore provide poor thermal conductivity and electrical insulation. Electrically conductive epoxies or polyimide adhesives can be formed by the addition of silver or gold particles to the organic matrix. Thermal conductivity may be improved by the addition of aluminum oxide (Al_2O_3) or beryllium oxide (BeO) to the organic matrix.

The problems typically associated with the use of organic adhesives for die attach include introduction of impurities into the sealed package, moisture absorbed by the adhesives and released into the package after sealing, and high thermal stresses resulting from the large differential thermal expansion between the adhesive and the die. Also, these commonly used adhesives are thermoset materials and thus, once cured, cannot be subsequently reflowed; this makes rework for chip and wire application impractical.

Adhesives that are thermoplastic (i.e., can be reflowed after solidification) and have relatively low melting temperatures are currently being considered for chip and wire applications. They will permit localized heating of the die, resulting in liquification of the thermoplastic material, thus facilitating die removal. A new die attach can be made by loading the previous die bond area, placing the new die in position, and reflowing the thermoplastic adhesive. This new adhesive technology may infuse new life into chip-on-board mounting schemes.

Glass bonding is the most recent die attach method and is used primarily for bonding silicon to low-TCE package and substrate materials such as ceramic and cermet. Glasses are dielectric in nature but can be loaded with silver to yield a conductive bond when required. The low TCE of the glass (6 to 8) is more compatible with both the silicon die and ceramic packages. This compatibility may assist in making the attachment of large dies more reliable.

Lead (Electrical) Interconnection

The three most common chip-to-package electrical interconnection schemes are wirebonding, tape bonding, and flip-chip or solder bumping techniques.

Wirebonding. Wirebonding is by far the most widely used method of interconnecting dies to package leads. It is performed on integrated circuits after a die has been separated from a wafer and attached to the package or substrate. The bonding pads are typically gold plated (or thick-film gold) in the areas where the package lead attach is to occur. Aluminum and aluminum-based alloys are used on integrated circuit dies. Aluminum is used because it is a good conductor, adheres well, and can form an ohmic contact with either heavily doped

n-type or p-type silicon. Aluminum also forms a Schottky barrier with lightly doped n-type silicon. Typically, 1% silicon is added to the aluminum to prevent voiding under bonding pads, and copper (less than 0.5%) is added, especially for VHSIC chips, to reduce electromigration effects brought about by scaling. As the scaling of integrated circuits continues, aluminum may have to be replaced with other contact systems with lower resistivity and resistance to corrosion and electromigration. These systems may be tri-level, using such materials as titanium, palladium, and gold.

There are two predominant wirebonding techniques used today, thermosonic and ultrasonic. Gold wire can be bonded by both techniques, while aluminum is bonded only ultrasonically. (A thermosonic technique for aluminum has been developed in research laboratories but has not achieved widespread commercial use).

Ultrasonic bonding is a low-temperature process where the source of energy to effect the bond is a transducer vibrating the bonding tip in the frequency range from 20 to 60 KHz. The tip of the wedge (bonding tool) vibrates parallel to the bonding pad interface at a temperature of 300 to 400°C. Ultrasonic bonds are usually formed with aluminum wire on aluminum or gold pads. The use of aluminum bonding wire is particularly useful when die temperatures exceed 85°C. Gold wire bonded to aluminum may result in the formation of undesirable gold-aluminum intermetallics at elevated temperatures.²⁴

Thermosonic bonding combines ultrasonic energy with the ball-bonding techniques of thermocompression bonding (pressure and heat). The combination of ultrasonic energy and heat eliminates the need for excessively high chip temperatures when wirebonding, as was required in the older thermocompression bonding method; the substrate temperature is usually held between 100 and 150°C while bonding. Ultrasonic energy is used to develop the high wirebonding pad-interface temperature necessary for a good weld. Since the die temperature is maintained at 150°C or less, the die may be attached with organic adhesives without fear of degradation. Also, there is less risk of significant intermetallic growth at these lower temperatures.

Both automatic thermosonic and ultrasonic wirebonders are in widespread use. Because of close spacings and high I/O densities of VLSI/VHSIC chips, automatic wirebonding is preferred. This process uses pattern recognition to locate the fiducial marks on both the chip and the package; then, once aligned, the programmed machine automatically bonds all of the I/Os at a rate of up to 10 bonds per second.

There are several problems associated with the use of wire-bonded interconnections with high density I/O

and high speed, integrated-circuit chips. The primary concern is the possibility of shorting between adjacent wires. This concern is highly warranted for the two-level or two-tiered package lead configuration. The problem can occur when fatigued wires droop and touch wires connected to the lower package leads. A secondary concern is the inability to control the impedance of wire leads. Impedance of wirebond leads are typically high ($> 150 \Omega$, high inductance, and low capacitance), and this value can change significantly depending on loop height and I/O density. For high speed gallium arsenide devices, the high inductance of round leads may significantly degrade circuit performance. The round leads also increase the amount of inductive and capacitive coupling between adjacent wirebonds.

Tape Bonding. Tape bonding is presently being considered as an alternative to wire bonding to achieve the reliability, electrical performance, and density that are not possible with the conventional automatic wirebonding techniques for chip-to-package interconnects. The tape-bonding process is also considerably faster than the automatic wirebonding process. Tape bonding is a "gang bonding" process in which all of the bonds are formed simultaneously. It involves the use of prefabricated metallic interconnection patterns (either single- or multilevel) on a carrier film. This film or tape material is typically polyimide, contains sprocket holes, and is wound around a reel much like a movie film so that the bonding can be performed automatically.

In order to be attached to these film-mounted lead frames, the semiconductor die must undergo an additional processing step that involves plating gold bumps over the bonding pads. If the integrated circuit has aluminum bonding pads, a gold diffusion barrier such as titanium or palladium must be used. This barrier seals off the exposed aluminum pad area, thus making these chips inherently more reliable. To form the bumps the barrier metal layers (plus a thin layer of gold to prevent oxidation) are deposited over the entire surface of the passivated wafer, usually by sputtering. The bumped pattern is then photolithographically etched using dry film resist, and the gold bumps are electroplated to a thickness of $25 \mu\text{m}$. The dry film is then removed and the conductive barrier layers are removed by means of selective etching techniques.

The outer lead bond connects the newly formed chip-film carrier-frame assembly with the package, hybrid substrate, or surface-mount wiring board. Again, the chip-film carrier assembly is positioned over the outer lead bonding sites, and a special outer lead thermode bonds the outer leads while excising the excess portion of the assembly from the tape carrier.

The tape is available in at least three varieties (single, double, and triple layer) and a host of widths ranging from 8 to 70 mm. Tape materials include polyimide, polyester polyethersulfane, and polyparabanic acid. Both two-layer and three-layer tape show the greatest potential for VLSI/VHSIC applications. High bonding densities can be achieved since these tapes can be constructed with 2-mil-wide fingers on 4-mil centers. The major limitation to the density of tape-bonded interconnects is the location of bonding pads. I/Os with densities up to 256 can be considered with multilayer perimeter tape bonding. However, area tape bonding will have to be used for I/Os with densities greater than 256, implying development of techniques for placing chip bonding pads not only around the periphery of the die but throughout the entire active area as well.

Electrically, tape leads are somewhat better than round leads because of the lower self- and mutual-inductance of flat leads and a lower skin resistance for very-high-frequency applications. This means lower crosstalk between adjacent leads. In addition, multilayer tape configurations can provide controlled $50\text{-}\Omega$ impedance stripline (three-layer metallized tape) or microstrip (two-layer metallized tape) transmission-line interconnects required for future VHSIC chips.

The problem with the use of such organics as polyimide is the moisture and other contaminants brought into the hermetically sealed package by these materials. Research is presently being conducted to reduce these potential problems. Some of this research includes the control of impurities of these organics, optimization of bakeout cycles, decomposition of enclosed organics, the determination of optimum sealing atmosphere, and the use of moisture-gettering materials inside hermetically sealed packages.

Another problem associated with use of tape bonding is the unavailability of a nondestructive evaluation for tape bonds. The polyimide film that mechanically supports the inner lead bonds and prevents shorting of leads to the adjacent leads and chip interconnection traces makes pull testing like that used on wirebonded chips impractical, if not impossible. Current research in this area involves the investigation of nondestructive techniques such as laser irradiation and reradiated IR wave analysis, and acoustic emission and laser scanning technology.

Solder Bumping (Flip Chip). In this attachment technique solder bumps are attached to the chip bonding pads and the substrate lead pattern. The die is then inverted over the substrate and the bond is performed by a "controlled bump collapse" reflow method. The process involves sequential evaporation of chromium, cop-

per, and gold through a metal mask on the aluminum bonding pads of the chip. The Cr/Cu/Au layer is then solder-plated typically with Sn5 solder (95 weight % Pb and 5 weight % Sn). Once the solder is deposited, the chip is heated to allow the solder to reflow into a hemispherical bump. The chip can then be inverted and aligned with the pretinned substrate pattern. After alignment the assembly is heated in an infrared oven or vapor-phase soldering system. The solder bump melts and gravity, coupled with surface tension, forms a near-truncated spherical soldered interconnect.

Solder bumping provides very short, low-resistance leads, which minimizes lead inductance. This is particularly useful for the high-frequency operation encountered in VHSIC chips. Solder bumping is also quite amenable to full area attach (i.e., bonding pads over the full active device area and not limited to the chip perimeter). The disadvantages in this process include solder joints under the chip that are not fully inspectable, poor heat removal since the only path is through the solder bumps, and the devices are difficult to repair if they fail. In addition, since the strain (on the solder joints as a result of TCE mismatch) is proportional to the lateral dimensions of the chip, this method may not be useful for interconnecting large VLSI devices.

DEVICE TO SUBSTRATE ATTACHMENT— LEVEL 2 INTERCONNECTS

Device Packaging

The use of discrete device packaging has become the predominant approach for interconnecting chips to the substrate or to circuit-level interconnects. The device package affords varying levels of protection for ICs and wirebonds from mishandling, contamination, and moisture, in addition to improving the repairability of faulty devices.

Presently, the two most popular methods for device-package-to-substrate interconnections are surface mount and through-hole mounting technologies. The primary surface-mount device package is the high-density, perimeter-style, chip-carrier package that consists of both a leadless and leaded variety, while the pin-grid array package is the high-density equivalent of the chip carrier for through-hole mounting.

In this section several high-density discrete device packaging alternatives will be examined for use in VLSI and VHSIC applications. Electrical package characteristics, thermal package resistance, and overall package reliability will be discussed for both surface and through-hole mounting technologies.

Surface-Mounted Technology/Through-Hole Mounted High-Density Packaging

There are two basic techniques for attaching packaged chips to circuit boards, through-hole mounting and surface mounting. In through-hole mounting, packages with bottom leads such as pin grid arrays are soldered into plated through-holes in multilayered printed wiring boards. These holes are typically placed on 100-mil centers (100-mil grid) and, in addition to holding the component lead, serve as vias for interconnections between the circuit board layers. Through-hole mounting is still the predominant form of electronic packaging, especially for consumer electronic applications.

This type of mounting has several disadvantages for VLSI and VHSIC applications, including reduced circuit board density (due to the through-hole via structure), difficulty of repair (removing package leads can damage through-hole structures, especially as I/O numbers increase), increased inductance due to long round wire leads, and radiation loss from unterminated stubs. The repair and removal of this type of package can be facilitated by use of a socket that is permanently mounted into the board. The package can then be easily plugged into and out of the socket. Sockets, however, add additional line inductance, capacitance, and resistance to the circuit path, which can slow down device operation as well as adding additional weight to the overall assembly. Mechanical integrity would also be questionable for high-reliability applications.

Surface mounting of leadless, beam-leaded, or "J"-leaded components to various circuit board materials is the dominant new thrust in modern device packaging. In this technique leadless or leaded packages are soldered to the surface of the host circuit board. No through-hole mounting is required. Vias can be made without through-hole drilling and plating; only the necessary levels or layers are involved. Thus, the density of circuit boards can be increased, with shorter leads and possessing higher (faster) electrical performance characteristics. Repair is easier because most joints are accessible and not locked into high-aspect-ratio holes. Surface-mounted packages such as the small-outline integrated-circuit package (SOIC) and the leadless chip-carrier package (LCC) have electrical performance characteristics that are far superior to their leaded through-hole-mounted counterparts. In addition, surface-mountable chip capacitors have approximately 1 to 2 nH of inductance as compared with 10 nH for the through-hole versions. Low-inductance chip capacitors will provide better decoupling, resulting in lower noise on power and ground returns. Chip capacitors can also supply currents faster than leaded ones. Since switching currents can be supplied to the device

more rapidly, device output rise and fall times are crisper, resulting in decreased delay times.

Physical Packaging Structures

The decision as to which physical packaging type will eventually house the integrated circuit(s) must be made very early in the integrated circuit design process. Packaging and assembly operations must be considered as fundamental as the design of the device that is to be packaged within. Such factors as use environment, reliability, cost, hermeticity, electrical performance (speed), device power dissipation, and the number of I/Os must all be considered before a device packaging structure can be selected. Today's sophisticated electronic systems require modern packaging schemes that (a) provide improved performance while still maintaining acceptable costs, (b) operate faster so that the subnanosecond performance (rise times) of modern silicon and gallium arsenide technologies can be realized, (c) provide the thermal and mechanical management made necessary by scaling, and (d) accommodate hundreds of I/O ports.

Dual-In-Line Package. The dual-in-line package (DIP) has been the standard integrated circuit packaging method for many years with, at times, over 90% of all integrated circuits manufactured being shipped in DIPs. Dual in-lines have been manufactured from various materials, including plastic, glass-ceramic, and ceramic (Al_2O_3).

Since DIPs have many desirable features, there has been a great reluctance by the packaging industry to move away from the DIP as a major packaging technique. However, the DIP cannot support the performance demands of state-of-the-art VLSI/VHSIC integrated circuit technologies. The major shortcomings are I/O densities, speed, electrical performance, and the relatively large real estate required for board mounting.

Both speed and electrical performance are hampered by the length of the longest DIP leads. They possess significant inductance, which can result in switching delays with voltage spiking on power and ground leads. Also, the differing lengths of package leads for bus structures can limit toggle frequencies. In many DIPs the longest leads in the package are reserved for the power and ground connections. Chip carriers (discussed below), on the other hand, use the shortest leads for these connections. This is an optimal situation for devices with large switching currents. The speed is affected by the long lead length and the slow propagation velocity in the cofired ceramic medium.

Electrical performance can be improved somewhat by integrating a ground layer into the multilayer pack-

age structure. This layer, if placed judiciously (beneath the power supply bus), can reduce the inductance in power leads, thereby reducing the switching time and eliminating switching transients. It has been suggested that I/O density can be improved by placing a second row of leads underneath the package, along the edge of both package sides. Here, the thought is to preserve the present in-line structure in order to facilitate placement of a heat sink between the four rows of package pins. This is not possible with four-sided perimeter packages. Although these changes could have some impact on moderate speed, medium-I/O-density applications, the DIP package structure falls far short of that required for future VLSI/VHSIC applications. For this reason, the chip carrier package and the pin-grid-array package are needed to satisfy at least the immediate requirements of VLSI/VHSIC circuitry.

Chip Carrier Package. The chip carrier is presently the predominant package for surface-mounting IC devices. It has found great favor in high-density surface mount applications for a number of compelling reasons. It can accommodate more than twice the number of I/Os per unit area than can the dual in-line package. The shorter package lead length per I/O is particularly useful in reducing lead inductance and capacitance, thereby enhancing electrical performance for high speed devices. Ceramic chip carriers made from either alumina or berylia can offer good thermal conductivity. Enhanced thermal conductivity can be achieved by using a thermal grid pattern directly beneath the die bond cavity for direct bonding to the underlying substrate. And because of the perimeter-style leads, these packages can be easily removed and replaced without significant damage to the underlying substrate.

The ceramic chip carrier package is available in either a leadless or leaded type. The I/O pitch for the leadless type is typically 40 or 50 mils. Custom chip carriers can be purchased commercially with pin spacings as low as 20 mils for the leadless variety and 25 mils for the leaded type. These packages use less space than does a pin-grid-array package with a conventional 100-mil pitch.

The primary advantages associated with use of leadless chip carriers over leaded ones are the lower component and production cost, low lead inductance and capacitance, and the ease of handling and testing. The primary problem with the leadless package is the different coefficients of thermal expansion of the ceramic carrier and the glass epoxy laminates. A controlled thermal-expansion substrate must be used to minimize the effect of thermally induced strain on the fatigue life of the solder joint.

The advantage in using leaded packages is the ability to mount ceramic packages to standard printed circuit boards; special circuit boards, however, are usually more expensive and may require special processing techniques. The primary problem associated with the use of the leaded package is the possibility of damage to leads while handling and testing. Also, increases in inductance and capacitance for these package types may be incompatible with very high speed applications. The "J" lead configuration is the most desirable lead style since the lead is tucked underneath the package and therefore uses no additional real estate, while affording some protection to the lead.

Presently, the level of reliability of soldered leads and the cost of processing and production have limited the practical number of package leads to less than 156 I/Os. This level of density may currently be sufficient for most applications owing to the present limitations in substrate wiring densities, but as new substrate technologies emerge to increase circuit wiring densities, further development in chip-carrier packages will be required.

Pin Grid Array Package. Pin-grid-array packages are similar to ceramic chip carriers in construction except that the I/Os are obtained through pins that cover the bottom exterior surface in a grid or array fashion. A typical pin-grid array is a square, cofired-ceramic package with an array of pins on 100-mil centers (50-mil centered pin configurations are currently being developed for I/Os exceeding 300) for through-hole mounting. The die cavity can be either on the opposite side of the pins (cavity up), allowing a full base array of pins, or on the same side as the pins (cavity down), requiring a concentric perimeter array of pins. The cavity-down configuration is preferred when the primary heat transfer mechanism is forced convective cooling. The standard high-density PGA contains up to 148 active pins arranged in a matrix about the package perimeter. Increasing pin density to include the center and corner portions of the package, in addition to reducing pin spacing, will require significant improvements in fine-line through-hole substrate technologies to permit routing of these lines between plated through-holes.

Low-pin-density PGAs can be soldered by conventional through-hole soldering methods (wave soldering, etc.). To replace the device, a hot spot air removal gun or other suitable technique must be employed. Care must be exercised to prevent damage to the substrate around the perimeter of the package as well as to the plated through-hole. As I/O density increases, the pin-grid-array removal problem becomes increasingly difficult, and a socket or connector becomes highly desirable. The chief advantage to the PGA package is that

it provides through-hole circuit board technologies with a suitable package having high I/O capabilities.

The pin-grid-array package should provide adequate electrical performance for most high speed applications. For very high speed applications involving the use of high performance silicon or gallium arsenide devices (with gate delays around 75 psec and clock rates as high as 4 GHz), pin-grid-array packages are not considered to be a viable alternative because of their inherently large lead inductance. In fact, packaging GaAs devices in PGAs or DIPs is not recommended due to the unterminated stubs created by the package pins.

Thermal management of the pin-grid-array package is difficult when forced convective cooling is not available. The standard through-hole circuit board (such as epoxy-glass, polyimide, etc.) is typically a poor thermal conductor. Thermal vias can be attached to the bottom portion of the package in a manner similar to that for the leadless chip carrier package. Thermal vias through the circuit board can significantly reduce the space required for routing signals already limited by large through-hole vias.

Pad Grid Array Package. The pad-grid-array package is the surface mountable counterpart of the pin-grid-array package. The pad-grid array has an area pad array of solderable bonding pads for electrical connection to the underlying substrate. This array features increased interconnection density over the more conventional perimeter-style leadless chip carrier package. Heat dissipation is improved for this style of package because of the increased number of solder pads and the availability of solder pads directly underneath the die cavity.

The primary reason for the limited use of the pad-grid array is the difficulty of inspecting solder joints underneath the package and not visible to the naked eye. Introduction of new inspection techniques involving laser acoustic microscopy and thermography (methods being investigated for the inspection of TAB bonds) may ultimately provide a method for evaluating solder attachment.

One pad-grid-array package that has achieved some moderate success is the open via chip carrier (OVCC)²⁵ that is currently being used by one VHSIC contractor. The OVCC package has solderable through-holes in the chip-carrier package itself, which extend down to the underlying bottom pads. A solder preform is attached to the bottom pad (which has a through-hole in the middle of the pad), and when the solder is reflowed, the joint can be visually examined by the through-hole channel, which will fill with solder upon reflow. Therefore, the main purpose of the open via, is to provide a method

for determining whether or not the solder preform has reflowed.

Direct Chip Mounting

Direct chip mounting by the inverted bumping technique is becoming increasingly popular. In this method a reflow alloy is placed on the chip bonding pads, and the chip is turned face down (inverted) and reflowed to an underlying substrate. This method can be used to replace wire bonds or TAB in chip-on-board mounting configurations. When used in this configuration, multiple chips can be placed on both sides of a very dense multilayer board structure, achieving densities equal to or greater than wafer scale integration, while retaining repairability and optimum configuration. One or more organic overcoats may be necessary to protect the bare die and board structures from environmental stresses.

Hybrid Packaging

Packaging chips individually requires more real estate than direct chip mounting. Denser packaging can be achieved by the use of a hybrid structure, as shown

in Fig. 23. In the hybrid, unencased, integrated circuit, dies are mounted (via eutectic, solder, epoxy, etc.) to host substrates. The substrate can be single- or multilayer. Interconnection of chips to the substrate is accomplished by either wire bonds or prepatterned, tape-mounted lead frames (TAB). The substrate is then placed in and interconnected to a large package structure by means of wire bonds or TAB. Once tested, the hybrid package is sealed, usually by welding.

Hybrids are complex, dense entities that are more difficult to repair than surface-mount assemblies. Once sealed, individual dies become inaccessible for further reworking, and failure of the hybrid may require replacement with another hybrid circuit. Also because a hybrid involves multiple high-density integrated circuits, it is much more difficult to test and determine the cause of failure if a circuit should not work. Care must be exercised in the design of VLSI/VHSIC hybrids to build in testability and self-diagnostics. Since hybrids are much denser forms of interconnections, thermal loading and heat dissipation are also of major concern.

The multichip module or hybrid is rapidly becoming a major portion of the VLSI/VHSIC packaging ef-

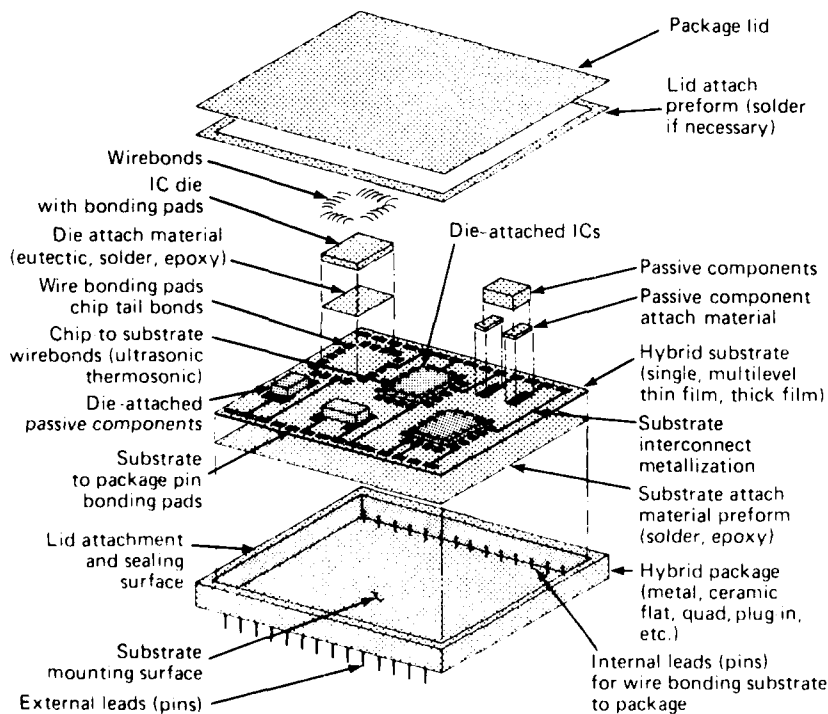


Figure 23 The anatomy of a chip-and-wire hermetic hybrid.

fort. The multichip module concept is simply a high-density version of the hybrid and is thus a subset of the hybrid packaging concept. It contains the necessary elements of a partitioned portion of a circuit to achieve high signal-line densities within the module while producing a reasonable number of module I/Os for interfacing with the host through-hole or surface-mount substrate. Special multichip modules can be mass produced for such specific processing applications as memory storage, digital signal processing, and computer processing.

PACKAGE-TO-PACKAGE INTERCONNECTIONS—LEVEL 3 INTERCONNECTS

Printed Wiring Boards

Epoxy-glass and Polyimide Laminates. The multilayer printed wiring board consists of four to eight conductor levels appropriately spaced between conductor (ground or power) planes. Vias to internal conductor layers are plated through-holes. Device packages may be either through-hole mountable or surface mountable. Large, ceramic, surface-mount components have compliant leads due to the large difference in TCE between ceramic and organic composite substrates. These organic insulator materials consist of glass-epoxy or polyimide laminate, and the conductor material is copper.

These organic laminate materials are generally poor thermal conductors and thus, without modification, they are inadequate for applications involving high power-dissipation densities where conduction through the circuit board is the primary method of heat removal. One popular method for improving the thermal conductivity of the substrate is achieved by bonding a metal heat sink to the component side of the substrate; the components themselves are bonded to the heat sink, and the leads are brought through holes machined into the heat sink and electrically connected to the substrate in the typical through-hole manner. This method is suitable for the dual-in-line configuration but is not conducive to mounting high-density perimeter and area-style packages such as the PGA package or the Quad package. An alternative is to use a metal core material bonded to and sandwiched between the organic laminates. These metal-core circuit boards, however, are more expensive to build than conventional, printed-circuit-board materials.

In applications calling for leadless ceramic chip carriers, ground planes are sometimes replaced with low-

TCE copper-invar-copper foil to provide a lower differential coefficient of expansion between components and substrate while at the same time improving the thermal conductivity of the circuit board. The copper is usually treated with a red or black oxide treatment prior to lamination to improve adhesion. Copper clad molybdenum is an alternate material being considered as a low-TCE metal core material for PWB applications. Copper clad molybdenum has a thermal conductivity that approaches that of alumina; however, it is also quite expensive and is recommended only when heat sinking is critical.

Fluorocarbon MPWB Laminates. Several alternative laminates that offer a low loss and low dielectric constant (with $\epsilon_r < 2.5$) for use in multilayer printed circuit boards are being investigated. These lower-K dielectric materials are essential for implementing subnanosecond device technologies. These fluorocarbon substrates may consist of either polypropylene, polyethylene, polybutadiene, PTFE (polytetrafluoroethylene), or FEP (fluorinated ethylene propylene). Of these, the lowest dielectric constant was obtained with PTFE, which has no dipole moment because of its symmetrical molecular shape.

The most popular PTFE material is DuPont Teflon. In most cases, Teflon is reinforced with glass although alternate reinforcing fibers such as Kevlar and quartz are currently being investigated. The dielectric constant is approximately 2.2 for Teflon at 10 GHz.

The chief disadvantage with Teflon is that it is highly unreactive; therefore, it becomes difficult to get materials to stick to it, and it is also difficult to process. Teflon is difficult to drill, and the resin tends to smear, creating problems in the electroless plating process that are not observed in other resin systems. Moreover, for applications where the circuit board may experience some external loading, Teflon may not possess the required flexural strength.

Another PTFE composite currently being investigated by the Rogers Corporation involves the use of a random glass-fiber-reinforced composite. The composite board material has a low dielectric constant (≈ 2.8) and a dissipation factor of 0.002 at 10 GHz. This translates into a 24% reduction in propagation delay over conventional epoxy-glass substrates. This composite has a z-component thermal coefficient of expansion of 24, which closely resembles that of copper and makes it suitable for through-hole applications. Using a proprietary process, Rogers is presently claiming the capability for making copper traces and spaces as small as 0.001 in., with tolerances of about ± 0.0001 in. This process yields a typical trace thickness of about 0.0005 in. with very

straight side walls. This well defined geometry is essential for use at microwave frequencies.

These fluorocarbon substrate materials are good thermal insulators and thus will require additional heat sinking for use in applications involving large power dissipation densities.

Kevlar (Aramid Fibers) Reinforced Laminates. Kevlar is an aramid fiber material developed by DuPont and having a low thermal coefficient of expansion. This fiber is quite strong and is used as a reinforcement fiber to lower the overall TCE of conventional printed wiring-board resins. Besides offering a TCE match to ceramic, Kevlar-reinforced laminates are as much as 25% lighter than epoxy glass substrates. The Kevlar fibers are extremely strong, and plasma etching is required after through-hole drilling to eliminate frayed fibers from interfering with the plating process. There are several reinforcement fibers available for controlling the TCE in printed circuit boards, but Kevlar is the most popular and the only one readily available in quantity.

Kevlar-reinforced polyimide has a dielectric constant in the range of 3.5 to 4.0. This system has a very low thermal coefficient of expansion in the x-y direction, somewhere between 3.4 and 6.7 in contrast to polyimide glass that is between 11 and 14. In the z-direction, however, polyimide Kevlar can be as high as 80, which is significantly higher than the polyimide glass. It also has a tendency to absorb large amounts of water (up to 4%). This particular Kevlar reinforced laminate may be unsuitable for through-hole mounting applications.

Westinghouse has considered several resin systems, primarily epoxy and polyimide reinforced with Kevlar fibers.²⁶ It has been their experience that Kevlar reinforcement tends to introduce cracking in some of the more brittle resins when thermally cycled. Furthermore, Kevlar-reinforced laminates are more expensive to produce, costing from about three times (for epoxy Kevlar) to eight times (for polyimide Kevlar) that epoxy-glass laminates, or from a half to greater than the cost for multilayer cofired ceramic.

A modified polyimide Kevlar laminate has been developed that is somewhat less brittle than the polyimide and less prone to absorb water (2%). The modification process involves introducing controlled amounts of epoxy resins into the precured polyimide mixture.

Ceramic Circuit Board Technologies

Ceramic materials such as alumina and berylia have long been considered desirable candidates for circuit boards because of their relatively high thermal conductivities, excellent mechanical strength, and compatibility with the surface-mountable ceramic packages. On

the negative side, the dielectric constant is considered too high for high speed applications. Recent advances in the application of ceramic in conjunction with the use of low-dielectric insulator materials (such as polyimide) are once again bringing ceramic technology into the era of high speed packaging.

High-Temperature Cofired Multilayer Ceramic. Multilayer, cofired, metallized-ceramic technology involves metallization of green (unfired) ceramic sheets, punching and filling vias into the green ceramic tape sheets, subsequent lamination of multiple metallized sheets (heat and pressure are used to thermoplastically bond metallized sheets together), and subsequently firing them into a multilayer circuit or package configuration. The refractory metallization material is tungsten (to withstand the high firing temperatures required for conventional ceramic materials), and the external package or substrate leads are plated with nickel and then flash-plated with gold to permit the brazing of numerous types of leads, studs, pins, braze rings, and heat sinks.

Some of the advantages of multilayer cofired ceramic include the following: Although the nominal dielectric constant for alumina is 9.0 to 10.0, the thickness of the insulating sheets may permit the fabrication of 50- Ω shielded striplines not achievable in conventional multilayer thick-film circuits. The thermal conductivity of ceramic is quite good. High circuit densities are achievable for use in VLSI and VHSIC applications. The monolithic unit is strong, hermetic, and dimensionally stable. Some of the disadvantages include relatively slow propagation velocity, high resistivity of the tungsten metallization, high tooling costs, and limitations in overall size as a result of shrinkage during firing.

Low-Temperature Cofired Multilayer Ceramic. Recent developments in low-temperature cofired ceramic tape products will now permit the use of lower-resistivity, conventional, thick-film conductor materials in place of tungsten. Conventional thick-film furnaces can be used in the firing process because of the low temperature needed to fire multiple green sheets of these new ceramic materials. The thermal conductivity is lower than that of conventional cofired tape; however, the dielectric constant is also significantly reduced, enhancing electrical performance. Tooling costs will remain high if standard methods of green-tape punching are required.

Currently, APL is investigating the effects of laser-drilling vias in green ceramic tape. Preliminary studies have indicated that via drilling with a CO₂ laser may be a quick, inexpensive method for producing the hundreds of vias required in dense multilevel circuits.

The advantages to the low-temperature cofirable ceramic include: (a) screen-printable low-resistivity conductors; (b) lower dielectric constant than thick-film dielectrics currently available; (c) no warpage problems resulting from TCE mismatch between ceramic and ink dielectrics; (d) thicker insulation layers that permit fabrication of controlled higher-impedance signal lines (fabrication of 25- to 45- Ω striplines); and (e) a larger number of signal layers. The penalties incurred when switching from high-temperature to low-temperature ceramic include reduced strength and thermal conductivity. These factors, however, are more than compensated for by the advantages of the system.

Thick-Film Multilayer Ceramic. Thick-film multilayer technology is relatively mature and is used primarily in the fabrication of hybrid microcircuits. It involves the alternate printing and firing (at temperature near 850°C) of thick-film conductors, vias, and dielectric layers to form a layered interconnection system. More recently, thick-film on ceramic has been used in fabricating large-area circuit board assemblies because of the recent popularity of leadless ceramic chip carriers and surface mounting. Advantages include: TCE match for hermetic chip carrier packages and ceramic chip components such as capacitors and resistors; excellent thermal conductivity for alumina; and utilization of existing hybrid capability for the manufacture of large-area circuit boards.

The primary disadvantage of multilayer thick-film circuits is the nominally high dielectric constant for thick-film insulating materials. This, combined with the difficulty in reliably printing fine conductor traces (width < 5 mils), makes the fabrication of controlled-impedance, high-impedance transmission lines difficult. The maximum unterminated length is at least half that for conventional printed wiring board traces and less than one fourth of that for fluorocarbon laminates.

Another disadvantage with the use of large ceramic substrates is the brittle nature of ceramic. Large substrates will usually require attachment to a back plate or frame for the purpose of mounting to card edge retainers. Also, warpage places restrictions on the number of dielectric layers available for both high-density and high-impedance circuits. Excessive dielectric thickness may predispose the substrate to cracking during subsequent firings or during later stages of assembly.

The perceived use of this technology for high speed-high density applications is in the hybrid multichip circuit. The two factors that will determine the impact of this technology on VLSI and VHSIC programs include the ability to fabricate fine conductor lines (2 to 5 mils), and the development of lower-K thick-film dielectrics.

Dielectric constants in the range of 4 or less and a capability to fabricate lines of 3 mils or less, will be necessary to insure the future of thick-film technology for high speed applications.

Polyimide Thin-Film on Ceramic. A polyimide thin-film circuit consists of multiple layers of thin-film copper-conductor patterns separated by polyimide dielectric layers and fabricated on a ceramic substrate. Polyimide is a good candidate for an interlayer dielectric because of its good dielectric properties, excellent thermal stability, and chemical resistance. The low dielectric constant and the ability to easily pattern 1-mil lines permits fabrication of dense 50- Ω transmission-line structures.

The polyimide thin-film circuit consists of a base conductor level wet-etched from a metallized ceramic substrate; The metallization layer consists of chrome-copper. The insulating layers are formed by depositing a thin layer of polyamic acid, either by spinning or spraying it onto the surface. If the polyimide is a negative-type photosensitive polyimide, vias can be formed by exposing the surface to light while masking those areas to be developed (vias). If the polymer is not photosensitive, the polyimide must first be cured and then coated with a resist material (except where the vias are to reside, typically a thin coating of SiO_2) and then plasma etched in an O_2/CF_4 plasma. After the vias are cleared, the next metal layer (copper for intermediate layers and gold for surface layers) is added, usually by sputtering. The sputtered thickness can be increased through an additional plating step.

Presently, the thin-film polyimide has been limited to hybrid applications only, which are presently being designed specifically for devices using chip-and-wire, flip-chip or TAB bonding. The size of these circuits is limited somewhat by the loss of adhesion, which occurs on larger substrates because of the propensity for polyimides to absorb water (which reduces adhesion) and the large differential thermal expansion between polyimide and alumina. Chips can be mounted directly onto the ceramic or onto plated thermal via structures for enhanced heat sinking. The nominal 1-mil lines and 5-mil spaces offer the necessary circuit density requirements for most VLSI and VHSIC devices currently available. The most immediate applications for this relatively new technology will be in the areas of VLSI memory arrays and processors.

Discrete Wiring Technology

Most available discrete wiring technologies use plated through-hole technology with discrete wiring for device interconnection. The discrete wiring consists of 34 or 38 AWG insulated copper wiring that can be locat-

ed either on the bottom portion of the substrate (Unilayer II) or between laminated layers of printed circuit board materials (Multiwire). Ground and power busses or planes are generally located on the top and/or bottom portions of the substrate or between laminated layers for multilayered configurations. Discrete wiring technologies can easily accommodate the wiring densities required for dual-in-line packages on two orthogonal circuit layers. Chip carriers and pin-grid-array packages (PGA) will require three to four circuit layers since these packages have almost twice the pin density of DIPs.

For the standard two-layer wiring, the characteristic impedance is approximately the same for each layer. The characteristic impedance is represented by the equation for a line over a ground plane,

$$Z_0 = \frac{60}{\sqrt{\epsilon_r}} \cosh^{-1}(h/r), \quad (113)$$

where ϵ_r is the effective dielectric constant (combination of the dielectric constant of the wire insulation and surrounding dielectric material), h is the height of the wire above the ground plane, and r is the radius of the wire.

For Unilayer II configurations the line impedance can be tailored by adjusting the height above the ground plane. The characteristic impedance, however, must be adjusted to account for the crossover capacitance inherent in multilayer circuit wiring. If a third or fourth level of wiring is required, the impedance for wire on this level will increase as a result of increased separation from the ground plane. The Multiwire configuration more closely resembles the multilayer printed wiring board concept; that is, wires sandwiched between laminated layers of epoxy glass. This permits the incorporation of solid ground planes between alternating wire layers.

Using discrete wire instead of an etched or printed conductor has the advantage that the impedance is easier to control because of its uniform geometry. Stripline and microstrip line configurations suffer from the tight dimensional tolerances on artwork and the changes in line geometry due to poor manufacturing control. The advantage in using a round wire is that the crossover capacitance is significantly lower than for flat wires. The disadvantage, of course, is that round wires have a somewhat higher self-inductance, and the coupling between parallel wires is significantly higher. This coupling can have a significant impact on parallel conductor crosstalk and thus will affect wiring density.

For the higher speed and higher density applications, crosstalk can become significant. To address this criti-

cal issue, Multiwire has developed a miniature coaxial cable using Gortex as the dielectric material ($\epsilon_r \approx 1.3$). The propagation speed for this cable is almost three times faster than cofired ceramic and twice as fast as polyimide. There are a number of additional advantages with using miniature coax wiring. These include the following: virtual elimination of crosstalk and noise pickup; elimination of sharp bends and corners usually found in etched circuit board traces; 50- Ω impedances compatible with VHSIC devices; and elimination of crossover capacitance, permitting higher wiring densities and shortest-distance wiring ("rats nesting"). Frequency limitations are present, however and depend on the thickness of the outer coaxial conductor (skin effects can increase ground resistance losses and permit the transmission of noise from nearby conductors). The plating thickness currently used in Multiwire coaxial conductors is 0.4 mil.

Wire connection and vias are made in either of two ways. In the first method (Unilayer II) the wire can be soldered to a prefabricated, plated, through-hole grid pattern. The second method (Multiwire) involves the following steps: routing the wires; coating them with an adhesive material and curing this material; drilling holes at the intersections of wires and in places where through-holes are required; and finally plating the through-holes.

Enhanced heat conduction can be achieved by laminating such metal core materials as copper-clad invar to the substrate. These metal core materials can be used for power and ground distribution. Low-TCE metal core materials can also be used to reduce the TCE for use with leadless ceramic chip carriers.

Wafer-Scale Integration

Currently, there are many misconceptions about wafer-scale integration and the role that it might play in the interconnection and packaging of VLSI and VHSIC devices. The basic building blocks of wafer scale integration schemes are PLAs, ALUs, registers, multipliers, and controllers. Early concepts involving wafer scale integration were monolithic in nature; that is, all of the interconnected devices would reside on the same wafer. Interconnection of good devices (e.g., array processors) was performed by wirebonding the adjacent good devices or by depositing and then patterning thin metal conductors and dielectric crossovers. Since both of these schemes require that functional dies be arranged in clusters so that they can be wirebonded or patterned with a single piece of artwork, yields would be low and costs typically high; furthermore, both of these factors would increase as the number of dies used in this scheme increased. Other problems include the

following: testing of such complex structures would be more complex than for VLSI chips; there would be a need for switches to disconnect faulty parts of the wafer and to connect spares; and practical methods for packaging large wafers and conducting vast amounts of heat would have to be found.

Although development of monolithic wafer-scale integration is moving slowly, subsequent variations on the theme have been introduced, all claiming wafer-scale integration. All of these hybrid approaches seek to take advantage of the fine-line photolithography technique that has permitted the complexity found in today's VLSI device technologies. One such approach²⁸ involves the process of selective etching to open areas in the silicon where chips can be placed. The die surface is then TAB or wirebonded to the host silicon substrate.

Although the concept sounds enticing at first, some sobering realizations immediately surface. Some of the apparent problems include the following: the area around and beneath the chip is unavailable for routing interconnections; multilayering is limited to two layers when using conventional aluminum metal conductors; controlling impedance with conventional transmission-line structures is not available in two-layer structures; and attachment to hermetic packaging materials such as Kovar and ceramic for large wafer substrates with a linear dimension exceeding 1 in. will be difficult. Essentially, this concept is identical to that for the thin-film hybrid multichip module. However, silicon's poor thermal conductivity makes it a somewhat poor substitute for a host substrate when compared with sapphire, alumina, aluminum nitride, porcelain-steel, copper-clad invar, or copper-clad molybdenum, all of which are suitable alternatives.

ESTIMATING CIRCUIT DENSITY BY RENT'S RULE

Limited success in determining wiring density for logic circuit applications has been achieved by some authors^{29,30} through the use of the empirical relationship commonly known as Rent's Rule. The relationship has been used primarily for device interconnections but can be applied with some success for device packages. Approximating the wiring density before committing to a particular substrate wiring technology can prevent costly redesigns and systems that must be operated at lower speeds as a consequence of coupled noise. Some approximate methods for determining circuit pack parameters will be discussed.

When deciding whether a wiring technology is sufficient to support a particular design, the following must

be considered: (a) determination of the maximum number of vertical and horizontal signal lines crossing any respective imaginary horizontal or vertical line drawn across the circuit pack; (b) the position of these lines where the crossings are most numerous or, equivalently, the density is greatest; (c) determination of the maximum lead length; (d) based on this length, a determination of design rules for parallel-lead spacing as a function of available manufacturing processes, capacitive loading, and noise parameters; and (e) reduction in wiring density due to vias such as plated through-holes in PWB and staggered vias in multilayered thick-film circuits. The first three considerations depend primarily on the circuit design and the partitioning of the circuit into discrete chips. Rent's rule can be particularly useful for approximating these parameters. The last two considerations depend on the substrate wiring technology itself and can be used to weigh the merits of the technology against the density requirements for the design.

Rent's Rule for multichip packaging states that the number of active leads, P , on a circuit pack (circuit board, hybrid package, etc.) containing g gates can be expressed by the empirical relationship

$$P = ag^b, \quad (114)$$

where a is the average number of connections per gate and b is the Rent's exponent, an experimental constant to be determined. This expression can be reformulated in terms of the ratio of package leads to chip I/Os. The total number of gates on a multichip circuit card or module containing an arbitrary number of ICs can be found approximately through the relation

$$G = \sum_{i=1}^m N_i g_i = \sum_{i=1}^m N_i (P_i/a), \quad (115)$$

where N_i is the number of type i components and m is the number of different devices. The total package lead count P_i for the multichip module can be expressed using the following relationship:

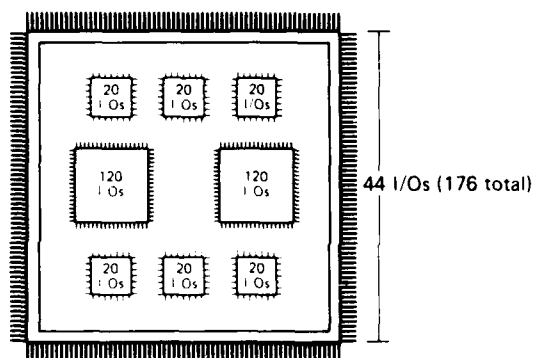
$$P_i = aG^b = \left(\sum_{i=1}^m N_i (P_i)^{1/b} \right)^b. \quad (116)$$

In actual circuit applications the number of package I/Os and the number of active pins for each device are known but the constant b is unknown. The Rent's exponent can be determined through the iterative relation

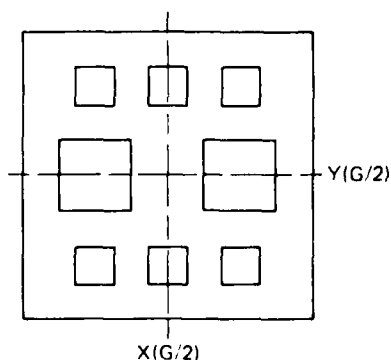
$$1/b = \log \left(\sum_{i=1}^m N_i (P_i)^{1/b} \right) / \log (P_b) . \quad (117)$$

This relationship will converge as long as the total number of package pins, P_t , is greater than the number of active pins on any one device or discrete package.

The application of Rent's Rule is particularly useful in determining the required circuit density and optimal device placement for a particular circuit design. In the following example we extend the model described by Schmidt³⁰ to estimate the maximum lead density for circuit cards with I/Os on all four sides. Consider the circuit layout in Fig. 24. The number associated with each device corresponds to the number of active I/Os. The chip set includes two devices with 120 active pins and six 20-pin devices. The total number of package



(a) Multichip hybrid module with 360 internal I/Os and 176 external I/Os.



(b) Imaginary lines $X(G/2)$ and $Y(G/2)$. Half the total number of gates lie on either side of these imaginary lines.

Figure 24 Multichip hybrid module (a) and coordinates $X(G/2)$ and $Y(G/2)$ (b) useful in estimating the maximum number of leads crossing any horizontal or vertical line drawn across the substrate.

I/Os is 176 (44 pins on each of four sides) yielding a Rent's exponent of approximately 0.5.

In this example we would like to evaluate the maximum number of signal lines crossing any horizontal (or vertical) line drawn across the circuit card for this particular device placement. We make the assumption that the maximum number of vertically (or horizontally) travelling lines will occur at the coordinate point at which there are $G/2$ gates above and below. The horizontal and vertical coordinates will be referred to as $Y(G/2)$ and $X(G/2)$, respectively. This results in the following relation for the maximum number of leads crossing any horizontal line:

$$P_h = a \left(\frac{1}{2} G \right)^b = \left(\frac{1}{2} \right)^b P_t . \quad (118)$$

Also, since we can assume that the number of leads leading to package I/O pins located beneath (or above) this line will not affect the wire congestion in the vertical direction, we must reduce the number of leads by a factor of $(1 - P'_t/W)$, where W is the total number of substrate leads and P'_t is the number of package leads available to the $G/2$ gates accessible without crossing over the imaginary line. Thus, the maximum number of vertically going leads can be given by the following relationship:

$$P_h = \left(\frac{1}{2} \right)^b P_t (1 - P'_t/W) \quad (119)$$

In our example, assuming an average of 1.25 segments per device pin, for a total of 450 substrate leads, and a Rent's exponent of 0.5, the maximum number of leads crossing the line in Fig. 24 can be estimated to be approximately 100.

It should be noted that in this case, because of the symmetry of the package I/Os, the maximum number of leads crossing any vertical line should be approximately equal to that for any horizontal line. Also, because of symmetrical placement of the devices, the results are the same regardless of which side of the imaginary line we focus on. If the devices were distributed as in Fig. 25, then the maximum number of leads would depend on which side of the line, $X(G/2)$ or $Y(G/2)$, you were considering; i.e., the term P'_t in the correction factor would differ depending on the gate and package lead distribution. Obviously, the $G/2$ gates will require, on average, one half of the output pins. The reason for the differences in the results is due to the fact that, for the $G/2$ gates on the side with the excess pinouts, the correction factor must include lines crossing over the imaginary line from the other side to reach these I/Os. The correction factor in this case (enclosed area where $P'_t > P_t/2$) would be $(1 - P'_t/2)W$.

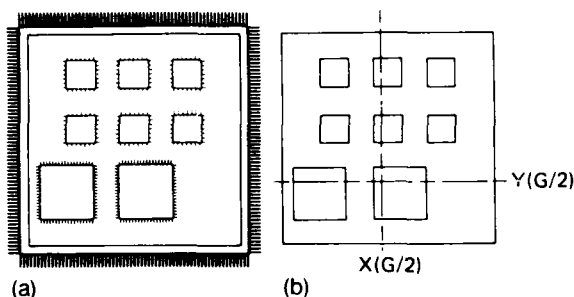


Figure 25 Unsymmetric chip placement leads (a) will break symmetry in the coordinates $X(G/2)$ and $Y(G/2)$ (b) with respect to the package leads. This condition requires modifications to Eq. 119.

+ (excess pinouts)/ W). Therefore, Eq. 119 is correct when $P'_i \leq P_i/2$.

A version of Rent's Rule that permits estimation of the number of circuit card I/Os required when the number of discrete package leads on that card has been specified has not been formally shown to exist. The Rent's Rule relationship for random logic was based on the assumption that a gate talks only to its nearest neigh-

bors. This is not the case for discrete packages and special function LSI or VLSI devices. However, packages placed within close proximity to each other, processing information in real time, would very closely resemble the "random logic" case.

Another circuit density consideration is the number of vias used in that circuit. The number of vias per line increases with increasing circuit density. In many substrate wiring technologies, vias for interconnecting multiple wiring layers can limit the circuit density per layer. This is most notable in PWB technologies using plated through-holes. At higher densities thick-film multilayered vias begin to severely affect routability, even for reduced line width and line spacing. Thick-film vias must be at least 20 mils in diameter—10 mils to insure that the via is not closed prior to or while firing, and another 5 mils on each side of the via to prevent shorting. Via staggering, usually recommended to provide reliability, further limits wiring densities. The effect of vias on wiring density becomes negligible as the via approaches the width of the line. It is for this reason among others that PWB and thick-film technologies are not finding widespread use in high-density circuit applications.

9. ELECTRICAL CHARACTERIZATION AND DESIGN OF MULTILAYER THICK-FILM CIRCUIT BOARDS

In this section some of the theoretical methods discussed previously are used to characterize thick-film multilayer circuits for use in high speed digital applications. Results from an extensive analysis that demonstrates the capabilities and limitations of this technology are then used to provide design guidelines for maximizing the electrical performance of large, thick-film, multilayer circuit boards.

FUNDAMENTAL ELECTRICAL PARAMETERS

In typical thick-film microcircuits gridded ground and power planes are used primarily for both ease of

manufacture and reliability. Grid-plane configurations typically consist of 10-mil lines on 20- or 30-mil centers. Signal lines are placed above or below ground-plane grids in a convenient manner often using automatic routing techniques. In this section the effect of placement of signal lines relative to the underlying ground-plane grid on line capacitance has been investigated. Electrical characteristics for the isolated signal line placed above ground-plane grid lines and those routed over grid spaces were evaluated. The choice of grid spacing in this case was 15-mil lines on 50-mil centers; it was chosen to coincide with the typical lead spacing for leadless ceramic chip carriers. The width of grid line was a somewhat more arbitrary choice; 15-mil lines were

chosen to keep resistance and inductance in ground and power leads to a minimum. Additional motivation for selecting this particular geometry was the eventual use of this configuration in a 40-MHz digital signal processor. The design goal was to keep the total line capacitance under 50 pF.

Calculations were performed using both boundary-element and finite-element methods. Boundary-element methods were used primarily in two-dimensional calculations. The computer programs for performing these calculations were based on the work of C. Wei, et al.⁸ and J. Venkataramen, et al.⁹. The three-dimensional calculations were performed using a finite-element preprocessor for mesh generation and a general finite-element code for solution. The multiconductor configurations analyzed included isolated lines, parallel lines, overlapping parallel lines, crossovers, and dual stripline. These were later analyzed for crosstalk.

Capacitance and impedance measurements were made on specially constructed thick-film test coupons. The geometries assumed for calculations performed in this section of this report were chosen to correspond to the experimental test structures for subsequent comparison. The measured dielectric constant for the thick-film dielectric was approximately 8.0, and the resistance of the gold conductor traces was approximately 3.6 mΩ per square. The typical dielectric layer thickness for these samples was approximately 1.4 mils or 0.7 mil per print. The impedance measurements were made using an HP Network analyzer and an S-parameter test set using methods discussed in the section, "Experimental Methods for Characterizing Device and Package Interconnection."

In Fig. 26 estimated and measured data are presented for the case of a line centered over ground-plane grid spaces and for a line centered over the ground plane grid lines. Comparison of the measured and estimated data shows an acceptable correlation between theory and experiment. As would be expected, the capacitance of the signal lines located directly over the grid lines is significantly higher than for those placed over the grid spaces. As the distance between the ground plane is increased, the differential capacitance between the two configurations decreases. Estimated characteristic impedances for both 10- and 7.5-mil signal lines are displayed in Fig. 27.

In Fig. 28 the capacitance of overlapping parallel signal lines is examined both theoretically and experimentally. Results indicate that significant reductions in line capacitance can be achieved if the top conductor is offset by at least one conductor linewidth.

Crossover capacitance was also estimated and compared with that measured from the capacitance test sam-

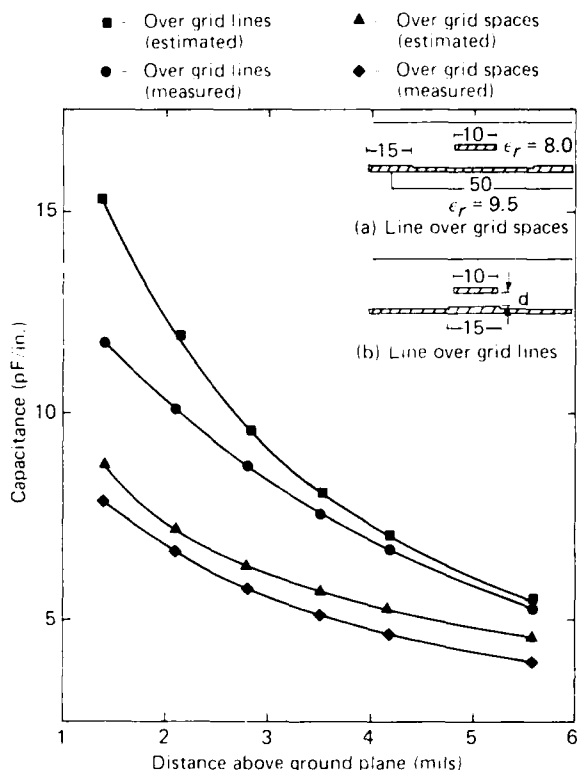


Figure 26 Measured and estimated capacitance for isolated signal lines above a ground plane grid.

ples. The results for 10-mil signal lines are shown in Fig. 29. Estimated values compared quite favorably with the measured ones. The change in the inductance as a result of crossing conductors was estimated to be relatively minor. Thus, the modified characteristic line impedance should be adequately represented by the equation

$$Z_0' = Z_0 / \sqrt{1 + C_c / C_0} \quad (120)$$

where Z_0 and C_0 are the isolated line impedance and capacitance, respectively, and C_c is the crossover capacitance.

The decoupling capacitance between the power and ground planes, and the lead inductance for an individual grid line, were estimated for grid planes configured in the stripline arrangement. This arrangement is desirable since it provides for small lead inductance and large power-supply decoupling capacitance. Inductance in the power-supply leads can introduce voltage spikes dur-

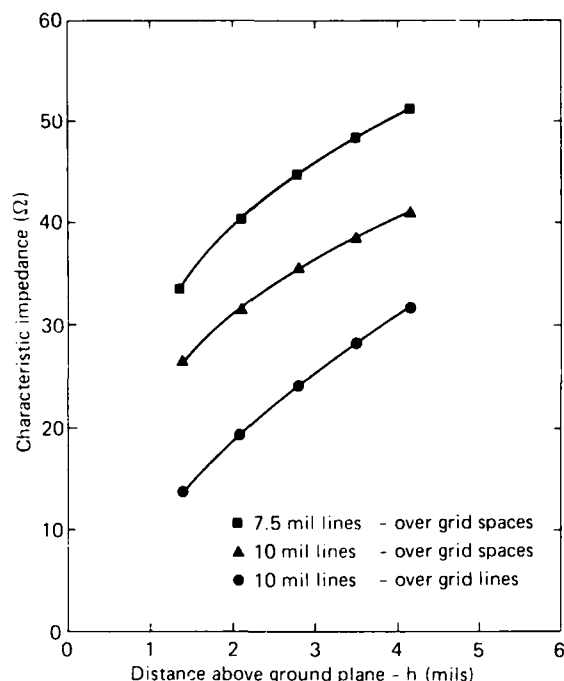


Figure 27 Estimated characteristic impedance for signal lines above a ground plane grid.

ing switching, while inductance in ground return leads can generate undesirable noise spikes that may trigger devices located nearby. The large decoupling capacitance provides a path for transients while storing energy required for rapid charging of signal lines. In Fig. 30 both the microstrip and stripline configurations are illustrated for power and ground planes.

The decoupling capacitance between power and ground (stripline configuration) can be estimated from a three-dimensional finite element analysis using the techniques discussed previously. Eight-fold symmetry considerations significantly reduce the number of finite elements needed in the analysis. The model used for the analysis is illustrated in Fig. 31. The results for ground and for power grid planes spaced 1.4 mils apart, with 15-mil grid lines on 50-mil centers and a dielectric constant of 8.0, yields a total capacitance available for decoupling of ≈ 1400 pF/in.².

The self inductance for a single grid line (stripline configuration) can be estimated using the techniques discussed previously. In Fig. 32 the current distribution from the source to system ground is depicted. For a grid structure each of the current paths represents a parallel inductance. We can neglect the effect of mutual inductance that results from the assumed proximity of overlapping ground and power line conductors. Since in-

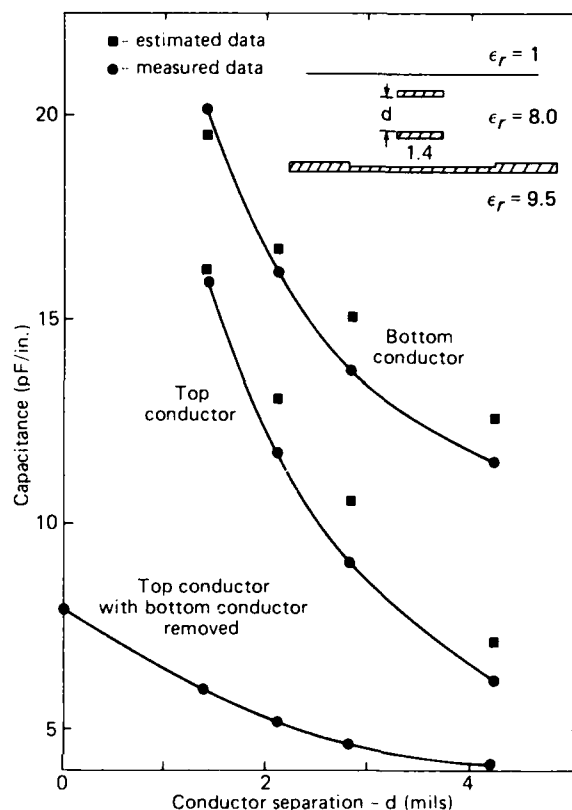


Figure 28 Effect of parallel overlapping conductors on signal line capacitance.

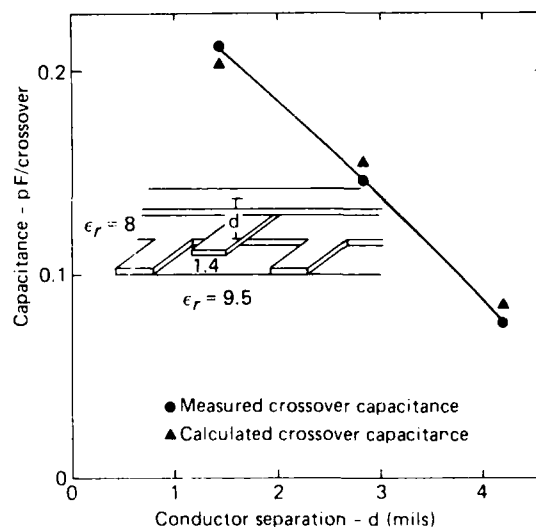


Figure 29 Crossover capacitance for lines over ground plane grid spaces.

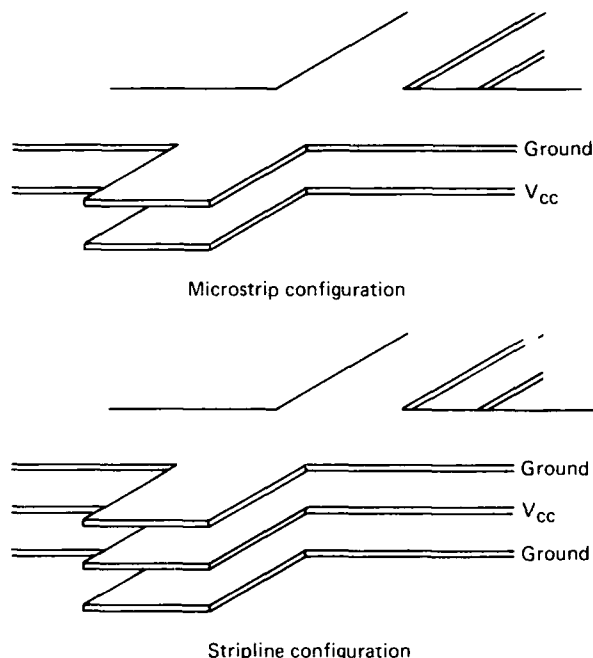


Figure 30 Low-impedance power and ground plane grid structures.

ductors in parallel result in a reduced net inductance, the inductance for the single grid line represents a rather conservative worst-case estimate. In Fig. 33 this worst-case inductance for both the stripline and microstrip configurations is shown as a function of line width and conductor spacing. For the 15-mil grid line on line in the example above, the self-inductance seen by the power- and ground-return leads for this particular configuration is ≈ 1.4 nH/in.

The voltage generated through an inductance L can be given approximately through the relation

$$V = L \frac{dI}{dt} \quad (121)$$

For a current pulse of 100 mA changing in 2 nsec, the voltage drop can be estimated to be less than 70 mV. Due to the parallel inductances of other ground return paths, the actual voltage drop will be much less.

CROSSTALK

For typical multilayer conductor configurations, the crosstalk between parallel lines and overlapping paral-

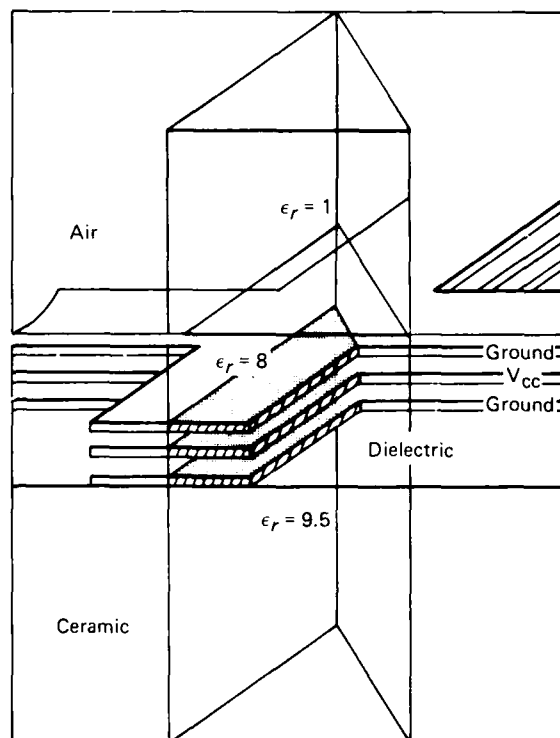
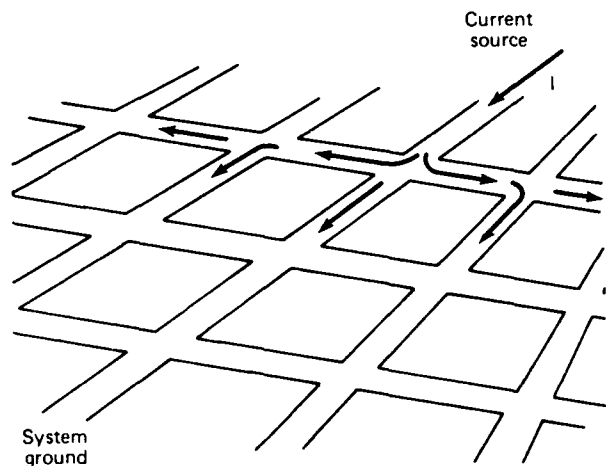


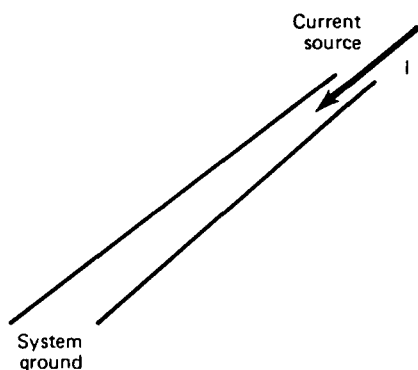
Figure 31 Geometry of a finite-element model to estimate the available decoupling capacitance for the stripline power and ground plane configuration.

lel lines is of primary interest. The results and geometrical configurations for the parallel overlapping conductors are shown in Fig. 34 for a coupled line length of 4 in. The dimensions shown in the figure are typical for multilayer thick-film geometries. For this particular case the crosstalk voltages are in excess of 40% of the voltage swing for an input pulse with a 4-nsec total ramp time. The model was a simulation for Series ALS-TTL logic. In Fig. 35 the same simulation is performed, with the exception that the top conductor is offset from the bottom conductor by approximately one linewidth. The resulting estimated crosstalk is shown to be significantly reduced to about 10% of the voltage swing.

The result for a similar calculation for parallel conductors is shown in Fig. 36. For this particular case two conductor traces were positioned symmetrically between the ground-plane grid lines and the crosstalk voltage evaluated for an input with a 4-nsec ramp time. The coupled length in this case was 6 in. This particular case is of interest because signal lines placed on 50-mil centers would be unacceptable for most practical circuit designs based on circuit density considerations. Calculated near- and far-end voltages for the quiet line (in the high state)



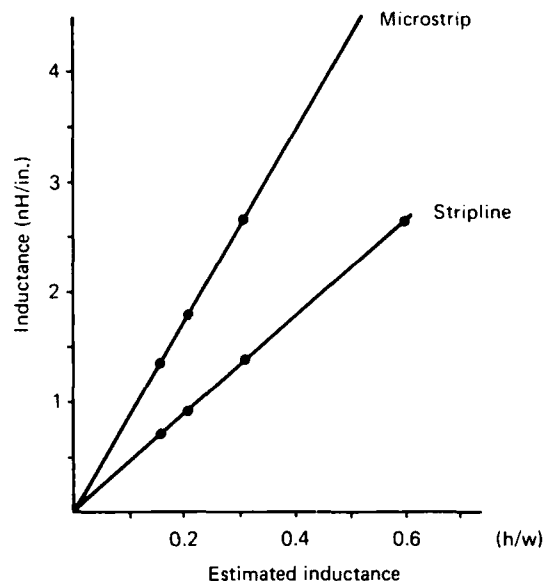
(a) Parallel current paths to system ground.



(b) Worst case model for estimating inductance in ground return paths.

Figure 32 Estimating inductance on ground return paths.

indicated crosstalk levels less than 10% of the voltage swing. The impedance for each line was approximately the same as that for the isolated-line case. This is because each line was only effectively being coupled to the nearest grid line. The same conductor configuration was used to simulate the crosstalk for the faster rising Series ASTTL logic. The results are shown in Fig. 37 for a 2-nsec ramp time. The crosstalk voltages are significantly higher as a result of the faster risetime of the output drivers. Ringing is apparent in this figure and results from the lower dynamic output impedance assumed for this calculation and the long, unterminated line lengths. For TTL devices this overshoot should be limited to 5.5 V to avoid emitter-to-emitter breakdown of the receiver gate.



2-D models to estimate the inductance of ground returns

Figure 33 Worst case estimates of the inductance of ground returns for low impedance ground and power plane grid configurations.

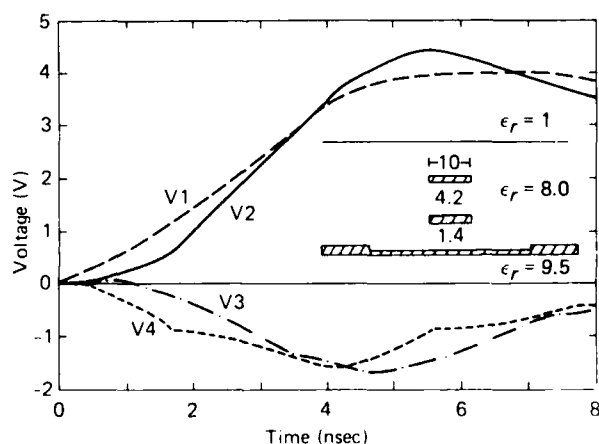


Figure 34 Estimated crosstalk between overlapping parallel conductors for simulated 4-nsec ALSTTL 0-1 transition, 4.0-in. coupled length.

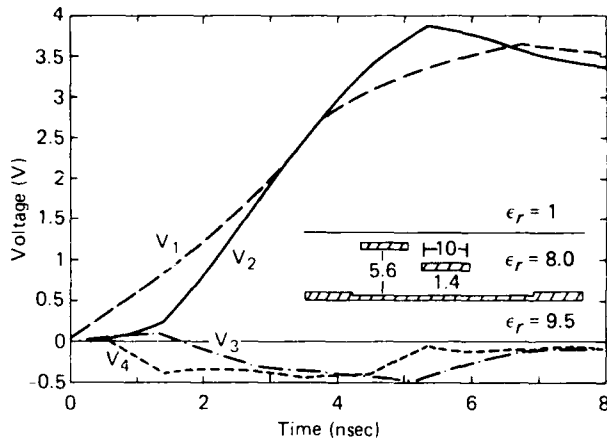


Figure 35 Estimated crosstalk between offset overlapping parallel conductors for simulated 4-nsec ALSTTL 0-1 transition, 4.0-in. coupled length.

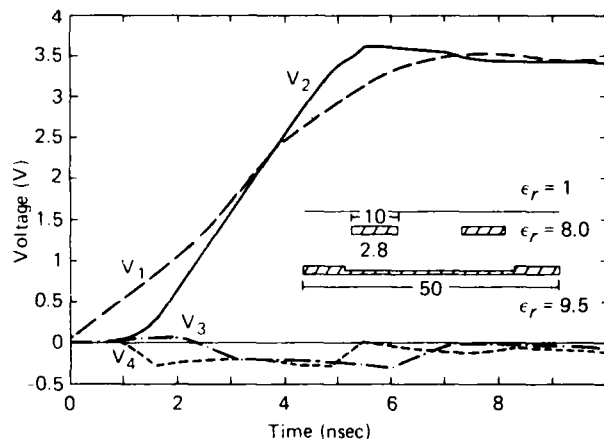


Figure 36 Estimated crosstalk voltage between parallel conductors with 4-nsec input ramp (6.0-in. coupled length).

The dual-stripline configuration was also studied for use in multilayer applications involving the faster logic technologies such as ECL. The dual stripline consisted of two orthogonal signal layers contained between two ground planes. Because of symmetry shared by these signal layers, their characteristic impedance will be approximately the same. Thus, an interconnect that must partially reside on both layers (e.g., horizontally oriented on one layer and vertically oriented on another) will not experience impedance discontinuities that will result in reflections. Also, crosstalk will be minimized owing to the orthogonality of the two partially shielded signal

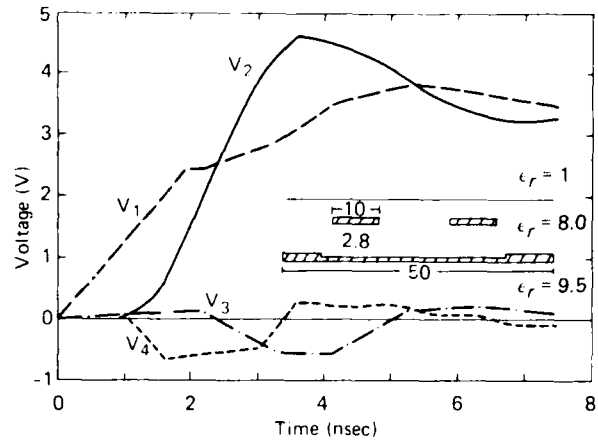


Figure 37 Estimated crosstalk voltage between parallel conductors with 2-nsec input ramp (6.0-in. coupled length).

layers. In Fig. 38 estimated crosstalk between signals separated by a ground-plane grid for two adjacent dual stripline layers is shown. A coupled length of 4 in. was assumed for a simulated 1-nsec ECL (100K) 0-to-1 transition. The coupling was maintained at less than 0.25% of the voltage swing. The reduced ringing for the relatively long unterminated length of transmission line is a result of the lower impedance of the dual-stripline configuration ($\approx 16 \Omega$). Because of the low signal-line impedance of this configuration, the thick-film dual stripline is not recommended for low-power device technologies that are unable to drive large capacitive loads.

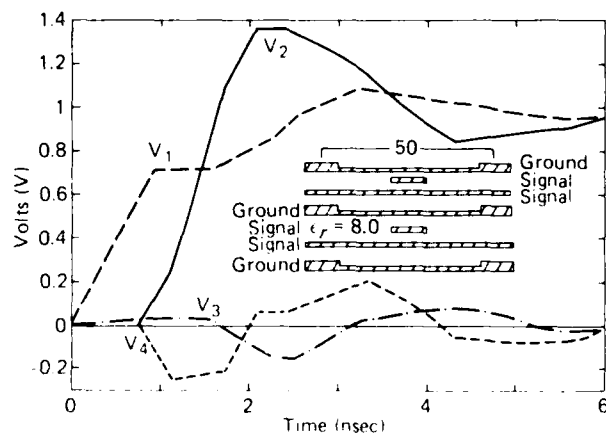


Figure 38 Estimated crosstalk between ground grid plane for dual stripline configuration for simulated 1-nsec ECL 0-1 transition (4-in.-coupled length).

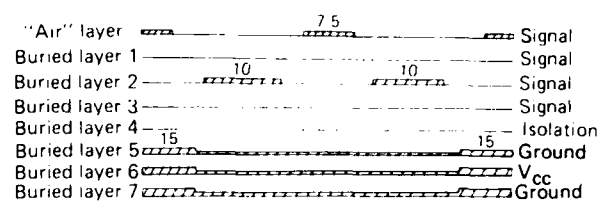
SUMMARY OF MULTILAYER THICK-FILM CHARACTERIZATION

Optimizing Circuit Layout

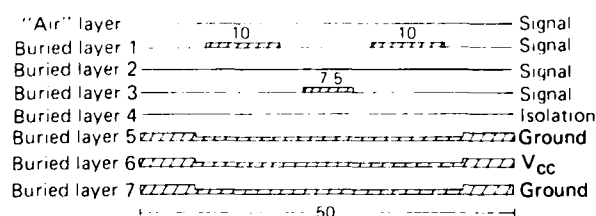
Significant improvements in circuit performance can be achieved by optimizing the circuit design. Improving system design through both effective circuit partitioning and optimization of component placement and data flow can reduce the overall length of device interconnections. Devices with I/Os coming on or off the circuit board should be placed as close to the edge connector as possible to reduce the length of these critical lines. Card- or board-edge connections should encompass as much of the circuit card edge as possible. Applying Rent's Rule to circuit wiring design indicates that significant reductions in circuit density can be achieved when circuit-edge connections are made as physically wide as practical. Lower circuit densities mean less crosstalk and higher line impedances. A significant reduction in wiring congestion can be achieved if edge connections can be made to two or more edges of the circuit card.

Low Capacitance Design

Time delays are primarily a function of the line and load capacitance when device interconnections are shorter than the critical length. Improving system performance requires that the longest device interconnects be located farthest from the ground plane. Locating these critical lines above the ground-plane grid spaces can significantly reduce the overall capacitive loading of conductor traces. An example of a high-density, low-capacitance configuration is illustrated in Fig. 39. This configuration provides excellent crosstalk immunity for coupled lengths up to 6 in. for pulse rise and fall times greater than 2 nsec. The design consists of seven buried metal layers and one surface or "air" layer. Thick-film circuits are generally limited to eight conductor levels because of manufacturing and reliability constraints. The full use of the maximum allowable number of layers is recommended to preserve the higher-characteristic line impedance even if the allowable number of layers is not warranted by circuit-density considerations. Minimum line widths are nominally set at 10 mils; however, capacitance considerations may necessitate the use of smaller line widths for longer lines. Three prints of dielectric (≈ 2 mils) are recommended between congested signal layers to keep crossover capacitance to a minimum and to preserve line impedance. Overlapping parallel conductors should be avoided. The "air" and first buried layers are reserved for high-frequency clock lines and long signal lines. Buried layers two and three are reserved for short lines.



(a) Signal line configuration for north-south traveling signals.



(b) Signal line configuration for east-west traveling signals.

Figure 39 High density-low capacitance conductor configuration for multilayer thick-film signal layers with ground and power grid plane.

For ground and power grid planes, the grid spacings should not be so large as to effectively limit current flow to a single grid line. Individual grid lines should be wide enough so that both resistance and self inductance of ground returns are sufficiently low to preserve noise margins. The optimal arrangement for ground and power grid planes is the stripline configuration (see Fig. 30), which should be placed either at the top or bottom of the multilevel stack. Power and ground grid planes consisting of 10-mil lines on 50-mil centers should be adequate for high speed TTL device technologies. Technologies using considerably more power should use wider grid lines with smaller spaces. The use of a ground strap may be useful in reducing the ground return length for the higher impedance grid lines.

Thick-film multilayer signal lines are inherently capacitive, with a characteristic impedance range of about 20 to 50 Ω . These low impedance values result from the typically large conductor-width-to-dielectric thickness ratio and the high K for thick-film dielectric materials. For large circuit board applications, the circuit design must be "soft" enough to accommodate a nominal line capacitance of 50 pF for long signal lines. Even when allowing for this amount of capacitance, considerable care must be exercised when routing interconnects. Additional decoupling capacitance should be provided close to devices to allow storage of sufficient energy for rapid charging of these high-capacitive loads.

Controlled Impedance Design

Controlling impedance for higher-speed-device technologies (such as ECL and GaAs) is important for eliminating signal reflections from impedance discontinuities. The results from impedance measurements and calculations indicate that a combination of linewidths, conductor spacings, and positions relative to ground-conductor grid lines can produce numerous orientations on several layers, yielding a narrow range of characteristic impedances. As was discussed in the section on "Substrate Interconnect Requirements," the dual stripline configuration is ideal for multilevel circuit-board applications. However, thick-film dual striplines

have a lower impedance ($\approx 16 \Omega$) than is desirable for high speed applications.

Before thick-film multilayer technology can become important for high speed applications, improvements must be made in thick-film dielectrics and printing techniques. Dielectrics will have to possess a considerably lower relative dielectric constant (< 4.0) and be resistant to the warpage that usually limits the number of dielectric prints, which limit conductor spacings. In addition, thick-film conductor lines will have to be narrower to increase characteristic impedance values while accommodating the wiring densities needed for VLSI and VHSIC devices.

10. FUTURE TRENDS IN VLSI/VHSIC PACKAGING

Development of a VLSI packaging concept requires that the designer have in mind those characteristics that are the embodiment of the ideal VLSI packaging scheme, which of course does not exist. This ideal packaging system would use a substrate and device package medium possessing the ideal dielectric constant (i.e., $K = 1$), infinite thermal conductivity, excellent mechanical strength for both circuit board and interconnections, and be inexpensive to fabricate. Other desirable characteristics would include tailorable characteristic impedance, high circuit density, high I/O support, hermetic packaging, ease of fabrication, testability, and repairability. Clearly, if a substrate and packaging material were available that possessed all of the above characteristics, the microelectronics industry would likely undergo a renaissance.

Currently, most of the research and development efforts in the VLSI and VHSIC areas are being focused on the development of high-density multichip modules. The multichip concept has been a result of the realization that for high speed operation, interconnect lengths must be kept short. The multichip module is composed of a complex (high-density) chip set, partitioned from the system for inclusion into the module in such a way that the internal speed is much greater than the bit trans-

ferral rates into and out of the module. Wiring densities in these modules must be high to accommodate the high I/O densities of these complex chips. Ultimately, the internal wiring density will determine the degree of functionality that VLSI and VHSIC devices can provide.

MULTICHIP MODULE SYSTEMS

At the present time these multichip modules have resembled the hybrid form and consist of VLSI chips TAB-bonded to a multilayer thin-film hybrid of polyimide dielectric on ceramic. The ceramic is then bonded to a metal package with a material of high thermal conductivity for transferring heat from the module. For maximum I/O capability, perimeter leaded metal packages with leads on 20-mil centers will be required. The ceramic currently being used for these applications is alumina. In the near future the base ceramic for these multichip modules may become aluminum nitride because of its superior thermal conductivity.

For various reasons it is more efficient to include several of these multichip modules in a larger circuit board, with room for VLSI and VHSIC glue chips. The glue chips would integrate several of the multipurpose,

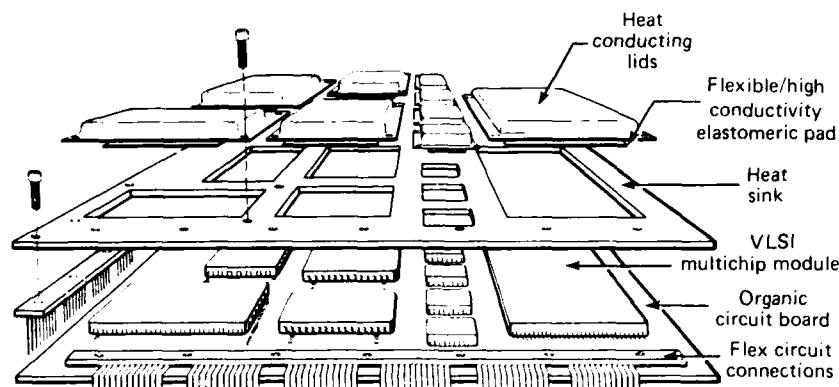


Figure 40 Conceptualization of the required electronic packaging scheme for high-speed/high-density VLSI/VHSIC applications.

multichip modules together and adapt them for use for a specific circuit application. In order to maintain the performance levels provided by the multichip modules, it is desirable to maintain high speed signal propagation at the circuit board level. Thus, the circuit board should be made of a low-K dielectric material and should be multilayered to accommodate the high circuit densities required by the multichip modules. Since low-K organic circuit board materials typically have very low thermal conductivities, some form of heat sinking will be required. For such operating environments as land-based or shipboard electronic equipment, conventional heat-sinking techniques such as forced convection and cryogenic cooling are available. For applications like air and space electronics, where thermal conductivity is the principal method of heat transfer, packages must be contacted directly by high-thermal-conductivity materials such as the direct attachment of a circuit board to a metal heat sink.

The ideal placement of the heat sink would be directly adjacent to the bottom of the chip or module package. This presents some real problems when attempting to heat-sink perimeter-style leadless and leaded packages. The obvious alternative to this type of heat sinking is to conduct heat away from the top portion of the package. This provides an ideal situation if the device package or module is in the cavity-down configuration. In this manner, the heat sink assumes the task of the ideal circuit board in conducting heat away from the devices while the circuit board provides high speed interconnects only.

A thermal conduction module and circuit board system for VLSI and VHSIC applications is shown schematically in Fig. 40. Here the circuit board serves only to connect the individual modules, while the sole func-

tion of the heat sink is that of heat removal. The heat sink has cutouts for the leaded (or leadless) packages to be inserted. The heat-conducting lids can be screwed onto the heat sink with a thermally conductive elastomeric material between the top portion of the package and the lid. This thin sheet of elastic material provides a nonbondable thermal contact, allowing both testing and subsequent rework. Once thoroughly tested, and prior to actual implementation, the lids can be epoxy-bonded or even soldered to the packages for improved thermal contact. For situations where the TCE of the heat sink is very different from that of the packages or modules (such as aluminum and ceramic), high-thermal-conductivity flexible adhesives such as silicones can be used.

The external I/O connections shown in Fig. 39 are of a flexible circuit material. The use of flexible connectors facilitates development of three-dimensional packaging schemes. Flexible circuits can be multilayered to provide for ground planes for 50- Ω transmission line interconnections. As for multichip modules, circuit board I/O connections should be available around the entire perimeter.

Currently, the two most promising candidates for the multichip module appear to be the copper/polyimide on a ceramic thin-film module (or any other suitable low-TCE material) and the low-temperature cofirable tape (either on ceramic or by itself). Both systems offer VLSI-compatible circuit densities with nominal line capacitance. The cofirable material, however, possesses the edge in the fabrication of transmission line interconnects as well as the ability to accommodate more layers. One possible combination may include both the copper/polyimide and the cofired multilayer ceramic. In this scheme, power and ground layers would be lo-

cated within the cofired ceramic, which would also serve as a substrate medium for the copper/polyimide signal and insulation levels.

With the increasing popularity of thin-film copper polyimide, multilevel cofired ceramic modules may become commercially available for use as a universal sub-

strate for copper/polyimide circuits. These universal substrates would have several buried layers for distributed ground and power planes, and vias would be distributed along the top portions of the modules for interconnection to the devices.

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APPENDIX A

The four computer programs in this appendix are the following: MAIN, a program to calculate the coefficients of capacitance for an arbitrary arrangement of n -conductors with a finite ground plane; MAINL, a complementary program to MAIN to calculate the coefficients of inductance; MAINI, a program to calculate the coefficients of capacitance for an arbitrary arrangement of n -conductors over an infinite ground plane; and MAINIL, a complementary program to MAINI that calculates the coefficients of inductance. The programs MAIN and MAINL are general, in that the ground planes can have any arbitrary shape or extent. The programs MAINI and MAINIL are included because in many cases the infinite ground plane approximation is applicable, and the formalism used to account for the effect of this ground plane does not require that any boundary elements be used to model these effects. This can result in significant savings in computational time when the approximation is valid. Any additional ground planes, however, must be discretized.

Included with these four programs is a basic program written to perform the discretization of the conductor and dielectric interfaces and to format the input to the main programs. The geometry of an arbitrary arrangement of two conductors, one thin and the other infinitely thin, embedded in two dielectric media over an infinite ground plane is illustrated in Fig. 41(a). The discretization of conductor boundaries and dielectric interfaces is illustrated in Fig. 41(b). This program, called DISCRETE, asks the user for information concerning the following items: the number of ground planes required; nature of ground planes, such as infinite or not; conductor shape (round or polygonal); radius and center or coordinates of corners for conductors (up to six); and the relative dielectric permittivity on either side of a dielectric-dielectric or conductor-dielectric interface (note: permittivity 1 is on the side of the boundary in which the normal vector to that boundary is positive).

The input variables required for the four main programs are illustrated in Figs. 42(a) and 42(b) for conductor-dielectric and dielectric-dielectric interfaces, respectively. They include a coordinate for each subinterval or boundary element, the length of each element, the angle of the element relative to a fixed coordinate, and the relative permittivities on either side of the element. More information on the details of this program can be found in Refs. 8 and 9.

The notations used for these variables within the following computer programs are listed below.

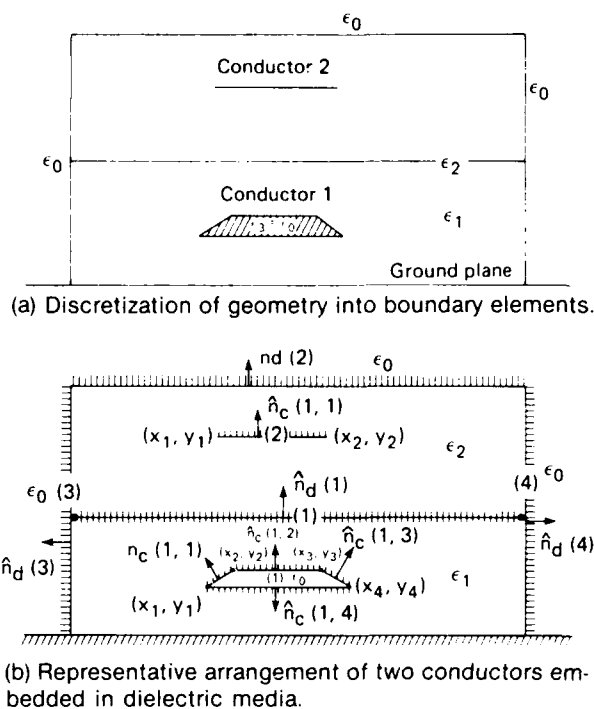
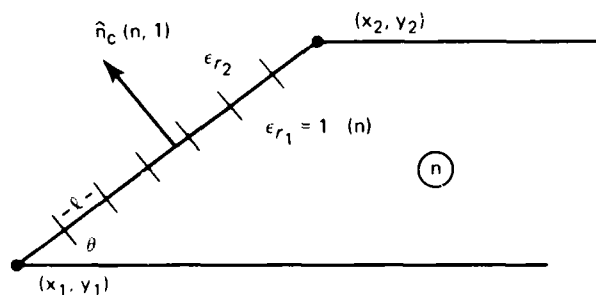
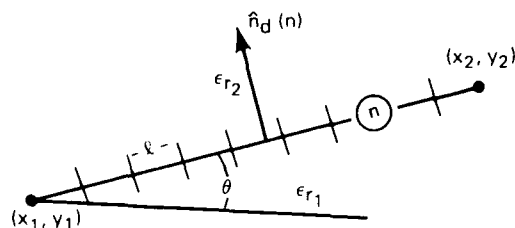


Figure 41 Discretization process for utilizing the boundary element computer program in Appendix A.

- nc—number of conductors
- ns(i)—number of sections for the i th conductor
- nscc(i,j)—number of elements for i th conductor and j th conductor section
- nd—number of dielectric interfaces
- nssd(i)—number of elements for the i th dielectric-dielectric interface
- $x(n), y(n)$ —coordinates of the n th boundary element
- theta(n)—angle of orientation for n th boundary element
- $l(n)$ —length of the n th boundary element
- er2(n)—relative permittivity of the medium on the positive normal side of the n th boundary element
- er1(n)—relative permittivity of the medium on the negative normal side of the n th boundary element



(a) Variables required to characterize conductor boundary elements.



(b) Variables required to characterize dielectric-dielectric interfaces.

Figure 42 Variables used to characterize boundary elements used in the computer programs of Appendix A.

MAIN

```
c Program Main. copyright The Johns Hopkins University/
c Applied Physics Laboratory, 1987
c
c Program to calculate capacitance and inductance matrix
c dimension ns(6),nssc(6,4),nssd(12),x(175),y(175),theta(175),
c $ er2(175),er1(175),z1(175),q(5,5),s1(175,175),
c $ ncd1(6),ncd2(6),si(175,175),fcd(175),v(175)
c real l(175),zz
c real*8 pi
c pi=3.141592
c e0=.225e-12
c ep=1/(4*pi*e0)
c
c
c Read data from file
c
c
c n=0
c open(7,file='b:data.for',form='formatted')
c read(7,*) nc
c do 30 i=1,nc
c read(7,*) ns(i)
c do 20 j=1,ns(i)
c read(7,*) nssc(i,j)
c do 10 k=1,nssc(i,j)
c n=n+1
c read(7,*) x(n),y(n),theta(n),l(n)
c read(7,*) er2(n),er1(n)
10 continue
20 continue
30 continue
c n1=n
c read(7,*) ncc
c
c
c Read in dielectric interface data
c
c
c read(7,*) nd
c do 50 i=1,nd
c read(7,*) nssd(i)
c do 40 j= 1,nssd(i)
```

```

n=n+1
read(7,*) x(n),y(n),theta(n),l(n)
read(7,*) er2(n),er1(n)
40 continue
50 continue
n2=n
close(7,status='keep')
c Assemble matrices S1 and S2
i=1
do 60 j=1,n2
s1(i,j)=1(j)
call intg1(x(i),x(j),y(i),y(j),theta(j),l(j),zz)
z1(j)=ep*zz
60 continue
do 80 i=2,n1
do 70 j=1,n2
call intg1(x(i),x(j),y(i),y(j),theta(j),l(j),zz)
s1(i,j)=-ep*zz+z1(j)
c write(*,*) 's1=',i,j,s1(i,j)
70 continue
80 continue
do 100 i=n1+1,n2
do 90 j=1,n2
if (i.eq.j) then
s1(i,j)=(er1(i)+er2(i))/2
else
call intg2(x(i),x(j),y(i),y(j),theta(j),theta(i),l(j),zz)
s1(i,j)=((er2(i)-er1(i))/(2*pi))*zz
endif
c write(*,*) 's1=',i,j,s1(i,j)
90 continue
100 continue
c
c calculate inverse of s1 matrix:
c
call inverse(s1,n2,s1)
c
c Assemble S2 matrix:
c
do 120 i=1,n1
do 110 j=1,n2
if (i.eq.j) then
s1(i,j)=(er2(i)+er1(i))/2
else
call intg2(x(i),x(j),y(i),y(j),theta(j),theta(i),l(j),zz)
s1(i,j)=((er2(i)-er1(i))/(2*pi))*zz
endif
110 continue
120 continue
c capacitance calculation portion of Main
c pause 'hit enter to continue'
call segmt(nc,ns,nssc,ncd1,ncd2)
c calculate voltage matrix:
do 180 i=nc+1,nc
c
c subroutine voltage returns voltage vector
c
call voltage(i,ncd1(i),ncd2(i),v,n1,n2)
c
c subroutine matrix performs matrix operations and returns free
c charge density vector
c
call matrix(s1,s1,v,n1,n2,fcd)
c
c sum up charge on each conductor and return capacitance coefficients
c

```

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```

do 170 j=ncc+1,nc
q(i-ncc,j-ncc)=0.0
do 160 k=ncd1(j),ncd2(j)
q(i-ncc,j-ncc)=fcd(k)*i(k)+q(i-ncc,j-ncc)
160 continue
170 continue
180 continue
do 190 i=1,nc-ncc
do 185 j=1,nc-ncc
write(*,*) 'capacitance ',i,j,q(i,j)
185 continue
190 continue
stop 'program terminated normally'
end

```

MAINL

```

c Program Mainl. copyright The Johns Hopkins University/
c Applied Physics Laboratory, 1987
c Program to calculate capacitance and inductance matrix
dimension ns(6),nssc(6,4),x(175),y(175),theta(175),
$ er2(175),er1(175),z1(175),s1(175,175),q(5,5),
$ ncd1(6),ncd2(6),si(175,175),fcd(175),v(175)
real l(175),zz,ind(5,5)
real*8 pi
pi=3.141592
e0=.225e-12
ep=1/(4*pi*e0)
c
c Read data from file
c
n=0
open(7,file='b:data.for',form='formatted')
read(7,*) nc
do 30 i=1,nc
read(7,*) ns(i)
do 20 j=1,ns(i)
read(7,*) nssc(i,j)
do 10 k=1,nssc(i,j)
n=n+1
read(7,*) x(n),y(n),theta(n),l(n)
read(7,*) er2(n),er1(n)
10 continue
20 continue
30 continue
n1=n
n2=n1
read(7,*) ncc
close(7,status='keep')
c Assemble matrix S1
i=1
do 60 j=1,n1
s1(i,j)=1(j)
call intg1(x(i),x(j),y(i),y(j),theta(j),l(j),zz)
z1(j)=ep*zz
60 continue
do 80 i=2,n1
do 70 j=1,n2
call intg1(x(i),x(j),y(i),y(j),theta(j),l(j),zz)
s1(i,j)=-ep*zz+z1(j)
70 continue
80 continue
c

```

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```

c calculate inverse of s1 matrix
c
      call inverse(s1,n1,s1)
c capacitance calculation portion of Main
c pause 'hit enter to continue'
      call segmt(nc,ns,nssc,ncd1,ncd2)
c calculate voltage matrix
      do 180 i=ncc+1,nc
c
c      subroutine voltage returns voltage vector
c
      do 85 ii=1,ncd1(i)-1
        v(ii)=0.0
      85 continue
      do 86 ii=ncd1(i),ncd2(i)
        v(ii)=1.0
      86 continue
      do 87 ii=ncd2(i)+1,n1
        v(ii)=0.0
      87 continue
c
c      subroutine matrix performs matrix operations and returns free
c      charge density vector
c
      call matmult(s1,v,n1,n1,fcd)
c
c      sum up charge on each conductor and return capacitance coefficients
c
      do 170 j=ncc+1,nc
        q(i-ncc,j-ncc)=0.0
        do 160 k=ncd1(j),ncd2(j)
          q(i-ncc,j-ncc)=fcd(k)*1(k)+q(i-ncc,j-ncc)
        160 continue
      170 continue
      180 continue
      do 190 i=1,nc-ncc
        do 185 j=1,nc-ncc
          write(*,*) 'capacitance ',i,j,q(i,j)
        185 continue
      190 continue
      n=nc-ncc
      call inversel(q,n,ind)
      do 210 i=1,nc-ncc
        do 200 j=1,nc-ncc
          write(*,*) ' Inductance ',i,j,ind(i,j)/1.395e20
        200 continue
      210 continue
      stop 'program terminated normally'
      end

```

MAIN1

```

c Program Main1. copyright The Johns Hopkins University/
c Applied Physics Laboratory. 1987
c      Program to calculate capacitance and inductance matrix
      dimension ns(6),nssc(6,4),nssd(12),x(175),y(175),theta(175),
$      er2(175),er1(175),s1(175,175),q(5,5),
$      ncd1(6),ncd2(6),s1(175,175),fcd(175),v(175)
      real l(175),zz,z1,z2
      real*8 pi
      pi=3.141592
      e0=.225e-12
      ep=1/(4*pi*e0)

```

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```

c
c Read data from file
c
      n=0
      open(7,file='b:data.for',form='formatted')
      read(7,*) nc
      do 30 i=1,nc
        read(7,*) ns(i)
        do 20 j=1,ns(i)
          read(7,*) nssc(i,j)
          do 10 k=1,nssc(i,j)
            n=n+1
            read(7,*) x(n),y(n),theta(n),l(n)
            read(7,*) er2(n),er1(n)
10          continue
20          continue
30          continue
            n1=n
            read(7,*) ncc
c
c Read in dielectric interface data
c
      read(7,*) nd
      do 50 i=1,nd
        read(7,*) nssd(i)
        do 40 j= 1,nssd(i)
          n=n+1
          read(7,*) x(n),y(n),theta(n),l(n)
          read(7,*) er2(n),er1(n)
40          continue
50          continue
            n2=n
            write(*,*) ' n2 = ',n2
            close(7,status='keep')
c Assemble matrices S1 and S2
      do 80 i=1,n1
        do 70 j=1,n2
          call int11(x(i),x(j),y(i),y(j),theta(j),l(j),z1)
          s1(i,j)=ep*z1
c
c write(*,*) ' s1= ',i,j,s1(i,j)
70          continue
80          continue
        do 100 i=n1+1,n2
          do 90 j=1,n2
            if (i.eq.j) then
              call int22(x(i),x(j),y(i),y(j),theta(j),theta(i),l(j),z1,z2)
              s1(i,j)=(er1(i)+er2(i))/2-(er2(i)-er1(i))*z1/(2*pi)
            else
              call int22(x(i),x(j),y(i),y(j),theta(j),theta(i),l(j),z1,z2)
              s1(i,j)=(er2(i)-er1(i))*(z2-z1)/(2*pi)
            endif
c
c write(*,*) 's1= ',i,j,s1(i,j)
90          continue
100         continue
c
c calculate inverse of s1 matrix:
c
      call inverse(s1,n2,s1)
c
c Assemble S2 matrix:
c
      do 120 i=1,n1
        do 110 j=1,n2
          if (i.eq.j) then
            call int22(x(i),x(j),y(i),y(j),theta(j),theta(i),l(j),z1,z2)
            s1(i,j)=(er2(i)+er1(i))/2-(er2(i)-er1(i))*z1/(2*pi)

```

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```

      else
        call int22(x(i),x(j),y(i),y(j),theta(j),theta(i),l(j),z1,z2)
        s1(i,j)=(er2(i)-er1(i))*(z2-z1)/(2*pi)
      endif
110  continue
120  continue
c    capacitance calculation portion of Main
c    pause 'hit enter to continue'
c    call segmt(nc,ns,nssc,ncd1,ncd2)
c    calculate voltage matrix
      do 180 i=ncc+1,nc
c
c    subroutine voltage returns voltage vector
c
      do 124 ii=1,ncd1(i)-1
        v(ii)=0.0
124  continue
      do 125 ii=ncd1(i),ncd2(i)
        v(ii)=1.0
125  continue
      do 126 ii=ncd2(i)+1,n2
        v(ii)=0.0
126  continue
c
c    subroutine matrix performs matrix operations and returns free
c    charge density vector
c
      call matrix(s1,s1,v,n1,n2,fcd)
c
c    sum up charge on each conductor and return capacitance coefficients
c
      do 170 j=ncc+1,nc
        q(i-ncc,j-ncc)=0.0
        do 160 k=ncd1(j),ncd2(j)
          q(i-ncc,j-ncc)=fcd(k)*l(k)+q(i-ncc,j-ncc)
160  continue
170  continue
180  continue
      do 190 i=1,nc-ncc
        do 185 j=1,nc-ncc
          write(*,*) 'capacitance ',i,j,q(i,j)
185  continue
190  continue
      stop 'program terminated normally'
      end

```

MAINIL

```

c Program Mainil. copyright The Johns Hopkins University/
c Applied Physics Laboratory, 1987
c    Program to calculate capacitance and inductance matrix
c    dimension ns(6),nssc(6,4),x(175),y(175),theta(175),
c    $ er2(175),er1(175),z1(175),s1(175,175),q(5,5),
c    $ ncd1(6),ncd2(6),s1(175,175),fcd(175),v(175)
c    real l(175),zz,ind(5,5)
c    real*8 pi
c    pi=3.141592
c    e0=.225e-12
c    ep=1/(4*pi*e0)
c
c    Read data from file
c

```

```

n=0
open(7,file='b:data.for',form='formatted')
read(7,*) nc
do 30 i=1,nc
  read(7,*) ns(i)
  do 20 j=1,ns(i)
    read(7,*) nssc(i,j)
    do 10 k=1,nssc(i,j)
      n=n+1
      read(7,*) x(n),y(n),theta(n),l(n)
      read(7,*) er2(n),er1(n)
10    continue
20    continue
30    continue
      n1=n
      n2=n1
      read(7,*) ncc
      close(7,status='keep')
c    Assemble matrix S1
      do 80 i=1,n1
        do 70 j=1,n2
          call int11(x(i),x(j),y(i),y(j),theta(j),l(j),zz)
          s1(i,j)=ep*zz
70      continue
80      continue
c
c    calculate inverse of s1 matrix
c
      call inverse(s1,n1,s1)
c    capacitance calculation portion of Main
c    pause 'hit enter to continue'
      call segmt(nc,ns,nssc,ncd1,ncd2)
c    calculate voltage matrix
      do 180 i=1+ncc,nc
c
c    subroutine voltage returns voltage vector
c
        do 151 ii=1,ncd1(i)-1
          v(ii)=0.0
151      continue
          do 152 ii=ncd1(i),ncd2(i)
            v(ii)=1.0
152      continue
          do 153 ii=ncd2(i)+1,n1
            v(ii)=0.0
153      continue
c
c    subroutine matrix performs matrix operations and returns free
c    charge density vector
c
          call matmult(s1,v,n1,n1,fcd)
c
c    sum up charge on each conductor and return capacitance coefficients
c
          do 170 j=1+ncc,nc
            q(i+ncc,j+ncc)=0.0
            do 160 k=ncd1(j),ncd2(j)
              q(i+ncc,j+ncc)=fcd(k)*l(k)+q(i+ncc,j+ncc)
160          continue
170          continue
180          continue
          do 190 i=1,nc-ncc
            do 185 j=1,nc-ncc
              write(*,*) 'capacitance ',i,j,q(i,j)
185            continue
190            continue

```

```

n=nc-ncc
call inversel(q,n,ind)
do 210 i=1,nc-ncc
do 200 j=1,nc-ncc
write(*,*) ' Inductance ',i,j,ind(i,j)/1.395e20
200 continue
210 continue
stop 'program terminated normally'
end

```

REQUIRED SUBROUTINES

Matmult

```

c this subroutine performs matrix multiplication
subroutine matmult(a,b,m,l,c)
dimension a(175,175),b(175),c(175)
do 100 i=1,m
c(i)=0.0
do 25 k=1,l
c(i)=c(i)+a(i,k)*b(k)
25 continue
c write(*,*) i,c(i)
100 continue
return
end

```

Segmt

```

c This subroutine associates conductor segments with a particular
c conductor
subroutine segmt(ii,jj,kk,mm,nn)
dimension jj(6),kk(6,4),mm(6),nn(6),nsc(6)
integer st
do 10 i=1,ii
nsc(i)=0
10 continue
do 40 i=1,ii
do 30 j=1,jj(i)
do 20 k=1,kk(i,j)
nsc(i)=nsc(i)+1
20 continue
30 continue
40 continue
st=1
nd=0
do 50 i=1,ii
mm(i)=st
nn(i)=nsc(i)+nd
st=nn(i)+1
nd=nn(i)
50 continue
return
end

```

Voltage

```

c This subroutine calculates the voltage matrix:
  subroutine voltage(ii,kk,ll,vv,mm,nn)
    dimension vv(175)
    do 10 i=1,kk-1
      vv(i)=0.0
10    continue
    do 20 i=kk,ll
      vv(i)=1.0
20    continue
    do 30 i=ll+1,nn
      vv(i)=0.0
30    continue
    return
  end
  
```

Inverse

```

c Invert an nxn matrix:
  subroutine inverse(a,n,b)
    dimension a(175,175),b(175,175)
    integer check,ret,sin
    assign 28 to sin
    assign 200 to check
    assign 250 to ret
    do 20 i=1,n
      do 10 j=1,n
        if (i.eq.j) then
          b(i,j)=1.0
        else
          b(i,j)=0.0
        endif
10      continue
20    continue
    do 60 j=1,n
      do 25 i=j,n
        if (a(i,j).ne.0.0) then
          goto sin
        endif
25      continue
        goto check
      do 30 k=1,n
        s=a(j,k)
        a(j,k)=a(i,k)
        a(i,k)=s
        s=b(j,k)
        b(j,k)=b(i,k)
        b(i,k)=s
30      continue
        t=1/a(j,j)
        do 40 l=1,n
          a(j,l)=t*a(j,l)
          b(j,l)=t*b(j,l)
40      continue
        do 45 l=1,n
          if (l.ne.j) then
            t=-1*a(l,j)
            do 43 k=1,n
              a(l,k)=a(l,k)+t*a(j,k)
              b(l,k)=b(l,k)+t*b(j,k)
            43      continue
          45      continue
        
```

```

43      continue
      endif
45      continue
60      continue
      goto ret
200     write(*,210) ' array is singular'
210     format(a)
250     return
      end

```

Matrix

```

c      This subroutine calculates the free charge density vector
      subroutine matrix(sii,s22,vv,mm,nn,g)
      dimension t(175),g(175),s22(175,175),sii(175,175),vv(175)
      call matmult(sii,vv,nn,nn,t)
      call matmult(s22,t,mm,nn,g)
      return
      end

```

Intg1

```

c      subroutine to calculate integral #1 - finite ground plane
      subroutine intg1(a1,a2,b1,b2,d,e,r)
      bb=(a1-a2)*cos(d)+(b1-b2)*sin(d)
      aa=(a1-a2)*sin(d)-(b1-b2)*cos(d)
      t2=e/2-bb
      t1=-1*e/2-bb
      if (aa.eq.0) then
        r=t2*alog(t2**2)-t1*alog(t1**2)-2*e
      else
        r=t2*alog(t2**2+aa**2)-t1*alog(t1**2+aa**2)-2*(t2-t1)
        $ +2*aa*(atan(t2/aa)-atan(t1/aa))
c      write(*,*) 'r=',r
c      pause 'hit enter to continue'
      endif
      return
      end

```

Int11

```

c      subroutine to calculate integral #1 for infinite ground plane
      suoroutine int11(a,b,c,d,e,l,r)
      real l
      a1=(a-b)*sin(e)+(c+d)*cos(e)
      a2=(a-b)*sin(e)-(c-d)*cos(e)
      b1=(a-b)*cos(e)-(c+d)*sin(e)
      b2=(a-b)*cos(e)+(c-d)*sin(e)
      t21=1/2-b1
      t11=-1/2-b1
      t22=1/2-b2
      t12=-1/2-b2
      if (a1.eq.0.0) then
        f1=t21*alog(t21**2)-t11*alog(t11**2)-2*l
      else
        f1=t21*alog(t21**2+a1**2)-t11*alog(t11**2+a1**2)-2*l
        $ +2*a1*(atan(t21/a1)-atan(t11/a1))
      endif

```

```

      if (a2.eq.0.0) then
        f2=t22*alog(t22**2)-t12*alog(t12**2)-2*1
      else
        f2=t22*alog(t22**2+a2**2)-t12*alog(t12**2+a2**2)-2*1
        $      +2*a2*(atan(t22/a2)-atan(t12/a2))
      endif
c      write(*,*) 'f1 and f2 =',f1,f2
      r=f1-f2
c      write(*,*) 'r=',r
      return
    end

```

Intg2

```

c      This subroutine calculates integral #2 for finite ground plane
      subroutine intg2(a1,a2,b1,b2,d1,d2,e,r)
      bb=(a1-a2)*cos(d1)+(b1-b2)*sin(d1)
      aa=(a1-a2)*sin(d1)-(b1-b2)*cos(d1)
      t2=e/2-bb
      t1=-1*e/2-bb
      if (aa.eq.0) then
        f2=(-1/t2+1/t1)
      else
        f2=(1/aa)*(atan(t2/aa)-atan(t1/aa))
      endif
      f3=(1/2)*(alog(t2**2+aa**2)-alog(t1**2+aa**2))
      if (sin(d2).eq.0) then
        r=(b1-b2-bb*sin(d1))*f2*sin(d1)*f3
      elseif (cos(d2).eq.0) then
        r=-1*((a1-a2-bb*cos(d1))*f2-cos(d1)*f3)
      else
        r=-1*sin(d2)*((a1-a2-bb*cos(d1))*f2-cos(d1)*f3)
        $ +cos(d2)*((b1-b2-bb*sin(d1))*f2-sin(d1)*f3)
      endif
      return
    end

```

Int22

```

c      subroutine to calculate integral for infinite ground plane
      subroutine int22(a,b,c,d,e,f,l,r1,r2)
      real l
      a1=(a-b)*sin(e)+(c+d)*cos(e)
      a2=(a-b)*sin(e)-(c+d)*cos(e)
      b1=(a-b)*cos(e)-(c+d)*sin(e)
      b2=(a-b)*cos(e)+(c+d)*sin(e)
      t21=1/2-b1
      t11=-1/2-b1
      t22=1/2-b2
      t12=-1/2-b2
      if (a1.eq.0.0) then
        f21=(-1/t21+1/t11)
      else
        f21=(1/a1)*(atan(t21/a1)-atan(t11/a1))
      endif
      f31=(1/2)*(alog(t21**2+a1**2)-alog(t11**2+a1**2))
      if (sin(f).eq.0.0) then
        r1=+1*((c+d+b1*sin(e))*f21+sin(e)*f31)
      elseif (cos(f).eq.0.0) then
        r1=-1*((a-b-b1*cos(e))*f21-cos(e)*f31)

```

```

else
r1=-sin(f)*((a-b-b1*cos(e))*f21-cos(e)*f31)+
$   cos(f)*((c+d+b1*sin(e))*f21+sin(e)*f31)
endif
if (a2.eq.0.0) then
f22=(-1/t22+1/t12)
else
f22=(1/a2)*(atan(t22/a2)-atan(t12/a2))
endif
f32=(1/2)*(alog(t22**2+a2**2)-alog(t12**2+a2**2))
if (sin(f).eq.0.0) then
r2=((c-d-b2*sin(e))*f22-sin(e)*f32)
elseif (cos(f).eq.0.0) then
r2=-1*((a-b-b2*cos(e))*f22-cos(e)*f32)
else
r2=-sin(f)*((a-b-b2*cos(e))*f22-cos(e)*f32)
$   +cos(f)*((c-d-b2*sin(e))*f22-sin(e)*f32)
endif
return
end

```

Inversel

```

c      Invert an n*n matrix
subroutine inversel(a,n,b)
dimension a(5,5),b(5,5)
integer check,ret,sin
assign 28 to sin
assign 200 to check
assign 250 to ret
do 20 i=1,n
do 10 j=1,n
if (i.eq.j) then
b(i,j)=1.0
else
b(i,j)=0.0
endif
10   continue
20   continue
do 60 j=1,n
do 25 i=j,n
if (a(i,j).ne.0.0) then
goto sin
endif
25   continue
goto check
28   do 30 k=1,n
s=a(j,k)
a(j,k)=a(i,k)
a(i,k)=s
s=b(j,k)
b(j,k)=b(i,k)
b(i,k)=s
30   continue
t=1/a(j,j)
do 40 k=1,n
a(j,k)=t*a(j,k)
b(j,k)=t*b(j,k)
40   continue
do 45 l=1,n
if (l.ne.j) then
t=-1*a(l,j)
do 43 k=1,n

```

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```

a(1,k)=a(1,k)+t*a(j,k)
b(1,k)=b(1,k)+t*b(j,k)
43 continue
endif
45 continue
60 continue
goto ret
200 write(*,210) ' array is singular'
210 format(a)
250 return
end

10 REM PROGRAM TO CALCULATE CAPACITANCE DATA
20 REM DIMENSION STATEMENTS
30 REM "end coordinates for conductor sections"
40 DIM CDX1(8,4), CDX2(8,4), CDY1(8,4), CDY2(8,4)
50 REM "end coordinates for dielectric interfaces"
60 DIM DIX1(12), DIX2(12), DIY1(12), DIY2(12)
70 REM determine whether conductor or dielectric interface is round or not
80 DIM GEOMC(8), GEOMD(12), ORIGXC(8), ORIGYC(8), ORIGXD(12), ORIGYD(12)
90 DIM RADC(8), RADD(12)
100 REM "number of conductor sections, conductor and dielectric subsections"
110 DIM S(8), NSSC(8,4), NSSD(12)
120 REM "length of conductor section or dielectric interface"
130 DIM CL(8,4), DL(12)
140 REM "conductor and dielectric subsection coordinates"
150 DIM CX1(8,4,10), CX2(8,4,10), CY1(8,4,10), CY2(8,4,10)
160 DIM DX1(12,25), DX2(12,25), DY1(12,25), DY2(12,25)
170 REM "dielectric constants"
180 DIM ERD2(12), ERD1(12), ERC2(8,4), ERC1(8,4)
190 REM "END OF DIMENSION PORTION OF PROGRAM"
200 REM
210 PRINT "This program calculates the capacitance for multiconductor"
220 PRINT "transmission line configurations. These transmission lines "
230 PRINT "are of rectangular crosssection and can be either infinitely"
240 PRINT "thin or a finite thickness. The use of either a finite ground "
250 PRINT "plane or an infinite one may be specified although this must "
260 PRINT "be specified at the outset since two different solution routines"
270 PRINT "are employed"
280 REM
290 REM
300 REM "BEGINNING OF DATA INPUT PORTION OF PROGRAM"
310 PRINT "If ground plane is finite type 1 if infinite type 0"
320 INPUT SOL
330 INPUT "Enter the number of conductors";NC
340 INPUT "enter number of ground conductors";NCC
350 REM "determine the number of sections per conductor"
360 FOR I=1 TO NC
370 PRINT "Enter the geometry for conductor ";I
380 INPUT "enter geometry code:1=rectangular,2=circular";GEOMC(I)
390 IF GEOMC(I)=2 THEN GOTO 590
400 PRINT "How many conductor sections for Conductor ";I
410 INPUT "Number of sections equals ";S(I)
420 IF S(I)=1 THEN GOTO 550
430 PRINT "enter 4 corner coordinates for conductor ";I
440 INPUT "x1,y1";CDX1(I,1),CDY1(I,1)
450 INPUT "x2,y2";CDX1(I,2),CDY1(I,2)
460 INPUT "x3,y3";CDX1(I,3),CDY1(I,3)
470 INPUT "x4,y4";CDX1(I,4),CDY1(I,4)
480 FOR J=1 TO 3
490 CDX2(I,J)=CDX1(I,J+1)
500 CDY2(I,J)=CDY1(I,J+1)
510 NEXT J
520 CDX2(I,4)=CDX1(I,1)
530 CDY2(I,4)=CDY1(I,1)

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540 GOTO 610
550 PRINT "enter endpoints for infinitely thin conductor segment number ";I
560 INPUT "x1,y1";CDX1(I,1),CDY1(I,1)
570 INPUT "x2,y2";CDX2(I,1),CDY2(I,1)
580 GOTO 610
590 INPUT "radius and origin of circle:r,x,y ";RADC(I),ORIGXC(I),ORIGYC(I)
600 S(I)=1
610 FOR J=1 TO S(I)
620 INPUT "relative dielectric constant 2 = "; ERC2(I,J)
630 INPUT "relative dielectric constant 1 = "; ERC1(I,J)
640 NEXT J
650 NEXT I
660 INPUT "enter the number of dielectric interfaces :ND
670 FOR I=1 TO ND
680 INPUT "enter initial coordinates, x1, y1"; DIX1(I), DIY1(I)
690 INPUT "enter final coordinates, x2,y2"; DIX2(I), DIY2(I)
700 INPUT "enter dielectric constant er2";ERD2(I)
710 INPUT "enter dielectric constant er1";ERD1(I)
720 NEXT I
730 INPUT "Enter scale factor for graphics (number between 1-10)";SF
740 REM
750 REM
760 REM
770 REM
780 REM
790 REM "GRAPHICS"
800 CLS
810 SCREEN 2
820 FOR I=1 TO NC
830 IF GEOMC(I)=2 THEN GOTO 880
840 FOR J=1 TO S(I)
850 LINE (1000*Sf*CDX1(I,J),100-1000*Sf*(20/48)*CDY1(I,J))-(1000*Sf*CDX2(I,J),10
0-1000*(20/48)*Sf*CDY2(I,J))
860 NEXT J
870 GOTO 890
880 CIRCLE (1000*Sf*ORIGXC(I),100-1000*Sf*(20/48)*ORIGYC(I)),1000*Sf*RADC(I)
890 NEXT I
900 FOR I=1 TO ND
910 LINE (1000*Sf*DIX1(I),100-1000*(20/48)*Sf*DIY1(I))-(1000*Sf*DIX2(I),100-1000
*(20/48)*Sf*DIY2(I))
920 NEXT I
930 IF SOL=0 THEN LINE (0,100)-(1679,100)
940 REM "the above generated line is not broken into subelements"
950 PRINT "this is your plot"
960 INPUT "to return to the program hit any key";ANS$
970 SCREEN 0
980 INPUT "Is this geometry correct?";ANS$
990 IF ANS$="no" THEN GOTO 500
1000 REM
1010 REM
1020 REM
1030 REM
1040 REM "Evaluate lengths for each section or interface"
1050 FOR I=1 TO NC
1060 IF GEOMC(I)=2 THEN GOTO 1100
1070 FOR J=1 TO S(I)
1080 CL(I,J)=SQR((CDX2(I,J)-CDX1(I,J))2+(CDY2(I,J)-CDY1(I,J))2)
1090 NEXT J
1100 NEXT I
1110 FOR I=1 TO ND
1120 DL(I)=SQR((DIX2(I)-DIX1(I))2+(DIY2(I)-DIY1(I))2)
1130 NEXT I
1140 REM
1150 REM "GENERATION OF SUBSECTION DATA"
1160 PRINT " Begin subdividing conductor sections and dielectric interfaces"
1170 FOR I=1 TO NC
1180 IF GEOMC(I)=2 THEN GOTO 1240

```

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```

1190 FOR J=1 TO S(I)
1200 PRINT "How many subsections for conductor ";I;" section ";J
1210 INPUT NSSC(I,J)
1220 NEXT J
1230 GOTO 1260
1240 PRINT "How many subsections for circular conductor ";I
1250 INPUT NSSC(I,1)
1260 NEXT I
1270 FOR I=1 TO ND
1280 PRINT "how many subsections for interface ";I
1290 INPUT NSSD(I)
1300 GOTO 1330
1310 REM "GENERATION OF FORTRAN DATA FILE"
1320 REM INPUT 'put data disk in drive b and hit any key to continue';ans%
1330 OPEN "B:data.fort" FOR OUTPUT AS #1
1340 REM "Calculate length,angle,coordinates for each subsection"
1350 WRITE #1,NC
1360 FOR I=1 TO NC
1370 WRITE #1,S(I)
1380 FOR J=1 TO S(I)
1390 WRITE #1,NSSC(I,J)
1391 IF GEOMC(I)=2 THEN GOTO 1800
1400 L=CL(I,J)/NSSC(I,J)
1410 FOR F=1 TO NSSC(I,J)
1420 IF (CDX2(I,J)-CDX1(I,J))=0 THEN GOTO 1460
1430 THETA = ATN((CDY2(I,J)-CDY1(I,J))/(CDX2(I,J)-CDX1(I,J)))
1440 IF (CDX2(I,J)-CDX1(I,J))=0 THEN THETA=THETA + 3.141592
1450 GOTO 1470
1460 IF (CDY2(I,J)-CDY1(I,J))=0 THEN THETA=-1.570796 ELSE THETA=1.570796
1470 X=CDX1(I,J)+(F*L-L/2)*COS(THETA)
1480 Y=CDY1(I,J)+(F*L-L/2)*SIN(THETA)
1490 WRITE #1,X,Y,THETA,L
1500 WRITE #1,ERC2(I,J),ERC1(I,J)
1510 NEXT F
1520 NEXT J
1530 NEXT I
1540 WRITE #1,NCC
1550 WRITE #1,ND
1560 FOR I=1 TO ND
1570 WRITE #1,NSSD(I)
1580 L=DL(I)/NSSD(I)
1590 FOR J=1 TO NSSD(I)
1600 IF (DIX2(I)-DIX1(I))=0 THEN GOTO 1640
1610 THETA=ATN((DIY2(I)-DIY1(I))/(DIX2(I)-DIX1(I)))
1620 IF (DIX2(I)-DIX1(I))=0 THEN THETA=THETA + 3.141592
1630 GOTO 1650
1640 IF (DIY2(I)-DIY1(I))=0 THEN THETA=-1.570796 ELSE THETA = 1.570796
1650 X=DIX1(I)+(J*L-L/2)*COS(THETA)
1660 Y=DIY1(I)+(J*L-L/2)*SIN(THETA)
1670 WRITE #1,X,Y,THETA,L
1680 WRITE #1,ERD2(I),ERD1(I)
1690 NEXT J
1700 NEXT I
1710 CLOSE
1720 GOTO 2000
1800 DEL=6.283185/NSSC(I,1)
1810 THETA=0
1815 RF=RADC(I)*COS(DEL/2)
1820 FOR M=1 TO NSSC(I,1)
1830 X=ORIG+RF+RF*SIN(THETA+DEL/2)
1840 Y=ORIG+RF+RF*COS(THETA+DEL/2)
1850 L=2*RADC(I)*SIN(DEL/2)
1855 ANGLE=PI+THETA+DEL/2
1860 WRITE #1,X,Y,ANGLE,L
1870 WRITE #1,ERC2(I,J),ERC1(I,J)
1875 THETA=THETA+DEL
1880 NEXT M
1890 GOTO 1920
1900 REM

```

APPENDIX B

The program MAINR is a special-purpose crosstalk analyzer for calculating near- and far-end crosstalk. The output data from this program are formatted to be used in conjunction with a plotting program such as LOTUS 123. The program is designed to be interactive. Input requirements include: the elements of the capacitance

and inductance matrixes; the eigenvectors and eigenvalues of Eqs. 53 or 54; the source and load resistances; the coupled line length; pulse rise (or fall) time; pulse width; pulse amplitude; voltage steps desired; delta t for the voltage plot; and the total number of time increments.

PROGRAM MAINR

```
c Program Mainr. Copyright The Johns Hopkins University/
c Applied Physics Laboratory, 1987
c Program for calculating crosstalk between 2 coupled lines
  dimension a(175),t(175),r(2,2),rs(2,2),ts(2,2),s(2,2),
  $ zc(2,2),v1(1000),v2(1000),v3(1000),v4(1000),
  $ c(1,2),cl(2,2),hss(2,2),sl(2,2),cl(2,2),d(2,2),e(2,2),f(2,2),
  $ v11(1000),v12(1000),v13(1000),v44(1000)
  real l(2,2),l1(2,2),lamsd(2,2)
1  input parameters
  write(*,*) 'enter c and d matrix elements'
  do 10 i=1,2
  do 10 j=1,2
    write(*,*) 'enter c(i,j)'
    read(*,*) c(i,j)
    write(*,*) 'enter d(i,j)'
    read(*,*) d(i,j)
  10 continue
20  continue
  write(*,*) 'enter smallest eigenvalue'
  read(*,*) alam1
  write(*,*) 'enter largest eigenvalue'
  read(*,*) alam2
  write(*,*) 'enter eigenvector matrix'
  do 20 i=1,2
  do 20 j=1,2
    write(*,*) 'enter v1(i,j)'
    read(*,*) v1(i,j)
  20 continue
25  continue
  call inverse(s,sl)
  write(*,*) 'enter source and load resistance matrix'
  do 30 i=1,2
  do 30 j=1,2
    write(*,*) 'enter source resistance r(i,j)'
    read(*,*) rs(i,j)
    write(*,*) 'enter load resistance l(i,j)'
    read(*,*) ls(i,j)
  30 continue
40  continue
  write(*,*) 'enter the coupled line length'
  read(*,*) al
  write(*,*) 'enter pulse risetime'
  read(*,*) tr
```

```

c      write(*,*) 'enter pulse falltime'
c      read(*,*) tf
c      write(*,*) 'enter pulse width'
c      read(*,*) pw
c      write(*,*) 'enter amplitude of pulse'
c      read(*,*) amp
c      write(*,*) 'enter the number of voltage steps'
c      read(*,*) nvs
c      write(*,*) 'enter the delta t for voltage plot'
c      read(*,*) delt
c      write(*,*) 'enter the total number of time increments'
c      read(*,*) nti
c      Calculate the impedance matrix
c      s(1,1)=.7071
c      s(1,2)=.7071
c      s(2,1)=-.7071
c      s(2,2)=.7071
c      si(1,1)=.7071
c      si(1,2)=-.7071
c      si(2,1)=.7071
c      si(2,2)=.7071
c      lamsq(1,1)=sqrt(alam1)
c      lamsq(1,2)=0.0
c      lamsq(2,1)=0.0
c      lamsq(2,2)=sqrt(alam2)
c      call inverse2(1,1i)
c      write(*,*) 'L inverse = ',li(1,1),li(1,2),li(2,2)
c      pause 'hit any key to return'
c      call matmul(li,lamsq,2,2,2,d)
c      write(*,*) 'li x lamsq = ',d(1,1),d(1,2),d(2,2)
c      pause 'hit any key to return'
c      call matmul(d,s,2,2,2,e)
c      write(*,*) 'li x lamsq x s = ',e(1,1),e(1,2),e(2,2)
c      pause 'hit any key to return'
c      call inverse2(e,d)
c      write(*,*) 'inverse = ', d(1,1),d(1,2),d(2,2)
c      pause 'hit any key to return'
c      call matmul(s,d,2,2,2,zc)
c      write(*,*) 'zc = ',zc(1,1),zc(1,2),zc(2,2)
c      pause 'hit any key to return'
c      calculate r and rs matrix
c      call matadd(rss,zc,2,d)
c      call matsub(rss,zr,2,e)
c      call inverse2(d,f)
c      call matmul(zc,f,2,2,2,d)
c      call matmul(si,d,2,2,2,ts)
c      write(*,*) 'ts = ',ts(1,1),ts(1,2),ts(2,1),ts(2,2)
c      pause 'hit enter to return'
c      call matmul(e,f,2,2,2,d)
c      call matmul(si,d,2,2,2,e)
c      call matmul(e,s,2,2,2,rs)
c      write(*,*) 'rs = ',rs(1,1),rs(1,2),rs(2,1),rs(2,2)
c      pause 'hit enter to return'
c      call matadd(r1,zc,2,d)
c      call matsub(r1,zc,2,e)
c      call inverse2(d,f)
c      call matmul(e,f,2,2,2,d)
c      call matmul(si,d,2,2,2,f)
c      call matmul(f,s,2,2,2,r)
c      write(*,*) 'r = ',r(1,1),r(1,2),r(2,1),r(2,2)
c      pause 'hit enter to return'
c      calculate the reflection coefficients
c      calculate time delays
c      td1=sqrt(alam1)*al
c      td2=sqrt(alam2)*al
c      write(*,*) 'td1 and td2 = ',td1,td2

```

```

      pause 'hit any key to return'
      call coeff(a,t,td1,td2,r,rs,ts)
c calculate the voltage pulse from input data
      nvs=tr/delt
      v0=amp/nvs
      ttt=0.0
      do 200 i=0,nvs-1
        time=ttt
        do 100 j=i+1,nti
          v=0.0
          call vone(time,v,a,t,i,delt,v0)
          v1(j)=v1(j)+v
          v=0.0
          call vtwo(time,v,a,t,i,delt,v0)
          v2(j)=v2(j)+v
          v=0.0
          call vthree(time,v,a,t,i,delt,v0)
          v3(j)=v3(j)+v
          v=0.0
          call vfour(time,v,a,t,i,delt,v0)
          v4(j)=v4(j)+v
        time=time+delt
100      continue
        ttt=ttt+delt
200      continue
c Convert mode voltages to real voltages
      do 250 i=1,nti
        v11(i)=s(1,1)*v1(i)+s(1,2)*v3(i)
        v33(i)=s(2,1)*v1(i)+s(2,2)*v3(i)
        v22(i)=s(1,1)*v2(i)+s(1,2)*v4(i)
        v44(i)=s(2,1)*v2(i)+s(2,2)*v4(i)
250      continue
c Store voltage data
      open(7,file='b:data.for',form='formatted')
c      write(7,*) nti
c      do 270 i=1,2
c        do 260 j=1,2
c          write(7,*) 'zc ',i,j,' = ',zc(i,j)
c260      continue
c270      continue
c        do 275 i=1,132
c          write(7,*) 'a ',i,' = ',a(i)
c275      continue
      tt=0.0
      do 300 i=1,nti
        write(7,*) tt,v11(i),v22(i),v33(i),v44(i)
c      write(7,*) tt
      tt=tt+(delt)*(1.0e+9)
300      continue
      close(7,status='keep')
      stop
      end

```

```

if (time.ge. (t(39)+i*delt)) v1=v1+(a(14)+a(39))*v0
if (time.ge. (t(46)+i*delt)) v1=v1+a(46)*v0
if (time.ge. (t(47)+i*delt)) v1=v1+(a(23)+a(47))*v0
if (time.ge. (t(50)+i*delt)) v1=v1+a(50)*v0
if (time.ge. (t(59)+i*delt)) v1=v1+(a(29)+a(59))*v0
if (time.ge. (t(62)+i*delt)) v1=v1+a(62)*v0
if (time.ge. (t(70)+i*delt)) v1=v1+a(70)*v0
if (time.ge. (t(71)+i*delt)) v1=v1+(a(65)+a(71))*v0
if (time.ge. (t(74)+i*delt)) v1=v1+a(74)*v0
if (time.ge. (t(83)+i*delt)) v1=v1+(a(56)+a(83))*v0
if (time.ge. (t(85)+i*delt)) v1=v1+(a(57)+a(85))*v0
if (time.ge. (t(88)+i*delt)) v1=v1+a(88)*v0
if (time.ge. (t(91)+i*delt)) v1=v1+(a(33)+a(91))*v0
if (time.ge. (t(94)+i*delt)) v1=v1+a(94)*v0
if (time.ge. (t(96)+i*delt)) v1=v1+a(96)*v0
if (time.ge. (t(97)+i*delt)) v1=v1+(a(36)+a(97))*v0
if (time.ge. (t(99)+i*delt)) v1=v1+(a(37)+a(99))*v0
if (time.ge. (t(102)+i*delt)) v1=v1+a(102)*v0
if (time.ge. (t(108)+i*delt)) v1=v1+a(108)*v0
if (time.ge. (t(109)+i*delt)) v1=v1+(a(109)+a(42))*v0
if (time.ge. (t(112)+i*delt)) v1=v1+a(112)*v0
if (time.ge. (t(113)+i*delt)) v1=v1+(a(44)+a(113))*v0
if (time.ge. (t(124)+i*delt)) v1=v1+a(124)*v0
if (time.ge. (t(125)+i*delt)) v1=v1+(a(52)+a(125))*v0
if (time.ge. (t(127)+i*delt)) v1=v1+(a(53)+a(127))*v0
if (time.ge. (t(130)+i*delt)) v1=v1+a(130)*v0
if (time.ge. (t(132)+i*delt)) v1=v1+a(132)*v0
if (time.ge. (t(135)+i*delt)) v1=v1+(a(76)+a(135))*v0
if (time.ge. (t(139)+i*delt)) v1=v1+(a(139)+a(79))*v0
if (time.ge. (t(142)+i*delt)) v1=v1+a(142)*v0
if (time.ge. (t(144)+i*delt)) v1=v1+a(144)*v0
if (time.ge. (t(145)+i*delt)) v1=v1+(a(145)+a(76))*v0
if (time.ge. (t(150)+i*delt)) v1=v1+a(150)*v0
if (time.ge. (t(151)+i*delt)) v1=v1+(a(151)+a(103))*v0
return
end

```

Vthree

c Subroutine Vthree. copyright The Johns Hopkins University/
 c Applied Physics Laboratory, 1987

```

subroutine vthree(time,v1,a,t,i,delt,v0)
dimension a(175),t(175)
v1=a(2)*v0
if (time.ge. (t(8)+i*delt)) v1=v1+a(8)*v0
if (time.ge. (t(9)+i*delt)) v1=v1+(a(4)+a(9))*v0
if (time.ge. (t(12)+i*delt)) v1=v1+a(12)*v0
if (time.ge. (t(13)+i*delt)) v1=v1+(a(5)+a(13))*v0
if (time.ge. (t(24)+i*delt)) v1=v1+a(24)*v0
if (time.ge. (t(30)+i*delt)) v1=v1+a(30)*v0
if (time.ge. (t(34)+i*delt)) v1=v1+a(34)*v0
if (time.ge. (t(35)+i*delt)) v1=v1+(a(16)+a(35))*v0
if (time.ge. (t(38)+i*delt)) v1=v1+a(38)*v0
if (time.ge. (t(41)+i*delt)) v1=v1+(a(18)+a(41))*v0
if (time.ge. (t(43)+i*delt)) v1=v1+(a(19)+a(43))*v0
if (time.ge. (t(51)+i*delt)) v1=v1+(a(25)+a(51))*v0
if (time.ge. (t(54)+i*delt)) v1=v1+a(54)*v0
if (time.ge. (t(55)+i*delt)) v1=v1+(a(27)+a(55))*v0
if (time.ge. (t(58)+i*delt)) v1=v1+a(58)*v0
if (time.ge. (t(63)+i*delt)) v1=v1+(a(31)+a(63))*v0
if (time.ge. (t(66)+i*delt)) v1=v1+a(66)*v0
if (time.ge. (t(67)+i*delt)) v1=v1+(a(48)+a(67))*v0
if (time.ge. (t(75)+i*delt)) v1=v1+(a(69)+a(75))*v0

```

SUBROUTINES

Vone

```
c Subroutine Vone. copyright The Johns Hopkins University/
c Applied Physics Laboratory, 1987
subroutine vone(time,v1,a,t,i,delt,v0)
dimension a(175),t(175)
v1=a(1)*v0
if (time.ge.(t(7)+i*delt)) v1=v1+(a(7)+a(3))*v0
if (time.ge.(t(10)+i*delt)) v1=v1+a(10)*v0
if (time.ge.(t(11)+i*delt)) v1=v1+(a(6)+a(11))*v0
if (time.ge.(t(14)+i*delt)) v1=v1+a(14)*v0
if (time.ge.(t(23)+i*delt)) v1=v1+(a(23)+a(15))*v0
if (time.ge.(t(29)+i*delt)) v1=v1+(a(29)+a(21))*v0
if (time.ge.(t(33)+i*delt)) v1=v1+(a(20)+a(33))*v0
if (time.ge.(t(36)+i*delt)) v1=v1+a(36)*v0
if (time.ge.(t(37)+i*delt)) v1=v1+(a(17)+a(37))*v0
if (time.ge.(t(42)+i*delt)) v1=v1+a(42)*v0
if (time.ge.(t(44)+i*delt)) v1=v1+a(44)*v0
if (time.ge.(t(52)+i*delt)) v1=v1+a(52)*v0
if (time.ge.(t(53)+i*delt)) v1=v1+(a(26)+a(53))*v0
if (time.ge.(t(56)+i*delt)) v1=v1+a(56)*v0
if (time.ge.(t(57)+i*delt)) v1=v1+(a(28)+a(57))*v0
if (time.ge.(t(64)+i*delt)) v1=v1+a(64)*v0
if (time.ge.(t(65)+i*delt)) v1=v1+(a(47)+a(65))*v0
if (time.ge.(t(66)+i*delt)) v1=v1+a(68)*v0
if (time.ge.(t(76)+i*delt)) v1=v1+a(76)*v0
if (time.ge.(t(77)+i*delt)) v1=v1+(a(70)+a(77))*v0
if (time.ge.(t(79)+i*delt)) v1=v1+(a(71)+a(79))*v0
if (time.ge.(t(82)+i*delt)) v1=v1+a(82)*v0
if (time.ge.(t(89)+i*delt)) v1=v1+(a(32)+a(89))*v0
if (time.ge.(t(103)+i*delt)) v1=v1+(a(39)+a(103))*v0
if (time.ge.(t(106)+i*delt)) v1=v1+a(106)*v0
if (time.ge.(t(116)+i*delt)) v1=v1+a(116)*v0
if (time.ge.(t(117)+i*delt)) v1=v1+(a(46)+a(117))*v0
if (time.ge.(t(120)+i*delt)) v1=v1+a(120)*v0
if (time.ge.(t(121)+i*delt)) v1=v1+(a(50)+a(121))*v0
if (time.ge.(t(134)+i*delt)) v1=v1+a(134)*v0
if (time.ge.(t(138)+i*delt)) v1=v1+a(138)*v0
if (time.ge.(t(148)+i*delt)) v1=v1+a(148)*v0
return
end
```

Vtwo

```
c Subroutine Vtwo. copyright The Johns Hopkins University/
c Applied Physics Laboratory, 1987
subroutine vtwo(time,v1,a,t,i,delt,v0)
dimension a(175),t(175)
v1=0.0
if (time.ge.(t(3)+i*delt)) v1=v1+(a(3)+a(1))*v0
if (time.ge.(t(6)+i*delt)) v1=v1+a(6)*v0
if (time.ge.(t(15)+i*delt)) v1=v1+(a(7)+a(15))*v0
if (time.ge.(t(17)+i*delt)) v1=v1+(a(11)+a(17))*v0
if (time.ge.(t(20)+i*delt)) v1=v1+a(20)*v0
if (time.ge.(t(21)+i*delt)) v1=v1+(a(10)+a(21))*v0
if (time.ge.(t(26)+i*delt)) v1=v1+a(26)*v0
if (time.ge.(t(28)+i*delt)) v1=v1+a(28)*v0
if (time.ge.(t(32)+i*delt)) v1=v1+a(32)*v0
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if (time.ge.(t(78)+i*delt)) v1=v1+a(78)*v0
if (time.ge.(t(80)+i*delt)) v1=v1+a(80)*v0
if (time.ge.(t(81)+i*delt)) v1=v1+(a(73)+a(81))*v0
if (time.ge.(t(90)+i*delt)) v1=v1+a(90)*v0
if (time.ge.(t(104)+i*delt)) v1=v1+a(104)*v0
if (time.ge.(t(105)+i*delt)) v1=v1+(a(40)+a(105))*v0
if (time.ge.(t(115)+i*delt)) v1=v1+(a(45)+a(115))*v0
if (time.ge.(t(118)+i*delt)) v1=v1+a(118)*v0
if (time.ge.(t(119)+i*delt)) v1=v1+(a(49)+a(119))*v0
if (time.ge.(t(133)+i*delt)) v1=v1+(a(133)+a(111))*v0
if (time.ge.(t(137)+i*delt)) v1=v1+(a(137)+a(72))*v0
if (time.ge.(t(147)+i*delt)) v1=v1+(a(147)+a(143))*v0
return
end

```

Vfour

Subroutine Vfour. copyright The Johns Hopkins University/
 © Applied Physics Laboratory. 1987

```

subroutine vfour(time,v1,a,t,i,delt,v0)
dimension a(175),t(175)
v1=0.0
if (time.ge.(t(4)+i*delt)) v1=v1+a(4)*v0
if (time.ge.(t(5)+i*delt)) v1=v1+(a(2)+a(5))*v0
if (time.ge.(t(16)+i*delt)) v1=v1+a(16)*v0
if (time.ge.(t(18)+i*delt)) v1=v1+a(18)*v0
if (time.ge.(t(19)+i*delt)) v1=v1+(a(8)+a(19))*v0
if (time.ge.(t(22)+i*delt)) v1=v1+a(22)*v0
if (time.ge.(t(25)+i*delt)) v1=v1+(a(9)+a(25))*v0
if (time.ge.(t(27)+i*delt)) v1=v1+(a(12)+a(27))*v0
if (time.ge.(t(31)+i*delt)) v1=v1+(a(13)+a(31))*v0
if (time.ge.(t(40)+i*delt)) v1=v1+a(40)*v0
if (time.ge.(t(45)+i*delt)) v1=v1+(a(22)+a(45))*v0
if (time.ge.(t(48)+i*delt)) v1=v1+a(48)*v0
if (time.ge.(t(49)+i*delt)) v1=v1+(a(24)+a(49))*v0
if (time.ge.(t(60)+i*delt)) v1=v1+a(60)*v0
if (time.ge.(t(61)+i*delt)) v1=v1+(a(30)+a(61))*v0
if (time.ge.(t(69)+i*delt)) v1=v1+(a(63)+a(69))*v0
if (time.ge.(t(72)+i*delt)) v1=v1+a(72)*v0
if (time.ge.(t(73)+i*delt)) v1=v1+(a(66)+a(73))*v0
if (time.ge.(t(84)+i*delt)) v1=v1+a(84)*v0
if (time.ge.(t(86)+i*delt)) v1=v1+a(86)*v0
if (time.ge.(t(87)+i*delt)) v1=v1+(a(58)+a(87))*v0
if (time.ge.(t(92)+i*delt)) v1=v1+a(92)*v0
if (time.ge.(t(93)+i*delt)) v1=v1+(a(34)+a(93))*v0
if (time.ge.(t(95)+i*delt)) v1=v1+(a(35)+a(95))*v0
if (time.ge.(t(98)+i*delt)) v1=v1+a(98)*v0
if (time.ge.(t(100)+i*delt)) v1=v1+a(100)*v0
if (time.ge.(t(101)+i*delt)) v1=v1+(a(101)+a(38))*v0
if (time.ge.(t(107)+i*delt)) v1=v1+(a(107)+a(41))*v0
if (time.ge.(t(110)+i*delt)) v1=v1+a(110)*v0
if (time.ge.(t(111)+i*delt)) v1=v1+(a(111)+a(43))*v0
if (time.ge.(t(114)+i*delt)) v1=v1+a(114)*v0
if (time.ge.(t(123)+i*delt)) v1=v1+(a(123)+a(51))*v0
if (time.ge.(t(126)+i*delt)) v1=v1+a(126)*v0
if (time.ge.(t(128)+i*delt)) v1=v1+a(128)*v0
if (time.ge.(t(129)+i*delt)) v1=v1+(a(129)+a(54))*v0
if (time.ge.(t(131)+i*delt)) v1=v1+(a(131)+a(55))*v0
if (time.ge.(t(136)+i*delt)) v1=v1+a(136)*v0
if (time.ge.(t(140)+i*delt)) v1=v1+a(140)*v0
if (time.ge.(t(141)+i*delt)) v1=v1+(a(141)+a(80))*v0
if (time.ge.(t(143)+i*delt)) v1=v1+(a(143)+a(75))*v0
if (time.ge.(t(146)+i*delt)) v1=v1+a(146)*v0

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if (time.ge.(t(149)+i*delt)) v1=v1+(a(149)+a(147))*v0
if (time.ge.(t(152)+i*delt)) v1=v1+a(152)*v0
return
end

```

Coeff

c Subroutine Coeff. copyright The Johns Hopkins University/
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```

subroutine coeff(a,t,td1,td2,r,rs,ts)
dimension a(175),t(175),r(2,2),rs(2,2),ts(2,2)
a(1)=ts(1,1)
a(2)=ts(2,1)
a(3)=r(1,1)*a(1)
a(4)=r(2,1)*a(1)
a(5)=r(2,2)*a(2)
a(6)=r(1,2)*a(2)
t(3)=td1
t(4)=td1
t(5)=td2
t(6)=td2
a(7)=rs(1,1)*a(3)
a(8)=rs(2,1)*a(3)
t(7)=2*td1
t(8)=2*td1
a(9)=rs(2,2)*a(4)
a(10)=rs(1,2)*a(4)
t(9)=td1+td2
t(10)=td1+td2
a(11)=rs(1,1)*a(6)
a(12)=rs(2,1)*a(6)
t(11)=td1+td2
t(12)=td1+td2
a(13)=rs(2,2)*a(5)
a(14)=rs(1,2)*a(5)
t(13)=2*td2
t(14)=2*td2
a(15)=r(1,1)*a(7)
a(16)=r(2,1)*a(7)
t(15)=3*td1
t(16)=3*td1
a(17)=r(1,1)*a(11)
a(18)=r(2,1)*a(11)
t(17)=2*td1+td2
t(18)=2*td1+td2
a(19)=r(2,2)*a(8)
a(20)=r(1,2)*a(8)
t(19)=2*td1+td2
t(20)=2*td1+td2
a(21)=r(1,1)*a(10)
a(22)=r(2,1)*a(10)
t(21)=2*td1+td2
t(22)=2*td1+td2
a(23)=rs(1,1)*a(15)
a(24)=rs(2,1)*a(15)
t(23)=4*td1
t(24)=4*td1
a(25)=r(2,2)*a(9)
a(26)=r(1,2)*a(9)
t(25)=td1+2*td2
t(26)=td1+2*td2
a(27)=r(2,2)*a(12)
a(28)=r(1,2)*a(12)
t(27)=td1+2*td2

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t(28)=td1+2*td2
a(29)=rs(1,1)*a(21)
a(30)=rs(2,1)*a(21)
t(29)=3*td1+td2
t(30)=3*td1+td2
a(31)=r(2,2)*a(13)
a(32)=r(1,2)*a(13)
t(31)=3*td2
t(32)=3*td2
a(33)=rs(1,1)*a(20)
a(34)=rs(2,1)*a(20)
t(33)=3*td1+td2
t(34)=3*td1+td2
a(35)=rs(2,2)*a(16)
a(36)=rs(1,2)*a(16)
t(35)=3*td1+td2
t(36)=3*td1+td2
a(37)=rs(1,1)*a(17)
a(38)=rs(2,1)*a(17)
t(37)=3*td1+td2
t(38)=3*td1+td2
a(39)=r(1,1)*a(14)
a(40)=r(2,1)*a(14)
t(39)=td1+2*td2
t(40)=td1+2*td2
a(41)=rs(2,2)*a(18)
a(42)=rs(1,2)*a(18)
t(41)=2*td1+2*td2
t(42)=2*td1+2*td2
a(43)=rs(2,2)*a(19)
a(44)=rs(1,2)*a(19)
t(43)=2*td1+2*td2
t(44)=2*td1+2*td2
a(45)=r(2,2)*a(22)
a(46)=r(1,2)*a(22)
t(45)=2*td1+2*td2
t(46)=2*td1+2*td2
a(47)=r(1,1)*a(23)
a(48)=r(2,1)*a(23)
t(47)=5*td1
t(48)=5*td1
a(49)=r(2,2)*a(24)
a(50)=r(1,2)*a(24)
t(49)=4*td1+td2
t(50)=4*td1+td2
a(51)=rs(2,2)*a(25)
a(52)=rs(1,2)*a(25)
t(51)=td1+3*td2
t(52)=td1+3*td2
a(53)=rs(1,1)*a(26)
a(54)=rs(2,1)*a(26)
t(53)=2*td1+2*td2
t(54)=2*td1+2*td2
a(55)=rs(2,2)*a(27)
a(56)=rs(1,2)*a(27)
t(55)=td1+3*td2
t(56)=td1+3*td2
a(57)=rs(1,1)*a(28)
a(58)=rs(2,1)*a(28)
t(57)=2*td1+2*td2
t(58)=2*td1+2*td2
a(59)=r(1,1)*a(29)
a(60)=r(2,1)*a(29)
t(59)=4*td1+td2
t(60)=4*td1+td2
a(61)=r(2,2)*a(70)

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a(62)=r(1,2)*a(30)
t(61)=3*td1+2*td2
t(62)=3*td1+2*td2
a(63)=rs(2,2)*a(31)
a(64)=rs(1,2)*a(31)
t(63)=4*td2
t(64)=4*td2
a(65)=rs(1,1)*a(47)
a(66)=rs(2,1)*a(47)
t(65)=6*td1
t(66)=6*td1
a(67)=rs(2,2)*a(48)
a(68)=rs(1,2)*a(48)
t(67)=5*td1+td2
t(68)=5*td1+td2
a(69)=r(2,2)*a(63)
a(70)=r(1,2)*a(63)
t(69)=5*td2
t(70)=5*td2
a(71)=r(1,1)*a(65)
a(72)=r(2,1)*a(65)
t(71)=7*td1
t(72)=7*td1
a(73)=r(2,2)*a(66)
a(74)=r(1,2)*a(66)
t(73)=6*td1+td2
t(74)=6*td1+td2
a(75)=rs(2,2)*a(69)
a(76)=rs(1,2)*a(69)
t(75)=6*td2
t(76)=6*td2
a(77)=rs(1,1)*a(70)
a(78)=rs(2,1)*a(70)
t(77)=td1+5*td2
t(78)=td1+5*td2
a(79)=rs(1,1)*a(71)
a(80)=rs(2,1)*a(71)
t(79)=8*td1
t(80)=8*td1
a(81)=rs(2,2)*a(73)
a(82)=rs(1,2)*a(73)
t(81)=6*td1+2*td2
t(82)=6*td1+2*td2
a(83)=r(1,1)*a(56)
a(84)=r(2,1)*a(56)
t(83)=2*td1+3*td2
t(84)=2*td1+3*td2
a(85)=r(1,1)*a(57)
a(86)=r(2,1)*a(57)
t(85)=3*td1+2*td2
t(86)=3*td1+2*td2
a(87)=r(2,2)*a(58)
a(88)=r(1,2)*a(58)
t(87)=2*td1+3*td2
t(88)=2*td1+3*td2
a(89)=rs(1,1)*a(32)
a(90)=rs(2,1)*a(32)
t(89)=td1+3*td2
t(90)=td1+3*td2
a(91)=r(1,1)*a(33)
a(92)=r(2,1)*a(33)
t(91)=4*td1+td2
t(92)=4*td1+td2
a(93)=r(2,2)*a(74)
a(94)=r(1,2)*a(74)
t(93)=3*td1+2*td2

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t(94)=3*td1+2*td2
a(95)=r(2,2)*a(35)
a(96)=r(1,2)*a(35)
t(95)=3*td1+2*td2
t(96)=3*td1+2*td2
a(97)=r(1,1)*a(36)
a(98)=r(2,1)*a(36)
t(97)=4*td1+td2
t(98)=4*td1+td2
a(99)=r(1,1)*a(37)
a(100)=r(2,1)*a(37)
t(99)=4*td1+td2
t(100)=4*td1+td2
a(101)=r(2,2)*a(38)
a(102)=r(1,2)*a(38)
t(101)=3*td1+2*td2
t(102)=3*td1+2*td2
a(103)=rs(1,1)*a(39)
a(104)=rs(2,1)*a(39)
t(103)=2*td1+3*td2
t(104)=2*td1+3*td2
a(105)=rs(2,2)*a(40)
a(106)=rs(1,2)*a(40)
t(105)=td1+3*td2
t(106)=td1+3*td2
a(107)=r(2,2)*a(41)
a(108)=r(1,2)*a(41)
t(107)=2*td1+3*td2
t(108)=2*td1+3*td2
a(109)=r(1,1)*a(42)
a(110)=r(2,1)*a(42)
t(109)=3*td1+2*td2
t(110)=3*td1+2*td2
a(111)=r(2,2)*a(43)
a(112)=r(1,2)*a(43)
t(111)=2*td1+3*td2
t(112)=2*td1+3*td2
a(113)=r(1,1)*a(44)
a(114)=r(2,1)*a(44)
t(113)=3*td1+2*td2
t(114)=3*td1+2*td2
a(115)=rs(2,2)*a(45)
a(116)=rs(1,2)*a(45)
t(115)=2*td1+3*td2
t(116)=2*td1+3*td2
a(117)=rs(1,1)*a(46)
a(118)=rs(2,1)*a(46)
t(117)=3*td1+2*td2
t(118)=3*td1+2*td2
a(119)=rs(2,2)*a(49)
a(120)=rs(1,2)*a(49)
t(119)=4*td1+2*td2
t(120)=4*td1+2*td2
a(121)=rs(1,1)*a(50)
a(122)=rs(2,1)*a(50)
t(121)=3*td1+2*td2
t(122)=3*td1+2*td2
a(123)=r(2,2)*a(51)
a(124)=r(1,2)*a(51)
t(123)=td1+4*td2
t(124)=td1+4*td2
a(125)=r(1,1)*a(52)
a(126)=r(2,1)*a(52)
t(125)=2*td1+3*td2
t(126)=2*td1+3*td2
a(127)=r(1,1)*a(53)

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a(128)=r(2,1)*a(53)
t(127)=3*td1+2*td2
t(128)=3*td1+2*td2
a(129)=r(2,2)*a(54)
a(130)=r(1,2)*a(54)
t(129)=2*td1+3*td2
t(130)=2*td1+3*td2
a(131)=r(2,2)*a(55)
a(132)=r(1,2)*a(55)
t(131)=td1+4*td2
t(132)=td1+4*td2
a(133)=rs(2,2)*a(111)
a(134)=rs(1,2)*a(111)
t(133)=2*td1+4*td2
t(134)=2*td1+4*td2
a(135)=r(1,1)*a(76)
a(136)=r(2,1)*a(76)
t(135)=td1+6*td2
t(136)=td1+6*td2
a(137)=rs(2,2)*a(72)
a(138)=rs(1,2)*a(72)
t(137)=7*td1+td2
t(138)=7*td1+td2
a(139)=r(1,1)*a(79)
a(140)=r(2,1)*a(79)
t(139)=9*td1
t(140)=9*td1
a(141)=r(2,2)*a(80)
a(142)=r(1,2)*a(80)
t(141)=8*td1+td2
t(142)=8*td1+td2
a(143)=r(2,2)*a(75)
a(144)=r(1,2)*a(75)
t(143)=7*td2
t(144)=7*td2
a(145)=r(1,1)*a(76)
a(146)=r(2,1)*a(76)
t(145)=td1+7*td2
t(146)=td1+7*td2
a(147)=rs(2,2)*a(143)
a(148)=rs(1,2)*a(143)
t(147)=8*td2
t(148)=8*td2
a(149)=r(2,2)*a(147)
a(150)=r(1,2)*a(147)
t(149)=9*td2
t(150)=9*td2
a(151)=r(1,1)*a(103)
a(152)=r(2,1)*a(103)
t(151)=3*td1+2*td2
t(152)=3*td1+2*td2
return
end

```

Inverse2

```

subroutine inverse2(a,b)
dimension a(2,2),b(2,2)
det= a(2,2)*a(1,1)-a(1,2)*a(2,1)
b(1,1)=a(2,2)/det
b(1,2)=-a(1,2)/det
b(2,1)=-a(2,1)/det
b(2,2)=a(1,1)/det
return
end

```

Matmul

```
subroutine matmul(a,b,m,l,n,c)
dimension a(2,2),b(2,2),c(2,2)
do 30 i=1,m
do 20 j=1,n
c(i,j)=0.0
do 10 k=1,l
c(i,j)=c(i,j)+a(i,k)*b(k,j)
10 continue
20 continue
30 continue
return
end
```

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