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STANFORD ELECTRONICS LABORATORIES
DEPARTMENT OF ELECTRICAL ENGINEERING
STANFORD UNIVERSITY · STANFORD, CA 94305

JSEP ANNUAL REPORT

1 May, 1986 through 30 April, 1987

James S. Harris, Jr.
JSEP Principal Investigator
and Program Director

(415) 723-9775

This work was supported by the
Joint Services Electronics Program
(U.S. Army, U.S. Navy and U.S. Air Force)
Contract DAAG29-85-K-0048,
and was monitored by the
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Abstract

This is the final report of the research conducted at the Stanford Electronics Laboratories under the sponsorship of the Joint Services Electronics Program from 1 May, 1986 through 30 April, 1987. This report summarizes the areas of research, identifies the most significant results, and lists the dissertations and publications sponsored by the contract (DAAG29-85-K-0048).

Key Words and Phrases: None.

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This work was supported by the Joint Services Electronic Program, contract DAAG-29-85-K-0048.

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JSEP ANNUAL REPORT
April 1, 1986 - March 31, 1987

INTRODUCTION

The JSEP contract supports a program of unclassified basic research in electronics conducted by faculty members of the Electrical Engineering Department of Stanford University as a component of the research program of the Stanford Electronics Laboratories. The Stanford Electronics Lab JSEP Director and Principal Investigator is Professor James Harris. He is responsible for the selection of the best individual proposals, coordination between Stanford and the JSEP TCC and coordination between the selected areas of the JSEP Program. In planning the JSEP Program at SEL, a general objective is to develop new projects with 3-6 years of JSEP sponsorship, leading to transition to DoD or other agency program funding. This report covers the second year of our current 3 year cycle. At the start of this year, the projects remained those defined in our proposal and continued from the first year since that proposal represented a considerable reorganization from the prior program. Early in the year, we started two new projects supporting newly appointed faculty, John Cioffi and Bruce Wooley. Near the end of this year, the discovery of the high T_c superconductors provided an opportunity to quickly fund several new projects in this area long before more conventional sources of research funding could respond to this opportunity. Approximately one third of the JSEP funds were switched into this area by the end of the current year and produced significant results within the first two months.

Three program highlights achieved during the past year are summarized below. Following these highlights, the specific objectives and progress in each work unit are reported.

The focus of the JSEP project on transport properties of 1-dimensional semiconductor structures was changed when the new high temperature superconductors were discovered because it was a natural extension of this work. We initiated growth of these materials by MBE in collaboration with researchers at Varian Associates. We have used effusion cells to obtain molecular beams

of the metals and a simple gaseous oxygen source. This approach yielded thin films of the superconductor, $\text{DyBa}_2\text{Cu}_3\text{O}_{7-x}$ grown on SrTiO_3 substrates. After a post growth oxygen anneal and solid phase epitaxy, the films exhibit sharp superconducting transitions with zero resistance observed as high as 87°K . Critical current densities of $4.8 \times 10^5 \text{ A/cm}^2$ at 4.2°K and $3.9 \times 10^4 \text{ A/cm}^2$ at 77°K have been measured. These are among the highest critical current densities for these materials. We are now developing an ionized oxygen source to realize true epitaxy of the superconductors such that no oxygen anneal is required.

The overall objective of the low temperature IC project has been to evaluate both MOS and bipolar device structures and interconnect metalization at 77°K to determine the potential of this technology for VLSI circuits. The principal benefit of 77°K circuit operation is enhanced performance due to both an increase in MOSFET drive current and a decrease in source/drain junction capacitance. Speed improvements in VLSI CMOS circuits operated at 77°K have been consistently less than expected. In an effort to understand these results a model has been developed to predict the propagation delay of an interconnect driven by cascaded drivers. The results of this investigation indicate that the driver resistance, rather than the interconnect resistance itself, limits performance. The use of bipolar transistors could greatly impact this problem in a low temperature BiCMOS approach. Bipolar transistors have traditionally been considered not useful at low temperatures. We have investigated bipolar structures and conclude that trap levels in the silicon bandgap determine bipolar transistor base currents at low temperatures. Bipolar transistors designed specifically for operation at 77°K were fabricated and showed very little current degradation between room temperature and 77°K . This approach may yield a much higher speed Si VLSI technology.

Since the early sixties, there has been considerable activity in the development of adaptive arrays for radar, sonar, communication, spectral estimation, etc. A key assumption in all previous work on adaptive beamforming is that the interfering signals are not coherent with the desired signal (i.e., one is not a scaled and delayed replica of the other). Coherence can completely destroy performance

of an adaptive array system, and is particularly serious when 'smart' jammers deliberately introduce coherent interference. A new processing scheme has been developed that retains its high resolution performance, regardless of the coherence of the sources. The robustness to the coherence of the sources is achieved by spatial-smoothing. We have also introduced a new adaptive beamformer which is able to work well even when the desired signal and the interference are coherent. The new adaptive processor uses both spatial and temporal sampled data to overcome the degradation of performance in coherent receiving environments.

The technical knowledge developed under the JSEP contract is widely disseminated through sponsor reviews, presentations of papers at technical meetings, publications in the open literature, discussions with visitors to the laboratories, and publication of laboratory technical reports.

UNIT 1 (a)

TITLE: Quantum Well and Reduced Dimensional Semiconductor Systems

SENIOR PRINCIPAL INVESTIGATOR: James S. Harris

RESEARCH ASSOCIATE: Eric S. Hellman

GRADUATE STUDENTS: Eric S. Hellman, Ed Wolak, Darrell
Schlom

SCIENTIFIC OBJECTIVE:

The objective of this project is to investigate heterojunction, quantum well and superlattice concepts and their application to new electronic devices with superior performance to devices based upon current semiconductor device principles. The small vertical dimensions which can now be readily achieved by molecular beam epitaxy (MBE) make it possible to fabricate superlattice structures which are totally dominated by quantum size effects. The long mean free path of the confined electrons in these structures makes it possible to fabricate lateral structures with a periodicity which is much less than the mean free path. The properties of carrier transport and storage in various regions of these ultra-small, 3-dimensionally confined structures are not well understood and their application to an entirely new generation of electron devices is in its infancy. At the outset this project focused on new quantum mechanical and ultra-small 3-dimensional device concepts and techniques to define and realize such ultra-small structures in both vertical and lateral dimensions. Near the end of the year, the 1 or 2-dimensional nature of the new high T_c superconductors provided an incentive to utilize the capabilities of MBE to grow and investigate the transport in these materials.

SUMMARY OF RESEARCH:

1. One Dimensional Electron Transport

One of the major goals of this project has been the investigation of transport of electrons confined to one-dimensional structures.

This is an extremely difficult fabrication problem because lateral definition of the order of 200-300Å must be achieved. One alternative to this approach is to utilize a high magnetic field to achieve carrier confinement in one-dimension. We sought to answer the question, how does one-dimensional confinement by a strong parallel magnetic field affect hot electron transport in high purity semiconductors? We have previously suggested (Hellman and Harris, 1986) that the one-dimensional confinement of electrons by a strong magnetic field might enhance the phonon emission process which dominates the energy relaxation of hot electrons in GaAs. Others have speculated (Argyres and Adams, 1956; Sakaki, 1980) that one-dimensional confinement could reduce low angle elastic scattering and thus enhance processes such as velocity overshoot. In this project, we have made measurements of longitudinal magnetoresistance in very lightly doped n-type GaAs which cover the range of electric fields up to 1kV/cm in 7T magnetic fields. Our data supports the conclusion that impact ionization of shallow donors dominates the conductivity of this material at 4K, with the major effect of magnetic fields being the deepening of the donor and the resonant excitation of the donors at certain fields. At 77K, the magnetic field induces a transition from sublinear to superlinear current-field characteristics, confirming for the first time the results of Sladek (1960), who attributed this behavior to the effects of one-dimensional confinement on elastic scattering rates.

Molecular beam epitaxy was used to grow a 3.0 μm thick layer of GaAs with nominally $1 \times 10^{15} \text{ cm}^{-3}$ silicon doping. This doping was chosen to be far below the impurity concentration required for impurity band transport (Sites and Nedoluha, 1981 and references therein), yet not so low that extremely thick layers would be required. The substrate temperature during growth was 645°C, the As/Ga flux ratio was 13 (gauge pressure) and the growth rate was 1 μm/hr. Techniques used in our group to reduce the background of acceptor impurities have been reported previously (Larkins, et al., 1986). The actual thickness of the layer was determined by the angle-lap and stain technique to be about 3.04 μm. Hall measurements using a sample in the van der Pauw geometry indicated a sheet carrier density of $3.4 \times 10^{11} \text{ cm}^{-2}$ at room

temperature and $4.2 \times 10^{11} \text{ cm}^{-2}$ at liquid nitrogen temperature. The higher carrier density at 77K may be due to ionization of deep traps in the substrate or at the growth interface. Adjusting for the surface and substrate depletion, (Chandra, et al., 1979) the carrier concentration was determined to be $2.43 \times 10^{15} \text{ cm}^{-3}$ at 77K. The mobility was $7780 \text{ cm}^2/\text{Vs}$ at room temperature and $56,700 \text{ cm}^2/\text{Vs}$ at 77K. Using the calculation of Wolfe, Stillman and Lindley (1970), this mobility would indicate a compensation ratio of 1.3 and a compensating acceptor concentration of $4 \times 10^{14} \text{ cm}^{-3}$.

In order to apply high electric fields to the GaAs layers while minimizing power dissipation and applied voltage, the epitaxial layers were patterned into small resistors with tapered current contacts at the ends and small arms along the side for parallel and transverse field contacts. The necks of the resistors were $10 \mu\text{m}$ (mask) wide and $200 \mu\text{m}$ long. The spacing between the field contacts was 30 and $50 \mu\text{m}$ on either side. Photoresist was used as an etch mask for a 3:1:50 $\text{H}_3\text{PO}_4/\text{H}_2\text{O}_2/\text{H}_2\text{O}$ mesa etch. The final width of the resistor was $3.8 \mu\text{m}$ on the top and $6.2 \mu\text{m}$ at the base, as measured by scanning electron microscopy. AuGeNi/Ti/Au metallization was deposited and patterned by lift-off using a plasma hardened two layer resist. This metal layer was used both to make ohmic contacts to the doped GaAs mesas, and to form wire bonding pads. After an anneal of the ohmic contacts in H_2 at 450°C for 5 minutes, the wafer was diced. Dice with well formed resistors and no growth defects close to the resistors were selected for electrical test. These dice were then mounted in non-magnetic ceramic packages, and the appropriate pads were wire bonded. Electrical measurements were done at liquid helium and near liquid nitrogen temperature. Packaged samples were mounted with thermal grease on a copper cold finger which was placed in the bore of a superconducting magnet. A current source was used to force current through the large contacts at the ends of the resistor, and voltages were measured at the side contacts using an electrometer with input impedance greater than $100 \text{ G}\Omega$ or using a multimeter with input impedance of $10 \text{ M}\Omega$.

Instabilities due to substrate effects made it impossible to reproduce the resistivity measurements precisely. At room temper-

ature, the measured fields were unstable above a critical applied voltage, typically about 40V. Measurement of significant zero-magnetic-field transverse voltages showed that this was due to the injection of current into the substrate. (Since the resistor itself is symmetric, the transverse voltage should be zero in the absence of a magnetic field. However, the metal lines from the field contacts wrap around the resistor in an asymmetric way, so that substrate current induces apparent transverse voltages.) Deep traps in the substrate are responsible for its semi-insulating character, but can also give rise to effects such as back-gating in MESFETs (Kocot and Stolte, 1982). Thus, when electrons are injected into the substrate, many of them are trapped there, and thus change the amount of substrate depletion in an epitaxial layer. At room temperature, the instabilities due to the substrate injection have time constants ranging from a few milliseconds to a few seconds. At lower temperatures, the time constants are much longer, so that measurements are repeatable as long as no current is injected into the substrate. For this reason, the compliance voltage of the current source was monitored to avoid substrate injection at the contacts, and the measurement software was written so that the the resistor spent a minimum time under bias.

Typical current-field characteristics of a single resistor measured above liquid nitrogen temperature with three different magnetic fields are shown in Fig. 1. The low field resistivity is increased by the magnetic field; however, substrate effects make it difficult to directly compare the current-field characteristics. At low electric fields, the curves are almost linear, while for fields above 100 V/cm, the differential conductivity is reduced. Fig. 2 shows the ratio of the differential conductivity to the low field

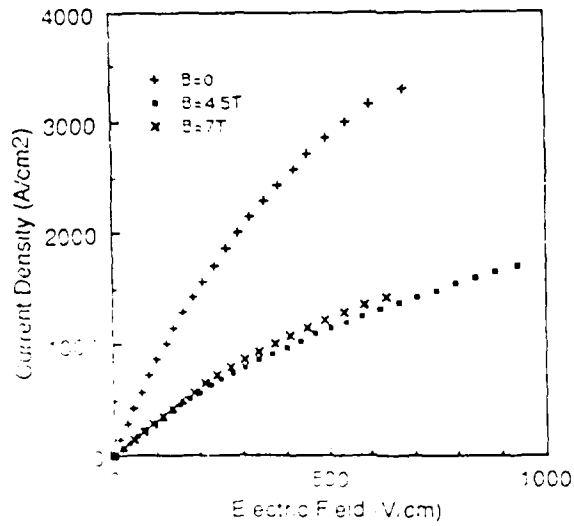


Fig. 1 Approximate current density versus electric field for parallel magnetic fields of 4.5 and 7T, and without magnetic field. The cross-sectional area is assumed to be $11.7\mu\text{m}^2$.

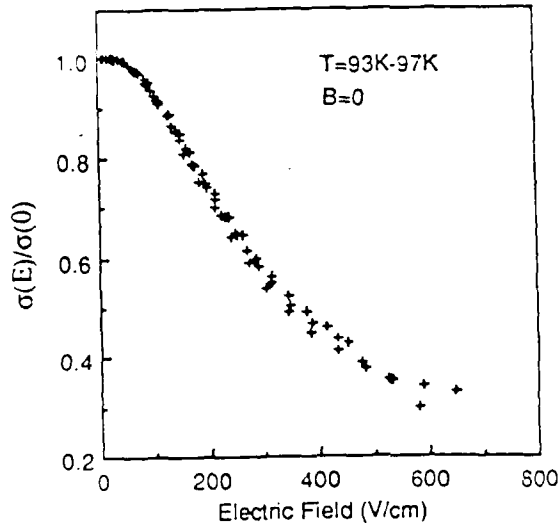


Fig. 2. Differential conductivity ratio vs. electric field for temperatures between 91K and 97K without magnetic field.

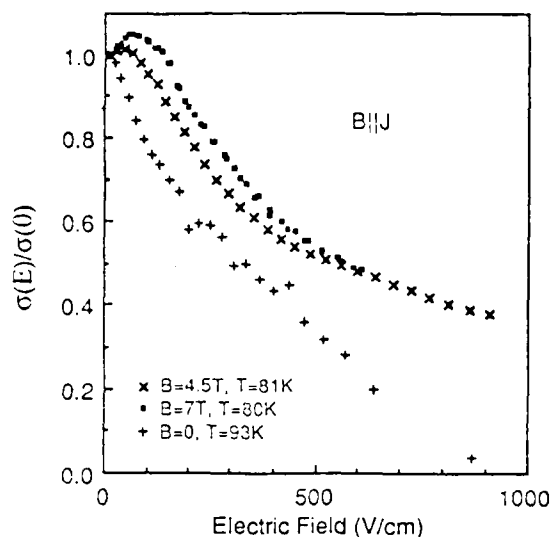


Fig. 3. Differential conductivity ratio versus electric field for measurements of a single sample made in parallel magnetic fields of 0T, 4.5T and 7T. Note the superlinear behavior below 100 V/cm in the parallel magnetic fields.

conductivity as a function of electric field in the absence of magnetic field. While the current field curves may change due to the substrate effects mentioned above, the differential conductivity ratio curves are completely unaffected by any slow instabilities. Note that the differential conductivity drops at a relatively low field, and then levels off above 400V/cm. Figure 3 shows a differential conductivity plot for one sample with parallel magnetic fields of 0T, 4.5T, and 7T.

Although the shapes of the two curves measured in magnetic fields are similar to those observed without magnetic field, there are significant differences. The current-field curves are slightly superlinear at fields below about 100V/cm. The drop in the differential conductivity appears to saturate at a higher value relative to the low field conductivity in the presence of magnetic fields.

At 4K, current-field characteristics showed sharp turn-ons of the conductance at about 5V/cm. When parallel magnetic fields were applied at liquid helium temperature, the field required to turn

on the conductance increased dramatically. However, contact resistances became so high that the high input impedance electrometer was required, which made electric field sweeps impractically slow. Sweeps of the magnetic field from 0 to 8.5T were made to get a better picture of the magnetic field dependence of the conduction at liquid helium temperature. These sweeps reveal large structure in the longitudinal magnetoresistance. Figure 4 shows the measured resistance as a function of parallel magnetic field for two different applied currents. A minimum is observed near 4.5T, while maxima are observed at 2.7T and at 7.5T. There appears to be some hysteresis in the curves; this may indicate that

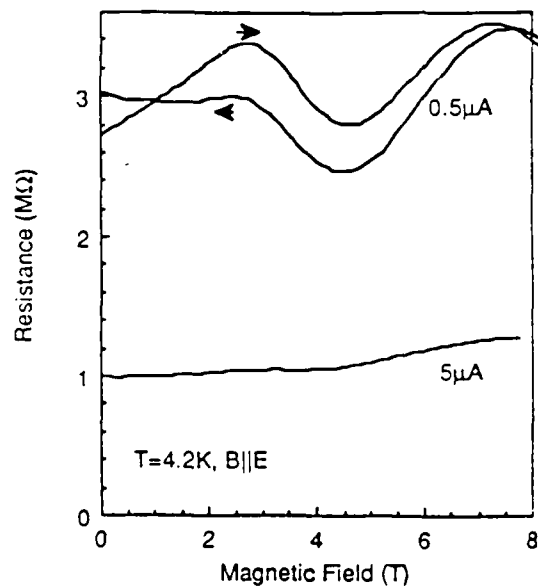


Fig. 4. Longitudinal magnetoresistance as a function of the magnetic field, for two applied currents. The two traces at the top are for magnetic fields sweeping up and down.

the sweep rate, ~ 0.5 T/min, was still too fast for the system to reach steady state. Larger currents reduce the resistance and the amplitude of the magnetoresistance variation. A significant increase of noise in the voltage measurement was observed for magnetic fields above about 5T. No magnetoresistance structure was observable in the same samples at liquid nitrogen temperature.

The importance of impact ionization of neutral impurities for low temperature transport in high purity semiconductors has been known since the late 50's from work on p-type Ge (McWhorter and Rediker, 1959). Superlinear current-voltage characteristics due to impact ionization of donors in GaAs were widely studied following the work of Oliver (1962). These effects are observed only in material with impurity densities low enough that the conductivity through impurity bands is small, and only at temperatures where the electrons are frozen onto the shallow impurity levels. Our helium temperature measurements correspond closely to this work. The interaction of impact ionization and the deepening of the impurity levels by magnetic fields (Yafet, Keyes, and Adams, 1956) was studied in some depth by Poehler (1971), who measured current-field characteristics of GaAs epitaxial films at low temperatures in magnetic fields of up to 4.1T. Poehler's samples had impurity concentrations five times larger than the samples used in the present work, and in contrast to this work, he saw almost no effect for parallel magnetic fields.

The structure observed in the magnetic field sweeps of the magnetoresistance appears to be closely related to a phenomenon known as the magneto-impurity resonance effect, which happens when multiples of the cyclotron energy become equal to the donor binding energy, or to a donor excitation energy. This topic has been reviewed by Eaves and Portal (1978). In comparison to the previous work on the magneto-impurity resonance effect, the magnetoresistance structure reported here is very broad and huge in magnitude, comparable only to the magnetoresistance oscillations reported by Zverev and Shovkun (1984) for GaAs excited by infrared radiation. Since the electron concentration of the samples is significantly larger than for previous magneto-impurity experiments, the breadth of the peaks is not surprising. The broad

dip between 4.5T and 5T in Fig. 4 can be attributed to a resonance of the cyclotron energy with the donor binding energy. Although this resonance is not the one usually observed in magneto-impurity experiments on samples with lower carrier densities, similar structure has been observed in tunnel junctions with lightly doped GaAs cathodes (Eaves and co-workers, 1987). The origin of the second maximum in Fig. 4 is uncertain. Still, the observation of donor ionization effects at current densities greater than $10\text{A}/\text{cm}^2$ and in electric fields higher than $200\text{ V}/\text{cm}$ allows us significant insight into the transport properties of warm electrons in GaAs. The large magnitude of the magnetoresistance oscillations indicates that donor impact ionization continues to dominate the conductivity at these currents and fields. This finding supports the models of Eaves and co-workers (1985) which explain phonon oscillations in the conductance of GaAs/AlGaAs tunnel junctions (Hickmott and co-workers, 1984) in terms of impact ionization of donors in similar material.

In the absence of magnetic field, the increase of the resistivity with increasing electric field (sub-linear conductivity exponent) seen in the liquid nitrogen current-field curves is well known to be a result of electron heating by the electric field, which allows increased loss of electron energy by phonon emission. The field range at which this occurs depends on the mobility. The observed field range is in good agreement with the available calculations (Ruch and Fawcett, 1970) and with elementary models incorporating energy dependent scattering rates (Hellman, 1987).

The superlinear conductivity measured in magnetic fields near 80K, seen in Fig. 3, is quite surprising. Sladek (1960) reported that quantizing parallel magnetic fields could induce superlinear conductivity in n-type InSb between 65K and 90K. This observation has not been confirmed or commented upon in the literature. Sladek's measured nonlinearities are in poor agreement with his theory and with other measurements (Kanai, 1960; Okazaki, 1985), suggesting that material inhomogeneities may have been significant. The low field, zero magnetic field nonlinearities measured in this study are in good agreement with the theory of Seeger (1971). Nicholas and Stradling (1975) have also reported effects of parallel magnetic

field on nonlinear conduction in very high purity GaAs, but only reported data for fields above 5kV/cm. The superlinearity in the present data is seen up to 100 V/cm in parallel magnetic field and coincides with a reduction of the low field conductivity. Since the change in carrier concentration due to magnetic freeze-out is negligible at this lattice temperature, the factor of two reduction in the low field conductivity must be related to a reduction of the electron mobility in parallel magnetic field. The corresponding superlinear conductivity below 100 V/cm suggests that this mobility increases with the temperature of the carriers. The sublinear conductivity associated with phonon emission also appears shifted to higher field in perpendicular magnetic fields, consistent with a lower mobility in parallel magnetic field. These data are consistent with the model of Sladek, who pointed out that one dimensional confinement by a magnetic field changes the dependence of elastic scattering on electron energy.

In conclusion, measurements of the current-field characteristics of very lightly doped gallium arsenide resistors at liquid nitrogen temperatures indicate that parallel magnetic fields have profound effects on the mobility of warm electrons. Large magneto-impurity effects at 4K confirm the dominance of impurity impact ionization over the conductivity in this material up to relatively large electric fields. These results provide insight into the physics of one-dimensional electron transport.

2. MBE of Superconductors

In collaboration with the MBE group at Varian Research Center (VRC) and with the superconductivity group in the Applied Physics Department at Stanford, we have embarked on an effort to make thin films of the new high temperature superconductors by MBE. The key to this effort is the availability of an old MBE system located at VRC. We have taken the approach of using all effusion cells to obtain molecular beams of the metals by using dysprosium instead of the more popular yttrium, and by using a simple gaseous oxygen source. This approach has been validated by our initial results on thin films of the high temperature superconductor $\text{DyBa}_2\text{Cu}_3\text{O}_{7-x}$ grown on SrTiO_3 substrates using these molecular beam epitaxy techniques. Reflection high energy electron diffraction (RHEED) patterns

observed during deposition indicate incomplete oxidation of copper and growth of oriented metallic copper microcrystals in a matrix of amorphous barium and dysprosium oxides. None of the films has indicated a superconducting transition as grown, however, after a post growth oxygen anneal and solid phase epitaxy, the films exhibit sharp superconducting transitions with zero resistance observed as high as 87K. Critical current densities of 4.8×10^5 A/cm² at 4.2K and 3.9×10^4 A/cm² at 77K have been measured. Since the RHEED indicates that we do not form the superconductor in-situ, we are developing an ionized oxygen source to realize true epitaxy of the superconductors such that no oxygen anneal is required. The second goal will be to investigate the layered nature of these materials and most importantly, if we can modify this layering by MBE.

JSEP SUPPORTED PUBLICATIONS

1. E. S. Hellman and J. S. Harris, Jr., "Energy-Momentum Relation for Polarons Confined to One Dimension," *Phys. Rev. B.*, **33**, 8284-8290 (1986).
2. E. S. Hellman and J. S. Harris, "Polaron Transport in Quasi-One Dimensional Semiconductor Heterostructures," *Surf. Sci.*, **174**, 459-465 (1986).
3. E. S. Hellman and J. S. Harris, Jr., "Polynomial Kinetic Energy Approximation for Direct-Indirect Heterostructures," *Superlattices and Microstructures*, **3**, 167-169 (1987).
4. E. S. Hellman and J. S. Harris, Jr., "Hot Electron Transport Parallel to Strong Magnetic Fields in Gallium Arsenide," to be published in *Solid State Electronics*.
5. C. Webb, S.-L. Weng, J. N. Eckstein, N. Missert, K. Char, D. G. Schlom, E. S. Hellman, M. R. Beasley, A. Kapitulnik and J. S. Harris, Jr., "Growth of High T_C Superconducting Thin Films Using Molecular Beam Epitaxy Techniques," to be published in *App. Phys. Lett.*
6. D. R. Allee, P. R. de la Houssaye, D. G. Schlom, J. S. Harris and R. F. W. Pease, "Sub-100 nm Gate Length GaAs MESFETs and MODFETs Fabricated by a Combination of Molecular Beam Epitaxy and Electron Beam Lithography," to be published in *J. Vac. Sci and Tech. B.*
7. D. R. Allee, P. R. de la Houssaye, D. G. Schlom, B. W. Langley, J. S. Harris and R. F. W. Pease, "Sub-100 nm Gate Length GaAs MESFETs

Fabricated by Molecular Beam Epitaxy and Electron Beam Lithography," to be published in Proceedings of IEEE/Cornell Conference on Advanced Concepts in High Speed Semiconductors for Devices and Circuits.

JSEP SUPPORTED PRESENTATIONS

1. E. S. Hellman and J. S. Harris, "Slow Polarons Below the Phonon Emission Threshold in High Magnetic Fields or in One Dimensional Semiconductor Heterostructures," presented at the American Physical Society Meeting, April 1986.
2. E. S. Hellman and J. S. Harris, "Polynomial Kinetic Energy Approximation for Direct-Indirect Heterostructures," presented at the International Conference on Superlattices, Microstructures and Microdevices, Goteborg, Sweden, August 1986.
3. E. S. Hellman D. G. Schlom, N. Missert, K. Char, J. S. Harris, Jr., M. R. Beasley, A. Kapitulnik, T. H. Geballe, J. N. Eckstein, S.-L. Weng and C. Webb, "Molecular Beam Epitaxy and Deposition of High T_c Superconductors," 8th MBE Workshop, Los Angeles, September 1987.

Ph.D. DISSERTATION

- E. S. Hellman, "Hot Electron Resistance and Magnetoresistance in High Purity Gallium Arsenide, Ph.D. dissertation, Stanford University, May 1987.

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UNIT 1(b)

TITLE: Ultra-Submicron Devices

SENIOR PRINCIPAL INVESTIGATOR: R. F. W. Pease

RESEARCH ASSOCIATE: S. Y. Chou

GRADUATE STUDENT: D. R. Allee

SCIENTIFIC OBJECTIVE:

The objective of this project is to investigate heterojunction, quantum well and superlattice concepts and their application to new electronic devices with superior performance to devices based upon current semiconductor device principles. The small vertical dimensions which can now be readily achieved by molecular beam epitaxy (MBE) make it possible to fabricate superlattice structures which are dominated by quantum size effects. The long mean free path of the confined electrons in these structures makes it possible to fabricate lateral structures with a periodicity which is much less than a mean free path. The properties of carrier transport and storage in various regions of these ultra-small, 3 dimensionally confined structures are not well understood and their application to an entirely new generation of electron devices is still in its infancy. The project will focus on new quantum mechanical and ultra-small 3-dimensional device concepts and techniques to define and realize such ultra small structures in both vertical and lateral dimensions

SUMMARY OF RESEARCH:

The development of molecular beam epitaxy (MBE) in the early 70's enabled the study of quantum size effects in tailored structures for the first time. Extensive investigation of AlGaAs/GaAs superlattice structures has uncovered a great deal of interesting physics. Novel electronic devices that are based on these quantum effects, such as the resonant tunneling diode, have been successfully fabricated. MBE however is a layer growth technology, and the quantum size effects demonstrated by MBE grown materials is necessarily perpendicular to the surface of the

wafer. Electrons are limited to one-dimensional confinement, that is confinement to a plane parallel to the wafer surface.

The potential to develop new electronic devices will be greatly enhanced if lateral electron confinement is a design option allowing the incorporation of lateral superlattices, quantum wires and quantum dots. There are two technologies capable of defining patterns laterally with sufficient resolution to observe quantum size effects: X-ray lithography and ultra-high resolution electron beam lithography (UHREBL). X-ray lithography has a resolution limit of 100nm structures on a 200nm period but has the advantage of high throughput. Using PMMA as the resist, UHREBL has a resolution limit of approximately 25nm structures on a 50nm period. These dimensions are not as small as the layer thicknesses obtainable with MBE but are small enough to observe quantum effects at low temperatures.

We are pursuing both lithographic techniques combined with GaAs technology and MBE to study the physics and device possibilities associated with one, two, and three-dimensionally confined electrons. X-ray lithography equipment has recently been donated by Varian and is currently being set up. An existing custom UHREBL has been adapted for device fabrication. These modifications include a stage that will hold 2 and 3 in. wafers for ease in later processing and a custom pattern generator that facilitates fine line lithography and has an alignment accuracy of 100nm.

As a precursor to the fabrication of quantum devices, a GaAs process sequence has been established by fabricating MESFETs and MODFETs with sub-tenth micron recessed gates on MBE grown wafers (Figs. 1,2). The gate was defined with UHREBL using a thin (70 nm) layer of PMMA resist. Before deposition and liftoff of the gate metal, the gate recess was formed with a citric acid etch that did not attack the PMMA unlike the more common etchants.

MESFETs with gate lengths down to 65 nm and transconductances as high as 330 S/m have been fabricated (Fig. 3). A study of transconductance vs gate length revealed no evidence of increased effective saturation velocity due to velocity overshoot phenomena

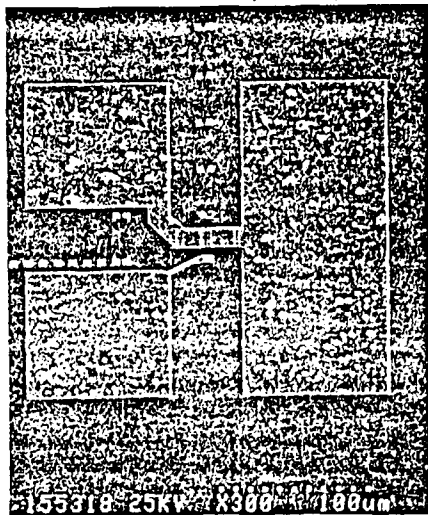


Fig. 1. Low magnification micrograph of a sub-100 nm gate length MESFET. The source, drain, and gate contact pads are prominent.

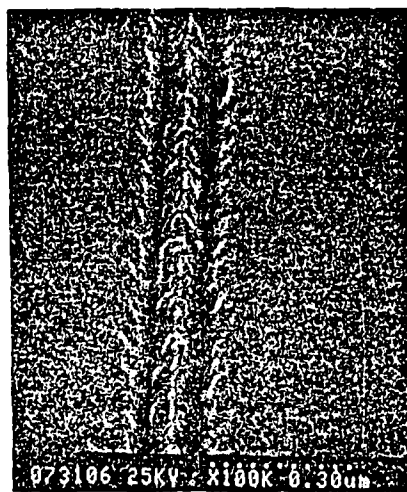


Fig. 2. High magnification micrograph of an 80 nm gate electrode in a 160 nm recess.

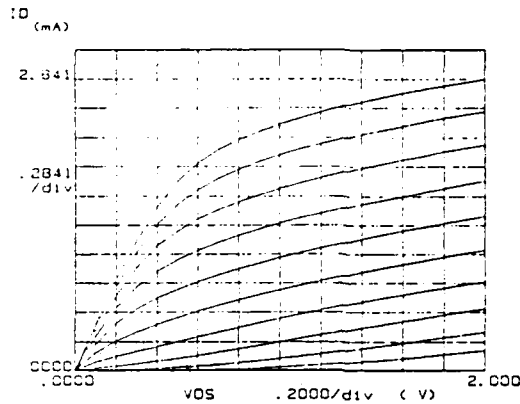


Fig. 3. IV characteristics for a 80 nm recessed gate scaled MESFET. The gate voltage varies from 0.5 V to -0.4 V in 0.1 V steps. This structure (B) has a 60 nm thick active channel doped with Si at $9 \times 10^{17} \text{cm}^{-3}$, and a 60 nm thick n+ cap doped with Si at $2 \times 10^{18} \text{cm}^{-3}$.

for gate lengths down to 90 nm. A strong variation in the drain source saturation current, I_{DSS} with gate length was determined to be the result of citric acid etch rate dependence on the size of the resist opening. A lower etch rate resulted in a shallower etch depth and hence, a thicker active channel. I_{DSS} could be predicted for any device to within +10% by examining the extent of etch undercut in a high performance SEM.

MODFETs with GaAs and InGaAs channels have been fabricated with gate lengths as small as 55 nm. The GaAs channel MODFETs had transconductances as high as 415 S/m, and the InGaAs MODFETs had transconductances as high as 315 S/m. GaAs channel MODFETs were found to have a maximum effective saturation velocity of $1.95 \times 10^7 \text{ cm/s}$ at a gate length of 150 nm. The occurrence of this maximum effective saturation velocity near a gate length of 150 nm agrees with the predictions of Kizilyalli et. al.

Work has begun on the first lateral quantum device, a lateral double barrier resonant tunneling MODFET. The depth of the central well is tunable with a stacked gate configuration. The confinement and tunneling characteristics of the electrons in the central quantum wire will be studied as a function of temperature, electric and magnetic fields. This structure has device potential as a high speed three terminal resonant tunneling transistor. Work is also underway on lateral surface superlattices. A literature review of research on this topic has been completed. The lateral surface superlattices to be built first involve various combinations of grid and grating stacked gates in a MODFET. The device applications include tunable photon detectors, high frequency oscillators, and high speed switching transistors.

On a related topic of high resolution electron beam lithography, work is underway on a Monte Carlo simulator to study space charge effects in an electron gun. The electron-electron interactions near the source where the particle velocity is small and the charge density is high significantly contribute to the energy spread of the electrons. This energy distribution results in lateral beam broadening and a larger chromatic disc of confusion. Both of these effects increase the minimum achievable spot size and hence affect the lithographic resolution. Novel data structures are being incorporated in the Monte Carlo code to increase either the speed of simulation or the number of particles that can be simulated in a given time. The sophisticated graphics capabilities of the MacII are being utilized to provide a intuitive interpretation of the physics that is usually lacking in numerical simulations.

JSEP SUPPORTED PUBLICATIONS AND PRESENTATIONS

1. D. R. Allee, P. R. de la Houssaye, D. G. Schlom, J. S. Harris and R. F. W. Pease, "Sub-100 nm Gate Length GaAs MESFETs and MODFETs Fabricated by a Combination of Molecular Beam Epitaxy and Electron Beam Lithography," to be published in *J. Vac. Sci and Tech. B*.
2. D. R. Allee, P. R. de la Houssaye, D. G. Schlom, B. W. Langley, J. S. Harris and R. F. W. Pease, "Sub-100 nm Gate Length GaAs MESFETs Fabricated by Molecular Beam Epitaxy and Electron Beam

Lithography," to be published in Proceedings of IEEE/Cornell Conference on Advanced Concepts in High Speed Semiconductors for Devices and Circuits.

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7. D.R. Allee, P.R. de la Houssaye, D.G. Schlom, J.S. Harris and R.F.W. Pease, "Sub-100 nm gate length GaAs MESFETs fabricated by a combination of molecular beam epitaxy and electron beam lithography", presented at the 1987 IEEE/Cornell Conference on Advanced Concepts in High Speed Semiconductor Devices and Circuits.
8. P.R. de la Houssaye, D.R. Allee, Y.C. Pao, D.G. Schlom, J.S. Harris and R.F.W. Pease, "Electron saturation velocity variation in InGaAs and GaAs channel MODFETs for gate lengths down to 55 nm", to be published.

9. C. Kiziyalli, K. Hess, J. L. Larson, D.J. Widiger, "Scaling properties of high electron mobility transistors", IEEE Trans. Electron Devices, vol. ED-33, pp. 1427-1433, 1986.

10. D.R. Allee and R.F.W. Pease, "Lateral surface superlattices", internal report.

11. T. Groves, "Mutual repulsion effects in a high throughput e-beam lithography column", J. Vac. Sci. Technol., 19(4), Nov./Dec. 1981.

Unit 1(c)

TITLE: Ga/As Silicon Integrated Circuits

PRINCIPAL INVESTIGATOR: B. A. Wooley

GRADUATE STUDENT: G. Nasserbakht

SCIENTIFIC OBJECTIVE:

The objective of this research is to investigate means by which newly emerging compound semiconductor technology, such as heteroepitaxial GaAs on silicon, can be exploited at the circuit and system level. The initial emphasis of the program is on the application of GaAs/Si technology to optoelectronic circuits for broadband communication systems.

SUMMARY OF RESEARCH:

Recent progress in the growth of device-quality heteroepitaxial films on silicon suggests the possibility of a merged GaAs and silicon integrated circuit technology. The potential benefits of such a merged technology are particularly significant in the area of optoelectronic applications, wherein the transition between optical and electronic signals is often necessarily accompanied by a transition in semiconductor material. We have therefore begun a collaborative effort among faculty and students with research interests in both integrated circuits and solid-state devices and materials to demonstrate the feasibility of merged GaAs and silicon technology.

A variety of GaAs devices have already been implemented in films grown on silicon substrates, and GaAs MESFETs have been successfully realized on substrates containing silicon MOS devices. However, the feasibility of forming such devices in a fashion compatible with a complete integrated circuit technology, as well as interconnecting the GaAs and silicon components, remains to be established.

To demonstrate the viability of merged GaAs on silicon technology we have chosen the front-end of a receiver for fiber-optic communications as a particularly important application

vehicle. Our initial goal is the fabrication of a GaAs photodetecting diode on a silicon substrate in which a receiver preamplifier has been integrated. With such a configuration it should ultimately be possible to overcome the limitations on receiver sensitivity and bandwidth that result from parasitic capacitance at the amplifier input.

To date, we have designed a silicon bipolar transimpedance amplifier that will incorporate a GaAs interdigitated MSM (metal-semiconductor-metal) photodetector. Substrates containing this circuit are now being fabricated at Hewlett-Packard. No special processing of the circuits is required other than that they be fabricated on substrates with a special orientation. The substrates will be removed from the silicon process prior to metallization, and selected regions will be etched. Within these etched areas GaAs will be grown via molecular beam epitaxy. Metal interconnections will be added after formation of the photodetector. Since the GaAs is grown in etched regions of silicon, the topology prior to metallization will be relatively planar.

In the integrated GaAs/Si receiver the capacitance at the input to the preamplifier, including both diode and interconnect capacitance, is estimated to be less than 200nF. This value is well below that achievable with discrete photodetectors, even when using the most advanced hybrid packaging technology. Simulation results suggest that the initial receiver circuit should operate at frequencies approaching 1 GHz while providing a transimpedance of 4k Ω .

We have also begun to investigate the design of an optoelectronic receiver wherein GaAs components are integrated on a substrate containing silicon MOS integrated circuits. An NMOS preamplifier has been designed so as to incorporate a GaAs MSM photodetector. As is the case for a bipolar receiver, in the initial circuits we are primarily concerned with determining the extent to which fabrication of the GaAs devices influences the characteristics of the silicon devices and circuits. Also of major importance is a demonstration of the ability to interconnect the GaAs and silicon components.

Unit 2

TITLE: The Chemical and Electronic Structure of Refractory Metal GaAs Interfaces

**SENIOR PRINCIPAL INVESTIGATORS: C. R. Helms, I. Lindau,
and W. E. Spicer**

GRADUATE STUDENTS: Margaret Kniffin and Carl McCants

SCIENTIFIC OBJECTIVES:

Refractory metals, particularly Ti, W, and Mo, are increasingly becoming the metallization of choice for the formation of Schottky barriers in GaAs devices. The objective of this work is to make a significant advancement in our level of knowledge of refractory metal-GaAs interfaces. This information will also contribute to a general understanding of GaAs Schottky barriers.

Having briefly described our general goals, more specific objectives of our experimental program are:

- To determine the effect of work function, metal electronic structure, interface intermixing, and chemical reactions on Schottky barrier height for refractory metal (especially Ti) GaAs interfaces.
- To quantitatively determine the effect of oxygen and GaAs surface defects on Schottky barrier height for Ti-GaAs interfaces.

SUMMARY OF RESEARCH:

Over the past year, particular attention has been focused on the changes that occur at the Ti/GaAs interface upon annealing for clean (UHV cleaved) and oxide covered (chemically cleaned) substrates. We have used a variety of surface spectroscopic techniques to correlate the changes in interfacial chemistry to the electrical properties of the interface. The following describes the comparisons between the interfacial reactions at room temperature and after annealing.

1. Room Temperature

We have studied the annealed Ti/GaAs(110) interface, using soft x-ray (SXPS), x-ray (XPS) and ultraviolet (UPS) photoelectron spectroscopies to monitor the substrate and overlayer core levels and the valence band for Ti thicknesses between 6.7 and 20 ML and annealing temperatures between 200° and 425° C [1]. For brevity, the SXPS results (6.7 ML annealed to 325°C) are described. Using computer controlled curve fitting, we decompose the Ga 3d spectra into bulk substrate (B), surface shifted (S), and chemically shifted reacted (R) components [1]. The surface component becomes negligible at 0.67 ML coverage; for this and higher coverages, the core level is then modeled by a two-component fit which consists of the bulk substrate component (B) and a chemically shifted reacted component (R). The reacted peak becomes visible at a coverage of .13 ML. As the substrate component attenuates, this component, which indicates the formation of a Ti-Ga compound, both increases in intensity and shifts towards lower binding energy due to a change in stoichiometry; this is also in agreement with results obtained by Ruckman et. al. [2] and Ludeke and Landgren[3]. At a coverage of 6.7ML, this Ti-Ga compound peak has decreased in intensity (relative to its value at 1.3 ML), but is still visible, shifted by 1.6 eV to lower binding energy relative to Ga in GaAs. We also note that the bulk substrate emission is negligible, confirming that what we observe is purely reacted Ga. The decrease in intensity may be related to the As outdiffusion, as it appears that the As is reacting with the Ti at a rate faster than the Ga; this will be discussed further in the next section. At this highest coverage, the peak is modeled with a single component modified by a Doniach-Sunjic (D-S) line shape parameter of .12 [1,3].

Deconvolution of the As 3d core level is more complex than that for the Ga [1,3]. The results from the Ga3d deconvolution, however, provide a basis to help simplify the analysis, and the results suggest two Ti-As reacted components, denoted R1 and R2. By comparing the spectra at the lower coverages to this, we find that the first of the reacted components (R1) is visible at 0.13 ML, near the value for the surface shifted component. At 0.67 ML, as stated earlier, the surface shifted component is negligible, and what remains are the

bulk substrate and two reacted components. By 6.7 ML, the intensity of each component is about half that at the previous coverage (3.3 ML), indicating further reaction with the Ti or possibly the Ti-As compounds being covered up by the unreacted Ti (due to kinetic limitation). At these coverages, both theoretical peaks are also modified by a D-S line shape parameter of .12 [1, 3].

Though UHV-cleaved GaAs - metal interfaces are of great theoretical importance, 'practical' metal-GaAs interfaces invariably contain oxides and impurities left by pre-deposition processing of the substrate. It is thought that this interfacial layer may play a role in the electrical properties of the interface, although the literature is sparse. One goal of this project is to ascertain what effects interfacial impurities and defects have on the physics and chemistry of refractory metal (Ti in particular) interfaces.

The aqueous chemistry of gallium arsenide is quite complex. As a result both the thickness and composition of the oxide layer left by substrate cleaning procedures is sensitive to the etching solution used in the process. We have characterized the residues left by several common etching solutions by using a combination of Auger electron spectroscopy and X-ray photoelectron spectroscopy and investigated the effect of these interfacial layers on the Ti-GaAs interface [4].

Thin (300 Å) titanium films were deposited on GaAs substrates which had been cleaned by the previously characterized processes. The as-deposited barrier heights were then measured using the internal photoemission technique. For comparison, the barrier heights of Ti deposited on clean (100) GaAs surfaces, which had been prepared in UHV by one of several methods (thermal desorption of As caps and passivating oxides, sputter cleaning and annealing), were also measured.

For the most part the as-deposited barrier height was insensitive to the presence of an interfacial layer. With the exception of the HCl:H₂O clean the barrier heights fell in the range .68 to .70 eV. This is in excellent agreement with the barrier height

for Ti on UHV-cleaved GaAs measured by I-V. We are currently investigating the possibility that the Ti reacts to completely consume the interfacial layer (although TEM results would suggest that this isn't the case).

The HCl:H₂O clean consistently gave a slightly higher barrier height (.73 eV). Preliminary results show slightly different reverse I-V characteristics. The origin of this behavior is unclear.

2. Effects of Annealing

Upon annealing, the intensity of the reacted Ga peak begins to increase and the peak begins to shift back towards higher binding energy. At 200° C, the shift is by 0.3 eV, and the intensity increases by a factor of two. The subsequent anneals (250° and 325° C) each show a shift of .3 eV to higher binding energy. At 325° C, the intensity of this reacted peak decreases, suggesting a slowing in the movement of Ga atoms away from the interface relative to the movement of As atoms, as will be seen in the following discussion. Analysis of the intensity vs. temperature for the reacted components shows that the area of the reacted Ga increases faster with temperature between RT and 200° C than that of the reacted As components. Between 200° C and 250° C, the rate of increase remains about the same for the reacted Ga, but the reacted As area increases sharply. This leads us to believe that at these temperatures, the Ti-As compounds may be acting to enhance the movement of Ga towards the overlayer surface. The width of the reacted Ga peak changes only slightly; there is an increase between RT and the 200° C anneal, but essentially no change between 200° and 325° C. The shape of the fitted Ga peak is a result of modification of the theoretical lineshape by the D-S lineshape parameter of .12. Even with this correction, we see little change in the width. This is of interest and also puzzling, as one would expect a broadening of the peak as the Ti-Ga compound changes composition. The final energy position of this reacted peak is .7 eV lower binding energy than the Ga in GaAs, which is close to the value for metallic Ga of 0.9 eV lower binding energy [5]. This suggests the presence of a Ga-rich compound.

The annealing results for the As 3d are quite different from those seen for the Ga 3d. First, the energies of both reacted components remain relatively unchanged ($\Delta E = \pm .04$ eV) between RT and 325° C. In addition, the overall intensity of the peak increases over the entire range of annealing temperatures, suggesting a constant movement of As away from the Ti-GaAs interface towards the overlayer surface. As stated earlier, the area increase of the As is large between 200° and 250° C. This increase, coupled with the slight change in the rate of change in the Ga area suggests that there is stronger bonding between the Ti and the As than between Ti and Ga at these elevated temperatures. The intensity ratio between the first reacted component and the second component decreases steadily with increasing temperature.

One of the most striking features observed is the difference in behavior between the Ga and As core levels upon annealing. The energy stability of the As core level energy position with temperature suggests that the Ti bonds readily with the As and forms stoichiometric Ti-As compounds. The steady intensity increase of the SXPS As spectra implies that this reaction is enhanced at elevated temperatures and that more of the Ti overlayer is becoming reacted; comparison with the XPS As spectra also suggests that these reaction products are distributed throughout most of the overlayer. The intensity increase further implies that there is a large amount of As moving from the substrate into the overlayer and bonding with the Ti very quickly. This appears to be a continuation of the trend begun at room temperature, as previous studies have shown that the As is visible for much higher coverages than the Ga [2,6] and seems to limit the amount of Ga moving into the Ti overlayer.

In contrast, the continuous RT Ga core level shift suggests that no stoichiometric Ti-Ga compound is favored to dominate. Analysis of the shifts in the reacted Ga core level component with temperature for spectra taken at different photon energies shows two important features. First, the surface-sensitive SXPS data show that the energy of the reacted Ga peak after the final anneal is at slightly higher binding energy than that for elemental Ga. This suggests that farther out into the overlayer, the Ti-Ga compound is

very Ga rich. This differs from the RT compound which is that of a dilute Ga-Ti alloy [6]. On the other hand, the more bulk-sensitive data show that the position of the reacted peak after annealing is approximately that for elemental Ga, ~ 0.9 eV. This suggests that some elemental Ga is very near the overlayer/semiconductor interface. The data also imply that clustering of the Ga at the overlayer surface may be occurring [7].

The reaction of titanium with chemically cleaned (100) GaAs substrates, for thick (1000 Å) films has also been investigated in the temperature range 250° to 600 °C [4,8].

In the as-deposited samples an interfacial oxide layer was clearly visible in the Auger depth profiles. High resolution TEM micrographs revealed a uniform oxide layer about 15Å thick.

The Ti films started to react with the GaAs substrate at about 380 °C. While no significant changes were detected by Auger sputter profiling, due to limited depth and spatial resolution, TEM resolved noticeable changes in and near the oxide layer. Changes in the contrast intensity of the oxide layer indicate that some diffusion has occurred through this layer. TiAs grains were also detected in the substrate just beneath the interfacial oxide layer.

Samples annealed at higher temperatures exhibited a layered structure at the interface. There was also a tendency for a small amount of Ga to segregate to the surface. Auger depth profiling shows that distinct Ti-As and Ti-Ga layers have formed, the former being closest to the GaAs substrate. This is in agreement with the results of Wada et al.[9]. It appears that the interfacial oxide layer has been completely consumed in the reaction.

It is interesting to note that the arsenic profile remained relatively constant throughout the course of the reaction. This suggests that the reaction involves the exchange of Ti and Ga across the original interface, with the TiAs layer growing in to consume the substrate and Ga diffusing out into the metal film to form Ti-Ga compounds.

This layered structure is maintained until the Ti film is completely consumed. From measurements of the reacted layer thickness, the kinetics of this reaction were determined. The reaction was found to obey a parabolic growth law, suggesting diffusion controlled growth. It is not clear, however, whether the diffusion of Ti or the removal of Ga is the rate limiting step. An activation energy of 1.75 eV was measured.

Of particular interest to those involved in device fabrication is how the metallurgical reaction at the interface affects the electrical properties. The effect of annealing on the Schottky barrier height was monitored by a variety of techniques. A sharp increase in barrier height, over the as-deposited value of .70 eV, was observed between 350° and 400 °C. This coincides with the onset of significant interdiffusion between the substrate and metal film, and the formation of TiAs at the interface. The I-V studies performed on diodes formed by depositing 500Å Ti on cleaved n-GaAs(110) also show that the barrier height increases by ~0.1 eV to 0.8 eV, although the change occurred at a slightly lower temperature (320°C). This difference may be related to the presence of the thin oxide layer at the interface of the GaAs(100) samples. At present, efforts are being made to correlate this barrier height change to the enhancement or decrease of As-related defects at the interface. Annealing at temperatures above 430 °C resulted in a stable high barrier. This can be attributed to the formation of a uniform TiAs-GaAs interface.

Additional studies planned will examine the role of the role of interfacial oxides on the reaction temperature. Data from experiments which investigated the effects of annealing on thin (0.3 -3.3 ML) Ti overlayers on n-GaAs(110) is being analyzed. Also, data from experiments taken at low temperature (-160°C) is being analyzed to further study kinetic effects on the chemical interactions. Finally, TEM studies of the UHV fabricated diodes are planned to correlate with the results from the TEM work on oxide covered layers.

JSEP SUPPORTED PUBLICATIONS:

1. M. Kniffin and C. R. Helms, *J. Vac. Sci Technol.* **A5** 1511 (1987).
2. K. B. Kim, M. Kniffin, R. Sinclair, and C. R. Helms, presented at 1987 AVS meeting, Anaheim, CA.
3. C. E. McCants, T. Kendelewicz, P. H. Mahowald, K. A. Bertness, M. D. Williams, I. Lindau, and W. E. Spicer, presented at 1987 AVS meeting, Anaheim, CA.

Ph.D. DISSERTATION: M. D. Williams, "The Effect of Chemical Reactivity and Charge Transfer on Gallium Arsenide (110) Schottky Barrier Formation," Stanford University, Physics Department, December 1986.

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Unit 3

TITLE: The Study of Crystal Properties Using Channeling Radiation

SENIOR PRINCIPAL INVESTIGATOR: R. H. Pantell

POST DOCTORAL FELLOW: Alan S. Fisher

**GRADUATE STUDENTS: Charles Gary, Meric Ozcan, Jae Kim,
Xiaoyu Yang**

SCIENTIFIC OBJECTIVE:

The purpose of the program is to investigate the properties of crystals in which channeling occurs. In previous work we have used this technique to measure crystalline potentials, to observe the effect of nitrogen platelets on the diamond lattice, to observe and quantify electron-induced damage effects in certain materials, to determine thermal vibrational amplitudes, and to measure channeling lengths in III-V compounds, alloys and superlattices. Future research will involve studies of defects and properties of electronic semiconductors, channeling investigations of strained superlattices, and observations of damage effects in semiconductors.

SUMMARY OF RESEARCH:

A channeling radiation beamline has been installed at Stanford University to replace the line that was formerly available at the Lawrence Livermore National Laboratory. This effort has been funded primarily by the Air Force Office of Scientific Research, to obtain a source of hard x-rays from channeled particles. The JSEP program provides an important increment in funding to allow this considerable investment in capital equipment to be used for studies of electronic semiconductors.

Figures 1 and 2 illustrate the main features of the channeling beamline that has been constructed. Between the two figures, i.e. to the left of Fig. 1 and to the right of Fig. 2, there are about two meters of straight pipe which is not shown. In Fig. 1, the electrons

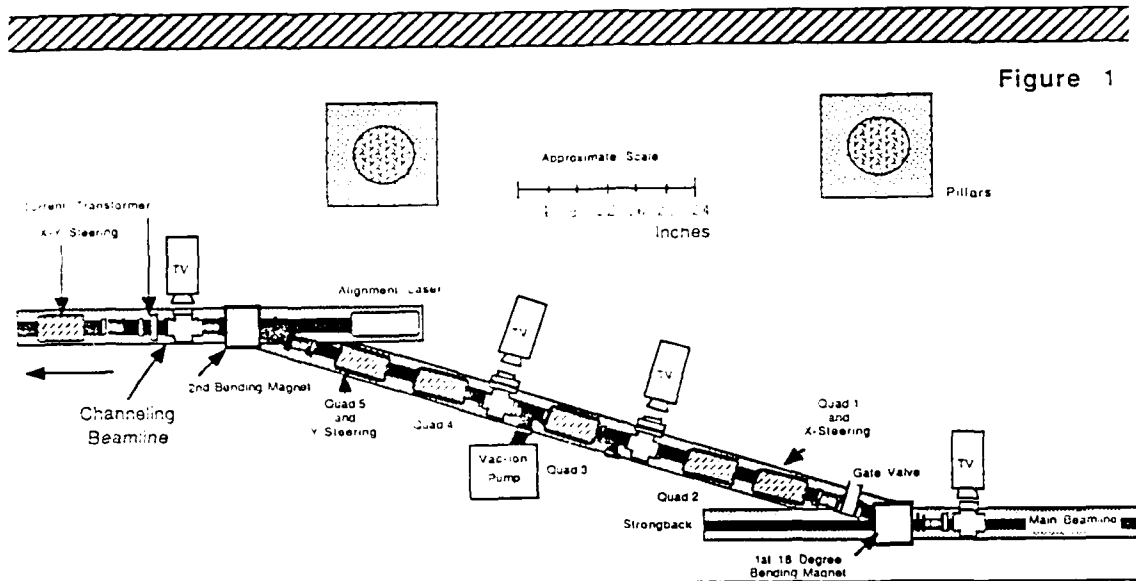


Figure 1

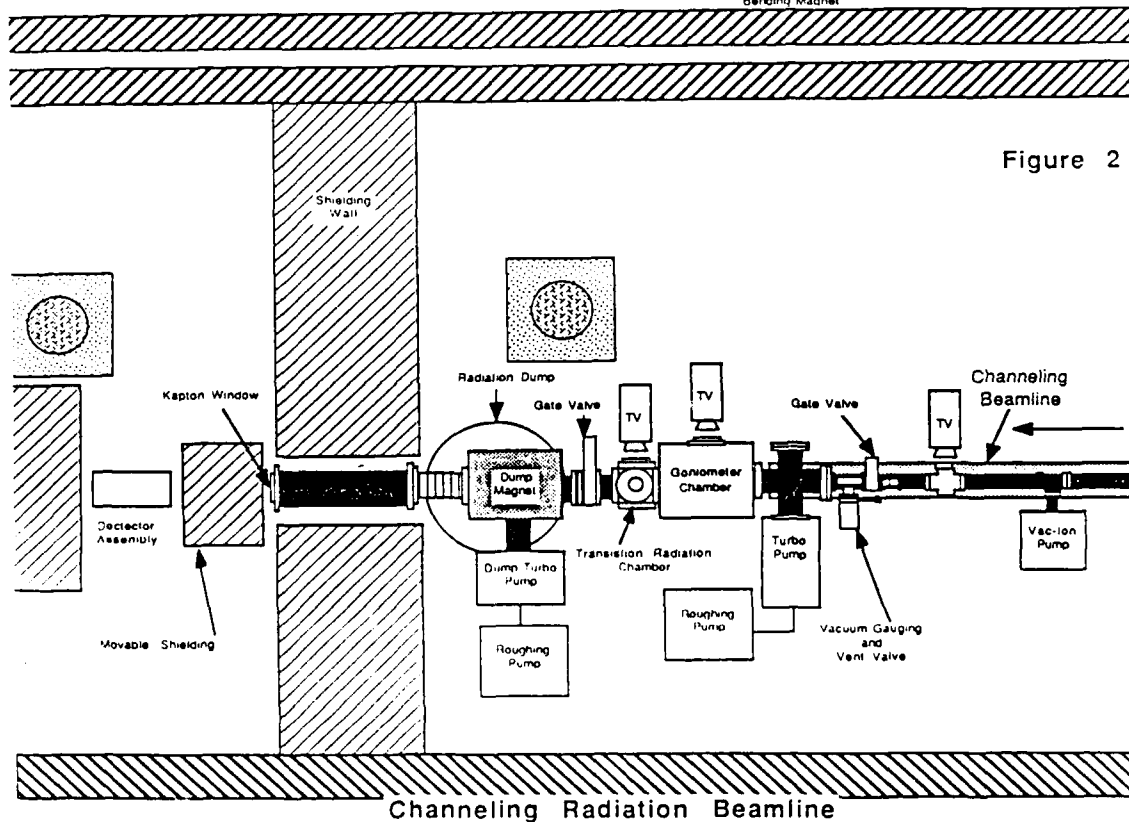


Figure 2

enter from a 40 MeV linac located to the right of the figure, and pass through an 18° bend into a dog leg containing focusing and steering magnets. The magnets were designed using the TRANSPORT code developed at SLAC. Two retractable phosphor screens, monitored by TV cameras, are located in this line to determine the size and position of the beam as a function of the magnet settings.

The electrons then pass through another bending magnet to enter the channeling beamline, the continuation of which is shown in Fig. 2. This line contains the goniometer in which the channeling crystal is mounted, the dump magnet for removing the electron beam from the path of the emitted radiation, several vacuum pumps, and viewing ports and screens with accompanying TV cameras. Downstream from the beam dump is the radiation detector assembly consisting of a Bragg crystal and photomultiplier tube. With this beamline facility we have recently measured x-ray channeling radiation from crystal planes of silicon.

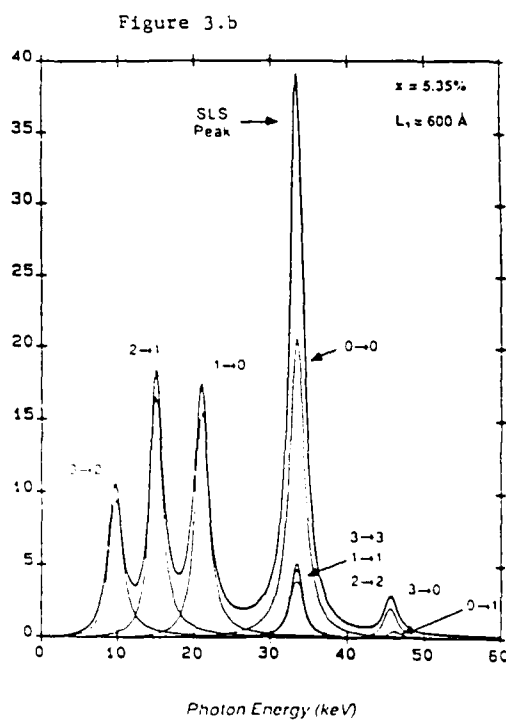
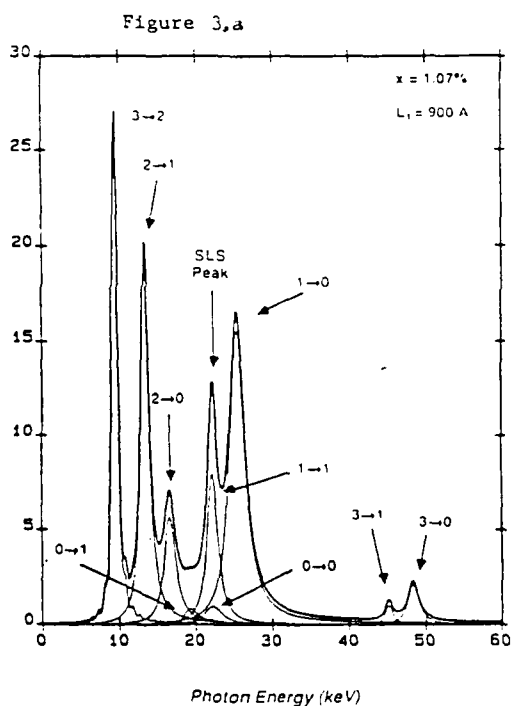
Several components of the beamline system remain to be completed. As yet, we do not have a satisfactory photon detector system. We are able to obtain a channeling spectrum by pulse-height analysis, using a scintillator and photomultiplier tube, but because of the low repetition rate (15 Hz) at least several hours are required for a reasonable signal-to-noise level. An alternative approach is to employ an energy filter such as a Bragg reflection crystal. The silicon crystal we have used, however, has too narrow an energy acceptance, thereby reducing the desired signal below the background noise. A graphite crystal has been ordered, which will increase the signal by 2-3 orders of magnitude and thus should operate satisfactorily. Another system component that has yet to be completed is the control software and associated electronics. The primary functions to be controlled are two angles of the goniometer on which the crystal is mounted, and the orientations of the Bragg reflection crystal and photomultiplier.

The electron beam that we will have at Stanford is superior to the beam that was available at the Lawrence Livermore National Laboratory. Channeling peaks will be more distinct because of smaller beam spot size and divergence. If the beam is operated at maximum intensity a significant defect concentration will be generated on a time scale of tens of minutes, allowing a monitoring of electron-beam induced defects as they form in superlattices and other materials by measuring the channeling radiation spectrum as a function of time.

Once the beamline system has been completed, we will explore the properties of strained and compositional superlattices. In our

previous experimental work at Livermore we achieved channeling in superlattices, and our theoretical work indicates that channeling radiation spectra should provide information on strain, interface quality, and periodicity.

Figure 3 shows calculated radiation spectra for 20-MeV electrons channeled by a (110) plane of a $\text{Si}_{1-x}\text{Ge}_x/\text{Si}$ strained superlattice (SLS). The normal to the (110) plane makes a 45° angle with the growth direction. In Fig. 3.a, the layer thickness of the superlattice is 900\AA and the Ge concentration is 1.1%.



A new peak appears in the spectrum at an energy of 22.3 keV, which is associated with the crossing frequency of the interfaces. Since our energy resolution is typically 1% or better, we ought to be able to measure the layer thickness of superlattices to this accuracy. The intensity of this extra "SLS peak" is determined by the Ge concentration in a somewhat more complicated (but calculable) way. In Fig. 3.b, the layer thickness has been decreased to 600Å, causing the peak to move up in energy by 50% to 33.4 keV. The Ge concentration has been taken to be five times greater than that in Fig. 3.a, causing the intensity of the SLS peak to increase significantly. These calculations indicate that channeling radiation spectra from strained-layer superlattices are extremely sensitive to the layer thickness and the dopant concentration. Additional theoretical work will be needed in order to incorporate the effects of defects into the calculation, but it is evident from our previous experiments on compositional superlattices that defects at the interface also have a direct, measurable effect on channeling radiation spectra.

JSEP SUPPORTED PUBLICATIONS:

1. S. Datz, B.L. Berman, B.A. Dahling, M.V. Hynes, H. Park, J.O. Kephart, R.K. Klein, R.H. Pantell, "On the Dependence of Electron Planar Channeling Radiation upon Lattice Vibration Amplitude," *Nuclear Instruments and Methods in Physics Research*, North-Holland, Amsterdam, **B13**, 19-22 (1986).
2. H. Park, J.O. Kephart, R.K. Klein, R.H. Pantell, M.V. Hynes, B.L. Berman, B.A. Dahling, S. Datz, R.L. Swent and M.J. Alguard, "Temperature Dependence of Planar Channeling Radiation," *Phys. Rev. B*, **35**, No 1, 13-17 (1987).
3. H. Park, J.O. Kephart, R.K. Klein, R.H. Pantell, B.L. Berman and S. Datz, "Channeling Radiation from GaAs," *Phys. Rev. B*, **36**, No 2, 1259-1261 (1987).
4. B.L. Berman, J.O. Kephart, R.H. Pantell, S. Datz, H. Park, R.K. Klein, and B.A. Dahling, "Channeling-Radiation Experiments between 10 and 100 MeV", *NATO ASI Series (B)*, Physics Vol. **165**, Relativistic Channeling, 239-270, (1987).
5. R.H. Pantell, J.O. Kephart, R.K. Klein, H. Park, B.L. Berman, and S. Datz, "The Study of Material Properties Using Channeling Radiation," *NATO ASI Series (B)*, Physics Vol. **165**, Relativistic Channeling, 435-454, (1987).

6. W. Beezhold, T.W.L. Sanford, H. Park, J.O. Kephart, R.K. Klein, R.H. Pantell, B.L. Berman and S. Datz, "Observation of Positron and Electron Channeling Radiation from Tungsten Crystals: Determination of Channeling Occupation Length," submitted to *J. Appl. Phys.*
7. J.O. Kephart, R.H. Pantell, B.L. Berman, S. Datz, H. Park, and R.K. Klein, "Measurement of the Occupation Lengths of Channeled 17-MeV Electrons and 54-MeV Electrons and positrons in Silicon by Means of Channeling Radiation", submitted to *Phys. Rev. B.*

Ph.D. DISSERTATION:

J.O. Kephart, "Beyond the Continuum Potential Approximation: Channeling Radiation from Nonideal Crystals," Stanford University Ph.D. thesis 1987.

Unit 4

TITLE: Complementary MOS Device and Material Physics at 77 Degree K

SENIOR PRINCIPAL INVESTIGATORS: J. D. Plummer and K. C. Saraswat

GRADUATE STUDENTS: A. Henning, T. Schreyer, J. Watt, J. Woo

SCIENTIFIC OBJECTIVES:

The overall objective of this work is to investigate the fundamental physics of operation and potential for VLSI circuits, of silicon CMOS devices operated at 77 K.

Our work in the past year has concentrated on four areas: experimental measurement and modeling of MOS and bipolar device characteristics at low temperature, measurement and modeling of hot carrier effects at low temperature; optimization of MOSFET devices and technology for cryogenic operation; and measurement and modeling of contact resistances at low temperature. Progress in each of these areas is described below.

SUMMARY OF RESEARCH:

A. MOS DEVICE PHYSICS AT LN₂

Accurate predictions of the performance of CMOS circuits as a function of temperature are necessary to assess the viability of a liquid nitrogen cooled CMOS technology. The performance of a circuit is determined by the MOS device characteristics as well as the properties of the load being driven and can be maximized through optimization of the technology for the particular temperature of operation. Both optimization of the technology and performance estimation require accurate prediction of device and circuit characteristics.

The intrinsic speed of MOS devices is determined by the transport properties of electrons and holes in the surface inversion layer. It is therefore necessary to have accurate models for carrier

transport in order to design a device structure which will maximize circuit speed at liquid nitrogen temperature. In addition, such models are needed to accurately predict circuit performance. Experiments are in progress to determine the dependence of the fundamental transport parameters - low field mobility and saturated drift velocity - on temperature, substrate dopant concentration and electric field. A new technique was developed to accurately extract values of surface mobility from measured, large geometry MOS transistor characteristics. The inversion layer mobility of electrons and holes has been examined over a wide range of substrate doping, substrate bias and anneal conditions. The room temperature results, presented at the 1987 Symposium on VLSI Technology, verified the existence of a universal mobility-field relationship for electrons and demonstrated, for the first time, the existence of a similar relationship for holes. A surface mobility model based on these universal curves has been developed and implemented in the two-dimensional device simulator PISCES. This simulator now has the capability to accurately predict MOS device behavior and can be used to optimize the device structure for high performance at 77°K and predict the resulting electrical characteristics.

The principal benefit of liquid nitrogen temperature CMOS circuit operation is enhanced performance; ring oscillator delays are typically observed to decrease by a factor of two between 300°K and 77°K. This improvement is due to both the increase in MOSFET drive current and the decrease in source/drain junction capacitance as temperature is reduced. While the improvement in ring oscillator performance is well understood and modeled, the performance of realistic circuits with significant interconnect delays has not been examined. The improvement in bulk aluminum resistivity by a factor of 13 between 300°K and 77°K has led to some speculation that substantial performance improvements may be obtained in interconnect delay dominated circuits. However, speed improvements in VLSI CMOS circuits operated at liquid nitrogen temperature have been consistently observed to be close to a factor of two. In an effort to understand these results a model has been developed to predict the propagation delay of an interconnect driven by cascaded drivers. This model has then been used, along with

measured aluminum thin film resistivities, to study the propagation delays of typical room temperature and liquid nitrogen temperature 0.8 micron CMOS processes. The results of this investigation, which will be presented at the 1987 International Electron Devices Meeting, indicate that the driver resistance, rather than the interconnect resistance itself, limits performance and the improvement in delay time achieved through low temperature operation is close to a factor of two irrespective of interconnect length. Upon the completion of the temperature dependent surface mobility characterization and PISCES model development, accurate prediction of performance of scaled low temperature CMOS technologies will be possible.

B. HOT CARRIER EFFECTS AT LOW TEMPERATURES

Silicon is the material of choice for fabrication of high density integrated circuits. CMOS technology provides the additional advantage of low power dissipation. These features make CMOS technology an attractive candidate to take advantage of the performance enhancements available through liquid nitrogen temperature operation. However, low temperature operation may increase the hot carrier generation of both substrate and gate currents - which can degrade device performance and reliability.

During the past year, a Ph.D. dissertation has been completed which describes the advantages and drawbacks of cryogenic device operation. Hot carrier effects are discussed in detail, since they prove detrimental to operation at both normal and cryogenic temperatures. In particular, characterization of the temperature, channel length, and voltage dependences of the weak avalanche substrate current between 77°K and 300°K is presented. A microscopic, physical model based on Shockley's lucky electron approach is described which explains this impact ionization behavior. The model incorporates a Maxwell-Boltzmann distribution of hot carrier energies beyond the band minima, and is implemented in the 2-D device simulators CADDET and PISCES. Specific tools have been developed in PISCES for analyzing hot carrier effects, using the results of this model.

Device gate current in short-channel NMOS FET's has also been characterized at low temperatures and realistic biases. The

measurements have implications for gate current modeling, device reliability, and reliability modeling. These implications are discussed in detail in the thesis, and specific, quantitative suggestions are made on the necessary attributes for a 2-D gate current model.

C. BIPOLAR DEVICE PHYSICS AT LOW TEMPERATURES

During the past year a second PhD dissertation on the physics of bipolar operation at low temperatures has also been completed. Bipolar transistors have traditionally been considered not useful at low temperatures. This dissertation examines the temperature dependence of bipolar transistors and shows experimentally that recombination mechanisms play a substantially larger role in determining base current at lower temperatures. The results are explained and quantitatively modeled using the conventional Shockley-Read-Hall theory, with the addition of the Poole-Frenkel high field effect. It is concluded that trap levels in the silicon bandgap due to bulk traps or interface states are very important in determining bipolar transistor base currents at low temperatures. Non-ideality factors larger than 2 are often observed. Such trap levels will have to be carefully controlled if low temperature operation of bipolar transistors is to be considered.

Bipolar transistors designed specifically for operation at 77°K are also discussed in this thesis. It is concluded that for high gain, high performance, low temperature bipolar transistors, the emitter concentration should be around $5 \times 10^{15} \text{ cm}^{-3}$. Compensating impurities in the base should be kept to a minimum. Test bipolar transistors with polysilicon emitter contacts were fabricated using these criteria. The devices show very little current degradation between room temperature and 77°K. Polysilicon emitter contacts are also shown to be somewhat more effective at lower temperatures.

D. CONTACT RESISTANCE AND INTERCONNECT RESISTANCE AT LOW TEMPERATURES

Etching SiO_2 in a CHF_3 plasma is an effective method used to etch contact holes. Very small dimensions can be obtained, and high (~15:1) etching selectivity over Si is possible. The high selectivity

is possible because this particular chemistry deposits fluorocarbon polymers on any bare silicon, thereby inhibiting the etching of the silicon. While this is advantageous during processing, it is obviously detrimental to the operation of electrical contacts.

In this work, the effect of polymer build-up on contact resistivity was examined. It was found that the polymer caused resistivity to be as high as 2×10^{-5} ohm-cm². After forming the contact holes, some of the contacts were cleaned in a NF₃/Ar plasma. This reduced the resistivity into the low 10⁻⁷ range. Similarly, contacts which were not cleaned in NF₃, but received a 350° anneal, were found to be in the low 10⁻⁷ range. Finally, contacts which received both the NF₃ clean-up etch as well as an anneal, had a resistivity in the low 10⁻⁸ ohm-cm² range.

Remaining work on this project involves obtaining chemical analysis of the polymer deposited. Furthermore, this etch is known to cause damage in the silicon layer, so it is necessary to examine the effect it has on leakage currents.

JSEP SUPPORTED PUBLICATIONS:

1. J. C. S. Woo and J. D. Plummer, "Short Channel Effects in MOSFETs at Liquid Nitrogen Temperature, *IEEE Trans. Elec. Dev.*, **ED-33**, No. 7, pp. 1012-1019, July 1986.
2. A. K. Henning, N. N. Chan, J. T. Watt and J. D. Plummer, "Substrate Current at Cryogenic Temperatures: Measurements and a Two-Dimensional Model for CMOS Technology," *IEEE Tran. Elect. Dev.*, Vol. **ED-34**, No. 2 pp. 64-74, January 1987.
3. J. T. Watt, B. J. Fishbein and J. D. Plummer, "A Low-Temperature NMOS Technology With Cesium-Implanted Load Devices," *IEEE Trans. Elec. Dev.*, Vol. **ED-34**, pp. 28-38, January 1987.
4. J.C.S. Woo, J. D. Plummer and J.M.C. Stork, "Non-Ideal Base Current in Bipolar Transistors at Low Temperature," *IEEE Trans. Elec. Dev.*, **ED-34**, No. 1, pp. 130-138, January 1987
5. T. A. Schreyer and K. C. Saraswat, "A Two-Dimensional Analytical Model of the Cross-Bridge Kelvin Resistor," *IEEE Elec. Dev. Letts.*, Vol. **EDL-7**, No. 12, pp. 661-663, December 1986.

6. W. M. Loh, S. E. Swirhun, T. A. Schreyer, R. M. Swanson and K. C. Saraswat, "Modeling and Measurement of Contact Resistances," *IEEE Trans. Elec. Dev.*, Vol. **ED-34**, No. 3, pp. 512-524, March 1987.

JSEP SUPPORTED PRESENTATIONS:

1. J. D. Plummer, "Prospects for Cooled MOS Devices and Circuits," invited paper presented at March 1987 American Physical Society Meeting, New York.
2. J. T. Watt and J. D. Plummer, "Universal Mobility Field Curves for Electrons and Holes in MOS Inversion Layers," 1987 VLSI Symposium Karuizawa, Japan, May 1987.
3. T. A. Schreyer, P. J. Wright and K. C. Saraswat, "The Effect of a Superconducting Interconnect on Circuit Performance," IEEE Device Research Conference (Santa Barbara, CA), June 1987.
4. T. A. Schreyer, A. J. Bariya, J. P. McVittie and K. C. Saraswat, "Specific Contact Resistivity Measurements of RIE Etched Contacts Symposium of the American Vacuum Society (Anaheim, CA) November 1987. (Proceedings to be published in the Journal of Vacuum Science and Technology, May 1988.)

UNIT 4(a)

TITLE: Real Time Statistical Signal Processing

PRINCIPAL INVESTIGATORS: T. Kailath, J. Cioffi

VISITING SCHOLARS: A. Paulraj, V. U. Reddy

POSTDOCTORAL FELLOW: Y. Bresler

GRADUATE STUDENTS: T. J. Shan, R. Roy

SCIENTIFIC OBJECTIVES:

The goals of this research program have been to study the emitter location problem and in particular focus on new techniques that have computational and performance advantages over existing methods. Another area of interest is to develop subspace (MUSIC) approaches to handle problems such as coherent interference, unknown noise fields, etc.

SUMMARY OF RESEARCH

A. ESPRIT - A New Approach to DOA Estimation

A new approach has been developed to the directions-of-arrival (DOA) estimation problem. This technique (which we call ESPRIT - Estimation of Signal Parameters by Rotational Invariance Technique) has some significant advantages over all the previous approaches to DOA estimation, subject to certain assumptions on the array geometry: pairwise-matched co-directional sensor doublets in far field (uniform linear arrays certainly qualify). The most important advantages are:

1. Given a certain array displacement structure the algorithm does not require knowledge of the array geometry and element characteristics (i.e., directional pattern or gain/phase response) and therefore does not need array calibration and the associated storage of such data.

2. It is computationally much less complex because it does not need the search procedure inherent in all the earlier methods.
3. ESPRIT substantially outperforms MUSIC in the low information content (low SNR/low data) situations where MUSIC has particular difficulty. Above the information threshold, MUSIC improves considerably and the advantages of ESPRIT then reduce to providing apparently unbiased estimates, while those of MUSIC still have a small bias that vanishes only asymptotically.
4. Extensive simulation studies have been performed comparing ESPRIT, MUSIC and ROOT-MUSIC. Results indicate that the performance of ROOT-MUSIC and ESPRIT is the same (in terms of lack of bias and sample variances) in the presence of only additive measurement noise. However, when random errors in the sensor gain, phase and positions are introduced, ROOT-MUSIC manifests severe degradation and the failure rate of MUSIC increases dramatically. ESPRIT exhibits remarkable robustness against array perturbations and degrades slowly as the modeling errors increase.
5. Recently a new formulation of ESPRIT has been developed. The Total Least-Squares (TLS) estimation concept is the basis of a new TLS-ESPRIT algorithm. The DOA estimates appear to be unbiased for even lower information to noise ratios with this new method. More extensive simulation studies on TLS-ESPRIT are currently being performed.

Papers on ESPRIT have appeared in the *Proc. IEEE* in July 1986 and *IEEE Trans. on ASSP*, October 1986. Two other notes submitted to the *IEEE* are under review. Conference papers describing ESPRIT have been presented at the 1986 ICASSP, the 20th Asilomar Conference held in November 1986, and the 1986 Platinum Jubilee Conference in Bangalore, India.

B. DOA Estimation in the Presence of Coherent Signals

T. J. Shan completed his Ph.D. thesis during this period, "Array Processing for Coherent Sources". A spatial smoothing solution to the coherent interference problem was developed and performance

analysis of the smoothing algorithm is presented.

The abstract of his thesis follows.

Since the early sixties, there has been considerable activity in the development of adaptive arrays for radar, sonar, communication, spectral estimation, etc. A key assumption in all previous work on adaptive beamforming is that the interfering signals are not coherent with the desired signal (i.e., one is not a scaled and delayed replica of the other). Coherence can completely destroy the performance of an adaptive array system. This is also the case for the recently developed high resolution methods, such as Maximum Entropy method, Minimum Variance method and eigenstructure method, for the localization of multiple sources. In practice coherent receiving environments often exist; for example, coherent interference can arise when multipath propagation is present, or when 'smart' jammers deliberately introduce coherent interference.

In this thesis we present a new processing scheme, applicable to the Maximum Entropy, the Minimum Variance and the eigenstructure methods, that will retain their high resolution performance regardless of the coherence of the sources. The robustness to the coherence of the sources is achieved by spatial-smoothing; the array is divided into overlapping subarrays, and a smoothing operation is performed in the spatial-domain. Based on the spatial-smoothing idea, we also introduce a new adaptive beamformer able to work well even when the desired signal and the interference are coherent. The new adaptive processor uses both spatial and temporal sample data to overcome the degradation of performance in coherent receiving environments; it is also a cure for signal cancellation phenomenon in adaptive arrays.

A statistical procedure called smoothed rank profile (SPR) test for determining the source coherent structure and the solvability of DOA estimation problem is proposed in the thesis.

In the thesis, an extension of the eigenstructure method is given for the case of incomplete information on the assumed signal subspace. A "signal implantation" technique is introduced to cope with the uncertainty model that accounts for phase and gain

perturbations in sensors as well as for inaccurate knowledge of sensor positions in DOA estimation.

The last topic of the thesis is the overlapping echoes separation problem. A eigenstructure based method is suggested for estimating the number and arrival time of overlapping echoes with a priori known shape, from noisy observations received by a sensor.

Several papers on the above thesis have already appeared, including [4]. A paper on the effect of spatial smoothing on DOA estimation performance has been submitted to *Trans. ASSP*. In related work, the effect of source correlation on optimum beamformers has been studied in the paper [3], appearing in the *IEEE Trans. Oceanic Engineering*. Two papers on related topics: beamforming in presence of multipath, and optimum beamforming for coherent signal and interferences have been submitted for publication.

C. Other Applications of Eigenstructure Methods

The eigenstructure methods have been applied to several new problems and have yielded encouraging results. The techniques developed in DOA estimation have direct applications in time series analysis. As an example, ESPRIT was successfully applied to the identification of a flexible robot arm, a problem that had not been amenable to more traditional identification methods.

Another study [9] addresses means of calibrating the sensor gain and phase of an array by exploiting a priori information on the DOAs of one or more sources in the presence of other sources whose DOAs may be unknown.

The publications list several papers on related ideas that arose in the course of our research.

D. Summary of Results

- A new approach to DOA estimation using a subspace rotation approach (ESPRIT, TLS-ESPRIT).
- A spatial smoothing technique to handle coherent interference

and a new subtraction method to handle unknown noise fields.

- Several new applications of subspace techniques to time series analysis, identification, calibrating the sensor gain and phase of an array exploiting a priori information, etc.

JSEP SUPPORTED PUBLICATIONS:

1. A. Paulraj, R. Roy and T. Kailath, "A Subspace Rotation Approach to Signal Parameter Estimation," *Proc. IEEE*, Vol. **74**, no. 7, pp. 1044-1046, July 1986.
2. R. Roy, A. Paulraj and T. Kailath, "ESPRIT -- A Subspace Rotation Approach to Estimation of Parameters of Cisoids in Noise," *IEEE Trans. ASSP*, Vol. **ASSP-34**, no. 5, pp. 1340-1344, October 1986.
3. A. Paulraj, V. U. Reddy and T. Kailath, "Analysis of Signal Cancellation Due to Multipath in Optimum Beamformers for Moving Arrays," *IEEE Trans. Oceanic Engineering*, special issue on Underwater Acoustic Signal Processing, Vol. **OE-12**, no. 1, pp. 163-172, January 1987.
4. T. J. Shan, A. Paulraj and T. Kailath, "On Smoothed Rank Profile Tests in Eigenstructure Approach to Directions-of-Arrival Estimation," *IEEE Trans. ASSP*, Vol. **ASSP-35**, no. 10, pp. 1377-1385, October 1987.
5. A. Paulraj and T. Kailath, "Direction of Arrival Estimation by Eigenstructure Methods with Imperfect Spatial Coherence of Wavefronts," *J. Acoust. Soc. of America*, March 1988.
6. V. U. Reddy, A. Paulraj and T. Kailath, "SINR Performance of the Minimum Variance Beamformer in The Presence of Correlated Interference," *International Symposium on Electronic Devices, Circuits and Systems*, India, December 1987. Also submitted *IEEE Trans. Antennas and Propagation*.
7. T. J. Shan and T. Kailath, "Adaptive Algorithms With An Automatic Gain Control Feature," *IEEE Trans. Circuits and Systems*, 1988.
8. Y. Yoganadam, V. U. Reddy and T. Kailath, "Performance Analysis of the Adaptive Line Enhancer for Sinusoidal Signals in Broadband Noise," *IEEE Trans. ASSP*, 1988.
9. A. Paulraj and T. Kailath, "Direction of Arrival Estimation by Eigenstructure Methods with Unknown Sensor Gain and Phase,"

IEEE Trans. ASSP.

10. Y. Bresler, T. Kailath and A. Macovski, "Model Based Tracking of Signal Shift and Shape," *Automatic Control and Production System*, special issue on *Modeling-Identification Techniques in Signal Processing*.
11. Y. Bresler, T. Kailath and A. Macovski, "Tracking of Shift and Shape Parameters," *IEEE Trans. on Automatic Control*.
12. V. U. Reddy, A. Paulraj and T. Kailath, "Performance Analysis of the Optimum Beamformer in the Presence of Correlated Sources and Its Behavior Under Spatial Smoothing," *IEEE Trans. ASSP*.
13. A. Paulraj, V. U. Reddy, T. J. Shan and T. Kailath, "Performance Analysis of the MUSIC Algorithm with Spatial Smoothing in the Presence of Coherent Sources," *IEEE Trans. ASSP*.
14. A. Paulraj and T. Kailath, "On Beamforming in Presence of Multipath," *IEEE Trans. Ant. and Prop.*, July 1985.
15. Y. Bresler, V. U. Reddy, and T. Kailath, "Optimum Beamforming for Coherent Signal and Interferences," *IEEE Trans. ASSP*.

PH.D. DISSERTATION

1. T. J. Shan, "Array Processing for Coherent Sources," Ph.D. Dissertation, Stanford University, Department of Electrical Engineering, December 1986.

JSEP SUPPORTED PRESENTATIONS:

1. D. Spielman, A. Paulraj and T. Kailath, "Performance Analysis of the MUSIC Algorithm," *ICASSP 1986*, pp. 1909-1912, Tokyo, Japan, April 1986.
2. A. M. Bruckstein, T. J. Shan and T. Kailath, "A Time-Domain Signal Resolution Problem," *ICASSP*, pp. 1665-1668, Tokyo, Japan, April 1986.
3. A. Paulraj, V. U. Reddy, T. J. Shan and T. Kailath, "Performance Analysis of the MUSIC Algorithm with Spatial Smoothing in the Presence of Coherent Sources," *MILCOM 1986*, Monterey, CA, October 1986.
4. R. Roy, A. Paulraj and T. Kailath, "Comparative Performance of ESPRIT and MUSIC for Direction-of-Arrival Estimation," Twentieth Annual Asilomar Conference on Signals, Systems and Computers, Pacific Grove, CA, November 1986
5. V. U. Reddy, A. Paulraj, T. J. Shan and T. Kailath, "Modified Capon's

Beamformer for Coherent Interference," Twentieth Annual Asilomar Conf. on Signals, Systems and Computers, Pacific Grove, CA, November 1986

6. R. Roy, A. Paulraj and T. Kailath, "Estimation of Signal Parameters via Rotational Invariance Techniques - ESPRIT," *Proc. Platinum Jubilee Conference on Systems and Signal Processing*, pp. 207-214, Bangalore, India, 1986.
7. T. J. Shan and T. Kailath, "Directional Signal Separation by Adaptive Arrays with a Root-Tracking Algorithm," *ICASSP-87*, pp. 2288-2291, Dallas, TX, April 1987.
8. D. T. Slock, J. M. Cioffi and T. Kailath, "A Fast Transversal Filter for Adaptive Line Enhancing," *ICASSP-87*, pp. 419-422, Dallas, TX, April 1987.
9. R. Roy, A. Paulraj and T. Kailath, "Comparative Performance of ESPRIT and MUSIC for Direction-of-Arrival Estimation," *ICASSP-87*, pp. 2344-2347, Dallas, TX, April 1987.
10. Y. Bresler, V. U. Reddy and T. Kailath, "A Polynomial Approach to Optimum Beamforming for Correlated or Coherent Signal and Interference," *ICASSP 87*, pp. 2292-2295, Dallas, TX, April 1987.

Unit 4(b)

TITLE: Coding for Spectrally Constrained Channels

PRINCIPAL INVESTIGATOR: J. Cioffi

GRADUATE STUDENTS: J. Aslanis, S. Kasturia, A. Ruiz

SCIENTIFIC OBJECTIVES:

Our objective is the design of codes for channels with severe intersymbol interference. This problem has been of growing significance in telecommunications, motivated by two main application areas: the efficient use of subscriber loops and mobile radio channels for wideband digital telecommunications.

Our work in the last year has produced two new code design methods for channels with spectral constraints. These methods have been used to design codes that come very close to theoretical limits (capacity) and significantly out perform (3 orders of magnitude better in error rate or 3db in SNR) any previously known techniques for spectrally constrained channels.

SUMMARY OF RESEARCH:

The advent of a ubiquitous digital telecommunications network has motivated recent interest in efficient use of existing (non-fiber) communication-channel media for data transmission. An example is the twisted-copper-pair subscriber loop, on which data rates of 384 kbps, 576 kbps, and perhaps 768 kbps, will be required in the future to sustain transmission of various compressed video, graphics, and teleconferencing services [1]. Another example is wideband digital radio, for which data rates of 280 kbps - 3 Mbps will be required over fading radio channels [2] in future, mobile and wireless communication networks. Spectral constraints on such channels prevent the use of conventional equalization methods, and some significant residual interference must be accommodated by the code designer. While a handful of such design procedures have arisen over the past few years [3-5], none come close to theoretical limits, and an uncoded system can usually be found to perform as well, or in

some common situations even better, than previous coded systems. Codes designed by our new methods significantly out perform existing codes and uncoded systems. We have developed two such coding methods: the first is called "basis-vector coding," the second "frequency-constrained coding."

A. BASIS-VECTOR CODING:

The basis-vector coding is illustrated in Figure 1.

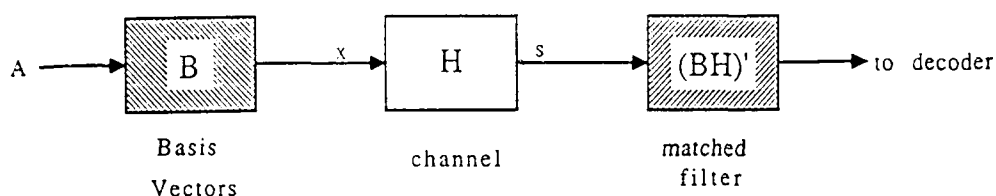


Figure 1 - Basis Vector Coding

The channel is used in a multidimensional sense, in that input symbols are blocked into successive groups of many symbols. Sequences of such blocks will be such that the corresponding sequences of blocks at the channel output will be more disparate than in a very good, uncoded system, thus improving the overall performance. The channel is described by a transfer matrix H . To ensure that any channel memory is not in effect, one can zero enough symbol periods at the end of a block input. In so doing, the new design procedure determines a set of basis vectors for the coder block signal intervals that satisfy the above (zeros) constraint and which correspond to independent or orthogonal signal vectors at the channel output. We can then think of an input code block, A , as projections on these vectors. Our channel is thus, through the use of the coding, orthogonalized into M subchannels, where $M \leq N$, and N

is the number of symbols per block. The gains on each of these channels can be different and a good level assignment for a given channel can be found by assigning equal energy to each of the subchannels (under channel-input power constraint). Then various numbers of bits are assigned to each subchannel to maximize the minimum signal separation within a block at the channel output. Standard, well-known, ISI-assumed-absent coset codes [6] can then be used. The overall coding gain can be substantial, as we see now with a simple example.

An often used channel shaping assumption is that the channel is

$$H(D) = 1-D \quad (1)$$

where $D = e^{-j2\pi fT}$ and f is the frequency while $1/T$ is the symbol rate. The corresponding 6-dimensional channel transfer matrix is

$$H = \begin{bmatrix} 1 & -1 & 0 & 0 & 0 & 0 \\ 0 & 1 & -1 & 0 & 0 & 0 \\ 0 & 0 & 1 & -1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 0 & 1 & -1 \\ 0 & 0 & 0 & 0 & 0 & 1 \end{bmatrix}, \quad (2)$$

where the input and output are 6-dimensional row vectors

$$\underline{y}_k = \underline{x}_k H \quad (3)$$

where \underline{x}_k , the input, has the following form

$$\underline{x}_k = [x_k \ x_{k-1} \ \dots \ x_{k-4} \ 0] \quad k=6m. \quad (4)$$

A collection of basis vectors for \underline{x}_k that satisfy all the desired

properties (not unique and can be determined from Gram-Schmidt decomposition) is

$$\underline{B} = \begin{bmatrix} -.21 & -.37 & -.42 & -.37 & -.21 & 0 \\ -.41 & -.41 & 0 & .41 & .41 & 0 \\ .58 & 0 & -.58 & 0 & .58 & 0 \\ -.71 & .71 & 0 & -.71 & .71 & 0 \\ .79 & -1.37 & 1.58 & -1.37 & .79 & 0 \end{bmatrix} \quad (5)$$

Note \underline{B} contains only 5 vectors, a consequence of the dimensionality loss in avoiding inter-block interference because of the finite-length channel. The input gains to the channel for each of these vectors are

$$\text{input powers} = .536, .667, 1, 2, 7.46 \quad (6)$$

To use a code for 1 bit/symbol transmission, we require 1 bit/symbol (6 symbols) +1 redundant bit = 7 bits per block. A good assignment is:

.536,	2 bits
.667,	2 bits
1.0,	2 bits
2.0,	1 bit
7.46,	<u>0 bits</u>
TOTAL	7 bits

A well-known (8 or 16-state) 4 dimensional coset code [6] can be used to achieve

$$\sigma^2_{\text{coded}} = 4 \sigma^2_{\text{coded}} \quad (7)$$

The required input power is

$$P_{\text{coded}} = (4^2 - 1)/3(.536 + .667 + 1) + (2^2 - 1)/3(2) = 13 \quad (8)$$

The uncoded power is 6. Thus taking the power increase penalty, the overall gain is

$$\text{Gain} = 24/13 = 2.66\text{dB}. \quad (9)$$

Better codes, with greater implementation complexity, have been found. For instance, in Fig. 2, we have plotted gain versus block length for several codes with varying numbers of bits/dimension. For lower numbers of bits per dimension, these codes are substantially more powerful than any previously found (about 3dB better for the same complexity codes). For large bits / T , the gains are only slightly better. Such gain drop for large bits / T has not been justified by theoretical analysis, so there still remains considerable room for additional improvement.

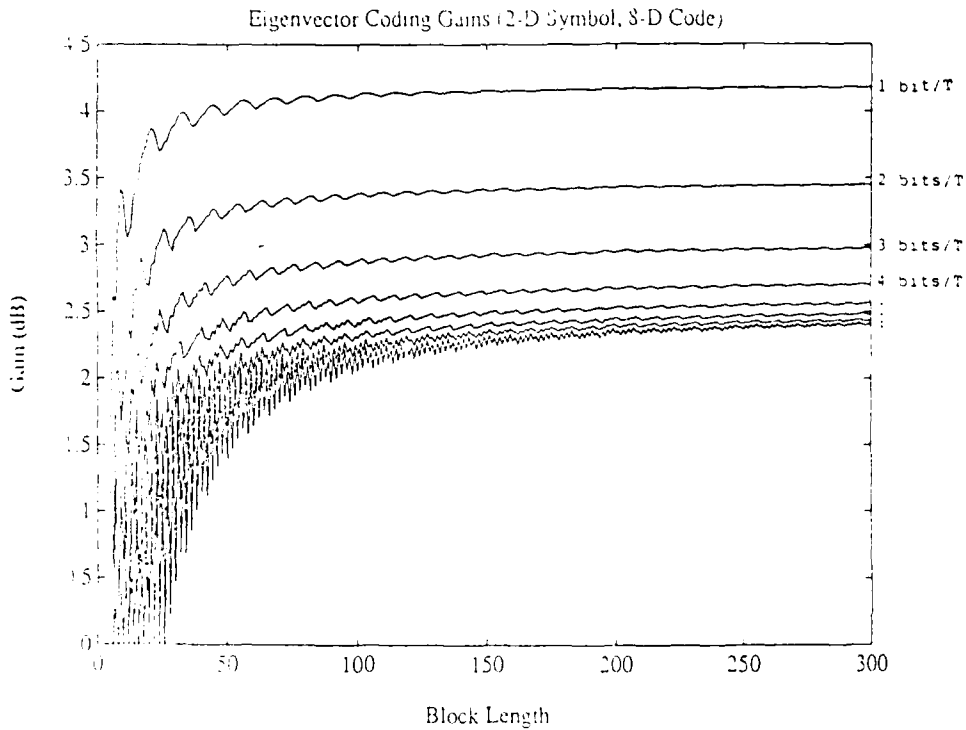


Figure 2 - Gains Versus Block Length For Basis Vector Codes

B. FREQUENCY-CONSTRAINED CODES:

Frequency-constrained codes are illustrated in Fig. 3.

Multitone Signalling

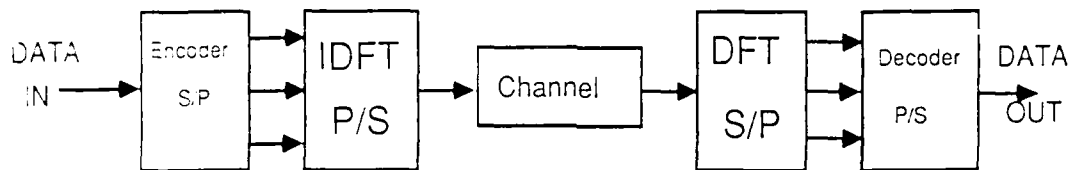


Figure 3 - Frequency-Constrained Codes

The objective here is the same as the basis-vector method, however, a method known as "cyclic extension" is used to create frequency subchannels, to which standard codes are applied. The reader is referred to [c] for more details. An interesting observation is that the extra dimension, nominally sacrificed in basis vector codes to prevent inter-block interference need not be eliminated. This provides a hint of the potential for having high coding gain at high numbers of bits $/T$. Research is ongoing in such improvement. The results of this work are described more fully in the three following publications.

JSEP SUPPORTED PUBLICATIONS:

1. A. Ruiz and J.M. Cioffi, "A Frequency Domain Approach to Combined Spectral-Shaping and Coding," *Int. Conf. on Communications*, June 1987, pp. 1711-1715.

JSEP SUPPORTED PRESENTATIONS:

1. S. Kasturia, J. Aslanis, and J.M. Cioffi, "Basis-Vector Coding for Partial-Response Channels," Submitted, *IEEE 1988 Symposium on Information Theory*
2. A. Ruiz, S. Kasturia, and J.M. Cioffi, "Frequency-Specified Coset Codes for Spectrally-Constrained Channels," Submitted, *IEEE 1988 Symposium Information Theory*.

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1. J. Lechleider, M. Honig and R. Hsing, private communication, Bell Communications Research, November 1987.
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4. G. D. Forney, Jr., "Coset Codes for Partial Response Channels; or, Coset Codes with Spectral Nulls," submitted, *IEEE Trans. on Information Theory*.
5. J. W. Ketchum, "Performance of Trellis Codes for M-ary Partial Response," in *Globecom '87*, pages 1720-1724, Tokyo, November 1987.
6. G. D. Forney, "Coset Codes I: Introduction and Geometrical Classification," 1988, to appear.

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