

AD-A192 197

THE INSPECTION OF ELECTRONIC METALLURGICAL BONDS(U)
ADVANCED RESEARCH AND APPLICATIONS CORP SUNNYVALE CA
B JACKSON ET AL. FEB 88 ARACOR-FR-563-88

1/1

UNCLASSIFIED

NO0014-86-C-0060

F/G 11/6.2

NL



1.0

2.8

1.2

3.15

2.5

1.1

3.5

2.0

4.0

1.8

4.5

1.25

1.4

1.6

AD-A192 197

ARAD



DTIC FILE COPY



THE INSPECTION OF ELECTRONIC METALLURGICAL BONDS

CONTRACT No. N00014-86-C-0860

FINAL REPORT 563-88

FEBRUARY 1988

DTIC
ELECTE
MAR 18 1988
S D

PREPARED FOR:

OFFICE OF NAVAL RESEARCH
ATTN: SCIENTIFIC OFFICER DR. R. C. POHANKA
ARLINGTON, VA 22217-5000

DISTRIBUTION STATEMENT A
Approved for public release
Distribution Unlimited

88 2 26 010

ADVANCED RESEARCH AND APPLICATIONS CORPORATION

THE DETECTION OF FLAWS IN ELECTRONIC METALLURGICAL BONDS

Contract No. N00014-86-C-0860

Final Report 563-88

February 1988

Prepared for:

Office of Naval Research
Attn: Scientific Officer Dr. R. C. Pohanka
Arlington, DC 22217-5000

Prepared by:

Bart Jackson, Jerel Smith, and James Stanley
Advanced Research & Applications Corporation
425 Lakeside Drive
Sunnyvale, CA 94086



Accession For	
NTIS CRA&I	☒
DTIC TAB	☐
Unannounced	☐
Justification	
By <i>per ltr.</i>	
Distribution/	
Availability Codes	
Dist	Avail and/or Special
<i>A-1</i>	

THE DETECTION OF FLAWS IN ELECTRONIC METALLURGICAL BONDS

SUMMARY

The solder bonds in electronic assemblies are an area of increased Non-Destructive Evaluation interest as the number of bonds per assembly increases, the size of the bonds decreases, and the dependence on the bonds for electrical and mechanical performance increases. The current inspection techniques are not detecting many defects, and the inspection techniques are not adequate for the near-term Surface Mount Technology improvements. Computed Tomography is a new NDE technology that is beginning to find its place in industry. The application of CT to electronics solder bond inspections is an area where ARACOR believes there is a good match between special inspection needs and special inspection capabilities. ARACOR has been a leader in the industrialization of CT. The systems that ARACOR has placed in the field, AF/ACTS-I and -II, AFLC/ACTS-I, and ARNIS-I and -II, are producing valuable inspection data for their users in the aerospace industry.

The area where improved inspection techniques are most needed is the emerging Surface Mount Technology product family. This new technology is placing more complicated Integrated Circuit components with a larger number of Input/Output connections closer together by eliminating the through-the-board holes and placing the pins closer together. SMT also includes package designs that use the entire perimeter of the IC, not just two opposite sides. Another advantage of the SMT technique is that, by eliminating the through-the-board holes, it allows the use of both sides of the board for mounting components. This advance in manufacturing technology has not been matched by an improvement in NDE technology.

This project, under the Phase I SBIR contract N00014-86-C-0860, has surveyed the field of printed circuit board manufacturing to determine the types of flaws that need to be detected to improve the reliability of solder bonds in electronic systems. The information about flaw types was used to determine CT system performance requirements for a scanner that could detect these flaws. The performance requirements were used to select several representative objects to be examined with existing CT scanners to verify the ability of a CT scanner to detect these flaws. The scans made during this

project used two standard scanners and a breadboarded prototype scanner to show that CT can detect many of the flaws that need to be found. None of the scanners used provided a complete capability yet all of them were able to detect flaws. This verification of our calculated performance parameters strongly suggests that a CT scanner can fill the inspection needs of the electronics community. ARACOR has developed a conceptual scanner design that addresses the special needs of the solder bond inspection problem. The construction of such a scanner is a challenge to the current state-of-the-art, but is not beyond reasonable extrapolations of existing technology.

ACKNOWLEDGEMENTS

ARACOR would like to thank James Olson of Hewlett-Packard for showing us around a modern SMT factory so that we could better understand the typical production techniques, flaw types, and flaw rates. This visit also helped us understand the current inspection techniques and their limitations. We also thank Charles Williams of Texas Instruments for supplying us with samples of their ceramic leadless chip carriers.

TABLE OF CONTENTS

Section	Page
THE DETECTION OF FLAWS IN ELECTRONIC METALLURGICAL BONDS.....	i
SUMMARY.....	i
ACKNOWLEDGEMENTS.....	iii
TABLE OF CONTENTS.....	iv
LIST OF ILLUSTRATIONS.....	v
1.0 INTRODUCTION AND OBJECTIVES.....	1
1.1 The Bond Inspection Problem.....	2
1.2 Program Objectives.....	3
1.3 Accomplishments and Recommendations.....	3
2.0 SOLDER BONDING TECHNIQUES SURVEY.....	5
2.1 SMT Manufacturing Techniques.....	5
2.2 Flaw Characterization.....	7
3.0 CT SCANNER PERFORMANCE REQUIREMENTS.....	8
4.0 COMPUTED TOMOGRAPHY PERFORMANCE VERIFICATION SCANS.....	13
5.0 CONCEPTUAL DESIGN OF A CT INSPECTION DEVICE.....	20
6.0 CONCLUSION AND RECOMMENDATIONS.....	23

LIST OF ILLUSTRATIONS

Figure		Page
1	AF/ACTS-I image of gull wing IC's.....	14
2	AF/ACTS-I image of ceramic leadless chip carriers.....	15
3	AF/ACTS-I image of SMT circuit boards.....	16
4	Tomoscope breadboard image of a good solder bond.....	18
5	Tomoscope breadboard image of an open solder bond.....	19

1.0 INTRODUCTION AND OBJECTIVES

Electronic systems are being used in more products every day, products ranging from refrigerators to jet fighters. While the sophistication of the electronic controls is rapidly increasing, the reliability of these electronic systems is becoming much more difficult to predict because of the difficulty of inspecting the solder bonds in the electronic assemblies. Solder bonds are becoming smaller and closer together as the complexity of the functions on each Integrated Circuit grows. The design of IC's (particularly VHSIC) and IC packages (for example Surface Mount Technology) has gotten ahead of the inspection techniques that are used to verify that a circuit board has been properly assembled. The ability to place more functions on an IC has brought about the need for more I/O connections per IC, and to the development of IC packages with closer pin spacings. This in turn has forced the pins to be soldered to bonding pads on the component side of the printed circuit board because the conventional through-the-board holes would merge with each other at the close spacings being used. This has led to the development of Surface Mount Technology, or SMT, for designing IC packages and their attachment to the boards. While these circuit board assemblies are built by many manufacturers and used in many systems because of performance advantages, there is no adequate inspection technique for them.

This project has addressed this growing inspection problem facing both military and consumer electronics systems, focusing on Computed Tomography (CT) inspection as the technology to solve the quality control problems of the printed wiring board built with SMT. The project has surveyed printed circuit board manufacturing techniques and the resulting solder bond defects, calculated the CT system performance required to detect these flaws, performed scans using existing CT scanners to verify the required performance parameters, and developed a conceptual design for a CT scanner that can meet the inspection needs of the electronics community.

The successful outcome of the development of a CT inspection system for inspecting solder bonds will provide a benefit both for the government and the consumer worlds. The military has become increasingly dependent on sophisticated electronics to control weapons systems, for communications, and for strategic and tactical surveillance. Improving the reliability of these systems will provide great benefit to the military.

The consumer markets are also using sophisticated electronics in many products. The reliability and price of these products can be strongly influenced by the inspection techniques used during their fabrication. There is a strong desire for an improved inspection modality in the consumer electronics world to improve reliability. We expect that there will be commercial interest in a successful inspection instrument.

1.1 The Bond Inspection Problem

Surface Mount Technology has been introduced as a means of increasing the density of IC connections and reducing the trace lengths between IC's. Higher connection densities allow for more functions per IC and thus fewer IC's and boards, thus improving reliability. Shorter trace lengths allow for higher speed signals by reducing signal degradation.

The previous standard of DIP packaging uses two rows of pins per IC, designed to be attached to a board using through holes, spaced 100 mils apart. The current standardized SMT packages space the pins 50 mils apart, sometimes using the entire perimeter of the IC. The next generation packages are already being designed with spacings of 20 or 25 mils. The use of packages with 10 mil spacing is being planned. In addition there are solder bonds made underneath many SMT IC packages to improve the transfer of heat from the IC to its environment, or to increase the number of I/O connections.

The large number of closely spaced pins, several hundred per IC in some military systems, makes human visual inspection (which currently is the primary technique) impractical. The current alternatives of inspection are to contact the board with a grid of pins that touches all the solder pads, to use an infrared detector to check the thermal properties of each solder pad, or to make a high resolution x-ray radiograph of the board. These techniques will have limited use as solder bond spacings decrease and both sides of the board

are used to mount components, which SMT permits. None of these techniques can adequately inspect bonds made underneath an IC. The only other type of inspection now available is to place the board in use and see if it works. This functional testing is not satisfactory, as it is time consuming and often impractical to evaluate all of the possible logic states of the board. In addition, bond flaws that lead to degradation and early bond failure after time in the field are not found by this functional testing. Examples include cold solder joints, flux residue corrosion of solder joints, and mechanical failure of joints with insufficient solder area. The lack of adequate inspection techniques is limiting the adoption of SMT and its benefits.

1.2 Program Objectives

The goals of this project were to collect information about the types of metallurgical bonds used in current and near term electronic systems, use this information to characterize the types of flaws in the bonds that an inspection system would be required to detect, use the flaw descriptions to generate a set of performance parameters for a CT system that meets the inspection system requirements, and to validate the CT system performance parameters by conducting scans using several different scanners. If this project met with success in verifying that a CT scanner can meet the inspection needs, a conceptual CT scanner design would be developed.

1.3 Accomplishments and Recommendations

This project has been successful. The survey of manufacturing processing techniques (and the flaw types that result) used in the fabrication of printed wiring board assemblies was completed. This information was used to estimate the performance parameters that a CT scanner would need in order to examine SMT board assemblies. The information was also used to select several board assemblies for examination by CT scanners to test our understanding of the capacity of CT inspection to reveal flaws within the limitations of the available CT scanners. The scan results were positive; most flaws that were known to be present were detected despite the performance shortcomings of the scanners that were used.

Our experiments show that, within the limits of the available instruments, the CT inspection technique is very promising. We have developed a concept that we feel can fulfill the requirements. However, before investing in prototype development it is necessary and prudent to demonstrate that all bond flaws have a signature that CT can detect and to experimentally determine the optimum instrument parameters. These experiments will guide the design tradeoffs, and more accurately determine the achievable performance levels.

The next section of this report describes the results of the solder bond flaw survey that was conducted as the first task of this project. This will be followed by a discussion of the performance parameters for a CT scanner to perform the required inspections, the results of the CT verification experiments, the conceptual design of a CT scanner for SMT solder bond inspections, and our conclusions and recommendations.

2.0 SOLDER BONDING TECHNIQUES SURVEY

We surveyed the manufacturing techniques by visiting the Hewlett-Packard facility in Corvallis, Oregon and by reading the literature related to soldering and solder flaw detection. The visit to H-P involved watching the complete solder process, including the inspection of the completed boards. We discussed the flaw detection that H-P achieves and the flaw detection that H-P desires to help us understand the problems involved in SMT soldering.

2.1 SMT Manufacturing Techniques

The primary types of flaws that the program has identified are related to the solder techniques that are used to attach ICs and passive components to the PC boards. A typical procedure is to screen onto the board a solder paste at each bond pad, to place the components onto the board by robot (where they are held by the solder paste or sometimes by glue), and then to apply heat to the board to melt the solder and make the bonds. The board may be heated in a vapor phase system where the entire assembly is heated by freon vapor, or the board may be heated in more localized areas by infrared heaters or by hot air jets directed at the solder pads. These techniques rely on the screening process to apply the correct amount of solder paste to each pad (and only to the pads), the flux in the paste to clean the surfaces for good solder contact, and the heating cycle to properly 'reflow' the solder. The board surface must be clean so that the solder can wet the bonding pads and is not wicked away from the pad by dirt. The screen must not be clogged or misregistered so that each pad receives the proper amount of solder without bridging the gap to any neighboring pad, and the solder paste must have the proper flux content and proper size of solder particles for the reflow process to work properly. In addition the board must be properly cleaned following the soldering process to remove all of the flux, which can cause corrosive failure of what were good solder bonds.

There are several types of IC packages; each has a characteristic lead spacing and lead shape. The Leadless Chip Carrier (LCC) is a package, often ceramic, that has metallization fired into it to act as the connection pads. This design is most often seen in military hardware due to its rugged nature and its low coefficient of thermal expansion. The absence of leads causes problems due to the complete lack of flexibility between the package and the

board. This means that any thermal or mechanical stresses are applied directly to the solder bonds. The fatigue properties of solder are typical of those of any alloy being used near its high temperature limits and thus are not very good. The long term reliability of the circuit boards depends critically on the size and the quality of the solder bonds. The pad spacing on these packages is 50 mil or 25 mil. The pads are most often on all four sides of the package, sometimes in two rows. When there are two rows, the inner row of pads are inspected by leaving an open via to the top of the package that allows a visual inspection of the solder from above.

There are two other package designs that are used in most consumer electronics as well as many military systems. The leads in one of these designs are called 'gull wing'; they are similar to the conventional DIP leads but with a bend away from the package. The package does not need through-the-board holes; it is surrounded by its solder pads. The other SMT design uses 'J' leads that are bent into a curve that brings the end of the lead back under the IC package pointed up away from the board. The bonds are at the perimeter of the package and thus the IC mounting requires less area. These packages are also available in 50 mil and 25 mil pad spacings, and are available both in two sided and four sided configurations.

The passive components, such as resistors and capacitors, are also available in SMT packages. They are often packaged with metallized ends or with leads bent at right angles under the component, similar to 'J' leads but without the radius or the rim that the IC packages have. The bonding areas are sized to match the sizes of SMT IC's so that the solder application techniques will match those used elsewhere on the circuit board.

The boards that are used with SMT have characteristic sizes for the traces, trace separations, and pad sizes. The copper traces are usually at least 40 microns thick by 250 microns wide. The traces are usually laid out with at least 250 microns of separation between traces. The solder bond pads are about half the pad spacing apart or for pins on 50 mil centers the pads are 25 mils apart. The new SMT packages at 20 mil centers will use smaller pads and smaller spacings. If the board has multiple trace layers they are usually spaced apart by at least 100 microns of insulation, often fiberglass. The boards are of many different sizes, mostly between 5" x 8" and 14" x 17".

2.2 Flaw Characterization

The bond flaws, simply stated, are too much solder, too little solder, poor adhesion of the solder (or a crack or void in the solder), solder bridging between pads, a shifted component (causing bridging or insufficient bond area for proper bond strength), incomplete removal of the flux, or the presence of solder balls on the PC board. These flaws are due to various processing errors during the soldering of the board. The solder screening process can be misregistered with the board and cause an improper amount of solder to be present at the solder pads, or a solder bridge to form between two pads. The solder screening can also fail due to bad solder paste or a clogged screen. Bad solder paste can also cause problems with solder adhesion or formation of solder balls if the flux is no longer active. A dirty board may cause poor wetting by the solder, wick the solder away from the solder pad and leave solder balls, bridged connections, or patches of stray solder. The components can be mislocated by the robot or they can shift during the heating cycle and end up with bridged connections or with insufficient solder contact area. The board must be cleaned following the soldering process to remove the solder flux which can cause corrosive failure of bonds or components.

The typical flaw sizes for the improper amount of solder in a bond will be comparable to the trace width, which is 250 microns. The flaw size for a cracked bond or a cold solder joint is reported in the literature as about 10 microns. Solder balls on a board is reported as about 100 microns and larger. Flux residues on a circuit board are found in patches about the same size as the bond pads, which are about 500 microns.

These flaws will show in CT images either as a direct image of the flaw such as a misregistered component or as a pixel (or region of pixels) with an anomalous density. A low density region could be caused by too little solder (or cracked solder) at a joint; a high density region could be caused by flux residue, solder balls, or by too much solder at a joint.

3.0 CT SCANNER PERFORMANCE REQUIREMENTS

An x-ray CT inspection instrument works by collecting many measurements of the x-ray transmission through a plane of an object at different angles. These measurements can be used to reconstruct the pattern of object densities that led to the transmission measurements. The scanner will collect a regular pattern of measurements at equally spaced intervals to provide the desired resolution and contrast sensitivity in the reconstructed image.

The CT parameters to be evaluated were slice thickness, resolution, contrast sensitivity, streak artifacts, and planarity. The slice thickness desired would be thin enough to avoid the circuit board surface with its tinned copper traces. This would concentrate the inspection on the solder bonds and decrease the amount of material other than solder bonds that the x-ray beam would have to penetrate. The resolution desired is fine enough to detect flaws, but coarse enough to permit high inspection throughput. As the pixel size decreases (resolution improves) the scan times increase to preserve the image quality.

The contrast sensitivity is a measure of the image quality, and is often used to determine the detectability of flaws that are smaller than the resolution. A flaw smaller than the resolution may still have a signature due to its influence on the density measured in the pixel containing the flaw. This technique can only be utilized if the contrast sensitivity is high enough to support this density discrimination.

The presence of streaks in an image is often caused by a highly attenuating feature in the object. Another type of image artifact is caused by the polychromatic nature of the brehmstrahlung sources which are used because of their high intensity. As a polychromatic beam passes through an object the low energy photons are preferentially removed first. This leads to the beam becoming progressively more penetrating, or harder. This can lead to a cupping in the reconstructed density of a uniform object or to streak artifacts between highly absorbing features of an object.

The planarity of the circuit board in the scanner will determine whether the solder bonds are in the scan plane. The bonds may wander in and out of the plane due to misalignment of the board in the scanner or lack of flatness of the board.

The resolution of a CT scanner is controlled by the detector element size and the x-ray source spot size in conjunction with the source to detector distance and the accuracy of the object handling system. The image contrast sensitivity is controlled by the source intensity and the accuracy of the detector electronics in measuring a wide range of signals, as well as the amount of time spent per measurement. The throughput of the scanner is determined by the efficiency of the detectors, the x-ray source intensity, and the desired contrast sensitivity.

The information this project has collected about solder bonding in electronic systems was used to derive the performance characteristics of a CT inspection tool for electronic assemblies. The performance specifications cover several areas: image resolution, image contrast sensitivity, image size, slice thickness, planarity, and penetration. These areas are interrelated, a change in the specification of one of these areas will cause changes in the other areas. As an example, if the system resolution is changed the image size will change because the maximum number of pixels is fixed by the available computer system and the size of each pixel has changed.

The two most important parameters of a CT scanner are the resolution and the contrast sensitivity. The resolution and the contrast sensitivity both strongly affect the utility of the scanner, and to some extent they can be traded against each other while preserving the scanners ability to detect flaws. These two parameters interact through the partial volume effect.

The partial volume effect is caused by the finite voxels (volume elements) that are used by the scanner as it collects transmission data about an object. The voxels are often filled nonuniformly, either because the composition of the object is changing or because the object has an edge in the voxel. The scanner data represents the average transmission in a voxel. The a-priori knowledge about an object being inspected can be used to interpret this average value, which can lead to detecting features and flaws that are smaller than the image pixels. If the object is known to be made of one material then any pixel showing a density below that density must be only partially filled, and the decrease in density can be used to determine what

fraction is filled. This can lead to dimensioning an object to better than the pixel size by interpreting the partially filled pixels that define the boundary of the object. The partial volume effect can also be exploited to detect flaws in an object that are smaller than the pixel. Features such as small cracks or voids will decrease the density in a pixel, and this decrease can be used to locate and identify such flaws.

The utility of the partial volume effect is determined by the contrast sensitivity of the scanner, which is determined by the data noise properties of the electronics. The variations in the calculated densities for the pixels will be caused by both the true variations in density and by the noise in the transmission measurements that the scanner makes. The lower the noise in the data, the smaller the density difference that corresponds to true density differences. The fundamental limit in the data noise is the number of photons that were detected. The photon counting noise is a Poisson phenomenon so this noise decreases as the square root of the number of photons detected. The data noise property of a CT scanner is usually specified by the contrast sensitivity which describes the density differences that are statistically significant.

The trace width in electronic assemblies of 250 microns makes it desirable to have pixel sizes of about 50-150 microns so that they will be well resolved. This, in combination with the maximum matrix size that the CT computer reconstructions can currently handle, leads to the maximum size board that the scanner can handle of about 5" x 8". This board size limitation is due to the large data set that must be manipulated by the reconstruction if the board is larger. The reconstruction time increases as a power of the size increase of the matrix, and the memory requirements for a large reconstruction also limit the matrix that can be handled. The ARACOR reconstruction technique now requires less than 5 minutes for a 2048 x 2048 matrix (using a VAX 11/750 with a MiniMap array processor), however a 4096 x 4096 matrix is required to cover a 5" x 8" board at 60 microns pixel size. A board size of 14" x 17" requires a 4096 x 4096 matrix to achieve 140 micron pixels.

A slice thickness of about 250 - 500 microns (based on the rule-of-thumb that the slice thickness can be no more than about 10 times the pixel size) will preserve the resolution and contrast sensitivity while increasing the voxel size to allow the photon flux to be sufficient at the detectors that the

scan time is reasonable. The slice thickness required may be influenced by the flatness of circuit boards and the planarity of the board mounting in the scanner. If the board is not flat or if it is tilted with respect to the scanner the solder bonds will not remain in the imaging plane. Small amounts of board waviness or tilted mounting can be accommodated by increasing the slice thickness. This may bring the circuit traces into the imaging plane and thus increase the penetrating power required of the x-ray source and confuse the image by including features that are not solder bonds.

An x-ray energy of at least 200 KV will be required to penetrate boards with highly attenuating solder and copper in the plane of the scan. A 5" x 8" board has a path over 9" long along the diagonal. This represents many half-value thicknesses of solder or copper. The scans performed with the GE9800 scanner showed that on these small boards an energy of 170KV is at best marginally adequate. The selection of the slice thickness to include only the solder pads will help to alleviate this problem.

The x-ray source spot must be small enough to preserve the desired resolution, but large enough to allow sufficient source intensity to keep the scan time short. The spot size depends on the pixel size that is chosen, it will range from about 85 to 200 microns.

The x-ray source intensity will be limited by the anode cooling design. The source intensity should be as high as possible to keep the scan times as short as possible. There are commercially available x-ray sources that achieve intensity limited by anode surface temperature.

There are two factors that determine the contrast sensitivity required. One is the sensitivity needed to allow the use of partial volume flaw detection in solder bonds and the other is the detection of flux residues, which are low in density and low in Z compared to solder. The contrast sensitivity that will be required to detect a cracked solder bond using partial volume is 10%. This is better contrast sensitivity than will be required to detect flux residues. Contrast sensitivity is defined as the standard deviation of the pixel noise in an image. The image contrast sensitivity is controlled by two factors, the number of x-ray photons detected in each channel and the noise performance of the electronics that measure the

photon signal. The noise and counting statistics will introduce small, random variations in density in the image which do not correspond to true density differences. These two factors control the size of the smallest difference in density in an image that is meaningful. The contrast discrimination specifies the size of the statistically significant differences in density in an image and includes in its specification the image area that the density measurement must include. There is a correlation in the data that allows the contrast discrimination to improve if the areas being compared get larger.

The controlling factors for scanner throughput are source intensity and detector efficiency. The goal for this instrument is board processing totaling no more than 10 minutes. This goal has been set by determining the typical production rates for board assemblies and by determining the amount of time currently spent inspecting boards. The speed as measured in bonds inspected per second will be high due to the large number of bonds per board. The geometry of the CT scanner will also influence the scanner throughput. A commonly used scanner geometry is known as 'Translate-Rotate'. The advantage of this geometry is its flexibility. Large variations in object size can be accommodated. The disadvantage of this geometry is its inefficiency in data collection. The object is not always in the x-ray beam so extra time is required to collect the data. The 'Rotate Only' geometry keeps the object always within the x-ray beam and is the fastest scan geometry. Since throughput will be an important user parameter for this scanner we are recommending the 'Rotate Only' geometry.

4.0 COMPUTED TOMOGRAPHY PERFORMANCE VERIFICATION SCANS

The performance parameters that were estimated are useful guidelines but it is always better to base extrapolations on measurements. We conducted CT measurements to validate our calculations and the results of these experiments are described in this section.

The first industrial scanner built for the Air Force is the AF/ACTS-I (Air Force/Advanced Computed Tomography System) installed by ARACOR at Aerojet near Sacramento, Cal. This scanner was used to verify our estimates of the penetration by the x-ray beam and to place limits on the required resolution and slice thickness. The scanner uses a 420 KV x-ray source and has a resolution of about 800 microns. The slice thickness used was 1000 microns, the thinnest possible on this scanner. The resulting image for a SMT board with 'gull wing' IC's supplied by H-P is shown as Figure 1. It should be noted that the range of density values in these images is from 0 to 32768, which is too large a range to photograph. Features are often much clearer on the computer display than in a photograph. The image of ceramic leadless chip carriers on a ceramic board supplied by TI is shown in Figure 2. Analysis of these images show that the slice thickness was too large with the result that the components and the board were interfering with the imaging of the solder bonds. The same two boards were scanned again together and are shown in Figure 3. This scan was more successful because the slice was more precisely aligned with the plane of the bonds and the signals were larger due to increased integration time at the detectors. The larger signals lead to improved image quality whether the slice thickness is large or small. This image shows that it will be possible to examine boards of typical flatness with a slice thickness thin enough to examine only the solder bonds.

The TOMOSCOPE breadboard scanner at ARACOR is designed to achieve 25 micron pixels. The program that developed this breadboard scanner is developing a prototype high-resolution CT scanner with a field of view of 100 mm. The current breadboard is limited to 5 mm objects. The TOMOSCOPE breadboard scanner was used to show that at high resolution bond defects can be detected. The low x-ray source energy, 200 KV, of this scanner raised

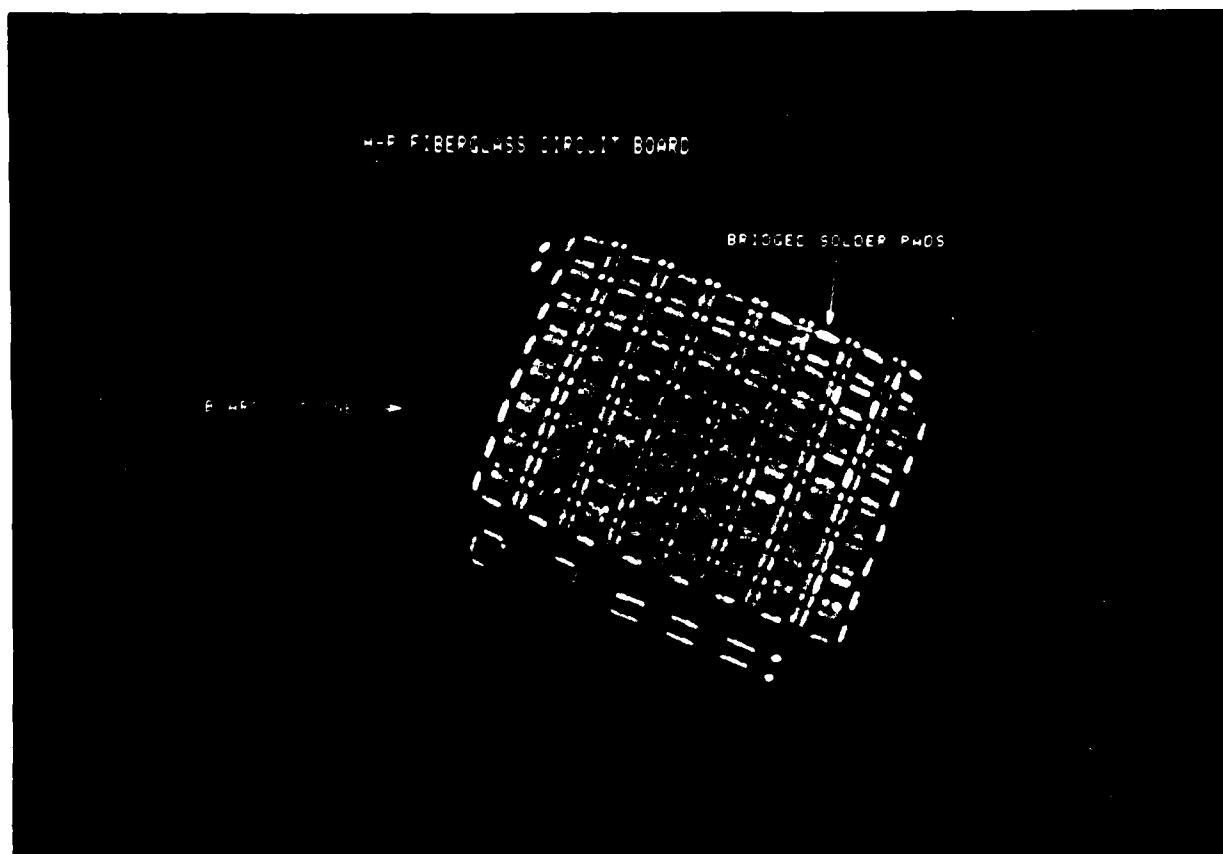


Figure 1: AF/ACTS-I image of gull wing IC's.

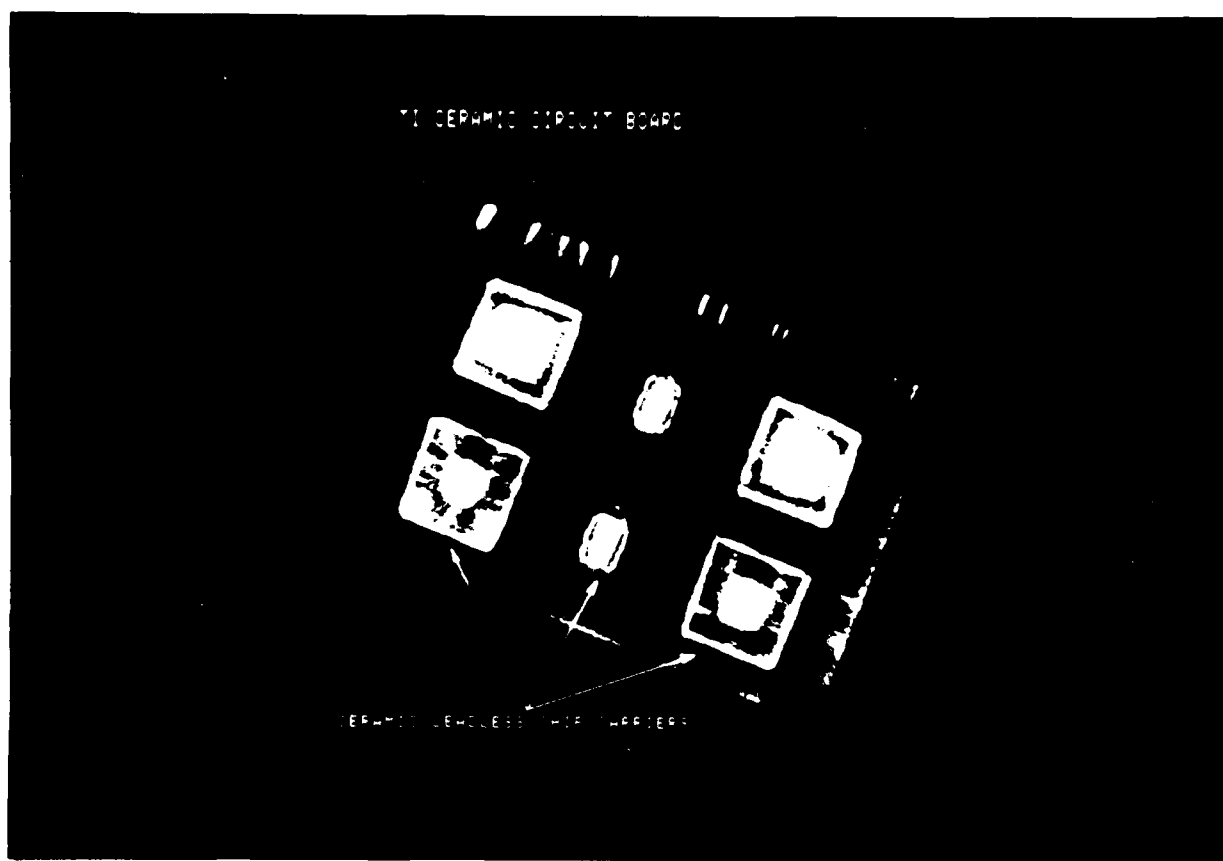


Figure 2: AF/ACTS-I image of ceramic leadless chip carriers.

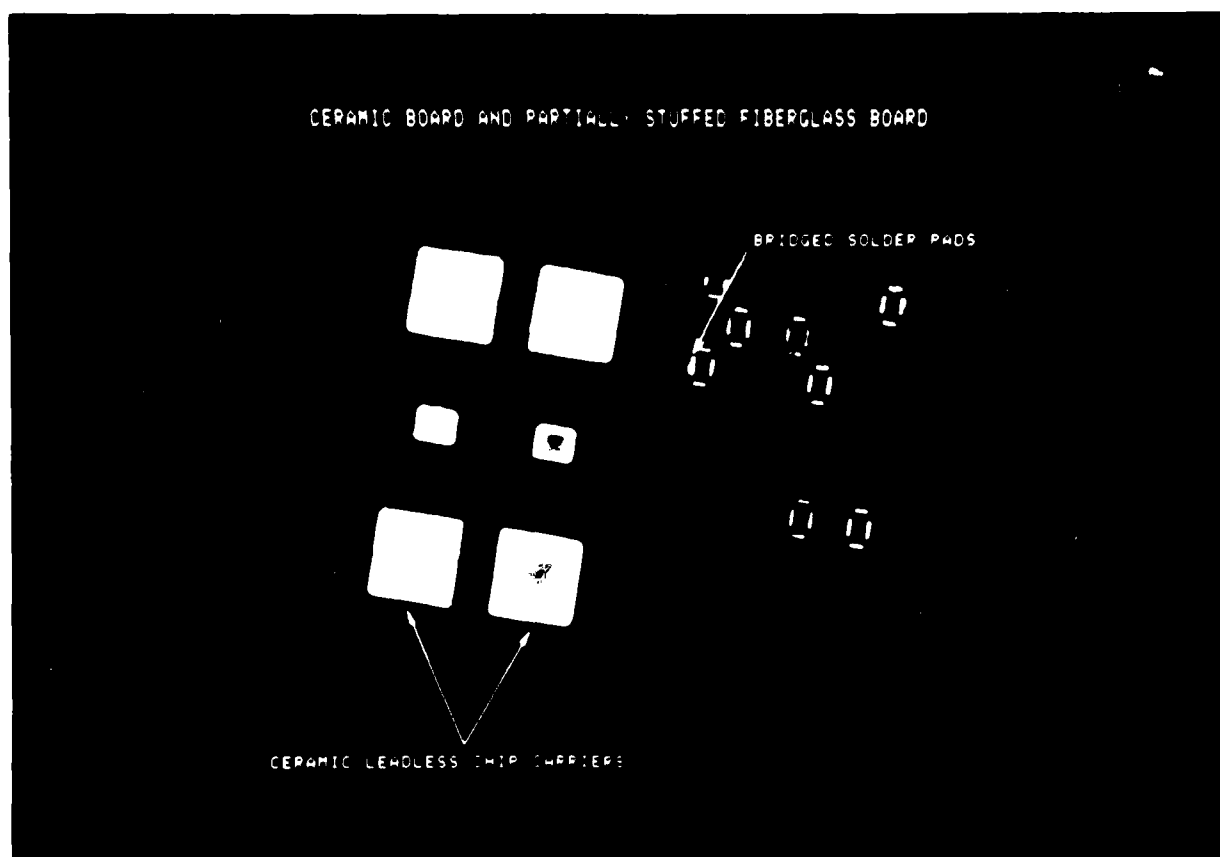


Figure 3: AF/ACTS-I image of SMT circuit boards.

the concern that the penetration would be too low and that streak artifacts would dominate the images. The object size limitation led to first scanning the solder bonds in a plane perpendicular to the board plane. These two images, Figures 4 and 5, show a good and bad bond and show that the scanner can penetrate solder with the lower x-ray energies that this scanner uses. We then scanned a portion of a 'J' lead IC package soldered to a board. The imaging plane and the board plane were parallel for this scan. This scan was affected by a collision between the object and the slice thickness collimator of the scanner. The image was poor as a result of this problem but close examination shows that in-plane scanning will reveal much information about bond quality. All of the scans were conducted using an effective focal spot size of 51 microns to increase the available flux and increase the speed of the scan. The slice thickness was 508 microns. The resolution achieved under these conditions is 75 microns.

The GE9800 CT scanner at UCSF was used to examine a board, with larger features than SMT boards, to further elucidate the capabilities of conventional CT scanners in examining printed boards. The resolution of the GE9800 is about 600 microns. The slice thickness used was 1000 microns, the thinnest possible. The x-ray source in a GE9800 is limited to 170KV. This scanner was used to study further the penetration of solder by comparatively soft x-ray beams and the streak artifacts that this can cause. The results showed that using a 170 KV x-ray source leads to an image with streak artifacts that makes image interpretation difficult. The other drawback of this particular scanner is the software package that performs the image reconstructions. This software is highly optimized for scanning human beings, and as a result filters out information that is unlikely to apply to the image of a human. The scans done using the GE9800 placed a lower limit on the x-ray source energy of 170 KV and showed that the reconstruction software must be written to match the solder bond inspection task.

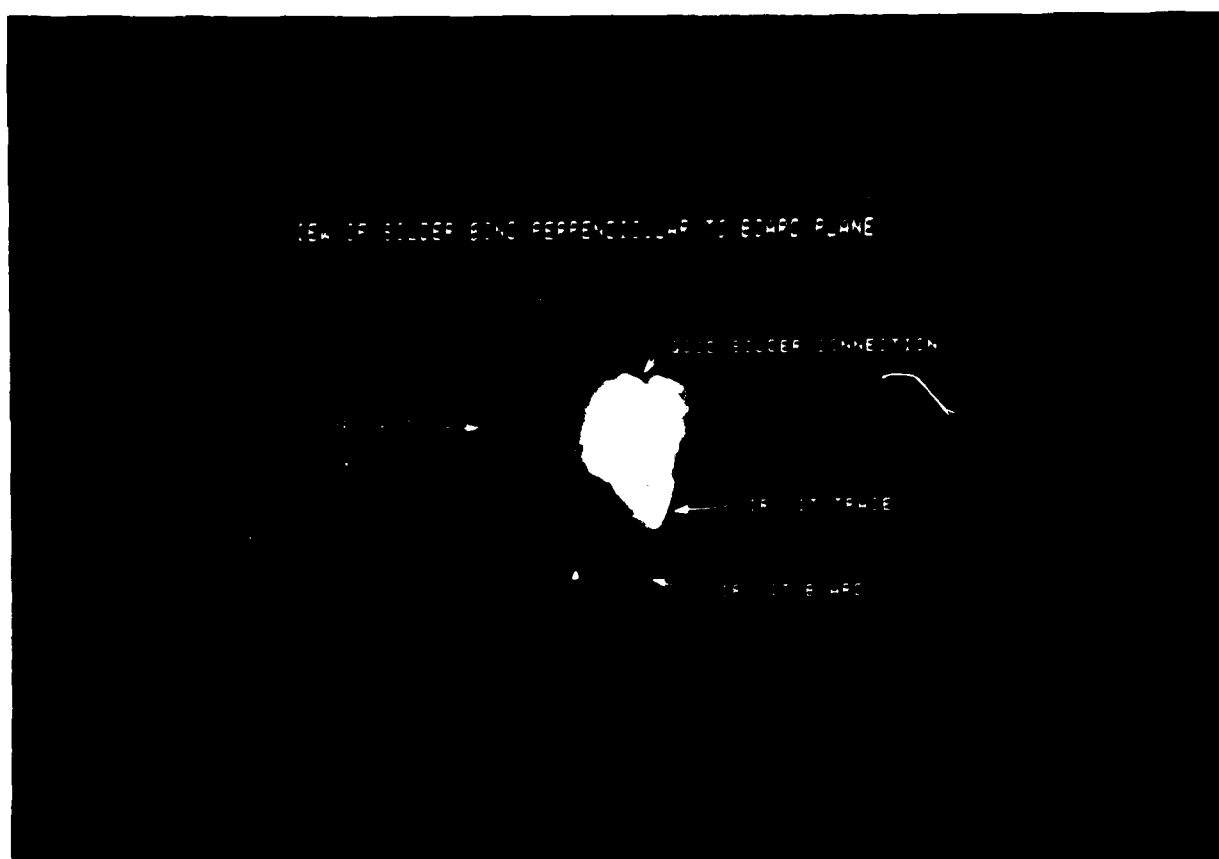


Figure 4: Tomoscope breadboard image of a good solder bond.

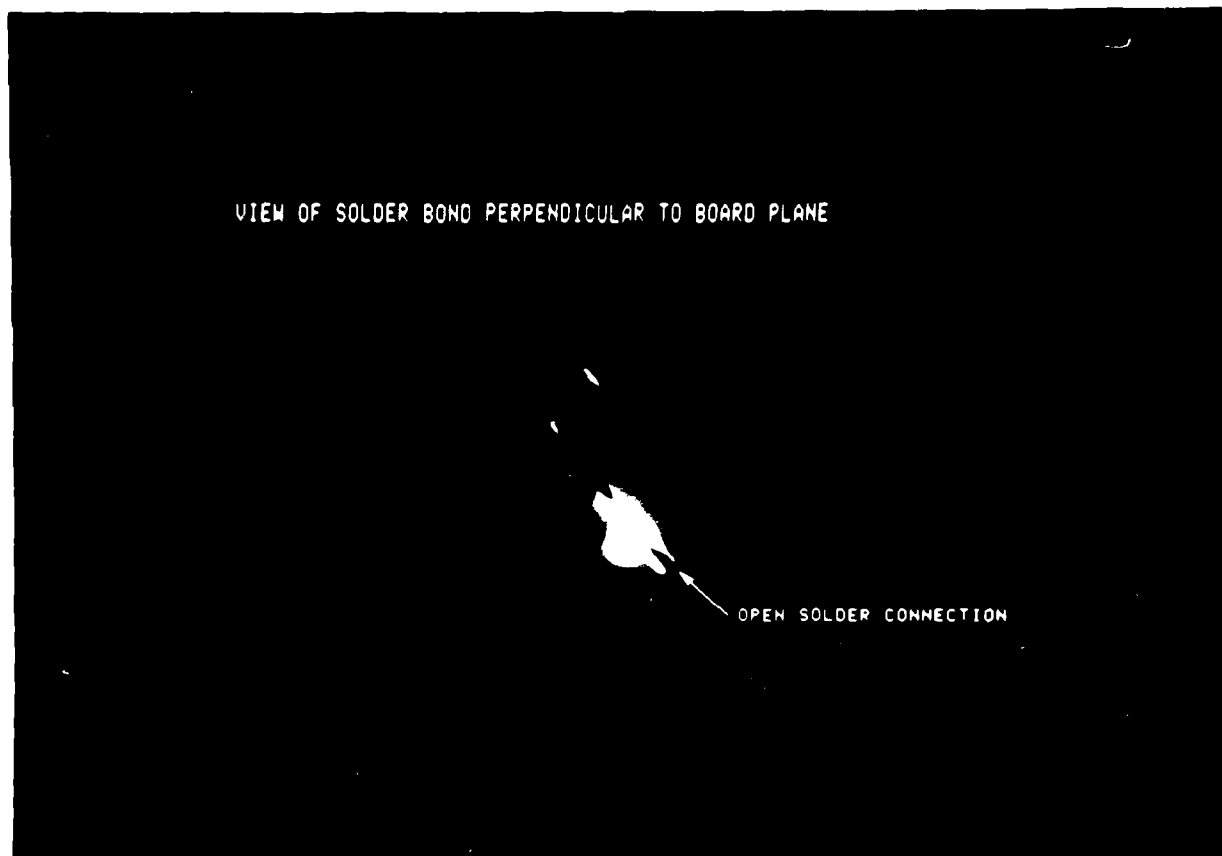


Figure 5: Tomoscope breadboard image of an open solder bond.

5.0 CONCEPTUAL DESIGN OF A CT INSPECTION DEVICE

A CT system is made from several subsystems that must all function together for the scanner to achieve its performance goals. The building blocks for all CT scanners are the x-ray source, the x-ray detectors, the object handling system, and the computer system that coordinates the data collection, reconstructs the image, and displays the image.

The resolution required of this CT scanner implies that the focal spot size of the x-ray source must be smaller than that of conventional x-ray tubes (at about 5 mm), but larger than that of microfocus tubes, which can have spots as small as 5 microns. The easiest solution to this problem is to modify a microfocus system by defocusing its electron beam. The power supply of the microfocus system should be upgraded to allow higher beam current and thus higher x-ray flux output. The focal spot size used will be the optimum tradeoff between small size to preserve resolution and large size for high flux to minimize the data collection time. The maximum voltage of the x-ray source should be no less than 200 KV, with 350 KV preferred. The higher energy is desired to penetrate the highly absorbing solder.

The resolution required of this CT scanner implies that the detector element size should be smaller than that used in conventional CT scanners, but larger than the 25 microns developed for the TOMOSCOPE. The scintillator/fiber optic coupled to RETICON photodiodes technology used in ARACOR's TOMOSCOPE is not easily made larger to meet the requirements of this scanner. One way to utilize this detector technology would be to sum groups of detector channels to create a larger effective element size. There is a cost and speed penalty associated with this approach due to the very large number of channels that must be handled before the summation occurs.

We are recommending that conventional discrete element technology be used but in an innovative array of elements that are much narrower than current detectors. The major problem to be solved in this approach is to keep the spacing of the detector elements as close as possible to avoid wasting x-ray

photons. We will accomplish this with an innovative design for the septa and collimators between the detector elements. We will deposit aluminum on the sides of the detector crystals so that they can be placed immediately adjacent to each other. The apertures for the crystals will be made from tungsten wires so that there is very little dead area at the front of the detector array. The photodiodes will be custom fabricated to put them at the correct locations and to ensure that they have the correct sensitive area to match the array of detector crystals.

The handling system of any CT scanner must move the samples being examined to very high precision to prevent blurring due to mislocation of the object. The scanners built by ARACOR have used several different types of handling systems, ranging from modified CNC machine tables to small stepper motor controlled translation and rotation tables. We are recommending a relatively simple stepper motor controlled rotation table for this scanner. This will provide the accuracy, speed, weight capacity, and size required for the prototype scanner at a very low expense.

ARACOR has built up a complete CT control and analysis software package on VAX-11/750 computers using CSPI MiniMap array processors and a VME68000 auxiliary computer. This computer technology is now old and better, more cost effective systems are beginning to appear. We recommend using a MicroVAX II for this prototype scanner. There is likely to be an improvement in array processors as well, but they are not yet available in the performance range that we require. The display system that ARACOR has used is a RAMTEK 1024 by 1280 pixel display and display driver. The 2048 x 2048 reconstructed images that this scanner will produce make an improved display system desirable. The bandwidth required for a higher resolution display monitor is so high that 2048 x 2048 monitors are unlikely to become commercially available soon, however as memory continues to become less expensive it will be possible to have the entire 2048 x 2048 image in the display driver memory and to scroll a 1024 x 1024 region around in the display. A production version of this inspection instrument will use the main computer to make the accept/reject decisions so the display system for this scanner is less important than it might otherwise be.

The ability of the CT inspection system to perform the accept/reject decisions can be enhanced by using the CAD/CAM data that was used to design and fabricate the board assemblies. This data would provide the CT scanner with the positions of the components and the solder bonds that mount them. This would speed the development of the accept/reject criteria for each board assembly. This is a capability that will be desired in a production version, but will not be attempted in the prototype design.

6.0 CONCLUSION AND RECOMMENDATIONS

The problem addressed by this project is the inspection of solder bonds in electronics assemblies. This project has successfully collected information about solder bond technology that identified common soldering techniques and the typical flaws that are found in the resulting solder bonds. The project has derived from this information the performance characteristics of a CT scanner that will detect these flaws, with an emphasis on the Surface Mount Technology characteristics. The SMT solder bond is being used in more and more systems and is a difficult bond to examine using current techniques.

The derived performance parameters were verified by using existing CT scanners to examine several PC boards. The results of these scans were positive detecting most flaws known to be present in any given object. The existing scanners do not provide a good match with the desired performance characteristics so that the ability of these scanners to perform useful inspections was limited, but the results suggest that a well designed scanner system will be able to provide the needed inspection tool.

Based on the success of this initial study we recommend that two steps be taken. The first step is to complete the correlation of the CT inspection images with solder bond flaws by modifying an existing scanner to more nearly match the required performance parameters. The correlation can be conveniently conducted using a modified in-house scanner at ARACOR. Experiments with this modified scanner will also guide the design tradeoffs for a prototype inspection instrument.

Following successful experiments on the modified scanner, the second step is to build a limited breadboard prototype scanner that will prove the innovative detector technology. The breadboard scanner will have performance that can be directly extrapolated to the performance of a CT solder bond inspection instrument. The breadboard will show what the defect detectability limits will be and what the inspection throughput will be. Towards this end, ARACOR will submit a Phase II SBIR proposal.

END

DATE

FILMED

5-88

DTIC