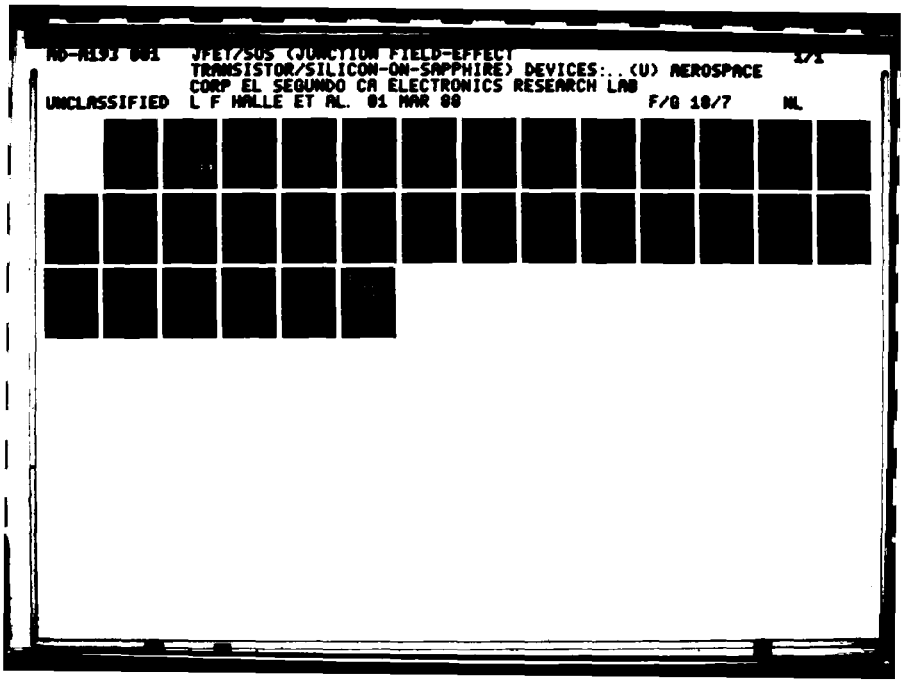
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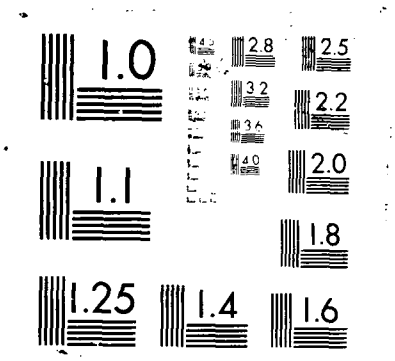
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JFET/SOS Devices: Gamma-Radiation-Induced Effects

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Enhancement- and depletion-mode JFETs have been fabricated on silicon-on-sapphire substrates. When these devices are irradiated under bias with a ^{60}Co source, their drain currents increase, and their threshold voltages shift in such a way that the devices become more difficult to "pinch off." These effects can be explained by positive charge trapping at the silicon/sapphire interface. Gate-to-drain leakage currents also increase, and can be traced to interface effects at the gate edges rather than to the passivating oxide. These effects were studied as a function of dose rate and postirradiation annealing. Deep-level transient spectroscopy (DLTS) was performed prior to and following both irradiation and anneal on both the gate-drain and gate-source p-n junctions. DLTS trap bands were observed whose characteristics depended on the depth of the depletion layer and on the total gamma dose received. The DLTS spectra suggest that a continuum of levels is responsible for the bands, and that the emission kinetics are influenced by band bending at the Si/sapphire interface. The ma jor

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Transistor

19. ABSTRACT (Continued)

bands corresponded in temperature with steps in capacitance-temperature curves. A correlation of these steps with the transistor characteristics suggests that channel pinch-off can be influenced by capture and emission at deep centers.

CONTENTS

FIGURES

I. INTRODUCTION

It is well known that the performance of metal oxide on silicon field-effect transistors (MOSFETs) degrades rapidly during exposure to ionizing radiation, as a result of the sensitivity of the insulating gate oxide to radiation.[1] Junction field-effect transistors (JFETs) are attractive for those circuit applications where high dose rate and total dose hardness are required for survival, because the controlling structure of these devices is a p-n junction and not an insulating oxide. In addition, silicon-on-sapphire (SOS) substrates provide a thin Si layer that minimizes the volume in which high-dose-rate photogeneration can occur. On the other hand, SOS substrates have a complicated Si-sapphire interface along which radiation-induced currents may be generated as a result of either interface states or trapped charge. In this study, the effects of gamma radiation on JFET/SOS devices are examined, and the JFET, in turn, is used to provide information about the Si-sapphire interface. This information is acquired by an examination of both the changes in device parameters and the changes in the spectra of deep levels as a result of irradiation and subsequent annealing.

II. EXPERIMENTAL PROCEDURE

The process development and resulting device characteristics for the JFET used to examine these radiation effects are presented elsewhere.[2] Briefly, both enhancement- and depletion-mode n-channel devices were fabricated in SOS wafers with a 0.6-μm epitaxial Si layer on sapphire. Dopant profiles were made by ion implantation. These wafers, purchased from Union Carbide as their type-A material, were not further treated prior to device processing.

Radiation-induced changes in drain current, threshold voltage, and gate-drain diode leakage were tracked. Unless otherwise noted, during irradiation and subsequent annealing the bias on the enhancement-mode devices was as follows: drain/source voltage V_{DS} = +10 V and gate/source voltage V_{GS} = 0.4 V; the bias on the depletion-mode devices was V_{DS} = +10 V and V_{GS} = -1.5 V. For the plots that follow, measurements of drain current were taken at V_{DS} = +3.0 V and V_{GS} = +0.5 V for the enhancement-mode devices, and at V_{DS} = +3.0 V and V_{GS} = 0 V for the depletion-mode devices. Threshold voltages were taken as the x-axis intercept of the linear portion of a plot of V_{GS} versus the square root of the drain/source current I_{DS}, with V_{DS} held constant at +2.5 V. (In particular for the enhancement-mode device, this linear region becomes difficult to discern as the device is irradiated. Because of this, the threshold voltages best describe a trend rather than absolute values.) The gate/drain leakage current was measured where the gate/drain voltage V_{GD} = +5 V, with the source floating.

Total dose effects were studied by means of a Shepherd ^{60}Co irradiator capable of widely varying dose rates. The dose rate used in these experiments, unless otherwise noted, was 200 krad(Si)/hr. A Sula spectrometer was used to perform deep-level transient spectroscopy (DLTS) and thus obtain information on the nature of the traps induced by radiation. Annealing studies were performed at room temperature and at 100°C with the devices held under bias. The devices under test were irradiated to 3 Mrad(Si), and their characteristics were measured as a function of time.

III. RESULTS AND DISCUSSION

A. CHANGES IN TRANSISTOR PARAMETERS WITH RADIATION

Typical results for the enhancement-mode JFET/SOS devices studied are shown in Fig. 1. During irradiation, the drain was biased at 10 V and the gate at 0.4 V, so that the devices were on. The drain current increased by roughly a factor of 4, and the average threshold decreased from ≈ 0.3 V to almost 0 V; this caused some devices to operate in depletion mode ($V_T < 0$). Also shown in this figure is the large increase in gate-drain leakage. These changes are all consistent with positive charge trapping at the Si-sapphire interface. Such trapping makes the devices turn on more easily, allowing larger drain currents at a given gate voltage; it also causes a high back-channel leakage. These effects appeared to reach maximum around 100 krad(Si) to 1 Mrad(Si), and even decreased at higher doses. Similar observations made previously were attributed to positive charge trapping.[3-5]

As shown in Fig. 2, corresponding results were obtained with depletion-mode devices. Again, the source/drain current and gate/drain leakage currents increased, and the threshold voltage decreased from about -0.9 V to about -1.6 V. These devices were turned off during the initial portion of the irradiation, with V_{DS} = +10 V, and V_{GS} = -1.5 V. The maximum change in parameters occurred at the same total doses as did the changes in parameters of the enhancement-mode devices. If this apparent saturation were due to self-annealing during the irradiation, the effects of radiation at higher dose rates would reach maximum at higher total doses. However, this does not occur for either enhancement-mode or depletion-mode devices, as shown in Figs. 3 and 4. For both types of devices the maximum value of source/drain current occurs at the same total dose, independent of dose rate. While some variation in the values measured is observed with the different dose rates, this variation is not significantly different from that observed among different devices irradiated at the same dose rate. Similar results were obtained for the changes in threshold voltage and gate/drain leakage current. Other researchers have attributed this saturation at higher doses to negative charge traps formed at

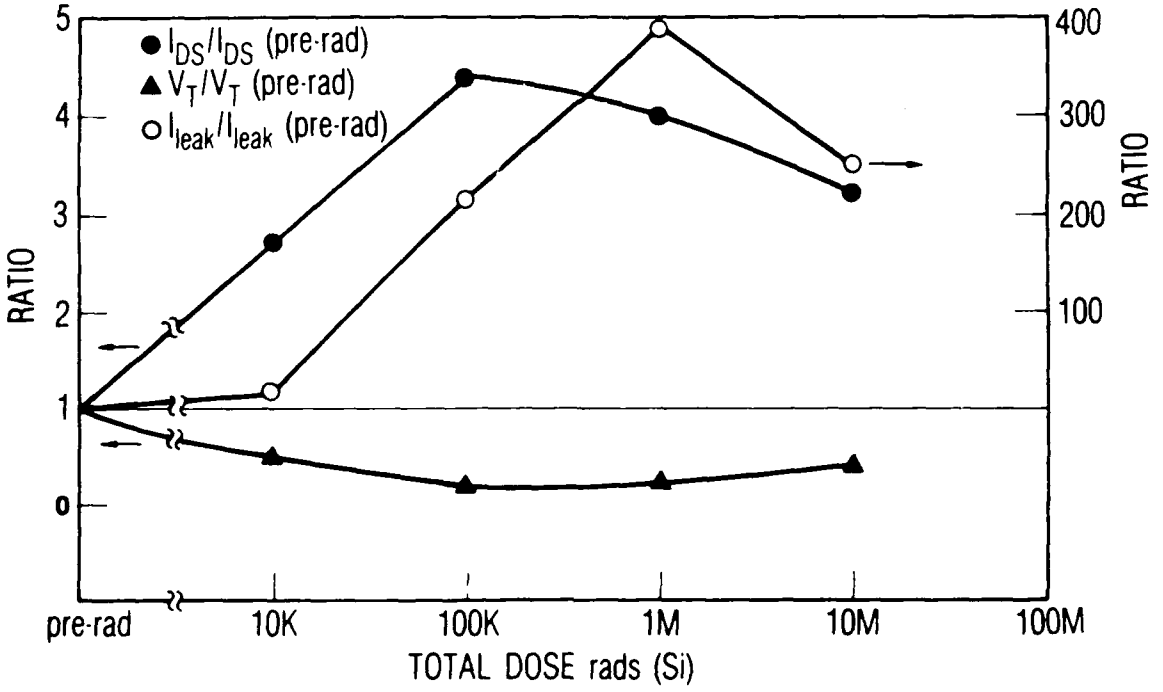

Fig. 1. Ratios of Postirradiation Values to Pre-irradiation Values for Source/Drain Current I_{DS}, Threshold Voltage V_T, and Gate/Drain Leakage Currents of the Enhancement-Mode JFET. The changes in I_{DS} and V_T correspond to the left axis, while changes in the leakage currents correspond to the right axis.

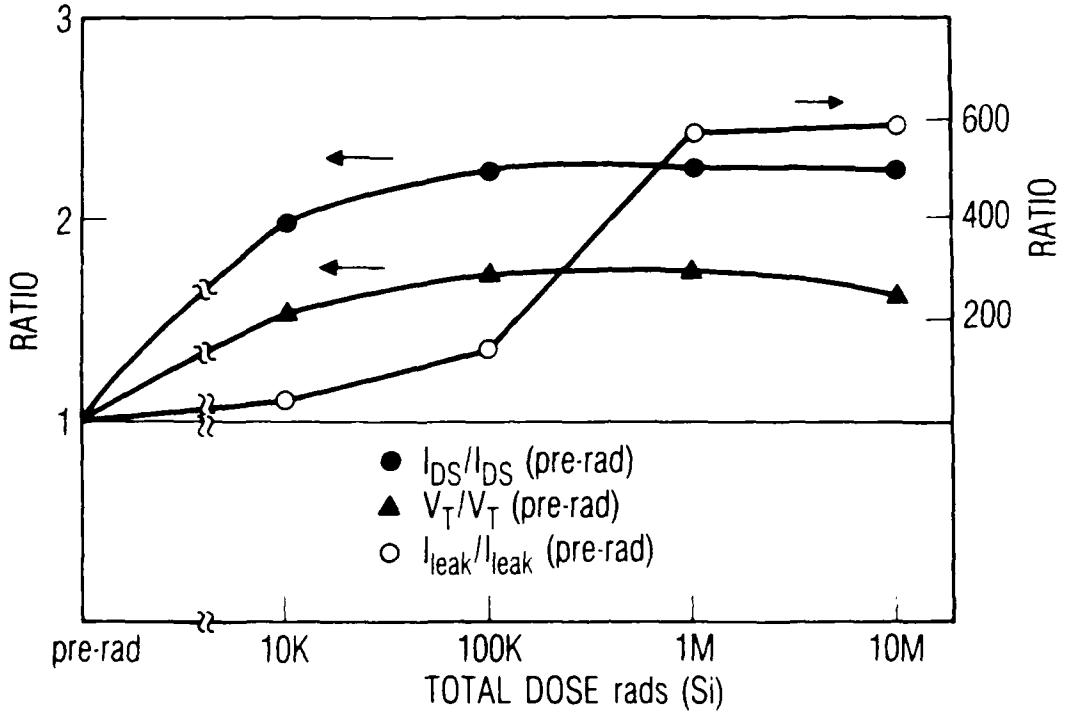

Fig. 2. Ratios of Postirradiation Values to Pre-irradiation Values for Source/Drain Current I_{DS}, Threshold Voltage V_T, and Gate/Drain Leakage Currents of the Depletion-Mode JFET. The changes in I_{DS} and V_T correspond to the left axis, while changes in the leakage currents correspond to the right axis. Note that the threshold voltage changes from its pre-irradiation value of about -0.9 V to a more negative value, thus decreasing, while the ratio of the two negative numbers increases.

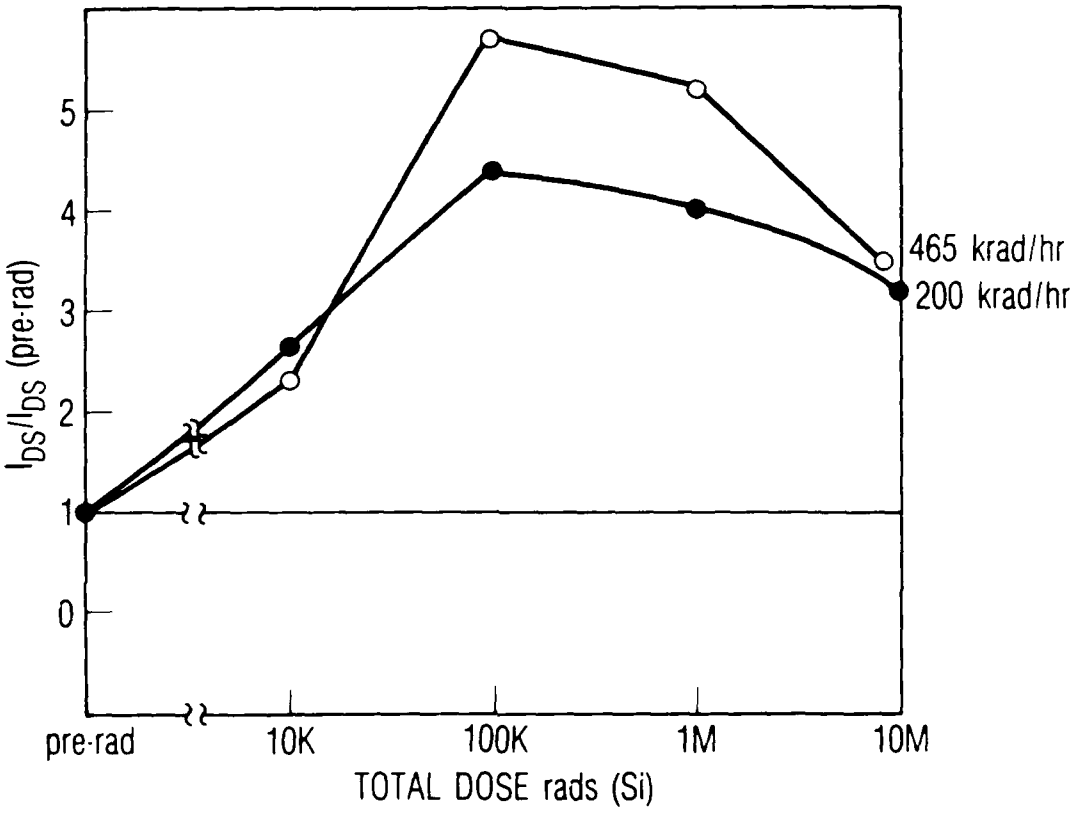

Fig. 3. Ratios of Postirradiation Values to Pre-irradiation Values for I_{DS} of the Enhancement-Mode Device Measured at Dose Rates of 200 and 465 krad(Si)/hr

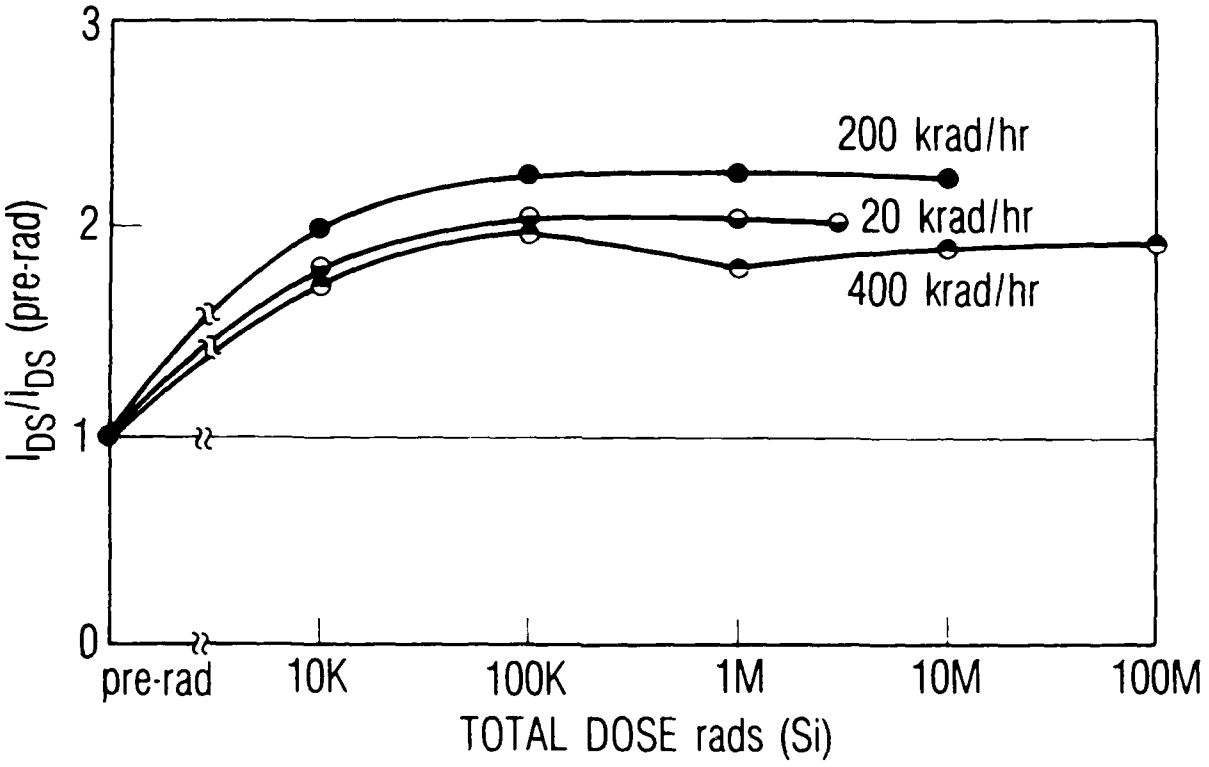

Fig. 4. Ratios of Postirradiation Values to Pre-irradiation Values for I_{DS} of the Depletion-Mode Device Measured at Dose Rates of 20, 200, and 400 krad(Si)/hr

the Si/sapphire interface or in the sapphire itself, which may compensate for the positive charge trapping.[3]

Typical results for the postanneal recovery of the drain current in a depletion-mode device are shown in Fig. 5. These devices anneal only slightly faster at 100°C than at room temperature; in either case, the devices had not fully recovered in over several hundred to a thousand hours. Interestingly, the effects of the irradiation can be reversed; that is, the parameters reverted back to the original values when the devices were irradiated to 10 krad(Si) with 0 V on the drain. This critical dependence on drain voltage was observed previously with SOS MOSFETs.[6] As noted below, the DLTS spectra exhibit similar recovery characteristics with annealing.

Also monitored were the effects of different bias conditions during irradiation. There was no observed effect on the parameters when the gate voltage was changed from 0 to -2.0 V for the depletion-mode device. However, a large effect was seen as the drain voltage was changed, as shown in Fig. 6. As this voltage approaches zero, the radiation-induced changes diminish. As illustrated in Fig. 6, at V_{DS} = 0 V there was virtually no effect from the irradiation. These results agree with earlier studies on both Si and SOS JFET devices.[5,7,8] The strong dependence on drain voltage suggests that the lateral field associated with this voltage increases the trapping of charge at the interface by separating the gamma-induced electron-hole pairs, thereby preventing electron-hole pairs from recombining and allowing the slower-moving holes to become trapped. This is similar to the effect of worst-case bias observed in irradiated MOSFETs, where a positive voltage on the gate is assumed to increase charge separation and thus increase charge trapping at the oxide-silicon interface.[9] Studies of the effects of radiation on JFETs fabricated on zone-melted recrystallized Si-on-oxide material (another type of Si-on-insulator material) indicate that these effects can be lessened by biasing the back substrate.[10]

For our JFET/SOS structures, an important issue is whether or not the passivating oxide covering the Si regions that lie between the gate, source, and drain metallization regions is a significant leakage path. To determine

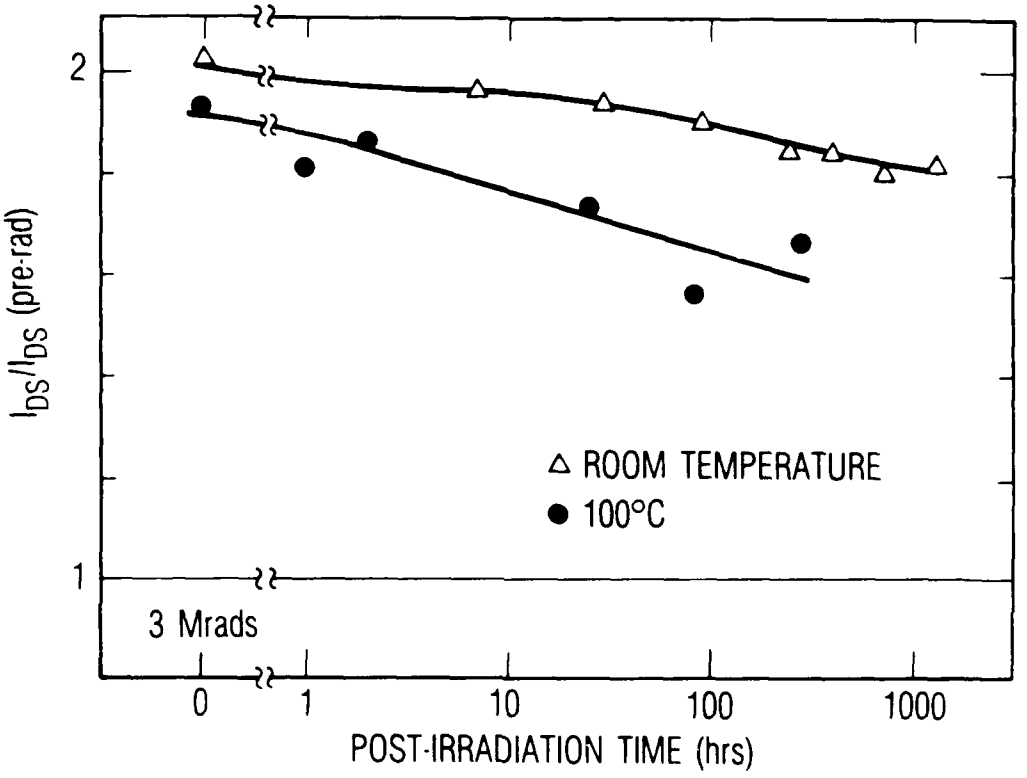

Fig. 5. Ratios of Postirradiation Values to Pre-irradiation Values for I_{DS} of the Depletion-Mode Device Measured as a Function of Annealing Time Following Irradiation to a Total Dose of 3 Mrad(Si) (Time Zero). During annealing, the devices were held at either room temperature or 100°C.

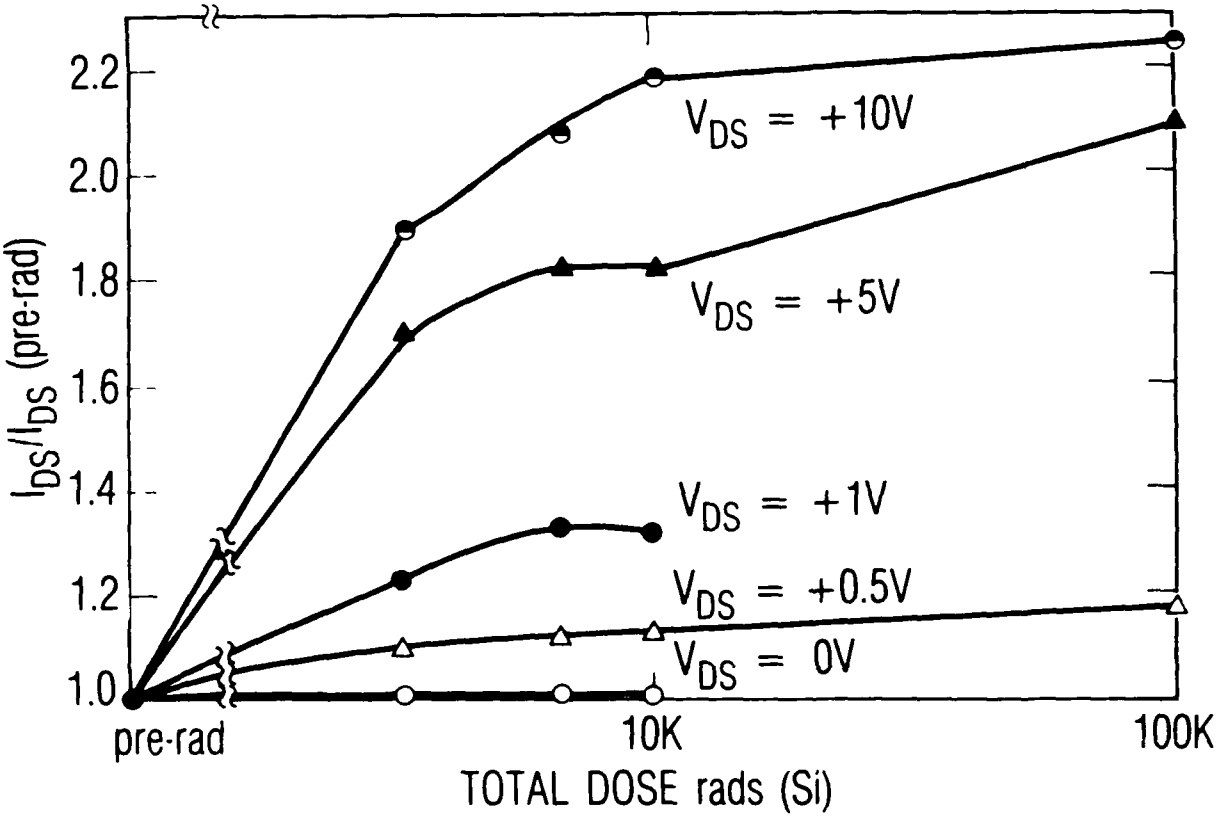

Fig. 6. Ratios of Postirradiation Values to Pre-irradiation Values for I_{DS} of the Depletion-Mode Device Measured as a Function of the Drain Bias. During irradiation, V_{GS} = -1.5 V.

this, we measured the gate/drain leakage current after irradiation on some "fat" JFETs, devices having dimensions 4 times wider and 70 times longer than the standard devices under investigation. If the leakage were due primarily to the oxide, one would expect the leakage to increase by a factor of 4 in the fat JFETs. However, as shown by the comparison given in Fig. 7 for the two device sizes, the leakage current (both pre- and postirradiation) appears to scale by a factor of about 37. Thus, we conclude that the dominant leakage path is due to the back channel at the Si/sapphire interface.

B. DLTS MEASUREMENTS

As noted above, prior studies of JFET/SOS structures have explained the postirradiation response of these devices as being largely due to the presence of a fixed charge created in the sapphire by the irradiation.[3-5] However, in addition to measuring the effects of radiation on transistor characteristics, we also measured capacitance as a function of temperature in conjunction with deep-level transient spectroscopy (DLTS). The results of these measurements imply that there is an important additional effect, one due to the formation of negatively charged interface states in the Si.

With DLTS it is possible to study those states that communicate with the conduction band of the n-type Si. This technique has been described previously in the literature.[11] A high-frequency (1 MHz) capacitance meter in the Sula spectrometer is employed to detect rapid changes in capacitance following the application of a voltage pulse to a p-n junction under dc reverse bias. The gate/drain and gate/source junctions of the JFET/SOS device are cooled to a temperature low enough so that the thermal emission of carriers from the trapping levels of interest is negligible. The application of a positive voltage pulse brings the reverse-biased junction to zero bias, momentarily filling the region from the edge of the zero-bias depletion layer to the edge of the depletion layer at the dc bias with majority carriers (electrons). The traps will capture electrons and remain filled at the low temperature. As the temperature is raised, thermal emission from the interface states occurs; the resulting change in the charge state then leads to a capacitance transient. Unlike other thermally stimulated techniques in which

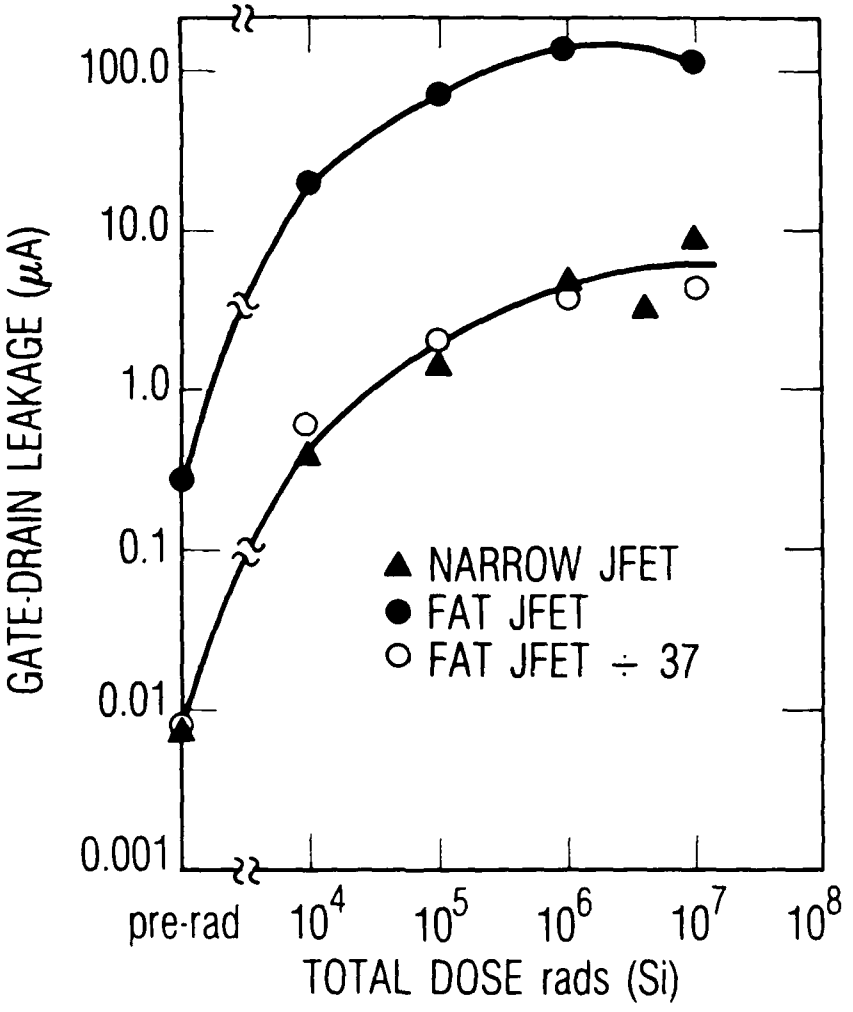

Fig. 7. Gate/Drain Leakage Currents Measured as a Function of Radiation Dose Plotted on a Log-Log Scale for the Standard Depletion-Mode Devices Used in These Studies: (1) a JFET having a 4 × 104 μm gate (triangles), and (2) a "fat" depletion-mode JFET (from the same wafer as the smaller device) having a 442 × 285 μm gate (closed circles). The open circles represent the leakage currents of the fat JFET divided by a factor of 37.

the trap-filling excitation is terminated prior to warm up, in DLTS the voltage pulses are applied continuously at some low frequency during both warm-up and measurement. The capacitance transient is sampled by a double-gated correlator whose time gates are selected according to the temperature range and trap depth of interest.

Typical DLTS spectra for an enhancement-mode device (E-JFET) are shown in Fig. 8 prior to and following irradiation. To obtain these spectra, we tied the drain and source together and examined the junction each formed with the gate. The dc bias for the DLTS measurement is the gate bias, as indicated in the figure. Weak bands are usually observed prior to irradiation. Following a dose of 100 krad(Si), a large band centered near 270 K is evident. As might be expected for an interface state, the peak temperature of these trap bands (i.e., the temperature at which the peak of the trap band occurs) depends on the applied bias; this bias affects the degree of band bending at the Si/sapphire interface and, hence, the kinetics of thermal emission between the trap and the conduction band.

The dependence of the location of the peak of the trap band on junction bias is one of several complicating factors which, taken together, preclude any detailed, quantitative interpretation of the DLTS data. Unlike a large-area planar p-n junction, the junction area in our JFET devices is small and difficult to define. While we cannot calculate trap concentrations, we note that because of the very small area, a significant trap-band intensity implies a large trap concentration. Also in contrast with the case of a planar junction, for a JFET the depletion-layer field lines between the gate and either the source or drain are complex. In addition, it is difficult to measure precisely the impact of the Si/sapphire interface on the depletion layer. This is further complicated by the fact that the sapphire substrate is electrically floating. In spite of these limitations, gamma irradiation, as clearly indicated in Fig. 8, causes dramatic changes in the DLTS spectrum, and the trends associated with these changes reveal important information about the effects of radiation on the JFET/SOS structures we studied.

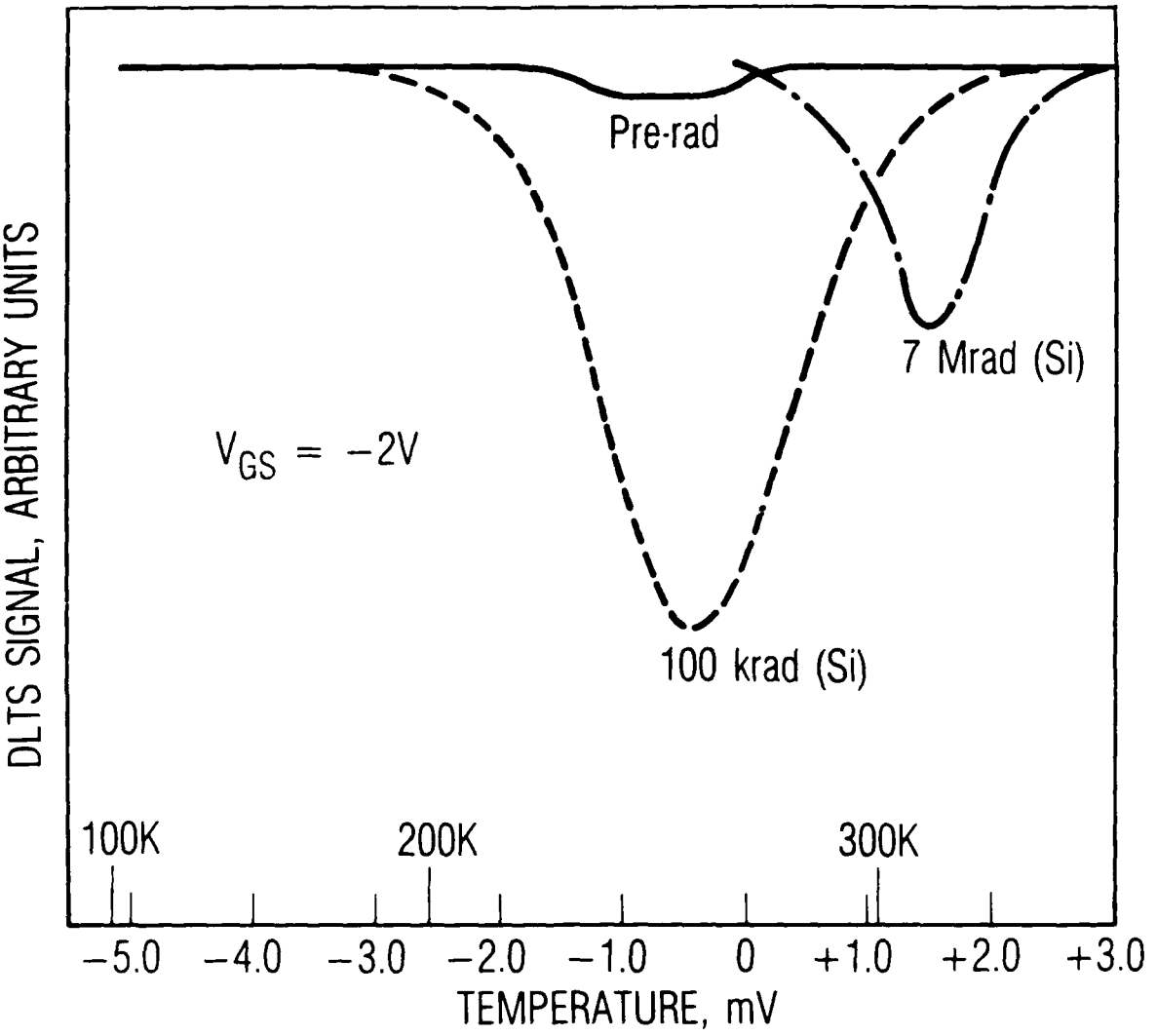

Fig. 8. DLTS Spectra for an Enhancement-Mode JFET/SOS Device, Showing Changes that Occur with Irradiation. During the DLTS runs, V_{GS} = -2 V. The rate window for these measurements was 128 sec^{-1}.

It is apparent from a large number of DLTS spectra that the total dose affects the peak temperature, as does the applied gate bias. Thus, the trap band shown in Fig. 8 after a dose of 7 Mrad(Si) is believed to be the same band as that shown for a dose of 100 krad(Si), even though the peak temperatures for the two doses are different. Varying the dose or the bias in small increments causes the location of these bands to change continuously. An important feature shown in Fig. 8 is that the trap-band concentration, as approximately revealed by the peak height, decreases with increasing dose above about 200 krad(Si); this correlates with the decreases in changes in transistor characteristics shown in Figs. 1 and 3.

Several different bias conditions were imposed during irradiation in order to determine the effect of such variations on the DLTS spectrum. In one experiment the gate/drain and gate/source junctions were examined individually following irradiation under different bias conditions. The results demonstrate that reversing the direction of the source/drain bias during irradiation has no effect on the growth of interface states at either junction. In other words, DLTS measurements on both junctions give the same results whether V_{DS} is +10 V or -10 V. Apparently the lateral direction of the fringing electric field in the sapphire does not affect the rate of growth of the interface state.

As indicated earlier, however, the presence of a source/drain bias is essential for the observation of significant radiation-induced changes (see Fig. 6). Figure 9 shows that the changes in the DLTS spectra for an E-JFET irradiated to 7 Mrad(Si) are similar to changes in the transistor parameters with respect to bias conditions during irradiation. Note that when V_{DS} was zero there was essentially no trap-band growth independent of the value of the gate voltage, and that the growth in the presence of a significant V_{DS} was also independent of gate bias. After irradiation at any of these biases, the pre-irradiation DLTS spectra, like the original transistor parameters, can be recovered by irradiating the device to 10 krad(Si) with the drain biased at 0 V. Postirradiation annealing under bias at the temperatures and times shown in Fig. 5 did not fully recover the pre-irradiation DLTS signals.

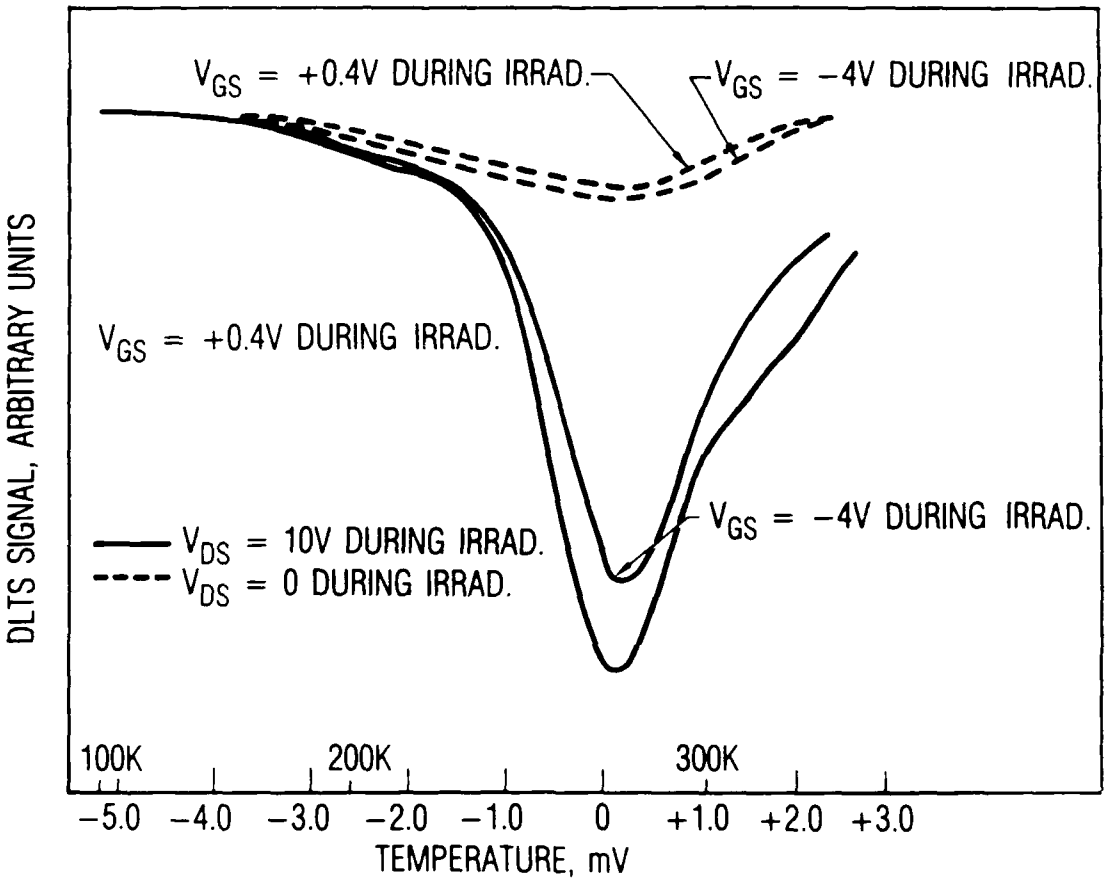

Fig. 9. DLTS Signals for an Enhancement-Mode JFET, Showing the Effect of Bias During Irradiation to 7 Mrad(Si). DLTS spectra were taken with V_{GS} = -2 V, with a rate window of 128 sec^{-1}. The pre-irradiation spectrum was approximately the same as that for V_{DS} = 0 (dashed curves).

Typical capacitance-temperature (C-T) data are shown in Fig. 10 for an E-JFET prior to and following irradiation to 100 krad(Si). Several pre-irradiation measurements of this type on both E-JFETS and depletion-mode devices (D-JFETS) demonstrated that when the channel is open, the capacitance is approximately twice that when the channel is pinched off. For D-JFETs the capacitance prior to irradiation at zero bias will be large and relatively constant over the entire temperature range shown in Fig. 10. Thus, the onset of an increase in capacitance corresponds approximately to the onset of current flow in the channel. One should expect this to be the case, since a shrinkage in the depletion layer sufficient to open the channel significantly should also lead to an increase in capacitance. As shown in Fig. 10, prior to irradiation the channel is closed below room temperature for zero and negative bias, as one would expect for an E-JFET. However, after irradiation, steps are observed in the C-T curves at various temperatures, depending on the bias. These data agree with the irradiation-induced decrease in threshold voltage shown in earlier figures. These measurements also provide additional evidence for irradiation-produced interface states, since trapped charge in the sapphire should not show any temperature dependence. The interface states, however, will undergo a change in charge state as they depopulate with temperature, which in turn will lead to a corresponding change in capacitance.

The correspondence between DLTS bands due to interface states and the steps in the C-T data is shown more clearly in Fig. 11 for an E-JFET irradiated to 100 krad(Si); note that the thermal emission from the interface states is maximum at the temperature corresponding approximately to the step, beginning at approximately 270 K, in the C-T curve. (The peak temperatures of the DLTS curves are of course dependent on the timing parameters with which they are measured. However, measurements taken with rate windows varying from 128 sec^{-1} to 1.28×10^3 sec^{-1} give resulting peak locations in the range of 297 to 266 K. This temperature range falls well within the rising region of the C-T curves. Also, the C-T step and the DLTS band vary together when the gate bias is changed.) In addition, the source/drain current at $V_{DS} = 3.0$ V as a function of temperature is shown for this device. The onset of this

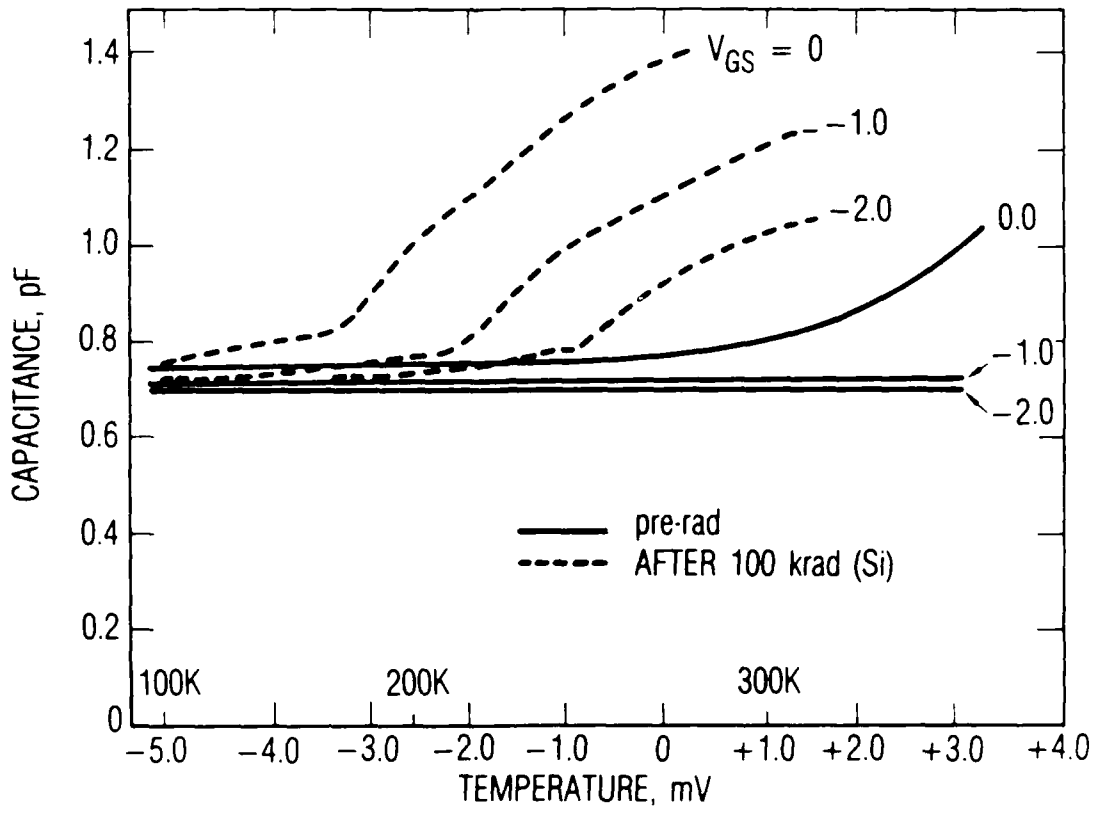

Fig. 10. Capacitance as a Function of Temperature for an Enhancement-Mode JFET Prior to and Following Irradiation to a Dose of 100 krad(Si)

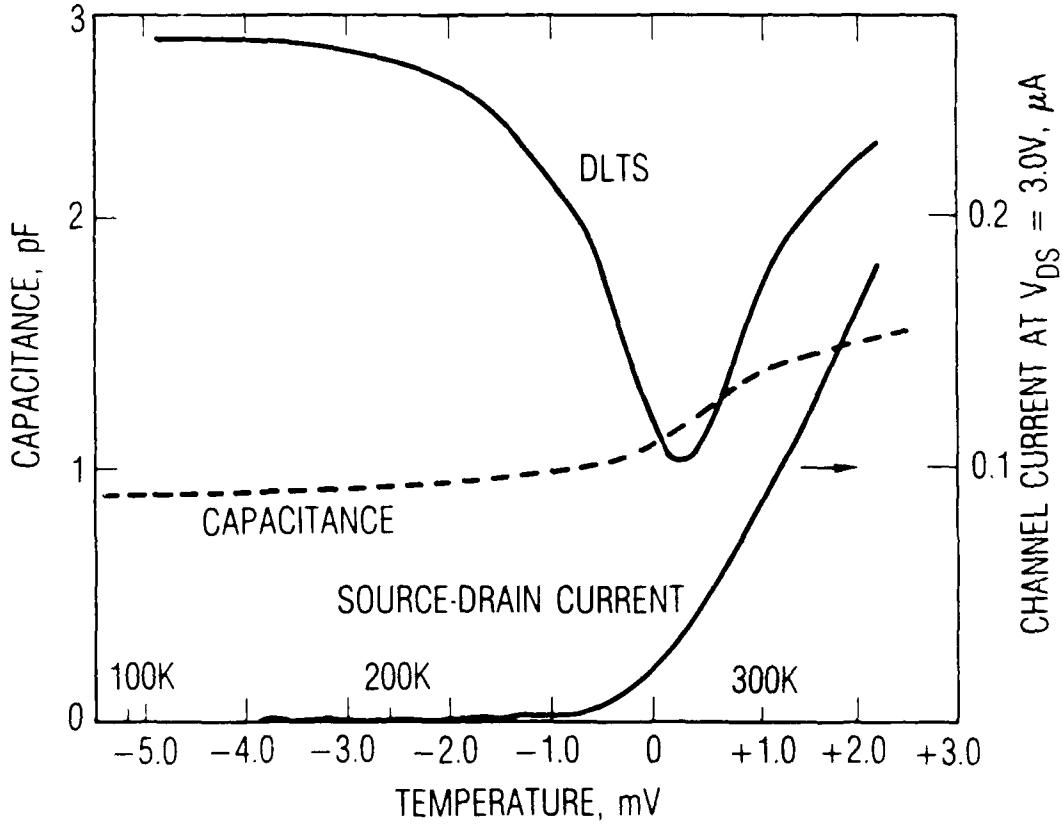

Fig. 11. DLTS Signal, Capacitance, and Source/Drain Current as a Function of Temperature for an Enhancement-Mode JFET Irradiated to 100 krad(Si). The rate window for the DLTS signal was 128 sec^{-1}.

current occurs at about the same temperature as the capacitance step and the peak of the trap band. This implies that the alteration in charge which results from emission from the interface states causes an increase in the capacitance of the channel; the resulting shrinkage of the depletion layer, in turn, allows current to begin to flow. In other words, the emission from interface states plays some role in lowering the threshold voltage of the device.

IV. CONCLUSION

Contrary to previous explanations of radiation-induced changes in device parameters, the results of our experiments, which combine measurements of transistor parameters with DLTS measurements, reveal the properties expected for both trapped-hole charge and interface-state growth. The degradation of transistor parameters with irradiation, and the dependence of this degradation on the presence of a source/drain bias, have been observed previously and attributed to the trapping of holes in the sapphire near the Si/sapphire interface.[3-5] The presence of a fringing field caused by V_{DS} allows the hole trapping to occur by separating holes from electrons. In addition, the recovery of transistor parameters to their pre-irradiation values after a device is further irradiated with its drain at zero bias also points to the presence of a trapped charge that is neutralized by a flood of electrons. On the other hand, because of the lack of communication with the Si conduction band, one would not expect the trapped-hole charge in the sapphire to manifest itself as a DLTS band. Moreover, the temperature-dependent steps in the C-T data, which we attribute to the emission of electrons from interface states, cannot be accounted for by trapped holes in the sapphire. The fact that the postirradiation DLTS band also diminishes to its pre-irradiation value when further irradiated with the drain biased at 0 V indicates that the detection of electron traps depends on the presence of trapped holes at the interface. This may be due to a local field created by this trapped charge. As a speculative conclusion, we suggest that the trapping of holes in the sapphire is accompanied by the formation of negatively charged states in the Si band gap, and that these two processes are strongly interrelated in the case of these JFET/SOS structures.

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