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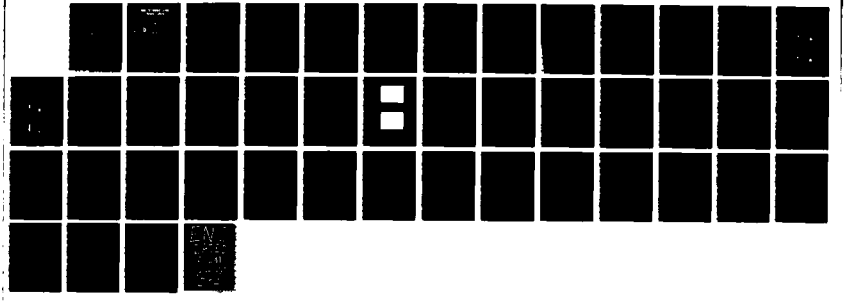

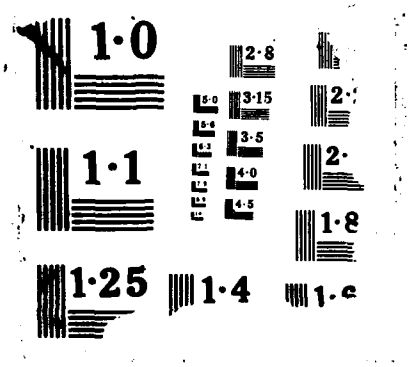
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NAVAL POSTGRADUATE SCHOOL
Monterey, California

THESIS

FREQUENCY HOPPING
WITH ANALOG MESSAGES

by

Suwito Kardisan

March 1988

Thesis Advisor G. A. Myers

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All presently known frequency hopping (FH) systems transmit digital data. Consequently a clock is a typical part of the system. This research consists of a breadboard realization of a FH transmitter and receiver. Voice and/or music in analog form are transmitted using a FH carrier. Hopping is random in time and pseudo-random in frequency. The message which is recovered and heard using a speaker is of good quality.

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Frequency Hopping
with Analog Messages

by

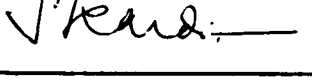
Suwito Kardisan
Major, Indonesia Air Force
B.S., Indonesia Air Force Academy , 1968

Submitted in partial fulfillment of the
requirements for the degree of

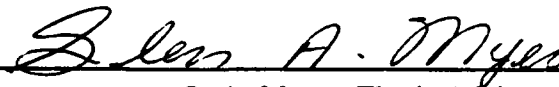
MASTER OF SCIENCE IN ELECTRICAL ENGINEERING

from the

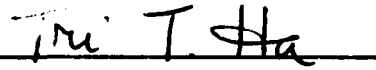
NAVAL POSTGRADUATE SCHOOL
March 1988

Author: 

Suwito Kardisan

Approved by: 

G. A. Myers, Thesis Advisor



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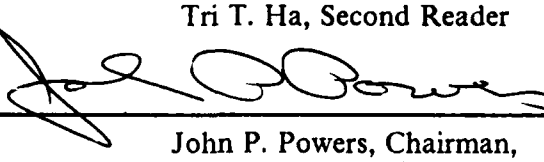

John P. Powers, Chairman,
Department of Electrical Engineering Science

Gordon E. Schacher,
Dean of Science and Engineering

ABSTRACT

All presently known frequency hopping (FH) systems transmit digital data. Consequently a clock is a typical part of the system. This research consists of a breadboard realization of a FH transmitter and receiver. Voice and/or music in analog form are transmitted using a FH carrier. Hopping is random in time and pseudo-random in frequency. The message which is recovered and heard using a speaker is of good quality.

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The author is indebted to Professor G. A. Myers for his patient guidance and knowledge during various development of my thesis. Also I wish to express my appreciation to Gloria White and Lily Nimri from the ECE supply department, Lt. Joseph T. James from US Navy and Major Lee Whan Su from Korea AF for their help and cooperation.

I. INTRODUCTION

Frequency hopping (FH) is used by the military as an electronic counter-countermeasure (ECCM) technique. The carrier frequency is caused to vary from one value to another over a range of values in usually a random or pseudo-random manner, as shown in Fig. 1. The message is converted to binary form. In slow FH, several bits are sent per hop. In fast FH, several hops occur per bit. The literature contains descriptions and analyses of various FH systems [Refs. 1,2,3,4].

This research considers use of analog messages (voice) with FH. No analog to digital conversion is used. An important consequence is that there is no clock in the system. Hopping can be and should be random in time as well as in frequency. This hopping is represented by Fig. 2.

A FH transmitter and receiver were built and tested using analog messages. The message is carried using amplitude modulation. This permits recovery of the message asynchronously in the receiver using an envelope detector. Further, an envelope detector is relatively insensitive to variation in frequency of the carrier. Clocked (pseudo random) FH is used with receiver hopping synchronization provided by hard wire. The voice signal was recovered (heard) with little apparent distortion.

Random hopping is also employed with noise determining each hop time. A receiver self synchronizing circuit was designed and used in this case. Because of the chosen design, interference and amplitude fluctuation of the recovered audio (intelligible) is experienced. (Keywords: Thesis; circuit [illegible]).

Chapter II provides background material on FH. The experimental system is described in Chapter III. Results are presented in Chapter IV. Conclusions and recommendations are listed in Chapter V. Various circuit descriptions and calculations are contained in the Appendix.

II. BACKGROUND

Frequency hopping is an antijam (AJ) communication technique. By varying the carrier frequency, a transmitter forces a jammer to spread the interference power over a wide band of frequencies. Or, the jammer must accept a reduced probability of effective jamming.

In conventional FH, the frequency f_c of the carrier $A\cos 2\pi f_c t$ is caused to vary in a discrete manner as shown in the frequency/time diagram of Fig. 1. A system clock controls the hopping rate equal to $\frac{1}{\tau}$ hops per sec. Binary data is sent by offsetting the hop pattern by one or more frequency cells for a binary 1 (or 0). Alternatively, m bits may be sent in τ seconds where m is a positive integer. This is called slow FH. If n hops occurs in the duration of the bit, then fast FH results. Again, n is a positive integer. The presence of the periodic clock signal can be exploited by an unintended receiver.

The need for a clock is avoided by using an analog message. The carrier must be then modulated in a continuous fashion using AM or FM. Because FH is a kind of FM, it was decided in this application to use AM to carry the analog message. This means that the receiver can use an envelope detector which is relatively insensitive to frequency and is an asynchronous demodulator. Therefore, the need to synchronize the receiver for demodulation is avoided. It is still necessary, however, to dehop the received carrier in the receiver.

The synchronization necessary to track the hopping carrier can be done in a variety of ways. A separate synchronizing signal can be sent (radiated), or the necessary synchronization can be recovered from the received FH carrier with a hopping recovery circuit. Two types of synchronization were used in this research. First, a hard wire connected to the transmitter in the laboratory provided the necessary synchronization to the receiver. Then, when random hopping was used, an attempt was made to recover the synchronization. The chosen design successfully recovered the audio signal but, with distortion.

This research established that frequency hopping can be used with analog messages. The advantages include the absence of a system clock which then makes possible truly random hopping of the frequency of the transmitted carrier.

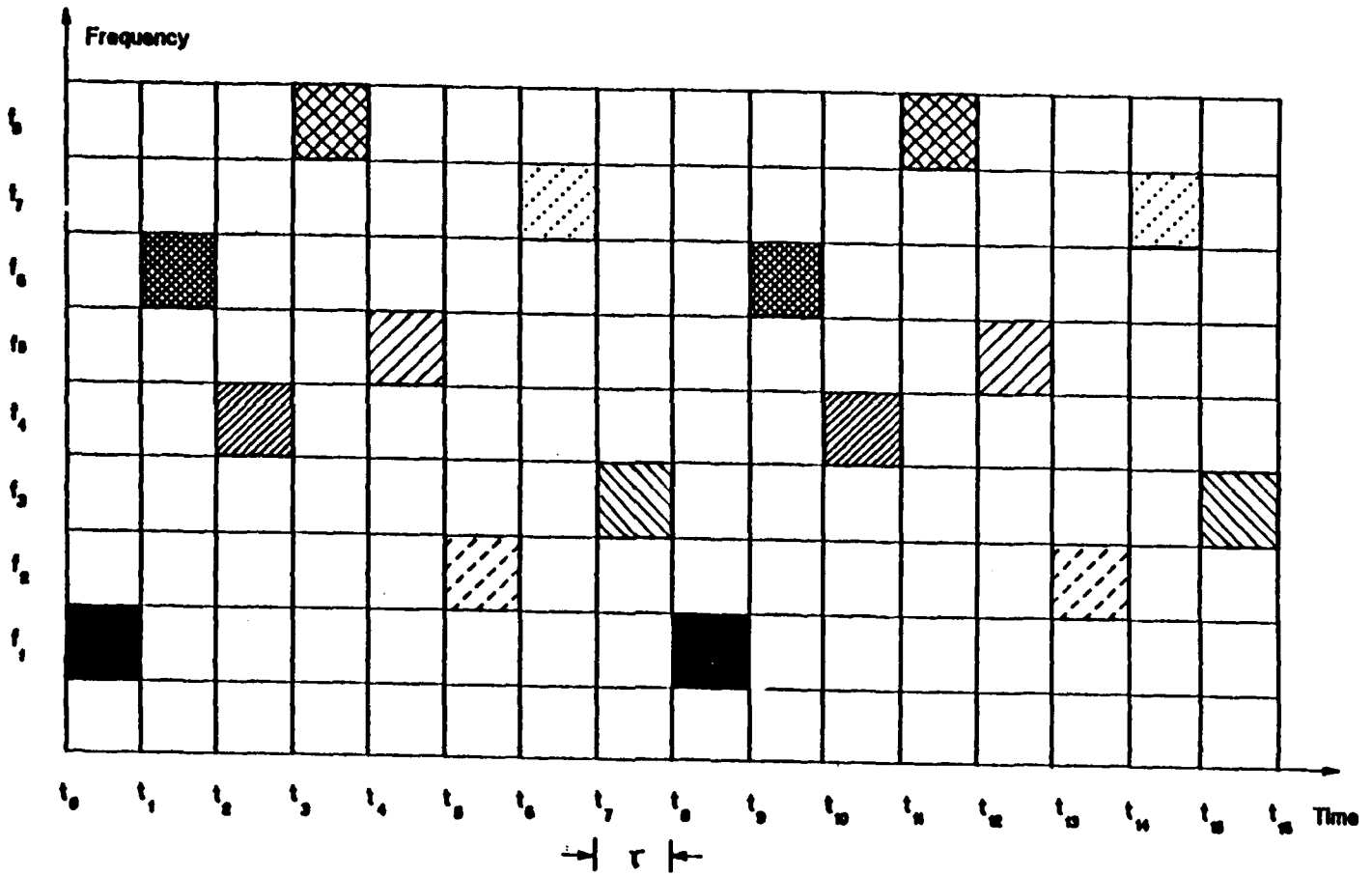


Figure 1. Frequency/Time Diagram

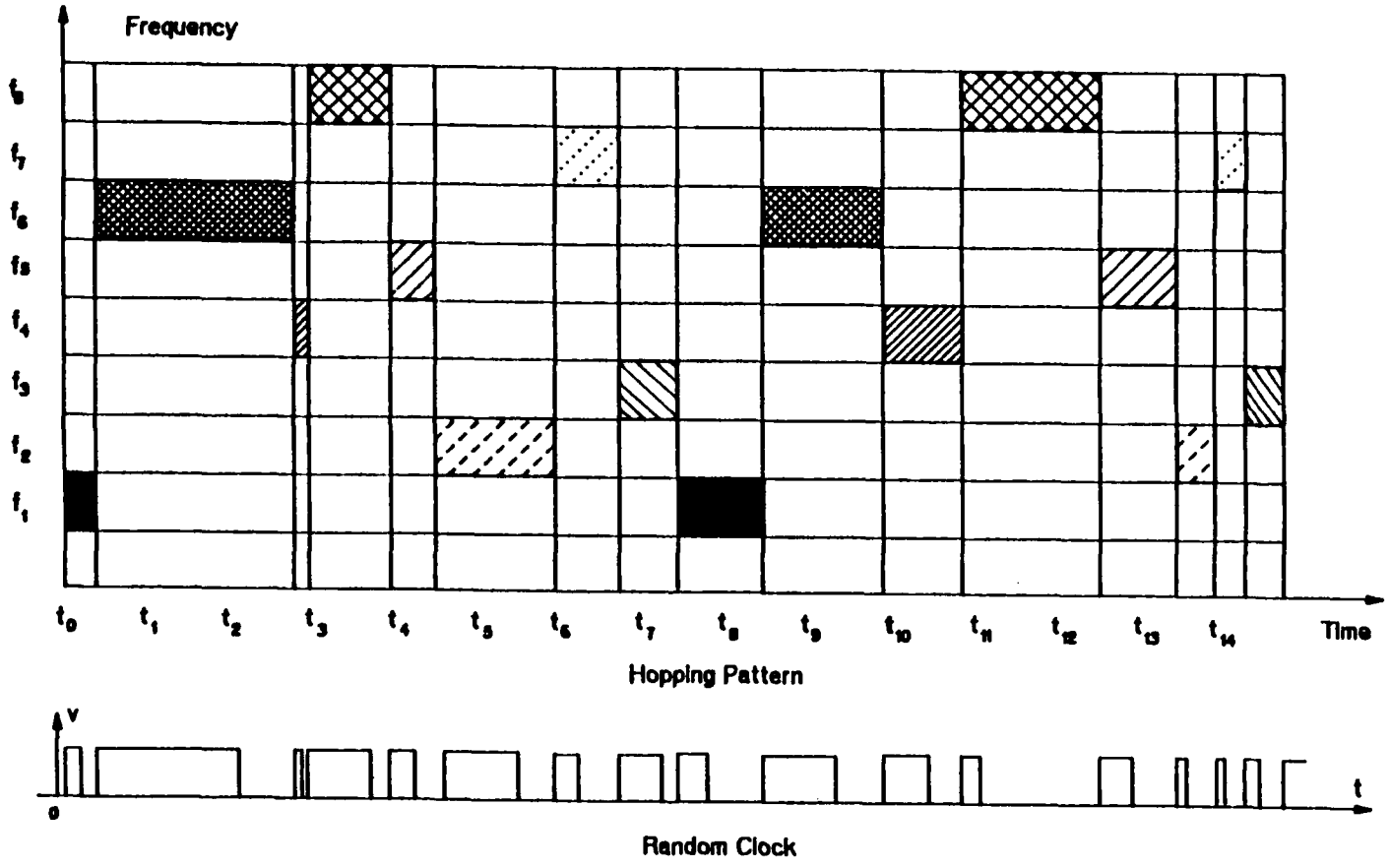


Figure 2. Frequency/Time Diagram Showing Hopping at Random Times

III. EXPERIMENTAL SYSTEM

A. GENERAL OPERATION

Figure 3 is a block diagram of the experimental system. The transmitter consists of a carrier modulator and a hopping frequency generator. The transmitter output is sent to the receiver using a piece of wire. No radiation occured in this experiment. Consequently, the system operates at low frequency (150 kHz - 194 kHz hop range).

The receiver consists of a mixer which is used to dehop the received carrier by means of a hopping local oscillator. The hopping recovery circuit of Fig. 3 provides a sinusoid which hops in the same manner as the received signal. Therefore, the mixer output is a constant frequency, amplitude modulated sinusoid. A bandpass filter is used to simulate the intermediate frequency amplifier (IFA) in a conventional superheterodyne radio receiver circuit. The filtered, amplified and dehopped signal is then envelope detected to recover the message. The message, which is a voice signal in this application, is then amplified and heard through a speaker.

B. TRANSMITTER

The transmitter consists of the hopping frequency generator and amplitude modulator as shown in Fig. 3. The analog message source is the output of a conventional radio tuned to a local broadcast station. The hopping frequency generator is described next.

1. Hopping Frequency Generator

The hopping frequency generator creates a sinusoid whose frequency is caused to vary in a pseudo random or truly random manner as a function of time. A hopping voltage is created. That variable voltage level is then applied to a voltage control oscillator (VCO) to create a hopping frequency. A block diagram of the hopping frequency generator is shown as Fig. 4. The hopping voltage is created by converting the contents of a shift register to a voltage level using a digital-to-analog converter. The shift register's contents are caused to vary in a pseudorandom manner by using feedback from particular stages to the input. The contents of the shift register change with the application of each clock pulse. In this research both a regular clock pulse and a random clock pulse are employed. The regular clock pulse is obtained directly from a function generator using a square wave output. The random clock pulse is obtained using a clock circuit.

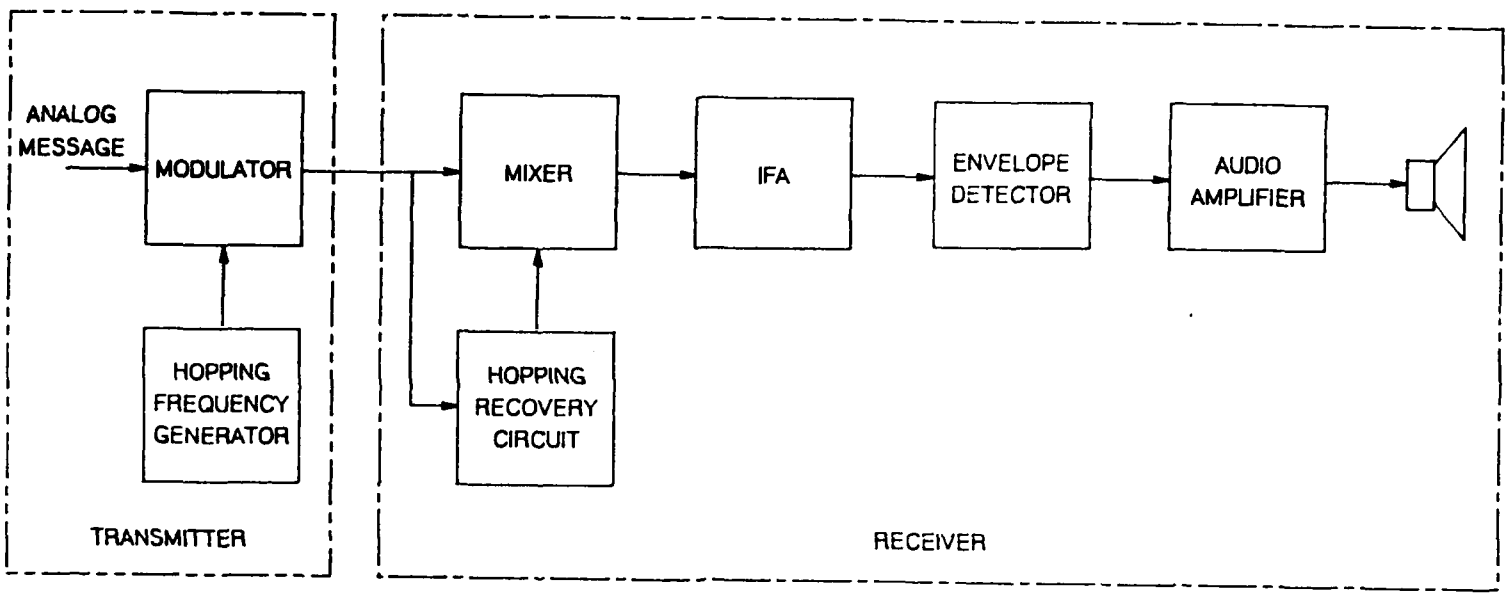


Figure 3. Block Diagram of the Experimental System.

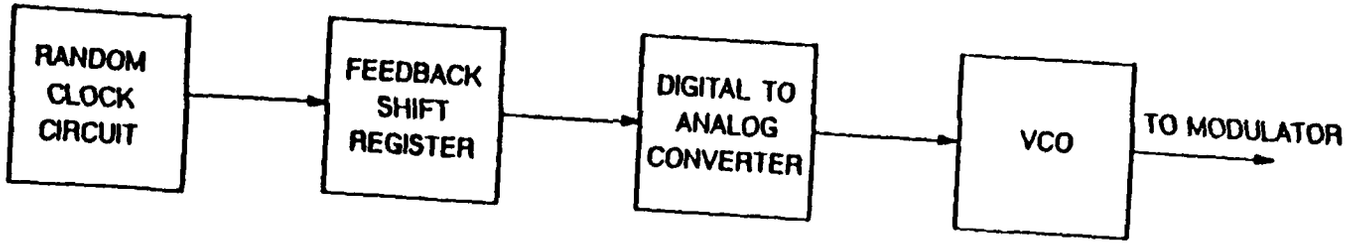


Figure 4. Block Diagram of the Hopping Frequency Generator.

a. The Random Clock Circuit

It is desired to create a clock pulse which occurs randomly in time. To achieve this, Gaussian noise is used. See Fig 5. (In this report, all capacitors are in μF and resisistors are in ohm unless otherwise indicated.) The output of the Gaussian noise generator is applied to the noninverting input of a comparator. The inverting input is a constant +5 volts. The output is the binary representation of the difference of these two voltages. A potentiometer controls the average frequency of the random clock pulses. Whenever the output of the noise generator exceeds the constant voltage reference, a clock pulse is generated. Since the peak values of the Gaussian noise occur randomly, the clock pulses also occur randomly. These randomly occuring clock pulses are conditioned by a diode circuit and then applied to the feedback shift register.

b. The Feedback Shift Register

The contents of the feedback shift register (FSR) can be represented by a binary number which changes as each clock pulse is applied. The following sequence was chosen for this application : 0000, 1000, 0100, 1010, 0101, 0010, 1001, 0011, 0000. This sequence was chosen to accomodate the receiver circuitry which is considered later in this chapter. Although the hopping from cell to cell is not random with this sequence, the hopping cycle is because of the random time at which the hops occur. See Fig. 2. The contents of the feedback shift register are converted to a voltage level using a digital-to-analog converter.

c. The Digital-to-Analog Converter

The digital to analog converter (DAC) chip DAC0800 is used to change the contents of the feedback shift register to a discrete voltage level. Each voltage level remains constant until the next clock pulse is applied to the feedback shift register. The DAC output is shown as Fig. 6. The output of the DAC is amplified to control the peak-to-peak voltage applied to the voltage controlled oscillator. This control establishes the hopping range of the broadcast carrier.

d. The Voltage Controlled Oscillator

In this research a model 142 WAVETEK signal generator is used as a VCO to produce the hopping carrier. An example of the hopping carrier is shown in Fig. 7. Values of the hopping frequency and the relationship to the DAC output and FSR content are listed in Table 1.

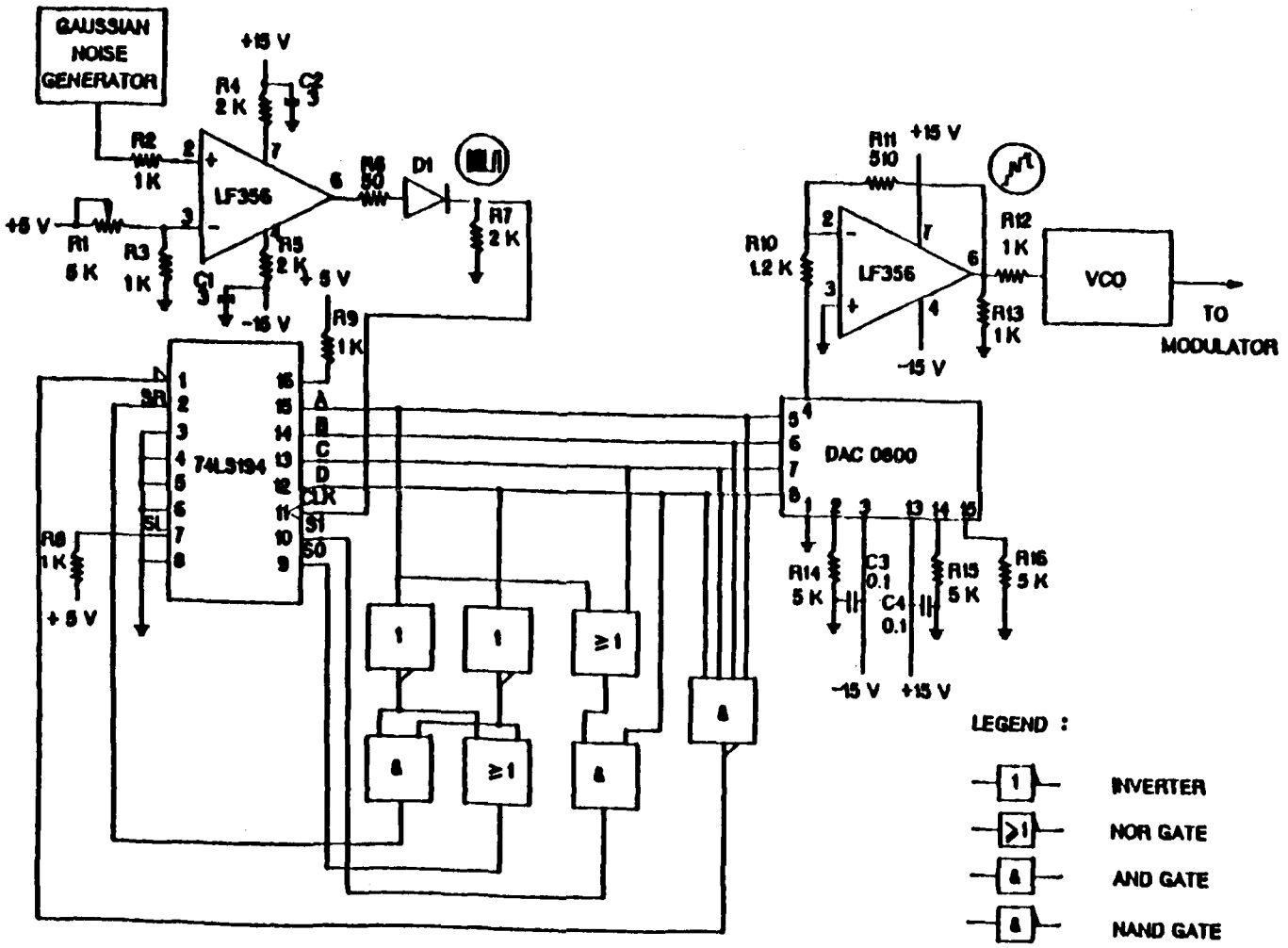


Figure 5. Schematic Diagram of the Hopping Frequency Generator.

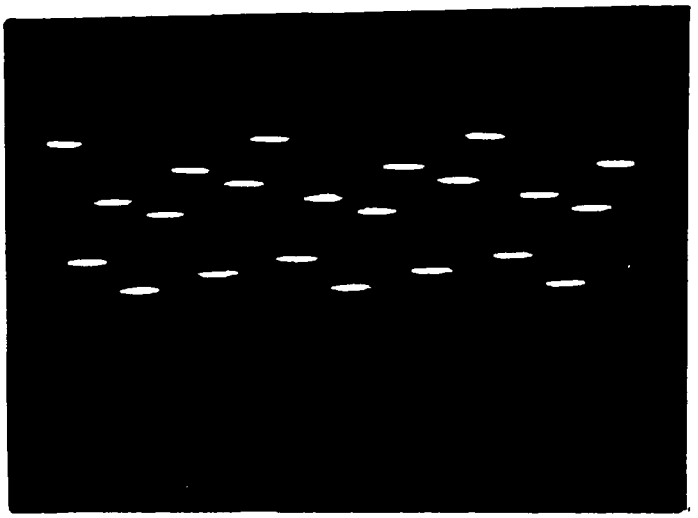


Figure 6. Photograph of the Digital to Analog Converter Output.

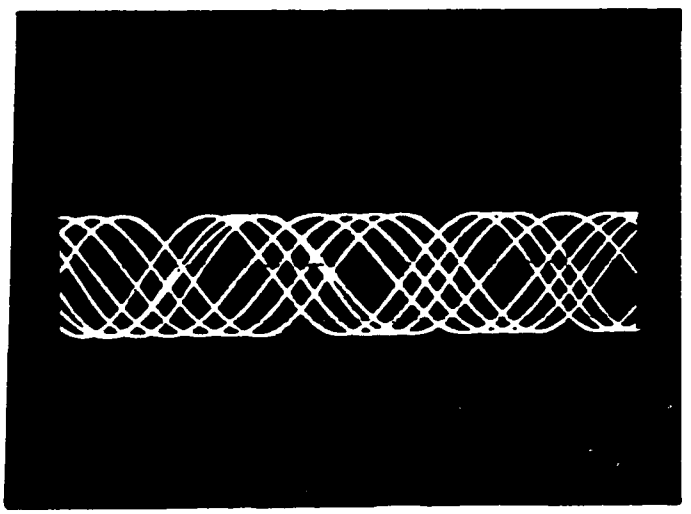


Figure 7. Photograph Showing Hopping Carrier.

Table 1. THE HOPPING SEQUENCE.

Bit Number	Voltage (volt)	Frequency (kHz)
0000	0.01	150.3
1000	0.34	184.8
0100	0.18	167.5
1010	0.43	193.4
0101	0.22	171.8
0010	0.09	159
1001	0.39	189.1
0011	0.14	163.3
0000	0.01	150.3

2. Modulator

The modulator is an analog voltage multiplier (AVM). The input to the AVM are the hopping carrier and the message. The output of the AVM is double side band amplitude modulation with a carrier component. The carrier component is created by adding DC voltage to the message before multiplication. The analog message in this experiment is voice and music.

Figure 8 is the schematic diagram of the modulator. Let m(t) be the message. Then the output of the modulator is $v_c(t) = A[1 + k_a m(t)]\cos 2\pi f_i t$. The carrier frequency f_i changes (hops) with time. The constant k_a is chosen so that the minimum value of m(t) times k_a is always greater than minus one. Consequently, with this condition, an envelope detector can recover the message without distortion. Figure 9 is an example of the spectrum of the modulated carrier where it is understood that f_i changes with time.

C. RECEIVER

The receiver block diagram is shown as part of Fig. 3. The function of the receiver is to first dehop the received carrier and then remove the message from the dehopped carrier.

The received carrier is dehopped by applying a local hopping frequency sinusoid to a mixer. When the local oscillator is hopping in the same manner as the received signal, the usable output of the mixer is a modulated carrier at the intermediate frequency (IF) which is the difference between the two hopping frequency signals applied to the mixer.

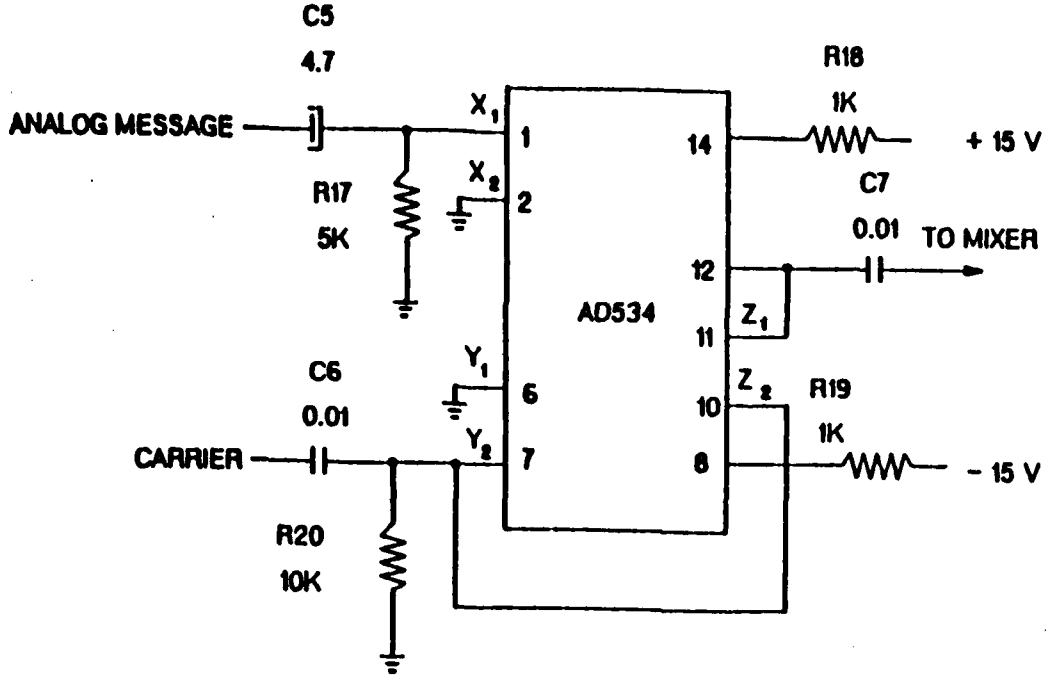


Figure 8. Schematic Diagram of the Modulator.

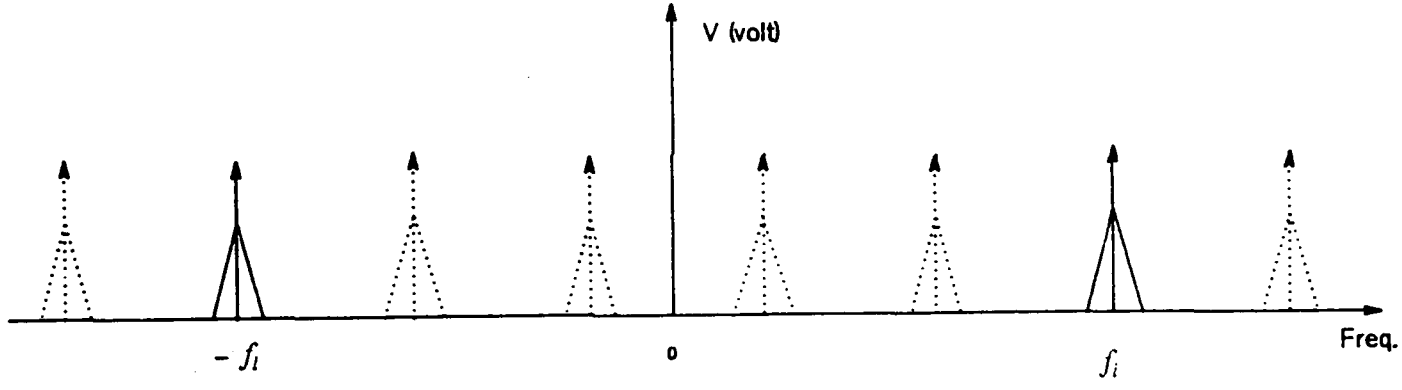


Figure 9. An example of the Spectrum of the FH Modulated Carrier.

1. Hopping Recovery Circuit

The function of the hopping recovery circuit is to create a sinusoid whose frequency changes in the same manner as that of the received signal. Two approaches are used in this research.

In the first approach the hopping voltage generated in the transmitter was applied directly to a voltage controlled oscillator in the receiver. By matching the VCO characteristics in the transmitter and the receiver, it is possible to obtain a hopping frequency in the receiver which is like that at the output of the transmitter.

In the second approach, when random hopping is used, it was decided to recover the hopping frequency from the received signal directly. This is accomplished by first initializing the feedback shift register which is part of the hopping recovery circuit as shown in Fig. 10. This sequence initialization is accomplished with the synchronizing signal.

The synchronizing signal resets the shift register to a particular state corresponding to the frequency of the received signal at that instant. The synchronizing signal is obtained by first converting the carrier frequency to a voltage and then using a voltage window circuit whose output corresponds to one of the frequencies in the transmitter hop pattern. Since this frequency corresponds to a known shift register state, it is possible to initialize an identical shift register in the receiver. It is then only necessary to step the shift register in the receiver as the frequency of the received signal changes. A circuit to detect the change in frequency of the input is required. Creation of the timing signals of Fig. 10 (clock and reset pulses for the feedback shift register in Fig. 10) begins with the frequency-to-voltage converter.

a. Frequency-to-Voltage Converter

The frequency-to-voltage converter detects a change in the frequency of the transmitter output. A step in voltage is produced whenever the carrier frequency changes. The step change in voltage is then differentiated to form a pulse at the hop time of the received signal. This pulse then steps the feedback shift register of Fig. 10 to ultimately change the frequency of the local oscillator in the receiver.

A phase-locked loop is used as the frequency-to-voltage converter. The VCO free running frequency, the lock range and the capture range of the NE565 PLL IC are 171.5 kHz, 85 kHz and 10 kHz respectively.

To prevent fluctuation in the output of the PLL during a hop interval, it is necessary to remove the AM of the received signal. This is done using a hard limiter.

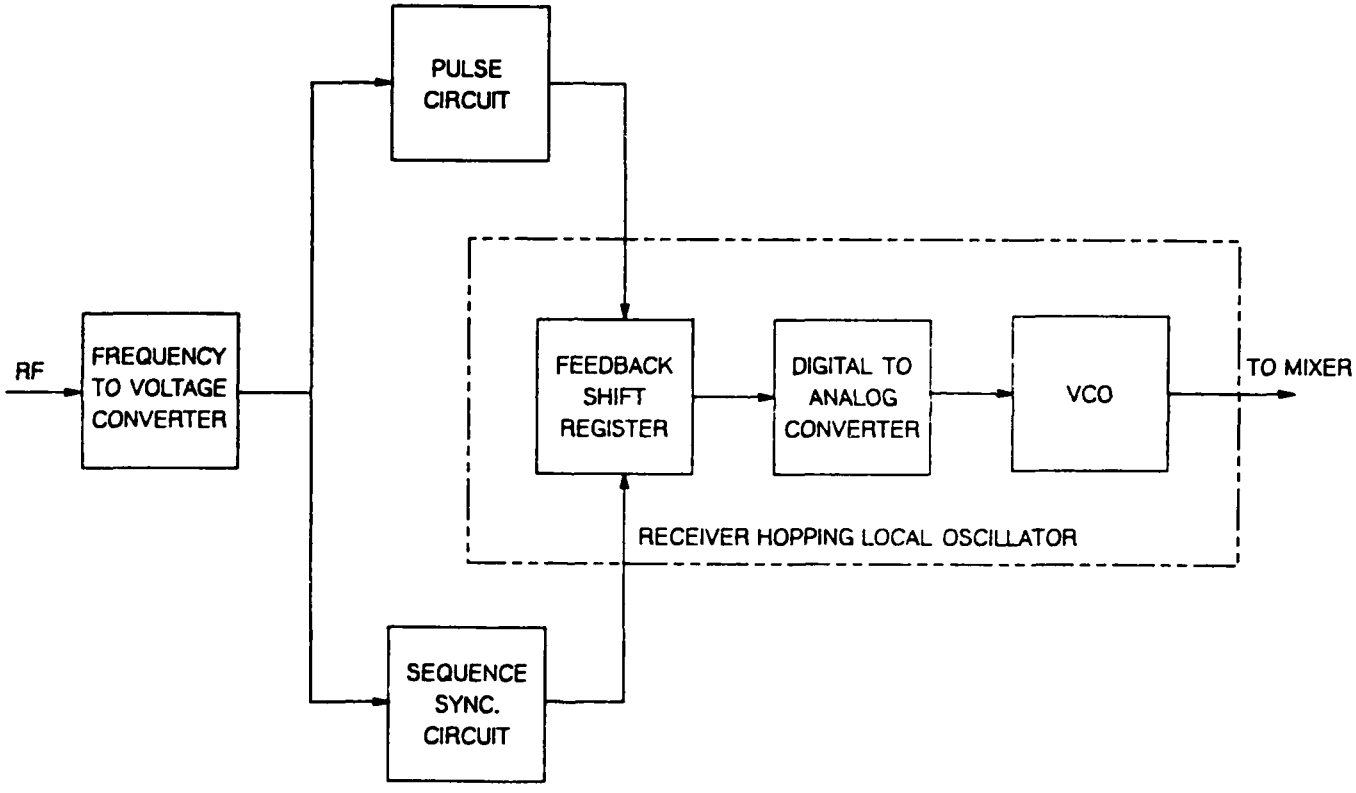


Figure 10. Block Diagram of the Hopping Recovery Circuit.

A bandpass filter receives the square wave output of the hard limitter and converts it to a sine wave input to the PLL. Figure 11 is a schematic diagram of the frequency-to-voltage converter [Refs. 4,5].

b. Pulse Circuit

The pulse circuit generates pulses suitable for changing the sequence in the feedback shift register whenever the frequency of the received signal hops to a new value. This is accomplished by differentiating the step voltage at the output of the frequency-to- voltage converter. Since the step output can increase or decrease in value, it is necessary to form the absolute value of the differentiator output. These unipolar pulses trigger a one shot multivibrator to create pulses of uniform amplitude for use by the feedback shift register. A schematic diagram of the pulse circuit is shown as Fig. 12 [Refs. 4,5].

A shift register, DAC, and VCO complete the receiver hopping local oscillator circuit as shown in Fig. 14 [Refs. 4,5]. These three subsystems replicate the design of the transmitter unit. The VCO characteristic is adjusted to create a constant intermediate frequency of 70 kHz.

c. Sequence Initializing Circuit

The FSR sequence is initialized whenever one particular chosen value of the various possible carrier frequencies is received. The PLL converts these various frequencies to corresponding voltage levels. The FSR is initialized by detecting a specific voltage level using a standard voltage window circuit consisting of appropriately connected op-amp as shown in Fig. 13 [Refs. 4,5]. The presence of the chosen frequency creates a voltage level in the circuit window which results in a pulse to reset the FSR.

2. Mixer

The function of the mixer is to create a fixed IF signal which is amplitude modulated by the message. This is accomplished by multiplying the received hopping signal and the hopping local oscillator signal. The product is formed with an AVM IC AD534 as shown in Fig. 15 [Refs. 4,5].

3. Intermediate Frequency Amplifier

The IFA removes the sum frequency component from the mixer output. This is accomplished with a bandpass filter having a center frequency of 70 kHz, a Q of 8.75 and a gain of 2. A schematic diagram of the IF amplifier is included in Fig. 16 [Ref. 6].

This IF amplifier performed satisfactorily when the receiver was synchronized with the signal from the transmitter. However, when the hopping frequency recovery

circuit was used and the carrier was randomly hopped, the IF amplifier allowed unwanted frequency terms to appear at the beginning of each hop while the receiver was adjusting to the change in frequency of the received signal. This created amplitude fluctuation, which was perceived as distortion in the recovered audio signal. To overcome this problem in future work, an attempt should be made to increase the Q of the IF amplifier thereby rejecting unwanted terms.

4. Envelope Detector

The envelope detector removes the message from the dehopped signal. The design of the envelope detector is shown in Fig. 17.

5. Audio Amplifier

The audio amplifier isolates the detector from the audio circuit and provides the power level necessary to drive the speaker. The design of the audio amplifier is shown in Fig. 18.

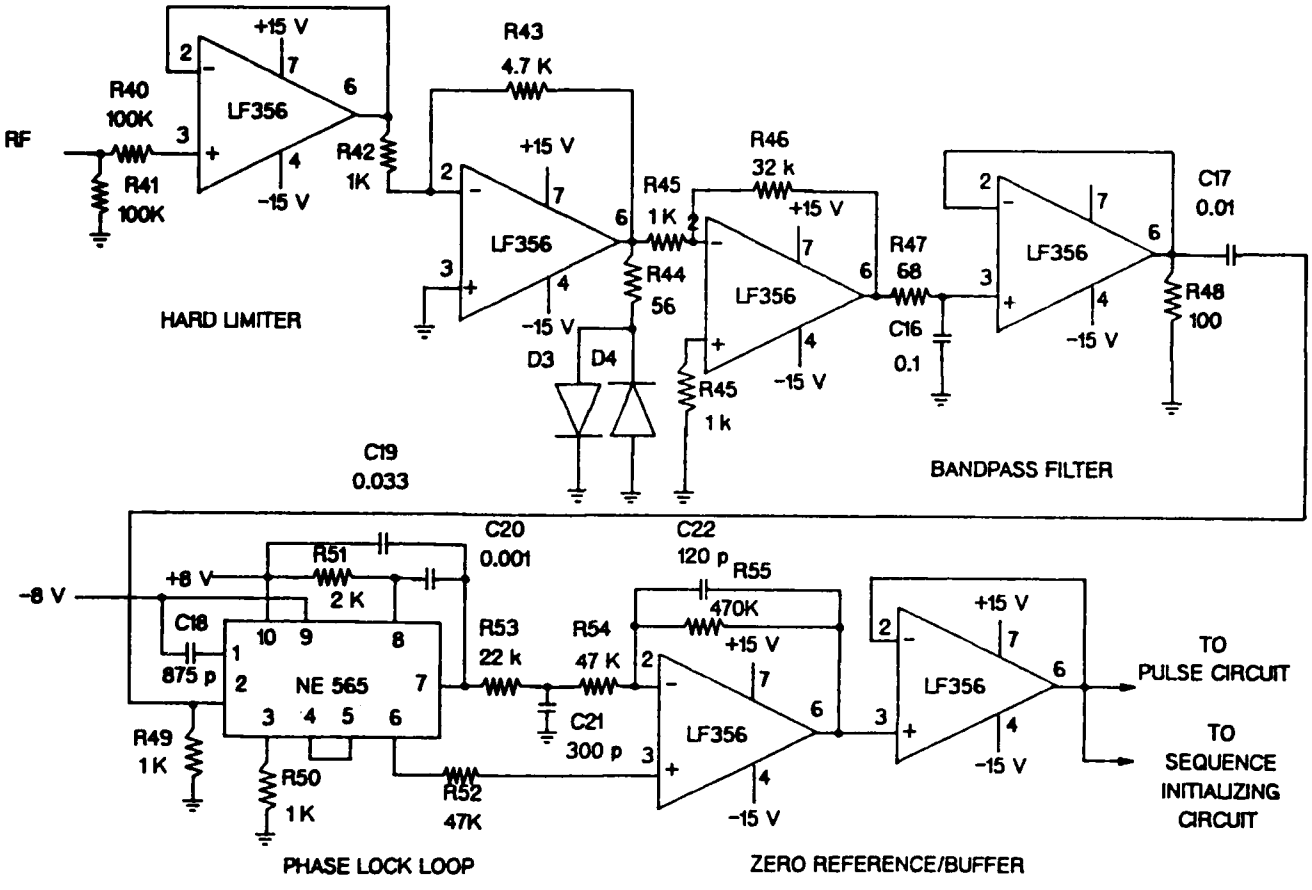


Figure 11. Schematic Diagram of the Frequency-to-Voltage Converter.

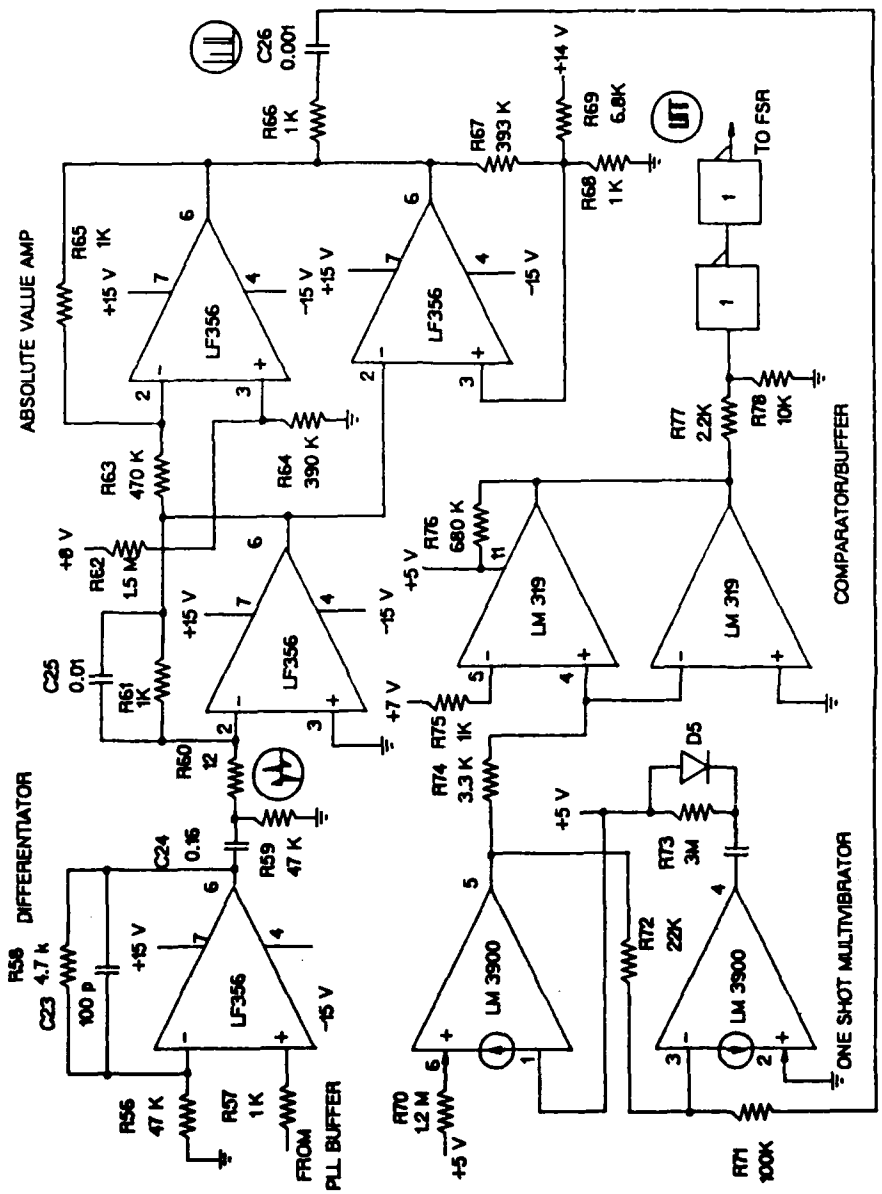


Figure 12. Schematic Diagram of the Pulse Circuit.

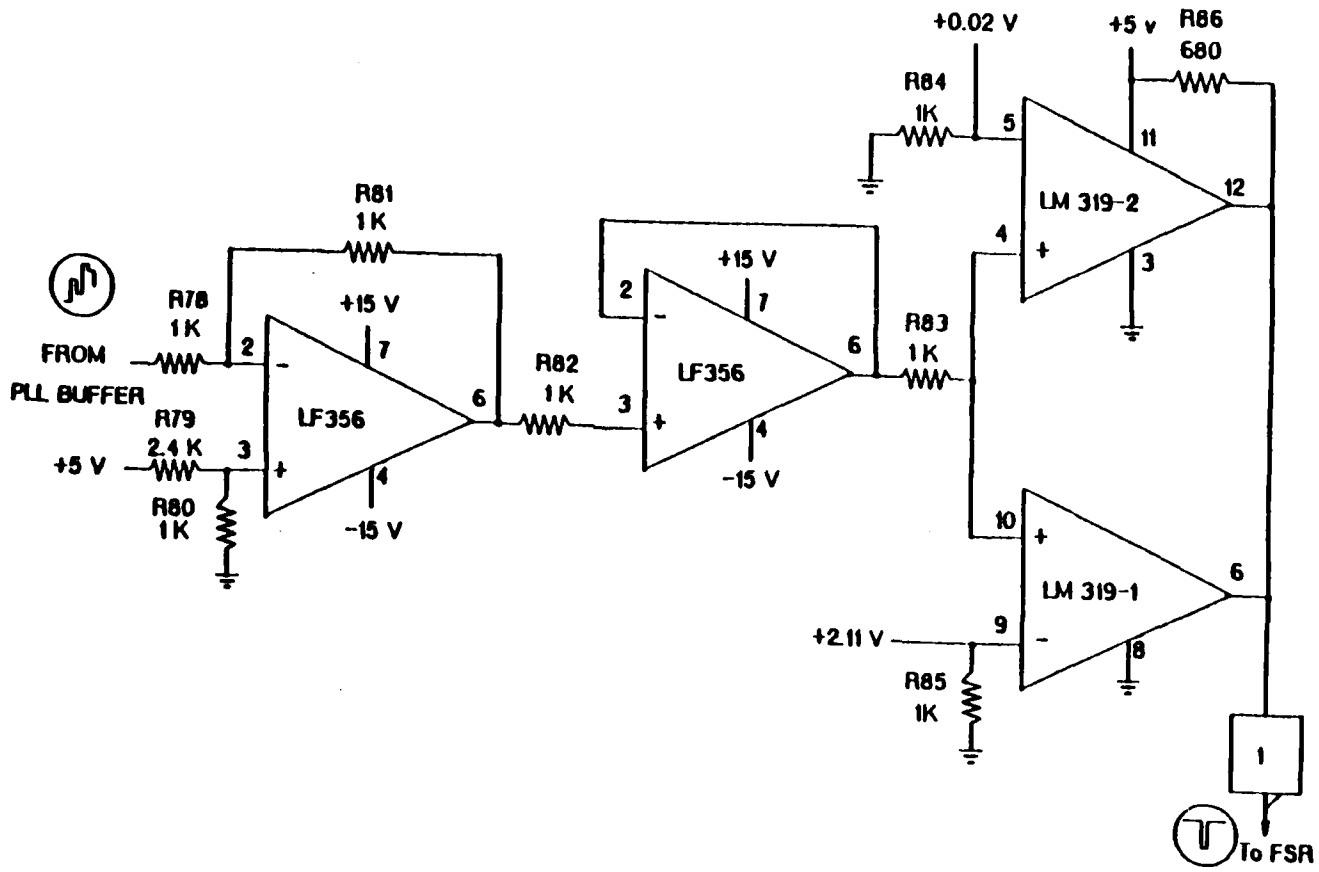


Figure 13. Schematic Diagram of the Sequence Initializing Circuit.

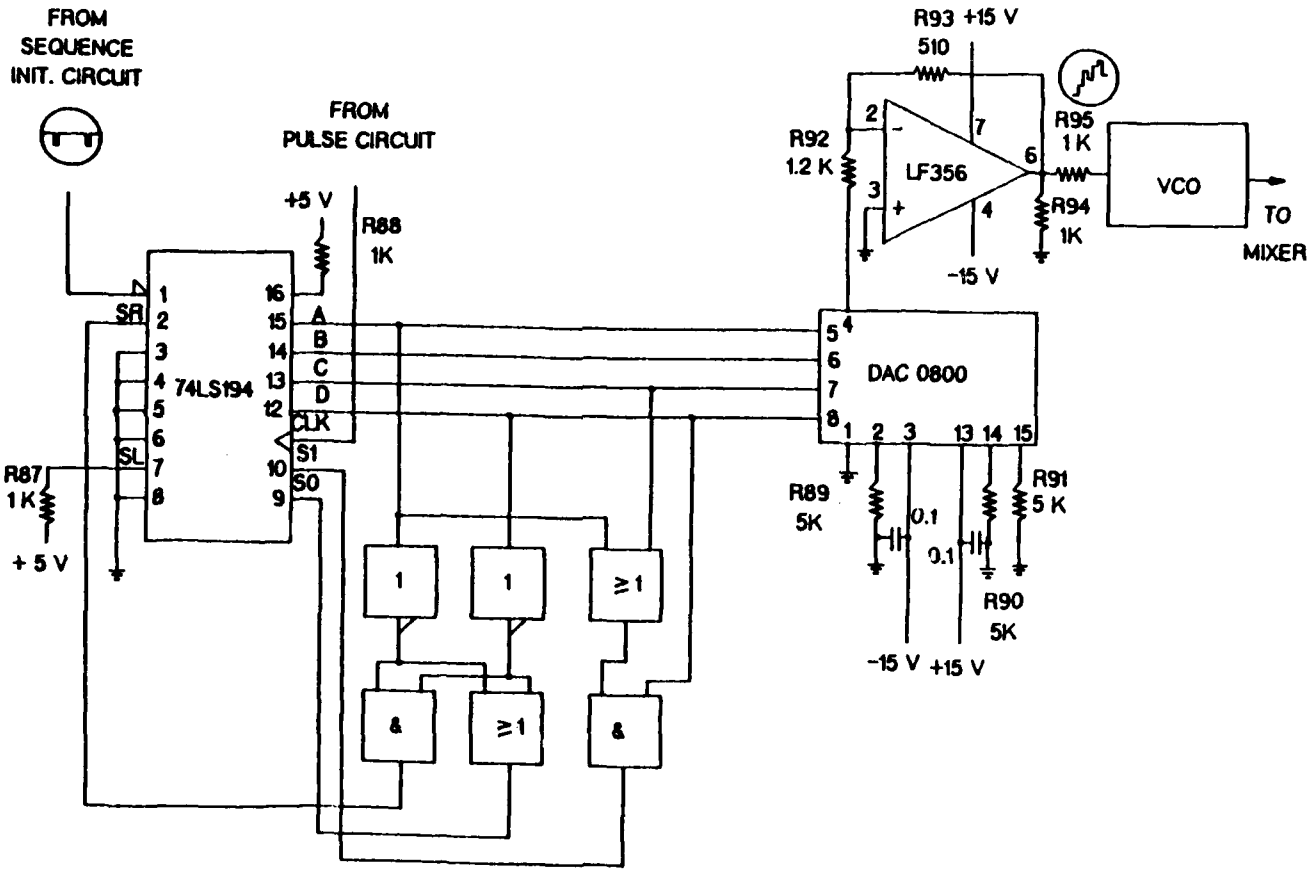


Figure 14. **Schematic Diagram of the Receiver Hopping Local Oscillator Circuit.**

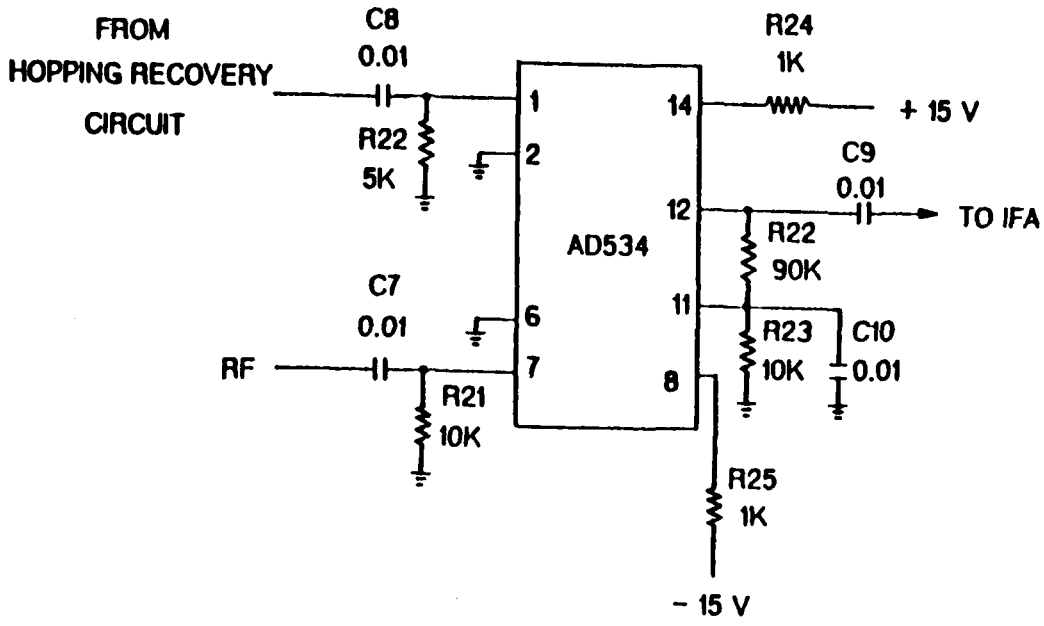


Figure 15. Schematic Diagram of the Mixer.

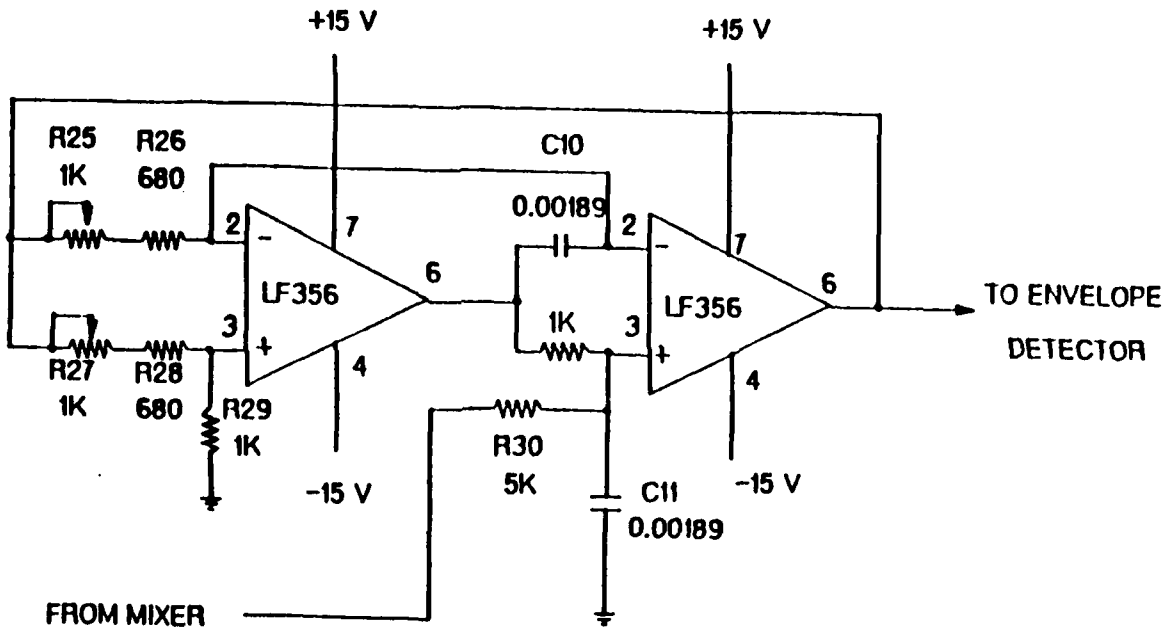


Figure 16. Schematic Diagram of the Intermediate Frequency Amplifier.

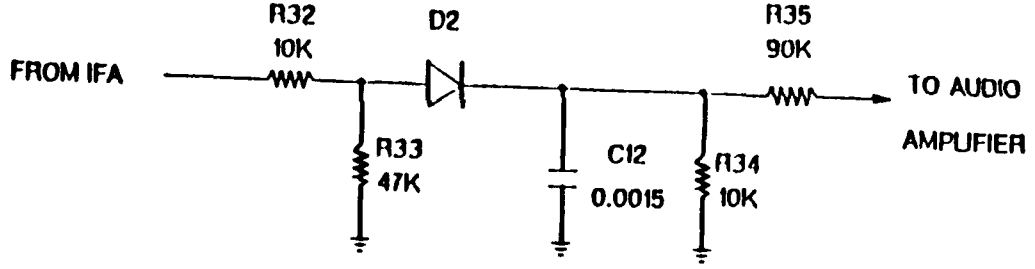


Figure 17. Schematic Diagram of the Envelope Detector.

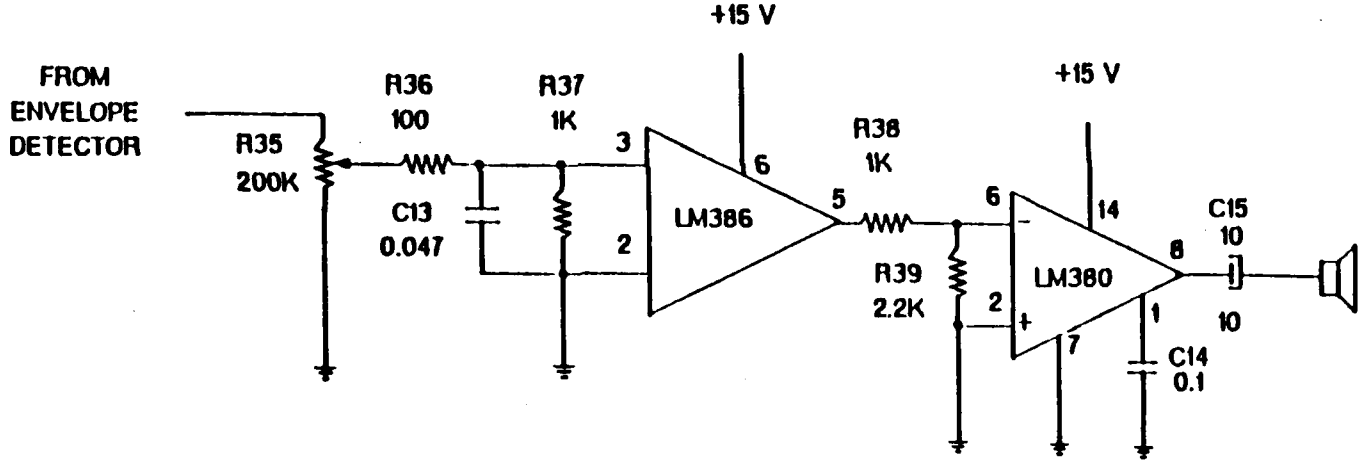


Figure 18. Schematic Diagram of the Audio Amplifier.

IV. RESULTS, CONCLUSIONS AND RECOMMENDATIONS

In general, the results of this research demonstrated that frequency hopping can be used with analog messages. This means that no clock signals are required in the transmission.

Specifically, an amplitude modulated frequency hopped carrier was created and sent to the receiver at a low frequency on a piece of wire. The effect of noise and interference is not considered in this research. The transmitted signal was caused first to hop regularly using a clock signal. Then random hopping was employed as described in Chapter III. In all cases the transmitter output was as expected. No difficulty was experienced in design and construction of the transmitter.

The received signal was dehopped in a conventional manner. In the case of random hopping, it was necessary to detect the hopping of the received signal with a circuit which used a frequency-to-voltage coverter and a differentiator. Delay experience in this process created distortion in the system output. This distortion can be reduced by minimizing the delay through further design. No attempt was made to optimize the dehopping circuit in the receiver. Rather, the motivation was to select the possible solution and to demonstrate that the receiver could be synchronized by using the received hopping signal. An improved filter characteristic of the IF amplifier would reduce considerably the distortion experienced when random hopping is used.

This experiment demonstrates the steps involved in designing a possible frequency hopping system using analog messages. It further shows that use of amplitude modulation with frequency hopping is possible. Good results were obtained when synchronization of the receiver was not a problem. It is recommended that consideration be given to other means of synchronizing the hopping local oscillator in the receiver with the hopping of the transmitted signal. Possible alternatives are use of a separate broadcast signal for synchronization, and other means in detecting a change in frequency of the received carrier.

APPENDIX CIRCUIT CALCULATIONS AND DESCRIPTIONS

To meet the requirement of the system, some external components are added to an IC and also several IC's are combined to complete a subsystem. The following calculations and descriptions are provided to clarify the experimental system performance. In the circuit diagrams, all capacitors are in μFd unless otherwise indicated.

A. MODULATOR CALCULATION

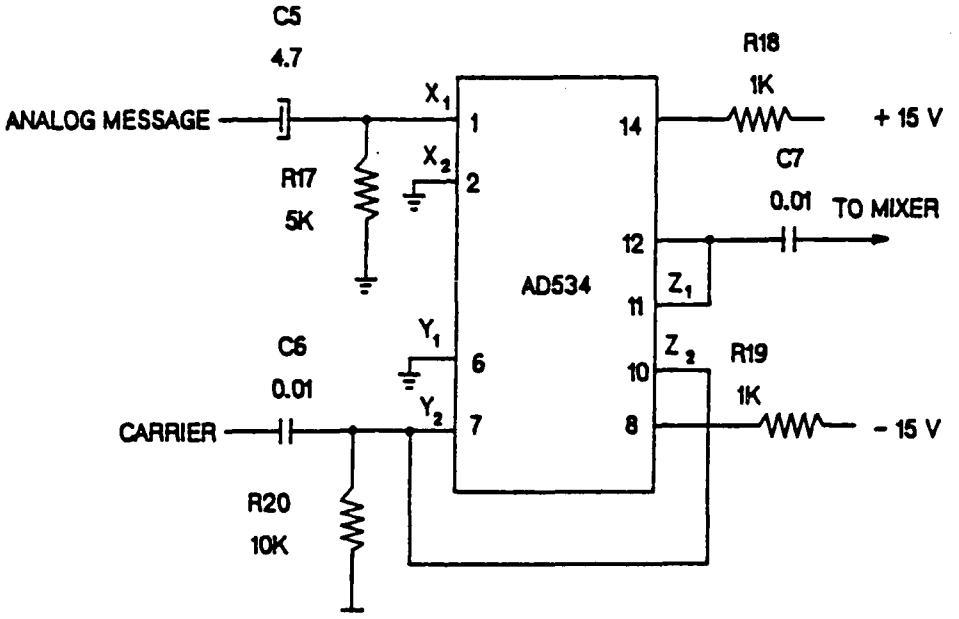


Figure 19. AM Modulator

An AD534 IC is used for an AM modulator as illustrated in Fig. 19. The analog message is applied to the modulator at X_1, while X_2 is grounded. So the input voltage is measured between X_1 and ground. C_5 blocks DC current from the message source. R_{17} provides a DC current path [Refs. 4,5].

The carrier is applied at point Y_2 through C_6 and measured with respect to ground since Y_1 is grounded. The DC path is provided by R_{20}. Feedback from Z_2 to Y_2 gives the scaling factor of 10.

The output voltage may be calculated by the equation:

$$V_{out} = \frac{A(X_1 - X_2)(Y_1 - Y_2)}{10} - (Z_1 - Z_2)$$

where A is the open loop gain of about 70 db.

B. MIXER

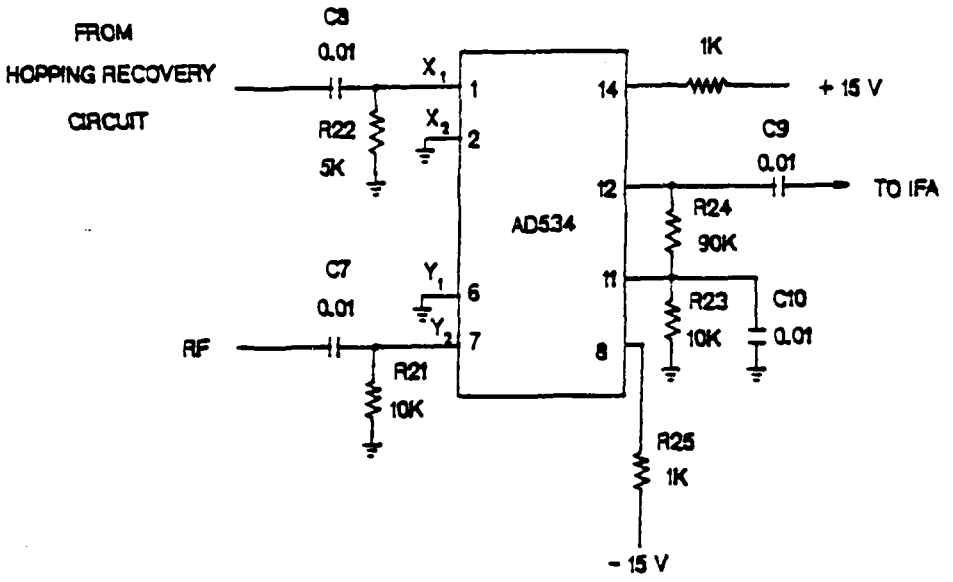


Figure 20. Mixer.

An AD534 IC is also used as a mixer. The signal from the hopping recovery circuit is fed to point X_1 while the RF signal is applied to point Y_2 through C_8 and C_7 respectively. R_{21} and R_{22} provide DCcurrent paths.

The scaling factor of the circuit is 1 and the output is taken from pin 12 with RC coupling R_{24} and C_9. R_{23} and C_{10} are a peaking eliminator [Refs. 4,5]. The output voltage is $V_{out} = X_1 Y_1$.

C. DIFFERENTIATOR

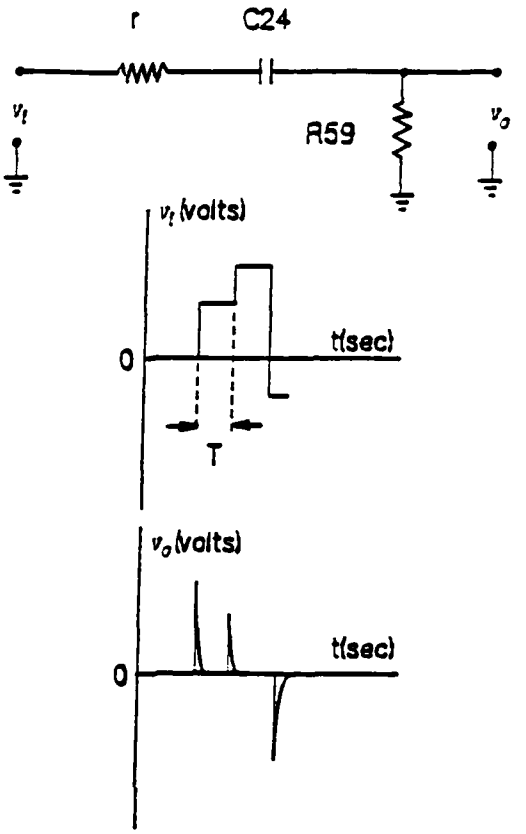


Figure 21. Differentiator.

Capacitive differentiation systems employ a series RC circuit with the output voltage v_o taken accross R_{59} . In this application, the circuit time constant RC is much smaller than T where T is the period of the input pulse [Ref. 7,8].

Considering the differentiator properties for a step input as applied in the experiment, an improper time constant will create two problems: opposite polarity output and zero output. The first problem is solved by applying the output to an absolute value circuit. And the second problem can be avoided by choosing a proper value of R_{59} and C_{24} as shown in the circuit, while r is the output impedance of the buffer.

The output amplitude is:

$$v_o = (\frac{R_{59}}{R})v_i$$

where,

$R = r + R_{59}$

D. FSR CONTROLLER

The FSR is intended to produce a sequence of 0000, 1000, 0100, 1010, 0101, 0010, 1001, 0011 and 0000. Also the FSR should be reset automatically when the outputs are high. To satisfy this need, all of the FSR outputs are fed to a Nand gate and its output used to control the FSR Reset. The FSR truth table is given in Table 2. The state sequence and the controller Karnaugh map are illustrated in Fig. 22 and Fig. 23 respectively.

Table 2. THE FSR TRUTH TABLE.

No	State	S1	S0	SR	SL
0	0000	0	1	1	X
1	0001	X	X	X	X
2	0010	0	1	1	X
3	0011	1	1	X	X
4	0100	0	1	1	X
5	0101	0	1	0	X
6	0110	X	X	X	X
7	0111	X	X	X	X
8	1000	0	1	0	X
9	1001	1	0	X	1
10	1010	0	1	0	X
11	1011	X	X	X	X
12	1100	X	X	X	X
13	1101	X	X	X	X
14	1110	X	X	X	X
15	1111	X	X	X	X

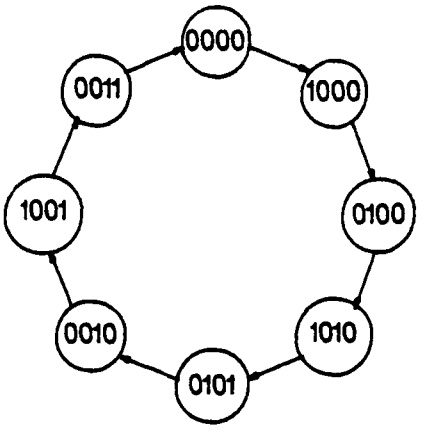
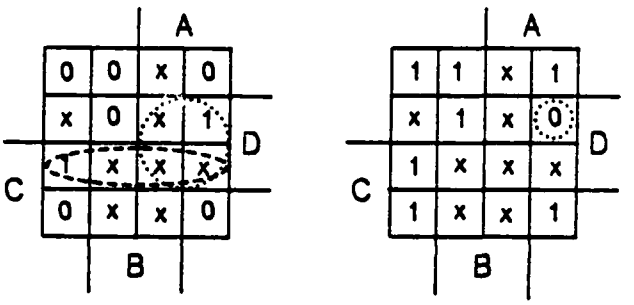
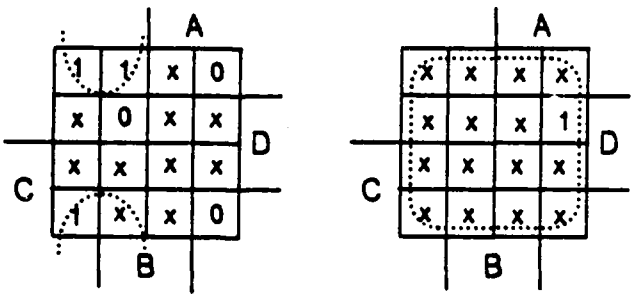


Figure 22. FSR State Sequence.



$S_1 = AD + CD = D(A + C)$ $S_0 = \bar{A} + \bar{D}$



$SR = \bar{A}\,\bar{D}$ $SL = 1$

Figure 23. FSR Karnaugh Map.

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