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COMPOUND SEMICONDUCTOR MATERIALS, DEVICES AND CIRCUITS

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This one year research program on compound semiconductor materials growth, devices and circuits has focused on: (a) organometallic vapor phase epitaxy (OMVPE) of GaInP/gaAs and AlInP/GaInP superlattices; (b) enhancement of heterostructure device speed performance via strain layer superlattices and mushroom gates in modulation doped FET's (MODFET's), and inserted tunnel barriers heterojunction bipolar devices (HBT); (c) fabrication and characterization of MODFET devices with gate lengths to 50 nm; (d) self-consistent Monte Carlo transport formulation and its applicat... to small graded heterostructure devices; (e) optical modulation based on the quantum confined Stark effect; and (f) femtosecond spectroscopy of hot carrier processes using the visible Rh6G laser and a new UV BaB_2O_4 laser.

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A. DIRECTORS OVERVIEW

The report at hand is for the eleventh year of the Joint Services Electronics Program at Cornell University. During the three previous program periods of March 1977 - April 1981, May 1981 - April 1984, and May 1984 - April 1987 all research was in the area of microwave semiconductors, primarily in compound semiconductor materials, devices and circuits. A total of 288 publications and 49 MS or PhD degrees were supported fully, or in part, by JSEP during that period. During the eleventh year research still continued on compound semiconductors but simultaneously a new broader research proposal was compiled for the years twelve and thirteen. The newly organized research covers two themes, one on ultra high speed compound semiconductors, and the other on real time signal processing.

The highly successful traditions were continued in the eleventh year of the JSEP program at Cornell. 28 research papers have been published. Numerous conference and workshop presentation have been given. 16 graduate students have been supported in part, or fully, by JSEP funds during this year. 3 MS and 7 PhD degrees have been, or will be, awarded to graduate students associated with the Cornell JSEP program during the 1987/1988 academic year.

B. DESCRIPTION OF SPECIAL ACCOMPLISHMENTS AND TECHNOLOGY TRANSITION

A large number of significant research results for high speed electronics have been obtained during this one year reporting period.

Work on the new OMVPE laboratory in the research building at Langmuir, ultimately with several machines including multi-chamber OMVPE, has continued. However, all OMVPE materials growth this year has been performed at the old site in the Electrical Engineering building. GaInP/GaAs and AlInP/GaInP superlattices have been grown and extensively characterized. Selective disordering studies of the visible bandgap superlattices have shown that the AlGaInP system is more stable than the AlGaAs system.

In the high speed heterostructure device research maximization of the electron velocity has been the main goal. A world record for the cut-off frequency, f_T, of 122 GHz has been obtained for strain-layer modulation doped FET's with $In_yGa_{1-y}As$ active channels on GaAs substrates. A mushroom gate with a length of 0.18 μm was used. Thin tunnel barriers have been inserted into heterostructure bipolar devices in order to effect the ballistic injection of carriers into the base and allow for a base drift field to be built in. Photoluminescence studies of single quantum wells (QW) have been performed to study the time scale for tunneling under an applied electric field. Carrier escape times from QW's have been shown to be sensitive to layer thicknesses and materials compositions. Zero bias escape times, measure to be as large as 60 ps, are believed to be slow and be dominated by recombination rather than tunneling. Planar doped barriers for injecting ballistic electrons have been studied with specially designed heterostructure analyzers. In this work with Schottky gate vertical FET's the highest transconductance values, 150 mS/mm at 300 K, of any vertical FET device structure, including the permeable base transistor, have been obtained. From these results it is inferred that high gain and high frequency operation will not be possible for THETA type devices (tunneling hot electron transistor).

Significant progress in the ultra short gate FET research has been obtained despite of this being a new task. A multi-layer electron beam lithography has been developed for fabricating FET gates with a mushroom cross section and a minimum footprint of 50 nm. The achieved gate resistance, 220 Ω/mm, is the smallest reported value for 75 nm long gates to date. Accurate on-wafer microwave characterization techniques based on the HP8510 network analyzer, the Cascade Microtech Prober, and newly developed de-embedding procedures have been developed. World record f_T values of 113 to 122 GHz have been obtained for 100 nm gate length modulation doped FET's (MODFET's). Such f_T values seem to correspond to a transit time

less than 1 ps. Analysis of electron transport in these channels is in a preliminary stage because of the reduction of the program period from the proposed three years to one. Average electron velocities in the MODFET channels do not seem to contain any evidence of non-equilibrium transport at 300 K contrary to expectations. This is due to the fact that extrinsic source and drain resistances limit the frequency response due to source-to-drain separations larger than 1 μm.

The task on theoretical studies of non-equilibrium transport in high speed heterostructure devices has been in a highly fruitful phase. The self-consistent Monte Carlo transport formulation and its software implementation for the IBM 3090-600 supercomputer for graded heterostructures with imbedded heterojunctions has been completed. Limits for this transport formulation have been derived. Fully self-consistent simulations with open boundaries to thermal reservoirs for a number of graded heterostructure devices have been performed for the first time. Significant new insight into ballistic electron launching, space charge effects of electron transport across heterojunctions, and Gunn diode operation with a heterojunction launchers has been obtained. The two-dimensional version has been completed as well, and is ready to be applied to more complex heterostructure devices.

The quantum confined Stark effect was demonstrated for the first time in a waveguide structure. This effect is an ideal integrable modulator with a projected 0.2 V/GHz modulation power to bandwidth figure of merit. Intermixing of quantum wells in the GaAs/AlGaAs materials system allowed the shifting of the absorption edge up to 40 meV. This facilitates individual tunability of modulators fabricated on the same substrate.

Two pioneering results have been obtained in the optical femtosecond dynamics research. The first UV femtosecond laser based on BaB_2O_4 has shown characteristics comparable to those of the visible Rh6G laser. Materials growth and laser fabrication has been done at Cornell. 43 fs pulses at 315 nm with a repetition rate of 100 MHz have been demonstrated. This will greatly expand the spectral range of femtosecond lasers, and gives prospects to extend the same concept into the IR region as well. Another significant success has been achieved in the up-conversion of hot luminescence emitted by highly excited non-equilibrium carriers in compound semiconductors. An unprecedented time resolution of 40 fs for this type of technique has been gained and applied to study hot carrier phenomena in undoped GaAs and related compounds. Extensions to doped semiconductors are in progress.

Interactions on JSEP and related research with outside researchers, including DoD, have continued strongly via several media. JSEP principal investigators, primarily professor L. Eastman, were instrumental in organizing the IEEE/Cornell Conference on Advanced Concepts in High Speed Semiconductor Device and Circuits held on the Cornell Campus August 10-12, 1987.

Professor J.R. Shealy, one of the Cornell principal investigators, organized the Third Biannual OMVPE Workshop in Cape Cod September 23-25, 1988. Technical interactions with more than 30 industrial and government organizations have been continued in the compound semiconductor area. DoD organizations included in this list are ERADCOM/Ft. Monmouth, NRL, and MIT/Lincoln Laboratories Interactions with these outside organizations take various forms such as additional research support, specific joint research, technology exchange, employment of former graduate students or post doctoral associates, or cooperative arrangements for graduate students studying toward their PhD degrees.

TASK 1 ***ADVANCED TECHNIQUES FOR THE GROWTH OF III-V SEMICONDUCTOR STRUCTURES***

Assistant Professor J.R. Shealy and Professor L.F. Eastman

OBJECTIVE

The objective of the materials task in the new JSEP program is to extend the capabilities of the OMVPE process for materials and structures used in high speed devices and support related tasks in femtosecond electron dynamic studies in III-V compounds. These structures are used for electron confinement to 1 or 2 dimensions and to inject electrons into a drift space at an elevated energy to achieve ballistic motion. In this materials task, the work breaks down into 3 areas:

i) the growth of AlGaAs/GaAs and related structures of known quality to supply samples for optical studies of electron dynamics,

ii) the realization of quantum wires in the AlGaAs/GaAs system by carefully controlling the surface migration of the reactants to result in the formation of lateral heterostructures, and

iii) the growth of device quality structures with the materials system AlInAs/GaInAs lattice matched to InP.

DISCUSSION OF STATE-OF-THE-ART

The OMVPE technique has recently addressed an increasingly number of technological problems which has limited its application to electron devices. The influence of growth conditions on residual carbon incorporation was established for GaAs films in the early 1980's. However, for Al containing alloys, the growth with the ethyl compounds has recently been established as a method for reducing the residual carbon contamination. The strength of the aluminum carbon bonds require growth at very high V-III ratios to reject carbon incorporation into the solid, especially when using methyl sources. The reduced carbon concentrations with this method is achieved at the expense of higher residual Si incorporation. However, for example, modulation doped AlGaAs/GaAs heterostructures perform better with Si in the electron confining layer as opposed to carbon.

High purity bulk alloys ($N_d + N_a < 5(10^{14}\ cm^{-3})$) of GaAs, GaInAs, GaInP and InP are readily prepared by OMVPE. However, aluminum containing compounds typically have $5(10^{16})cm^{-3}$ or greater levels of carbon contamination. In spite of this, atomically abrupt lattice matched heterostructures are achieved with negligible impurity induced interface

broadening. Two dimension electron gases are realized at these interfaces in GaInP/GaAs/GaInAs/InP, and AlGaAs/GaAs materials. For example, the present state of the art in these two dimensional electron gases as determined by LN_2 Hall mobility data is 60,000, 80,000 and 150,000 $cm^2/(v\text{-}s)$ in GaInP/GaAs [1], GaInAs/InP [2] and AlGaAs/GaAs [3] OMVPE grown heterostructures, respectively. For the Al containing HEMT structures, the carbon acceptors near the interface limit the performance, while the GaInP/GaAs system suffers with hetero-interface problems which adversely affects the 2D gas at this interface. Narrow quantum well heterostructures with individual layer thickness approaching two or three monolayers are achieved in each of these systems. In fact, the multichamber OMVPE reactor technology under development at Cornell has demonstrated smoother, more abrupt GaAs/AlGaAs interfaces than is achieved by MBE under comparable growth conditions. This conclusion is based on Raman spectroscopic examination of the confined phonon vibrations in ultra thin quantum wells. This technique is primarily sensitive to the structural properties of the interfaces and not impurities or defects. This is in sharp contrast to the attempts to analyze interface structures with the PL method. Quantum confinement in two directions (quantum wires) have been predicted to possess such characteristics as extremely high electron mobilities [4] and increased energy quantization. Efforts on quantum confinement in two directions on the order of 100 A dimensions have been few in number [5,6] and limited mostly to discussions rather than attempts.

One novel approach originally proposed by Petroff and Gossard at ATT (now at the UC-Santa Barbara) was to grow at partial monolayer of GaAs by MBE on a stepped AlAs surface, then grow thick AlAs on top [6]. For this technique to be successful, the group III atoms must have sufficient surface mobility to move to steps to incorporate and surface roughness must not exceed one monolayer. Recent results obtained at UC-Santa Barbara (presently unpublished) have shown that sub atomic layer growth in MBE will produce quantum wires. However, the controllability was lacking as the wire dimensions varied over small substrate areas. The confirming evidence of the presence of the 1D confinement was both structural properties (TEM lattice images) and optical properties (PLE polarization studies of the light and heavy hole transitions). However, this same approach by OMVPE was recently demonstrated [7] where an AlAs/GaAs superlattice oriented vertically (the superlattice interfaces normal to the substrate surface) resulted. The OMVPE approach seems to have produced a more homogeneous array of the laterally confined heterostructures. This suggests that the growth requirements for such structures are better met with the higher surface mobility growth species which are characteristic of the OMVPE process.

PROGRESS

In the last JSEP report, we detailed the structure and orientation of this ordered state and determined it crystalline orientation with TEM. The OMVPE growth parameters may be altered to yield lattice matching films with or without the existence of the order state, however the optical properties are generally better in the "ordered" films as demonstrated by low temperature photoluminescence intensity, and linewidths (12 meV @ 4 K). AlInP was grown over a range of compositions to determine its optical properties via Raman spectroscopy (phonon energies) and electro-reflectance (direct bandgap).

In the last year of this program, superlattice heterostructures have been grown with GaInP/GaAs and AlInP/GaInP which have been analyzed with photoluminescence, TEM, and Raman spectroscopy. The arsenide to phosphide interface formation has been investigated because of the difficulty encountered with switching the group V sources under group V rich conditions. The interface abruptness in this case is approximately 15 A, while the GaInP/AlInP interfaces are as abrupt as one monolayer.

The work was extended by examining a selective disordering process for visible bandgap superlattice. The disordering of an ordered state of $Ga_{.5}In_{.5}P$ and the partial intermixing of GaInP/AlInP superlattices has been demonstrated at temperatures between 650°C to 975°C. The localized disordering or intermixing was accomplished by the deposition of SiO_2 followed by rapid thermal annealing. Regions with no SiO_2 showed minimal intermixing over this temperature range while the capped areas exhibited superlattice energy shifts up to 34 meV at room temperature. Bulk $Ga_{.5}In_{.5}P$ disordered at 900-925°C for these samples with SiO_2 while remaining ordered for samples with no SiO_2. The degree of disordering or intermixing was measured using room temperature and low temperature photoluminescence, and Raman spectroscopy. The interdiffusion coefficient as a function of temperature was also estimated by assuming a simple model and performing numerical calculations. These results indicated that the phosphide system, AlGaInP is thermal more stable and AlGaAs structures.

SCIENTIFIC IMPACT OF RESEARCH

The potential impact of the proposed research in this task is the realization of ultra high speed semiconductor devices (subpicosecond switching times) based on ballistic electron transport in compound semiconductor materials. The investigations carried out with the OMVPE materials will examine hot electron relaxation in two and one dimensional systems. The one dimensional systems of electrons (or holes) will allow a new generation of high speed electrical and optical devices to follow.

DEGREES

D.P. Bour, January 1988, Ph.D. Thesis
"Organometallic Vapor Phase Epitaxial Growth and Characterization of AlGaInP for Visible Emitters"

M. Lestina, May 1988, M.S. Thesis
"A Low Thermally Resistive Process for the CW Operation of Laser Diodes"

REFERENCES

1. M. Razeghi, Thomson CSF, private communication.

2. "Epitaxial Growth and Characterization of Indium Phosphide and Gallium Indium Arsenide by Metalorganic Chemical Vapor Deposition", D.T. Chan, Cornell University, Ph.D. Thesis (Aug. 1986).

3. N. Kobayashi and T. Fukui, Elec. Lett., 20, 887 (1984).

4. "Mobility in a Quasi-One-Dimensional Semiconductor: An Analytical Approach", G. Fishman, Phys. Rev., B34, 2394 (1986).

5. P.M. Petroff, A.C. Gossard, R.A. Logan and W. Wiegmann, Appl. Phys. Lett., 41 (7) 635 (1982).

6. "Structure of AlAs-GaAs Interfaces Grown on (100) Vicinal Surfaces by Molecular Beam Epitaxy", P.M. Petroff, A.C. Gossard and W. Wiegmann, Appl. Phys. Lett., 45 (6) 620 (1984).

7. "$(AlAs)_{0.5}(GaAs)_{0.5}$ Fractional-Layer Superlattices Grown on (001) Vicinal Surfaces by Metalorganic Chemical Vapor Deposition", T. Fukui and H. Saito, Appl. Phys. Lett., 50 (13) 824-826 (March 1987).

JSEP PUBLICATIONS AND PRESENTATIONS

1. "Investigation by Raman Scattering of the Properties of III-V Compound Semiconductors at High Temperature", J.R. Shealy and G.W. Wicks, Appl. Phys. Lett., 50 (17) 1173-1175 (April 1987).

2. "$Ga_{0.5}In_{0.5}P$/GaAs Interfaces by Organometallic Vapor Phase Epitaxy", D.P. Bour, J.R. Shealy and S. McKernan, J. Appl. Phys., 63 (4) 1241-1243 (Feb. 1988).

3. "TEM Studies of Ordering in MOCVD Grown GaInP on GaAs", S. McKernan, B.C. DeCooman, C.B. Carter, D.P. Bour and J.R. Shealy, Proc. Materials Res. Symp., 104, 637-640 (1988).

4. "Disordering, Intermixing, and Thermal Stability of GaInP/AlInP Superlattices and Alloys", S. O'Brien, D.P. Bour and J.R. Shealy, submitted to Appl. Phys. Lett. (1988).

TASK 2 ***PHYSICAL ELECTRONICS OF III-V HETEROJUNCTION DEVICE STRUCTURES***

Professor L.F. Eastman

OBJECTIVE

The objective of this task is to determine the limits of electron velocity in special small structures that can be used in very high frequency transistors and related devices.

DISCUSSION OF STATE-OF-THE-ART

Electrons traveling in pure GaAs at .25 eV will have ~ .18 μm mean free path at room temperature, and ~ .22 μm mean free path temperatures at or below 77 K. For energy values above .31 V, electrons can transfer to a low mass upper valley in ≤ 100 fs. When such ballistic electrons travel through a thin sheet of thermalized electrons, they interact with the coupled plasmon-phonon quanta in such a sheet. On the average, a ballistic electron at .25 V will lose half of its forward momentum when passing through an electron sheet density of $1 \times 10^{13}/cm^2$. For only $2.5 \times 10^{12}/cm^2$ electrons in the path of ballistic electrons ~30% remain ballistic in character, but this sheet density is low for obtaining low transistor base resistance.

When electrons travel along pure GaAs quantum wells, they have substantial mean free paths unless they have enough momentum to surmount the finite potential wall on the side of the quantum well. To date no definitive data has been obtained to show enhanced velocity for shorter (.2 μm gate) field effect transistors, compared to longer (1 μm gate) ones. Higher velocity has been achieved at any such gate lengths for quantum wells with higher barriers; e.g. 1.8×10^7cm/s for the best $In_{.25}Ga_{.75}As$ quantum wells with $Al_{.3}Ga_{.7}As$ potential walls of .44 V magnitude. This compares with 1.2×10^7cm/s for GaAs wells with $Al_{.3}Ga_{.7}As$ potential walls of .24 V in the usual MODFET. There is not yet an understanding of this lack of velocity overshoot or ballistic electron acceleration along quantum well field effect transistors.

PROGRESS

Electron motion parallel to, and perpendicular to, heterojunctions have been studied in this task.

In the area of electron motion parallel to the heterojunctions, strained-layer modulation-doped field effect transistors (SMODFET's), with $In_yGa_{1-y}As$ active channels, on GaAs substrates were studied. With y = 0, AlGaAs/GaAs/AlGaAs quantum wells were found [1] to have the best performance when the substrates were misoriented above 4^o from the (001)

planes toward the (111)A plane. Improved mobility and good average electron transist velocity in FET's resulted. The same was true for $0 < y < .25$ structures. With $y = .25$ the electron sheet density was raised to $2.4 \times 10^{12}/cm^2$ when the doping was on one side (the last grown) only. Average electron transit velocity of 1.8×10^7cm/s was determined in these channels with $y = .25$, for $y = .15$ this velocity was 1.5×10^7cm/s, and for $y = 0$ it was 1.2×10^7cm/s. Ph.D. theses were completed on the MBE growth and characterization of these wafers [2] as well as on transistors made from them [3,4]. Efforts at General Electric in the summer of 1987, and at Hughes in the summer of 1988 have allowed the transfer of optimized design and MBE growth technology, of such SMODFET wafers, to those locations. At Cornell, a world record value of $f_T = 122$ GHz was obtained for such SMODFET's with .18 μm mushroom shaped gates, and with $y = .25$ in the active channel.

In order to confine electrons to the active channel when short gates are used, acceptor planar doping in the MODFET buffer layer was studied, and an M.S. thesis completed [5]. With this buried player, the MODFET's had a lower knee (drain-source) voltage (~.3 V) than usual (~.5 V), and had improved performance up to ~2.5 V. This performance improvement included significantly higher f_T, and output resistance, and significantly lower noise figure. The superior noise figure at lower voltage and current would allow very low power dissipation in state-of-the-art low-noise amplifiers at high microwave frequencies, for future space applications.

In the area of transport perpendicular to the heterojunctions there were a number of projects undertaken.

One project involved heterojunction bipolar transistors. In these devices abrupt emitter-base heterojunctions have been used to inject electrons ballistically into the base. Earlier work on this at Cornell has led to a patent [6]. As long as the acceptor sheet doping in the base is moderate, such as $< 2 \times 10^{13}/cm^2$, the electron momentum from the ballistic injection did not entirely die out, and fast transit was possible. In order to reduce the base resistance, the base thickness of 1000 A and the doping at $5 \times 10^{19}/cm^3$ needed yield $5 \times 10^{14}/cm^2$ holes in the path of the ballistic electrons. In order to increase the velocity of these electrons losing momentum during their transit through the base, a built-in electric field is required. We initiated the use of $In_yGa_{1-y}As$ strained-layer base regions, with y rising from 0-5% across the side of the base nearest the collector, to cause 5-10,000 V/cm electric field. This raised the current gain, as well as the electron velocity, since electrons had less time to recombine radiatively in the base. Since hot electrons are less likely to recombine with cold holes, the recombination rate for the electron minority carriers is reduced, if the electrons are kept hot by the built-in fields. In order to diagnose the electron radiative recombination

location, the spectrum of the device radiation was analysed. The longer wave length recombination showed that the recombination occurred near the collector, in good designs, for example.

In order to have a potential step to inject ballistic electrons, an abrupt emitter-base heterojunction is desired, as explained above. The amount of aluminum in $Al_xGa_{1-x}As$ is limited to x = .20-.25 in order to prevent unwanted electron trapping in the emitter due to the deep donor/DX levels. If x = .20, the conduction band discontinuity is only .16 V, and the valance band discontinuity is only ~.093 eV. This valance band step is not high enough to lower hole emission much more than a ratio of ~35:1. Since the base doping could be as much as 200:1 more than the emitter, this causes relatively low gain in such abrupt heterostructure bipolar transistors. In order to recover this gain, a thin tunnel barrier at the abrupt emitter-base heterojunction has been studied [7], and a Ph.D. thesis is presently being written up. The thin tunnel barrier allows fast, easy low-mass electron tunneling, while heavier hole tunneling is much less. An optimized device would have $Al_{.20}Ga_{.80}As$ emitter, and either 11.3 A AlAs or 17 A $Al_{.5}Ga_{.5}As$ barrier, then the graded $In_yGa_{1-y}As$ base and GaAs collector. In such a device there would be high injection efficiency, due to the tunnel barrier, high base transport factor, due to ballistic injection and base drift field, as well as high frequency response.

In order to study the tunneling rate through single tunneling barriers, structures were grown by MBE with different composition and thickness. These were tested for photoluminescence decay rate, at the University of Rochester, as part of the URI program there monitored by AFOSR.

The time for electrons to build-up inside a quantum well (QW) and the time for electrons to escape from the QW by tunneling through a thin barrier are the two key processes to govern the ultimate speed of resonant tunneling devices. These two times are roughly the same when resonant tunneling devices operate within the complete coherence of electron waves [8]. In a semiclassical model, the time t_T can be expressed as $1/\nu T$ of the frequency ν of electron collision with the barrier and the tunneling probability T of electrons through a single barrier. Since the resonant tunneling device is operated under the electrical bias, which can significantly influence the tunneling probability T and consequently escape time t_T, the escape time under the bias needs to be investigated. We have done time resolved PL on a single QW subject to an electric field recently. The results show a strong influence of the field on the escape time as theoretically expected.

Experimentally, a single QW sample held at 6 K was excited by a 10 picosecond dye laser at a 100 mHz repetition rate. The pump energy was tuned so that only the electron-heavy hole

transition in QW was allowed. The PL from QW was collected by a 3D streak camera with temporal resolution limit of 20 psec. The measured PL decay rate can be expressed as:

$$1/(t_{Dec}) = 1/(t_T) + 1/(t_{Rec}),$$

where t_{Rec} is electron-hole recombination (radiative and nonradiative) time which is on the order of nanosecond or subnanosecond [9,10]. The escape time t_T is equivalent to the measured PL decay time, when it is much faster than t_{Rec}. In order to have the time t_T be success finally determined, the QW structure should be designed to have the value of t_T between the streak camera limit (~20 psec) and the electron hole recombination time (<1 ns).

The samples under study were composed of 34 A-thick QW, a thick barrier on the right and a thin barrier on the left. Five samples have been prepared for comparison. Three of them, with 30% Al composition, have different thickness of 96 A, 124 A and 135 A of the thin barrier (see Figure 1b). The other two have the same thickness of 96 A, but different Al composition of 30% and 40% (see Figure 1a). This undoped single QW structure was clad between an n^+ buffer layer and p^+ cap layer. A 600 μm diameter mesa was etched down to the n^+ buffer and ohmic contacts were made on both n^+ buffer and p^+ cap, except that a 200 μm diameter hole was left on cap was left for optical access.

Our results show the time t_T, at zero bias, was very sensitive to the barrier thickness as reported in [8] and barrier Al composition as well. As an example, t_T from a 34 A thick GaAs QW through a 96 A thick barrier of $Al_{.3}Ga_{.7}As$ was measured as 60 picosec. With reverse bias t_T was found exponentially decreased with the field. The escape time from the one with a thicker barrier decreased much quicker than the one with a thinner barrier. This can be explained that, as the field increased to tilt the barrier, the effective barrier thickness to the tunneling electron from these two samples would get closer and finally be the same. An analytic approximation derived from the semiclassical model is given as

$$t_T(F) = t_T(O) \exp\{-b^2/2h\sqrt{2m/v\text{-}E}F\}$$

where $t_T(O)$ is the escape time at zero bias, b the barrier thickness, and F the field which is evaluated by C-V measurement. This analytic expression can fit our experimental results in a very good agreement. The data from the samples with 124 A, 135 A thick barrier and 40% Al composition deviate from the theoretical expression near zero bias. This is believed to be due to the fact that the escape time $t_T(F)$ from these samples near zero bias is slow and the measured decay time is dominated by recombination time.

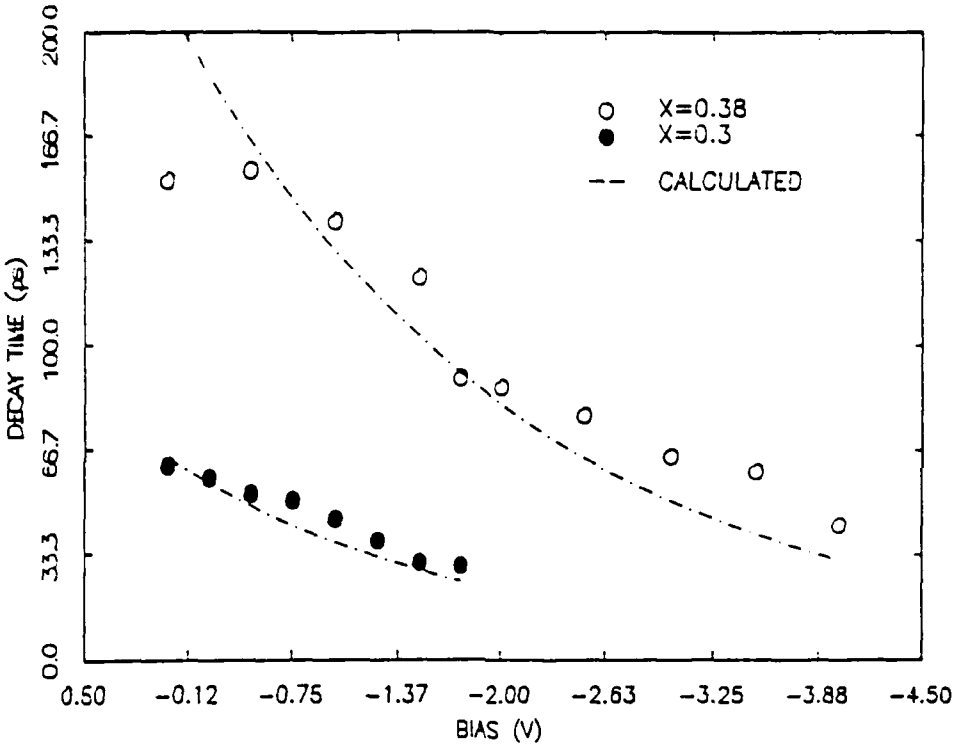


Figure 1a Photoluminescence decay time vs bias in P-N junction - for different Al composition in 96 Å barrier.

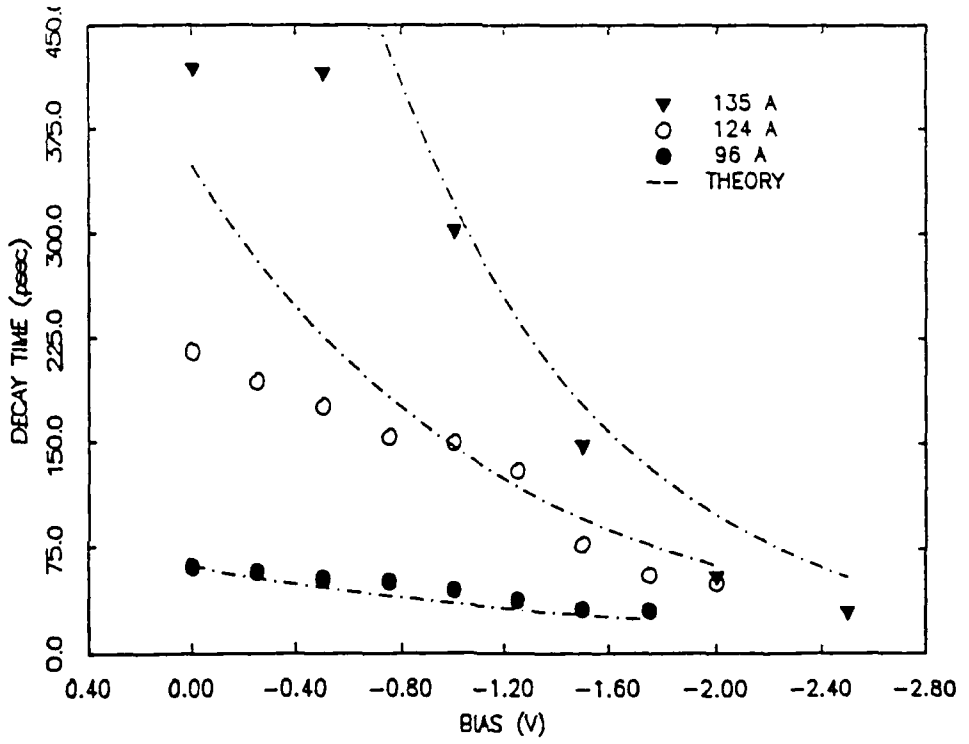


Figure 1b Photoluminescence decay times vs bias in P-N junction - for 30% Al and different barrier thickness.

The use of planar doped barriers for injecting ballistic electrons has the benefit of designing any barrier height, and thus any injection energy, without the electron traps in heterojunctions involving $Al_xGa_{1-x}As/GaAs$. One potential problem is the possibility that the acceptor ions causing the potential barrier are separated in their plane by over 100 A. This could cause little potential dips along the plane of the potential barrier, and might cause a spread in kinetic energy of injected electrons. Tests were undertaken using an undoped $Al_xGa_{1-x}As$ barrier for electron energy spectroscopy, as Heiblum of IBM has done. With an electron sheet density of $\sim 1 \times 10^{13}/cm^2$ in the path of the injected electrons, virtually all of the injected electrons had momentum changes, yielding a negligible density of ballistic electrons. The electrons' directed energy distribution had a broad peak at about .1 V after being injected at .3 V and traveling through 1400 A of GaAs drift region, with $\sim 1 \times 10^{13}/cm^2$ electrons and 1000 of undoped $Al_{.3}Ga_{.7}As$ in the energy analyser. An M.S. thesis [11] has been completed on this analyser project. At .1 V the electrons were moving at 5-6 x 10^7cm/s, compared with 1 x 10^8cm/s when they were launched at .3 V. These three-terminal spectroscopy devices had only unity current gain in their DC common emitter transistor characteristics, measured at 77 K. Other spectroscopy devices with a thinner GaAs drift region with only $2.5 \times 10^{12}/cm^2$ electrons showed a sharp ballistic peak in the spectrum. This peak was at a higher energy, equivalent to the launch energy.

Using a planar doped barrier launcher ballistic electrons up into a .6 μm wide channel, only .10 μm long in the electron drift direction, improved results have been achieved with Schottky-gated vertical FET's. G_m values of over 150 mS/mm at 300 K and over 230 mS/mm at 77 K were obtained with ballistic injection, and these are by far the highest values ever, with or without the ballistic injection, gotten on PBT or other vertical field effect transistors, and clearly show the optimum direction for future research. The conclusion is that no device of the type of Heiblum will succeed in obtaining high gain and high frequency performance. This is due to the sharp drop in ballistic electron momentum when these electrons pass through a sheet of electrons > $1 \times 10^{13}/cm^2$ in the base of the transistor with no drift field. For low base resistance, $10^{14}/cm^2$ electrons, and $10^{15}/cm^2$ holes in the bipolar case, are required. On the other hand, if Schottky gates are used to modulate the current flow, only fast electrons are flowing and an electric drift field is able to be applied, yielding fast transit through .1-.5 μm of drift region.

SCIENTIFIC IMPACT OF RESEARCH

The unity current gain of a transistor depends on the reciprocal of 2π times the carrier

transit time through the transistor. With these 50-100% rises in electron velocity, f_T is 50-100% higher, having a direct impact on higher frequency performance in transistors. The maximum velocity for 300 K operations heterojunction field effect transistors is still less than a quarter of that possible for ballistic electrons. Near term good high frequency performance is best obtained from heterojunction FET's, but effort on obtaining near ballistic electron velocity should be redoubled for ultimate performance in the longer term.

DEGREES

D.C. Radulescu, May 1988, Ph.D. Thesis
"Molecular Beam Epitaxial Growth and Characterization of Aluminum Gallium Arsenide/Indium Gallium Arsenide Single Quantum Well Modulation Doped Field Effect Transistor Structures"

S.S. Lu, August 1988, M.S. Thesis
"Fabrication and Characterization of the Planar Doped Barrier Spectrometer"

REFERENCES

1. "Effects of Substrate Misorientation and Background Impurities on Electron Transport in Molecular-Beam-Epitaxial Grown GaAs/AlGaAs Modulation-Doped Quantum-Well Structures", D.C. Radulescu, G.W. Wicks, W.J. Schaff, A.R. Calawa and L.F. Eastman, J. Appl. Phys., 62 (3) 954-960 (Aug. 1987).

2. "Molecular Beam Epitaxial Growth and Characterization of Aluminum Gallium Arsenide/Indium Gallium Arsenide Single Quantum Well Modulation Doped Field Effect Transistor Structures", Ph.D. Thesis, Cornell University (May 1988).

3. "Ultra Short Gate Lattice Mismatched Modulation Doped Field Effect Transistors", Ph.D. Thesis, Cornell University (May 1988).

4. "Submicrometer Gate Planar-Doped Pseudomorphic Multiple-Heterojunction MODFETs for Millimeter-Wave and Optical Communication", Ph.D. Thesis, Cornell University (May 1988).

5. "The Use of Buried Beryllium-Doped Layers to Reduce Buffer Current in Low Noise Pseudomorphic Modulation-Doped Field-Effect Transistors", M.S. Thesis, Cornell University (Aug.1988).

6. "Ballistic Heterojunction Bipolar Transistor", D.G. Ankri, L.F. Eastman and W.H. Ku, Patent (June 1987).

7. "DC Characterization of the AlGaAs/GaAs Tunneling Emitter Bipolar Transistor", F.E. Najjar, D.C. Radulescu, Y.K. Chen, G.W. Wicks, P.J. Tasker and L.F. Eastman, Appl. Phys. Lett., 50 (26) 1915-1917 (June 1987).

8. M. Tsuchiya, T. Matsusue and H. Sakaki, Phys. Rev. Lett., 59, 2356 (1987).

9. J.E. Fouquet, A.E. Siegman, R.D. Burnham and T.L. Paoli, Appl. Phys. Lett., 46, 374

(1985).

10. T. Matsusue and H. Sakaki, Appl. Phys. Lett., 50, 1429 (1987).

11. "Fabrication and Characterization of the Planar Doped Barrier Spectrometer", S.S. Lu, M.S. Thesis, Cornell University (Aug. 1988).

JSEP PUBLICATIONS AND PRESENTATIONS

1. "DC Characterization of the AlGaAs/GaAs Tunneling Emitter Bipolar Transistor", F.E. Najjar, D.C. Radulescu, Y.K. Chen, G.W. Wicks, P.J. Tasker and L.F. Eastman, Appl. Phys. Lett., 50 (26) 1915-1917 (June 1987).

2. "MBE Growth and Materials and Device Characterization of Strained Layer GaInAs/GaAs for Application to MODFETs", W.J. Schaff and L.F. Eastman, Proc. E-MRS, Vol. XVI, 295-301, Strasbourg, France (June 2-5, 1987).

3. "Heterojunctions for Improved Electron Confinement in Modulation Doped FET's", L.F. Eastman, Invited, E-MRS, Strasbourg, France (June 2-5, 1987).

4. "Bias-Dependent Microwave Characteristics of an Atomic Planar-Doped AlGaAs/InGaAs/GaAs Double Heterojunction MODFET", Y.K. Chen, D.C. Radulescu, G.W. Wang, A.N. Lepore, P.J. Tasker, L.F. Eastman and E. Strid, IEEE MTT-S Int. Microwave Symp., Las Vegas, NV (June 9-11, 1987).

5. "Tunneling, Ballistic, and Hot Electron Devices", L.F. Eastman, DRC, Santa Barbara, CA (June 22-24, 1987).

6. "MBE Growth and Material and Device Characterization of AlInAs/GaInAs MODFETs on a GaAs Substrate", W.J. Schaff, Y.K. Chen, L.F. Eastman and K.L. Kavanaugh, EMC, Santa Barbara, CA (June 24-26, 1987).

7. "Effects of Substrate Misorientation and Background Impurities on Electron Transport in Molecular-Beam-Epitaxial Grown GaAs/AlGaAs Modulation-Doped Quantum-Well Structures", D.C. Radulescu, G.W. Wicks, W.J. Schaff, A.R. Calawa and L.F. Eastman, J. Appl. Phys., 62 (3) 954-960 (Aug. 1987).

8. "Characterization of the AlGaAs/GaAs Tunneling Emitter Bipolar Transistor", F.E. Najjar, D.C. Radulescu, Y.K. Chen, G.W. Wicks, P.J. Tasker and L.F. Eastman, Proc. 11th Biennial Conf. on Advanced Concepts in High Speed Semiconductor Devices and Circuits, Cornell University, Ithaca, NY, 284-292 (Aug. 10-12, 1987).

9. "A Study by Raman Spectroscopy of the Effects of Growth Stops on the Interfaces of AlAs/GaAs Superlattices Grown by MBE", G.W. Wicks, J.T. Bradshaw and D.C. Radulescu, 8th MBE Workshop, University of California, Los Angeles, CA (Sept. 9-11, 1987); J. Vac. Sci. Tech. (March/April 1987).

10. "Influence of Substrate Misorientation on Defect and Impurity Incorporation in AlGaAs/GaAs Heterostructures Grown by Molecular Beam Epitaxy", D.C. Radulescu, G.W. Wicks, W.J. Schaff, A.R. Calawa and L.F. Eastman, 8th MBE Workshop, University of

California, Los Angeles, CA (Sept. 9-11, 1987).

11. "The Effect of Substrate Orientation on Deep Levels in N-AlGaAs Grown by Molecular Beam Epitaxy", D.C. Radulescu, W.J. Schaff, G.W. Wicks, A.R. Calawa and L.F. Eastman, 14th Int. Symp. on GaAs and Related Cpds., Crete, Greece (Sept. 28-Oct. 1, 1987); Inst. Phys. Conf. Ser. 91, 299-302 (1988).

12. "Carrier Injection and Base Transport in Heterojunction Bipolar Transistors with InGaAs Base", Y. Ashizawa, S. Akbar, G.W. Wicks and L.F. Eastman, 14th Int. Symp. on GaAs and Related Cpds., Crete, Greece (Sept. 28-Oct. 1, 1987); Inst. Phys. Conf. Ser. 91, 705-708 (1988).

13. "Low Temperature Operation of Heterojunction Bipolar Transistors", L.F. Eastman, P.J. Tasker, Y. Ashizawa and G.W. Wicks, Invited, 172nd Meet. Electrochemical Society, Honolulu, Hawaii (Oct. 18-23, 1987).

14. "Compound Semiconductor Heterostructures for 21st Century Transistors", L.F. Eastman, W. Schaff, R. Shealy and G. Wicks, Invited, 172nd Meet. Electrochemical Society, Honolulu, Hawaii (Oct. 18-23, 1987).

15. "Influence of an Intentional Substrate Misorientation on Deep Electron Traps in AlGaAs Grown by Molecular Beam Epitaxy", D.C. Radulescu, W.J. Schaff, G.W. Wicks, A.R. Calawa and L.F. Eastman, Appl. Phys. Lett., 51 (26) 2248-2250 (Dec. 1987).

TASK 3 ***FUNDAMENTAL PHENOMENON IN ULTRASHORT DEVICES***

Professor E.D. Wolf, Professor L.F. Eastman and Research Associate P.J. Tasker

OBJECTIVE

The ultimate objective of this project in the initial three year proposal was to investigate the electron transport properties in FET structures where the dimensions of the transistor are comparable to the mean free path for electrons. The best approach to studying the electron transport properties of short gate length transistors using electrical measurements is via the investigation of the variation of the intrinsic current gain cut-off frequency $(f_T)_i$ with gate length. Alternative approaches, such as investigating the variation of the DC transconductance $(g_m)_i$ with gate length are prone to errors and misinterpretation. The $(g_m)_i$ of transistors is a strong function of gate-to-channel separation. Control of this parameter during transistor fabrication, particularly when the gate length is a variable, is very difficult due to recess etching nonuniformity. The $(f_T)_i$ is, however, only a very weak function of gate-to-channel separation and so is an ideal parameter for studying variations with gate length.

The accurate determination of $(f_T)_i$ from measured microwave data is not simple, particularly when the gate length is reduced to nanometer dimensions (50-250 nm). First the measured current gain is modified by various effects:

i) microwave test fixture,
ii) parasitic capacitances, and
iii) parasitic resistances.

Secondly, the measured data must be extrapolated since the value of $(f_T)_i$ is much larger than the measurement bandwidth. This extrapolation must be performed correctly if meaningful data is to be obtained [1,2].

As a consequence of these considerations, the main research effort in this one year program has been focused towards three important objectives;

A) Development of the fabrication technology for realizing small footprint "T" cross-section FET gates,
B) Development of a low parasitic FET layout, along with a test cell structure that includes:
   i) variable gate length (50-250 nm)
   ii) variable gate width (25-150 μm), and
   iii) parasitic calibration standards (DC and RF),

C) Development of accurate on-wafer microwave characterization capability and the necessary analysis techniques to determine physical parameters from the measured microwave data unambiguously.

At present there has only been a very preliminary analysis, in terms of electron transport implications, of the measured data. More effort is needed to further develop the analysis techniques.

DISCUSSION OF STATE-OF-THE-ART

In recent years, with the development of high spatial resolution (submicron electron beam lithography) fabrication techniques, the performance of compound semiconductor field effect transistors has improved significantly as the gate length (L_g) has been reduced down to 250 nm [3,4]. GaAs MESFET's with values of current gain cut-off frequencies as high as 37 GHz and ring oscillator propagation delay/gate as small as 10 pS at room temperature have been achieved for L_g = 250 nm. As the gate length is reduced further, in order to avoid short channel effects, other transistor parameters must also be scaled. This involves the need for high channel doping to reduce channel thickness. The increased scattering of electrons by these donor atoms will reduce their average velocity. This effect is expected to limit the performance improvements as the gate dimensions are reduced in the MESFET and may explain the disappointing experimental results obtained [5].

In order, therefore, to achieve short transit times over short distances, it is very important that the donor atoms are removed from the path of the electrons. This can be achieved using a modulation doped heterojunction. The donor ions are placed in the larger bandgap material, e.g. $Al_xGa_{1-x}As$, while the electrons transfer to the narrow bandgap material, e.g. GaAs or $Ga_{1-y}In_yAs$, and accumulate in a thin (≤ 160 A) two-dimensional electron gas (2DEG) near the heterojunction. Since the electrons are in pure material, spatially removed from their donor atoms, they exhibit high electron mobilities and are predicted to exhibit higher electron velocities. $Al_xGa_{1-x}As$/GaAs MODFET's with values of current-gain cut-off frequencies greater than 50 GHz (at room temperature) have been achieved at both Cornell University and General Electric (Syracuse), when the gate length is scaled down to 250 nm [6,7]. Recently further improvements in MODFET performance have been achieved through the use of the $Al_xGa_{1-x}As/Ga_{1-y}In_yAs$ pseudomorphic system [8,9]. Figure 1 summarizes the state-of-the-art results, as of May 1987. Analysis of the variation of f_T versus L_g indicates electron velocities of 1.2 x 10^7cm/s and 1.5 x 10^7cm/s for the $Al_{.3}Ga_{.7}As$/GaAs and the $Al_{.2}Ga_{.8}As/Ga_{.85}In_{.15}As$ MODFETs, respectively [10]. The results indicated the following effects

i) improved electron velocities over the GaAs MESFET,

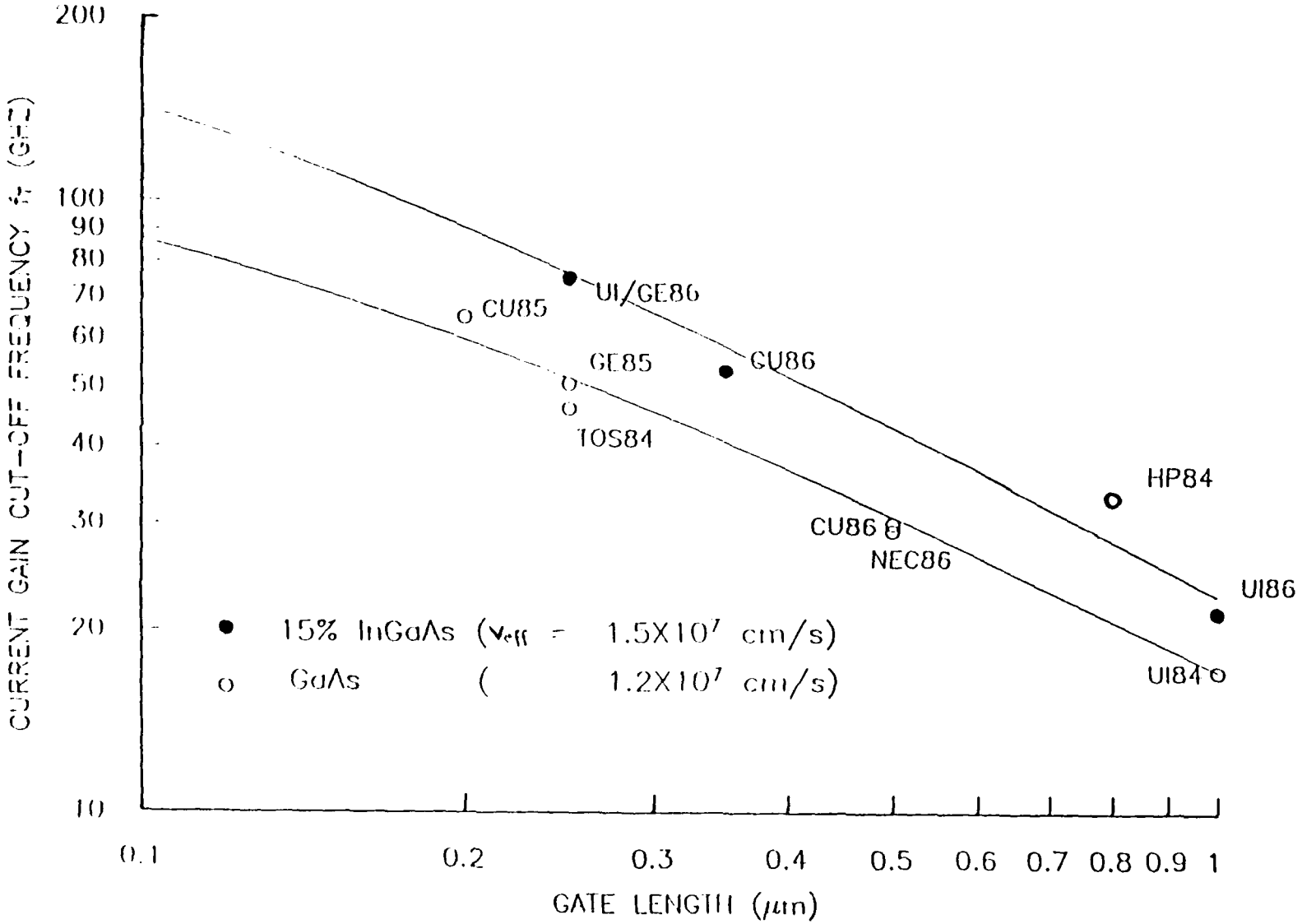


Figure 1 State-of-the-art GaAs and GaInAs channel MODFET results as of May 1987.

ii) electron velocities less than the theorically predicted value ~ 2.0 x 10^7cm/s,

iii) electron velocities obtained are sensitive to material composition, and

iv) no apparent increase in the average velocity as the gate dimension was reduced to 250 nm.

It had been theoretically predicted that the transistor performance would improve as the gate length is reduced because of various non-equilibrium transport effects, e.g. velocity overshoot. However, the experimental results indicated no evidence of non-equilibrium transport effects. A further reduction of the gate dimension was thus postulated so that the dimensions of the active region would become smaller than the mean free path of electrons (180 nm for 0.25 eV energy electrons in GaAs at room temperature). At these dimensions it is expected that non-equilibrium transport effects would become dominant. The research effort in this project was therefore directed towards the investigation of electron transport in MODFET structures with gate lengths less than 200 nm.

PROGRESS

In all objectives pursued during the report year, considerable progress has been made. As a consequence, short gate length MODFETs (L_g = 100 nm) have been fabricated which demonstrated world record measured f_T values of 113 to 122 GHz [10,11] which correspond to electron transit times of less than 1 ps.

A. Fabrication Technology

Electron beam lithography was used extensively for the fabrication of these ultra-short gate length transistors. The process steps are as follows. The transistors are mesa isolated, defined by photolithography and wet etch. Polymethylmethacrylate (PMMA) resist with a 1 μm thickness was used to define the ohmic source and drain contacts. AuGeNiAg/Au was lifted off and then alloyed using a rapid thermal process. The wafer was then coated with either a single or multilayer of PMMA. The gate level lithography level was performed in two steps by the JEOL 5DIIU electron-beam system. The first exposure conditions were 1 nA specimen current, 50 kV acceleration potential, and the 11 mm shrt working distance mode. Registration was accomplished by a global wafer registration and then by a die-by-die registration. The gate-to-source distance is 250 nm. The exposure dosages for the 50 and 100 nm gate lines are 2 and 3.5 nC/cm, respectively. The current was then changed to 10 nA, the global wafer and chip registration performed again, and the large area pads were exposed at 280 μC/cm^2. The image was then developed and the gate recess etched using a hydrogen peroxide etch, just prior to the Ti/Pt/Au metallization. Liftoff was accomplished by immersion in a warm bath of methylene

chloride. Figure 2 shows the processed FET.

Initially single level resist was used to define the gates. By carefully choosing the exposure and development conditions linewidths from 50 to 250 nm with an undercut profile can be obtained. MESFETs and MODFETs were processed. Figure 3a shows a typical FET with a drain to source channel length of 1.8 μm, a gate to source separation of 250 nm and a gate length of 100 nm. The current voltage characteristic, Figure 3b, shows an extrinsic transconductance of 540 mS/mm. Despite the fact that the gate resistance was as high as 1600 Ω/mm, these devices demonstrated state-of-the-art d.c. and microwave performance [12].

After this initial phase, work was begun to reduce the gate resistance while maintaining the ultrashort gate length. A multi level resist process was developed. Previous work by Chao et al. [3] used three levels of resist (PMMA/copolymer PMMA/PMMA) to form a resist profile with a 0.25 μm gate "foot print" and a top opening as wide as 0.75. In order to use this process for ultrashort gate lengths a barrier layer was added to improve the selectivity of developers. Figure 4a shows the four layer structure, the gate length is 100 nm and the top opening is 500 nm. This resist structure provides approximately a five fold increase of the cross sectional area of the gate metal. Figure 4b shows the processed gate, in this case the gate length is 75 nm and the end to end resistance of a one millimeter pattern is 220 to 300 Ω/mm. This is the shortest gate length reported for such a low resistance gate.

B. FET Layout and Test Cell

In order to measure the high intrinsic current gain cut-off frequency $(f_T)_i$ predicted for these short gate length transistors, it is essential that the parasitics associated with the FET are eliminated. While this is not possible, parasitic parameter values can be minimized, to maximize the measured $(f_T)_m$, and a test cell designed to provide for accurate de-embedding of the residual parasitics effects.

Figure 5, shows the FET layout that was designed to minimize the inductive and capacitive parasitics. The source configuration is such that it can be wafer probed at microwave frequencies. Microwave characterization of this FET layout indicated that input pad capacitance was less than 14 fF, gate and drain inductances less than 40 pH and a source inductance less than 10 pH. While these values are small so that they only perform a small pertubation of the measured data, to achieve accurate values of the intrinsic FET parameters, e.g. $(f_T)_i$, it is essential that they are accurately determined and de-embedded. To achieve this goal, the test cell shown in Figure 6 was designed. It consists of four rows (A-D) and seven columns (1-7),

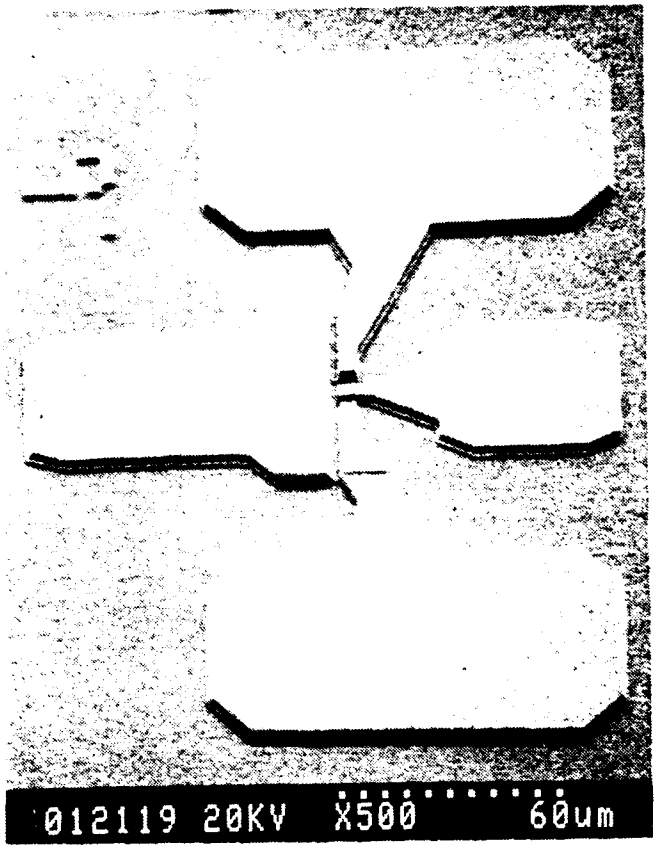
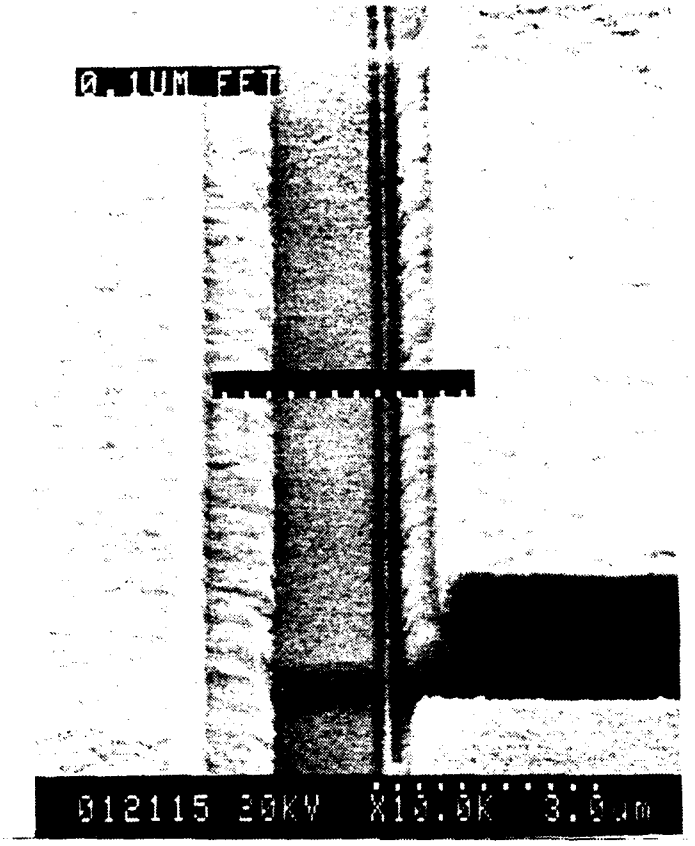


Figure 2 Processed FET. Gate length is 100 nm and gate width is 50 um.

(a)



(b)

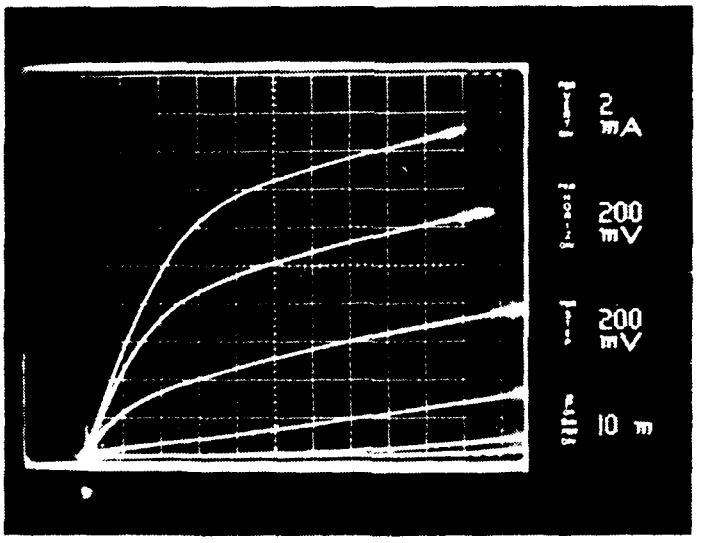
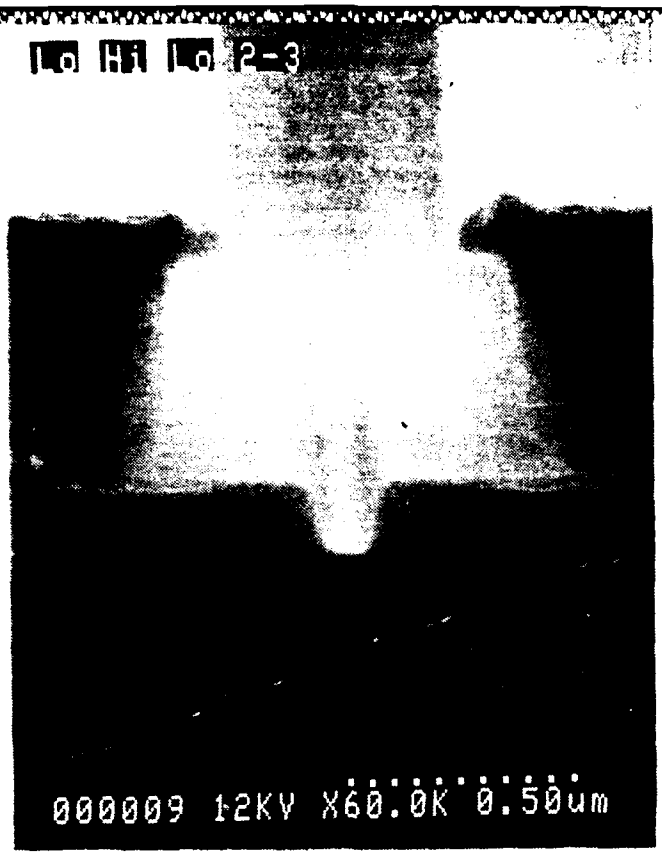


Figure 3 (a) 100 nm gate length FET, gate to source spacing is 250 nm. (b) I_{DS} vs V_{DS} vs V_g transistor characteristic.

(a)



(b)

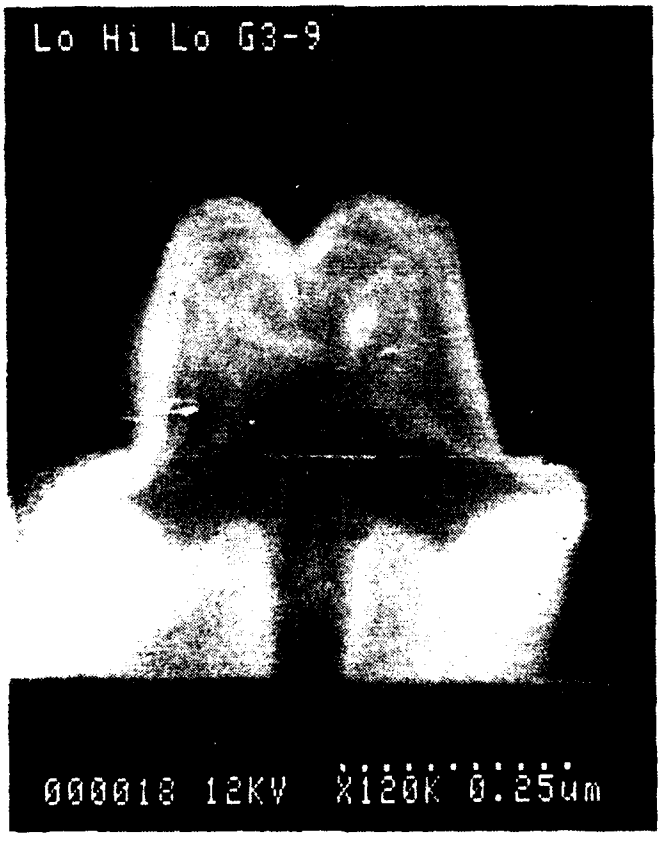


Figure 4 (a) Four level resist for low resistance and short gate length, and (b) gate metal cross section, gate length is 75 nm.

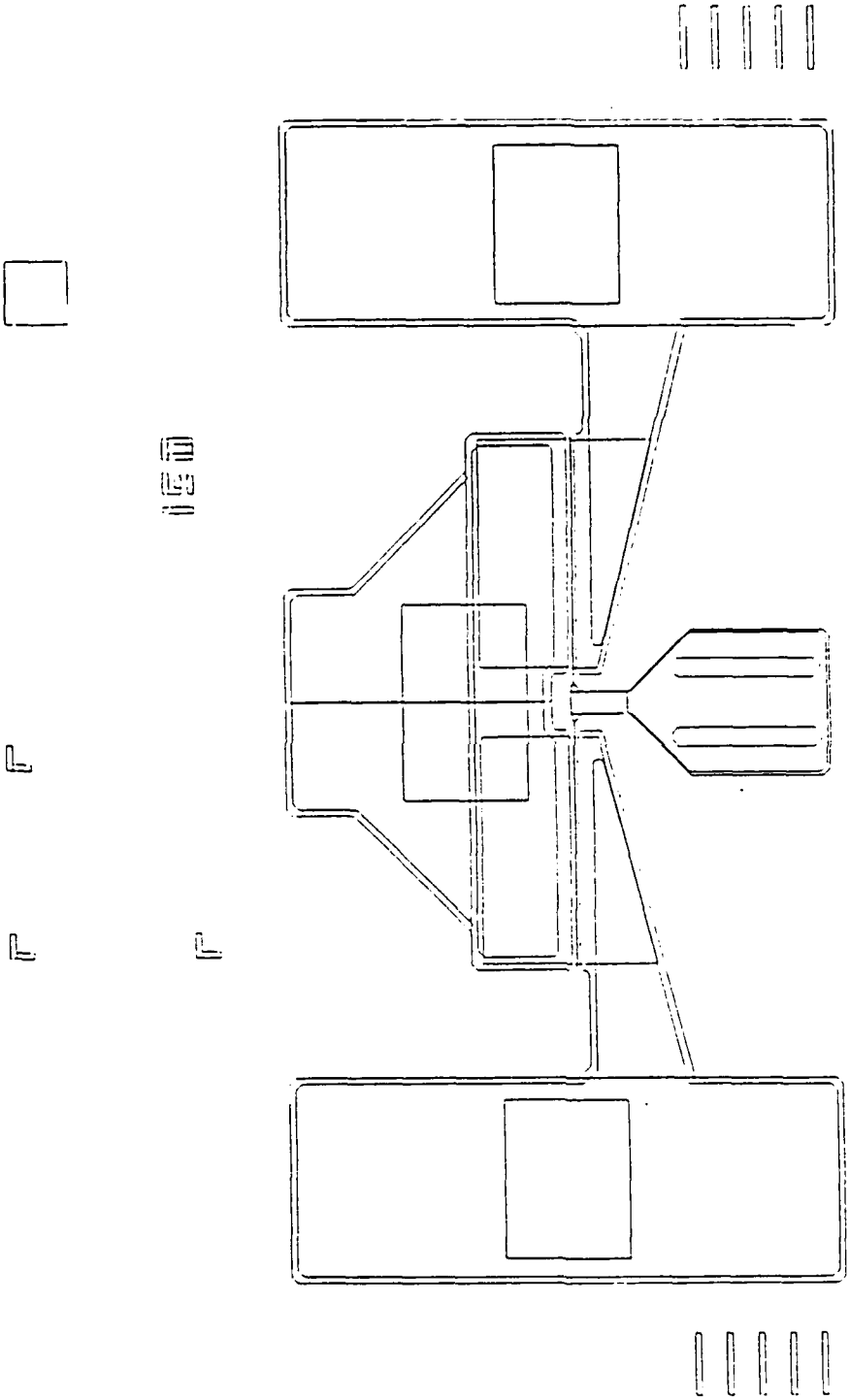


Figure 5 Low parasitic microwave FET layout for cascade wafer probing.

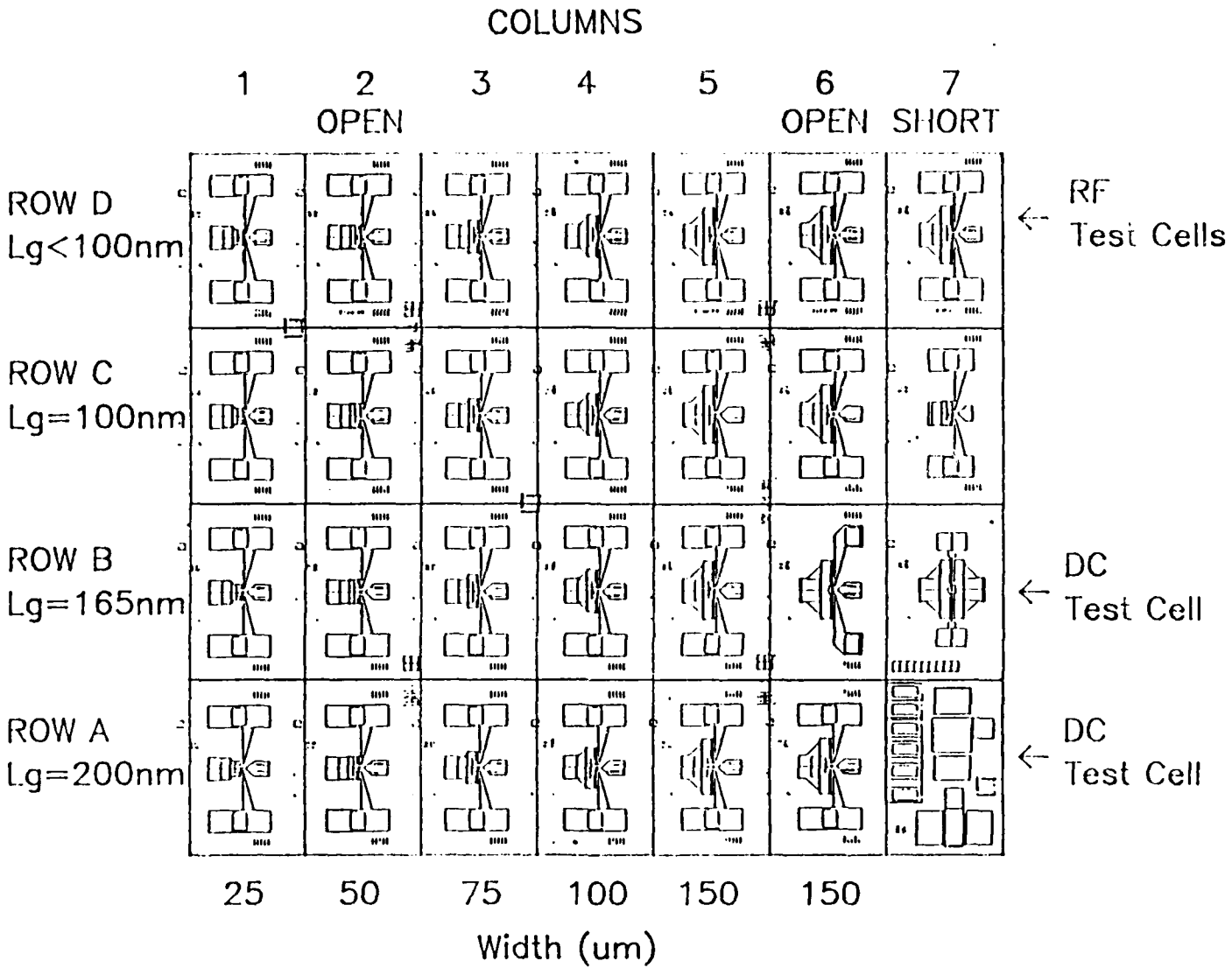


Figure 6 FET test cell.

plus some DC test patterns. The gate length was varied from 200 to 100 nm in rows A to C; row D was used for developing a smaller gate length process and for calibration standards. Six columns were used for varying the FET width from 25 μm to 150 μm. The transistor parameters varied linearly with width, while the parasitics were constant. Analysis of the variation of transistor parameters with width allows the parasitics to be determined and their effect removed (de-embedded).

The calibration standards provided a direct measurement of the parasitic parameters and so provided verification of the de-embedding procedure.

C. Accurate On-Wafer Microwave Characterization

In order to characterize short gate length FET structures accurately, it was necessary to upgrade the microwave measurement facilities. Measurement of FET structures in coaxial test fixtures introduce parasitics that distort considerably the results. To overcome these problems an on-wafer characterization capability was developed using a HP8510B Network Analyzer and a Cascade Microtech Probe Station.

On-wafer characterization provides a low parasitic test environment which can be calibrated to the FET reference plane. It is this capability that allows FET structures of different gate lengths and widths and FET calibration standards to be measured simply and accurately with the same test environment parasitics and reference plane, thus allowing the full potential of the test cell developed to be utilized.

To further improve the utilization of this new measurement capability, new analysis techniques and software were developed. The measured S-parameter data was processed using Y-matrix and Z-matrix malipulations. This allows for:

i) de-embedding of parasitic effects,

ii) synthesis of the FET circuit topology,

iii) direct extraction of FET circuit parameters without the need for an optimizer,

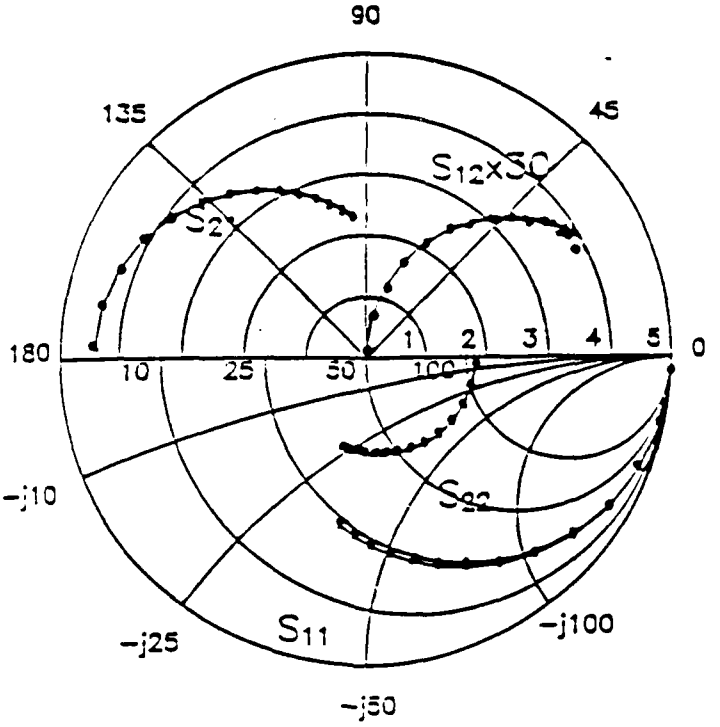
iv) extraction of FET parasitic components, e.g. R_S, R_D, and

v) bias scans to be performed at microwave frequencies in real time.

D. Analysis of Measured Data

While each of the stages in the project have been characterized and analyzed in great detail, at present only a few fabricated wafers have been characterized in order to obtain information about electron transport.

Figures 7 and 8 show the S-parameters and calculated current gain of a pulse doped $Al_{.3}Ga_{.7}As/GaAs$ and uniformly doped $Al_{.2}Ga_{.8}As/Ga_{.85}In_{.15}As$ MODFETs, respectively, both



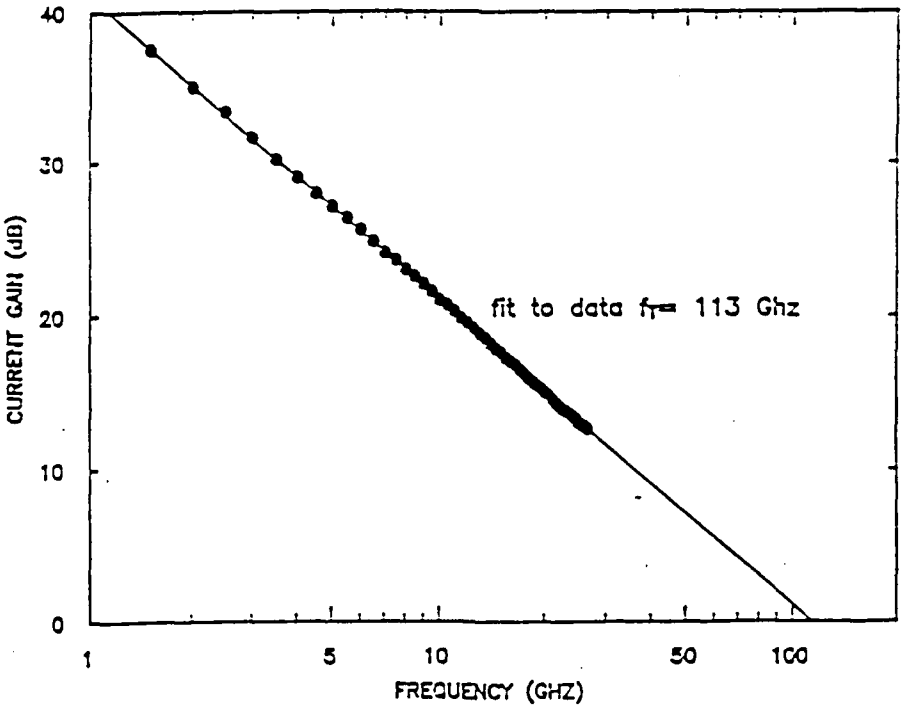
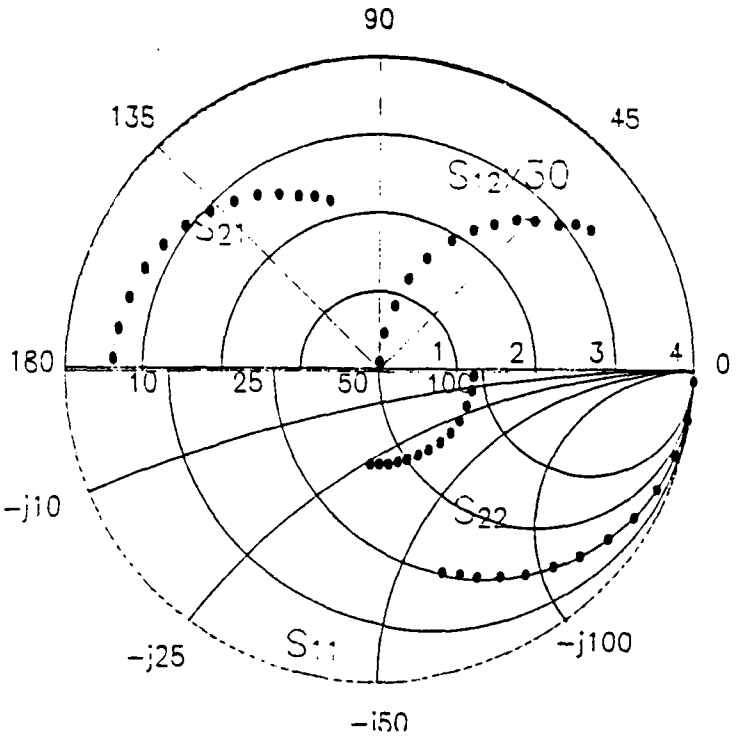


Figure 7 S-parameters and calculated current gain of a pulse-doped $Al_{.3}Ga_{.7}As$/GaAs MODFET, L_g = 100 nm, width = 150 μm.



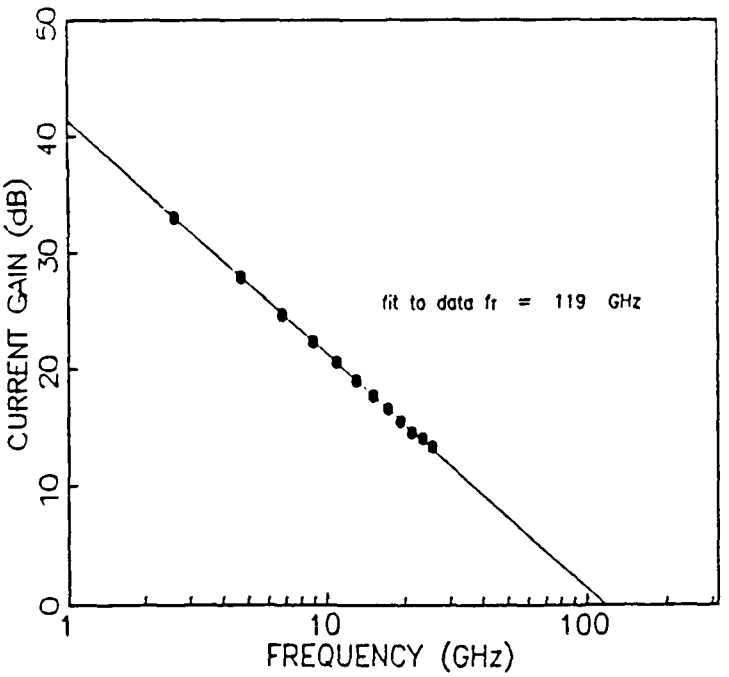


Figure 8 S-parameters and calculated current gain of a uniformly doped $Al_{.2}Ga_{.8}As/Ga_{.85}In_{.15}As$ MODFET, L_g = 100 nm, width = 150 μm.

with a gate length of L_g = 100 nm and width of 150 μm. The results show how the combination of low parasitic FET layout with on-wafer characterization produced "clean" S-parameters. The calculated current gain rolls off at 6 dB per octave (predicted theoretically) and so can be extrapolated unambiguously to give the measured current gain cut-off frequency $(f_T)_m$. The values obtain 113 GHz and 118 GHz for the AlGaAs/GaAs and AlGaAs/GaInAs MODFETs, respectively, are the best values ever reported for each transistor structure.

To eliminate the effect of the pad capacitance parasitics, the $(f_T)_m$ is analyzed as a function of gate width. Figure 9a shows the variation of $(f_T)_m$ with gate width for the AlGaAs/GaInAs MODFET structure. The function form of $(f_T)_m$ with gate width observed is given by

$$(f_T)_m = g_m.W/(2\pi\{C_{gs}.W + C_{gd}.W + C_{pad}\}), \qquad (1)$$

where W = gate width

g_m = normalized extrinsic transconductance

C_{gs} = normalized gate to source capacitance

C_{gd} = normalized gate to drain capacitance

C_{pad} = input parasitic pad capacitance.

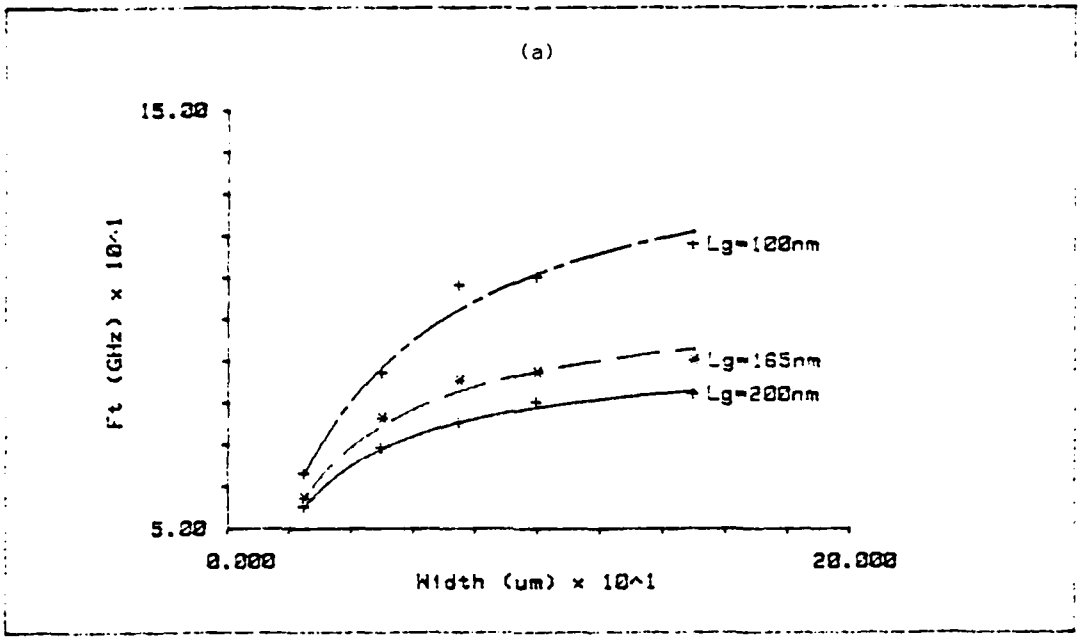
Rearranging this expression gives

$$1/(2\pi(f_T)_m) = 1/(2\pi(f_T)_\infty) + \{C_{pad}/(g_m)\}\{1/(W)\}, \qquad (2)$$

where $(f_T)_\infty$ = current gain cut-off frequency of a transistor with an infinite width where input pad parasitics have no effect.

Figure 9b shows the measured data plotted in this linear form, confirming expression (2). From the slopes of these graphs, the input pad capacitance was found to be 12-14 fF, which was consistent with the value of 12 fF measured directly using the calibration standards. This confirmed that the input pad capacitance was being correctly determined and so the de-embedded $(f_T)_\infty$ of transistor was being correctly extracted.

Table 1 summarizes the de-embedded results, all these values are the state-of-the-art.



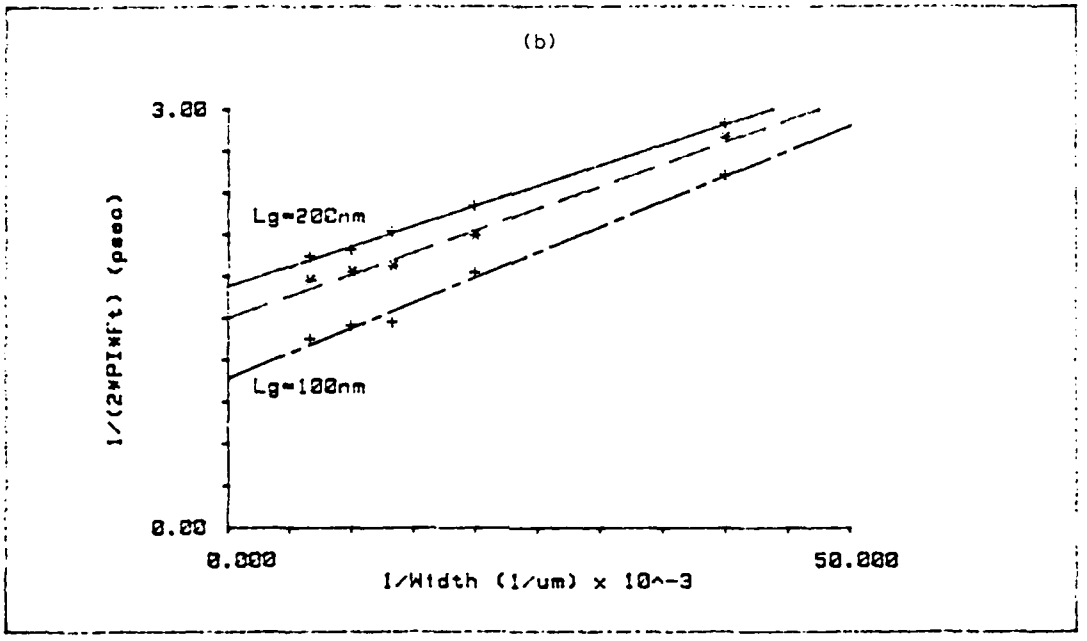


Figure 9 Variation of $(f_T)_m$ with FET width and L_g for the uniformly doped $Al_{.2}Ga_{.8}As/Ga_{.85}In_{.15}As$ MODFET.

AlGaAs/GaAs	Pulse Doped MODFET
L_g (nm)	$(f_T)_\infty$ (GHz)
200	78
165	89
100	124

$Al_{.2}Ga_{.8}As/Ga_{.85}In_{.15}As$	Uniformly Doped MODFET
L_g (nm)	$(f_T)_\infty$ (GHz)
200	92
165	106
100	149

Table 1

To determine the effective electron velocity, the variation of $(f_T)_\infty$ versus gate length is considered. This is shown in Figure 10a. The functional form of $(f_T)_\infty$ with gate length observed is the same as that observed for longer gate length transistors, and is given by

$$(f_T)_\infty = v_{EFF}/(2\pi(L_g + d)), \qquad (3)$$

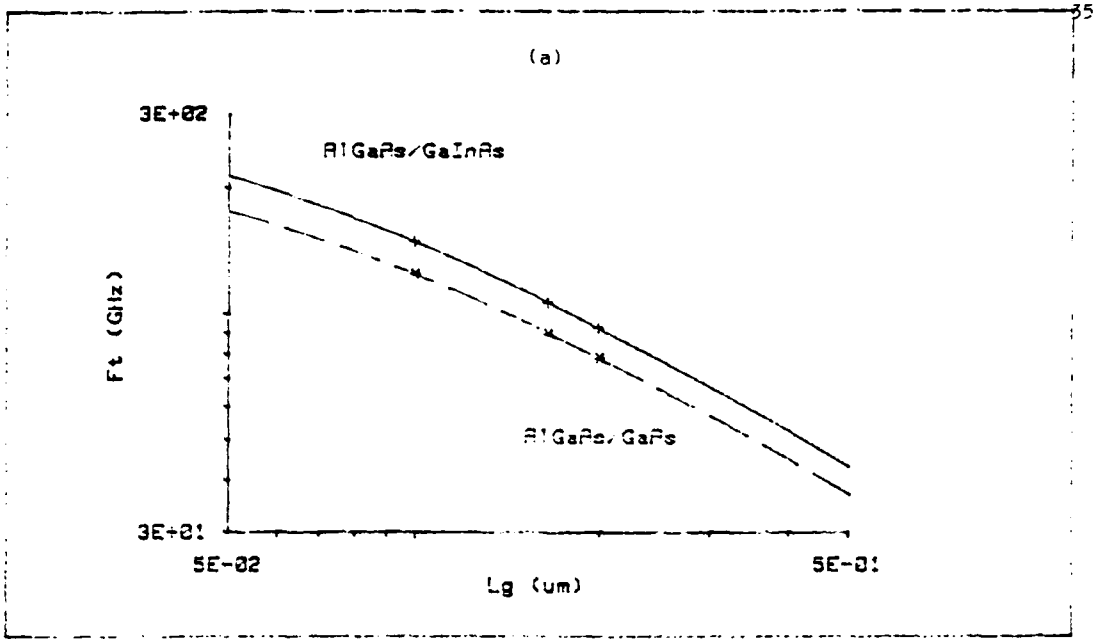
where v_{EFF} = effective saturated electron velocity

d = apparent extension of gate length caused by fringing effects and parasitic resistance effects.

Rearranging this expression gives

$$1/(2\pi(f_T)_\infty) = (L_g + d)/v_{EFF}. \qquad (4)$$

Figure 10b shows the measured data plotted in this linear form, confirming expression (4). From the slopes of these graphs the effective electron velocities are determined. A value of 1.3 x 10^7cm/s is obtained for the pulse doped $Al_{.3}Ga_{.7}As$/GaAs MODFET and a value of 1.5 x 10^7cm/s is obtained for the uniformly doped $Al_{.2}Ga_{.8}As/Ga_{.85}In_{.15}As$ MODFET. These values are very similar to those obtained on MODFET with gate lengths greater than 250 nm.



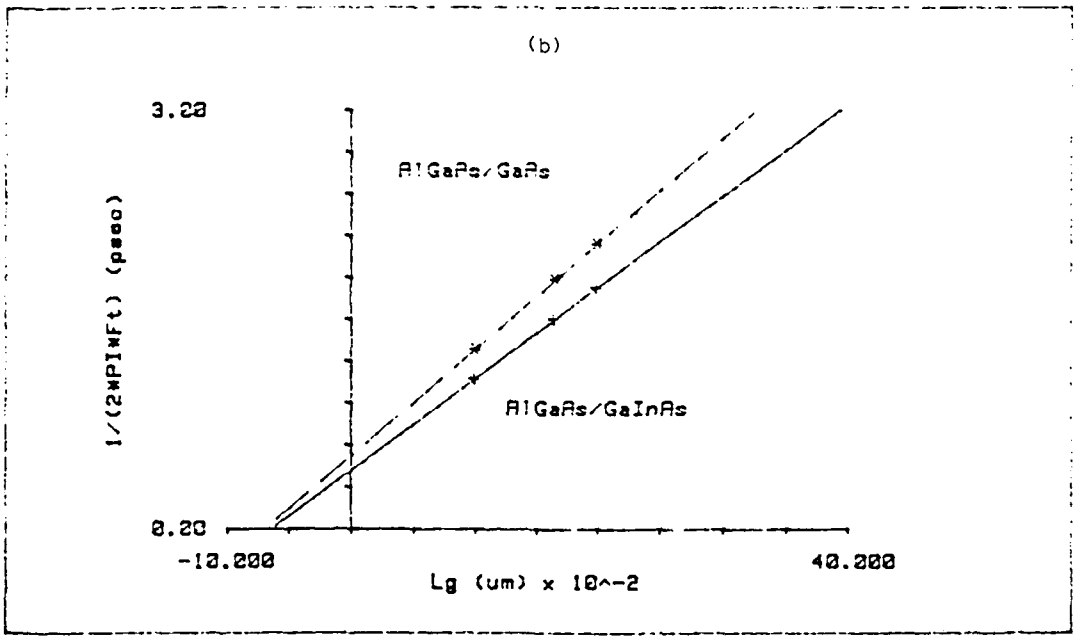


Figure 10 Variation of $(f_T)_\infty$ with gate length for the pulse doped $Al_{.3}Ga_{.7}As/GaAs$ MODFET and the uniformly doped $Al_{.2}Ga_{.8}As/Ga_{.85}In_{.15}As$ MODFET.

Preliminary analysis of the measured results thus indicating

i) no evidence of non-equilibrium transport, or

ii) that non-equilibrium transport effects may not dominate the terminal characteristics of nanometer gate length FETs.

As well as the variation of $(f_T)_\infty$ with gate length, the I-V characteristics of 100 nm gate length FET are similar to longer gate length structures, see Figure 11. For example, the bias dependence of transconductance and f_T, shown in Figure 12, of 100 nm gate length FETs are identical to that obtained previously on 1 μm gate length structures.

A detailed model has been developed at Cornell University which can explain the variation of f_T of MODFETs at 1 μm gate lengths with material structure and bias in terms of charge considerations [14,15]. It can be shown that the intrinsic f_T of MODFETs is actually given by

$$(f_T)_i = v_{sat}/(2\pi L_g) \cdot ME = v_{eff}/(2\pi L_G) \quad (5)$$

where v_{sat} = saturated electron velocity

v_{eff} = effective saturated electron velocity

The additional term ME (Modulation Efficiency) is introduced by this analysis represents how efficient the MODFET structure is in utilizing the charge modulated by the gate. It has been determined that in MODFET structures two mechanism dominate ME:

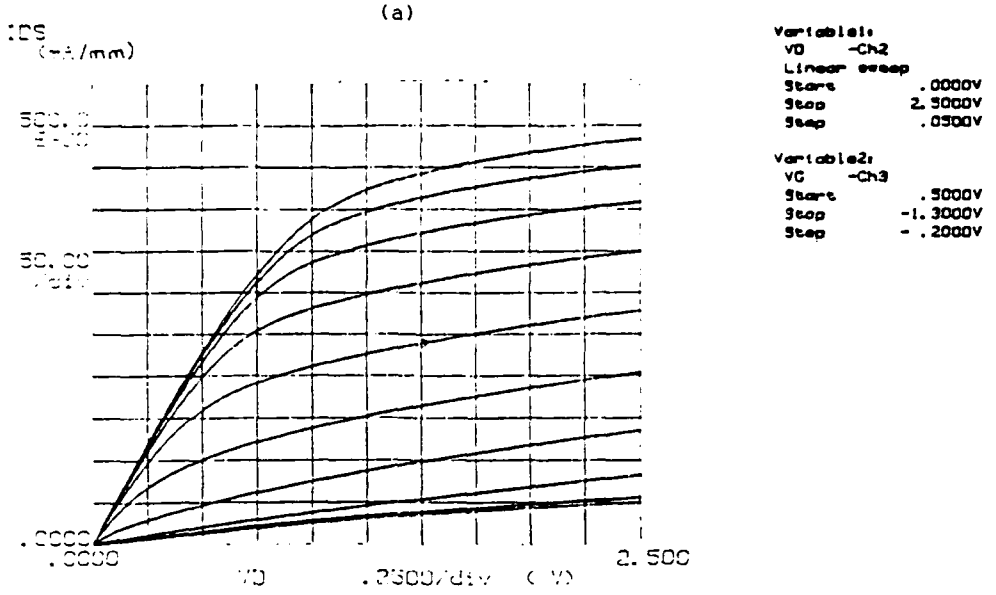
i) parasitic charge modulation in the electron supply layer which degrades the modulation efficiency at high current levels, and

ii) non-uniform electron velocities under the gate (gradual channel behavior) which degrades the modulation efficiency at low current levels.

The interaction of these two mechanisms explains the Gaussian shaped, g_m and f_T characteristics of MODFETs. In addition, the interaction of these two mechanisms limits the maximum ME achieved to values less than unity and can thus explain the variation of f_T, hence v_{eff}, with material structure, i.e. spacer thickness, uniform versus pulse doped, GaAs versus GaInAs channels, etc. and bias with a constant value of $v_{sat} = 2.0 \times 10^7$cm/s [15].

The basic conclusion of this model is that the peak f_T of the transistor, thus the maximum effective electron velocity, will increase if the 2DEG sheet density can be increased. This has recently been achieved using a high indium composition pulsed doped $Al_{.3}Ga_{.7}As/Ga_{.75}In_{.25}As$ MODFET structure. The maximum 2DEG sheet density of this

(a)



(b)

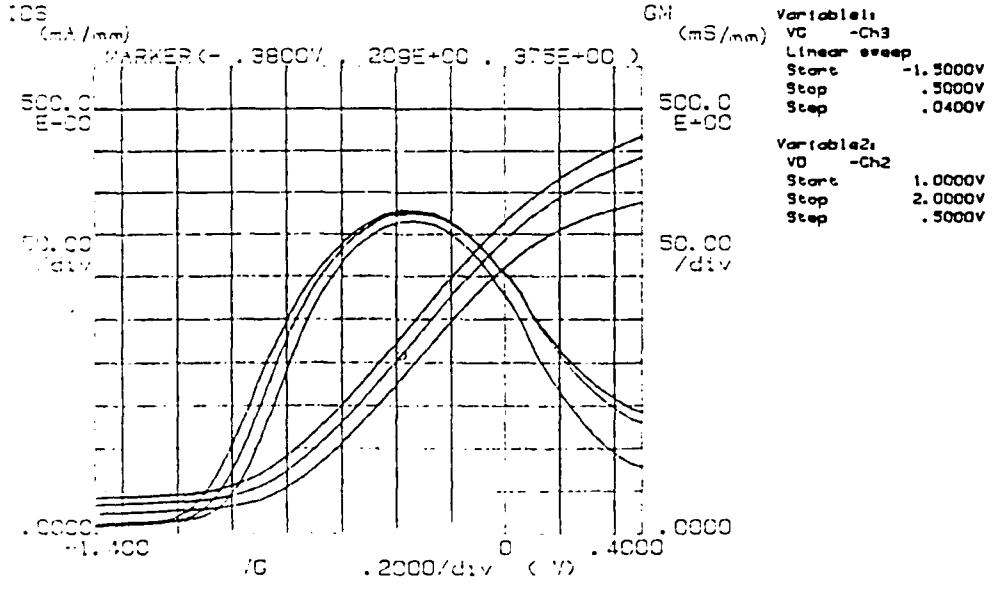
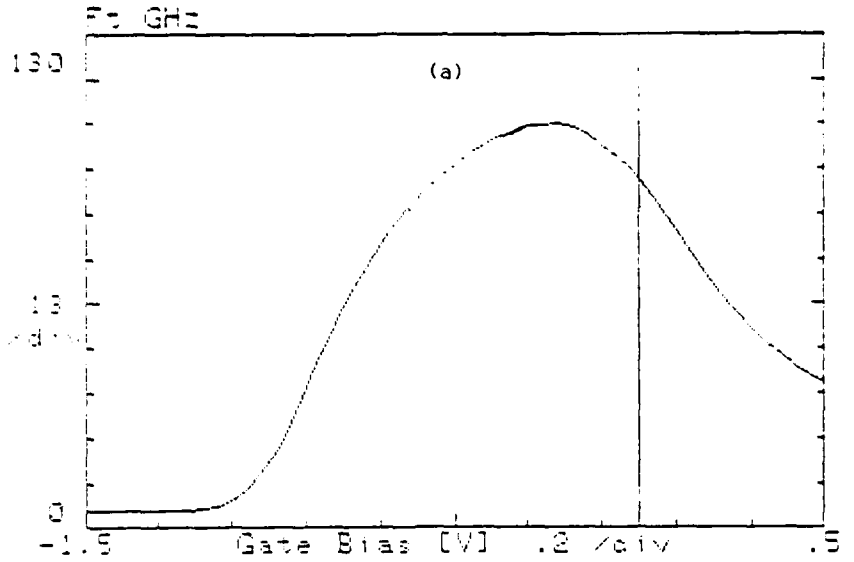


Figure 11 I-V characteristics (a) and transfer characteristics (b) of a short gate length (L_g = 100 nm, width = 150 μm) uniformly doped $Al_{.2}Ga_{.8}As/Ga_{.85}In_{.15}As$ MODFET.



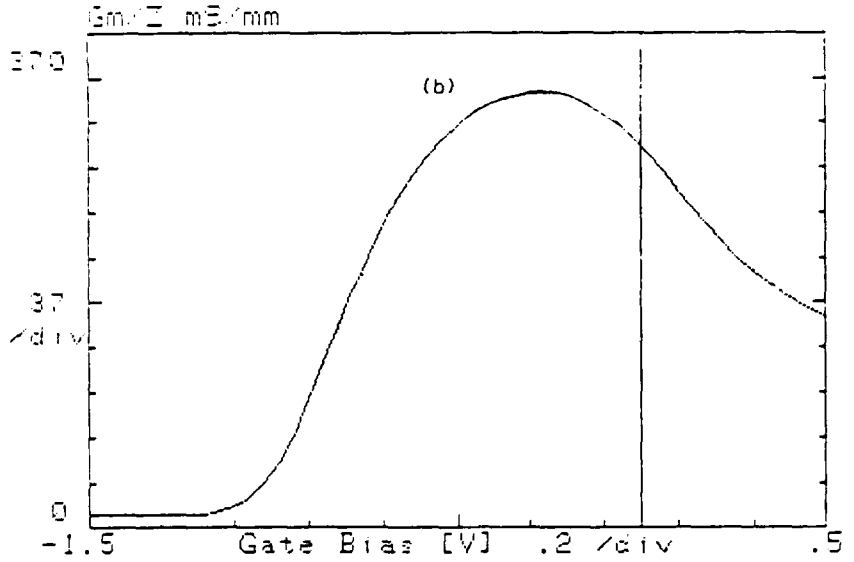


Figure 12 Variation of $(f_T)_m$ and extrinsic transconductance with gate bias (V_{DS} = 1.5 volts) obtained from a S-parameter bias scan performed at 10 GHz.

structure is greater than 2.4 x $10^{12}cm^{-2}$. A L_g = 180 nm MODFET using this structure gave a $(f_T)_m$ = 122 GHz, for a 150 μm width transistor [16]. This is the highest value ever reported for a GaAs substrated based transistor and corresponds to an effective electron velocity of 1.8 x 10^7cm/s [13]. Figure 13 summarizes the state-of-the-art results as of May 1988.

These results indicate that the simple model appears to be not only able to explain the behavior of long gate length transistors but also short gate length transistors (100-200 nm) since the characteristic are identical, indicating that, at 300 K, charge control considerations may still dominate over non-equilibrium transport considerations in determining the terminal characteristics of the MODFET even at 100 nm gate lengths.

A detailed analysis of the FET circuit model of 100 nm gate length transistor indicated that the measured $(f_T)_m$ is not only limited by pad capacitance parasitics but also by source and drain parasitic resistances. To first order the relationship between the measured $(f_T)_\infty$ and the intrinsic $(f_T)_i$ is as follows:

$$1/(2\pi(f_T)_\infty) = \{1/(2\pi(f_T)_i) + t_{RC}\} \cdot \text{Factor} \quad (6)$$

where $\text{Factor} = 1 + G_{ds}(R_S + R_D)$

and $t_{RC} = R \cdot C_{gd}$

$= (R_S + R_D)/(1 + G_{ds}(R_S + R_D))$

These terms account for the fact that when measured the intrinsic FET is not short circuited but is loaded by $R_S + R_D$, the sum of the parasitic source and drain resistances.

When the gate length was large > 250 nm, the intrinsic time delay of the FET was large compared to t_{RC}. This is no longer true as the gate length is reduced to 100 nm. The accurate determination of these parasitic resistive components is not, however, simple. Using the new analysis techniques developed during this work combined with measurements of the active FET, passive FET and calibration standards, a self-consistent set of solutions was obtained from which R_S and R_D could be determined [17].

Table 2 summarizes the components effecting the measured $(f_T)_\infty$ of the 100 nm gate length MODFET (width = 150 μm).

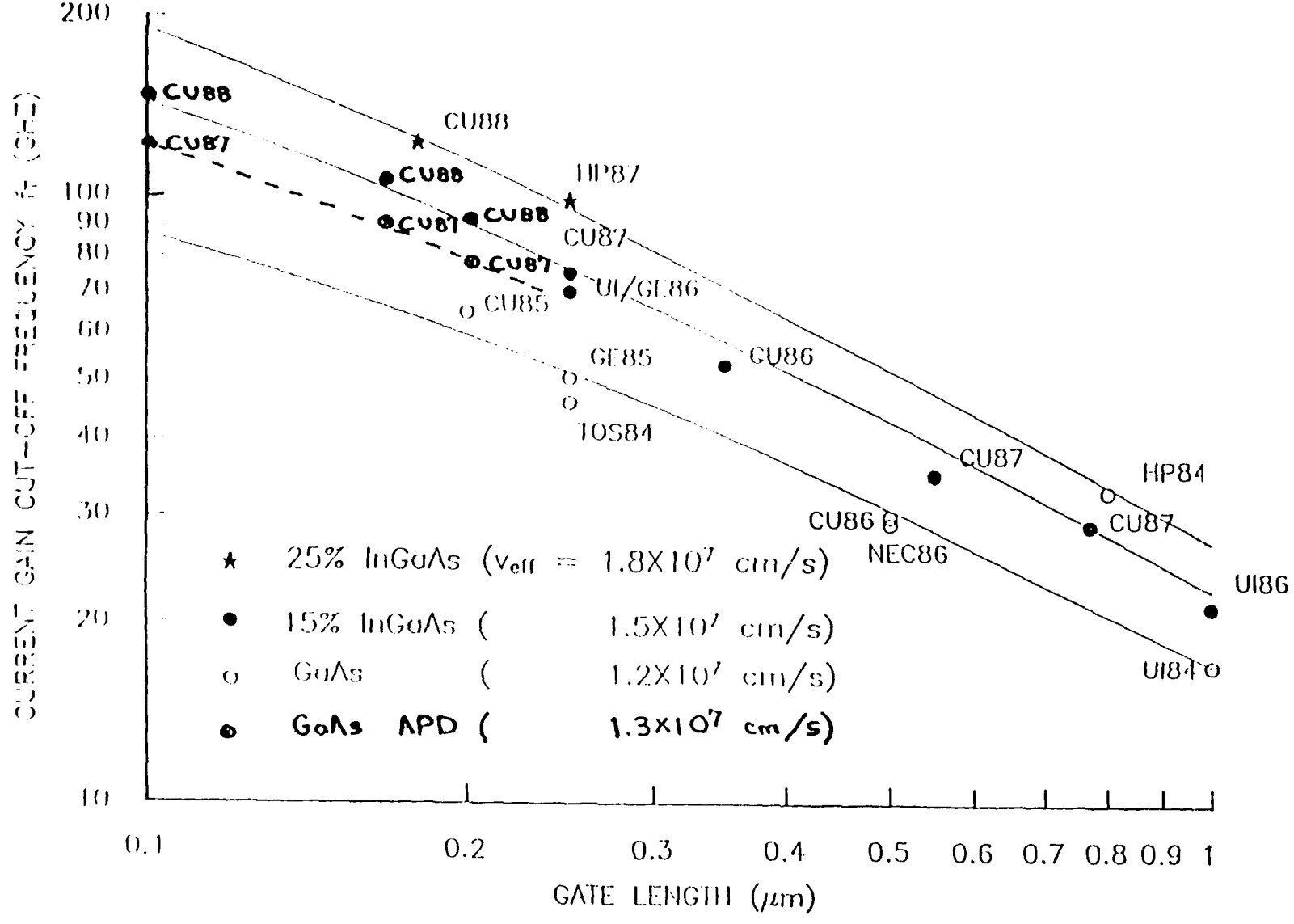


Figure 13 State-of-the-art GaAs and GaInAs channel MODFET results as of May 1988. All results for gate lengths less than 200 nm were obtained on this JSEP Task #3. [APD = Atomic Planar Doped (Pulse Doped)].

	Pulse Doped AlGaAs/GaAs MODFET	Uniformly Doped AlGaAs/GaInAs MODFET
$(f_T)_\infty$	124 GHz	149 GHz
$(1/f_T)_\infty$	1.284 pS	1.075 pS
Factor	0.156	0.16
t_{RC}	0.138 pS	0.0668 pS
$(1/f_T)_i$	0.972 pS	0.860 pS
$(f_T)_i$	164 GHz	185 GHz

Table 2

These results are preliminary but they do indicate that parasitic resistances play for the first time a major role in limiting the performance of short gate length transistors. In addition, the de-embedded results indicate that the electron transit time of these transistor structures is now well below 1 ps.

This correction of the measured data does not change the extracted velocity but only the value of d, the effective gate length extension. Removal of the parasitic resistance effects, for example, reduced d to 364 A for the AlGaAs/GaInAs MODFET. This remaining component of parasitic delay capacitive results from capacitive fringing effects which will become very important as the gate length is further reduced.

Apart from f_T, f_{max} (frequency up to which the transistor exhibits power gain) is also an important figure of merit. The maximum value of f_{max} achieved was only 160 GHz. This was a disappointingly low number, indicating a poor f_{max}/f_T ratio. Analysis of the FET circuit components combined with a detailed characterization of the calibration standards indicated that the gain of these short gate length transistors was limited by a parasitic feedback capacitance associated with the FET layout. Using the analysis tool developed, with on-wafer microwave characterization coupled with transistor fabrication, the FET layout has been redesigned [18]. Recently transistors fabricated using this modified layout were fabricated using L_g = 300 nm gate length, a value of f_{max} = 160 GHz was achieved in this case, when f_T = 53 GHz, indicating

that redesigning the FET layout to eliminate the feedback capacitance term did significant improvement in f_{max}/f_T ratio. Short gate length transistor fabricated using this new layout have the potential for realizing f_{max} values greater than 400 GHz.

SCIENTIFIC IMPACT OF RESEARCH

Transistors with nanometer gate lengths (100-200 nm) have been fabricated that have demonstrated superior performance over 250 nm gate length transistors. This is the first time such results have ever been reported. These transistors had measured extrinsic current gain cut-off frequencies over 110 GHz and intrinsic current gain cut-off frequencies over 160 GHz. This corresponds to an electron transit time of less than 1 psec.

In order to achieve these results, the following key technologies and procedures were developed:

A. A 75 to 200 nm footprint "T" cross section FET gate technology.

B. Low parasitic FET layout that optimizes the performance of short gate length FET structures. An FET test cell designed that includes noval microwave FET calibration standards that allowed layout parasitics to be measured directly at microwave frequencies, and

C. Microwave on-wafer characterization combined with specialized analysis techniques that provide for unambiguous parasitic de-embedding and circuit modeling of FET structures.

All of these developments have greatly advanced the state-of-the-art in fabrication, design and characterization of short gate length transistors which, for example, resulted in the recent re-optimization of the FET layout for millimeter wave applications. This research has demonstrated that short gate length transistors have great potential for millimeter wave and sub millimeter wave system applications. It is believed that continued progress of this project, using the new high indium composition materials recently developed, combined with the recently re-designed FET layout, could have produced a transistor with a measured extrinsic $(f_T)_m$ > 175 GHz with a f_{max} > 500 GHz (i.e., 18 dB of gain at 60 GHz).

Analysis of the results have indicated that the behavior of short gate length transistors is similar to long gate length transistors. No evidence of non-equilibrium transport mechanisms, e.g. velocity overshoot has been obtained. The behavior of these transistors is consistent with that predicted by a simple theory developed at Cornell for long gate length transistors that indicates that charge control considerations dominate over non-equilibrium transport considerations in determining the terminal characteristics of FETs. The implications of these initial observations need further investigation.

Analysis of the FET circuit model indicate that parasitic resistance components are now an important factor in limiting the speed of FET structures (when the gate dimension is reduced to 100 nm). Further improvements in transistor speed and performance are going to require, therefore, the scaling down of these parasitic resistance components as well as the gate dimensions. The dimensions of the gate to source and the source to drain separations must be also reduced to nanometer dimensions. Initial work at Cornell using the JEOL e-beam lithography machine indicated that the source-drain separation can be reduced to at least 500 nm. Further research is clearly required in this area.

DEGREES

A.N. Lepore, May 1988, Ph.D. Thesis
"Design, Fabrication, and Performance of Aluminum Gallium Arsenide/Gallium Arsenide Modulation-Doped Field-Effect Transistors for High-Speed Applications"

G.W. Wang, May 1988, Ph.D. Thesis
"Ultra Short Gate Lattice Mismatched Modulation Doped Field Effect Transistors"

Y.K. Chen, May 1988, Ph.D. Thesis
"Submicrometer Gate Planar-Doped Pseudomorphic Multiple-Heterojunction MODFETs for Millimeter-Wave and Optical Communication"

S.F. Anderson, August 1988, M.S. Thesis
"The Use of Buried Beryllium-Doped Layers to Reduce Buffer Current in Low Noise Pseudomorphic Modulation-Doped Field-Effect Transistors"

REFERENCES

1. "The Correct Determination of Intrinsic f_T of FET Devices from Measured Microwave Data", 11th European Workshop on Compound Semiconductor Devices and Integrated Circuits, Grainau, W. Germany (May 4-6, 1987).

2. Comments on "A New Low-Noise AlGaAs/GaAs 2DEG FET with a Surface Undoped Layer", L.D. Nguyen, P.J. Tasker and W.J. Schaff, IEEE Trans. Elec. Dev., ED-34 (5) 1187-1188 (May 1987).

3. "Electron Beam Fabrication of Quarter Micron T-Shaped Gate FETS Using a New Tri-Layer Resist System", P.C. Chao, P.M. Smith, R.C. Tiberio and E.D. Wolf, IEDM, 613 (Dec. 1983).

4. "Gate-Length Dependence of the Speed of SSI Circuits Using Submicrometer Selectively Doped Heterostructure Transistor Technology", N. Shah, S.S. Pei, C.W. Tu and R.C. Tiberio, IEEE Trans. on Elec. Dev., 543 (May 1986).

5. "Scaled GaAs MESFET's with Gate Length Down to 100 nm", H. Jaeckel, V. Graf, B.J. Van Zeghbroeck, P. Vettiger and P. Wolf, IEEE Elec. Dev. Lett., Z (9), 522 (Sept. 1986).

6. "Microwave Characterization of Very High Transconductance MODFET", L. Camnitz, P.J. Tasker, H. Lee, D. van der Merwe and L.F. Eastman, IEDM Technical Digest, 360-363 (Dec. 1984).

7. "Sub-Micrometer Quantum Well HEMT with $Al_{0.3}Ga_{0.7}As$ Buffer Layer", L.H. Camnitz, P.A. Maki, P.J. Tasker and L.F. Eastman, 11th Int. Symp. on GaAs and Related Cpds., Biarritz, France (Sept. 26-28, 1984); Inst. Phys. Conf. Ser. No. 74, Ch. 4, 333-338 (1985).

8. "Charge Control, DC and RF Performance of a 0.35 μm Pseudomorphic AlGaAs/InGaAs Modulation-Doped Field Effect Transistor", IEEE Trans. Elec. Dev., 35, 139-144 (Feb. 1988).

9. "Carrier Deconfinement Limited Velocity in Pseudomorphic AlGaAs/InGaAs Modulation-Doped Field Effect Transistors (MODFET's)", L.D. Nguyen, M.C. Foisy, P.J. Tasker, W.J. Schaff, A.N. Lepore and L.F. Eastman, Proc. IEEE/Cornell Conf. on Advanced Concepts in High Speed Semiconductor Devices and Circuits, 60-69 (1987).

10. "0.1 μm Gate Length MODFET's with Unity Current Gain Cut-Off Frequency Above 110 GHz", A.N. Lepore, H.M. Levy, R.C. Tiberio, P.J. Tasker, H. Lee, E.D. Wolf, L.F. Eastman and E. Kohn, IEEE Elec. Lett., 24 (6) 364-366 (March 1988).

11. "Influence of Quantum Well Width on dc and rf Device Performance in Pseudomorphic $Al_{0.3}Ga_{0.70}As/In_{0.25}Ga_{0.75}As$ MODFETs", L.D. Nguyen, DRC, University of Colorado, Boulder, CO (June 20-22, 1988).

12. "Fabrication and Characterization of Ultrashort Gate Length GaAs Field-Effect Transistors", R.C. Tiberio, E.D. Wolf, S.F. Anderson, W.J. Schaff, P.J. Tasker and L.F. Eastman, Proc. 31st Int. Symp. on Electron, Ion, and Photon Beams, J. Vac. Sci. Tech. B, 6 (1) (Jan./Feb. 1988).

13. "Electron Velocities in Submicron Gate-Length MODFETs", P.J. Tasker, M. Foisy, L. Nguyen and L.F. Eastman, 12th Workshop on Compound Semiconductor Devices and Integrated Circuits, Lugano, Switzerland (May 9-11, 1988).

14. "Modulation Efficiency Limited High Frequency Performance of the MODFET", M.C. Foicy, J.C. Huang, P.J. Tasker and L.F. Eastman, Picosecond Elec. and Optoelec. II, ed. F.J. Leonberger, C.H. Lee, F. Capasso, H. Morkoc (Springer-Verlag, Berlin) p. 181 (1987).

15. "The Role of Inefficient Charge Modulation in Limiting the Current Gain Cutoff Frequency of the MODFET", M.C. Foisy, P.J. Tasker, B. Hughes and L.F. Eastman, IEEE Trans. (July 1988).

16. "0.2 μm Gate-Length Atomic-Planar Doped Pseudomorphic $Al_{0.3}Ga_{0.7}As/In_{0.25}Ga_{0.75}As$ MODFET's with f_T over 120 GHz", L.D. Nguyen, D.C. Radulescu, P.J. Tasker, W.J. Schaff and L.F. Eastman, Elec. Dev. Lett. (July 1988).

17. P.J. Tasker, to be published.

18. P.J. Tasker, to be published.

JSEP PUBLICATIONS AND PRESENTATIONS

1. "DC and Microwave Performance of Single-Gate and Dual-Gate AlGaAs/InGaAs Double-Heterojunction MODFETs", Y.K. Chen, D.C. Radulescu, A.N. Lepore, G.W. Wang, P.J. Tasker and L.F. Eastman, 11th European Workshop on Compound Semiconductor Devices and Integrated Circuits, Grainau, W. Germany (May 4-6, 1987).

2. "Optimized Heterojunction Barriers for MODFETS", L.F. Eastman, 11th European Workshop on Compound Semiconductor Devices and Integrated Circuits, Grainau, W. Germany (May 4-6, 1987).

3. "The Correct Determination of Intrinsic f_T of FET Devices from Measured Microwave Data", P.J. Tasker and L.F. Eastman, 11th European Workshop on Compound Semiconductor Devices and Integrated Circuits, Grainau, W. Germany (May 4-6, 1987).

4. "The Effect of Buried p-Doped Layers on the Current Saturation Mechanism in AlGaAs/InGaAs/GaAs MODFETs", S.F. Anderson, W.J. Schaff, P.J. Tasker, M.C. Foisy, G.W. Wang and L.F. Eastman, DRC, Santa Barbara, CA (June 22-24, 1987).

5. "Enhancement of 2DEG Density in GaAs/InGaAs/AlGaAs Double Heterojunction Power MODFET Structures by Buried Superlattice and Buried P^+-GaAs Buffer Layers", Y.K. Chen, D.C. Radulescu, M.C. Foisy, A.N. Lepore, G.W. Wang, P.J. Tasker and L.F. Eastman, DRC, Santa Barbara, CA (June 22-24, 1987).

6. "Carrier Deconfinement Limited Velocity in Pseudomorphic AlGaAs/InGaAs Modulation-Doped Field Effect Transistors (MODFET's)", L.D. Nguyen, M.C. Foisy, P.J. Tasker, W.J. Schaff, A.N. Lepore and L.F. Eastman, Proc. 11th Biennial Conf. on Advanced Concepts in High Speed Semiconductor Devices and Circuits, Cornell University, Ithaca, NY, 60-69 (Aug. 10-12, 1987).

7. "A High-Gain Short-Gate AlGaAs/InGaAs MODFET with 1 Amp/mm Current Density", G.W. Wang, Y.K. Chen, D.C. Radulescu, P.J. Tasker and L.F. Eastman, 14th Int. Symp. on GaAs and Related Cpds., Crete, Greece (Sept. 28-Oct. 1, 1987); Inst. Phys. Conf. Ser. 91, 737-740 (1988).

8. "Multilayer Electron Beam Resist for Fabrication of Ultra-Short Gate MODFETs", G.W. Wang, Y.K. Chen, D.C. Radulescu, W.J. Schaff, P.J. Tasker and L.F. Eastman, 172nd Meet. Electrochemical Society, Honolulu, Hawaii (Oct. 18-23, 1987).

9. "A High Performance 0.25-μm T-Shape Gate $Ga_{0.5}In_{0.5}As/Al_{0.5}In_{0.5}As$ MODFET Grown by MBE Lattice Mis-Matched on a GaAs Substrate", Y.K. Chen, G.W. Wang, W.J. Schaff, P.J. Tasker, K. Kavanaugh and L.F. Eastman, Proc. IEDM, Washington, DC, 431-434 (Dec. 6-9, 1987).

10. "Electron Velocities in Submicron Gate-Length MODFETs", P.J. Tasker, M. Foisy, L. Nguyen and L.F. Eastman, 12th Workshop on Compound Semiconductor Devices and Integrated Circuits, Lugano, Switzerland (May 9-11, 1988).

11. "Influence of Quantum Well Width on dc and rf Device Performance in Pseudomorphic

$Al_{0.3}Ga_{0.70}As/In_{0.25}Ga_{0.75}As$ MODFET's", L.D. Nguyen, D.C. Radulescu, P.J. Tasker, M.C. Foisy and L.F. Eastman, DRC, University of Colorado, Boulder, CO (June 20-22, 1988).

12. "0.1 μm Gate Length MODFET's with Unity Current Gain Cut-Off Frequency Above 110 GHz", A.N. Lepore, H.M. Levy, R.C. Tiberio, P.J. Tasker, H. Lee, E.D. Wolf, L.F. Eastman and E. Kohn, IEEE Elec. Lett., 24 (6) 364-366 (March 1988).

13. "0.2 μm Gate-Length Atomic-Planar Doped Pseudomorphic $Al_{0.3}Ga_{0.7}As/In_{0.25}Ga_{0.75}As$ MODFET's with f_T over 120 GHz", L.D. Nguyen, D.C. Radulescu, P.J. Tasker, W.J. Schaff and L.F. Eastman, Elec. Dev. Lett. (July 1988).

14. "Fabrication and Characterization of Ultrashort Gate Length GaAs Field-Effect Transistors", R.C. Tiberio, E.D. Wolf, S.F. Anderson, W.J. Schaff, P.J. Tasker and L.F. Eastman, Proc. 31st Int. Symp. on Electron, Ion, and Photon Beams, J. Vac. Sci. Technol. B, 6 (1) 134-136 (Jan./Feb. 1988).

TASK 4 *ENSEMBLE MONTE CARLO SIMULATIONS OF III-V HETEROSTRUCTURE DEVICES*

Professor J.P. Krusius

OBJECTIVE

The objective of this task was to explore the physics of hot carrier transport in high speed devices made from graded ternary III-V compound semiconductors. Non-equilibrium carrier transport in position dependent heterostructures with imbedded hetero-interfaces, ballistic electron launching and collection, boundary interactions with open reservoirs and microwave cavities were to be examined using theoretical ensemble Monte Carlo simulation methods.

DISCUSSION OF STATE-OF-THE-ART

A number of important problems in carrier transport in small inhomogeneous compound semiconductor device structures can be identified. For unipolar devices these are transport in the boundary influenced domain, transport in materials with position dependent composition, and high energy injection and collection of carriers at heterointerfaces.

Carrier transport can in large devices be decoupled from boundaries because the mean free path of carriers is much larger than the characteristics geometrical dimensions. For small devices the distribution function is no longer only determined by lattice and carrier-carrier scattering processes but also significantly influenced by carrier exchange and interactions across boundaries. On the semiclassical scale within the effective mass approximation it is prudent to assume that carrier states are not altered by the presence of boundaries. It is thus sufficient to determine the characteristics of the media outside the device boundaries in the sense of the effective mass theorem and then allow for carrier interaction processes across each boundary according the the appropriate physical laws. This approach avoids the arbitrary postulation of boundary conditions for the distribution function [1] . In the semiclassical domain the most important boundary is the thermodynamically open boundary to external reservoirs. Similar considerations have shown to be necessary for the existence of meaningful solutions on the quantum mechanical scale when solving for the Wigner function in resonant tunneling [2].

Most high speed compound semiconductor device designs dependent on band gap engineering have a position dependent composition with imbedded heterojunctions. Compositional grading introduces compositional disorder in ternary and quarternary materials, typically on cation sites, changes electron states, and alters scattering rates.

Compositional grading is thus an important property, which has be considered in full detail in order to describe carrier dynamics and scattering processes properly. Transport in graded heterostructures with imbedded step heterojunctions has previously been studied within the drift and diffusions formulation [3]. Transport perpendicular to heterostructures with a step-wise constant composition has also been studied with ensemble Monte Carlo methods previously [4].

Saturated electron velocities in semiconductors are three orders of magnitude smaller than the phase velocity of electromagnetic fields propagating along metal lines. Because of this active regions in semiconductor devices have been aggressively scaled down in the past. Band gap engineering allows in addition to construct carrier injectors, which enhance velocities across active regions. The combination of a short active region and high energy injection of carriers has been successfully applied to the heterojunction bipolar transistor [5] and the tunneling hot electron transfer amplifier [6]. While the concept of using heterojunctions to launch ballistic electrons is physically simple in the single particle picture, carrier ensemble processes, such as current continuity and space charges, have not been considered in past studies.

PROGRESS

An effort to explore the carrier transport under high field conditions in unipolar, small size, inhomogeneous, high speed compound semiconductor device structures was started four years ago with JSEP support. The emphasis was to simultaneously include all the essential microscopic physics. The following results have been obtained during the fourth year of this task.

1. Transport Formulation

A new hot electron transport formulation for the self-consistent semi-classical ensemble Monte Carlo method suitable for graded compound semiconductor devices was developed during the three year period. Energy bands, phonon spectra, and scattering processes are treated position dependent. The **k.p** interpolation method is used to model the position dependent energy bands. Scattering rates are calculated using overlap integrals with proper symmetry characteristics. Ionized impurity scattering, based on Ridley's reformulation of the Brooks-Herring scattering matrix with collective effects and overlap integrals, is employed. Compositional cation disorder enters via alloy scattering. Degenerate statistics and freeze out for impurities, quantum mechanical reflection at interfaces, and contact resistances were also included. Device boundaries are open in the thermodynamic sense and allow the device to

interact with outside reservoirs postulated to be in thermodynamic equilibrium. Consequently we can now describe full carrier exchange processes at device contacts including, for example, transient states of the device violating charge neutrality and noise phenomena. The details of our transport formulation have been documented during the current reporting period (JSEP publications 4,1). During the fourth year we have examined the validity of this formulation. Perturbation theory has been used to derive a new expression for the critical minimum length scale (JSEP publication 2).

2. Algorithms and Software

The above transport formulation has been implemented in our self-consistent Monte Carlo computer code for one-dimensional ternary compound semiconductor devices (TCMC) during the three year period. New momentum and energy conserving algorithms have been developed in order to integrate the equations of motion of electrons with position dependent dynamics and over abrupt heterojunctions. The first and second generation versions of this code are running under FORTRAN on HARRIS 800 and DEC Microvaxll minicomputers respectively. The code had been calibrated against measured drift velocity-electric field distributions with and without overlap integrals (JSEP publication 2). A port to the Cornell production supercomputer (IBM 3090-600) has been completed during the fourth year (version 3.0).

The main emphasis in the software development during the fourth year was the coding, debugging, and testing of a two-dimensional implementation, called 2DTCMC, of our transport formulation. Version 1 of this code can accommodate up to ten different ternary compound semiconductor regions in a rectangular domain, either with constant or graded composition in one space direction and homogeneous in the orthogonal direction. Up to six contacts are permitted anywhere around the device periphery. Thermodynamically open boundaries to thermal reservoirs, reflective boundaries, and periodic boundaries have been implemented to model ohmic contacts, insulating regions, and cyclic conditions. Schottky contacts will be added later. Poisson's equation in the rectangular domain is solved using the Fourier analysis cyclic reduction algorithm POT4A employing the capacitance matrix (Beard and Hockney [7]). An efficient scheme for advancing particles in heterogeneous media was formulated and coded with the aid of MACSYMA. Scattering angles are calculated by sampling on overlap integrals and post-scattering components are calculated in full three dimensional fashion. An interface to the commercial 3D plotting package DISSPLA (Computer Associates) has been completed as well for graphics post processing of data with contour and surface capabilities. Extensive debugging and testing has been performed. Equilibrium limits, real space symmetry characteristics, and

velocity-field distributions have been verified.

3. Device Physics

Device-reservoir interactions have been studied in short one-dimensional GaAs resistors and ballistic $Al_xGa_{1-x}As$/ GaAs diodes in order to study the coupling between transport and device interfaces for open systems. The calculated distribution functions show strong non-Maxwellian boundary effects. Results have been published (JSEP publication 1).

A detailed study of one-dimensional thermionic ternary/binary heterojunction electron injectors of the generic $A_xB_{1-x}C$/DE type been completed. Space charge, cation grading, temperature and applied voltage effects on the injection process and the resulting self-consistent electron distribution function have been explored. Our results show that the simple injection concept based on a single particle picture is incorrect. It is crucial to incorporate space charges into the theory of small compound semiconductor structures. For example, the existence of flat band conditions at such heterojunctions depends on current continuity via a complicated injection/drift current ratio. Based on our self-consistent Monte Carlo results we have derived a simple model, which correctly predicts whether a particular heterojunction can be pulled into flat band using the applied voltage, temperature or materials parameters. The space charge state of a heterojunction can affect average downstream velocities by a factor as large as four. These results have been summarized in JSEP publications 5,4, and 2.

Injection of ballistic electrons from thermionic $Al_xGa_{1-x}As$/GaAs heterointerfaces into GaAs drift regions has been explored in order to establish the decay length and the ballistic electron fraction. The distribution function as a function of position has been calculated. Ballistic electron decay lengths of 250 and 150 nm have been found in GaAs for 77 and 300 K respectively. The width of the ballistic electron distribution is on the order of two optical phonon energies and carries up to 80 per cent of the electron passing the ballistic injector. These results are documented in JSEP publication 4.

Real time oscillations in Gunn diodes with heterojunction cathodes have been explored with our new formulation using time dependent large signal boundary conditions in collaboration with an experimental device fabrication effort in Prof. L. Eastman's group. Extensive simulations of conventional n^+-n-n^+ GaAs diodes and graded $Al_xGa_{1-x}As$/GaAs launcher diodes have been performed. Both types of diodes were simulated with an appropriate microwave cavity for various operating points typically with over 10^5 time steps of about 12 fs each and $2x10^4$ super-electrons. The launcher diodes were able to generate 21 mW of RF power in a frequency band centered at 69 GHz compared to 8.5 for the conventional diode. The

experimentally measured triplication of the power conversion efficiency was thus confirmed. A close examination of the simulation results, including the distribution function, shows that the power conversion enhancement results from the reduction of the dead zone at the cathode. Preliminary results have be presented at the 1987 Cornell Conference (JSEP publication (3). Further discussion of the results are given in the PhD thesis (see Degree Section) and in a forthcoming publication (JSEP publication 6).

SCIENTIFIC IMPACT OF RESEARCH

A thorough understanding of carrier transport in small inhomogeneous compound semiconductor heterostructure devices is crucial for high speed electronics. Of particular significance is the fact that transport studies focusing on complete devices must consider all significant elementary processes simultaneously. Correlations with measured data, which is available in abundance, then allows to assess the relative importance of the individual processes and the correctness of the associated models. This will not only provide quantitative guidance to heterostructure materials growth and device design but also allow to establish reliable limits for the underlying semiclassical transport formulation. We believe that we are now in this position for unipolar one-dimensional graded heterostructures with imbedded heterojunctions.

DEGREES

MS- None
A. Al-Omar, August 1988, Ph.D.
"Hot Electron Transport in Graded Ternary III-V Semiconductor Heterostructures".

REFERENCES

1. "Large Scale Computational Device Modeling", H.L. Grubin and J.P. Kreskovsky, edited by K. Hess, Coordinated Sciences Laboratory, University of Illinois, 1986, Urbana, Illinois.

2. "Transient Response of A Tunneling Device Obtained from the Wigner Function", R. Frensley, Phys. Rev. Lett. 57 (22) 2853-2856 (1986).

3. "Thermionic Emission-Diffusion Theory of Isotype Heterojunctions", R.J. Shuelke and M.S. Lundstrom, Solid State Elec., 27 (12) 1111-1116 (1984).

4. "Simulation of Near Ballistic Electron Transport in Submicron GaAs Diode with Al(x)Ga(1-x)As/GaAs Heterojunction Cathode", K. Tomizawa, Y. Awano, N. Nashizume and M. Kawashima, IEE Proc., Part I, 132, p. 37 (1985).

5. "GaAlAs-GaAs Ballistic Heterojunction Bipolar Transistor", D. Ankri and L.F. Eastman, Electron. Lett., 18, 750 (1982).

6. "Direct Observation of Ballistic Transport in GaAs", M. Heiblum, M. Nathan, D.C. Thomas and C.M. Knoedler, Phys. Rev. Lett., 55, 2200 (1985).

7. "POT4A- A Program for the Direct Solution of Poisson's Equation in Complex Geometries", S.J. Beard and R.W. Hockney, Computer Physics Communications, 36, 25-57 (1985).

JSEP PUBLICATIONS AND PRESENTATIONS

1. "Boundary Limited High Field Transport in Ultra Small Devices", A. Al-Omar and J.P. Krusius, in Fundamental Research on the Numerical Modelling of Semiconductor Devices and Processes, Edited by J.J.H. Miller, Boole Press, Dublin, 1987, pp. 3-9.

2. "Microscopic High Field Transport in Graded Heterostructures", A. Al-Omar and J.P. Krusius, Fifth International Conference on Hot Carriers in Semiconductors, 31(July 1987); Solid State Elec., 31 (3/4) 329-332 (1988).

3. "Space Charge Effects on Heterojunction Cathode (Al:Ga)As Gunn Oscillators", A. Al-Omar, J.P. Krusius, Z. Greenwald, D. Woodard, A.R. Calawa and L.F. Eastman, Proc. IEEE/Cornell Conf. on Advanced Concepts in High Speed Semiconductor Devices and Circuits, IEEE, New York, 365-372 (1987).

4. "Self-consistent Monte Carlo Study of High Field Carrier Transport in Graded Heterostructures", A. Al-Omar and J.P. Krusius, J. Appl. Phys., 62 (9) 3825-3835 (Nov. 1987).

5. "Conditions for Space-Charge Reversal at Thermionic Heterojunctions Designed for Ballistic Electron Injection", A. Al-Omar and J.P. Krusius, IEEE Elec. Dev. Lett., 9 (2) 81-83 (Feb. 1988).

6. "Analysis of of Heterojunction Launcher Gunn Diode Operation", A. Al-Omar and J.P. Krusius, manuscript in preparation, to be completed summer 1988.

TASK 5 *HIGH SPEED OPTICAL DEVICES*

Professor L.F. Eastman, Research Associate G. Wicks

OBJECTIVE

The objective of this research is to explore high speed optical devices based on band gap engineered MBE compound semiconductor materials including quantum wells. Integrable high speed modulators are in the center of the effort. The integration of a high speed modulator with a laser source is the ultimate goal.

DISCUSSION OF STATE-OF-THE-ART

Optical modulation techniques have been recently reviewed by Coldren et al. [1]. While many figures of merit can be defined, the drive power per bandwidth is frequently used. In the above article all recently published modulation techniques were analyzed and ranked according to this figure of merit. The quantum confined Stark effect (QCSE), the depletion edge translation (DET), and the Franz-Keldysh effect (F-K) were identified as leading optical modulation techniques. QCSE modulators achieve the highest bandwidth but simultaneously consume a lot of power. From the point of view of applications modulators should be compared for device dimensions resulting in an identical loading capacitance. Performing modulator designs according to this requirement, results in 0.2 V/GHz and 0.5 V/GHz figures of merit for the QCSE and FK modulators. An optimized DET modulator, which has not yet been fabricated, is projected to have a figure of merit of 0.4 V/GHz. All three modulators types can be integrated in the GaAs materials system.

PROGRESS

For the first time the quantum confined Stark effect (QCSE) has has been demonstrated in a waveguide structure. Ridge waveguides were fabricated in both as-grown and partially intermixed quantum well (QW) samples in the GaAs/AlGaAs materials system. The electric field dependent optical absorption was studied for light propagating parallel to the plane of the layers. This geometry is of interest both for studies of the fundamental physical behavior and for device applications. In the waveguide geometry, light can propagate with its electric field vector polarized either parallel or perpendicular to the plane of the QW layers. The latter polarization is inaccessible to light propagating perpendicular to the layers. The band to band transitions are predicted to be anistropic for the two different polarizations. In particular, the heavy hole exciton absorption vanishes for light polarized perpendicular to the layers, while the oscillator

strength increases for the single remaining light hole peak at higher photon energies. Furthermore, excitons in QW's undergo large shifts in energy when an electric field is applied perpendicular to the layers. This phenomena is known as the quantum confined Stark effect (QCSE). It has been experimentally shown in this task that both the absorptive polarization and the QCSE are preserved in the waveguide samples, in which the exciton peaks have first been permanently blue shifted up to 39.6 meV as a result of partial intermixing of the QW's. As a result the enhanced polarization sensitive electroabsorption can be utilized over a greatly expanded range of photon energies in a single epitaxially grown QW structure.

The transmission resonance technique has been utilized to calculate the expected shifting, broadening, and weakening of the exciton absorption peaks as function of the applied field. Good agreement has been obtained between the experimentally observed absorption spectra and the predicted behavior.

Waveguide structures in a GaAs/$Al_xGa_{1-x}As$ superlattice confi- guration have been grown using MBE. Intermixing was accomplished by a deposition of a thick layer of electron beam evaporated SiO_2 on the sample followed with rapid thermal annealing (RTA) in an Ar/H_2 ambient. RTA cycles at temperatures on the order of 985^o C and times of 15 to 30 s gave absorption edge shifts around 20 to 40 meV compared to as-grown material. Ridge waveguides were fabricated using established fabrication techniques. Typical devices had a length of 150 μm and a width of 26 μm. An Argon ion pumped Styryl 9M dye laser with a tunability range from 790 to 900 nm was used as the light source in the electroabsorption measurements. Typical laser power levels entering the waveguide were on the order of 10 MW. The resulting spectra constitute a dramatic demonstration of the QCSE. Even more impressive was the about 80 meV wide range through which exciton absorption could be tuned in a single structure.

The ability to continuously vary the effective band gap and still retain the exciton related absorptive and refractive properties of the QW structures has a variety of potential optical device applications. A large number of the applications of room temperature excitons should be accessible over greatly expanded photon energies using partial selective interdiffusion. Devices operating over a number of different energy ranges could, as a result, be integrated into a single epitaxial wafer, with immediate applications to wavelength division and multiplexing of optical signals.

One particularly important application is the integration of diode lasers and waveguide modulators. The QCSE facilitates the shifting of an abrupt absorption edge into a spectral region where the QW sample is normally transparent. These results are significant for device applications. The intermixing process is selective and compatible with most standard III-V semiconductor device fabrication processes. The resulting ability to integrate many

optoelectronic devices in a single chip, each capable of exhibiting QCSE and additional excitonic behavior over a different range of wavelengths, has a wealth of applications in optoelectronic integrated circuits.

SCIENTIFIC IMPACT OF RESEARCH

Quantum confined Stark effect (QCSE) based optical modulators in a waveguide structure have the potential to serve as an easily integrable modulator. Using intermixing the modulators can be made tunable, a feature which is necessary for matching to the light source. In addition, intermixing allows to realize integrated modulators operating at different wavelengths on the same substrate. The intermixing process should be extendable to other Ga containing III-V materials systems as well, which open up new applications. Hence the results obtained in this project are potentially of far reaching value for optoelectronic and integrated optic systems, for optical communication, optical signal processing, and optical computing.

DEGREES

J.D. Ralston, August 1988, Ph.D. Thesis

"Molecular Beam Epitaxial Growth, Selective Interdiffusion, and Room Temperature Exciton Electroabsorption of Gallium Arsenide/Aluminum Gallium Arsenide Quantum Well Waveguides"

REFERENCES

1. "Design of Optimized High Speed Depletion Edge Translation Optical Waveguide Modulators in III-V Semiconductors", L.A. Coldren, J.G. Mendoza-Alvarez and R.H. Yan, Appl. Phys. Lett., 51, 792-794 (1987).

JSEP PUBLICATIONS AND PRESENTATIONS

1. "Room Temperature Exciton Transitions in Partially Intermixed GaAs/AlGaAs Superlattices", J.D. Ralston, S. O'Brien, G.W. Wicks and L.F. Eastman, Inst. Phys. Conf. Series, 91, 521-524 (1988).

2. "Use of Raman Spectroscopy to Examine the Effects of Growth Stops in the Interface of Superlattices Grown by MBE", G.W. Wicks, J.T. Bradshaw and D.C. Radulescu, Appl. Phys. Lett., 52 (7) 570-572 (1988).

TASK 6 ***FEMTOSECOND STUDIES OF THE ULTRAFAST RELAXATION SEMICONDUCTORS***

Professor C.L. Tang

OBJECTIVE

The main objective of this program is to investigate the relaxation dynamics of hot carriers in III-V compounds and quantum wells. The results are important to the development of high speed electronic and optical devices which make use of hot electrons in semiconductors.

DISCUSSION OF STATE-OF-THE-ART

All current optical studies of the ultrafast relaxation dynamics of hot carriers in semiconductors are based on femtosecond Rh6G dye lasers operating in the visible at a wave length of approximately 620-630 nm. Thus, the initially excited states are generally near 2 eV above the top of the valence band.

Using the 2 eV photons, there are two basic approaches to the study of ultrafast relaxation dynamics of hot carriers in semiconductors. The monochromatic pump-and-probe or the related optical correlation spectroscopic techniques are limited to probing the dynamics of the nonequlibrium carriers in the initially excited states. Currently, the optical correlation spectroscopic technique for monitoring the initially excited state is a well developed and established technique. In the complementary polychromatic experiments, the optically accessible final states are probed. However, in many semiconductors, the carriers in the initially excited states can relax to final states not directly accessible optically. For example, in the case of GaAs and related compounds, the dominant relaxation channel within the first 100 femtoseconds (fs) is deformation potential scattering to the satellite valleys which are not accessible by direct optical transitions from the valence band. Thus, both types of experiments are needed. To expand the range of possible initial and final states that can be studied, there is a need for good tunable femtosecond sources beyond the 620-630 nm range. There is currently a great deal of effort on either developing different femtosecond laser sources at a wider range of wavelengths or finding new techniques that can give information on a wider range of final states for each excitation wavelength. We have made significant progresses during the past year in both respects.

PROGRESS

Nearly all the current results on ultrafast processes are derived from femtosecond

lasers in the visible or near infrared. There is a clear need to extend the wavelength range of femtosecond pulses into the uv. Recent success in our laboratory in growing and fabricating high quality ß-BaB_2O_4 crystal has enabled us to generate 43 fs pulses at 315 nm. The pulses generated in our experiment are, to our knowledge, the shortest ever in the uv spectral range at a high repetition rate (100 MHz) and high average power level (20 mW per arm of laser). It is the first report of a uv femtosecond laser with performance characteristics comparable to the Rh6G visible laser at 620 nm. This should lead to new physical studies by expanding the present spectral range of femtosecond laser sources. Also, the scheme we used to generate the uv femtosecond pulses can be generalized to the ir region as well. We are very hopeful that we will be able soon to extend the femtosecond optical techniques to throughout the near-uv, visible, and well into the ir spectral range.

We have also succeeded in applying the femtosecond up-conversion technique to the hot luminescence emitted by highly excited nonequilibrium carriers in GaAs and related compounds. This allows us to monitor all the states the carriers relax to in the central valley. An unprecedented time resolution for this type of experiments of around 40 fs is achieved in our experiment. Extensive data are being collected on GaAs and related compounds and structures.

So far, in both our correlation experiments and in the hot-luminescence up-conversion experiments, we have concentrated on undoped materials. We are now extending the studies to heavily doped samples.

SCIENTIFIC IMPACT OF RESEARCH

A clear understanding of the relaxation dynamics of hot carriers in GaAs and related compounds is of fundamental importance to the development of high speed electronic and opto-electronic devices. The experimental results are also much needed to complement the extensive theoretical studies that have been and are being carried out in various laboratories.

PUBLICATIONS AND PRESENTATIONS (* means primary JSEP support)

1. "Polarization Switching in Single-Frequency External-Cavity Semiconductor Lasers", T. Fujita, A. Schremer and C.L. Tang, Elec. Lett., 23, 803-804 (July 1987).

2. "Femtosecond Laser Studies of Ultrafast Processes in Semiconductors and Large Molecules", C.L. Tang, F.W. Wise and I. Walmsley, Invited, Special Issue on Femtosecond Lasers and Ultrashort Phenomena, Revue de Physique Applique, 22, 1695-1703 (Dec. 1987)

3.* "Picosecond Relaxation of Hot-Carrier Distributions in GaAs/GaAsP Strained-Layer Superlattices", D.C. Edelstein, A.J. Nozik and C.L. Tang, Appl. Phys. Lett., 51 (1) 48-50 (July 1987).

4.* "Application of Linear Prediction Least-Squares Fitting to Time-Resolved Optical Spectroscopy", F.W. Wise, R.J. Rosker, G.L. Millhauser and C.L. Tang, J. Quant. Elec., QE-23 (7) 1116-1121 (July 1987).

5.* "Experimental Determination of Hot-Carrier Scattering Processes in $Al_xGa_{1-x}As$", F.W. Wise, I.A. Walmsley and C.L. Tang, Appl. Phys. Lett., 51 (8) 605-607 (Aug. 1987).

6. "Femtosecond Relaxation Dynamics of Nonequilibrium Carriers in GaAs and Related Compounds", C.L. Tang, F.W. Wise and I.A. Walmsley, Proc. Fifth Int. Conf. on Hot Carriers in Semiconductors, Boston, MA (July 20-24, 1987); Solid State Elec., 31 (3/4) 439-442 (1988).

7. "Ensemble Monte Carlo Simulations of Femtosecond Energy Relaxation of Photoexcited Electrons in Bulk GaAs", D. Bailey, C. Stanton, M. Artaki, K. Hess, F. Wise and C.L. Tang, Proc. Fifth Int. Conf. on Hot Carriers in Semiconductors, Boston, MA (July 20-24, 1987).

8. "Materials for Nonlinear Optics", C.L. Tang, Invited, Proc. IUPAC Chemrawn VI, Tokyo, Japan (May 17-22, 1987).

9. "Bistability in Two-Mode Semiconductor Lasers via Gain Saturation", C.L. Tang, A. Schremer and T. Fujita, Appl. Phys. Lett., 51, 1392-1394 (Nov. 1987).

10. "Birefringence-Induced Polarization Counter-Rotation in a Semiconductor Laser", T. Fujita, A. Schremer and C.L. Tang, Appl. Phys. Lett., 51, 1487-1489 (Nov. 1987).

11. "Polarization Bistability in External-Cavity Semiconductor Lasers", T. Fujita, A. Schremer and C.L. Tang, Appl. Phys. Lett., 51, 392-394 (Aug. 1987).

12. "Simultaneous Formation of Solitons and Disperive Waves in a Femtosecond Ring Dye Laser", F.W. Wise, I.A. Walmsley and C.L. Tang, Optics Lett., 13, 129-131 (Feb. 1988).

13. "Single-Step Multi-Level Etching Technique for Monolithic Integrated Optics", W.J. Grande, W.D. Braddock, J.R. Shealy and C.L. Tang, Appl. Phys. Lett., 51 (26) (Dec. 1987).

14. "Measurement of Ultrashort Optical Pulses with Barium Meta-Borate", K. Cheng, W. Bosenberg, F. Wise, I. Walmsley and C.L. Tang, Appl. Phys. Lett., 52 (7) 519-521 (Feb. 1988).

15. "Semiconductor Laser Diode Logic Gate Suitable for Monolithic Integration", W.J. Grande and C.L. Tang, Appl. Phys. Lett., 51, 1780 (Nov. 1987).

16. "Electro-Optic Effect in Barium Metaborate", H. Nakatani, W. Bosenberg, K. Cheng and C.L. Tang, Appl. Phys. Lett., 52, 1288-1290 (April 1988).

17. "Instability Threshold Resonances in Directly Modulated External-Cavity Semiconductor Lasers", A. Schremer, T. Fujita, C.F. Lin and C.L. Tang, Appl. Phys. Lett., 52, 263-265 (Jan. 1988).

18. "Femtosecond Ultraviolet Pulse Generation in ß-BaB_2O_4", D.C. Edelstein, E.S. Wachman,

L.K. Cheng, W.R. Bosenberg and C.L. Tang, Appl. Phys. Lett. (June 1988).

19. "Growth and Characterization of Barium Metaborate", L.K. Cheng, W. Bosenberg and C.L. Tang, J. Crystal Growth (1988).

20. "Growth and Characterization of Nonlinear Optical Crystals Suitable for Frequency Conversion", L.K. Cheng, W.R. Bosenberg and C.L. Tang, Invited Review, Progress in Crystal Growth and Characterization.

21. "Broadly Tunable Optical Parametric Oscillation in ß-BaB_2O_4", L.K. Cheng, W.R. Bosenberg and C.L. Tang, Appl. Phys. Lett. (July 1988).

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