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FAULT MODEL DEVELOPMENT FOR FAULT TOLERANT VLSI DESIGN

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FAULT MODEL DEVELOPMENT FOR FAULT TOLERANT VLSI DESIGN

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Fault models provide systematic and precise representations of physical defects in microcircuits in a form suitable for simulation and test generation. The current difficulty in testing VLSI circuits can be attributed to the tremendous increase in design complexity and the inappropriateness of traditional stuck-at fault models. This report develops fault models for three different types of common defects that are not accurately represented by the stuck-at fault model. The faults examined in this report are: bridging faults, transistor stuck-open faults, and transient faults caused by alpha particle radiation. A genaralized fault model could not be developed for the three fault types. However, microcircuit behavior and fault detection strategies are described for the bridging, transistor stuck-open, and transient (alpha particle strike) faults. The results of this study can be applied to the simulation and analysis of faults in fault tolerant VLSI circuits.

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Evaluation

Fault models provide systematic and precise representations of physical defects in microcircuits in a form suitable for simulation and test generation. The objective of this effort was to develop fault models that could be used in the evaluation of fault tolerance in VLSI designs. The results of this effort provide the basis for more accurate and realistic evaluations of CMOS VLSI designs and for the development of more efficient fault detection strategies.

This report evaluates three common types of microcircuit faults that are not generally represented by the traditional stuck-at (zero and one) fault model. The three fault types examined were:

1. Bridging faults - "shorts" between input lines and "shorts" at the transistor level (e.g. gate-to-drain or drain-to-source shorts);
2. Transistor stuck-open faults; and
3. Transient faults caused by alpha particle radiation.

This report provides a rigorous transistor-level analysis of microcircuit behavior resulting from these faults. It is shown that transistor-level analysis was required to obtain accurate descriptions of faulted circuit behavior. A generalized fault model could not be developed because of the variability of the behavior produced by the faults. The faulted circuit behavior was strongly dependent upon the location and electrical characteristics of the fault and the structure of the logic adjacent to the fault site (i.e. logic stages preceding and following the faulted portion of the microcircuit). The analysis results can, however, be used to develop fault detection strategies. Several possible fault detection strategies are described in the report conclusions.

The results presented in this report substantiate that the objectives of the study have been met. Further, the study represents a significant step forward in the development of fault models and methods of fault detection in complex microcircuits. Future work can apply the results of this study to the design and analysis of fault tolerant VLSI circuits and the development of new fault tolerant design techniques.

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CONTENTS

SECTION 1

INTRODUCTION

Fault modelling is concerned with the systematic and precise representation of physical defects in a form suitable for simulation and test generation. This involves the representation of actual physical defects in terms of faults that produce approximately the same erroneous behavior.

The current difficulty of testing VLSI circuits can be attributed to the tremendous increase of chip complexity and the inappropriateness of the traditional stuck-at-fault models. With increased chip complexity, both test generation and test evaluation become very cumbersome, and in most cases computationally infeasible.

Both the suitability and effectiveness of the traditional fault model and associated testing techniques for contemporary VLSI technologies are unclear. Most of the existing testing methodologies and associated software tools were originally developed for testing printed-circuit boards containing TTL SSI/MSI components. Most of the traditional testing techniques share the following three characteristics[Hayes,1985]:

(i) Single-level or "flat"approach: Most of the existing techniques assume a logic gate level model.

Although MSI level macros are often used in logic simulators, most systematic test generation algorithms require a gate level representation.

(ii) Technology-independent fault model: Regardless of the technology used in the implementation, the logic line stuck-at-0/1 fault model is frequently used. In fact, the single line stuck-at fault model is the most widely used fault model.

(iii) Unranked fault list: The fault list used for test generation and fault simulation is usually unranked. In other words, the relative importance of different faults is not emphasized.

On the other hand, a true fault model should be straightforward, accurate and easy to use. Firstly, it should match the type of circuit (bipolar, nMOS, CMOS etc.) in which it is to be used. Secondly, the complexity of faults and the number to be considered should not entail excessive amounts of computation. Finally, a fault model should reflect the behavior of the underlying physical defects with sufficient accuracy for the intended applications. Unfortunately, these requirements are frequently at odds with one another.

A study [Hayes,1985] showed that more accuracy can be achieved at the lower electrical level but at the expense of more computation. On the other hand, physical failure modes such as excessive current leakage and threshold voltage shifts, which have fairly simple electrical models, are impossible to model directly in logical terms.

Shen et. al. [Shen,1985] conducted an experiment to study the effect of physical defects in MOS circuits. The circuit used in the study was a full adder cell of an array multiplier. The results showed that thirty percent of the significant physical defects manifested as bridging faults. Furthermore other fault types exhibited a lower percentage occurrence. This comes as no surprise as increased circuit density would increase the probability of bridging faults.

A class of permanent faults which does not conform to the traditional stuck-at fault model and hence needs to be studied at the transistor level is the transistor stuck-open or stuck-off fault.

Transient faults are non-recurring faults which are mainly caused by alpha particle radiation. Intermittent faults on the other hand are recurring faults that occur on a regular basis. Such faults may occur due to poor design or environmental conditions such as temperature, humidity, vibrations etc.

Detailed analysis of bridging faults, transistor stuck-open faults and transient faults caused by alpha particle radiation are presented in Sections 2,3 and 4 respectively.

During the course of the analysis, a LEVEL 2 SPICE model is used for simulating faulty circuits.

SECTION 2

BRIDGING FAULTS

A bridging fault in a digital circuit connects two or more conducting paths of the circuit. The resistance associated with this connection is denoted the "bridging resistance". These bridging faults may arise due to failure of insulation between adjacent layers of metallization on a chip, or they can be due to a connection between two conductors in the same layer, which could be a result of the improper masking or the etching.

Most of the work done in relation to bridging faults have two major drawbacks. Firstly, most researchers [Kodandapani,1980], [Karpovsky,1980] have assumed a wired-AND (for positive logic) or wired-OR (for negative logic) short which is true of TTL type circuits. For CMOS this is not true as this report will clearly show. Secondly, most of the work has been done for gate-level fault simulation and hence the papers by Mei and Friedman [Mei,1974], [Friedman,1974] restrict their discussion to input and output bridging faults. As shown by Malaiya et.al. [Malaiya,1986] a gate level representation of bridging faults is inadequate for a complete analysis of these faults.

Unlike the approach used in most of the existing literature this report studies bridging faults in CMOS circuits at the transistor level. It has been shown that bridging faults at transistor level are technology dependent and become important as the transistor dimensions are reduced [Banerjee,1985], [Rajsuman,1987]. The sheer complexity of shorted faults at transistor level make a complete study infeasible. Hence, a few practical assumptions are made at the onset. This study will restrict itself to single bridging faults as opposed to multiple ones. Also, it is assumed that not more than two "lines" or conducting paths are shorted.

In order to analyze the possible bridging faults and their effects, the 3-input NOR gate shown in Figure 1(a) is chosen as a test circuit.

The first important thing to be noted is that the kind of bridging faults to be considered is dependent on the layout of the circuit. This is because the layout determines the possible points where the most probable shorts may occur.

Certain layout guidelines must be established if we are to generalize the results obtained from a test circuit to other circuits. If not, then different layout schemes would give rise to different potential "shorts" and hence development of any general model is difficult.

The layout strategy adopted is that described by Uehara et.al. [Uehara,1981]. It should be noted that this algorithm was chosen not because it minimizes the number of bridging

faults but because of the ease with which the layout principles can be automated. This implies a high degree of layout simplicity for different circuits and this is indeed what is to be exploited if any bridging fault model is to be developed.

According to Uehara's algorithm the CMOS circuit is converted to a graph where:

(1) the vertices in the graph are the source/drain connections, and

(2) the edges in the graph are transistors that connect particular source-drain vertices.

Two graphs, one for the n-logic tree and one for the p-logic tree result. Figure 1(b) shows the graph transformation for the 3-input NOR gate. The edges for the p-graph i.e. the graph corresponding to the p-logic structure, are shown as solid lines while those for the n-graph are shown as broken lines. The vertices of the p-graph are identified by circles while those for the n-graph by crosses. The connection of edges in the graphs mirror the series-parallel connection of the transistors in the circuits. Each edge is named with the gate signal name for that particular transistor. Thus, for instance, the p-graph has four vertices representing Z, I_2, I_1 and V_{dd} and three edges, representing three transistors in the p-logic structure. Furthermore, if there exists a sequence of edges (containing all edges) in the p-graph and n-graph that have identical labeling, then the circuit layout may be designed with no breaks. This path is known as the Euler path. The main

points of the algorithm are as follows:

(i) Find all Euler paths that cover the graph.

(ii) Find a p- and n- Euler path that have identical labeling (a labeling is an ordering of the gate labels on each vertex).

(iii) If (ii) is not found, then break the gate in the minimum number of places to achieve (ii) by separate Euler paths.

The sequence of gate signal labels in the Euler path corresponding to Figure 1(b) is (A,B,C) and is shown in Figure 1(c). Note that the graph for the n- and p-graph allow this labeling. To complete a layout the transistors are arranged in the ordering of the labeling, n- and p-transistors in parallel rows, as shown in Figure 2. Vertical polysilicon lines complete the gate connections. Metal routing wires complete the layout.

We now enumerate the most probable bridging faults for the layout shown in Figure 2.

(i) Input bridging faults which are a result of input lines getting connected together. For instance the polysilicon layers corresponding to inputs A and B may get shorted.

(ii) Faults caused by points in the circuit getting connected to either the V_{DD} or V_{SS} lines.

(iii) Crossover faults which result from connections between different mask levels.

Points on the layout which are prone to crossover "shorts" have been numbered. According to the kind of faults

they produce the different numbers have been grouped together. Figures 3 through 6 describe the different fault groups. It has been shown [Soden,1986] that electrostatic discharge shorts are more likely to occur at the edges. Hence gate to source or gate to drain shorts are more probable than drain to source faults. Accordingly the latter category has not been considered in Figures 3 through 6.

The faults described thus far are obviously not all the possible bridging faults. However, for the layout described, these would be the most probable bridging faults.

In order to show how different layouts affect the class of most probable bridging faults, an alternate layout given in Figure 7 is considered for the same 3-input NOR circuit. As far as specific faults are concerned the only additional fault is output stuck-at-A because of short at point 12 as shown. But the more important problem related to this layout is the fact that the possibility of the fault output stuck-at-zero due to some short is much higher than the previous case. This is because the output metallization overlaps the n-diffusion over a significant portion. Thus, it turns out that the layout chosen on the basis of easy automation is also efficient in terms of decreasing the possibility of bridging faults for this example.

The discussion so far has been restricted to the physical location of bridging faults and generalization rules to do so for any circuit. It is now important to analyze the effects of the bridging faults.

We remark here that faults caused by a point in the

circuit getting connected to V_{DD} or V_{SS} lines, if detectable, can be modelled as the point stuck-at-one or stuck-at-zero. Thus such faults will not be analyzed any further.

A detailed analysis of input bridging faults is presented in Section 2(a).

We note here that the only other category of bridging faults that need further analysis are those caused by shorts between either the gate and source or gate and drain of a transistor. We denote them as "Transistor Bridging Faults" and analyze them in Section 2(b).

It should be noted that for very large values of bridging resistance we would expect any bridging fault to be masked because the limiting case of infinite bridging resistance corresponds to the fault free circuit.

SECTION 2(a)

INPUT BRIDGING FAULTS

Most of the existing literature on input bridging faults is based on the assumption that such faults introduce WIRED-ANDing or WIRED-ORing of the input lines that are shorted [Breuer,1976]. All subsequent test models or test generation schemes are developed within the framework of this basic assumption.

This section examines the validity of such an assumption for CMOS circuits by a more careful examination and subsequent computer simulation of the physical faults.

To understand the effect of an input bridging fault we first note that for a fault free CMOS circuit there is no direct path or connection from V_{DD} to V_{SS}. A short between any two input nodes in the circuit can change this condition and cause the circuit to produce incorrect results when the two shorted inputs are supposed to have different logic values in the fault free circuit. The key to understanding the effect of an input bridging fault is thus to examine the path, between V_{DD} and V_{SS}, created by the fault. In case of bridging fault, most of the previous work in this topic assumed that one logic value is "stronger" than the other, and hence the former dominates over the latter.

This led to the concept of WIRED-AND (where "0" is the

dominant logic) and WIRED-OR (where "1" is the dominant logic), of which the former is more frequently used in analysis. While this may be true in the case of TTL circuits, the case for CMOS is entirely different for reasons outlined before.

Our initial studies first revealed that the structure of the circuits driving the two input nodes which have a short between them are crucial in determining the effect of the short. This is shown in Figure 8(a) where the output of the two inverters drive a NOR gate whose inputs are shorted. Simulation results show that the short behaves like a WIRED-AND and the corresponding NOR output is logic HIGH. By changing one inverter to a 3-input NAND gate we notice that for input conditions shown in Figure 8(b) the same bridging fault now behaves like a WIRED-OR and the NOR output is logic LOW. Simulation results exhibit a further variation of the structural dependence of the driving gates. For the circuit of Figure 9, if one input of the NAND gate is logic LOW the bridge behaves like a WIRED-AND whereas if two or all inputs are logic LOW then the bridge behaves like a WIRED-OR.

An input bridging fault causes a path from V_{DD} to V_{SS} via the P-network of one circuit and N-network of another circuit (see Figure 10). Hence voltages V_X and V_Y depend on the effective resistance of the path. For small values of R, $V_X$and V_Y are nearly the same and depend on the ratio of the resistance of the path in the P-network to that of the path in the N-network. This is why the same fault can give

different results (namely WIRED-AND or WIRED-OR) depending on the path in question, which in turn depends on the inputs to the previous circuits.

Typically the ON resistance of a p-transistor is 2 to 2.5 times that of an n-transistor because of the corresponding ratio between electron and hole mobilities. Also fully complementary CMOS circuits are usually ratio-less because under normal operating conditions there is no path from V_{DD} to V_{SS} and voltage outputs do not depend on the p and n- resistances. Now it can be clearly seen why the fault in Figure 8(a) caused a WIRED-OR behavior. In Figure 11(a) we see the conduction path through R from V_{DD} to V_{SS} consists of one p-transistor (T_{P1}) and one n-transistor (T_{N2}).

$$\text{Thus } V_1 = \left[\frac{R + R_N}{R + R_N + R_P}\right] V_{DD}$$

where R_N = ON resistance of n-transistor

and R_P = ON resistance of p-transistor

If $R_N, R_P \gg R$, then V_1 and V_2 are approximately equal to

$$V_{DD}\left[\frac{R_N}{R_N + R_P}\right].$$

Since $R_P > 2R_N$, V_1 and V_2 are both less than $V_{DD}/3$ which is LOGIC LOW.

On the other hand Figure 11(b) demonstrates the reason why Figure 8(b) exhibited WIRED-OR behavior. In this case, V_1

and V_2 are approximately equal to $V_{DD}\left[\frac{3R_N}{3R_N + R_P}\right]$ which is LOGIC HIGH.

The equations used so far are approximate and can only be used to deduce whether outputs are logic LOW or HIGH. For instance, in Figure 11(b) because of body effect (for two of the n-transistors the source to body voltage is non zero) the resistances of all three n-transistors are different, although we have used the same value R_N. However, the equations can be used to determine logic levels.

Figure 12(a), 12(b), 12(c) show only the conducting transistors for Figure 9(a), 9(b), 9(c) respectively. It is now apparent, in light of the discussion before, the cause of WIRED-AND in Figure 9(a) and WIRED-OR in Figure 9(b) and 9(c). The situation in Figure 12(a) is identical to that in Figure 11(a) whereas in Figure 12(b) and Figure 12(c) multiple p-transistors in parallel cause the effective resistance of the pull-up circuit to be lower than that in Figure 12(a), thereby raising the voltage level at the short. An exact analysis would depend on the physical parameters of the devices in question.

EFFECT OF INPUT BRIDGING FAULTS ON TEST SETS

In this section we examine the validity of test sequences derived on the basis of the WIRED-AND and WIRED-OR models. Most of the previous work done on this subject made use of one of the two models to derive tests. However, as pointed out before, fault simulation using various circuits showed that depending on the input pattern, both these effects (OR-ing and AND-ing) can be present in the same circuit and that no single model can be used to develop test sets.

We present here two examples to illustrate the invalidity of both the models.

Figure 13 shows two 3-input NAND gates driving a 2-input NOR gate. The bridging fault is present at the input of the NOR gate. The accompanying table shows a set of seven tests used to detect all single and multiple stuck-at-faults[Berger,1973],[Hartmann,1984]. If the WIRED-AND model is used this test set would detect the bridging fault but simulation result shows that it does not.

For the bridging fault to be detected the output of one NAND gate must be logic low while that of the other must be logic high. The former condition implies that there are exactly three n-transistors in series in the pull-down part of the conduction path formed due to the bridge. The latter condition implies that the maximum resistance of the pull-up part of the conduction path due to the bridge is that of one

p-transistor. Thus for small values of R (typically a few ohms) the ratio of the equivalent p and n resistances will always result in a logic high input to the NOR gate and hence this fault cannot be detected.

Analogously the circuit of Figure 14 serves to invalidate the WIRED-OR model because the fault is undetectable for small values of R.

Thus we conclude that the effect of input bridging faults depend not only on the structure of the circuits driving the input nodes which are bridged but also the input pattern to these driving circuits. Hence both these factors have to be taken into account while deriving test sets for input bridging faults.

SECTION 2(b)

TRANSISTOR BRIDGING FAULTS

All possible cases of transistor bridging faults are enumerated with the help of the tree diagram shown in Figure 15. Before analysing each of the cases we would like to emphasize a few points. The entire analysis has been done for fully complementary CMOS logic only. Thus every transistor in the p-FET part would have a corresponding one in the n-FET part and vice versa. It is convenient during the course of analysis to lump a group of transistors together, replace it by a block, and label it with the subscript p or n depending on the kind of transistors involved. For example A_p or B_{2p} could refer to a group of p transistors. It should be noted that each block does not represent an arbitrary collection of transistors but rather a subcircuit which has exactly two nodes for connection to transistors not in this subcircuit. We will frequently use the term "closed path" in a block to represent the situation where the inputs to the transistors in the block are such that there exists at least one path of conducting transistors between the two nodes of the block. In the case that there is indeed a "closed path" as defined above then associated with each block is a resistance, for example, r_{Ap} (for block A_p). It is important to note that this resistance

is not a constant but a function of various factors. Among these factors are the number of conducting transistors in the block and the location and size of the bridging fault present in the circuit.

Continuing on the topic of notation, the potential of any node labelled X with respect to the reference (V_{ss} in our case) will be termed V_X.

Only the steady state analysis has been done for the bridging faults. The only time aspect that has been dealt with is the amount of time required for the faulty circuit to reach steady state vis a vis the normal circuit. Also in calculating currents, the gate currents of the transistor have been ignored because they are usually several orders of magnitude smaller than drain currents.

To make the analysis less complex we have not considered any case where there is fanout from the nodes which are shorted by the bridging fault.

CASE I

The most general structure of Case I is shown in Figure 16.

We first show that any input pattern P that detects this fault must create a closed path in A_p and B_p. Assume that there is no closed path in B_p. This implies that there is a closed path from the output Z to V_{ss} through B_N. Since there is no charging path for Z, the output for the faulty

circuit is identical to that of the normal circuit. Now assume that there is no closed path in A_p. As before, this would imply a closed path from Z to V_{SS}, now through A_N. T_P cannot conduct and charge Z under these circumstances. If it did, there would be current flow in resistor R from the gate to source of transistor T_P. This would imply that V_{GS} of T_P is positive which in turn would imply that T_P is off. As before, the output of the faulty circuit would be identical to that of the normal circuit. Thus an input pattern that detects this fault must create a closed path in A_P and B_P. Therefore for Case I we will henceforth assume that the input pattern P satisfies these conditions. The resulting equivalent circuit is shown in Figure 17.

The fault could manifest itself differently depending on whether the output of the gate driving input X is high or low. We now consider these cases separately.

(i)In this case the input pattern P is such that the output of the gate driving X is high. The resulting equivalent circuit is given in Figure 18. We will show by contradiction that T_p cannot conduct. Assume T_p conducts ; then I_1 cannot be zero. Because if I_1 is equal to zero then V_X is V_{DD} and hence T_p is off which contradicts the assumption that T_p conducts. Since V_X cannot be greater than V_{DD} , I_1 not equal to zero implies current flow from X to W. Since Y cannot be the source of T_p hence $V_X - V_W$, the gate to source voltage of T_p, is positive and hence T_p is off. This contradicts the assumption that T_p conducts. Thus T_p is off, $I_1 = 0$, V_X is

high and the voltage V_Z is low, which is the output of the normal circuit. Thus P is not a test for this fault for any value of R.

(ii) In this case the input pattern P is such that the output of the gate driving X is low. The resulting equivalent circuit is given in Figure 19. It can be shown that

$$V_X = \left[\frac{r_{In}\, V_{DD}}{r_{Ap}\left(\frac{R + r_{In}}{r_{Tp} + r_{Bp} + r_{Tn}}\right) + r_{Ap} + R + r_{In}} \right]$$

$$V_W - V_X = \left[\frac{R\, V_{DD}}{r_{Ap}\left(\frac{R + r_{In}}{r_{Tp} + r_{Bp} + r_{Tn}}\right) + r_{Ap} + R + r_{In}} \right]$$

and

$$I_1 = \left[\frac{V_{DD}}{r_{Ap}\left(\frac{R + r_{In}}{r_{Tp} + r_{Bp} + r_{Tn}}\right) + r_{Ap} + R + r_{In}} \right]$$

Since $r_{Ap}\left(\frac{R + r_{In}}{r_{Tp} + r_{Bp} + r_{Tn}}\right) + r_{Ap} + r_{In} > 0$,

for sufficiently large values of R, I_1 is a decreasing function of R. Since r_{In} is the effective resistance of conducting transistors and cannot grow unbounded, V_X ($= I_1 r_{In}$) decreases with increasing R. Thus for sufficiently large values of R, $V_X = 0$. Thus T_N will be off and T_P will conduct, charging Z to a logic high. Hence the input P will not detect the fault.

Since $\left(\frac{R + r_{In.}}{r_{Tp} + r_{Bp} + r_{TN}}\right) r_{Ap} + r_{Ap} + r_{IN} > 0$,

for small values of R, $V_W - V_X$ is an increasing function of R. So for sufficiently small values of R, $V_W - V_X < V_{Tp}$, where V_{Tp} is the threshold voltage of transistor T_p. So transistor T_p is off and Z cannot be charged. So V_Z will be at logic low and P will detect the fault.

For this case we conclude that there exists an R_h such that the input P is not a test for $R > R_h$ and P detects the fault for $R < R_h$. We note that P is also a test for input X stuck-at-one. It should be noted that for values of R close to R_h it is difficult to predict the behavior of the circuit because V_Z might be in the transition region between logic high and low.

CASE II

The most general structure for Case II is shown in Figure 20. Using the same argument as in Case I it can be shown that any input P which detects this fault must create a closed path in B_p. However, unlike Case I we may obtain an input pattern which does not create a path in A_p but is a test for this fault. Thus for Case II we will henceforth assume that the input pattern P creates a closed path in B_p. We now analyze several different situations.

(a) There exists a closed path in A_p.

(a)(i) In this case the input pattern P is such that it creates a closed path in A_p and causes the output of the gate driving X to be low. The equivalent circuit is shown in Figure 21. We first show by contradiction that the transistor T_p must conduct. Assume T_p does not conduct. Thus all currents are zero and hence $V_X = 0$ and $V_W = V_{DD}$. This implies T_p conducts, which is a contradiction. It can be shown that

$$I_1 = \frac{V_{DD}}{\left[\frac{(r_{Ap} + r_{Tp})(R + r_{In})}{(r_{Bp} + r_{Tn})} + r_{Ap} + r_{Tp} + r_{In} + R \right]}$$

Since $\frac{(r_{Ap} + r_{Tp})(R + r_{In})}{(r_{Bp} + r_{Tn})} + r_{Ap} + r_{Tp} + r_{In} > 0$

for sufficiently large values of R, I_1 is a decreasing function of R. Since r_{In} is the effective resistance of conducting transistors, it cannot grow unbounded, V_X ($= I_1 r_{In}$) decreases with increasing R. Thus for sufficiently large values of R, V_X approaches 0. Thus T_N will be off and T_p will conduct, charging Z to a logic high. Hence input P will not detect the fault.

We now show that for any given circuit the input P satisfying the conditions of Case II a(i) is always a test for sufficiently small values of R.

We first investigate whether this fault can be detected by the input pattern P when $R = 0$. If P were not to detect

the fault then V_Z must be logic high. So we investigate the conditions under which V_Z attains a maximum value under the condition R = 0. We would expect this to happen when $r_{Ap} = r_{Bp} = 0$ because then V_Z would differ from V_{DD} by only the V_{DS} drop across T_p. Simulation results confirm this reasoning. The equivalent circuit with $r_{Ap} = r_{Bp} = R = 0$ is shown in Figure 22.

Simulation results show that as I_1 is decreased by increasing the value of r_{in}, V_Z asymptotically rises to a value which is still logic low. Thus there always exists sufficiently small values of R for which the input P is a test.

For this case we conclude that there exists an R_h such that the input P is not a test for $R > R_h$ and P detects the fault for $R < R_h$. We note that P is also a test for input X stuck-at-one.

(a)(ii) In this case the input pattern P is such that it creates a closed path in A_p and causes the output of the gate driving X to be high. The equivalent circuit is shown in Figure 23. We first show by contradiction that T_N must conduct. If we assume that T_N does not conduct, then all currents are zero and hence $V_X = V_{DD}$. This implies T_N conducts, which is a contradiction.

It can be shown that

$$I_1 = \frac{V_{DD}}{\left[r_{Ip} + R + r_{Bp} + r_{Tn} + \frac{(r_{Bp} + r_{Tn})}{(r_{Ap} + r_{Tp})} (r_{Ip} + R) \right]}$$

Since $r_{Ip} + r_{Bp} + r_{Tn} + \frac{(r_{Bp} + r_{Tn})(r_{Ip} + R)}{(r_{Ap} + r_{Tp})} > 0$

for sufficiently large values of R, I_1 is a decreasing function of R. Hence V_X increases with increasing R and for sufficiently large values of R, V_X is approximately V_{DD}. Thus T_p will be off and T_N will discharge V_Z to a logic low. Hence the input pattern P will not detect the fault.

If R decreases, we expect the current I_1 to increase. So V_X decreases causing r_{Tn} to increase and r_{Tp} to decrease. Thus it is not clear what happens to V_Z because of the conflicting changes in R and r_{Tn}. Simulation results show that there are circuits for which the fault is masked for all values of R. On the other hand, there are circuits for which the fault can be detected for small values of R. The circuits for which this fault can be detected are those for which r_{Bp} is extremely small. Figure 24(a) shows a circuit for which the fault is not detected by P for any values of R whereas Figure 24(b) shows a circuit for which P is detects the fault for small values of R.

For this case we conclude that there are circuits for which the input pattern P is not a test irrespective of the value of R. On the other hand, there are circuits for which P is a test provided R is very small. Note that P is also a test for the input X stuck-at-zero.

(b) There is no closed path in A_p.

(b)(i) In this case the input pattern P is such that it causes the output of the gate driving X to be low. The equivalent circuit is shown in Figure 25. In this case V_Z is always going to be low because there is no path to charge the output. Thus P is not a test for this fault.

(b)(ii) In this case the input pattern P is such that it causes the output of the gate driving X to be high. The equivalent circuit is shown in Figure 26.

Suppose an input pattern P_b, satisfying the conditions of Case II (b) (ii), is a test for this fault. We will show that there exists an input pattern P_a, satisfying the conditions of Case II (a) (ii), which is also a test for this fault. We construct P_a from P_b by changing only those inputs in P_b which will create a closed path in A_p. Thus when P_a is applied the equivalent circuit is the same as in Figure 23. If P_b is a test then V_Z is logic high in Figure 26. If we now consider Figure 23, we expect that input P_a will cause V_Z to be higher than in Figure 26 because of the presence of a pull up path via T_p and r_{Ap} and the absence of the pull down path through r_{AN} which is present in Figure 26. Thus we expect V_Z in Figure 23 to be logic high also. Thus P_a is also a test for the fault. Simulation results have confirmed this reasoning. Recall here that P_a is a test for X stuck-at-zero.

In the following two cases there is a path to charge V_Z

which does not include the faulty transistor T_p. Thus we must consider the value of V_Z when P is applied. There is a charging or discharging time constant associated with the load capacitance at the gate output Z. Due to the bridging fault this time constant may increase to a value higher than that of the normal circuit. In such a situation, depending on the clock rate, the output of the circuit may not reach its steady state value within one clock cycle. Thus it is possible that the input pattern P may or may not detect the fault depending on the value of V_Z prior to P being applied. However, if the time constant associated with the faulty circuit does not exceed that of the normal circuit then it is not necessary to consider the value of V_Z prior to P being applied in order to determine whether P is a test for the fault.

CASE III

The most general circuit for this case is shown in Figure 27. By using an argument similar to that in Case I we can show that any input pattern that detects this fault must create a closed path in B_{2p}. We now have to investigate different cases where the fault may possibly affect the output.

Let us consider the case where the input P is such that there exists no closed path in A_{1p}. If the output of the gate driving X is low, then there is no charging path for V_Z but V_Z can discharge to its normally logic low value through A_{1n}. Thus the fault cannot be detected by any input pattern P which satisfies the above conditions. So we only have to consider input patterns P which make the output of the gate driving X high. In this case we first show that T_p cannot conduct. Since V_Z can be at most V_{DD} when P is applied, then if T_p conducts then W must be the source and Y must be the drain. But that would imply that V_{GS} of T_p is positive because $V_X > V_W$. Hence T_p does not conduct. P can be a test only if there is a charging path for V_Z through A_{2p} and C_p. The equivalent circuit is shown in Figure 28. Thus V_Z stabilizes at

$$V_Z = \left[\frac{r_{A1n} \cdot V_{DD}}{r_{A1n} + r_{B2p} + r_{Cp} + r_{A2p} + R + r_{1p}}\right]$$

with a time constant never exceeding that of the normal

circuit. Thus V_Z can be a logic high depending on the structure of the circuit. For large values of R, V_Z will be logic low and the fault cannot be detected. However, for small values of R, depending on the structure of the circuit, P may be a test for this fault.

We now consider the case when the input P is such that there exists a closed path in A_{1p}. To study the influence of the fault we must investigate several cases.

(a) We first look at the situation when input P creates a closed path in C_p. Hence there is a charging path for the output V_Z which in the normal circuit will be logic high. If P is such that the output of the gate driving X is high, then there is no discharging path for V_Z and P cannot detect the fault. So for the rest of this case we assume that P is such that the output of the gate driving X is low. Furthermore, for V_Z to have a discharging path P must be such that there exists a closed path in either A_{2p} or B_{1p}.

(a) (i) P is such that there is a closed path in A_{2p} and no closed path in B_{1p}. The equivalent circuit for this case is shown in Figure 29. In this case V_Z will stabilize at

$$V_Z = V_{DD} \cdot \left[\frac{1}{1 + \left(\frac{r_{A1p}}{r_{A2p} + r_{In} + R} \right)} \right]$$

with a time constant which never exceeds that of the fault free circuit. Thus for large values of R, V_Z is almost V_{DD} and P does not detect the fault. On the other hand, for

small values of R, V_Z given by the above equation, can be logic low depending on the structure of the circuit. Hence there are circuits for which this P is a test for the fault. An example of such a circuit is shown in Figure 30 where P = ABCDEFG = 0011000 is a test.

(a) (ii) P is such that there is a closed path in B_{1p} and no closed path in A_{2p}. The equivalent circuit for this case is shown in Figure 31. In this case V_Z will stabilize at

$$V_Z = V_{DD} \cdot \left[\frac{1}{1 + \frac{(r_{Cp} + r_{A1p})}{r_{B1p} + r_{Tp} + R + r_{In}}} \right]$$

with a time constant that never exceeds that of the fault free circuit. For large values of R, V_Z is almost V_{DD} and P does not detect the fault.

We now inspect this case when R = 0. For P to detect this fault V_Z as given by the above equation should stabilize at logic low. We expect this to happen when the voltage drops across r_{B1p} and r_{In} is as small as possible and that across r_{A1p} and r_{Cp} as large as possible. Simulation results confirm this line of reasoning. Figure 32 shows a circuit where P is a test for this fault.

(a) (iii) P is such that there is a closed path in B_{1p} and a closed path in A_{2p}. The equivalent circuit for this case is shown in Figure 33. In this case V_Z will stabilize at

$$V_Z = V_{DD} \cdot \left[\frac{1}{1 + \dfrac{r_{A1p} + \dfrac{r_{Cp} \cdot r_{A2p}}{r_{Cp} + r_{A2p} + r_{Tp} + r_{B1p}}}{R + r_{In} + \dfrac{r_{A2p} \cdot (r_{Tp} + r_{B1p})}{r_{A2p} + r_{Tp} + r_{B1p} + r_{Cp}}}} \right]$$

with a time constant never exceeding that of the fault-free circuit. For large values of R, V_Z is almost V_{DD} and P does not detect the fault. Note that V_Z here is always less than the stable V_Z value given in Case III a(i). So if the P corresponding to Case III (a) (i) detects the fault then there exists some input pattern P satisfying the conditions of Case III (a) (iii) which also detects the fault.

(b) We now investigate the situation when the input P is such that there is no closed path in C_p. It is easily shown that for P to detect the fault it must create a closed path in B_{1p}. Moreover, if P is such that the output of the gate driving X is high, then it can be shown that T_p will be off and V_Z will be logic low. Thus this P will not detect the fault. Hence for the rest of this case we consider input pattern P such that the output of the gate driving X is low. The equivalent circuit is shown in Figure 34.

We now investigate the following cases separately:

(b) (i) The input P is such that in addition to the conditions specified in case III (b) it also creates a closed path in A_{2p}. The equivalent circuit is shown in Figure 35.

If V_Z is low prior to P being applied, the analysis is very similar to that in Case I (ii). So in this case there

is a resistance value R_{h0} such that the input P will detect the fault only if $R < R_{h0}$.

Now we analyze the case when V_Z is high prior to P being applied. Similar to the previous case, for large values of R the current through R is going to be negligible and the circuit will behave as normal and thus P will not detect the fault. Now consider small values of R. Decreasing R will increase the current in r_{IN} thereby increasing the voltage V_X which may push T_N into conduction. This would provide a discharge path for the load capacitance in V_Z. There may also exist another discharge path through T_p which may conduct in saturation with Y as the source and W as the drain. So depending on the circuit parameters for small values of R, V_Z may discharge to a logic low. Thus P may detect the fault even if V_Z is logic high prior to P being applied. So in this case there is a resistance value R_{h1} such that the input P would detect the fault if and only if $R < R_{h1}$.

Let us define P(L) to be the input pattern P such that V_Z is low prior to P being applied and P(H) to be the input pattern P such that V_Z is high prior to P being applied. We emphasize here that P(H) = P(L) but their effects may be different because the initial condition of V_Z is involved. We now proceed to show that if P(H) detects the faults, then P(L) will also detect the fault. In other words R_{h1} is never greater than R_{h0}. Assume that P(H) detects the fault but P(L) does not for a given value of R. Under this assumption consider the situation when P(L) is applied. Since P(L) is

not a test we expect V_Z to reach a logic high. But this is equivalent to P(H) being applied and hence V_Z will discharge to a logic low proving that P(L) is also a test, which is a contradiction. So we may have values of R such that $R_{th1} < R < R_{th0}$ where P(L) is a test but P(H) is not. Thus we may have bridging faults which exhibit sequential behavior. That is, a test set may or may not detect this fault depending on the sequence in which the test patterns are applied. An example where this sequential behavior is seen is given in Figure 36. Here SEQUENCE 1 does not detect the fault but SEQUENCE 2 does. Note that both SEQUENCE 1 SEQUENCE 2 are minimal test sets that detect all single stuck-at faults for the gate level representation of the circuit which is shown in the figure [Berger,1973], [Lala,1985]. Thus if the fault is detectable it will be detected by a test for T_P stuck-open.

(b) (ii) We now consider the situation where the input P satisfies the conditions of Case III (b) and also does not create a closed path in A_{2P}. The equivalent circuit is shown in Figure 37. There always exists a discharge path for V_Z through A_{2N} and C_N but there is no charging path. Thus V_Z is always logic low and P is never a test for this fault.

CASE IV

The most general structure of Case IV is shown in Figure 38. As before we can show that any input pattern that detects the fault must create a closed path in B_{2D}. We

now investigate different cases separately.

(a) P is such that it creates a closed path in A_{1p}.

(a)(i) Moreover if P is such that it does not create a closed path in B_{1p} then T_p can conduct only if the output of the gate driving X is low. In this situation for the fault to be detected P should also create closed paths in A_{2p} and C_p. This is shown in Figure 39. In this case V_z will stabilize at

$$V_Z = V_{DD}\left[\frac{1}{1 + \left(\frac{r_{A1p}}{(r_{A2p} + r_{Tp} + R + r_{In})}\right)}\right]$$

with a time constant not exceeding that of the normal circuit. Thus for large values of R, P does not detect the fault. However, for sufficiently small values of R and depending on the values involved in the above equation, V_z could be logic low and P may detect the fault.

(a)(ii) We now examine the case where P creates a closed path in B_{1p} and C_p. Hence there is always a normal charging path for V_z. Thus if the output of the gate driving X is high the fault will be masked because there is no discharging path. Therefore, P should be such that the output of the gate driving X is low.

(a)(ii-1) We now consider the situation where in addition to the conditions of Case IV (a) (ii) we have the

added constraint that input P does not create a closed path in A_{2p}. This is shown in Figure 40. The voltage V_z stabilizes at

$$V_z = V_{DD}\left[\frac{1}{1 + \frac{(r_{A1p} + r_{Cp})}{(r_{B1p} + R + r_{In})}}\right]$$

with a time constant which never exceeds that of the normal circuit. Thus for large values of R, V_z is logic high and the fault is masked. However, for sufficiently small values of R, depending on the circuit structure V_z may be logic low and hence P might detect the fault.

(a)(ii-2) Now we modify P in Case IV (a) (ii-1) such that there is a closed path in A_{2p}. If T_p conducts, then it is easily shown that W has to be the source. This is shown in Figure 41.In this case it can be shown that V_z stabilizes at

$$V_z = V_{DD}\left[\frac{1}{1 + \frac{(r_{A1p} + R_1)}{(R_2 + R + r_{In})}}\right]$$

with a time constant never exceeding that of the normal circuit where,

$$R_1 = \frac{r_{Cp}(r_{A2p} + r_{Tp})}{(r_{Cp} + r_{A2p} + r_{Tp} + r_{B1p})}$$

$$R_2 = \frac{r_{B1p}(r_{A2p} + r_{Tp})}{(r_{Cp} + r_{A2p} + r_{Tp} + r_{B1p})}$$

Thus for large values of R the fault cannot be detected by P. However, for sufficiently small values of R, depending on the circuit structure, V_z may be logic low and P would detect the fault.

(a)(iii)Now we consider P such that it creates a closed path in B_{1p} but does not create a closed path in C_p. We investigate two different situations of this case depending on whether or not P creates a closed path in A_{2p}.

(a)(iii-1) If P is such that it does not create a closed path in A_{2p}, then the only way P can detect the fault is when it causes the output of the gate driving X to be high. This is shown in Figure 42. In this case V_z will stabilize at

$$Vz = V_{DD} \left[\frac{1}{1 + \frac{(r_{B1p} + r_{B2p} + R + r_{1p})}{r_{A2n} + r_{Cn}}} \right]$$

with a time constant never exceeding that of the normal circuit. Thus for large values of R, V_z is approximately zero and hence the fault is masked. However, for sufficiently small values of R and depending on the circuit structure V_z may be logic high and P may detect the fault.

(a)(iii-2) We now consider P such that it creates a closed path in A_{2p}.In this case it cannot be proven that the charging/discharging constant of the load capacitance of Z

is upper bounded by the time constant of the fault free circuit. Hence the effect of the fault may be different depending on the same value of V_z prior to P being applied. If V_z is low prior to P being applied the analysis is very similar to Case II (a). However, unlike Case II (a) (i), we can no longer claim that P is always a test for sufficiently small values of R. This is because of the existence of r_{Cn} between transistor T_N and V_{SS} which was not present in Case II (a) (i).

Now we analyze the situation where V_z is high prior to P being applied. If P is such that the output of the gate driving X is high then the equivalent circuit is as shown in Figure 43. Recall the definitions of P(L) and P(H) introduced in Case III (b). Since the output of the fault free circuit is logic low then if P(L) is a test for this fault then P(H) is also a test for this fault.

If P is such that the output of the gate driving X is low, then the equivalent circuit is shown in Figure 44. Analogous to the argument used for Figure 43 if P(H) is a test for this fault then P(L) is also a test for this fault.

(b) We now consider the case when P is such that there exists no closed path in A_{1p}. Under this condition if the output of the gate driving X is low then there is no charging path for V_z but there exists a discharging path through A_{1n} so that V_z becomes low irrespective of its value before P was applied. Hence the fault cannot be detected by P. Thus for detection, P must be such that the output of

the gate driving X is high. This situation is illustrated in Figure 45. Furthermore for P to detect the fault it must create a closed path in B_{1p}. If there is no closed path in B_{1p} then T_p can only conduct with Y as source but that would imply that V_{GS} of T_p is positive. Hence T_p is off and there is no path to charge V_z but discharge path through A_{1n} exists.

(b)(i) Under these conditions let us first consider the case when input P does not create a closed path in C_p. This situation is shown in Figure 46. For P to detect this fault V_z must be logic high. But if the P described in this case detects the fault then the P for Case IV (a) (iii-2) will also detect the fault as per the reasoning used in Case II (b) (ii).

(b)(ii-1) We now consider P such that it creates a closed path in C_p but none in A_{2p}. This is shown in Figure 47. It can be shown that V_z will stabilize at

$$V_z = V_{DD} \left[\frac{1}{1 + \frac{(r_{B1p} + r_{B2p} + R + r_{1p})}{r_{A1n}}} \right]$$

with a time constant not exceeding that of the normal circuit. Thus for large values of R, V_z will be logic low and P cannot detect the fault. However, for sufficiently small values of R and depending on the circuit structure, V_z may be logic high and P would detect the fault. However, we expect that if this P detects the fault then the P of Case

IV (a) (iii-2) also detects the fault for practical circuits. This is because in Case IV (a) (iii-2) we have an additional charging path and the discharging path is worse than that for Case IV (b) (ii-1) because T_n of Figure 43 is not fully conducting since V_x is less than V_{DD}. Simulation results verify this line of reasoning.

(b)(ii-2) We now consider P such that it creates closed paths in C_p and A_{2p}. This is shown in Figure 48. It can be easily shown that transistor T_p cannot conduct. Hence the situation is identical to that of Case IV (b) (ii-1).

Analysis of Cases V through VIII can be done in a manner analogous to the dual Cases I through IV. We note that if a particular p-FET bridging fault is testable by a stuck-at-zero (one) test then the corresponding n-FET bridging fault is testable by a stuck-at-one (zero) test. The analogy between p-FET bridging faults and n-FET bridging faults is illustrated by considering Case V and showing its similarity to Case I. The analysis of the remaining cases can be done in an identical fashion.

CASE V

The general structure for Case V is shown in Figure 49. Following the argument used in Case I we can conclude that any input P that detects this fault must create closed paths in A_n and B_n. If we now draw the equivalent circuits with

the modification that V_{ss} is at the top and V_{dd} at the bottom and marking electron current directions instead of conventional current directions, we obtain Figure 50 and 51. Comparison with Figure 18 and Figure 19 exhibit the analogous nature of the analysis of n-FET faults. Thus as in Case I we can conclude that for a certain $R < R_{th}$ input P as shown in Figure 50 will detect the fault and that P is also a test for X stuck-at-zero.

SECTION 2 (b)(i)

ANALYSIS OF RESULTS FOR TRANSISTOR BRIDGING FAULTS

We now proceed to analyse the different cases outlined in the previous sub-section and develop a model which can be used to generate tests for these faults.

We have already shown that all detectable faults in Cases I and II are detected by tests for single stuck-at-faults.

We now consider the faults described by Case III. When P does not create a closed path in A_{1P} (see Figure 28) we have shown that if P detects this fault then the value of R must be small. This implies that the input P(L) for Case III (b) (i) also detects this fault since transistor T_P cannot conduct for small values of R. But P(L) is a test for transistor T_P stuck-open.

We have seen in Cases III (a) (i) and III (a) (ii) that if P detects the fault then the value of R is small. As explained earlier this implies that the test for transistor T_P stuck-open will also detect the fault.

For Case III (a) (iii), shown in Figure 33, for P to detect the fault, V_Z must be logic low. P is now modified to P' by changing inputs so that there is no closed path in C_P. If P' is applied when V_Z is low then we expect V_Z to reach a value which is lower than that of Figure 33 because we have

removed a charging path (C_P). Thus P' also detects the fault. Note however that P' is a test for T_P stuck-open.

In Case III (b) (i) we have already shown that the fault can be detected by the test for transistor T_P stuck-open.

Note that for Figure 39 and 41 [Cases IV (a) (i) and IV (a) (ii-2)] V_Z must be logic low for the fault to be detected. Comparing the V_Z values obtained earlier for these two cases we conclude that the V_Z value is lower for Case IV (a) (ii-2). This V_Z value is expected to be higher than that of Case IV (a) (iii-2) with the output of gate driving X made low (see Figure 44) because in the latter we remove a charging path (C_P). Thus if P for Case IV (a) (i) or IV (a) (ii-2) detects the fault then that for Case IV (a) (iii-2), as shown in Figure 44, also detects the fault. Note that P for Case IV (a) (iii-2) is always an input pattern in any test set that detects stuck-at and stuck-open faults.

In Case IV (a) (iii-1), V_Z must be logic high for P to detect the fault. If this P detects the fault then we expect that P for Case IV (a) (iii-2) with X high (see Figure 43) will also detect the fault. This is because in the latter case we have an additional charging path through A_{2P} whereas A_{2N} no longer has a closed path.

Up to this point, we have analysed all cases except IV (a) (ii-1). We have shown that for these cases if corresponding input pattern P detects the fault then the fault is also detected by any test set that detects stuck-at faults at the input of the gate and transistor stuck-open

faults. Simulation results have confirmed the reasoning used in the above analysis.

As far as Case IV (a) (ii-1) is concerned, simulation results for the circuit given in Figure 52 show that P detects this fault for bridging resistances less than 80 kilo-ohms. Note that the circuit of Figure 52 was chosen so that P of Case IV (a)(ii-1) has the maximum likelihood of detecting the fault. In other words this circuit would give the maximum value of resistance R for which this P will detect this fault. However, the test for X stuck-at-one detects the fault for short resistances less than 70 kilo-ohms. Thus we have an example of a bridging fault in a "practical" circuit where a test set designed to detect all single stuck-at and transistor stuck-open faults does not detect the fault but a test for this fault exists. By the term "practical" circuit we mean a circuit which does not have more than four p (or n) transistors in any series path from V_{DD} to output (or output to V_{SS}). A larger number of transistors result in impractically large delays. However, in practice it has been observed [Soden,1985] that the value of bridging resistance ranges from a few ohms to about 5 kilo-ohms. Thus a test set designed to detect all single stuck-at and transistor stuck-open faults would detect all practical cases of transistor bridging faults.

SECTION 3

TRANSISTOR STUCK-OPEN FAULTS

Analysis of an open fault in a CMOS gate is based on determining the presence of a break in a conduction path [Chandramouli,1983]. If there is an open fault in the drain or source of a p (n) transistor, then that p (n) transistor will not conduct. So if there is a break in the drain or the source of a p (n) transistor, all the pull up (down) paths that have that transistor in series, will not conduct. Thus to check a drain or a source open fault in a p (n) transistor, the output of the circuit is first pulled to 0 (1). Then the pull up (down) path, with the p (n) transistor in question, is activated. If there is a fault, the pull up (down) path will not conduct; and the load capacitance at the output node cannot be charged. Thus the output will remain at 0(1) and the fault can be detected.

It is possible to localize a fault to a particular path since a fault in any transistor in that path will have the same effect. To check for open faults in any particular path one has to apply a pair of inputs [Jha,1986]. The first is an initialization input which sets the output node at a certain voltage. The next is the evaluation input which should produce a change in the output node voltage if the path being checked does not have an open fault.

Assume that there is only one transistor with an open fault at its drain or source. We can test for the presence of this fault in a p-transistor T_P and it's corresponding n-transistor T_N by applying three tests. The first sets the output to logic high. The second activates pull down path(s) such that all closed paths pass through T_N. The third activates pull up path(s) such that all closed paths pass through pass through T_P. In this case, high-low-high is the fault free output. Alternately, the output could be set to logic low instead, and the paths checked in the reverse order. In this case, low-high-low would be the fault free output. Note that the second and third tests are tests for single stuck-at faults at the gate input which is common to T_P and T_N. Furthermore these three tests may detect multiple stuck-open faults if the inputs used to activate the paths described are chosen carefully.

The presence of input skews can prevent the faults from being detectable by the above method. Suppose there is an open fault in a pull down path and there is a particular input combination that is applied to charge the output node to logic high. In general, only some of the inputs have to be changed to activate the pull down path. Due to different inputs changing at different times, this may result in another pull down path being activated momentarily due to a transient input combination. This could discharge the output node and make the circuit appear fault free even if it is not. One way to avoid the skewing problem is to use an extra control input.[Reddy,1986]

We now propose a testing scheme that cannot be invalidated by input skewing and does not require any additional control inputs. Let P_1 P_2 P_3 denote the three tests described earlier. If P_2 and P_3 differ only in the gate input X, common to T_N and T_P, and $P_1 = P_3$ then the resulting test sequence cannot be invalidated by input skewing. This is because consecutive stages of the P_1 P_2 P_3 sequence involve a change in a single input.

We now show that if a test for T_N or T_P stuck-open exists then we can always find P_1 and P_2 satisfying the requirements of our proposed scheme. In order to test for T_N stuck-open there must exist an input pattern such that all closed paths from output to V_{SS} pass through T_N. This is the P_2 required in our scheme. We note that the input X must be set to 1 in P_2. P_1 can be obtained from P_2 by only changing X to 0. Thus in P_1 there can be no paths from output to V_{SS}. So there is closed path(s) from V_{DD} to output. Moreover all these paths must pass through T_P. This is because we did not have a closed path from V to output in P_2 but by changing only X closed path(s) were obtained. Hence the described scheme avoids the problem of input skewing.

Lastly, if the gate of a transistor is open, the fault may not be easily detectable. For example, if a p transistor was on when a break occurred at the gate, the capacitance associated with the gate will keep the transistor conducting for some time. So the circuit will behave as a pseudo-nMOS circuit as long as the transistor conducts. This can, however, be detected by current monitoring. SPICE

simulations show that the current drawn by the faulty circuit (an inverter) will be in the milliamp range while the current drawn by the normal circuit is in the order of picoamps. Moreover, if the open gate is affected by voltage fluctuations in adjacent lines, it's voltage may change and make the circuit behavior unpredictable.

SECTION 3.1

STUCK-OPEN FAULTS IN CMOS INVERTERS

The circuit for a CMOS inverter is shown in Figure 53. In this figure, Cg is the gate capacitance of a p or a n transistor, and Cl is the capacitance of the output node of the inverter. The possible locations of open faults are marked as 1 to 7. Another inverter has been used as a load in the SPICE simulations and resistances varying from 1 to 50 Megaohms have been used to simulate a constriction in the line which may lead to a break. Vout should follow Vin in the fault free case, while Vl should be the complement of Vin. Faults 1,2 and 3 are classified as gate faults, 4 to 7 as drain and source faults.

SECTION 3.1(a)

DRAIN AND SOURCE FAULTS

Positive and negative pulses are defined as follows:

A positive pulse has a value of 0 V for a time sufficiently large for the circuit under consideration to reach a steady state. The pulsed value is 5 V for a duration of 50 ns and the final value is 0 V for a further 50 ns.

A negative pulse has a value of 5 V for a time sufficiently large for the circuit under consideration to reach a steady state. The pulsed value is 0 V for a duration of 50 ns and the final value is 5 V for a further 50 ns.

FAULTS 4 AND 5

The faults 4 and 5 can be treated together, as they exhibit identical behavior.

Positive Pulse applied at Vin:

Before the pulsed period, in the steady state, T1 is conducting, Vout is 0 V while V1 is 5 V. During the period when the pulse is 5 V, the n transistor T2 conducts as expected, and the load capacitance C1 is discharged. Thus Vout becomes logic high. When Vin is 0 V again, T1 conducts but due to the fault resistance C1 cannot charge to a logic high in the remaining 50 ns. So V1 remains logic low and Vout remains logic high for the remainder of the pulse.

Negative pulse applied at Vin:

Before the pulsed period, T1 is off, T2 is on, and C1 is discharged. V1 is logic low and Vout is logic high. When the pulse is 0 V, T1 turns on, but due to the fault resistance C1 cannot charge to a logic high. So V1 remains at logic low and Vout remains at logic high. When the pulse returns to 5 V, T2 is turned on again, C1 remains discharged and Vout remains logic high.

These have been verified by SPICE simulations. Resistances of the open faults were varied from 1 to 50 Megaohms. Both faults 4 and 5 showed identical behavior. The value of C1 used in the simulations was the capacitance associated with the model parameters. In practice it will be larger than the value used in the simulations (due to the

contacts and metal lines), which reinforces the validity of the results.

FAULTS 6 AND 7

Similarly, faults 6 and 7 can be treated together.

Positive pulse applied at Vin :

Initially T1 is on, T2 is off, V1 is at logic high and Vout is logic low. After Vin reaches 5 V, T2 turns on but due to the large fault resistance, C1 cannot discharge to a logic low. As a result, the logic levels of V1 and Vout do not change. After Vin goes back to 0 V, V1 remains at logic high and Vout at logic low.

Negative pulse applied at Vin:

The transistor T2 is on before the pulse occurs and so C1 is discharged. When the pulse occurs, T2 is turned off, T1 is turned on, and the circuit behaves normally. After Vin returns to 5 V, T2 turns on but C1 cannot discharge during the remainder of the pulse due to the presence of the fault resistance. Hence V1 remains at logic high and Vout remains at logic low.

The above analysis have been verified by simulation.

The results can be summarized as follows:

	Drain or Source fault in	
Input Voltage	T1	T2
Vin	Vout	Vout
	case 1	case 2
Positive Pulse 0 V	logic low	logic low
5 V	logic high	logic low
0 V	logic high	logic low
	case 3	case 4
Negative Pulse 5 V	logic high	logic high
0 V	logic high	logic low
5 V	logic high	logic low

The effect of the fault was observed for cases 2 and 3 during the pulsed period, and for cases 1 and 4; after the pulse.

SECTION 3.1(b)

STUCK-OPEN FAULTS AT THE GATES

Gate fault modelling can be considerably more complicated than the modelling of drain and source faults. Here the current values are extremely small, and the coupling of the open gate with neighboring lines may make the transistor behavior unpredictable. The behavior of the transistor after the gate open fault has occurred depends on whether the channel of the transistor exists or not.

If a transistor is in conduction when its gate is opened, its channel will be present for some time until the charge in the channel leaks away. During this time period the transistor will conduct. If the p transistor has a gate open fault, the CMOS inverter will behave as a pseudo-nMOS inverter while the p transistor conducts, and the fault will be masked during this period. The current drawn by the circuit will increase significantly. If the n transistor has a gate open fault, then the circuit may give a wrong result, depending on the resistance of the fault.

The line open faults at the gates (1,2,and 3) have been modelled by a large resistor whose value was varied from 1 to 50 Megaohms. There is a shunt capacitance across this resistor which results from the break. It was observed from the simulations that the existence of the shunt capacitance (estimated, to be of the order of fF, from the physical dimensions of the break) did not change the circuit

behavior. The circuit behavior is dependent on the time constant of the RC circuit that comprises of the RC equivalent of the break and the gate capacitances to the right of the break. The simulation results are explained in the following sub section.

FAULTS 2 AND 3

Faults 2 and 3 are similar.The response of the circuit in the presence of faults 2 and 3 are identical for complementary input pulses.

Fault 2:

Positive pulse applied at Vin:

Before the pulsed period T1 is on, V1 is logic high and Vout is logic low. When the pulsed period occurs, T1 does not turn off as its gate capacitance is not charged due to the presence of the fault resistance. T2 however, turns on, and the circuit behaves as a pseudo-nMOS inverter. The subsequent gate sees the output as a logic low, and hence gives the proper output. However, the current drawn in this case is much larger (a factor of a million) than the normal value.

Negative pulse applied at Vin:

Initially T2 is on, T1 is off, V1 is logic low, and Vout is logic high. When the pulsed period occurs, for a resistance of 1 Megaohm, the circuit exhibits a large rise time. For larger fault resistances however, T1 cannot turn on in the pulse duration (50 ns) and V1 stays logic low;

Vout remains at logic high during and after the pulsed period. Therefore, the fault can be detected during the pulsed period.

Fault 3:

Positive pulse at Vin:

Initially T1 is on, T2 is off, V1 is logic high, and Vout is logic low. When the pulsed period occurs, for a fault resistance of 1 Megaohm, the circuit exhibits a large rise time. For higher fault resistances, T2 cannot turn on during the pulsed period. So C1 remains charged at logic high, and Vout remains at logic low. Hence the fault can be detected during the pulsed period.

Negative pulse at Vin:

Initially T1 is off, T2 is on. During the pulsed period, T1 turns on but due to the presence of the fault resistance, T2 does not turn off. So V1 is determined by the resistances of T1 and T2. V1 varies from 0.16V, at the beginning of the pulsed period, to 1.9v (for 1 Megaohm) and 0.8v (for 50 Megaohms) at the end of the pulsed period. The next inverter thus sees V1 as a logic low, and so Vout stays at logic high. So this fault is detectable.

FAULTS AT BOTH GATES

Fault 1:

In the presence of this fault, the circuit shows a memory effect. For this fault, the gates of both the

transistors are affected. The combined gate capacitances are not charged sufficiently through the fault resistor. So for all values of fault resistors used, the effective logic value at the input of T1 and T2 remains unchanged during the pulsed period. Hence voltages V1 and Vout retain their previous logic values. So for both cases, the fault is detectable.

Tabulating these results:

Fault	Positive pulse	Negative pulse
1	detectable	detectable
2	detectable*	detectable
3	detectable	detectable

* detectable by current monitoring only.

SECTION 3.2

ANALYSIS OF RESULTS FOR TRANSISTOR STUCK-OPEN FAULTS

The study of open faults in inverters shows that faults can be classified broadly into two categories: those on the output side (i.e. source and drain faults) and those on the input side (gate faults).

The drain and source faults have identical behavior, and results in a break in the conduction path. If detectable, these faults can be detected by employing a sequence of three tests.

The gate faults are more difficult to model due to smaller currents at the gate,and due to unpredictable coupling between the open gate and other neighboring lines. For the fault resistances used in the simulation, faults 2 and 3 are detectable. Fault 1 is also detectable and gives rise to the 'memory' effect as the circuit retains its previous logic value. Fault 2 cannot be detected by a positive pulse input unless current monitoring is used.

SECTION 4

TRANSIENT FAULTS CAUSED BY ALPHA-PARTICLE RADIATION

A transient fault is a temporary nonrecurrent fault. Alpha-particles are a major source of this type of fault. It is conjectured that alpha-particles produce high current density pulses which in turn may cause electromigration resulting in open lines[Kornreich,1987]. Figure 54(a) shows a simplified model for a CMOS inverter. A theoretical model for representing the effect of alpha-particles in the CMOS inverter is shown in Figure 54(b). In this model alpha-particles affect only the lines containing capacitors C_2 and C_3, and do not affect the lines containing C_1 and C_4. This is because C_1 and C_4 are connected to V_{dd} and V_{ss} respectively and are hence more immune than C_2 and C_3 to external effects.In this model pulse current sources I_1 and I_2 are placed as shown in the figure.

In CMOS circuits, alpha particles can cause both 1 --› 0 and 0 --› 1 transition. As mentioned above, they do not in general affect the V_{dd} and V_{ss} lines as they are very well protected. If an alpha-particle strikes a signal line in a CMOS circuit, a pulse is usually generated which may or may not propagate through the circuit. It is necessary to investigate the effect of the pulse on the circuit.

To simulate the effect of alpha-particles in logic

circuits a circuit consisting of cascaded inverters, as shown in Figure 55, was used. A pulse was fed to the input of inverter 1 and its effect was noted as it propagated through the other inverters. Pulses of varying widths, as shown in Figure 56, were fed at the input of inverter 1.

The width of the pulse, measured at an amplitude of 3.2 Volts, for the outputs of inverters 2, 4, and 6 (i.e. the voltages V(2), V(4), and V(6)) is tabulated in Figure 57. When the input pulse width is 1ns, it was observed that the amplitude of the pulse decreases as the number of inverter stages increase. This effect is not noticed for wider input pulses. From Figure 57 we notice that the pulse width at the measured amplitude increases with the number of inverter stages. This is because the associated RC time constant increases with the number of inverter stages. However, irrespective of the number of inverter stages the pulse is always propagated to the output. The effect of pulses of width less than 1ns could not be studied because of the limitation of SPICE.

Currently there are two major techniques for dealing with such transient faults. The first method is based on the duplication of hardware. This has two drawbacks : (i) the overhead is very large ; (ii) both copies of circuits may fail causing wrong data to be accepted as being correct.

The alternative approach is to use 'filtering'. In this approach filtering circuits are placed between combinational logic blocks and registers. The filters are basically integrators which eliminate the transients caused by alpha-

particles. However, this introduces additional delay in the circuit.

The conclusion that can be drawn from our experiment is that pulses caused by alpha-particle radiation may trigger latches and hence cause sequential circuits to behave incorrectly.

SECTION 5

CONCLUSION

In this report we have presented a detailed examination of the most probable permanent faults in CMOS circuits i.e. bridging faults and stuck-open faults. Bridging faults were studied under two categories viz. input bridging and transistor bridging faults.

We have concluded that it is not possible to develop a generalized model for input bridging faults. The effect of an input bridging fault depends not only on the structure of the circuits driving the input nodes which are bridged but also the input pattern to these driving circuits. Hence both these factors have to be taken into account while deriving test sets for input bridging faults. We concluded that a test set designed to detect all single stuck-at and transistor stuck-open faults would detect all single transistor bridging faults in practical circuits where the bridging resistance is less than 70 kilo-ohms. We remark that in practice it has been observed [Soden, 1985] that the value of bridging resistance ranges from a few ohms to about 5 kilo-ohms. We have seen earlier that the charging/discharging time constant of the faulty circuit is crucial in determining the effect of certain transistor bridging faults. We also recall that if the

charging/discharging time constant of the faulty circuit exceeds that of the normal circuit then whether or not the fault will be detected within one test period depends on the test frequency. Consequently for a particular fault the masking resistance is higher for a test sequence with a lower frequency than that with a higher one.

Stuck-open faults at the drain and source of a transistor can be detected by employing a sequence of three tests. We have proposed a testing scheme that is not invalidated by input skewing and does not require additional control inputs. Stuck-open faults at the gate of the transistor are more difficult to model due to smaller currents at the gate and due to unpredictable coupling between the open gate and other neighbouring lines. We have verified by simulation that certain cases of a stuck-open faults give rise to a "memory" effect.

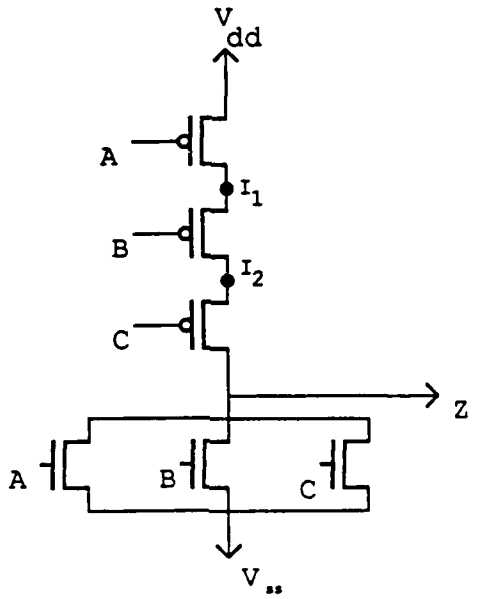
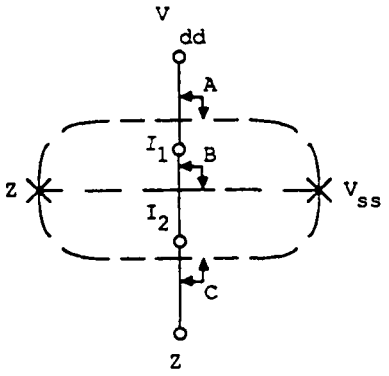
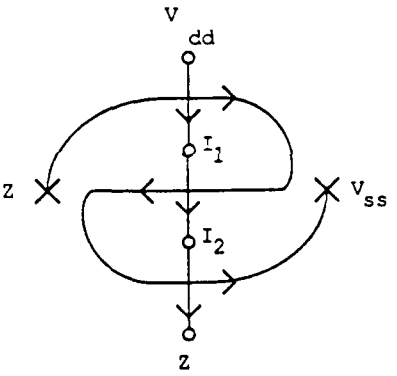


FIGURE 1(a)



Algorithm For Layout.

FIGURE 1(b)



Euler Path A -B -C.

FIGURE 1(c)

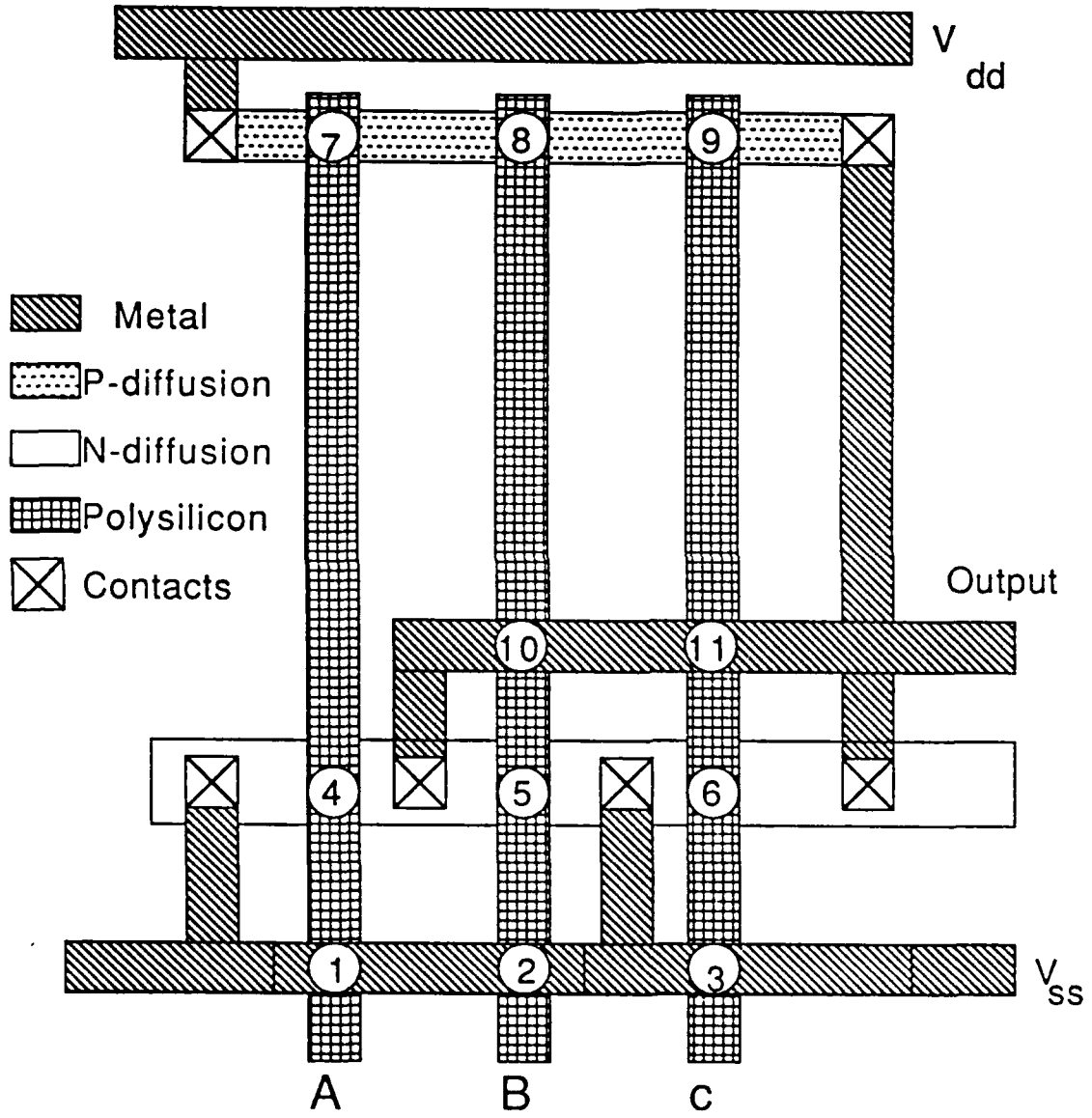
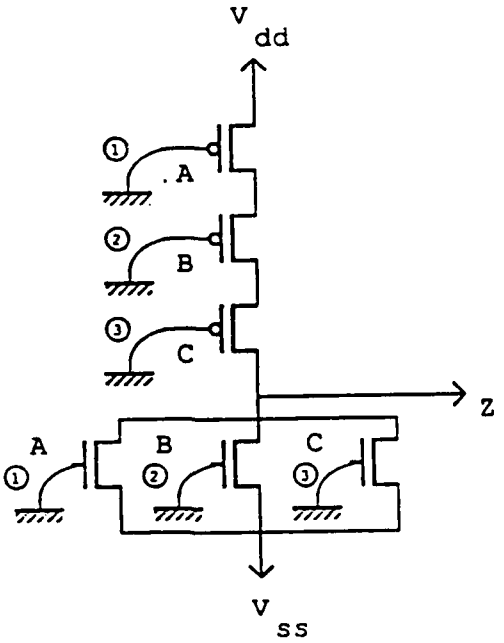

V dd
7
8
9
Metal
P-diffusion
N-diffusion
Polysilicon
Contacts
Output
10
11
4
5
6
1
2
3
V ss
A
B
c

FIGURE 2

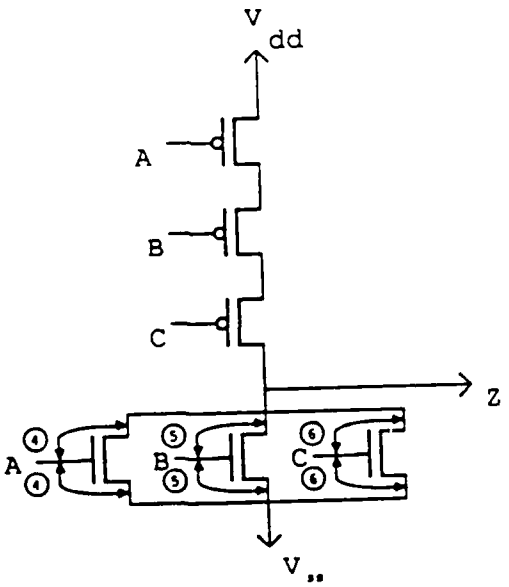


GROUP 1

Points On Layout : 1,2,3

Metal - Polysilicon short.

FIGURE 3

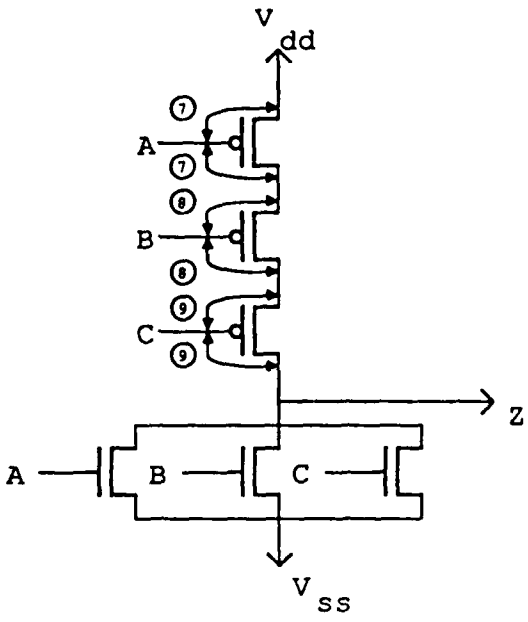


Group 2

Points On Layout: 4,5,6.

Polysilicon N-Diffusion Short.

FIGURE 4

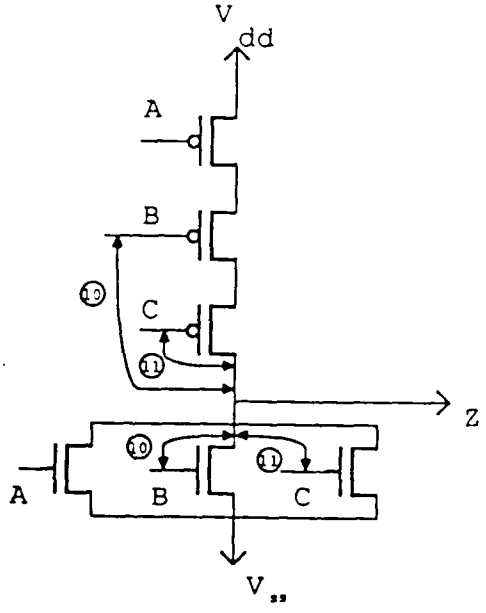


GROUP 3

Points On Layout : 7,8,9.

Polysilicon P-Diffusion Short.

FIGURE 5.



Group 4

Points On Layout: 10,11.

Metal Polysilicon Short.

FIGURE 6.

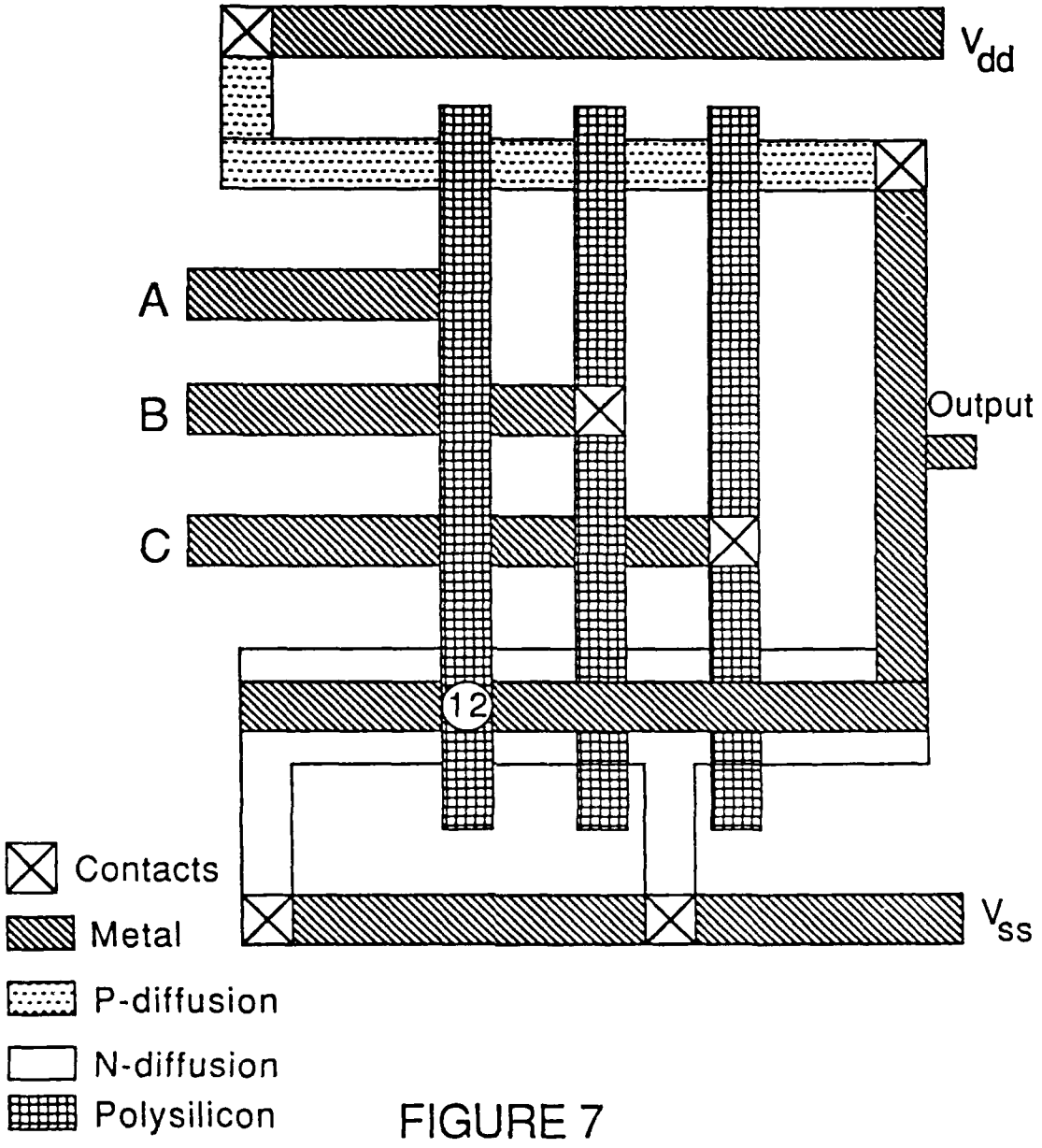
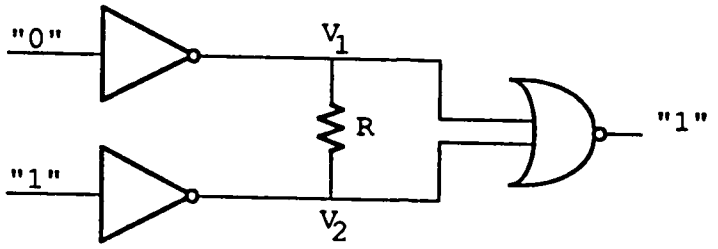

V_{dd}
A
B
C
Output
12
V_{ss}
Contacts
Metal
P-diffusion
N-diffusion
Polysilicon

FIGURE 7



R = 100

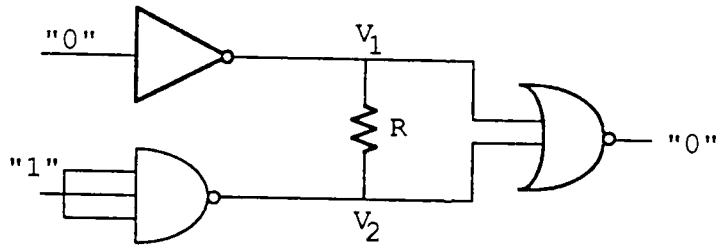
SIMULATION RESULTS

V_1 = 0.78 v

V_2 = 0.766 v

} LOGIC LOW

FIGURE 8 (a)



R =100

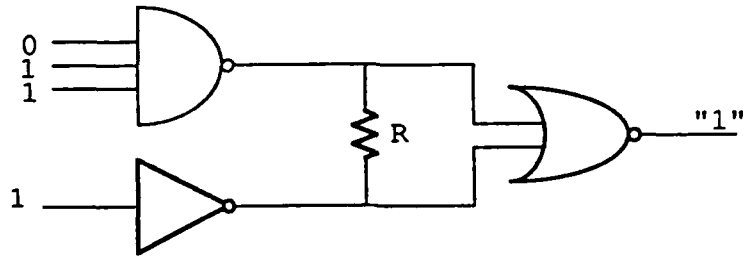
SIMULATION RESULTS

V_1 = 2.779 v

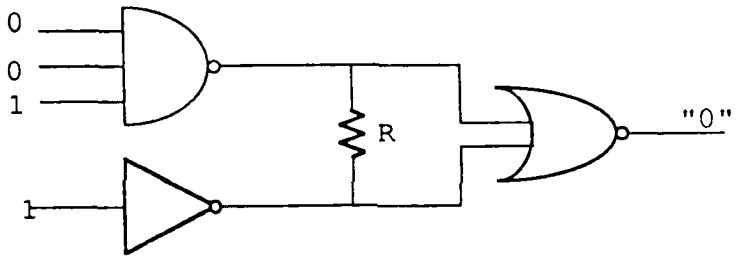
V_2 = 2.766 v

} LOGIC HIGH

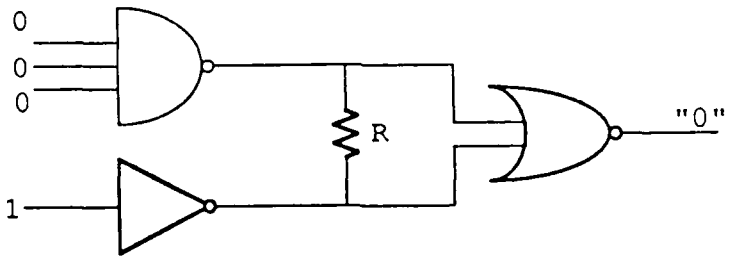
FIGURE 8(b)



(a). WIRED -AND



(b). WIRED-OR



(c). WIRED-OR

FIGURE 9.

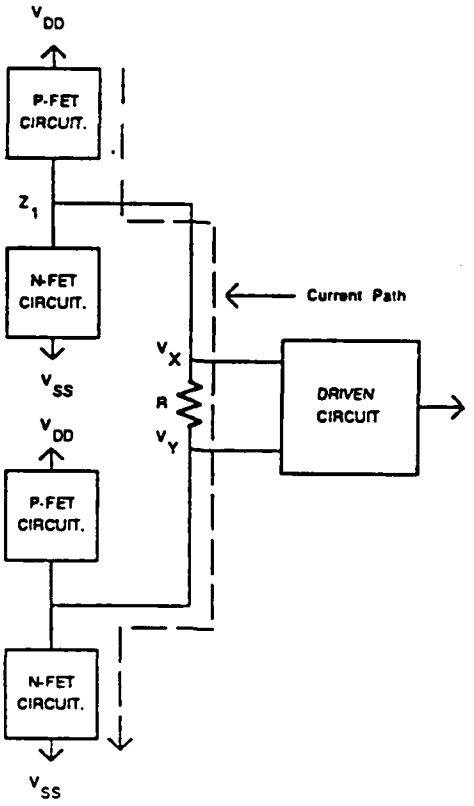


FIGURE 10

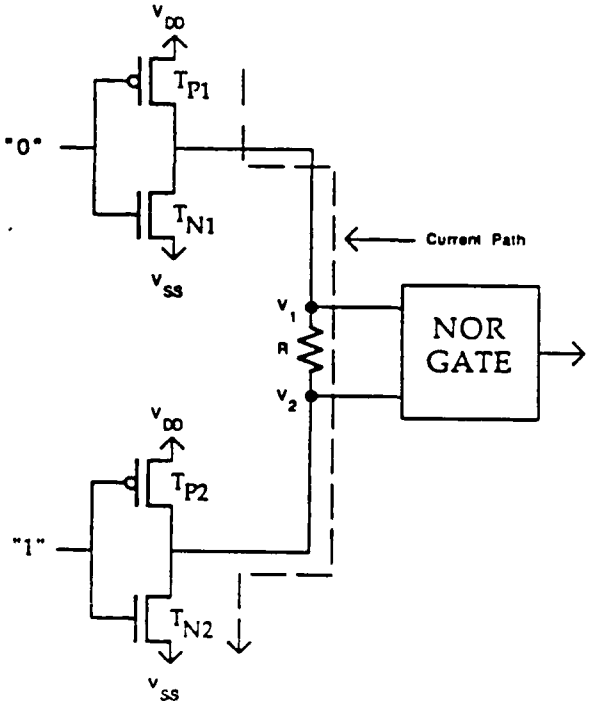


FIGURE 11(a)

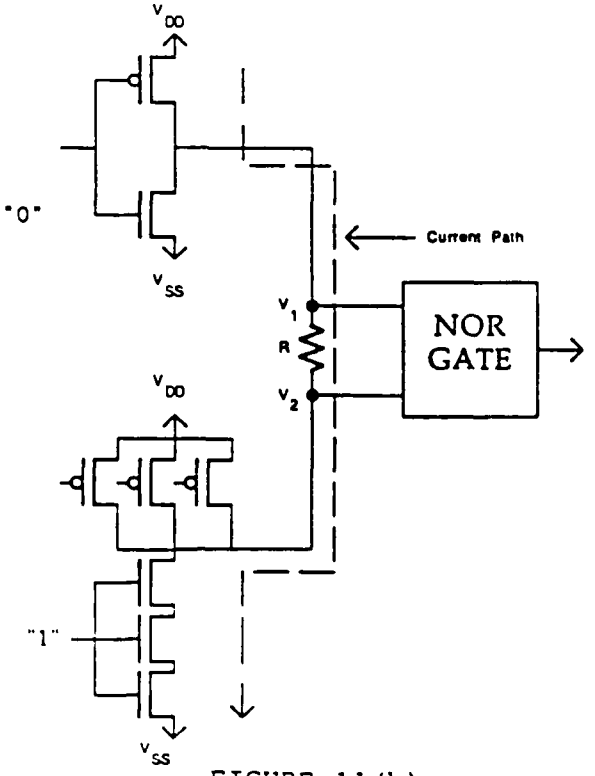


FIGURE 11(b)

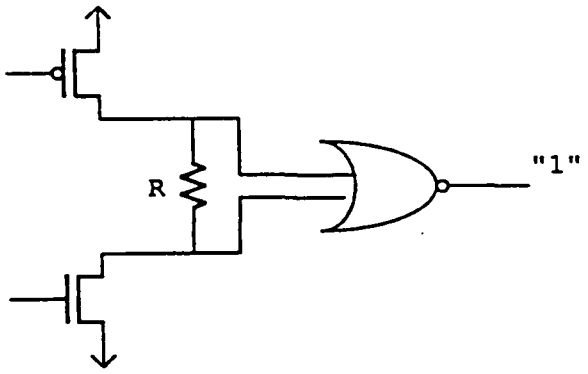


FIGURE 12(a)

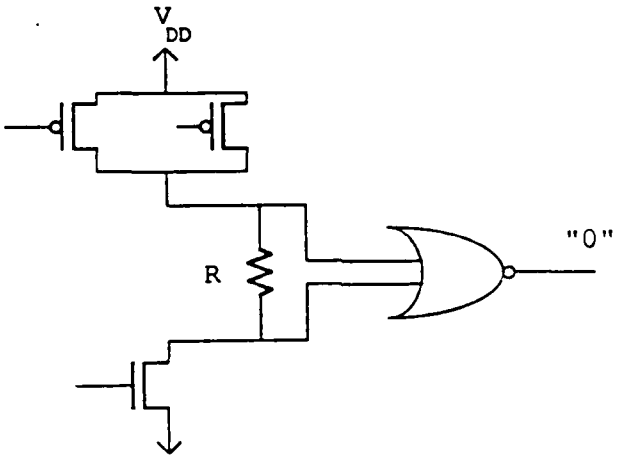


FIGURE 12(b)

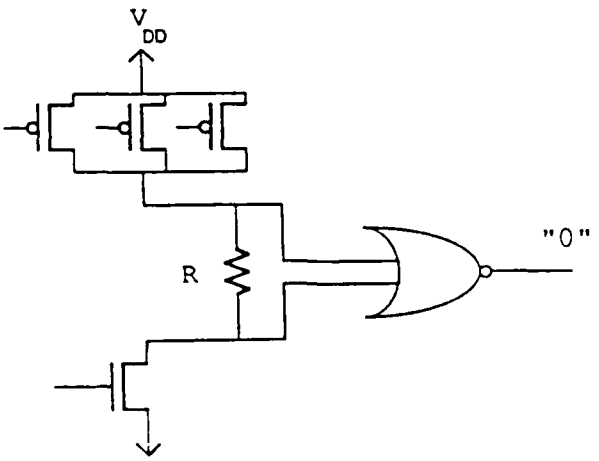
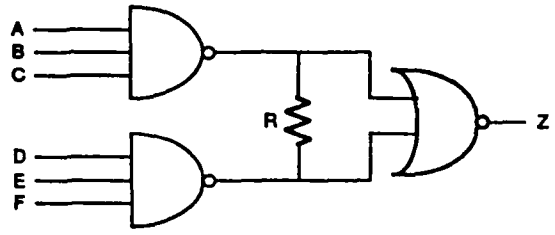
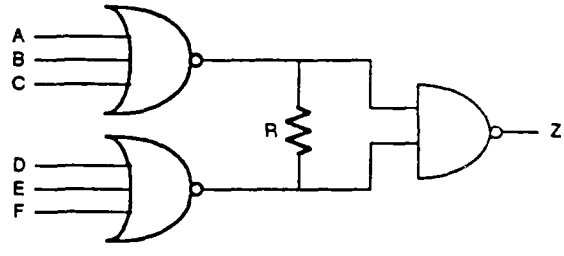


FIGURE 12(c)



A B C D E F	Z Normal	Z using Wired-And Model	Z Simulation Result
1 1 1 1 1 1	1	1	1
0 1 1 1 1 1	0	1	0
1 0 1 1 1 1	0	1	0
1 1 0 1 1 1	0	1	0
1 1 1 0 1 1	0	1	0
1 1 1 1 0 1	0	1	0
1 1 1 1 1 0	0	1	0

FIGURE 13.



A B C D E F	Z Normal	Z using Wired-or Model	Z Simulation Result
0 0 0 0 0 0	0	0	0
1 0 0 0 0 0	1	0	1
0 1 0 0 0 0	1	0	1
0 0 1 0 0 0	1	0	1
0 0 0 1 0 0	1	0	1
0 0 0 0 1 0	1	0	1
0 0 0 0 0 1	1	0	1

FIGURE 14

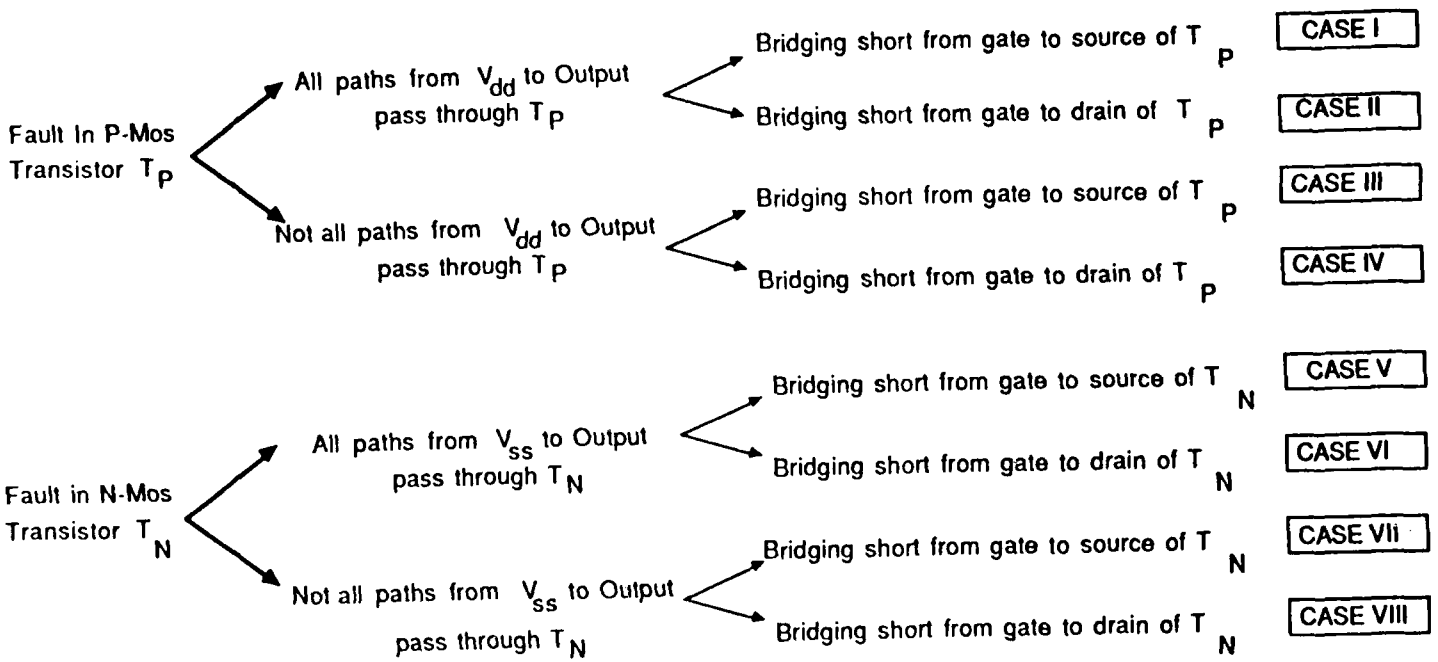


FIGURE 15. TRANSISTOR BRIDGING FAULTS.

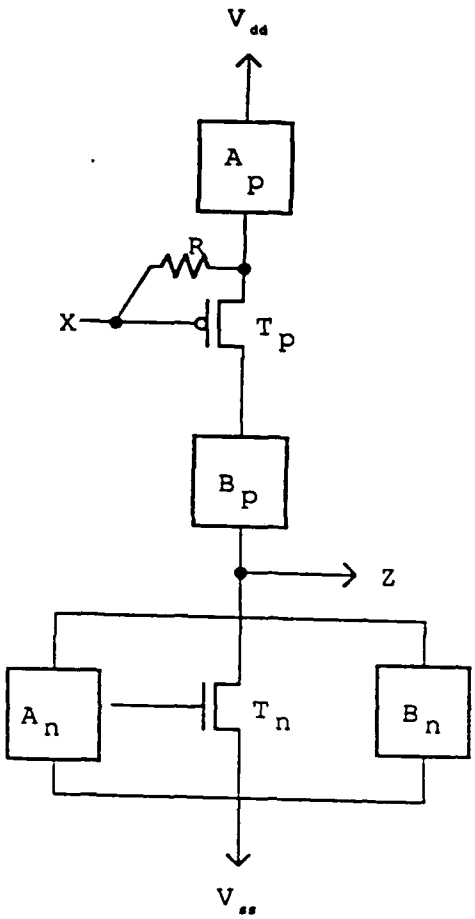


Fig 16. GENERAL CIRCUIT FOR CASE I

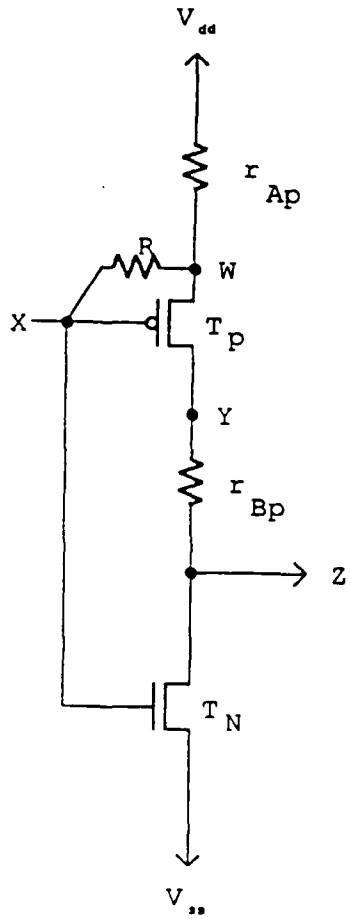


Fig 17. CIRCUIT FOR CASE I WITH INPUT CONSTRAINTS REQUIRED TO DETECT THE FAULT

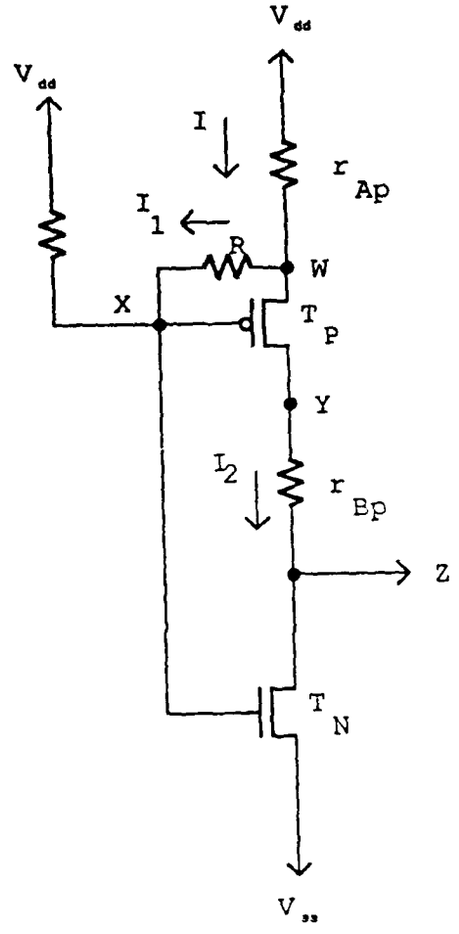


Fig 18. CIRCUIT FOR CASE I(i)

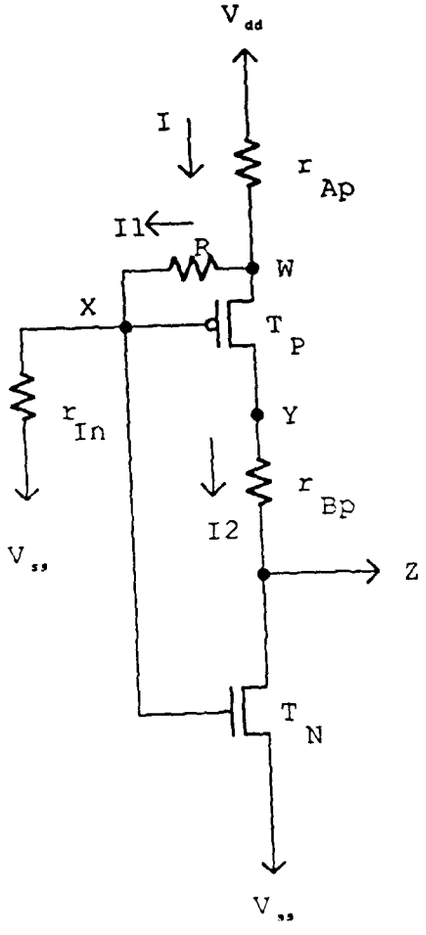


Fig 19. CIRCUIT FOR CASE I(ii)

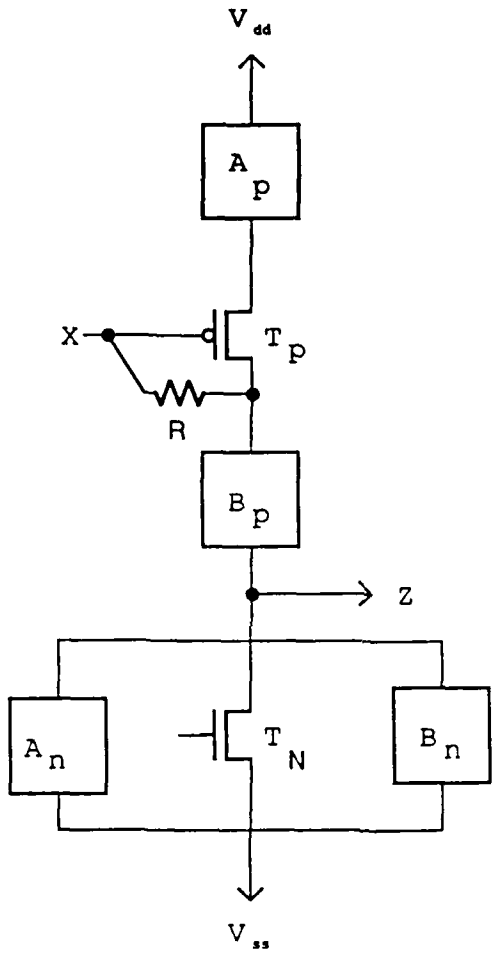


Fig 20. GENERAL CIRCUIT FOR CASE II

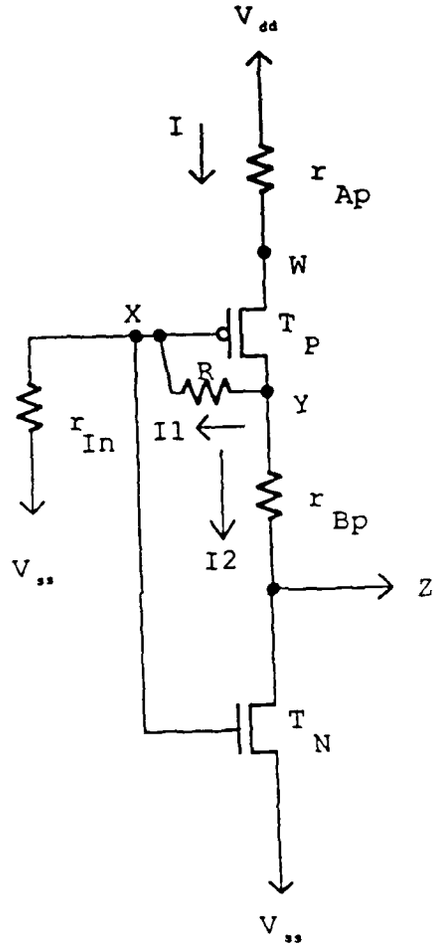


Fig 21. CIRCUIT FOR CASE II (a)(i)

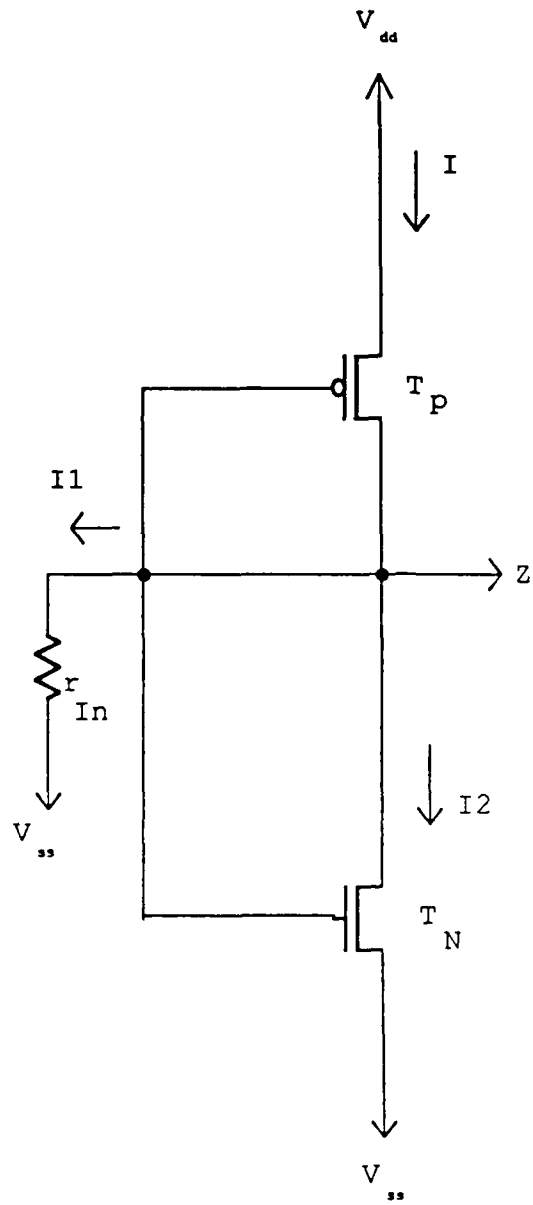


Fig 22. CIRCUIT FOR CASE II (a) (i) WHEN

$$R = r_{Ap} = r_{Bp} = 0$$

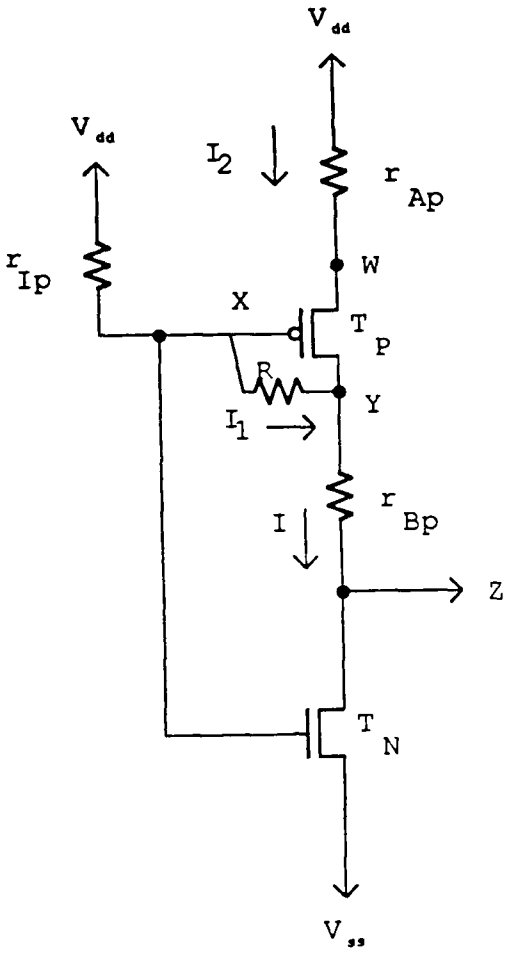


Fig 23. CIRCUIT FOR CASE II (a) (ii)

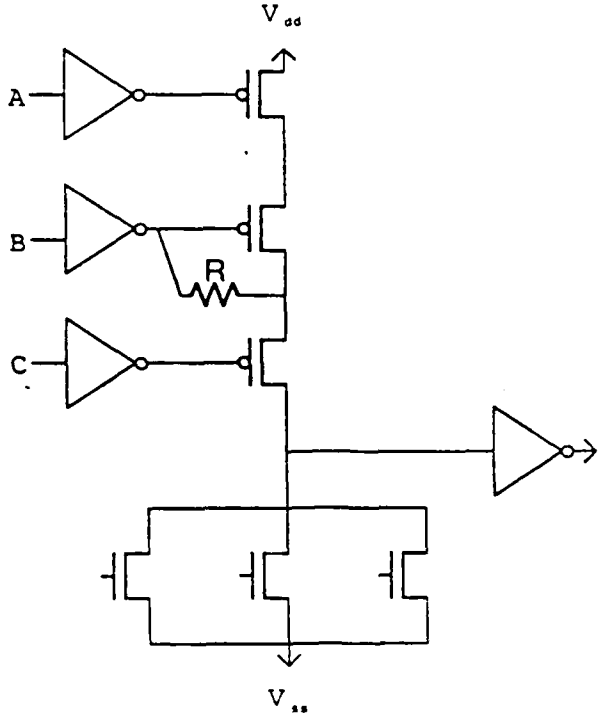


Fig 24(a) CIRCUIT FOR CASE II(a)(ii) WHERE P =ABC= 010 DOES NOT DETECT THE FAULT FOR ANY VALUE OF R.

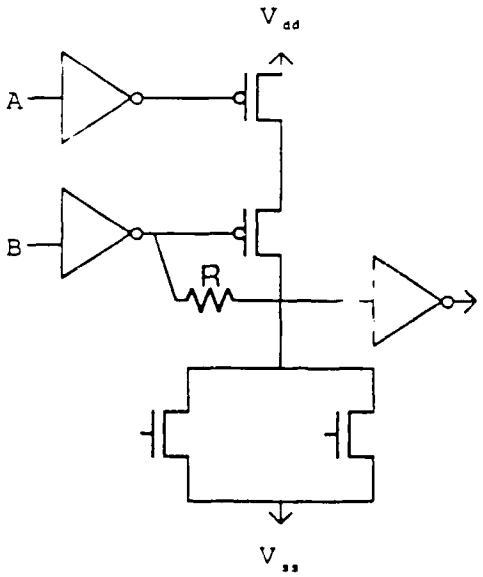


Fig 24(b) CIRCUIT FOR CASE II(a)(ii) WHERE P =AB= 01 DETECTS THE FAULT.

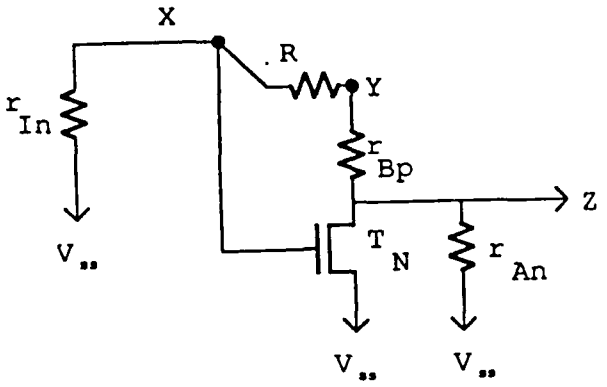


Fig 25. CIRCUIT FOR CASE II (b) (i)

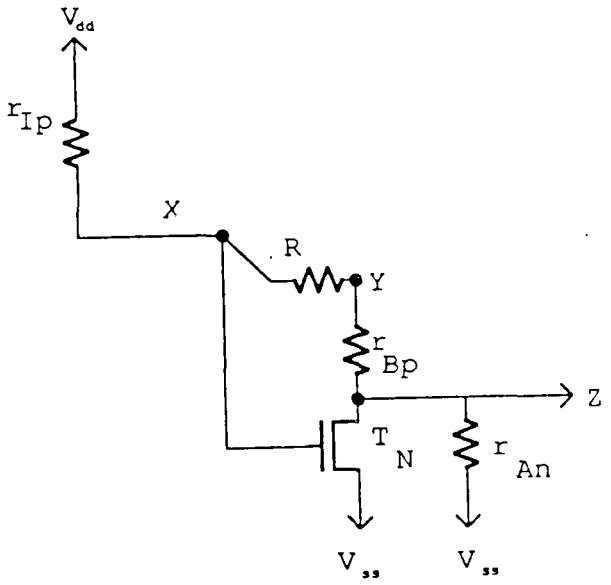


Fig 26. CIRCUIT FOR CASE II (b) (ii)

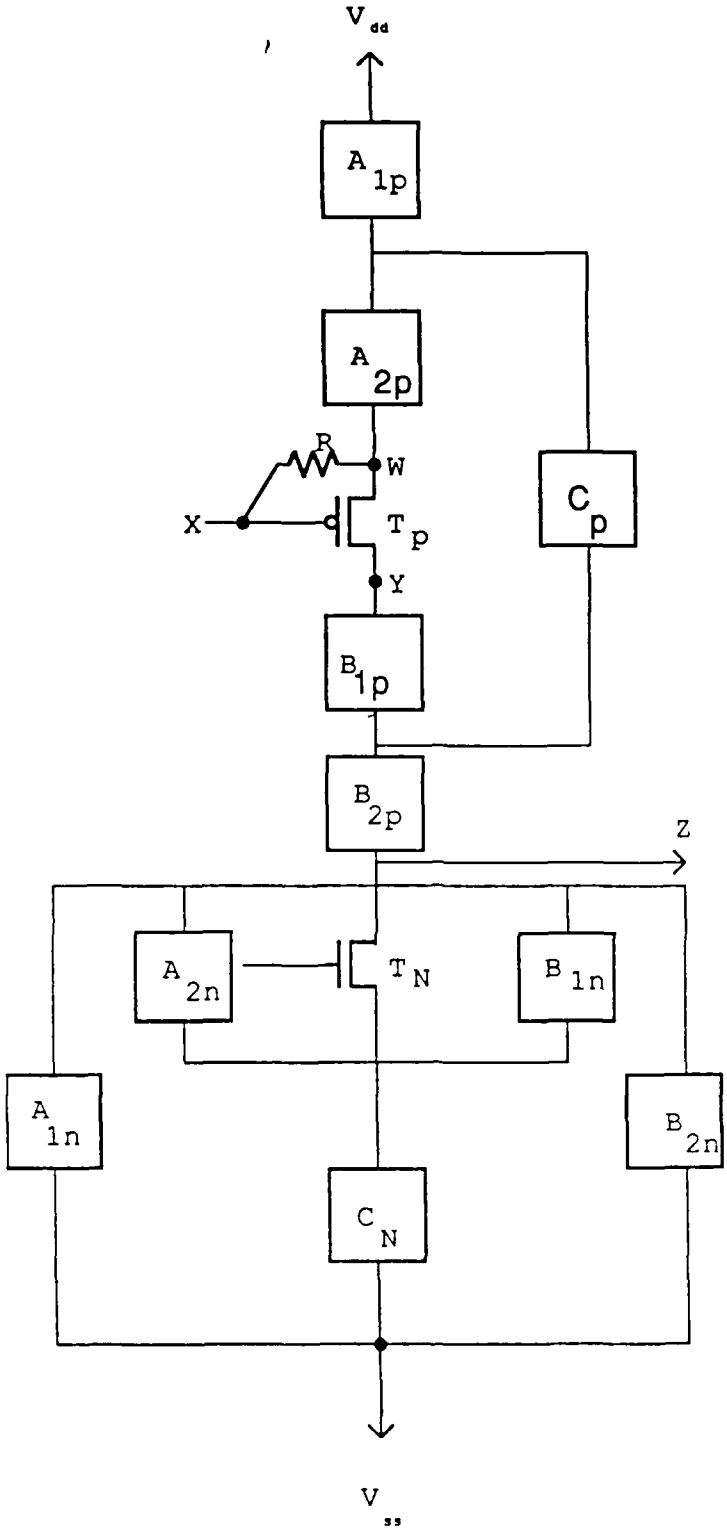


Fig 27. GENERAL CIRCUIT FOR CASE III

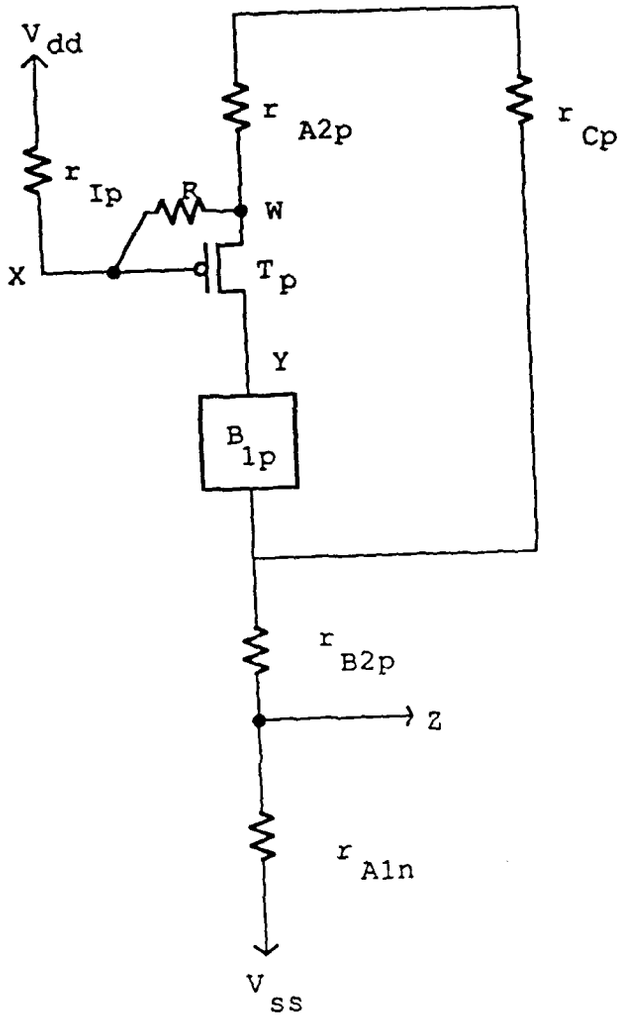


Fig 28. CIRCUIT FOR CASE III WHEN P CREATES CLOSED PATHS IN A_{2p}, C_p, B_{2p} AND A_{1n}

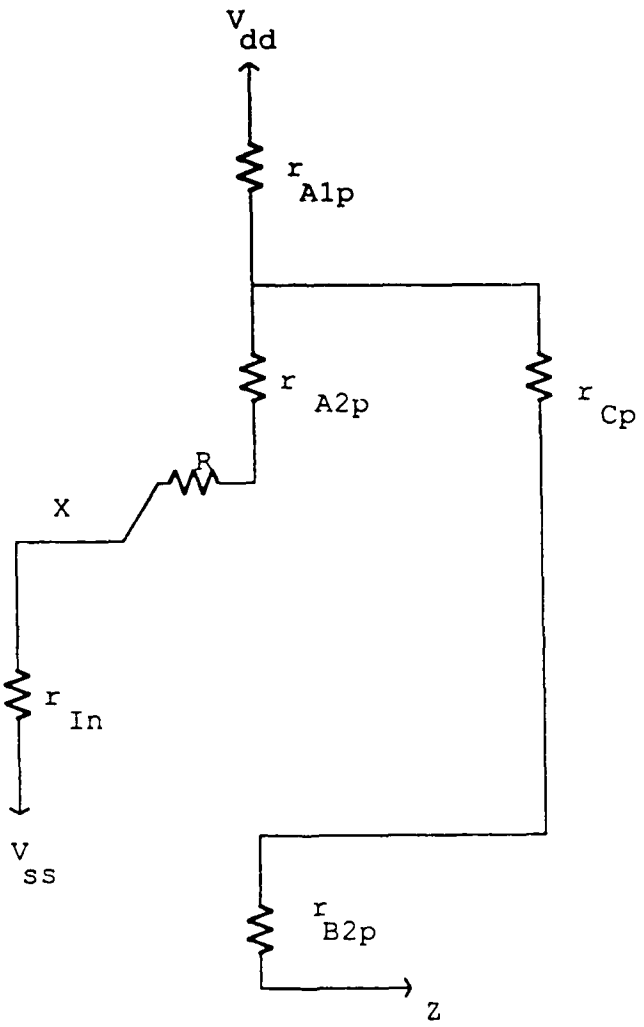


Fig 29. CIRCUIT FOR CASE III (a) (i)

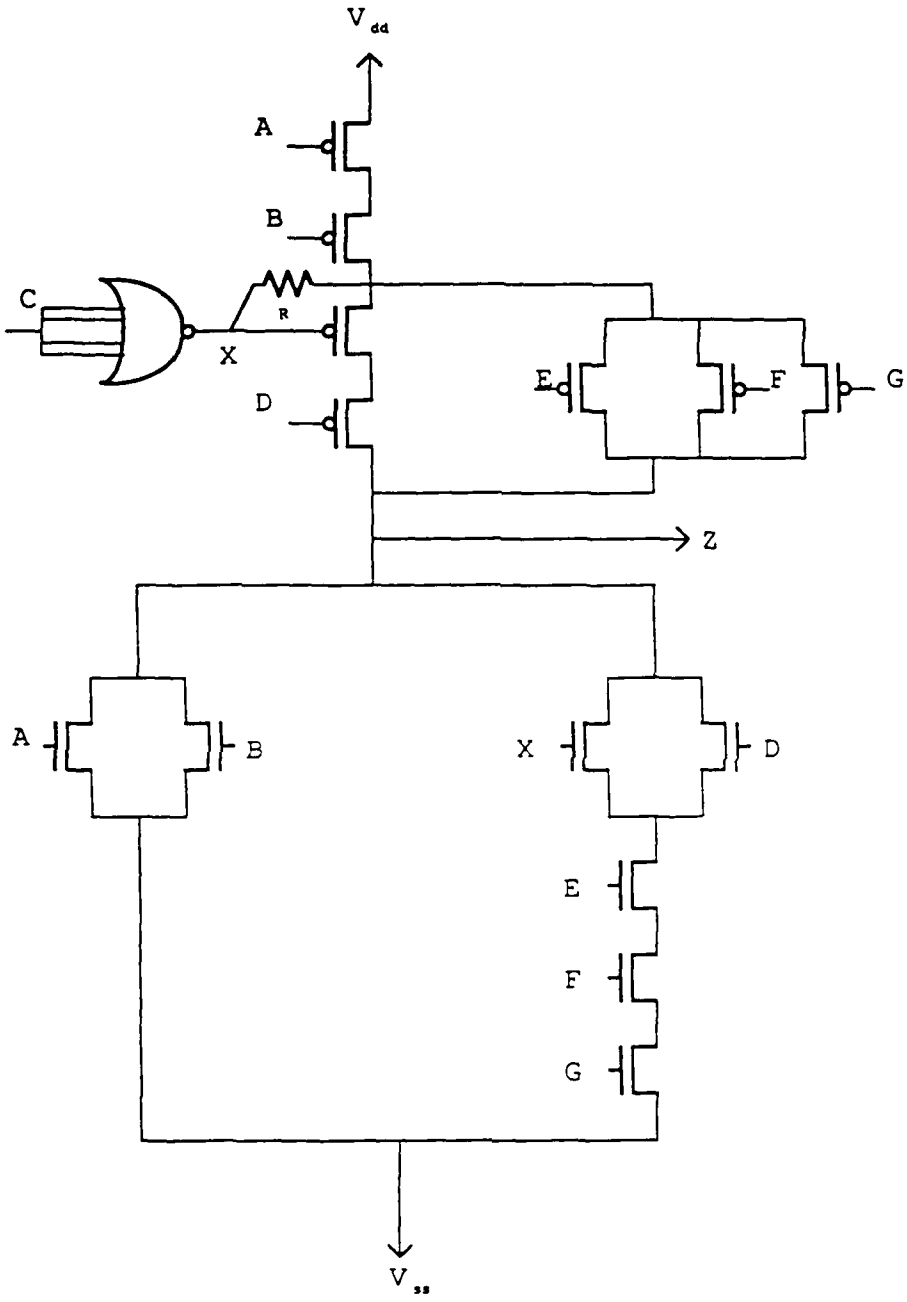


Fig 30. EXAMPLE FOR CASE III (a) (i) WHERE

P = ABCDEFG = 0011000 IS A TEST

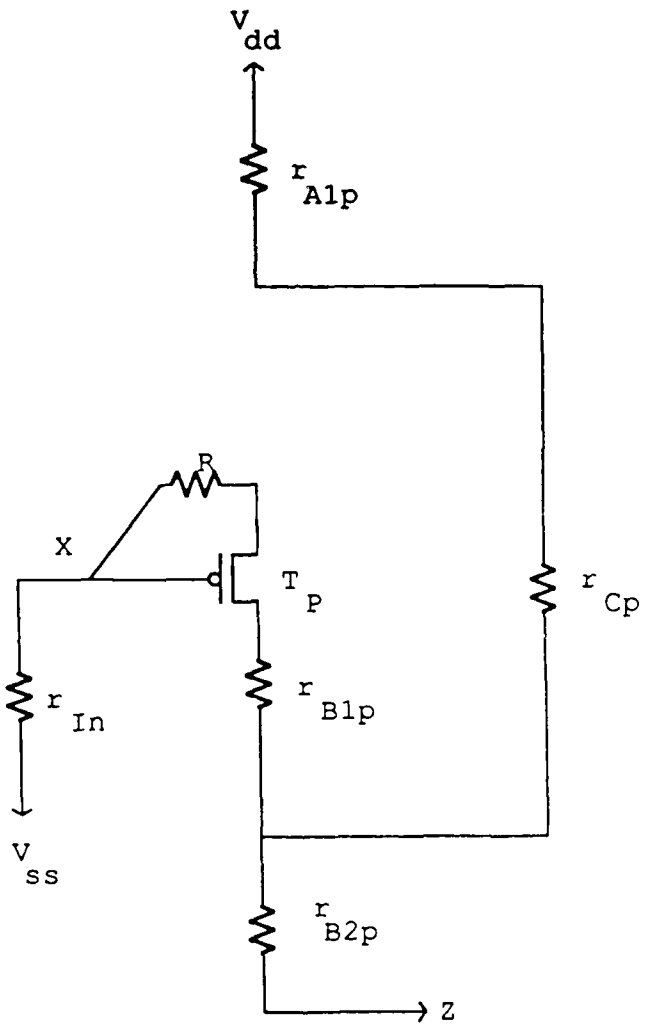


Fig 31. CIRCUIT FOR CASE III (a) (ii)

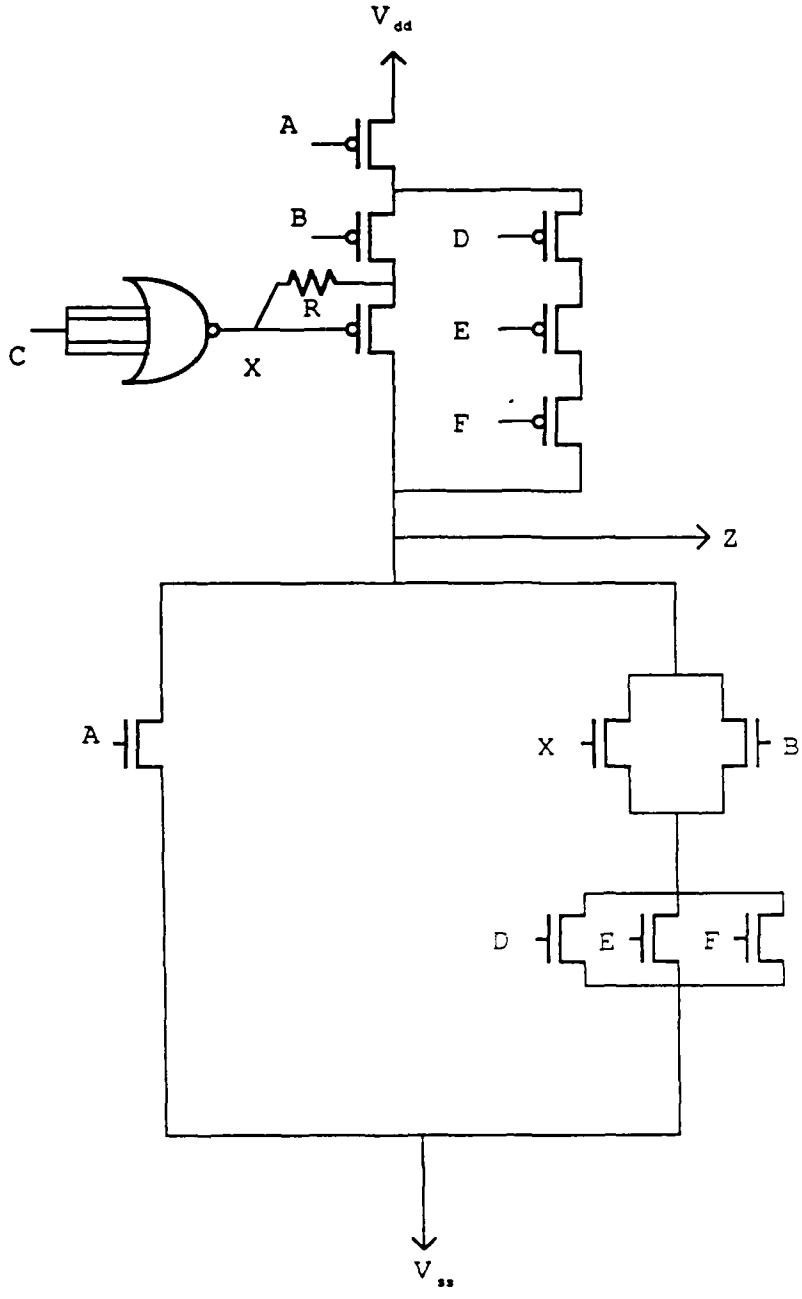


Fig 32. EXAMPLE FOR CASE III (a) (ii) WHERE

P = ABCDEF = 011000 IS A TEST

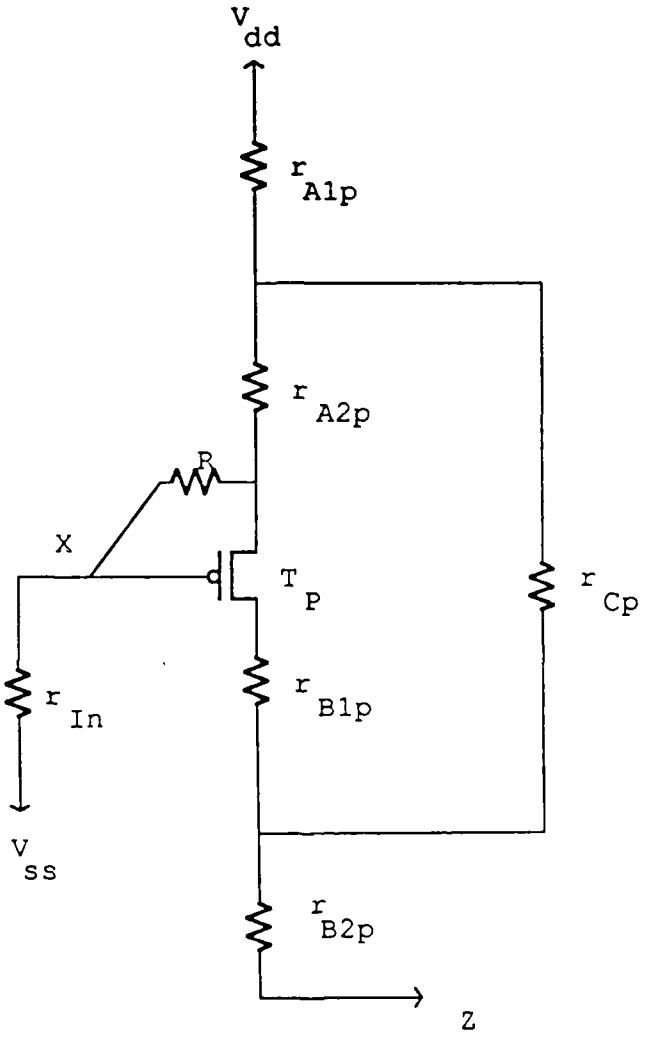


Fig 33. CIRCUIT FOR CASE III (a) (iii)

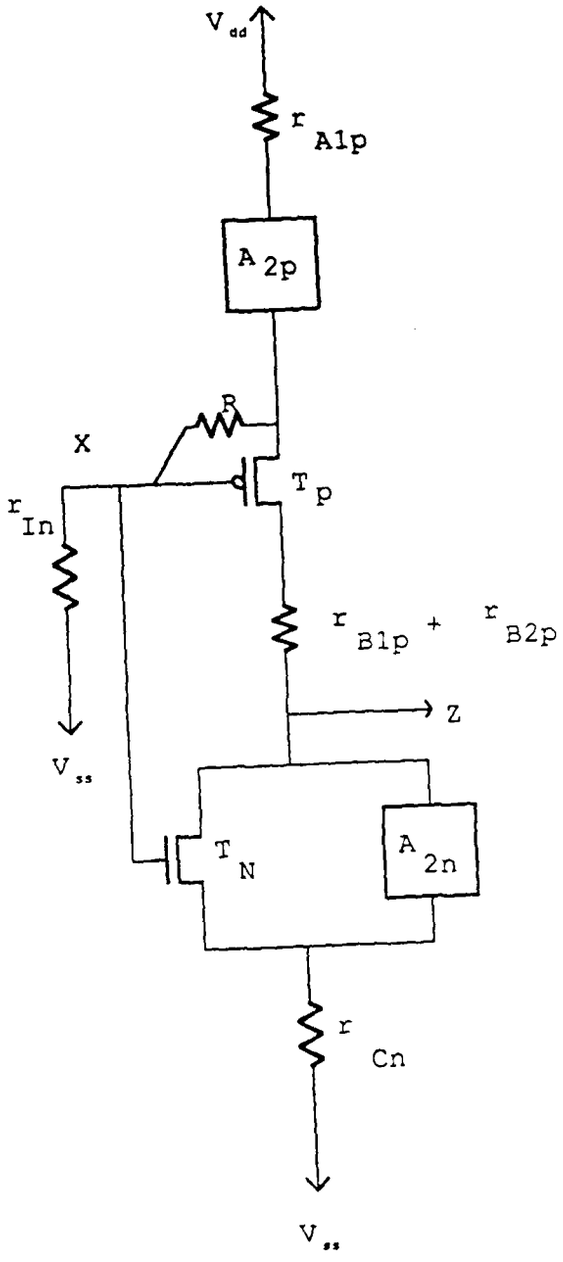


Fig 34. CIRCUIT FOR CASE III (b)

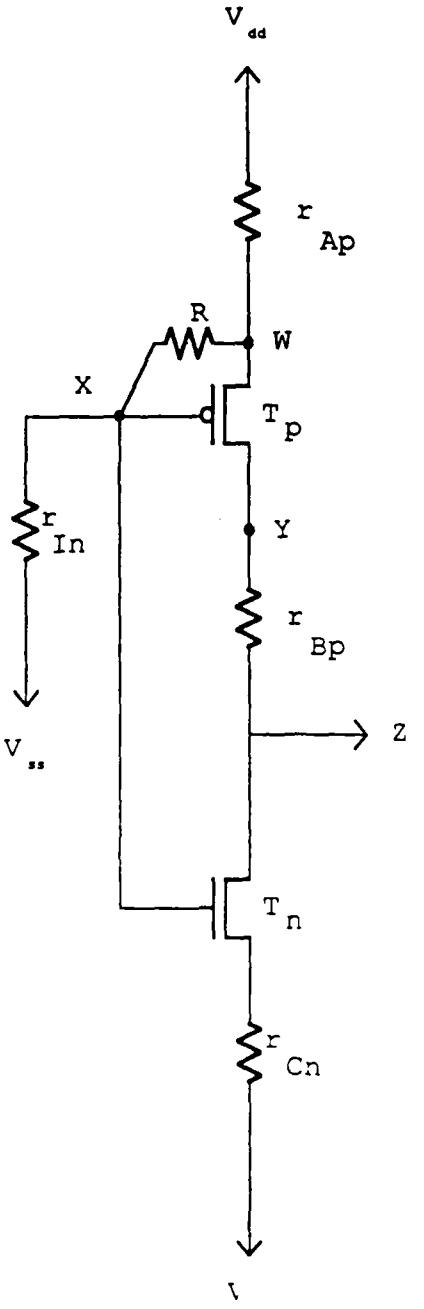
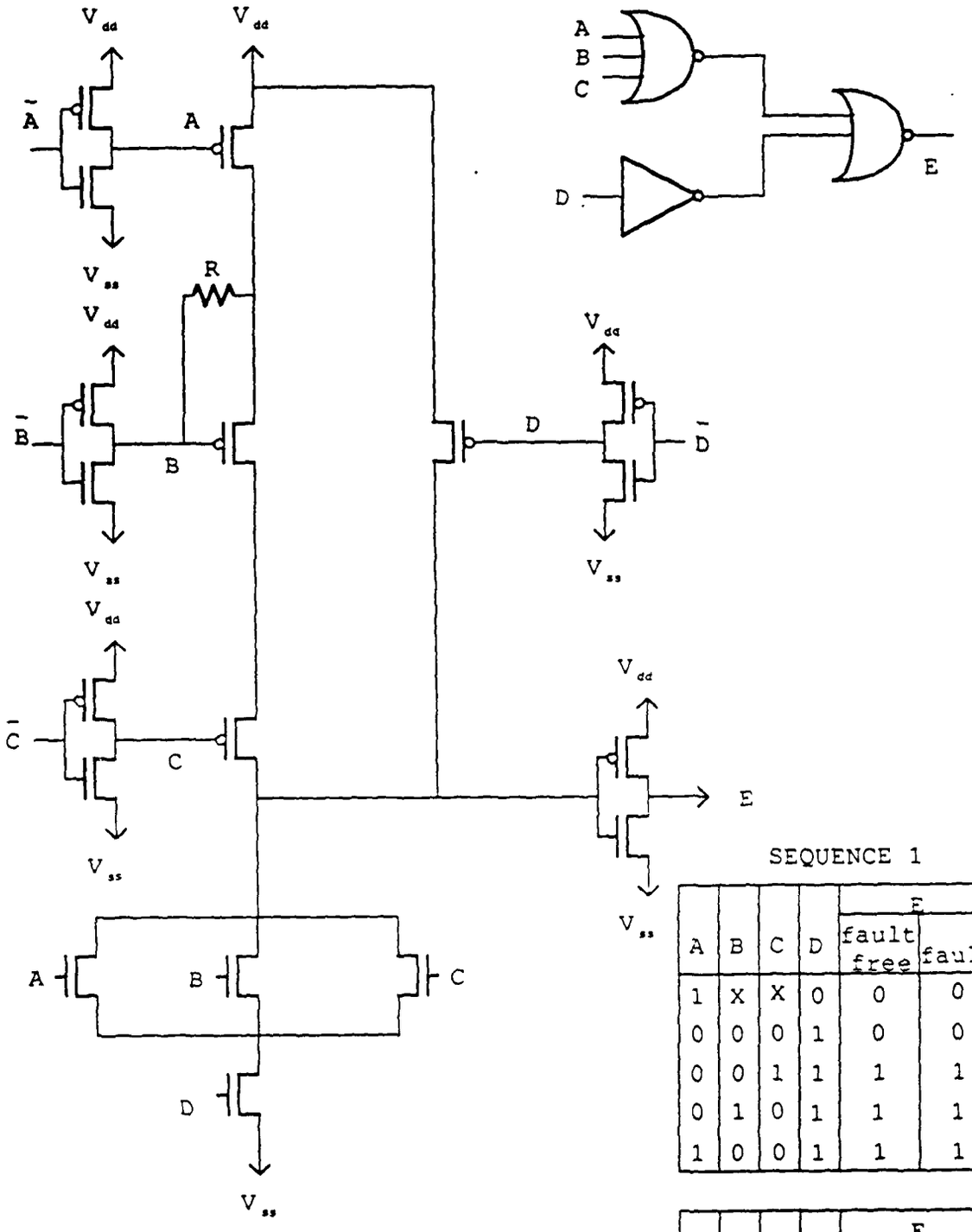


Fig 35. CIRCUIT FOR CASE III (b) (i)



SEQUENCE 1

A	B	C	D	E fault free	E faulty
1	X	X	0	0	0
0	0	0	1	0	0
0	0	1	1	1	1
0	1	0	1	1	1
1	0	0	1	1	1

A	B	C	D	E fault free	E faulty
1	X	X	0	0	0
1	0	0	1	1	1
0	1	0	1	1	1
0	0	1	1	1	1
0	0	0	1	0	1

SEQUENCE 2

FIG 36. EXAMPLE FOR CASE III(b)(i) WHICH EXHIBITS SEQUENTIAL BEHAVIOR FOR R = 6000 OHMS.

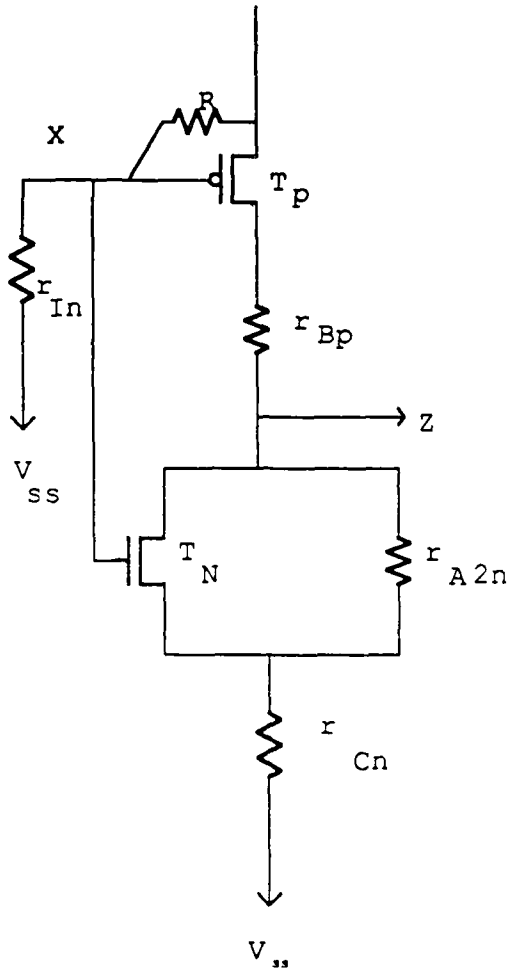


Fig 37. CIRCUIT FOR CASE III (b) (ii)

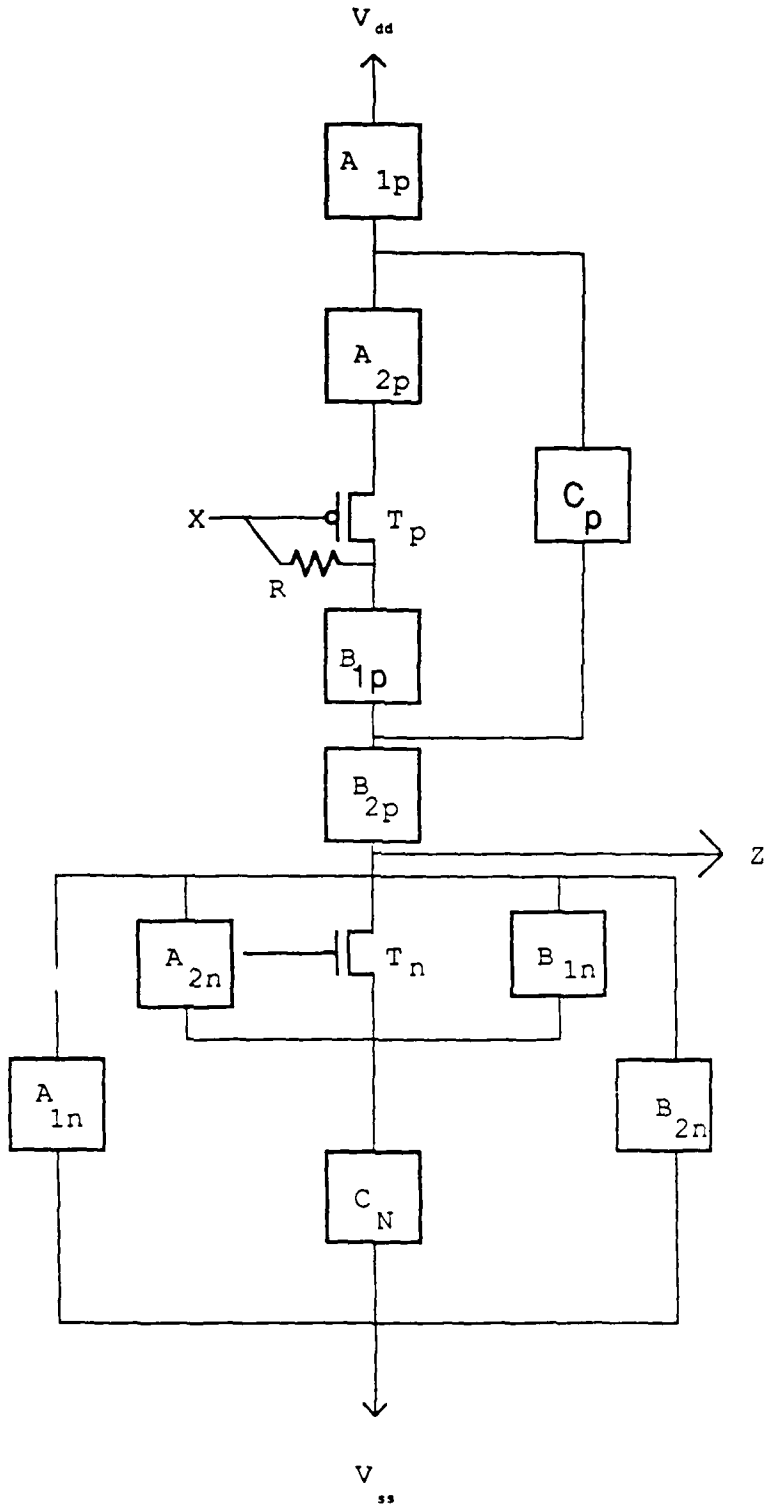


Fig 38. GENERAL CIRCUIT FOR CASE IV

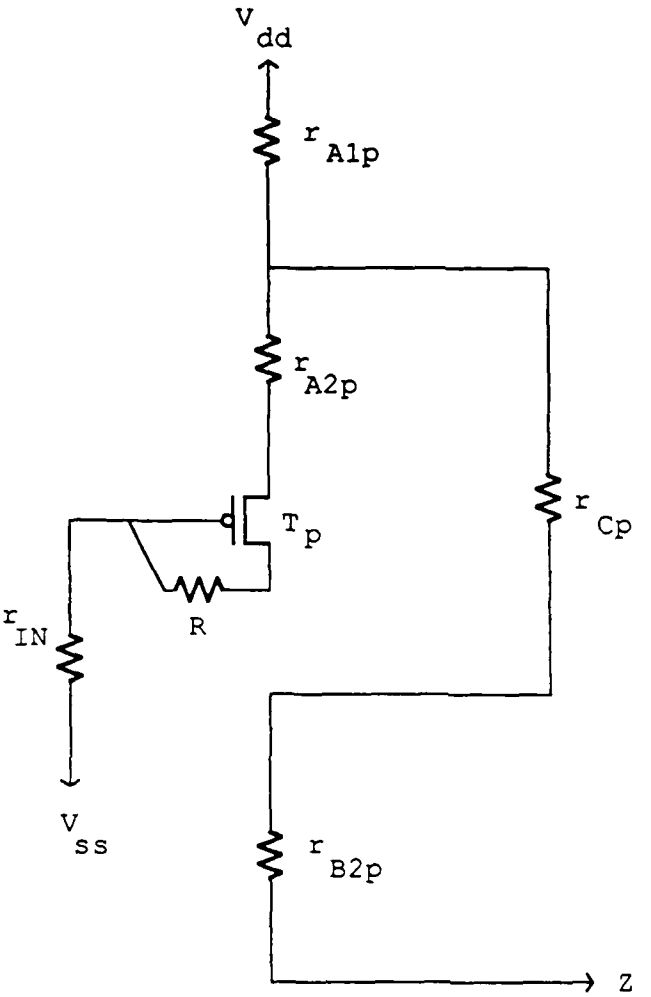


Fig 39. CIRCUIT FOR CASE IV (a) (i)

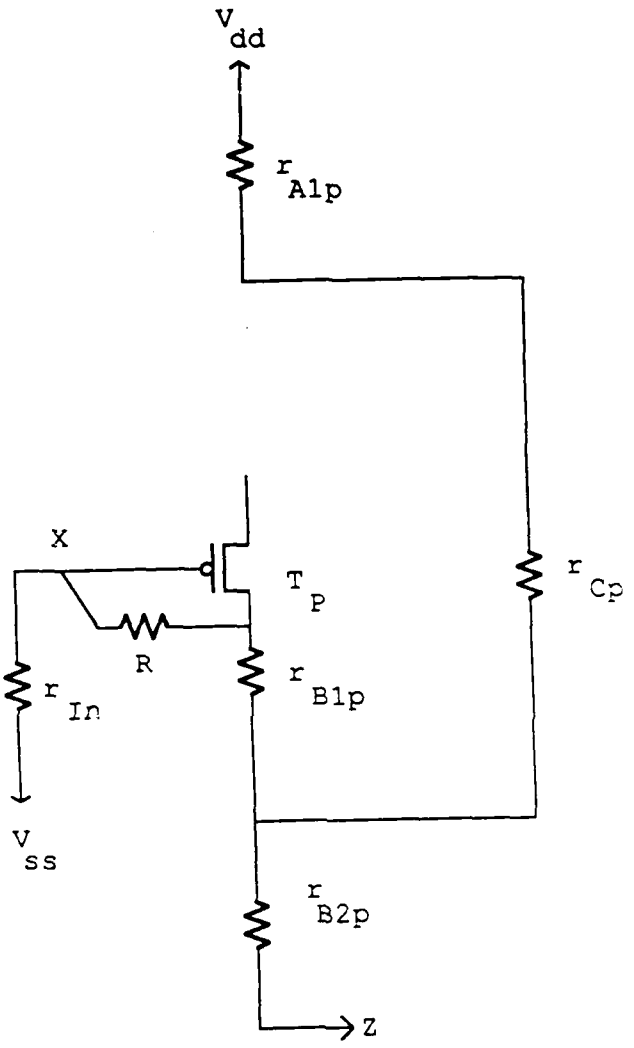


Fig 40. CIRCUIT FOR CASE IV (a) (ii-1)

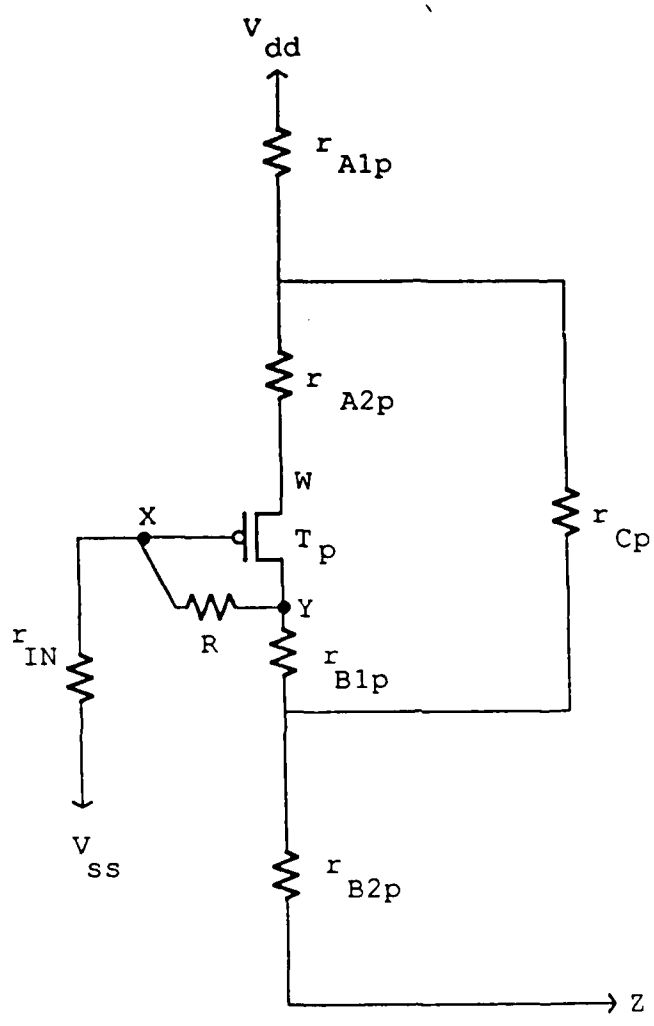


Fig 41. CIRCUIT FOR CASE IV (a) (ii - 2)

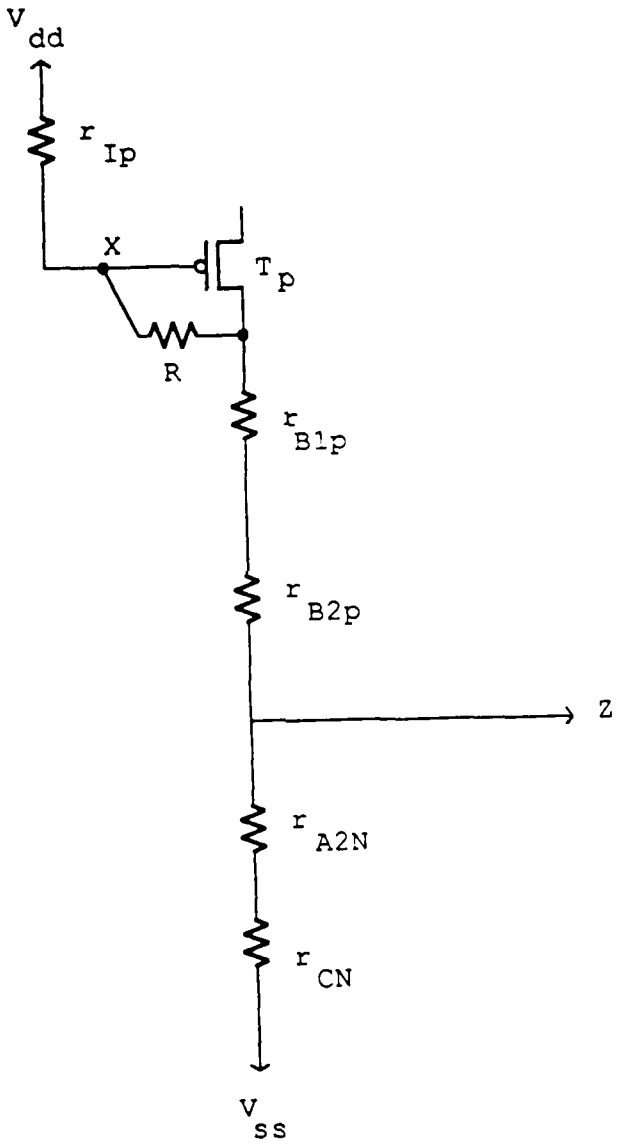


Fig 42. CIRCUIT FOR CASE III (a) (iii -1)

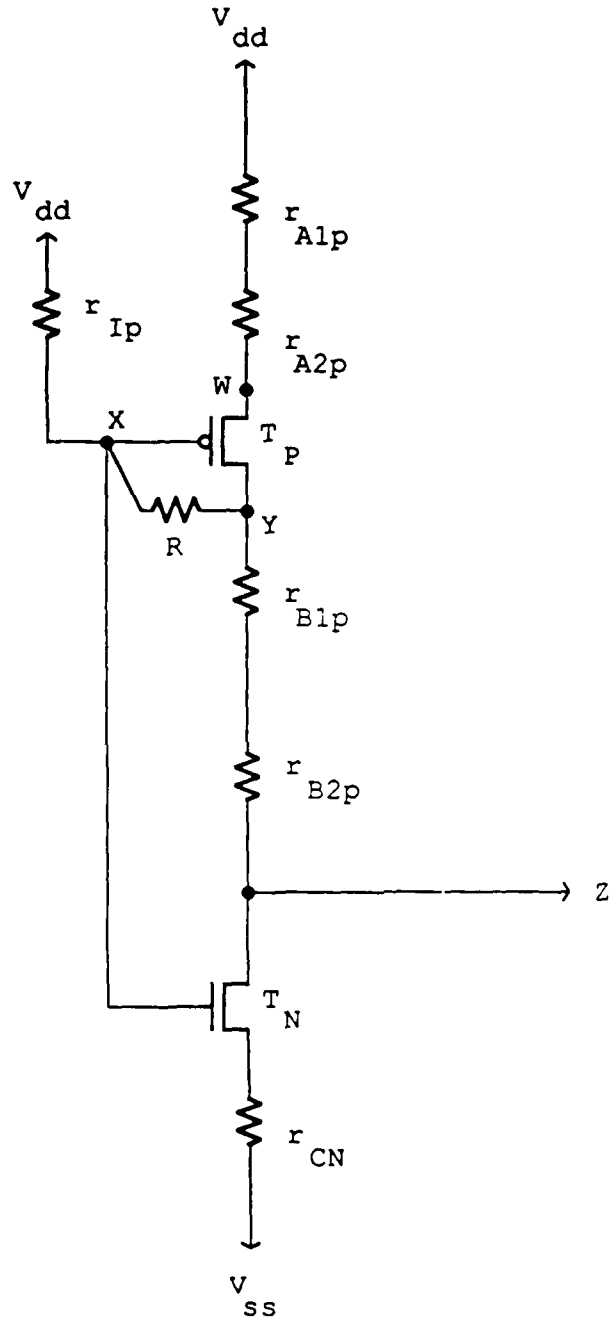


Fig 43. CIRCUIT FOR CASE IV (a) (iii -2) WHEN OUTPUT OF GATE DRIVING X IS HIGH

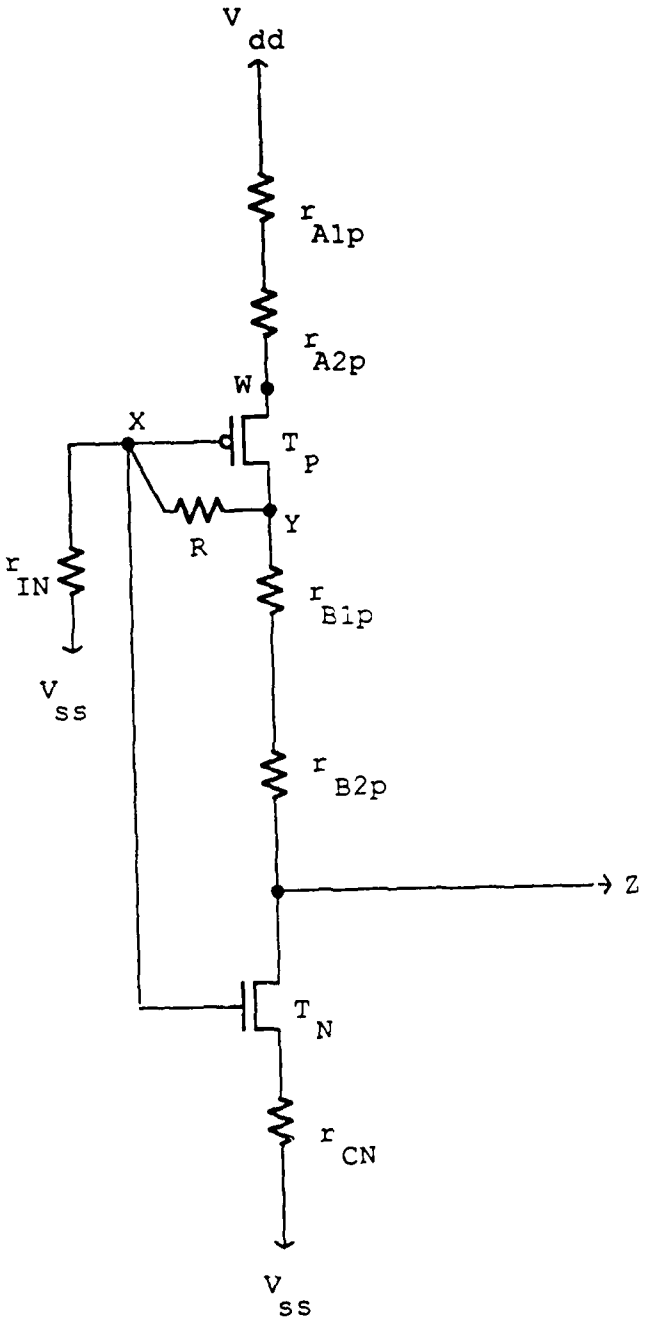


Fig 44. CIRCUIT FOR CASE IV (a) (iii -2) WHEN OUTPUT OF GATE DRIVING X IS LOW

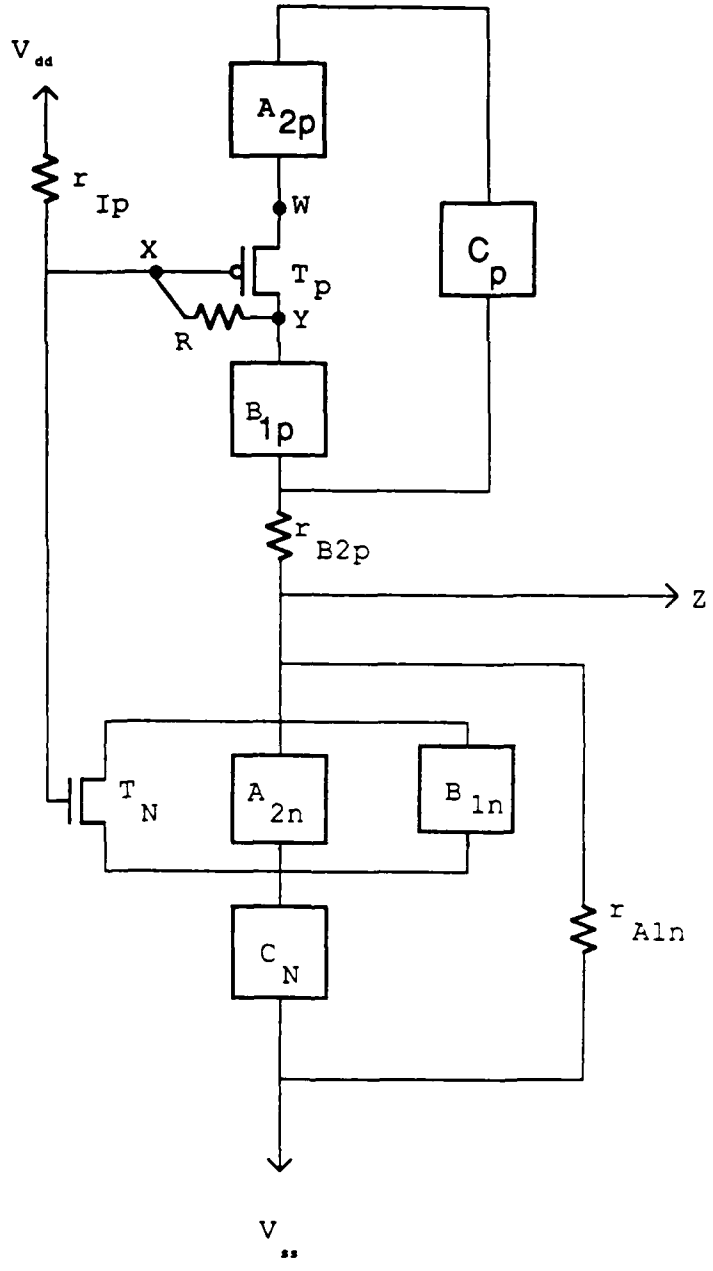


Fig 45. CIRCUIT FOR CASE IV (b) WITH CLOSED PATH IN A_{1n} AND OUTPUT OF GATE DRIVING X IS HIGH.

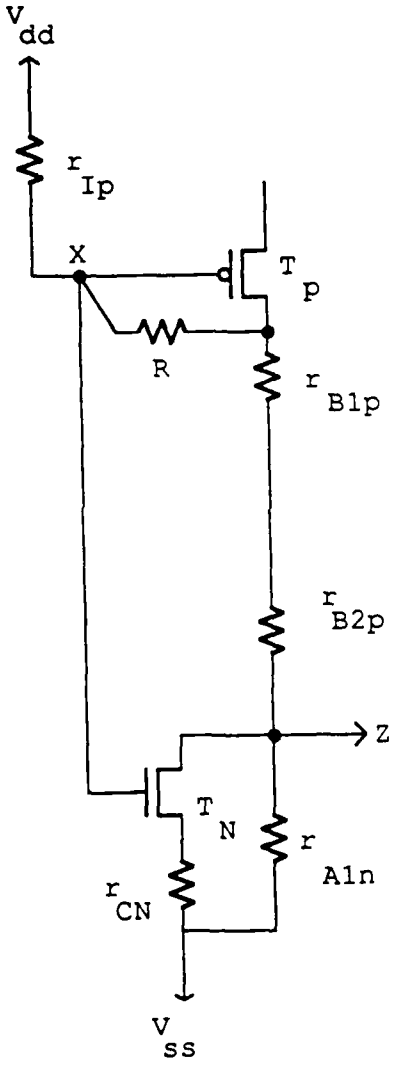


Fig 46. CIRCUIT FOR CASE IV (b) (i)

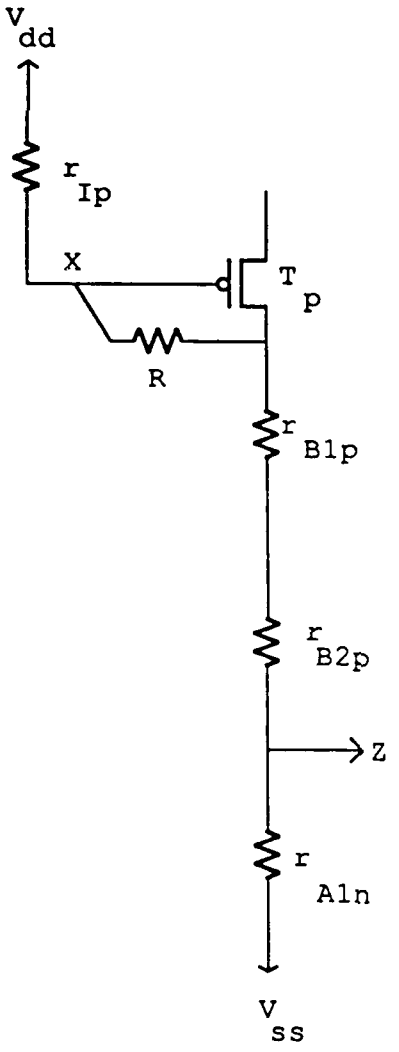


Fig 47. CIRCUIT FOR CASE IV (b) (ii -1)

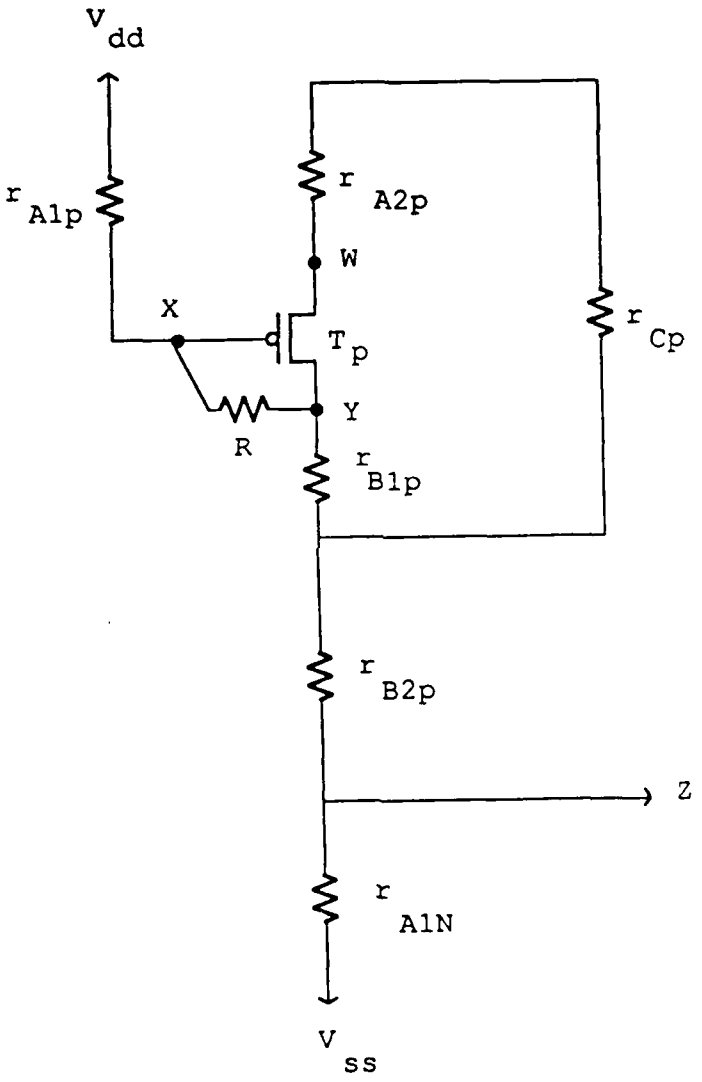


Fig 48. CIRCUIT FOR CASE IV (b) (ii - 2)

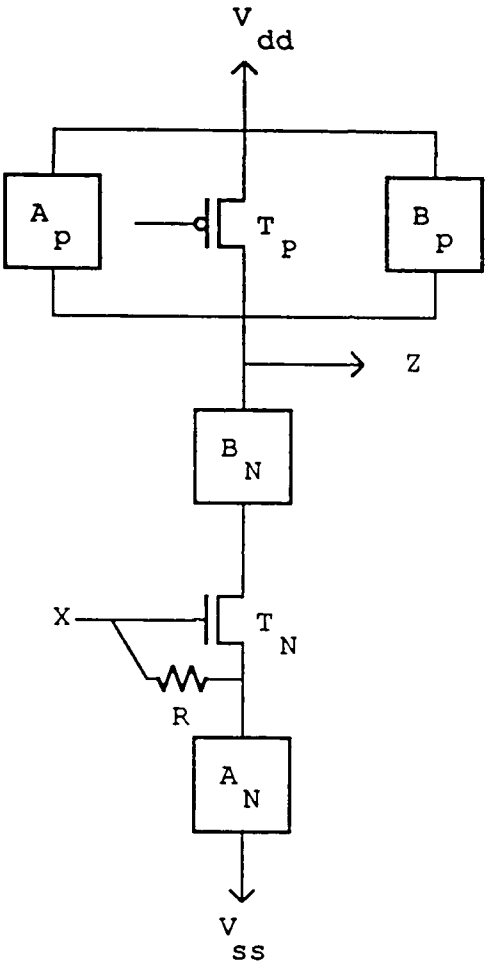


FIGURE 49. GENERAL CIRCUIT FOR CASE V

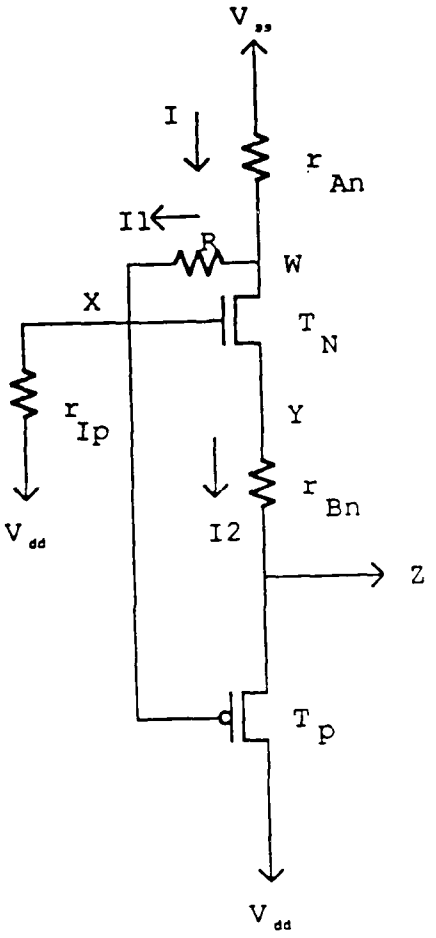


Fig 50. CIRCUIT FOR CASE V(i)

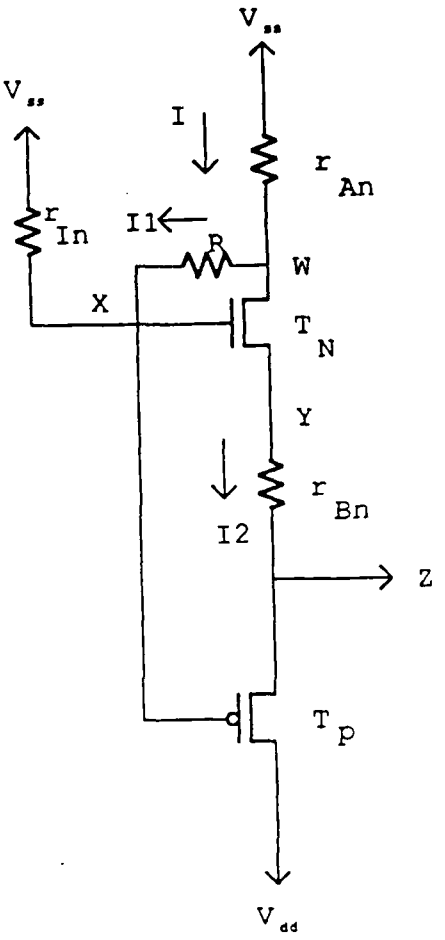


Fig 51. CIRCUIT FOR CASE V(ii)

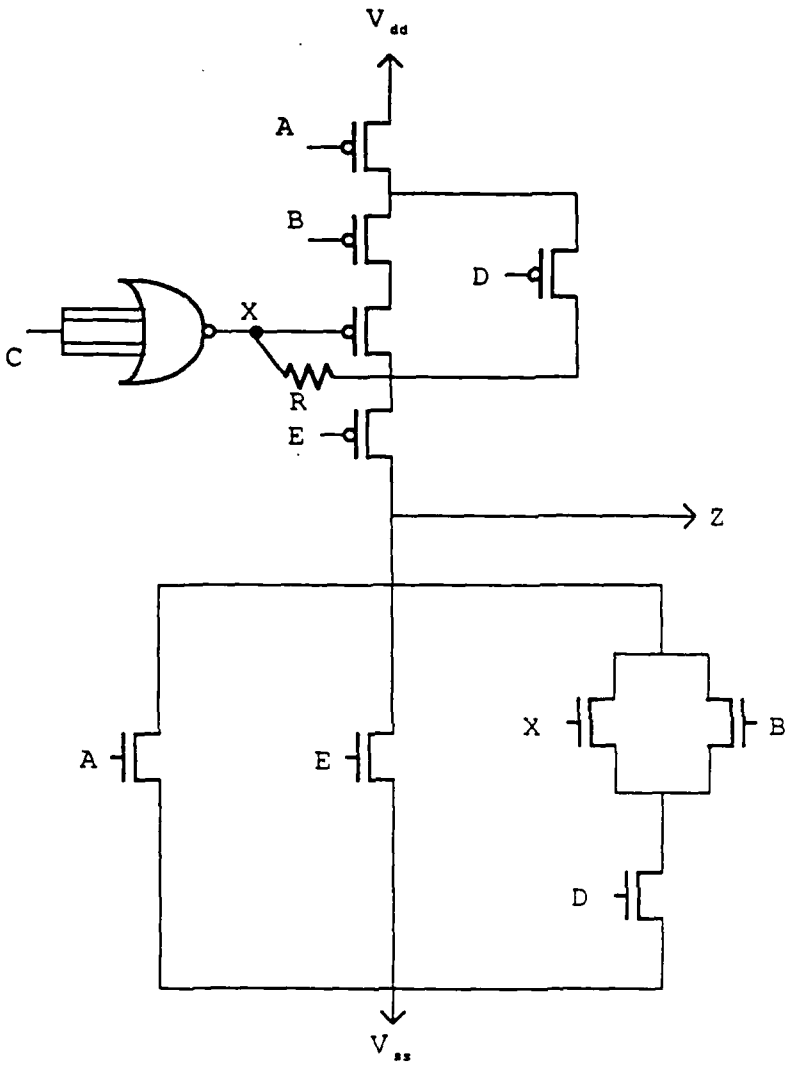


Fig 52. EXAMPLE FOR CASE IV (a) (ii -1) WHERE

P (= ABCDE = 01100) IS A TEST

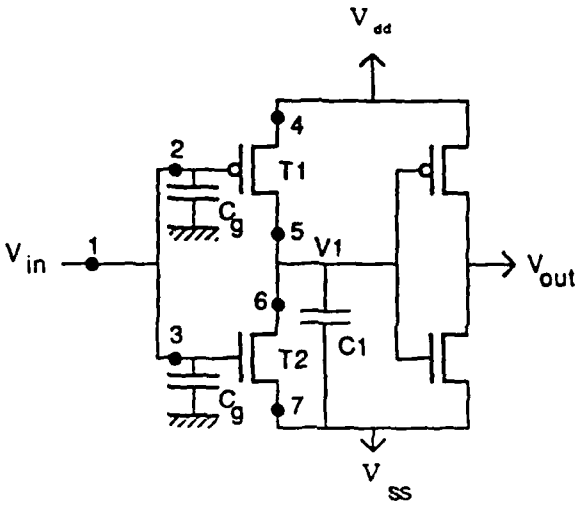


FIGURE 53.

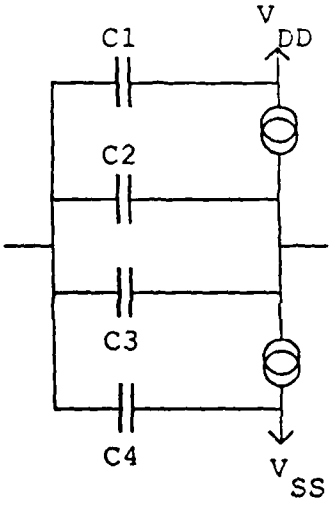


FIGURE 54(a). SIMPLIFIED MODEL FOR A CMOS INVERTER.

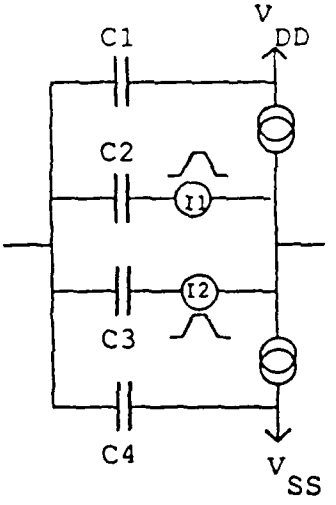


FIGURE 54(b). POSSIBLE MODEL FOR REPRESENTING THE EFFECT OF ALPHA PARTICLE RADIATION IN A INVERTER

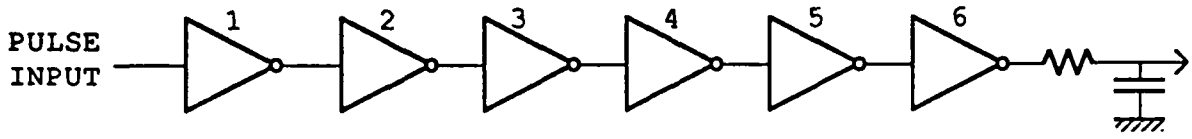
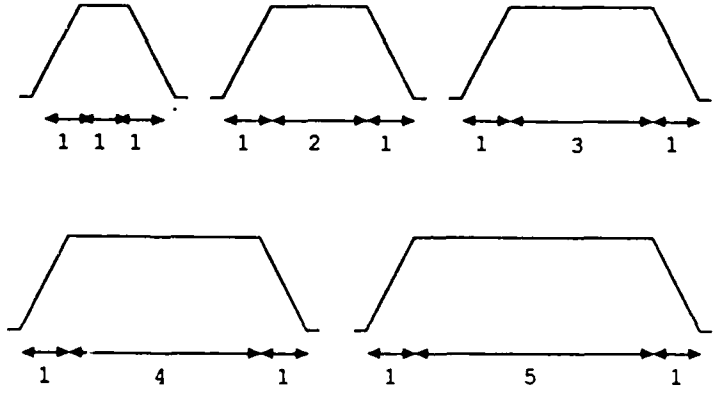


FIGURE 55.



ALL VALUES ARE IN NANOSECONDS.

FIGURE 56.

INPUT PULSE WIDTH	PULSE WIDTH AT 3.2 VOLTS.		
	V(2)	V(4)	V(6)
1ns	1.5ns	2 ns	2 ns
2ns	2.5ns	2 ns	3 ns
3ns	3 ns	3 ns	4 ns
4ns	4 ns	3.5ns	4 ns
5ns	5 ns	5 ns	5.5ns

FIGURE 57.

SECTION 7

REFERENCES

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