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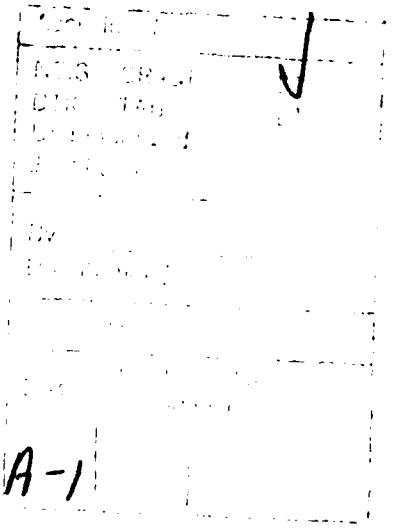

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1.0 INTRODUCTION

This report describes the results of a Phase I SBIR program entitled "Deposition of InP on Si substrates for Monolithic Integration of Advanced Electronics;" the basic objective of this project was the demonstration of the feasibility of growing high-quality InP layers on Si substrates by the metalorganic chemical vapor deposition (MOCVD) process.

1.1 Background

Recently, the epitaxial growth of III-V compounds on Si has been attracting strong interest. Some reasons for this are that Si is low cost and light weight, has high mechanical strength, excellent crystalline quality and high thermal conductivity and is available as large area substrates. The last and probably most significant reason for growing III-V semiconductors on Si is for monolithic integration of III-V and Si devices, thus combining the high speed and/or optical communication capabilities of III-V's with the sophistication of Si VLSI technology.

Spire is proposing the epitaxial growth of InP on Si substrates for applications as discussed above.

1.1.1 Why InP?

The importance of InP as a semiconductor is based on a number of its material properties. Some of the more important ones are listed below:

(1) High Peak Velocity of Electrons - The peak (or saturated-drift) velocity of electrons in InP is higher than that of GaAs (2.5×10^7 cm/sec versus 2.2×10^7 cm/sec); this makes InP an excellent choice for transferred-electron devices, such as Gunn diodes, used as very high frequency (millimeter wave) oscillators and amplifiers. Also important is the fact that InP typically has a relatively low noise figure at high frequency.

(2) Radiation Hardness - This is an important feature for any devices to be utilized in the SDI program. The radiation resistance of InP has been demonstrated (in terms of solar cell experiments) to be quite superior to that of either GaAs or Si.[1,2] In fact, photovoltaic p/n junction devices irradiated by 1 MeV electrons have been shown to almost totally recover their electrical performance by annealing at room temperature.[3]

(2) Low cost - Si substrates are approximately 100 times less expensive than InP;

(3) Light weight - The density of Si (2.3 gm/cm^3) is about half that of InP (4.7 gm/cm^3);

(4) Mechanical Strength - Si wafers are much more rugged than InP. An indication of this is the Knoop microhardness values, which are 1150 and 535 kg/mm respectively for Si and InP;

(5) Thermal Conductivity - The thermal conductivity of Si (1.68 W/cm°K) is more than twice that of InP (0.7 W/cm°K);

(6) Monolithic Integration - The epitaxial growth of InP on silicon would allow for the monolithic integration of the optoelectronic and microwave capabilities of InP with the high-speed circuitry of Si VLSI technology.

1.3.2 Advantages of MOCVD

The use of MOCVD is a good choice for the program for the reasons listed below:

- Proven material quality - InP epitaxial layers of excellent electrical quality have been grown by the MOCVD process. Undoped films with 77°K mobilities of 300,000 $cm^2/V\text{-}sec$ at a background impurity level of 3×10^{13} cm^{-3} have been achieved.[11] Excellent InP/GaInAsP lasers have also been demonstrated with MOCVD-grown layers.[8]

- Volume-amenable process - MOCVD is the technique of choice for the large-scale production of many III-V devices. Reactors up to 1000 cm^2 per batch are currently being used in a production mode for GaAs devices.[12] Reactor sizes up to 1800 cm^2 per batch have been reported[13] and much on-going research in terms of material quality and reactor design continue to make MOCVD a rapidly advancing field.

1.4 Literature Review

This section reviews the literature concerning the growth of InP on Si; all these reports utilize the MOCVD technique. In addition, a brief review of the growth of InP on GaAs and GaAs on Si is also presented.

The growth of single crystal InP on Si was first reported in 1986 by researchers at NTT in Japan;[14] since then a few other reports have appeared in the literature.[15-22] The NTT group has succeeded in growing InP films directly on Si substrates and in fabricating solar cells (approximately 3% efficient) from these wafers.[17] These 5-μm-thick InP-on-Si films have been characterized by X-ray rocking curves to have a

2.0 SUMMARY OF PHASE I RESULTS

The goal of the Phase I effort was to establish a basic growth process for depositing single-crystal InP films on Si substrates; our experience in growing high-quality GaAs-on-Si and GaP-on-Si structures was to provide a background to guide the experiments.

2.1 Experimental Procedures

Depositions were carried out by atmospheric-pressure MOCVD in a SPI-MO CVD 450 reactor; the sources chemicals used were trimethylindium (TMIn) and phosphine (PH_3) and the main carrier gas was H_2. The basic GaAs-on-Si growth procedure developed in our laboratory consists of three steps:

1. A high-temperature bakeout in H_2 for 30 minutes at approximately 1000°C
2. A low-temperature nucleation step in which approximately 200 Å of GaAs is deposited at 400°C
3. A film growth step in which GaAs is grown at "normal" MOCVD conditions utilizing a growth temperature of approximtely 675°C

Starting from these basic guidelines, a similar process for InP-on-Si was attempted, with the major variables occurring in Step 2, the nucleation procedure, which is really the most critical step since the surface-oxide-removal procedure (Step 1) had been previously optimized for other heteroepitaxy-on-Si projects. Several different types of nucleation layers/procedures were attempted. These included different materials (InP, In, or P), different thicknesses, and different temperatures; a brief summary of these runs is listed in Table 2-1. In all cases, our standard H_2 bakeout procedure was performed (Step 1), and our standard InP growth conditions (600°C, 1 μm/hr) were used to grow a thick (1-4 μm) InP layer on top for evaluation. The last two lines of the table are based on conditions used at Spire for deposition-on-Si processes other than the three-step method described above, but which have also shown to be useful. These processes include growing GaAs-on-Si using a nucleation step of pure Ga deposited at the growth temperature of typical GaAs (~650°C), and growing GaP-on-Si by a process which employs a first step of flowing PH_3 over the Si wafer at a temperature of 950°C.

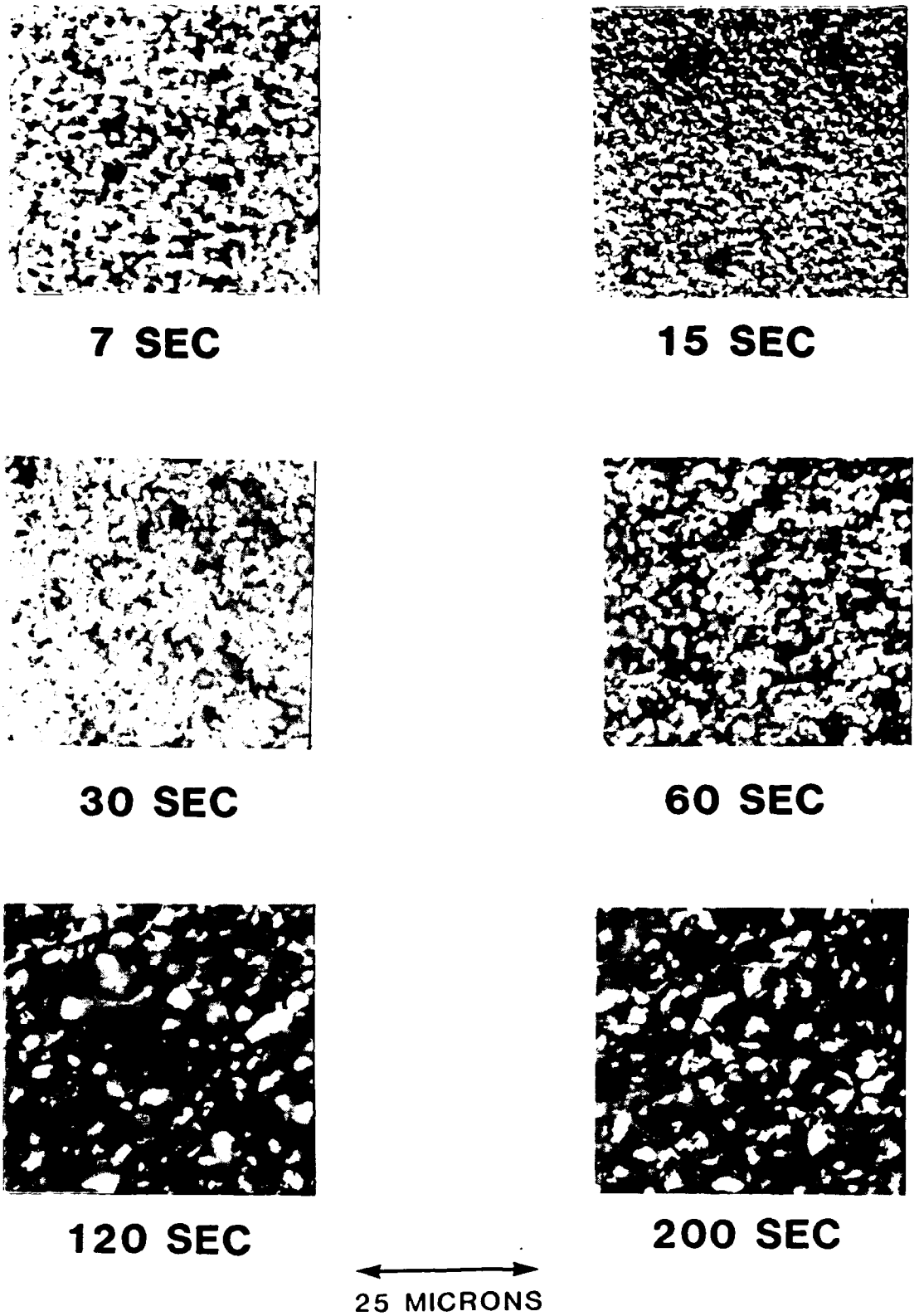


FIGURE 2-1. NOMARSKI MICROGRAPHS OF InP ON (100) Si WITH LOW TEMPERATURE InP NUCLEATION. Times shown are for the deposition of the low-temperature layer.

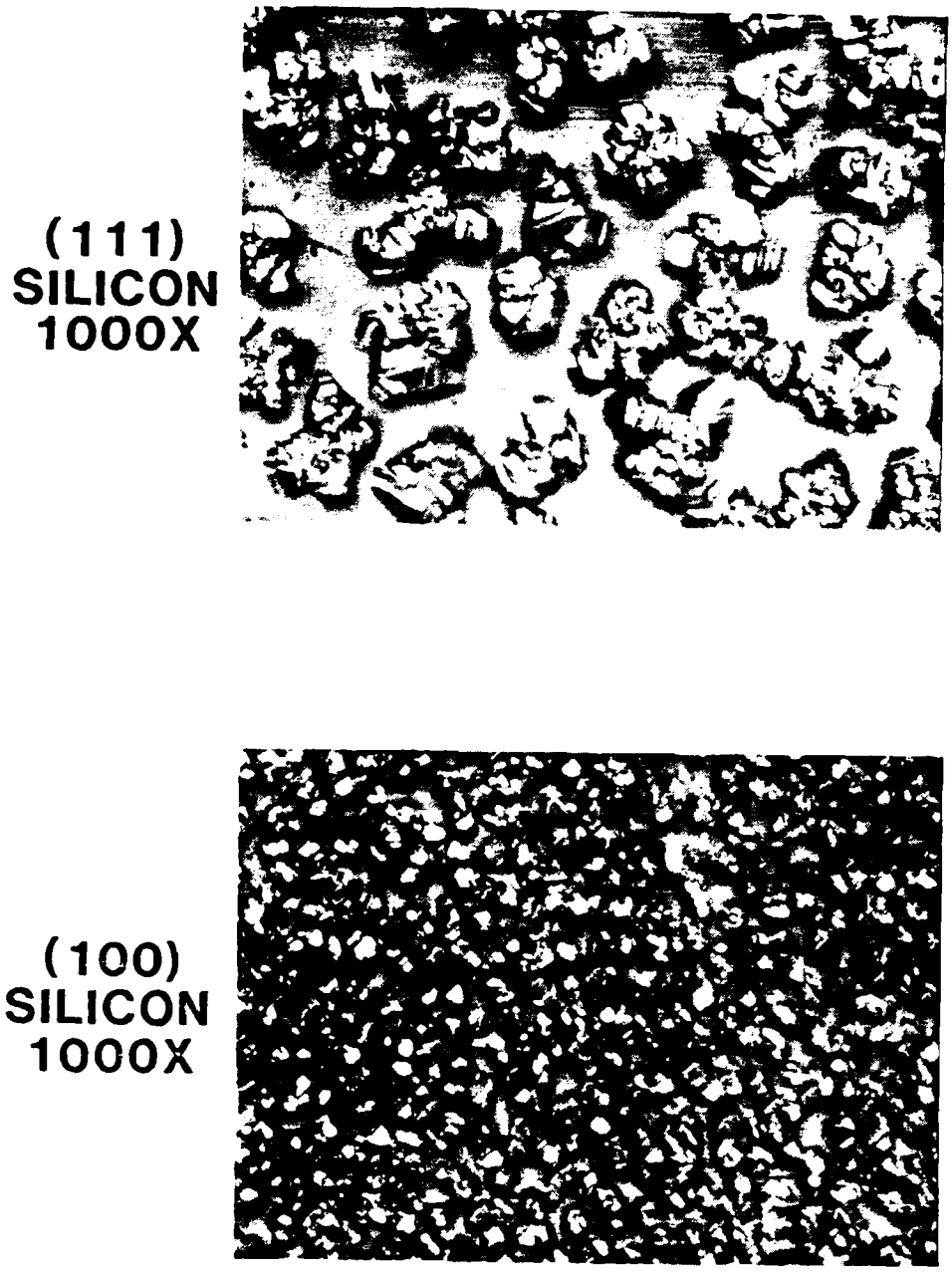
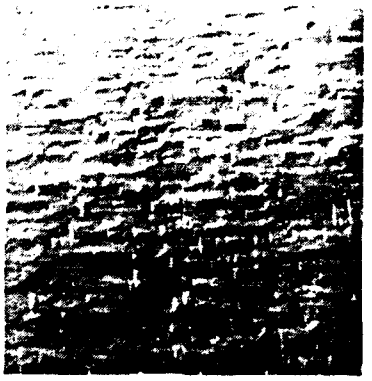


FIGURE 2-3. NOMARSKI MICROGRAPHS OF InP ON Si BY THE SINGLE-STEP PROCESS AS A FUNCTION OF SUBSTRATE ORIENTATION. The InP growth is at 600°C; the (100) substrate is actually 2° off in the (011) direction.

1000X

2μm InP/Si WITH 1μm
GaAs INTERMEDIATE LAYER



1000X

3μm GaAs/Si

25 MICRONS

FIGURE 2-5. NOMARSKI MICROGRAPHS COMPARING SURFACE MORPHOLOGIES OF InP-GaAs-Si AND GaAs-Si SAMPLES. Both samples appear quite specular to the unaided eye.

TABLE 2-2. DOUBLE-CRYSTAL X-RAY ROCKING CURVE DATA FROM AT&T BELL LABS

Sample	Structure	FWHM (arc-sec) InP	GaAs
414-3	4μ InP-4μ GaAs-Si	440	320
414-2	4μ InP-1μ GaAs-Si	420	470
414-4	4μ InP-0.1μ GaAs-Si	400	1000
405-2	1μ InP-4μ GaAs-Si	1160	330
405-1	1μ InP-1μ GaAs-Si	1380	560
405-3	1μ InP-0.1μ GaAs-Si	1420	1770
412-1	1μ InP-Si	5100	
414-1	4μ InP-GaAs	260	26
405-4	1μ InP-InP	11.5	

Data obtained from AT&T Bell Labs, Murray Hill, NJ, through the courtesy of Drs. A. Macrander and S.J. Pearton.

Another point to note in the data of Table 2-2 is that for both the 4μm-thick and 1-μm-thick InP films on GaAs-on-Si, the thickness of the GaAs layer appears to have only a small effect on the quality of the InP layer.

As mentioned above, a few samples were also examined by double-crystal X-ray rocking curve analysis at SUNY at Buffalo by Dr. Wie. These data are shown in Table 2-3. The GaAs-on-Si sample has a small FWHM (180 arc-sec) in this case because it was grown by our more optimized thermal-cycle-growth process[31] which had not been incorporated into the other samples. The InP-on-GaAs FWHM is larger than that measured at AT&T because the InP layer is thinner; for the InP-GaAs-Si sample, the GaAs FWHM agrees well with the data from AT&T, which was taken on another piece of the same wafer, while there is an unexplained discrepancy in the InP value.

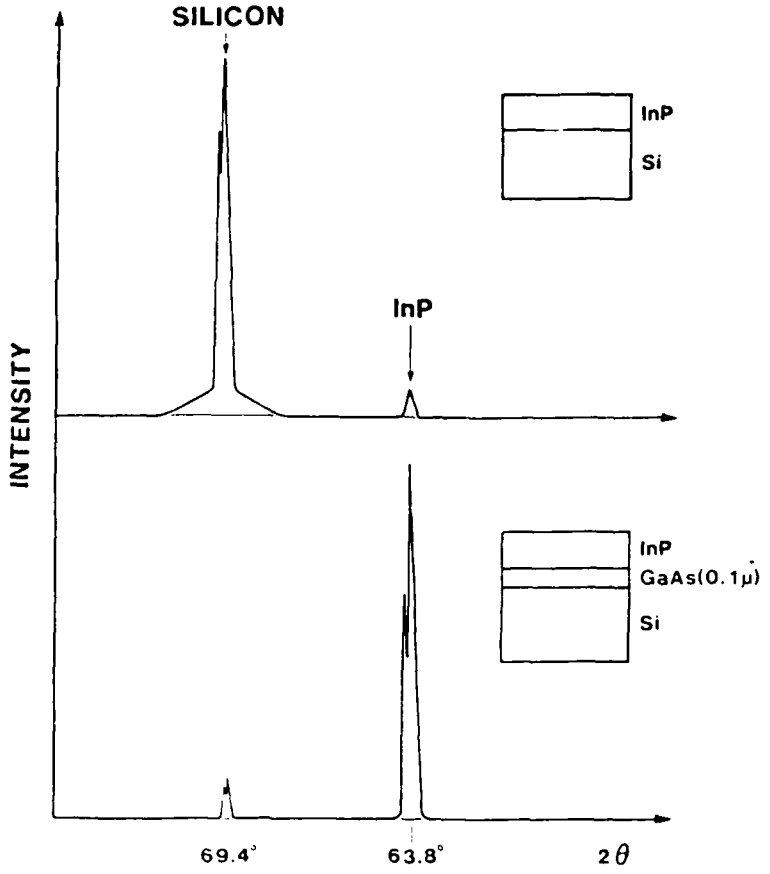


FIGURE 2-7. X-RAY DIFFRACTOMETER SCANS OF InP ON Si WITH AND WITHOUT A THIN GaAs BUFFER LAYER.

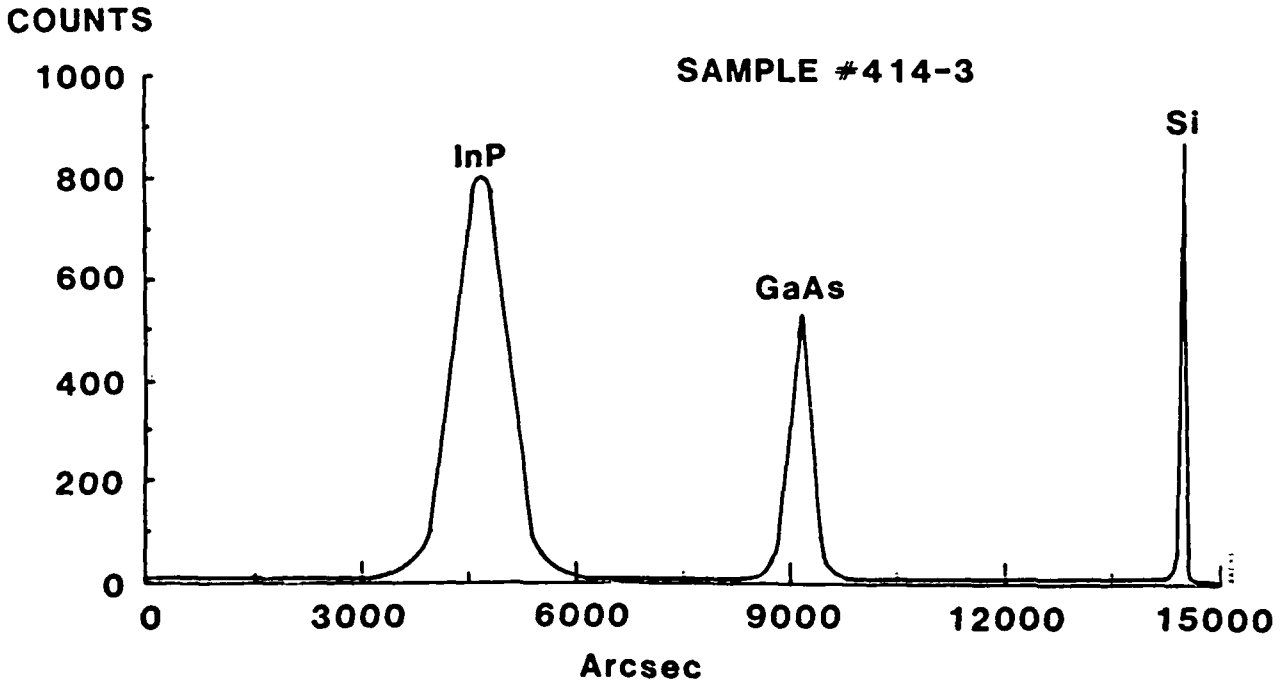


FIGURE 2-8. DOUBLE-CRYSTAL X-RAY ROCKING CURVE OF InP-GaAs-Si SAMPLE #414-3. Data courtesy of AT&T Bell Laboratories.

TABLE 2.3 DOUBLE-CRYSTAL X-RAY ROCKING CURVE DATA FROM SUNY AT BUFFALO

Sample	Structure	FWHM (arc-sec) InP	GaAs	Comments
1326-1	2.3 μ GaAs-Si		180	Thermal Cycle Growth
410-1	2.0 μ InP-GaAs	482		
414-2	4.0 μ InP-1 μ GaAs-Si	576	475	

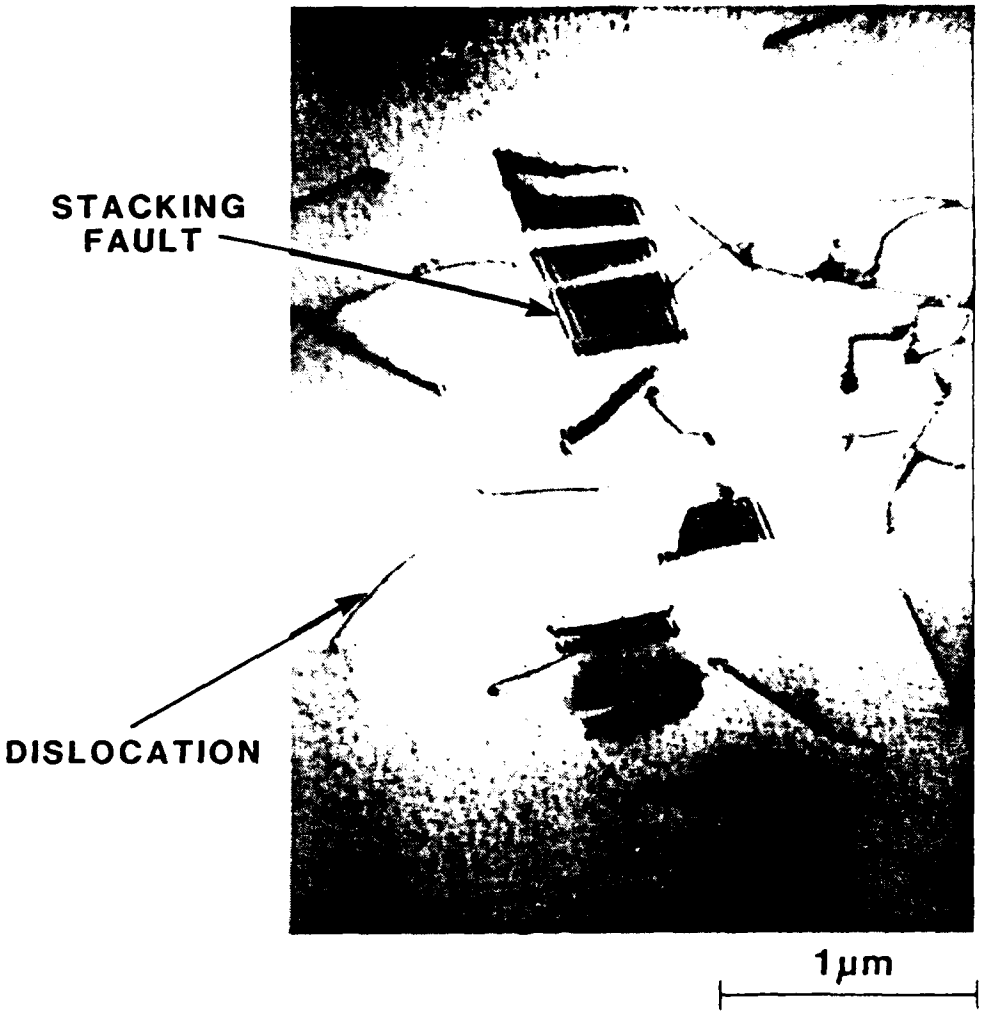
Data obtained from Dr. Chu Wie at SUNY at Buffalo, NY.

2.2.4 Transmission Electron Microscopy (TEM)

Four InP films were analyzed by TEM at the Solar Energy Research Institute (SERI) through the courtesy of Dr. M.M. Al-Jassim. The results are shown in Table 2-4. From these results, we see that a GaAs thickness of 1 μm appears optimal, and that the defect density of the InP films is identical (within experimental error) to our standard unannealed GaAs-on-Si films (3×10^8 cm^{-2}). A planview TEM of an InP/GaAs/Si sample is shown in Figure 2-10 where both dislocations and stacking faults are evident. Figure 2-11 shows a cross-sectional TEM of the same sample; it is obvious in this figure that many defects in the InP layer originate at the GaAs-InP interface and are probably not caused by the existing defects in the GaAs layer. This is not surprising, since both interfaces have a lattice mismatch of approximately 4%.

TABLE 2-4. TEM RESULTS OF In-on-GaAs-on-Si SAMPLES

Sample	Thickness (μm) InP	GaAs	Dislocations (cm^{-2})	Stacking Faults (cm^{-2})	Comments
414-3	4	4	8.4×10^8	1.6×10^8	
414-2	4	1	2.9×10^8	3.6×10^7	
414-4	4	0.1	3.2×10^8	1.0×10^8	
412-1	1	0	-	-	Polycrystalline



InP THICKNESS = 4μm, GaAs THICKNESS = 1μm

FIGURE 2-10. PLANVIEW TRANSMISSION ELECTRON MICROGRAPH OF InP-GaAs-Si SAMPLE #414-2.

TABLE 2-5. ROOM TEMPERATURE PHOTOLUMINESCENCE DATA

Sample	Structure	FWHM of InP Peak (meV) UCLA	Spire	Comments
414-3	4μ InP-4μ GaAs-Si		33.7	Undoped N ~ 10^{15} cm^3
414-2	4μ InP-1μ GaAs-Si	34.4	33.7	Undoped N ~ 10^{15} cm^3
414-4	4μ InP-0.1μ GaAs-Si		30.8	Undoped N ~ 10^{15} cm^3
405-2	1μ InP-4μ GaAs-Si		69.9	Doped N ~ 10^{17} cm^3
405-1	1μ InP-1μ GaAs-Si	59.7	66.8	Doped N ~ 10^{17} cm^3
405-3	1μ InP-0.1μ GaAs-Si		66.8	Doped N ~ 10^{17} cm^3
405-4	1μ InP-InP	59.7	77.8	Doped N ~ 10^{17} cm^3

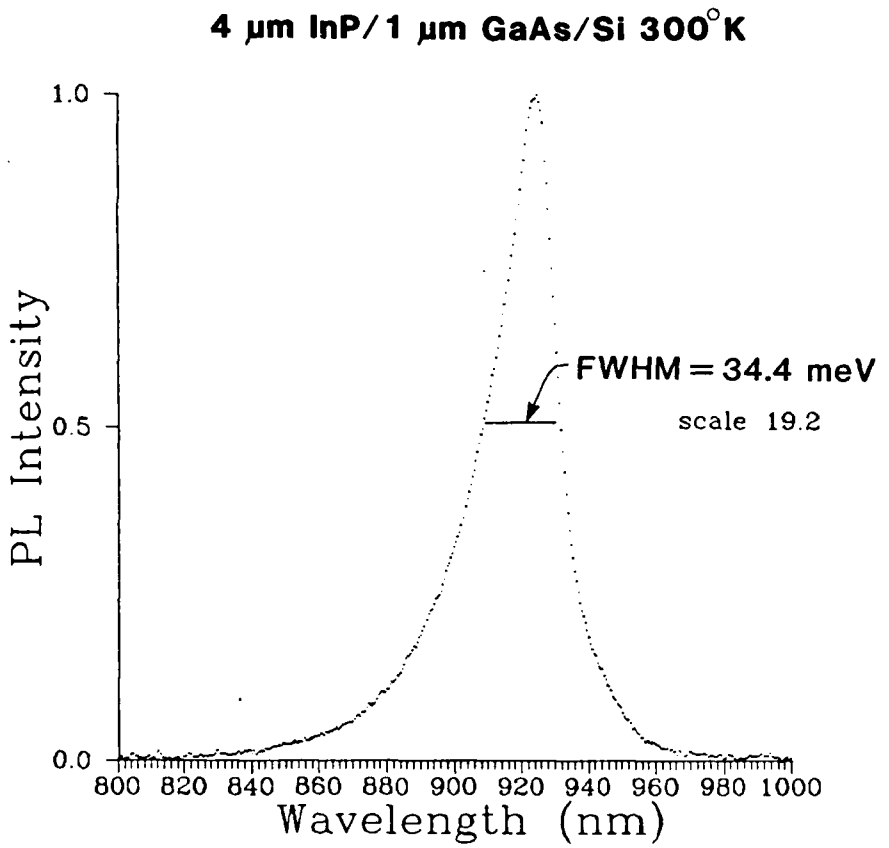


FIGURE 2-12. ROOM-TEMPERATURE PHOTOLUMINESCENCE OF InP-GaAs-Si SAMPLE. Data courtesy of UCLA.

- The InP-GaAs interface appears to generate as many dislocations as does the GaAs-Si interface.

- InP-GaAs-Si samples show reasonably good PL at room-temperature and 4.4°K and that the PL halfwidth at 300°K is fairly insensitive to the GaAs buffer thickness.

4.0 CONCLUSIONS

The Phase I effort has led us to make the following conclusions:

- The feasibility of deposition single-crystal InP-on-Si structures by MOCVD has been clearly demonstrated in this program.

- The use of a thin GaAs buffer layer facilitates the growth of high-quality, single-crystal InP overlayers on Si substrates.

- Much optimization of the heteroepitaxial structure and growth process is possible.

5.0 ACKNOWLEDGEMENTS

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- Dr. M.M. Al-Jassim for TEM studies at SERI.

- Drs. S.J. Pearton and A. Macrander for X-ray analyses at AT&T Bell Laboratories.

- Drs. N.M. Haegel an V.P. Mazzi for PL characterization at UCLA.

- Mr. V.E. Haven for MOCVD growth at Spire.

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